Novel Processes, Test Structures and Characterisation for Future Germanium Technologies

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I, Maryam Shayesteh, certify that this thesis is my own work and I have not obtained a degree in this university or elsewhere on the basis of the work submitted in this thesis.

Maryam Shayesteh

To Masoud, Ryan
& my parents

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Abstract

Since Si is struggling with fundamental limitations in aggressively scaled devices, new higher mobility materials like Ge and III-V have become of interest as potential replacements in advanced CMOS technology. However with respect to the underlying knowledge and research, these materials seem quite young, compared to Si which has more than 40 years of research behind it. Undoubtedly to be widely used in advanced CMOS devices, the process and integration of these materials has to be well established so that their high mobility benefit is not swamped by imperfect manufacturing procedures.

In this dissertation number of key bottlenecks in realization of Ge devices are investigated;

First we address the challenge of the formation of low resistivity contacts on n-type Ge, comparing conventional and advanced rapid thermal annealing (RTA) and laser thermal annealing (LTA) techniques respectively. LTA appears to be a feasible approach for realization of low resistivity contacts with an incredibly sharp germanide-substrate interface and contact resistivity in the order of 10^{-7} $\Omega.cm^2$. The thermal stability of these contacts has to be carefully addressed.

Further obstacles were also studied from a dopant activation level and leakage current point of view, where the influence of RTA and LTA on dopant activation and leakage current suppression in n+/p Ge junction were compared. Providing very high active carrier concentration > 10^{20} cm^{-3}, LTA resulted in higher leakage current compared to RTA which provided lower carrier concentration ~ 10^{19} cm^{-3}. This is an indication of a trade-off between high activation level and junction leakage current. Obtaining high I_{ON}/I_{OFF} ratio ~ 10^7 was the main achievement of this study, which to the best of our knowledge is the best reported value for n-type Ge so far.

The final part of this PhD was devoted to studies on Ge thin body structures. Simulations were carried out to investigate how target sputtering, dose retention, and damage formation is generated in thin-body semiconductors by means of energetic ion impacts and how they are dependent on the target physical material properties. Solid phase epitaxy studies in wide and thin Ge fins confirmed the

formation of twin boundary defects and random nucleation growth, like in Si, but here 600 °C annealing temperature was found to be effective to reduce these defects. Finally, a non-destructive doping technique was successfully implemented to dope Ge nanowires, where nanowire resistivity was reduced by 5 orders of magnitude using PH_3 based in-diffusion process.

List of Publications

Based on results presented in this thesis:

[1] **M. Shayesteh**, C. L. L. M. Daunt, D. O'Connell, V. Djara, M. White, B. Long, and R. Duffy, "NiGe contacts and junction architectures for P and As doped germanium devices," *IEEE Transactions on Electron Devices*, vol. 58, pp. 3801-3807, 2011.

[2] **M. Shayesteh**, C. L. M. Daunt, D. O'Connell, V. Djara, M. White, B. Long, and R. Duffy, "N-type doped germanium contact resistance extraction and evaluation for advanced devices," in *European Solid-State Device Research Conference*, 2011, pp. 235-238.

[3] **M. Shayesteh**, V. Djara, M. Schmidt, M. White, A. M. Kelleher, and R. Duffy, "Fluorine implantation in germanium for dopant diffusion control," in *AIP Conference Proceedings*, 2012, pp. 115-118.

[4] **M. Shayesteh**, R. Duffy, B. McCarthy, A. Blake, M. White, J. Scully, R. Yu, V. Djara, M. Schmidt, N. Petkov, and A. M. Kelleher, "Germanium fin structure optimization for future MugFET and FinFET applications," in *ECS Transactions*, 2011, pp. 27-34.

[5] **M. Shayesteh**, K. Huet, I. Toque-Tresonne, R. Negru, C. L. M. Daunt, N. Kelly, D. O'Connell, R. Yu, V. Djara, P. B. Carolan, N. Petkov, and R. Duffy, "Atomically flat low-resistive germanide contacts formed by laser thermal anneal," *IEEE Transactions on Electron Devices*, vol. 60, pp. 2178-2185, 2013.

[6] **M. Shayesteh**, D. O' Connell, F. Gity, P. Murphy, R. Yu, K. Huet, I. Toqué-Tresonne, F. Cristiano, S. Boninelli, H. H. Henrichsen, P. F. Nielsen, D. H. Petersen, and R. Duffy " Optimised Laser Thermal Annealing on Germanium for Reduced Access Resistance and Low Leakage Current ", *IEEE Transactions on Electron Devices, under publication.*

[7] **M. Shayesteh**, D. O'Connell, F. Gity, F. Murphy-Armando, R. Yu, K. Huet, I. Toque-Tresonne, F. Cristiano, S. Boninelli, H. H. Henrichsen, D. H. Petersen, P. F. Nielsen, and R. Duffy, "Laser thermal annealing of Ge, optimized for highly activated dopants and diode ION/IOFF ratios," *20th International Conference on Ion Implantation Technology (IIT), 2014*, 2014.

[8] R. Duffy and **M. Shayesteh**, "FinFET doping; material science, metrology, and process modeling studies for optimized device performance," in *AIP Conference Proceedings*, 2010, pp. 17-22.

[9] R. Duffy and **M. Shayesteh**, "Germanium doping, contacts, and thin-body structures," in *ECS Transactions*, 2012, pp. 189-201.

[10] R. Duffy and **M. Shayesteh**, "Novel processing for access resistance reduction in Germanium devices," in *2014 International Workshop on Junction Technology, IWJT 2014*, 2014, pp. 155-160.

[11] R. Duffy, **M. Shayesteh**, I. Kazadojev, and R. Yu, "Germanium doping challenges," in *Extended Abstracts of the 13th International Workshop on Junction Technology 2013, IWJT 2013*, 2013, pp. 16-21.

[12] R. Duffy, **M. Shayesteh**, B. McCarthy, A. Blake, M. White, J. Scully, R. Yu, A. M. Kelleher, M. Schmidt, N. Petkov, L. Pelaz, and L. A. Marqués, "The curious case of thin-body Ge crystallization," *Applied Physics Letters*, vol. 99, 2011.

[13] R. Duffy, **M. Shayesteh**, M. White, J. Kearney, and A. M. Kelleher, "The formation, stability, and suitability of n-type junctions in germanium formed by solid phase epitaxial recrystallization," *Applied Physics Letters*, vol. 96, 2010.

[14] K. Huet, **M. Shayesteh**, I. Toqué-Tresonne, R. Negru, C. L. M. Daunt, N. Kelly, D. O'Connell, R. Yu, V. Djara, P. Carolan, N. Petkov, and R. Duffy, "Laser thermal anneal formation of atomically-flat low-resistive germanide contacts," *Physica Status Solidi (C) Current Topics in Solid State Physics*, vol. 11, pp. 169-173, 2014.

[15] R. Duffy, **M. Shayesteh,** K. Thomas, E. Pelucchi, R. Yu, A. Gangnaik, Y. M. Georgiev, P. Carolan, N. Petkov, B. Long, J. D. Holmes, "Access resistance reduction in Ge nanowires and substrates based on non-destructive gas-source dopant in-diffusion," *Journal of Materials Chemistry C*, vol. 2, pp. 9248-9257, 2014.

Other contributions that are not discussed in the thesis:

[1] B. Long, G. Alessio Verni, J. O'Connell, J. Holmes, **M. Shayesteh**, D. O'Connell, and R. Duffy, "Molecular Layer Doping: Non-destructive doping of silicon and germanium," in *20th International Conference on Ion Implantation Technology (IIT), 2014*, 2014, pp. 1-4.

[2] B. Long, R. Duffy, G. Alessio-Verni, J. O'Connell, **M. Shayesteh**, A. Gangnaik, Y. M. Georgiev, P. Carolan, D. O'Connell, K. J. Kuhn, S. B. Clendenning and J. D. Holmes, "Conformal and non-destructive doping of germanium nanowires," Journal of Materials Chemistry C, Ready for submission

[3] R. Yu, S. Das, I. Ferain, P. Razavi, **M. Shayesteh**, A. Kranti, R. Duffy, and J. P. Colinge, "Device design and estimated performance for p-type junctionless transistors on bulk germanium substrates," *IEEE Transactions on Electron Devices*, vol. 59, pp. 2308-2313, 2012.

[4] R. Yu, Y. M. Georgiev, S. Das, R. G. Hobbs, I. M. Povey, N. Petkov, **M. Shayesteh**, D. O'Connell, J. D. Holmes, and R. Duffy, "Junctionless nanowire transistor fabricated with high mobility Ge channel," *Physica Status Solidi - Rapid Research Letters*, vol. 8, pp. 65-68, 2014.

[5] R. Yu, A. N. Nazarov, V. S. Lysenko, S. Das, I. Ferain, P. Razavi, **M. Shayesteh**, A. Kranti, R. Duffy, and J. P. Colinge, "Impact ionization induced dynamic floating body effect in junctionless transistors," *Solid-State Electronics*, vol. 90, pp. 28-33, 2013.

Chapter 1

Introduction

1.1 Motivation and background

The idea of making a transistor goes back to 1925 when Julius Edgar Lilienfeld invented a field effect transistor (FET) [1]. He only filed a patent on his work but later on it was proved that his device was operational [2].

In 1947 a new working transistor was made from Ge semiconductor. A couple of years later another transistor made from Si was introduced, which was more interesting than Ge transistor due to the inexpensive, abundant, Si substrate and its superb stable native oxide. The amorphous SiO_2 has a large energy gap of approximately 9 eV, and a dielectric strength which is sufficient for supporting electric field strengths of several megavolts/cm, (10^6 V/cm) which is especially critical for metal-oxide-semiconductor field effect transistor (MOSFET) operation [3]. Since then Si has been the main material used in semiconductor industry.

In 1965 Gordon Moore, considering the fabrication cost and technological capabilities in that time, speculated that the number of transistors on a single integrated circuit could be doubled per year [4]. The idea which was called "Moore's Law" was later on amended to double transistors on a chip every 2 years [5].

For more than four decades this guideline has been the driving force for endless innovations in design and fabrication of transistors and integrated circuits which appeared to be smaller in size and more densely packed at each technology node, providing incredible sophisticated functionalities.

Apparently the path has never been easy since each new generation of electronic devices would impose challenges from processing and fabrication to circuit integration, test and reliability issues [6].

According to Dennard *et al.* continuous device scaling while maintaining the same electric field in the device needs a transformation of the transistor dimensions

as well as the voltage and doping by a factor of α [7]. This reduction includes the vertical as well as horizontal dimensions of the device. The applied voltage to the device should also be reduced by α. On the other hand the substrate doping concentration should be increased using the same scaling factor i.e. ($\alpha.N_a$) [7, 8]. As a result the switching speed is boosted by a factor of α when the power consumption is reduced by a factor of α^2. In Table 1.1 a summary of the scaled features as well as the effects on the device performance is shown.

Table 1.1: Scaling results for circuit performance which follow from circuit dimension. The rules apply to constant electric field scaling [7].

Device or circuit parameter	Scaling factor
Device dimension, t_{ox}, L, W	1/α
Doping concentration N_a	α
Voltage V	1/α
Current I	1/α
Capacitance	1/α
Delay time/circuit VC/I	1/α
Power dissipation/circuit VI	$1/\alpha^2$
Power density VI/A	1

For more than 4 decades lots of efforts have been made in order to meet Moore's law with respect to the scaling factor proposed by Dennard.

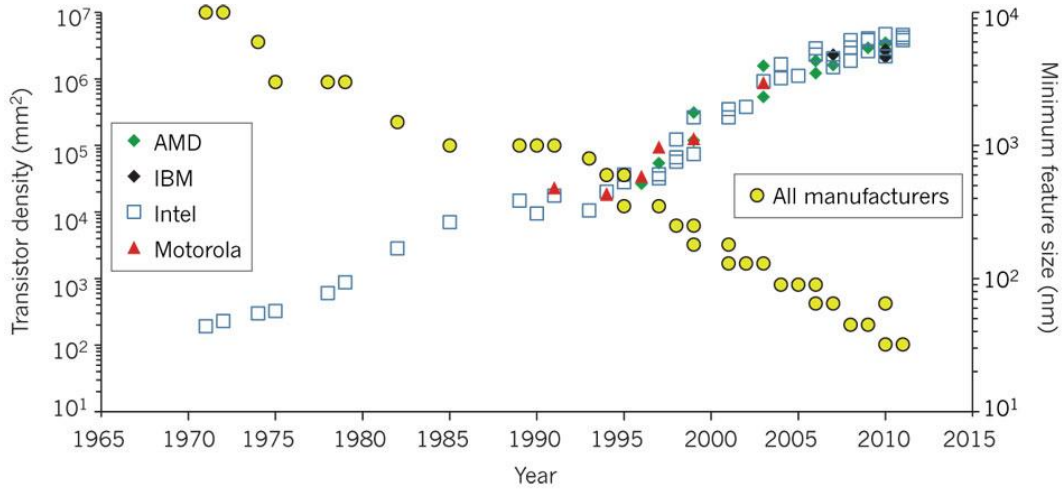


Figure 1.1: Transistor density per square millimetre versus the year of the device introduction (left axis) along with transistor gate length shrinkage versus the year of the device introduction (right axis) Copyright 2011 Nature publishing group [9].

Figure 1.1 shows the evolution of gate length and the density of transistors in microprocessors over the last decades. The gate length shrank from 10 µm to 28 nm

and the number of transistors per square millimetre increased from 200 to over 1 million [9].

With respect to microprocessors and integrated circuits CMOS technology is facing two major problems; power dissipation and variability [10]. From power density perspective, the complexity of the integrated circuits has been accompanied by an increase in power dissipation. As the transistors become smaller in size and faster in performance the overall active power increases due dissipative switching of charge between transistor terminals during logic operations. Although it was relatively negligible a few generations back the standby power has become significantly high and comparable to the active power density. This is caused by the overall increase in the off-state leakage current as a result of gate length scaling and oxide thickness reduction [11]. Figure 1.2 depicts the passive power trend based on the Subthreshold current and show a cross-over point below 20 nm gate length [12].

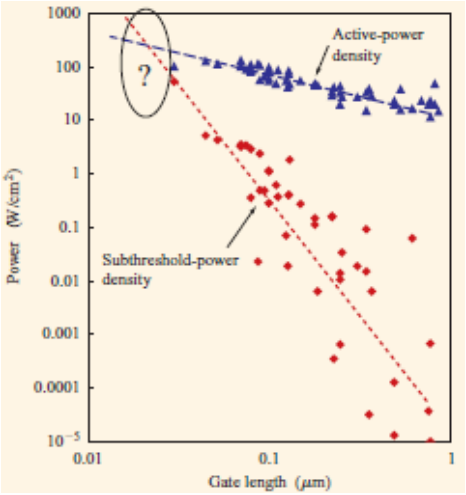


Figure 1.2: Active and subthreshold power density trends plotted from the industry data versus the gate length for junction temperature of 25 °C. The empirical extrapolated dashed-lines show that the active and standby power equal at 20 nm gate length [12].

Regarding the variability issue, doping processes require a very precise control in nanoscale devices. At this scale a random displacement of the dopants can influence the electrical characteristics of the device. In addition fluctuations of channel dopants can cause variations in the threshold voltage which is problematic for circuit design in terms of yield and reliability [10]. In fact other processes (e.g. lithography, etch) can also introduce variability or defects in the substrate. All of these things become more critical as the transistor scales.

1.1.1 Transistor shrinking challenges

In a typical n-type bulk transistor like Figure 1.3 the channel is controlled by the gate. When the gate voltage reaches a certain value called threshold voltage the holes are pushed away and electrons are attracted to the channel forming an inversion layer underneath the gate. At this stage, increasing drain voltage results in electron current flowing from source to the drain. The current keeps increasing by the drain voltage until the pinch off stage happens where some part of the channel is disappeared due to the spreading depletion region that is heavily affected by the drain. Meanwhile the strong electric field around the drain region pulls the electrons to the channel. From now on the current is a function of the gate voltage and is almost independent of the drain voltage. This is where the transistor enters the on state (saturation region).

In this case the on current is calculated from

$$I_{on} = \mu W \frac{\varepsilon_{ox}}{2 L_g t_{ox}} \left(V_{GS} - V_T\right)^2 \tag{1.1}$$

where μ is the carrier mobility in the channel, W is the width of the gate, L_g is the gate length and ε_{ox} and t_{ox} are the oxide permittivity and thickness respectively.

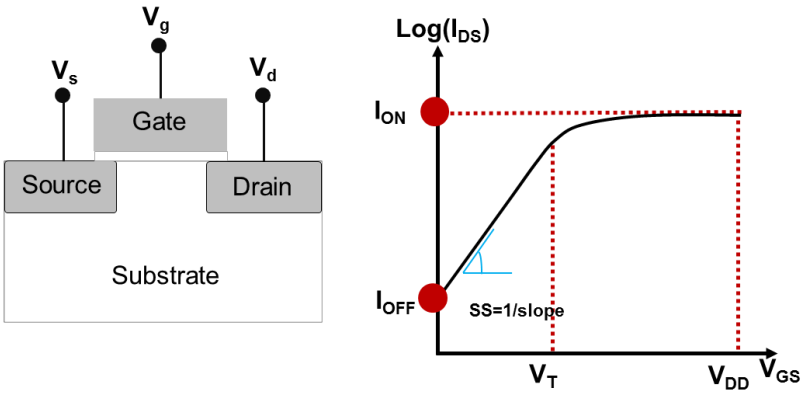


Figure 1.3: Schematic representation of a typical bulk transistor and the corresponding current voltage characteristic.

From the equation above it is clear that a thinner gate oxide, shorter gate length as well as a wider gate can boost the on current as it has been achieved over the last decades of conventional transistor downscaling. Nevertheless the continuous

shrinking trend came with consequences as the Si technology reached fundamental physical limits.

For instance, the gate oxide thinning can no longer improve the device performance. Poor silicon dioxide (less than about 3 nm thickness) results in high tunnelling leakage current (~ 3× for every 0.1 nm thickness reduction [11]) through the film which increases the device power consumption. High-κ dielectrics such as zirconia (ZrO_2) and hafnia (HfO_2) have already been introduced to allow further scaling without sacrificing the device throughput.

Moreover the reduced spacing between the source and drain at shorter gate lengths causes short channel effects (SCE) which manifests itself in number of undesired behaviours. The issue looks more critical considering the fact that the practical source drain distance is approximately 50% shorter than the gate length, for example for a 30 nm gate length the actual effective channel length is 15 nm [9]. Figure 1.4 shows a schematic of a transistor and SCE.

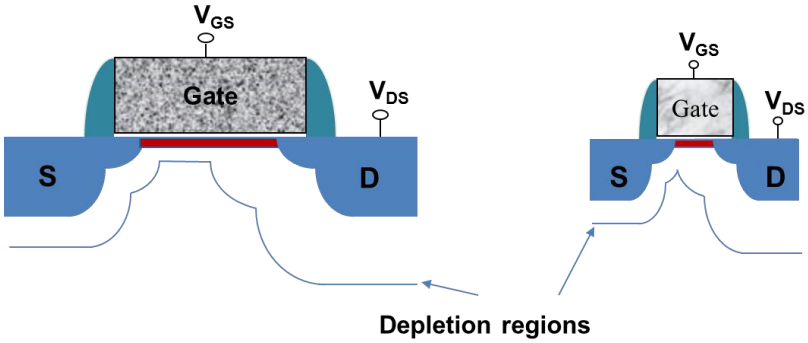


Figure 1.4: Schematic of bulk transistor and short channel effect due to transistor shrinkage. High leakage current and mobility reduction degrade the transistor performance.

In classical transistors there is a potential barrier for electrons to flow from source to the drain. When the gate length is long enough (~ 1 μm) the source and drain are far apart therefore the channel is controlled by the gate whereas at shorter gate lengths, the drain depletion region is extended under the gate, taking over the control of the channel by reducing the potential barrier for electrons to flow from source to the drain. So, as the drain voltage is increased, the current starts increasing even before the voltage on the gate reaches the threshold value. This effect known as drain induced barrier lowering (DIBL) results in reduction of the threshold voltage as the drain voltage increases [9]. This is equivalent to Vt roll-off effect that the gate threshold voltage decreases as the channel length is reduced. The resulting

current flow is called Subthreshold current. The rate of the current increase below the threshold voltage is referred to as subthreshold swing (SS) which is another figure of merit for the device performance and is formulated as [13]

$$SS = \frac{kT}{q} \cdot \ln(10) \cdot n \tag{1.2}$$

corresponding to the inverse of the slope of the linear region in Id-Vg curve (see Figure 1.3). The unit is mV/decade. Here, k_B is the Boltzmann constant, q is the charge of an electron, T is the temperature in Kelvin, ln (10) is coming from the logarithmic scale of the plot and n is the body factor which is an indication of the level of efficiency of the gate control over the channel. The body factor can be calculated from

$$\begin{aligned} n &= \left(1 + \frac{C_b}{C_g}\right) \\ C_b &= \frac{\varepsilon_{Si}}{W_d} \\ C_g &= \frac{\varepsilon_{ox}}{t_{ox}} \end{aligned} \tag{1.3}$$

where C_b and C_g are the bulk and gate capacitance respectively. ε_{si} and ε_{ox} denote the Si and oxide dielectrics respectively. W_d is the depletion region under the channel and t_{ox} is the gate oxide thickness.

As is seen in the equation SS cannot be below a certain value due to the theoretical limits. In fact in the best possible case where gate has the full control over the channel the SS is approximately 60 mV/decade at room temperature. However, in practice the body factor is larger than 1, so the SS is always above 60 mV/decade. To minimize SS the gate should establish a relatively fixed bulk charge in the depletion region as the gate voltage is changing so that the bulk capacitance is kept as small as possible.

Again the importance of maintaining the gate control over the channel is highlighted. In short channel devices the extended electric field from the drain can result in increased SS value. One possible solution for this issue is lightly doped substrate.

Another side effect of transistor shrinkage is velocity saturation. Due to strong electric field in the channel the velocity of carriers reaches the maximum, and does

not follow the linear relation with the electric field. This is attributed to increased levels of scattering that the accelerated electrons are going through so that they lose their energy. Saturation velocity was observed for 250 nm gate length in SOI transistors [14].

Generally speaking the main outcome of the SCE is high leakage current which results in more power dissipation.

In order to minimize SCE and access resistance in conventional planar devices it is necessary to highly dope source and drain regions while maintaining shallow and abrupt junctions. In this case the scattering rate of the ionized dopant atoms is higher resulting in mobility degradation.

Higher doping concentration in the channel in order to reduce the depletion width is also required along with mobility enhancement techniques such as strain engineering by using SiGe, or SiC to introduce strain in Si lattice.

One of the important features that affect the transistor performance is parasitic source drain resistance (R_{SD}). It is suggested that four components contribute to the R_{SD}, which can be listed as: overlap resistance (R_{ov}), extension resistance (R_{ex}), deep resistance (R_{dp}), and contact resistance (R_c). In nanometre size transistors R_{SD} is more pronounced and needs special attention. Among the resistance components overlap resistance is strongly dependent on the doping concentration in the overlap region as well as the lateral abruptness of the region which can affect the current spreading and the accumulation carrier density. So care must be taken when doping this region [15].

In an extensive study by Seong-Dong *et al.* it was predicted that at 50 nm gate length the contact resistance and the overlap resistance contribute up to 70% of the total source drain resistance and as the transistor gets smaller the contact resistance contribution in the total resistance becomes more significant [16]. Therefore it is essential to implement novel processing techniques for doping and annealing in order to minimize contact resistance in new generations of the scaled transistors.

A feasible solution for advanced CMOS technology to pursue the downscaling trend seems to be the emergence of new generations of transistors with innovative geometrical structures such a multi-gate MOSFETs and FinFETs [9] as well as introduction of new alternatives for silicon e.g. III-V materials and Ge.

1.2 Potential replacements for Si

In the first place Si became the prevailing material in semiconductor technology due to its excellent native oxide, but because of the failure of the gate oxide in aggressively scaled transistors new hi-κ materials had to be introduced to do the task. When SiO_2 was replaced, one of the main reasons for using Si was lost and researchers began investigating new high mobility semiconductor materials such as III-V compounds, Ge, graphene, and transition metal dichalcogenides (TMD) [17]which seem to have the potential to replace Si. Table 1.2 shows the properties of several high mobility materials that could be used in nanoscale devices.

Table 1.2: Comparison of high mobility materials with Si [11].

Property	**Si**	**Ge**	**GaAs**	**InP**	**InAs**	**InSb**
Electron mobility (cm^2/ Vs)	1500	**3900**	8500	5400	40000	77000
Hole mobility (cm^2/ Vs)	475	**1900**	400	200	500	850
Bandgap (eV)	1.12	**0.66**	1.42	1.34	0.35	0.17
Dielectric constant (mterial)	11.7	**16.2**	12.9	12.5	15.2	16.8

These materials benefit from high electron mobility that is essential in making high speed devices. GaAs and InAs, and InSb have significantly higher electron mobility than Si which makes them promising materials for high performance n-type transistors. On the contrary, they have less or comparable hole mobility as compared to Si which is not quite favourable for making p-type transistors. Processing and fabrication of these expensive materials is costly as well and may need a separate fabrication line as these materials cannot be processed in conventional Si labs due to contamination issues. On the other hand, Ge appears to have several distinctive characteristics over the other candidates. Compared to Si, it benefits from higher carrier mobility for both electrons (2×) and holes (4×). More importantly, Ge is a non-contaminant element, which makes it compatible with Si fabrication tools and infrastructure. Note that Ge has already been used in the form

of SiGe in 90 nm and smaller technology node transistors to obtain higher mobility and faster devices.

Although these advantages suggest Ge as a good choice, Ge technology is not fully mature [18] in order to extensively incorporate this material in the advanced CMOS technology. Perhaps the biggest challenge is process and integration of Ge in an efficient way so that high-mobility benefit is not swamped by imperfect manufacturing procedures.

1.3 New device architectures

The transistor miniaturization has led to the emergence of various revolutionary device architectures. Figure 1.5 shows the evolution of transistors from 1980s till now. The main point of these architectures is to improve the gate control over the channel. It is well established that silicon-on-insulator (SOI) devices have the potential to improve SCE in traditional bulk transistors.

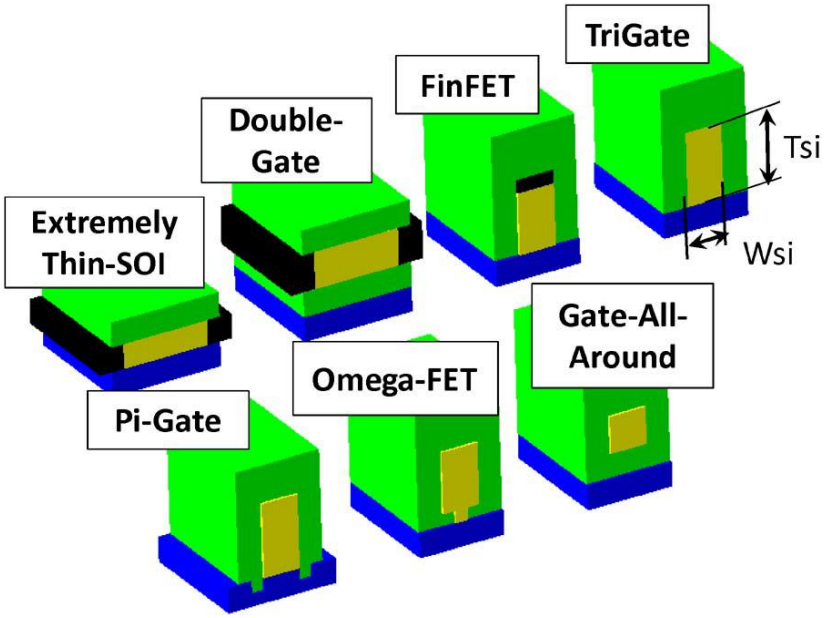


Figure 1.5: Illustration of the alternative transistor designs reducing the short channel effect [19].

In these devices that are known as extremely thin SOI device (ETSOI) the Si film thickness is thinner than the channel depletion depth [19]. These devices benefit from smaller source/drain to substrate capacitance, switch faster and run at lower voltages and offer body bias [19]. However the necessity for very small thickness of the Si film create challenges such as thickness targeting and variations

in the ETSOI wafer, high parasitic source drain resistance, quantum confinement and scattering. Also, the drive current in these devices is less than comparable bulk transistors.

Another alternative approach is surrounding the gate with two or more opposing gates where each additional gate improves the SCE. These devices can be oriented horizontally (double-gate device) or vertically (FinFETs) and also can be fabricated on SOI substrates. They have the advantage of enhanced gate control therefore the leakage current is suppressed and the switching speed is increased. An additional benefit of these devices compared to ETSOI devices is that the total electrical area can be dramatically larger than the device footprint [19].

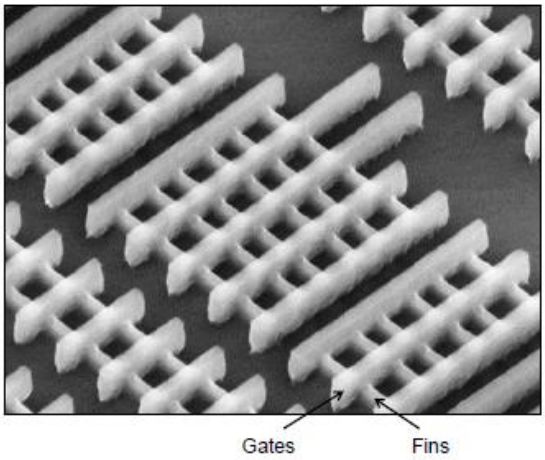


Figure 1.6: 22 nm Tri-gate transistors on bulk Si made by Intel [20].

Switching to new non-planar structures has enabled the industry to proceed to the 22 nm technology node. The vertical architecture of these devices allows integration of more devices on a chip and making faster circuits and probably a wider range of functionalities. Manufacturing of these devices is quite challenging. The higher device current achieved in these devices can very well pay off the difficulties for fabricating these devices. In fact patterning and fabrication of high aspect ratio fin structures at aggressively reduced fin pitches impose new challenges and demand new doping and annealing techniques. In 2011 Intel introduced a new generation of the CPUs fabricated from Tri-gates on SOI. Figure 1.6 is a representative image of the transistors demonstrated on bulk Si substrate.

It is generally accepted that the FET devices will continue the transistor scaling toward ultrathin body channels [17].

The ultimate CMOS device is likely to be a nanowire with a gate-all-around geometry, a hi-κ gate dielectric and conductive gate electrode. In these devices scaling the gate pitch can be done by scaling the source and drain regions, spacer and overlap regions or the channel length, however there are trade-offs associated with that. For example, a wider spacer can decrease the parasitic capacitance but at the cost of increased parasitic source drain resistance as these regions will have to be smaller. If there are good electrostatics then the channel length can be shorter enabling larger S/D regions and smaller parasitic resistance but it is accompanied by increased gate parasitic resistance [19]. The interference of parasitic resistance in each region of these devices can impede the device performance by reducing the drive current and making the device slower. As an example the gate region contains a gate contact with underlying gate metal layers and there is a resistance associated with each of these layers. The resistance of the S/D regions includes the resistances of the contact, the silicide, and an epi layer, and the most critical task is probably minimizing the Schottky barrier height. Parasitic capacitance will be more challenging in new devices due to the reduced distance between the gate and the other parts [19]. Therefore it appears that advanced technologies and materials are needed to address the traditional as well as the new challenges in device scaling.

1.4 Challenges for introducing Ge to CMOS technology

Even though Ge is very similar to Si, there are some differences in terms of material characteristics that make it a challenging task for industry to fabricate fully operational Ge transistors.

The most well-known challenges facing the Ge technology can be summarized as:

- The substrate / integrate Ge on Si wafer
- Gate dielectric
- **Doping**
- **Contacts**
- **Thin body devices**
- **Leakage current**

The issues in bold will be discussed in this thesis. Regarding the material strength Ge wafers (in 300 or 450 nm diameter) are not strong enough to survive the auto-feed handling involved in mass production of integrated circuits. The lattice constant of Ge is ~4% greater than that of Si, therefore Ge growth on Si will start to relax almost immediately via the formation of misfit dislocations. To solve this problem, a thick Si_xGe_{1-x} buffer layer is grown on the Si substrate and the active Ge layer is grown on top of that, where the defect density is reduced considerably. This buffered-growth technique provides a way of integrating Ge devices on a Si handle wafer [17]. Another approach is growth in trenches using the aspect ratio trapping technique [21].

One of the most well-known obstacles rises from the unstable water soluble germanium oxide (GeO_2) that cannot be used as gate dielectric in Ge MOSFETs in a straightforward approach. In fact GeO_2 when in contact with Ge transforms into GeO which tends to desorb at temperatures above 400 °C. The consequence is the loss of the underlying Ge layer as well as desorption of the oxide layer, and roughness of the surface.

Various approaches have been proposed to form a proper dielectric on Ge such as, such as Si, GeO_2, and oxynitride interfacial layers, high pressure thermal oxidation, sulphur passivation, plasma oxidation, etc. Other high-κ materials are also introduced for Ge CMOS devices, like HfO_2, $LaLuO_3$, ZrO_2, and GeO_2/AlO_3 gate stacks for n-type Ge devices [17].

The other major problem is realization of n-type ultra-shallow junctions with highly activated dopants. It is well established that n-type dopants in Ge tend to diffuse quickly and are relatively difficult to activate. In contrast, p-type dopants i.e. B exhibit low diffusivity as well as high activation levels ($> 10^{20}cm^{-3}$) in Ge, favourable for fabricating high performance PMOS Ge devices [18]. The shallowest p-type profile in Ge has been generated by B 2 keV implant [22] whereas As 5 keV implant have been carried out to produce the shallowest n-type doping profile [23].

Point defect engineering techniques such as co-implants as well as non-implant doping approaches like plasma doping, spin-on-dopant along with novel annealing techniques like laser, flash lamp or microwave annealing might be helpful to offer solutions for these problems.

Realizing a low resistive contact on n-type Ge is another key bottleneck. The problem arises from the material properties which lead to formation of high Schottky barriers between Ge and the contact metal. In contrast formation of ohmic contacts on p-type Ge is more straightforward. Several solutions have been proposed to minimize the barrier height and form an ohmic contact mainly with two approaches; terminating the dangling bonds on the surface and optimization of the germanide alloy with high doping concentrations underneath.

Ge band gap (0.67 eV) is about half of that of Si leading to higher leakage current in pn junctions [24]. Utilizing advanced processing techniques, and point defect engineering would allow formation of junctions with minimum defects which are one of the main reasons for leakage current.

Modelling capabilities are not developed as compared to extensive experimental works that are being done on Ge and need to be improved in order to give substantial input for time and cost effective development of Ge devices [17] .

As stated earlier there are many unknowns about Ge that need to be answered and this entails application of novel approaches for doping, annealing, fabrication so that Ge can be extensively used in device fabrication. The main focus of this thesis is on the problems related to doping, contacts, leakage current and thin body devices.

1.5 Thesis structure

This dissertation addresses different issues in the fabrication and characterization of Ge based devices.

Chapter 2 provides a short introduction on metal semiconductor contacts, Fermi level pinning and the mechanism involved in this phenomenon. A short literature review on contacts on n-type Ge is presented as well. Formation and characterization of low resistance NiGe contacts on Ge with respect to dopant type, dopant concentration, and annealing techniques is discussed.

In Chapter 3 we discuss different doping and annealing methodologies with main focus on laser and rapid thermal annealing techniques where we systematically compare the impact of the two on dopant activation, and leakage current in n+/p

junctions. The effect of F for controlling dopant diffusion is studied. The Ge desorption phenomenon and its contribution to dopant loss is investigated as well.

In Chapter 4 we briefly analyse the effect of ion implantation into thin body structures using SRIM simulation tool. Next we study solid phase epitaxy in thin body Ge structures. In the final section we implement a MOVPE-based non-destructive doping technique for doping nanometre thick fin resistors and show the results of material characterizations and extract electrical parameter associated with resistance.

Finally Chapter 5 summarizes the key points of this study and discusses possible future works that can help to expand the understanding of Ge challenges and their potential solutions.

Chapter 2

Contacts on Germanium Devices

2.1 Introduction

Metal semiconductor (MS) contacts are known as a key part in every semiconductor based device. They can be classified as: (i) Ohmic, which is essential in connecting the integrated circuits to the outside world with no/negligible resistance so that it does not affect the performance and efficiency of the device, and (ii) Schottky, which is used in high speed rectifying diodes, solar panels, and power devices.

A brief introduction of MS contacts and Fermi level pinning (FLP) phenomena are in the opening of this chapter followed by the state-of-the-art work that has been reported so far to address the issue. The main focus of this chapter is on formation of low resistance contacts on n-type Ge and their characteristics with regard to dopants concentration, dopant type and annealing techniques.

2.2 Metal semiconductor contacts

Metal work function is defined as the energy (in electron volts) required for freeing an electron from the metal Fermi level to the vacuum level while the electron is still close to the surface in macroscopic scale. This value is a property of the material and cannot be changed. In semiconductors the work function can be tuned by changing the concentration of the dopants. Figure 2.1 illustrates the band diagram of the metal-semiconductor system before making contact. $q\Phi_M$ and $q\Phi_S$ are the metal and semiconductor work functions respectively. $q\chi$ is the semiconductor electron affinity referring to the energy required to extract an electron from the conduction band to the vacuum level. If the materials do not interact then for $\Phi_M > \Phi_S$ it can be said that the average total energy of an electron in semiconductor is higher than that of metal.

The opposite is true if ΦM< ΦS. When these materials come to an intimate contact, electrical current flows across the interface in a non-linear fashion against the biased voltage [25].

The underlying story is that after the contact is made in order to establish equilibrium the conduction band (CB) electrons flow from the semiconductor to the metal. For p-type semiconductors this role belongs to the holes in the valence band (VB). As a result Fermi levels are aligned, with a new arrangement made in the band diagrams as is shown in Figure 2.2.

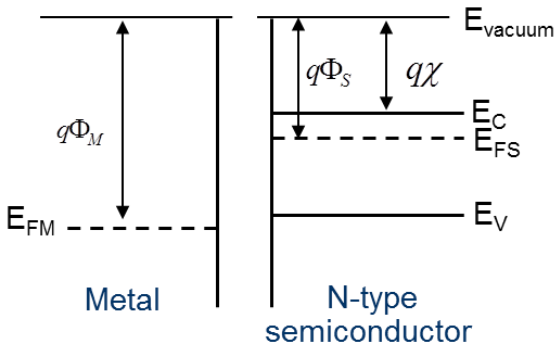


Figure 2.1: Schematic of the energy band diagram of metal and n-type semiconductor before making contact.

Migration of electrons from the semiconductor CB to the metal leaves fixed positive charges behind leading to formation of a depletion region at the interface.

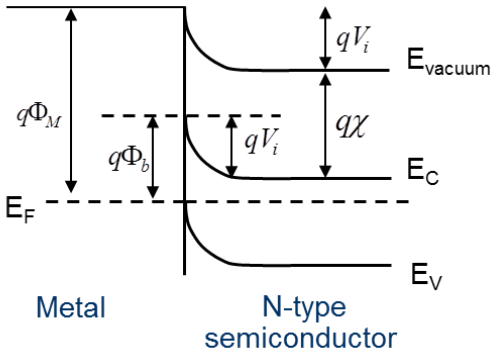


Figure 2.2: Energy band diagram of the MS Schottky contact under equilibrium [26].

At this point a potential barrier is formed preventing further movement of electrons and is given by

$$qV_i = q\Phi_M - q\chi \qquad (2.1)$$

In the meantime on the metal side a built-in potential barrier is formed known as electron Schottky barrier height (eSBH):

$$q\Phi_b = qV_i + (E_c - E_V) \tag{2. 2}$$

This barrier leads to a rectifying behaviour allowing the current flow only from one side to the other. The current flow from the semiconductor to the metal changes depending on the applied bias voltage. If a positive voltage bias is applied to the MS contact the potential barrier is reduced for the electrons in semiconductor but not for the electrons in metal. Therefore the electron current flow from the semiconductor to the metal increases. In a reversed bias situation the potential barrier increases and the current flow from semiconductor to the metal decreases drastically. In both situations the SBH is not changed and therefore the electron current flow from the metal to the semiconductor remains unchanged leading to a rectifying non-linear current–voltage behaviour [26]. The MS contact is a majority carrier device with little minority carrier conduction, and therefore it is a fast switching device. Similar discussion is applied for p-type semiconductor with holes being the majority carriers [27].

Ohmic contacts in MS system are possible via: (i) formation of tunnelling barriers where the metal is a degenerately doped n-type semiconductor (ii) MS systems where the metal work function is smaller than that of the semiconductor [27]. In a degenerately doped n-type semiconductor Fermi level is near the conduction band. In this case the dopant concentration is very large so that the depletion region is very small where tunnelling through the potential barrier can happen (see Figure 2.6 c)). In this case in reversed bias condition the electrons easily tunnel through the barrier from metal to the semiconductor and in forward bias they tunnel through the barrier from the semiconductor to the metal. Much of the same can be said for metal Schottky tunnel barriers on degenerate p-type semiconductors in which the holes flow from the metal to the semiconductor and vice versa.

Regarding the second approach, the metal with smaller work function has the electrons with higher energy levels so the intimate contact between the two materials would lead to the electron flow from metal to the semiconductor. Here the

surface of the semiconductor consists of free mobile electrons, which is not the case for the Schottky contacts. Also the electrons from the conduction band of the semiconductor see no barrier towards the metal as is shown in Figure 2.3[27].

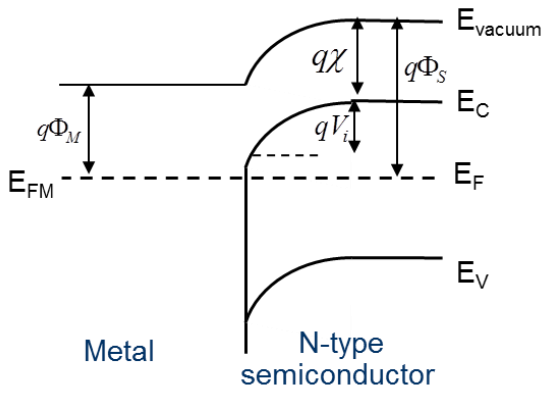


Figure 2.3: Energy band diagram of an ideal the MS ohmic contact under equilibrium [27].

Nevertheless, this approach does not seem to be applicable for n-type Ge in contrast to Si according to the extensive experimental studies carried out in this area [28]. The mechanism involved in this is discussed in the following section.

In general a large SBH and Schottky MS system on n-type Ge is expected to behave ohmic for the equivalent MS system on p-type Ge. For example in a study by Nishimura *et al.* an identical process fabrication on n and p-type Ge resulted in Schottky and ohmic contacts on the n and p-type Ge substrates respectively [29].

2.3 Fermi level pinning

Experimental works on SBH measurements in Ge revealed that in many of the materials SBH is independent of the metal work function [25]. This phenomenon, which is called Fermi level pinning (FLP), was later attributed to two mechanisms.

2.3.1 Surface states

During the fabrication procedure of a semiconductor device the surface integrity and crystal lattice of the semiconductor is perturbed leading to formation of dangling bonds at the semiconductor surface. This would subsequently give rise to the number of surface states in the semiconductor band gap near the interface.

Being called interface traps these states lie within the band gap and are occupied with electrons if they are below the Fermi level.

When contact is formed between metal and the semiconductor, again Fermi levels should align on both sides and as a result band bending should happen. If the interface state density is large then a negligible movement of Fermi level at the semiconductor surface will transfer sufficient amount of charge from the semiconductor to the metal (see Figure 2.4).

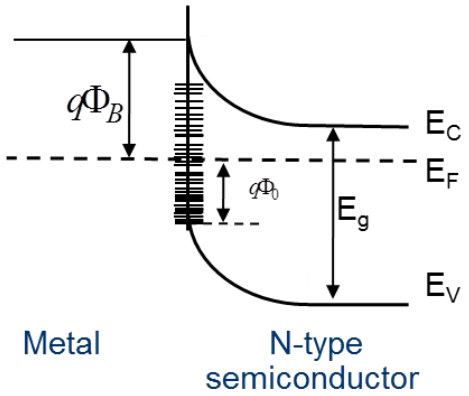


Figure 2.4: Energy band diagram of a non-ideal MS contact.

Therefore the alignment of the Fermi level is accomplished by movement of the electrons in the interface traps to the metal indicating that the contribution of band bending in alignment of Fermi level is negligible [26]. For Ge, the Fermi level is pinned close to the Charge Neutrality Level (CNL) located only 0.09 eV above the valence band [30], resulting in a large electron SBH and high contact resistance for n-type devices. As is shown in Figure 2.5 the SBH formed on Ge is almost independent of the metal work function.

The barrier height is calculated from

$$q\Phi_b = E_g - q\Phi_0 \qquad (2.\ 3)$$

According to Nishimura *et al.* the barrier height in Ge is hardly modulated by annealing in forming gas, metal-germanide/Ge interface or changing the substrate orientation [28]. Figure 2.5 shows the SBH extracted for various metals on n-type Si and Ge. Nevertheless it appears that processing and surface preparation techniques can significantly affect the SBH in MS contacts [25].

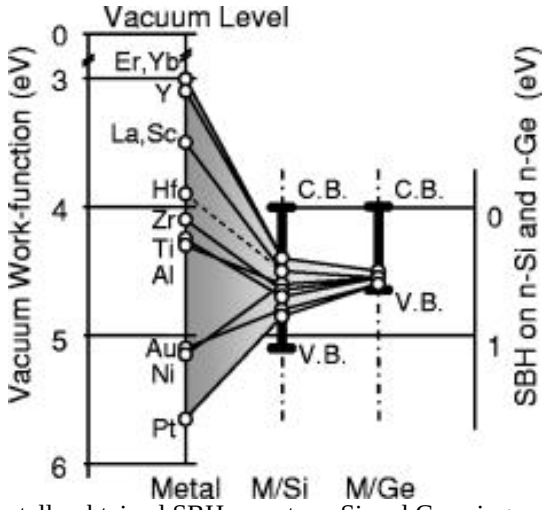


Figure 2.5: The experimentally obtained SBH on n-type Si and Ge using metals with a wide range of work functions. In contrast to Si SBH in Ge is nearly independent on the work function of the metal [28].

2.3.2 Metal induced gap states (MIGS)

Another possible reason proposed for FLP is metal induced gap states (MIGS) that are the energy states in the semiconductor originated from the tailing of the metal electron wave functions. As a result there is a scattering of negative charge from the metal into the semiconductor. In this case inserting an ultrathin insulating layer could depin the FL as the tailing of the metal electron wave function is blocked.

Engineering the barrier height in order to form ohmic contacts seems to be impractical at this stage since the formation mechanism of the SBH is still unclear itself. However it is possible to tune the depletion width at the interface by manipulating the semiconductor doping. This is also the case study for formation of low ohmic contacts on n-type Ge which is one of the stumbling blocks associated with the successful integration of advanced Ge devices.

As mentioned earlier, as a result of making a contact between a metal and n-type semiconductor, electrons transfer from the semiconductor to the metal, and a depletion region is formed. The width of this region changes depending on the doping concentration of the semiconductor (N_D) affecting the conduction mechanism in MS contacts [31] which is shown in Figure 2.6.

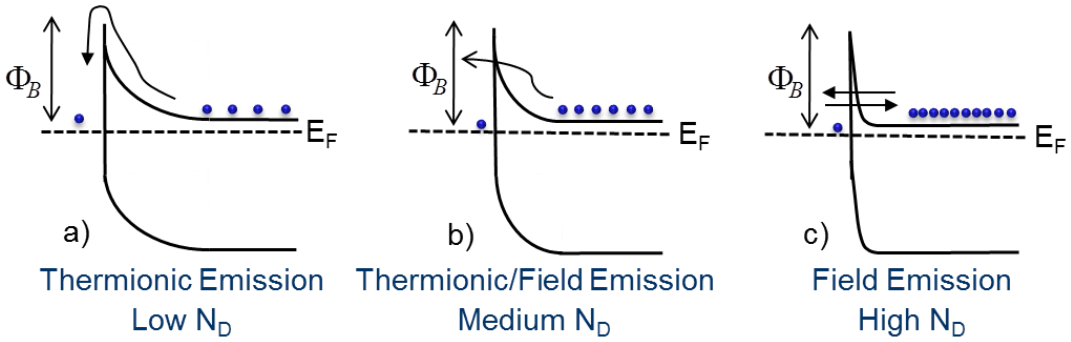


Figure 2.6: Electron flow mechanism for metal-n-type semiconductor contacts for different semiconductor doping concentrations. a) is for lowly doped Ge and c) is for highly doped Ge [31].

In lowly doped semiconductors the electrons leap over the barrier when they are thermally excited. This mechanism is shown in Figure 2.6 a) and is called thermionic emission (TE). For a moderately doped semiconductor the dominant mechanism is thermionic-field emission (TFE). In this case conduction happens in two steps in which electrons are thermally excited to a higher energy level where the barrier width is narrow so that they can tunnel through to the other side (Figure 2.6 b). For a highly doped semiconductor current flows under field emission (FE) mechanism where the electrons can tunnel through the barrier which has become sufficiently narrow as is shown in Figure 2.6 c) [31].

2.4 State-of-the-art work for contacts to n-type Ge

2.4.1 Thin insulating layers

Several methods and techniques are suggested to modulate eSBH. Ultra-thin amorphous insulating layers, such as Ge_3N_4 [32] or GeO_x (1.6-2.2 nm) [29] can terminate the free dangling bonds, and eliminate FLP. A GeO_x layer between a metal and n-type Ge has been used to improve contact performance [33]. MgO ultrathin layers can also depin the surface and exhibit a weak thickness dependence [34]. It was shown that an amorphous interlayer at TiN/Ge contacts which contains nitrogen can alleviate FLP [35]. An extensive theoretical study by Roy *et al.* predicted contact resistivity (ρ_c) of tunnel barrier contacts where the variable was the thickness of a thin insulating layer [36].

2.4.2 NiGe optimization

Another approach to creating stable low resistive contacts is to form a metal-semiconductor compound at the surface in combination with high doping concentrations underneath. Gaudet *et al*. examined twenty transition metals as candidates for metal-germanium reaction [37]. Based on the low formation temperature, stability, resistivity, and sensitivity to oxidation, NiGe and PdGe were suggested as the most promising candidates. NiGe is often favoured due to less problematic removal of unreacted Ni [38] during the full MOSFET process flow. Lee and Zhang also performed NiGe material studies where the germanides were formed at different reaction temperatures [39, 40]. Sheet resistance rose sharply above 500 °C, attributed to NiGe agglomeration. P and As segregation during NiGe formation reduces the eSBH due to the snowplow effect of the dopant atoms in front of the growing germanide front [41]. In that work the dopants were ion implanted, and As had a stronger influence than P, presumably due to a more effective snowplow of the larger atom.

Selenium segregation was also used to reduce eSBH for NiGe/n-Ge contacts [42]. NiGe contacts formed by a 300-400 °C germanidation anneal showed ohmic behaviour (derived from I-V characteristics) in combination with high phosphorus doping [43, 44]. Furthermore, Ikeda *et al.* modulated eSBH by Sulphur snowplow during germanidation [45]. Gallacher *et al*. extracted specific contact resistivity (ρ_c) of 2.3×10^{-7} $\Omega.cm^2$ on n-type Ge that was doped during epitaxial growth [46]. The optimum NiGe formation temperature was a 340°C RTA. However the NiGe interface with the underlying substrate was not smooth. Recently ohmic Ni contacts on n-type GeSn were reported [47].

2.4.3 High dopant activation

Hutin *et al.* presented further evidence of eSBH reduction with increased dopant concentration at the surface [48]. Koike *et al.* performed two step P implantation prior to formation of NiGe contact on Ge [49]. After the first P ion implantation high-temperature annealing (at 600 °C for 1 min) was carried out to form n+/p junctions. This was followed by the second P implantation into the n+-Ge after contact holes were formed on the surface. In order to suppress P diffusion no

activation annealing was carried out. After Ni deposition and RTA treatment at 350 °C $\rho_c \sim 3\times10^{-8}$ $\Omega.cm^2$ was obtained.

Low ρ_c was reported by Miyoshi *et al.* using carrier-activation enhancement (CAE) technique. In that work P/Sb co-implantation was used to reduce SBH in NiGe/n+ Ge contacts [50].

2.4.4 Other interface engineering techniques

The other promising segregation technique known as Implantation Through Silicide (ITS) was used by Dubois et al., where dopants were implanted after the alloy formation [51]. In that method dopants segregate at the interface during low temperature post RTA, while the silicide front is not growing. P segregation has also been employed during PtGe formation to reduce eSBH, where P was originally in-diffused from a spin-on-resist, and the process variable was the in-diffusion anneal step [52]. Dumas *et al.* used an evaporation of a mixed alloy of Ag/Sb (99%/1%) onto to a moderately doped ($N_D=1\times10^{18}$ cm^{-3}) n-type Ge and showed formation of AgSb ohmic contacts. In that work Ge was epitaxially grown on Si wafers with P in-situ doping [53]. CF_4 plasma treatment of the Ge surface was demonstrated experimentally to alleviate FLP [54]. Zheng *et al*. reported ohmic contacts to n-type Ge using Yb-germanide where 60 nm of Yb was deposited followed by SiO_2 deposition to prevent Yb oxidation and finally RTA treatment at 500 °C [55].

One of the state-of-the-art techniques which has been proven to be effective in formation of low resistance contacts is laser thermal annealing (LTA). Firrincieli *et al*. studied ρ_c of NiGe contact using two different approaches; sub-melt laser anneal (LA) prior to germanidation and Snowplow effect. Using LTA for dopant activation, in combination with RTA for NiGe formation resulted in ρ_c of 8×10^{-7} $\Omega.cm^2$ on n-type Ge. In snowplow effect the implantation of n-type dopant species is followed by NiGe formation at low temperatures (maximum 400 °C) leading to segregation of dopants during germanidation to the NiGe/Ge interface. The group reported ρ_c of 2×10^{-5} $\Omega.cm^2$ using this technique. In that work the NiGe layers were thermally stable up to 350 °C, but the interface with the Ge substrate was not flat. This is common for NiGe layers formed by RTA [56].

Lim *et al.* have demonstrated Fermi-level depinning using multi-pulsed LTA by the formation of epitaxial $NiGe_2$ [57]. While the steps accompanying the growth of germanides, and closely related silicides, by RTA have been studied to some extent, the formation pathway for the LTA processed materials has not been thoroughly investigated.

2.5 Contacts on p-type Ge

On the contrary to n-type, FLP is favourable in making ohmic contacts to p-type Ge [29, 30]. It is a common practice to form contacts on Ge after a pre-amorphisation implant (PAI) followed by ion implantation (II) and RTA. Bhatt *et al.* achieved a record low ρ_c of 1.7×10^{-8} $\Omega.cm^2$ and 7.7×10^{-8} $\Omega.cm^2$ using cryogenic and room temperature (RT) B implantation respectively. A summary of ρ_c obtained for p-type Ge is presented in Table 2.1. A table on the n-type doped Ge is shown later in this chapter.

Table 2.1: Representative ρ_c values reported to for p-type doped germanium (from Ref. [58])

Method	$N_{peak}(cm^{-3})$	$R_{sh}(\Omega/sq)$	ρ_c $(\Omega.cm^2)$
PAI+II+RTA	1×10^{19}	NA	8×10^{-8}
p-Ge	1×10^{19}	NA	2×10^{-6}
p-Ge	1×10^{18}	NA	3.5×10^{-7}
RT II+RTA	$>1.2\times10^{19}$	155	7.7×10^{-8}
Cryo II+RTA	$>4\times10^{20}$	28	1.7×10^{-8}

In the following section ρ_c dependence on implant dose will be determined, as well as a comparison of P-doped and As-doped Ge layers. P is the slowest n-type dopant in terms of diffusion in Ge [59] thus this parameter extraction is of vital importance. Also we aim to extract a set of ρ_c in the low activation anneal temperature regime (500 °C), consistent with solid-phase-epitaxial-recrystallization [60]. 500 °C appears to be an optimum annealing temperature for n-type dopants, as lower temperatures (e.g. 400 °C) result in poor sheet resistance and activation while at higher temperatures (e.g. 600 °C) diffusion is a concern [61]. A few studies have shown high activation levels (especially for P) without visible diffusion at 500 °C [61, 62].

2.6 NiGe contacts made by Rapid Thermal Anneal

2.6.1 Experimental procedure

In order to extract ρ_c we use the Transfer Length Method (TLM) [31]. Figure 2.7 depicts the schematic of a typical TLM structure. Resistance between two adjacent metal strips is measured, and as shown in the inset of Figure 2.7 resistance is plotted versus contact spacing. A linear fit to the data yields the transfer length (L_T), and contact resistance (R_c) from which sheet resistance R_{sh}, and ρ_c are extracted by

$$R_{sh} = \frac{R_c W}{L_T} \tag{2. 4}$$

$$\rho_c = R_{sh} L_T^2 \tag{2. 5}$$

where W is the width of the structure. In our TLM test structure each NiGe bar was 380×100 µm^2 and the spacings in-between were 4, 16, 36, 64, 100, 144, and 196 µm.

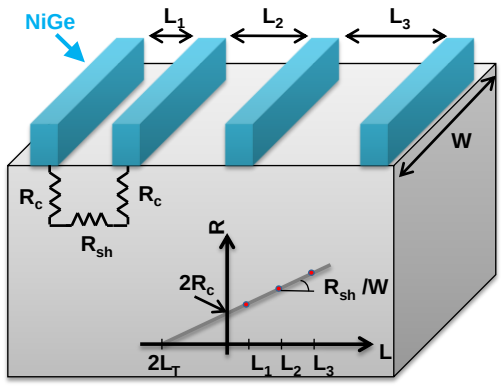


Figure 2.7: A schematic of the Transfer Length Method structure.

The layout consisted of a repeated array of this TLM design. More than 20 TLM structures within each array were electrically measured in order to extract values for ρ_c and R_{sh}. Figure 2.8 shows a summary of the process flow in the experiments undertaken here.

After cleaning, high-resistivity (>40 Ω.cm) n-type (100) Ge wafers received well implants, namely P with a dose of 4×10^{12} cm^{-2} and energy of 180 keV, and B with a dose of 1×10^{13} cm^{-2} and energy of 40 keV, to create a semi-insulating layer.

Next the shallow dopant implant was performed. In one sample set the P implant dose was varied from 5×10^{14} to 2×10^{15} cm^{-2}. The implant energy was 12 keV. In another sample set P and As implants were compared by implanting with the same dose (1×10^{15} cm^{-2}) and with two different energies (15, 28 keV respectively). The dopant profiles had the same projected range (approx. 15 nm) and junction depth (approx. 60 nm) calculated by SRIM modelling [63]. A furnace anneal at 500 °C 3 min in N_2 was performed for dopant activation in all the samples [60].

Sheet resistance measurement of selected samples was performed using Prometrix OmniMap RS35e. The tip spacing was 1.016 mm. Thereafter, 20 nm Ni was deposited on the samples by thermal evaporation. Lift-off process was performed afterwards. A trench was dry etched down to 400 nm deep to avoid leakage current. The samples were subjected to 250, 350, or 450 °C RTA for 30 sec in N_2 for the NiGe reaction. According to data in [37], [39], and [40] this is the process window for low-resistive NiGe formation. Scanning Electron Microscopy (SEM) was done for inspection, using a QUANTA FEG 650. Electrical characterization was done using a KEITHLEY 37100 and a KEITHLEY 2602.

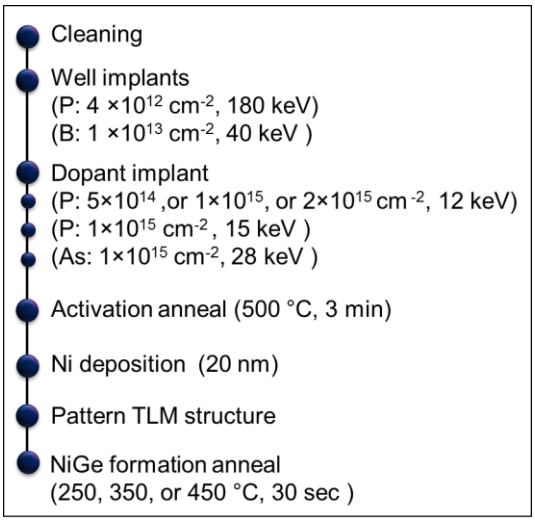


Figure 2.8: A summary of the experimental process flow.

2.6.2 Results of the electrical characterization

Figure 2.9 shows a representative SEM image of the finished TLM patterns. A dashed box highlights an individual TLM, with bright NiGe strips created on the Ge

substrate, surrounded by a 400 nm deep trench which is also labelled. The gaps were measured by SEM to confirm the outcome of the lithography process.

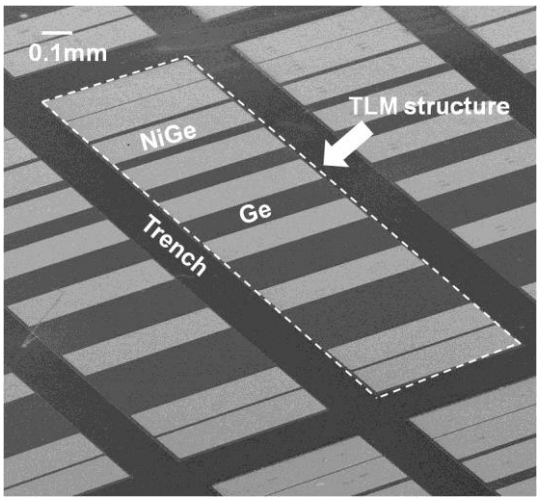


Figure 2.9: A representative SEM image of the TLM structures. Bright strips are NiGe formed on bulk Ge. The TLMs are surrounded by a 400 nm deep trench.

2.6.2.1 ρ_c versus P implant dose

First we consider the sample set where the P implant dose was varied from 5×10^{14} to 2×10^{15} cm^{-2}. Here a 350 °C NiGe formation anneal was applied.

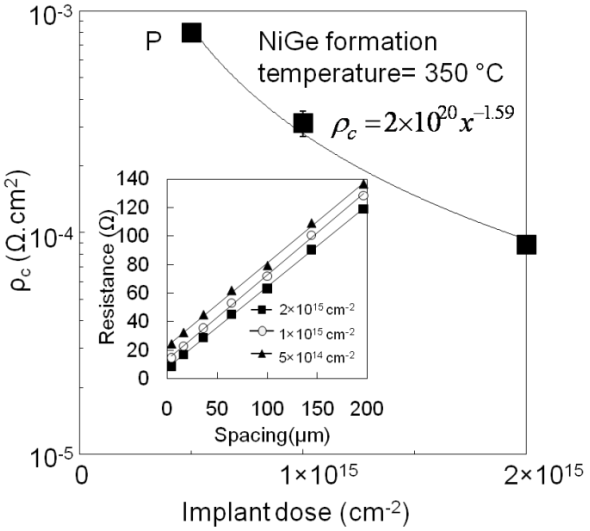


Figure 2.10: ρ_c versus the P implant dose. Increasing the implant dose resulted in decreasing the ρ_c. The inset shows the resistance between two consecutive metal contacts versus the spacing for all the P implant doses. Straight lines are well fitted to the data.

Figure 2.10 represents the result. The inset shows the total resistance as a function of the contact spacing, extracted from a typical TLM electrical measurement, for the three P implant doses.

As is seen straight lines are fitted to the data. Intercepts of the line with vertical and horizontal axes yield R_c and L_T respectively. ρ_c and R_{sh} were then calculated. ρ_c versus P implant dose is shown in the main part of Figure 2.10.

Note that the standard deviation was plotted in the form of error bars, but are so small here that they are barely visible (standard deviation in this case is between 2 to 5 percent). Increasing the implant dose resulted in decreasing the ρ_c, from 7.97×10^{-4} $\Omega.cm^2$ at the dose of 5×10^{14} cm^{-2} to 8.81×10^{-5} $\Omega.cm^2$ at the dose of 2×10^{15} cm^{-2}. The trend line empirically fitted to the data shows that the resistivity is proportional to $x^{-1.59}$, where x is the implant dose. When NiGe TLMs were used to extract ρ_c on p-type Ge [64], ρ_c was found to be proportional to $N_A^{-0.62}$, where N_A was the acceptor concentration and was in the 10^{17}-10^{20} cm^{-3} range, i.e. increasing B concentration reduces ρ_c. For the P implant dose = 2×10^{15} cm^{-2}, the I-V characteristics are shown in Figure 2.11. It can also be seen in the figure that the resistance between contacts increases as the spacing increases.

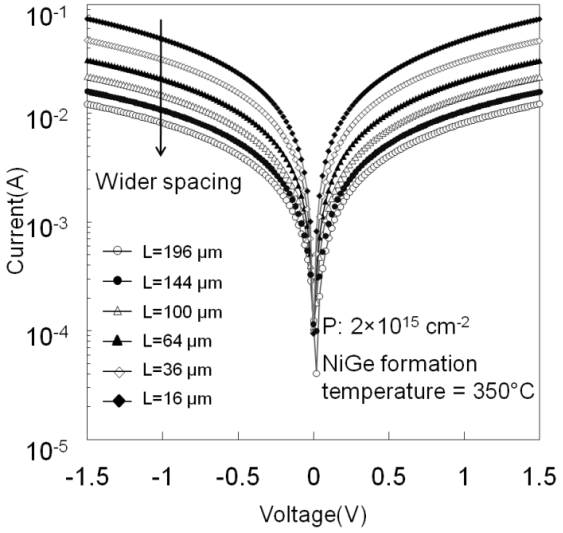


Figure 2.11: I-V characteristics for TLM structures where P implant dose is 2×10^{15} cm^{-2} and NiGe formation temperature is 350 °C.

Figure 2.12 presents the R_{sh} of the P implanted samples versus the implant dose, extracted by standard 4PP and by the TLM structure. The error on the 4PP measurement was ± 10 %. The purpose here is to sanity-check the data extracted from the TLM electrical characterization. Essentially, R_{sh} of the samples is compared before and after TLM patterning, and show reasonable agreement.

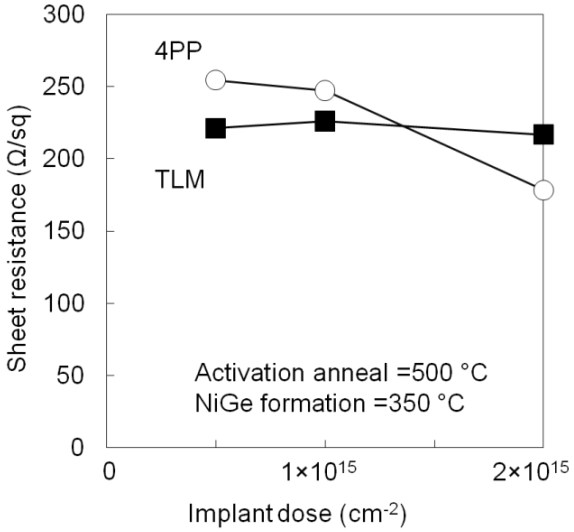


Figure 2.12: R_{sh} calculated from TLM patterns versus the implant dose, comparing the R_{sh} of the samples before and after TLM patterning.

Secondary ions mass spectroscopy (SIMS) and spreading resistance probe (SRP) profiles for similar implant doses and RTA conditions to our work was done by Chui *et al.* [61] and is shown in Figure 2.13.

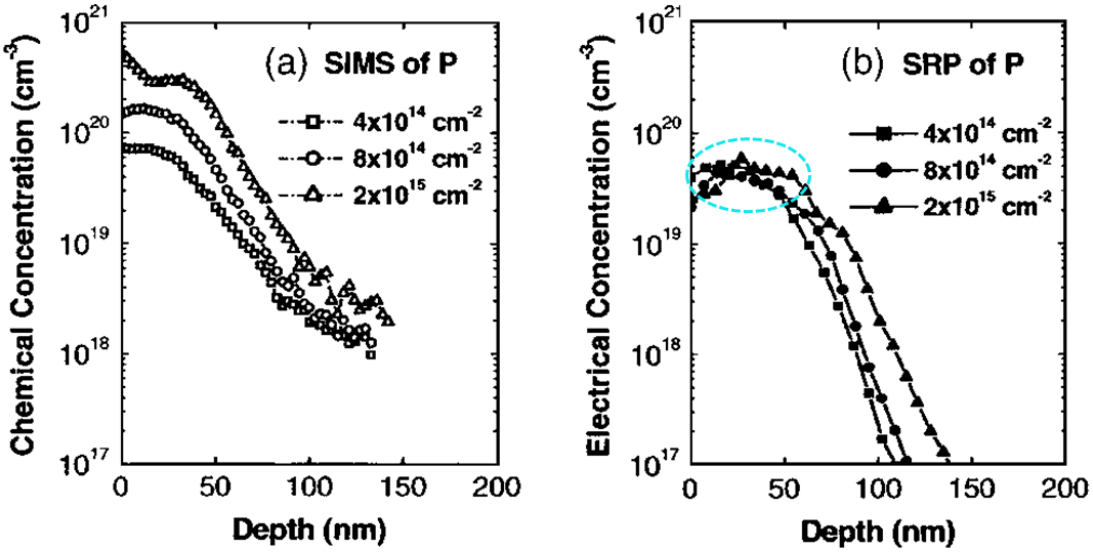


Figure 2.13: SIMS and SRP profiles of P after 10 s RTA at 500 with varying implanted doses from 4×10^{14} to 2×10^{15} cm^{-2}. The electrical concentration in all the samples is limited to ~ 5×10^{19} cm^{-3} due to solubility limit of P in Ge. Copyright 2005 American Institute of Physics [61].

The results show very similar levels of active dopant concentrations for implant doses from 4×10^{14} to 2×10^{15} cm^{-2} which indicates a solid solubility limit, and consequently R_{sh} does not show significant change for the implant range. R_{sh} values and SRIM modelling of the implanted profiles reveals that increasing the implant dose has increased the inactive P dose without significant change in the active P

dose. Regarding this, the decreasing ρ_c in Figure 2.10 could be attributed to the increase in inactive P dose piling up at the NiGe/Ge interface. There are many reports of impurities at the germanide or silicide interface modulating the eSBH [51], [45],[65].

2.6.2.2 ρ_c versus choice of implant

Next we consider the sample set where P and As implants were compared by implanting with the same dose and with energies so that the dopant profile had the same projected range. The inset in Figure 2.14 shows the total resistance of contacts versus spacing for the P and As implanted samples after 350 °C NiGe formation anneal. ρ_c of the TLM structures patterned on these samples were also extracted (Figure 2.14). The variable in this section was the NiGe formation temperature. It can be seen that at each temperature ρ_c of the P implanted sample is lower than that of the As case.

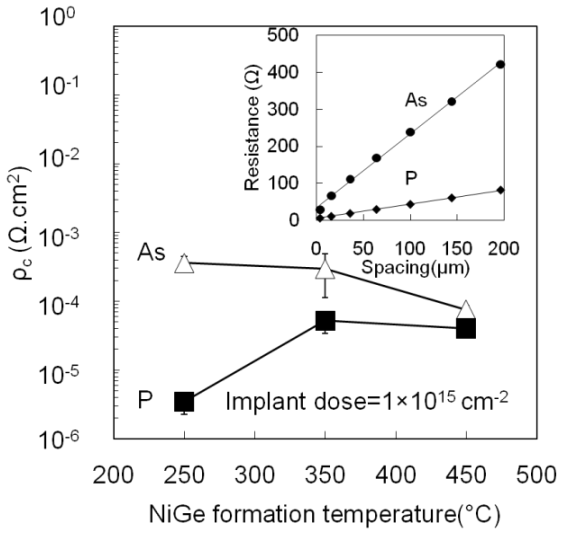


Figure 2.14: ρc versus NiGe formation temperature. TLMs patterned on P implanted samples have lower resistance compared with As implanted samples. The inset shows the resistance as a function of spacing for both cases.

Chui *et al.* reported higher active doses for P over As after a 500 °C RTA [61]. Activation of As at 500 °C is poor presumably due to unfavourable solubility and tendency to form clusters at this temperature. Following the same methodology as in [60] the active levels for the P implanted samples here are in the order of 3-6×10^{19} cm^{-3}, depending on the implant dose and energy. Higher active levels were achieved in [60] using a Ge pre amorphisation implant (PAI).

Table 2.2 represents ρ_c data, which to the best of our knowledge are currently in the public domain, relating to metal contacts on n-type doped Ge. Information regarding the contact material, dopant, and process conditions are listed therein.

Table 2.2: ρ_c values reported to date for n-type doped germanium.

Contact	Dopant	Method	Activation anneal (°C)	NiGe formation (°C)	ρ_c ($\Omega.cm^2$)	
NiGe	not specified	not specified	not specified	300	4×10^{-5}	[66]
NiGe	not specified	not specified	not specified	400	8×10^{-5}	
NiGe	not specified	not specified	not specified	500	6×10^{-3}	
NiGe	As	PAI+ II	600	250/330	5×10^{-4}	[67]
NiGe	As	PAI+ II	800(LSA)	250/330	4×10^{-5}	
NiGe	As	PAI+ II	900(LSA)	250/330	2.5×10^{-6}	
Al/Ti	P	II	650		6×10^{-5}	[68]
Al/Ti	Sb	II	LSA		7×10^{-7}	[69]
Al/Ti	P+Sb	Co-implant	500		8×10^{-7}	[70]
NiGe	P	II	500	250	3.46×10^{-6}	This work
NiGe	P	Two step II	600/350	350	3×10^{-8}	[49]
AgSb	P	In-situ	-	400	1.1×10^{-5}	[53]
NiGe	P/Sb	Co-implant	not specified	350	6.4×10^{-7}	[50]

Oh *et al.* [66] used TLM to extract ρ_c on n-type Ge, p-type Ge, n-type Si, and p-type Si, using NiSi and NiGe processes where n-type Ge was shown to be the most problematic system, producing the highest ρ_c. TLM structures were also used to extract ρ_c with Ti contacts on in-situ doped or implanted n-type Ge, as well as on SiGe [68]. In that work the 80% Si in-situ doped layer showed about two orders of magnitude lower contact resistivity compared to implanted Ge. Low $\rho_c=7\times10^{-7}$ $\Omega.cm^2$ was reported using a process with Al/Ti contacts on Sb-doped Ge combined with laser anneal (LSA) [69]. The same group recently reported $\rho_c=8\times10^{-7}$ $\Omega.cm^2$ using a 500 °C anneal to activate a P/Sb co-doped n+ region [70]. Alternative strategies involve NiGe combined with an As implant and LSA, or highly n-doped Si capping to reduce n-type Ge ρ_c [67]. In the NiGe part of that work, ρ_c decreases with increasing LSA temperature. $\rho_c< 2\times10^{-6}$ $\Omega.cm^2$ was reported using a 900 °C LSA. ρ_c is reduced by over 2 orders of magnitude switching from a 600 °C anneal to the 900 °C LSA. For both optimized processes in [69] and [67] diffusion control may be a concern as both As and Sb were shown to diffuse during LSA. A record low $\rho_c=3\times10^{-8}$ $\Omega.cm^2$ was recently achieved using two step P implantation prior to NiGe formation [49]. Using AgSb on epitaxially grown n-type Ge $\rho_c=1.1\times10^{-5}$ $\Omega.cm^2$ was obtained [53].

The lowest ρ_c we achieved in this work was 3.46×10^{-6} $\Omega.cm^2$ using a 1×10^{15} cm^{-2} 15 keV P implant, followed by a 500 °C activation anneal, 20 nm Ni, and 250 °C NiGe formation anneal. Material studies on Ni_xGe_y formation at different temperatures are reported in sec 2.7 as well as similar works by [37, 41]. It has been shown that at 250 °C there is a mix of NiGe, Ni_2Ge, and Ni_5Ge_3 which may be significant in achieving low ρ_c obtained in this work.

2.6.3 Discussion; Metal-Oxide-Semiconductor Devices

At this stage it is worthwhile to put the experimental ρ_c values into context, using the specs and definitions of future generation Metal-Oxide-Semiconductor (MOS) devices as set-down by the International Roadmap for Semiconductor ITRS Roadmap [71]. If R_{ON} is defined as the resistance of a transistor in on-state, then

$$R_{ON} = \frac{V_{dd}}{I_{dsat}} \qquad (2.\ 6)$$

where I_{dsat} is the drain current in saturation, and V_{dd} is the supply voltage. For example the High Performance (HP) devices in the 22 nm technology node target 2.188 mA/μm, with V_{dd}=0.9 V. Assume for now that the device width=1 μm, then R_{ON}=411.3 Ω. The resistance associated with a contact is:

$$R_{Contact} = \frac{\rho_c}{A_{Contact}} \qquad (2.\ 7)$$

where $A_{Contact}$ is the area of the contact. For our 1 μm wide device, $A_{Contact}$ is a direct function of the contact length in the direction of the current flow, and this is defined as 2× (MPU ½ pitch) [71]. For the 22 nm HP device this is 2× (32 nm), thus

$$R_{Contact} = \frac{\rho_c}{2\left(32\times10^{-7}\times1\times10^{-4}\right)}\Omega \qquad (2.\ 8)$$

In this exercise we vary ρ_c and calculate $R_{Contact}$ for HP devices in the 22, 20, 18, and 17 nm technology nodes, and for the Low Operating Power (LOP), and Low Standby Power (LSTP) devices in the 22 nm technology node.

In the targeted device we initially assume

$$R_{Contact} << R_{ON} \tag{2. 9}$$

For a device with highly resistive contacts we recalculate:

$$R_{ON}^{*} = R_{ON} + 2R_{Contact} \tag{2. 10}$$

thus

$$I_{dsat}^{*} = \frac{V_{dd}}{R_{ON}^{*}} \tag{2. 11}$$

For simplicity we normalize I_{dsat}*, with respect to the targeted I_{dsat} to determine at what stage ρ_c becomes significant in the overall performance of the device,

$$\frac{I_{dsat}^{*}}{I_{dsat}} = \frac{R_{ON}}{R_{ON}^{*}} = \frac{R_{ON}}{\left(R_{ON} + 2R_{Contact}\right)} \tag{2. 12}$$

Thus the drop in I_{dsat} can be calculated as a function of $R_{Contact}$ and also ρ_c.

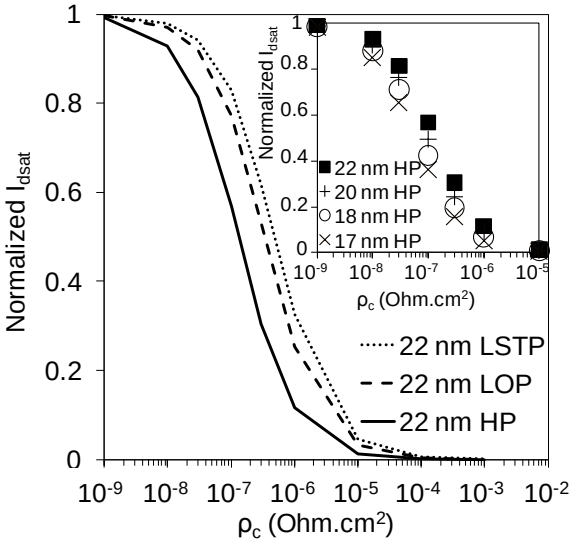


Figure 2.15: Calculated normalized I_{dsat} vs ρ_c for HP, LOP, and LSTP devices in the 22 nm technology node, with specs taken from the ITRS Roadmap. The inset shows the same graph for HP devices in the nodes between 22 and 17 nm.

Figure 2.15 shows the resulting normalized I_{dsat} versus ρ_c for the various technologies and device options. As one expects the current drive drops with increased ρ_c. In general the effect is more significant for scaled technologies, and for HP devices, where the targeted R_{ON} is more aggressive (*i.e.* lower). A 10 % drop in drive is associated with $\rho_c \sim 10^{-8}$ $\Omega.cm^2$ in the 22 nm HP device, and with $\rho_c \sim 10^{-7}$

$\Omega.cm^2$ in the corresponding LOP and LSTP devices. It is obvious ρ_c needs to be in the order of 10^{-7} $\Omega.cm^2$ and below to avoid R_{ON} being dominated by the contacts.

In the next section we examine the effect of LTA for NiGe contact formation, and systematically compare the results with conventional RTA, considering surface topography, interface quality, crystal structure, material stoichiometry, specific contact resistivity, and thermal stability.

2.7 NiGe contacts made by Laser Thermal Anneal

2.7.1 Experimental procedure

Figure 2.16 summarizes the process flow undertaken in this study. After cleaning, high-resistivity (>40 Ω.cm) n-type (100) wafers received well implants to create a semi-insulating layer. The wafers then received a shallow P implant with the dose of 1×10^{15} cm^{-2} and energy of 12 keV. This was performed through a native oxide, and should amorphize approximately to a depth of 25 nm. Dopant activation was performed using an RTA at 500 °C for 10 s in an N_2 ambient. It seems that 500 °C is an optimum annealing temperature for n-type dopants, as lower temperatures (e.g. 400 °C) result in poor sheet resistance and activation, whereas at higher temperatures (e.g. 600 °C), diffusion is a concern. Thereafter 20 nm of Ni was deposited using thermal evaporation. Many works to date have studied germanide formation with Ni thicknesses in this range. Transfer length method (TLM) patterning and mesa dry etch was then carried out to minimize leakage currents. The Ni layer was patterned by a standard lift-off technique. It's worth noting that laser light can be reflected by metal layers [72]. For the thickness of Ni in this work (20 nm) the reflection difference is not expected to have a significant effect.

The only variable in the process was the NiGe formation anneal. One set of samples received RTA treatment either at 250, 275, 300, 325 or 350 °C in N_2 for 30 s. Another set of samples received LTA processing (λ= 308 nm, single-pulse) at Excico with laser densities ranging from 0.25-0.55 J/cm^2 and time durations ranging from 144-165 ns. The laser beam area was approximately 10×10 mm^2. Note, these energy densities are significantly lower than those required for proper LTA assisted dopant activation in Ge [73]. The melting threshold was characterized by visual

observation (surface color change) on test samples prior to the processing of these experimental samples.

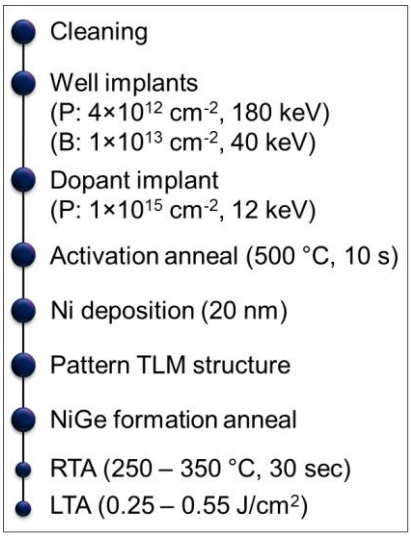


Figure 2.16: A summary of the experimental process flow in this study.

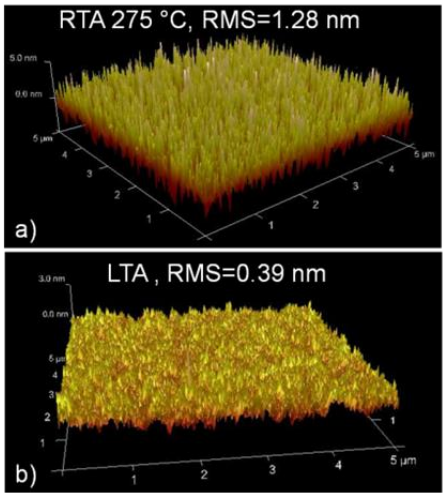
According to SRIM, a 1×10^{15} cm^{-2} 12 keV P implant into Ge should produce a junction depth ~55-60 nm deep, even with a diffusionless anneal, so the germanide layers in this work should still be contained in the n-doped region.

Various material characterization techniques were applied to inspect surface topography and crystalline quality of the germanide layers. Top-down SEM was performed on same tool as in section 2.6.1. AFM was performed in tapping/non-contact mode at room temperature on $5\times5\mu m^2$ scanning area. XTEM imaging was carried out using the JEOL 2100 high-resolution TEM under bright field conditions. Scanning TEM (STEM) imaging and *Energy-dispersive X*-ray spectroscopy (EDX) line scan analysis was undertaken using the Helios Nanolab system equipped with Oxford Instruments X-Max-80 EDX detector with spot size well below 1 nm. The analysis was conducted at 30 kV using moderate beam currents. For electrical characterization TLM was used to extract ρ_c. X-ray diffraction (XRD) was done in symmetric θ°-2θ° mode using PANalytical X'pert pro diffractometer (Cu Kα radiation λ=1.540598 Å). Similar equipment was used as in 2.6 for electrical characterization. Furthermore, the LTA process was simulated using the enthalpy model described in [74]. This approach allows the modelling of light coupling, heat diffusion and Ge melting. It does not take into account the effects of stoichiometry change during germanide formation.

2.7.2 Results of the material characterisation

In order to study the effects of RTA and LTA, first surface roughness and continuity of the layers was evaluated by top-down SEM and AFM. In both cases continuous layers were formed with no evidence of breakages.

Figure 2.17 shows representative AFM images of the surface topography which were formed by (a) RTA at 350 °C and (b) LTA at the energy of 0.35 J/cm^2. Table in the Figure 2.17 shows the Root mean square (RMS) data extracted for all the samples. RMS is larger for the RTA set, except for the highest ED LTA. Much like there is a process window for NiGe formation by RTA [39, 40] where at high temperatures the thin film agglomerates into islands, this data indicates that LTA also has a process window for germanide formation above which the film degrades. 0.55 J/cm^2 is clearly too high for this application.



Formation Anneal	Roughness (nm)
250 °C	1.11
275 °C	1.28
300 °C	1.55
325 °C	1.47
350 °C	1.74
0.25 J/cm^2	0.4
0.35 J/cm^2	0.39
0.45 J/cm^2	0.62
0.55 J/cm^2	2.07

Figure 2.17: Representative AFM images of NiGe layers formed by (a) RTA at 350 °C and (b) LTA at the energy of 0.35 J/cm^2. The table shows the surface roughness data for all the RTA and LTA samples in this work.

Mazzocchi *et al.* also reported a change in AFM RMS versus ED in their LTA dopant activation study in Ge, which was attributed to the transition from non-melt, to sub-melt, to melt conditions [73].

Figure 2.18 depicts SEM images comparing a) one RTA sample after RTA at 500 °C where agglomerated NiGe is formed, and b) one LTA sample after 0.35 J/cm^2 ED. From the scale bars it is evident that LTA gives has much smoother surface.

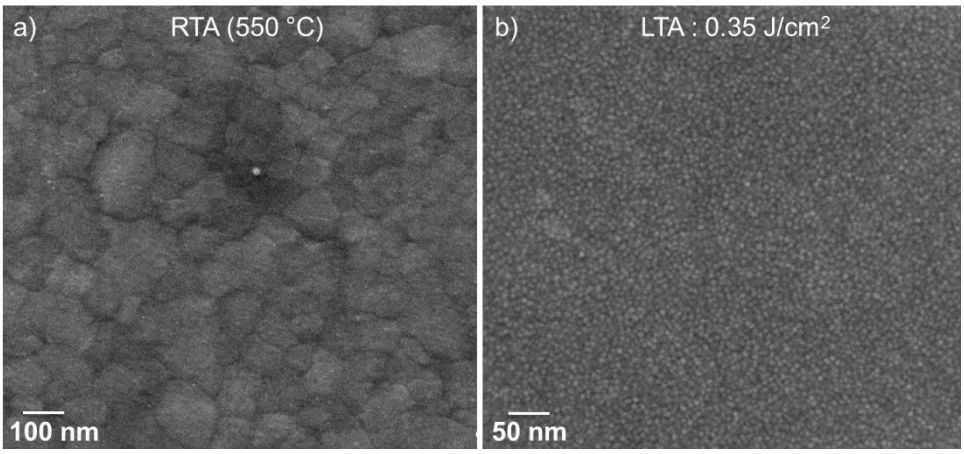


Figure 2.18: Representative SEM images of the a) sample annealed at 500 °C RTA and b) subjected to LTA at 0.35 J/cm2.

Representative XTEM images from a germanide contact formed by a) RTA at 350 °C for 30 s in N_2, and b) LTA at 0.45 J/cm^2 are shown in Figure 2.19.

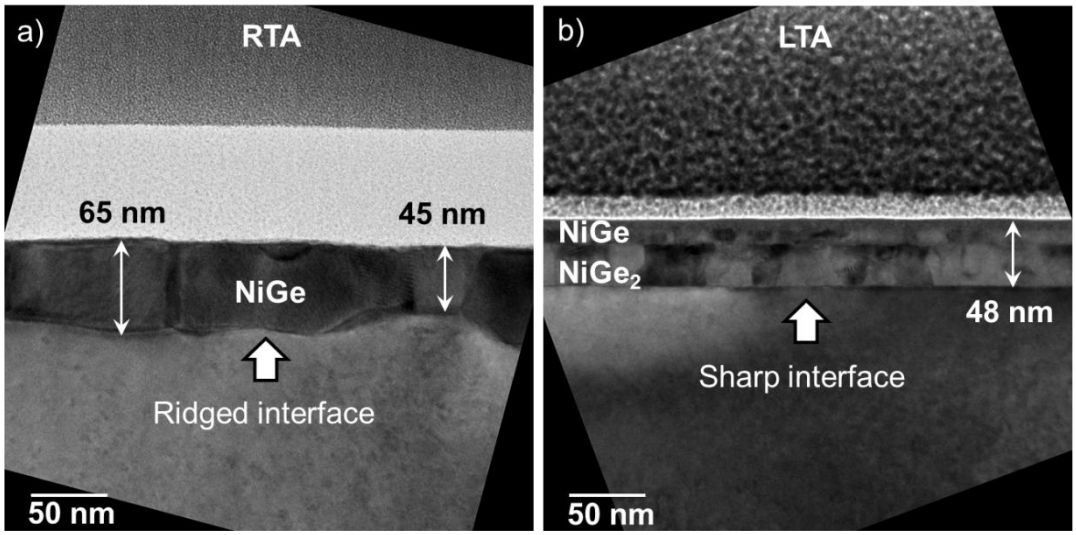


Figure 2.19: Representative XTEM images of NiGe layers formed by (a) 350 °C RTA and (b) formed by 0.45 J/cm^2 LTA.

The LTA process resulted in germanide formation having sharp interface with the underlying Ge substrate. In stark contrast, the germanide layer formed by RTA exhibited a rough and ridged interface with the Ge substrate with larger crystalline domains. This is nothing new, as non-smooth NiGe interfaces are commonplace when RTA is used for the formation anneal [42, 46, 75].

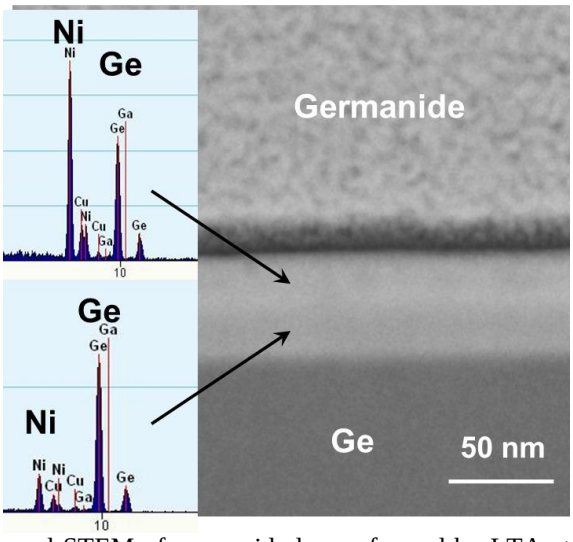


Figure 2.20 : EDX data and STEM of germanide layers formed by LTA at 0.45 J/cm^2, identifying $NiGe_2$ in the lower portion of the germanide layer.

Additionally, the germanide layer formed by LTA showed two definite sub-layers with different stoichiometries identified by EDX line scans using a tightly focused electron probe. The quantification of the obtained EDX spectra (Figure 2.20) showed the existence of a $NiGe_2$ layer in contact with Ge covered by a NiGe surface layer. The germanide layer formed by RTA was identified as NiGe across its whole thickness.

The germanide-substrate interface was studied at lattice resolution with the corresponding HRTEM images shown in Figure 2.21. Note Figure 2.21 a) and b) are from the same LTA sample but at different locations along the surface. Figure 2.21 a) shows two grains of the $NiGe_2$ phase and the corresponding interface with the (001) oriented Ge substrate. The lattices for both $NiGe_2$ domains show some epitaxial relation.

Several stacking fault defects along the (111) set of planes were observed in the Ge substrate as well as at the boundary between $NiGe_2$ domains. In comparison, Figure 2.21 b) demonstrates a case where $NiGe_2$ grains have no clear epitaxial alignment with the underlying (001) Ge substrate despite the fact that a very sharp interface is formed. In this regard, the interface between the two layers is effectively atomically flat. Lim *et al*. [76] argued that epitaxial $NiGe_2$ on (001) Ge, although not thermodynamically favourable, may form as a result of minimization of the interfacial energy. Lattice-matched NiSi growth on Si has been reported by Gao *et*

al., where ultra-thin Ni layers were deposited on Si [77], and $NiSi_2$ preferentially formed as it has a similar lattice spacing to Si. In contrast, the lattice resolution TEM images of the NiGe/Ge interface for the RTA treated sample revealed a corrugated surface far from being fully relaxed (Figure 2.21 c)).

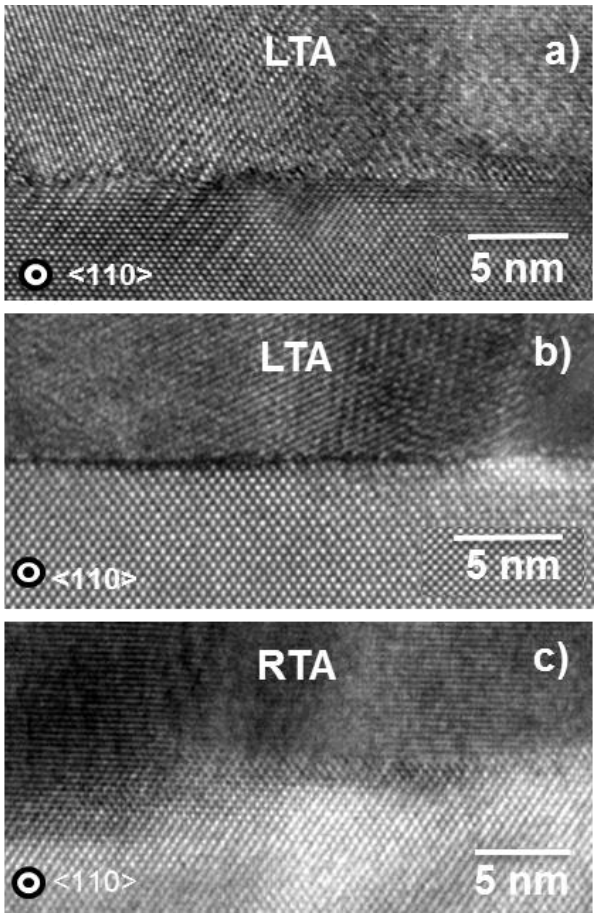


Figure 2.21: a) and b) representative HRTEM images from the interface between Ge and the Ni-germanide after LTA 0.45 J/cm^2, and c) RTA at 350 °C.

Nevertheless epitaxial alignment of the (111) set of planes of NiGe to the (001) planes of the Ge substrate was identified. A large amount of residual strain has been observed by HRTEM lattice imaging. There is a lattice mismatch between NiGe and Ge which can be a cause of the residual strain as no Ge lattice defects are observed and the number of grain boundaries in the NiGe layer is relatively small. This is in contrast to the LTA sample where both Ge lattice defects and larger number of grain boundaries help $NiGe_2$/Ge interface to relax.

Herein we outline the importance of thorough structural examination of the germanide-substrate interface properties in relation to the obtained contact resistance. Moreover the stark difference in the structure of the germanide layers

obtained by LTA and RTA is a result of a fundamentally dissimilar formation pathway.

Figure 2.22 shows a representative TEM image from a sample subjected to LTA at the energy of 0.55 J/cm^2 where polycrystalline Ni_xGe_y with ridged interface is formed. The relatively rough surface of the contact is also visible in the Figure 2.22 a). It was confirmed earlier from AFM measurements that surface morphology is deteriorated after 0.55 J/cm^2 LTA. Figure 2.22 b) shows a zoom in view of the interface where defects and the interface are visible.

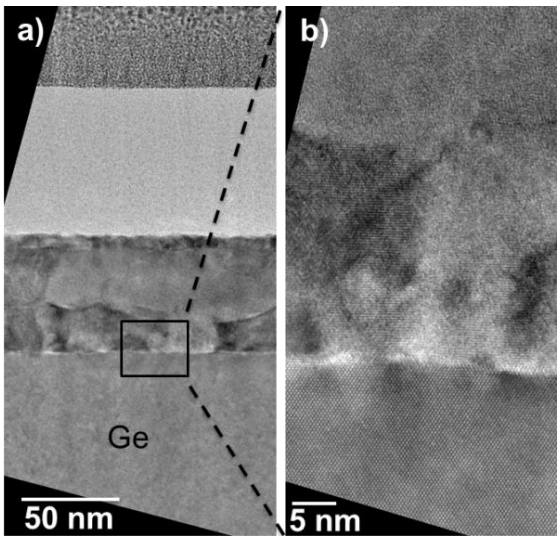


Figure 2.22: representative HRTEM images from the interface between Ge and the Ni-germanide after LTA 0.55 J/cm^2.

The explanation for the huge improvement in interface roughness observed in Figure 2.21 is linked to the thermal gradient and shallow heat distribution associated with ultra-short-pulse LTA. Using a simple enthalpy model, we could simulate the thermal dynamics during the LTA process, taking standard values for Ni and Ge optical and thermal properties. It should be noted that within this simple approach, the effect of germanide formation on thermal and optical properties is not taken into account. Most of the UV laser light is absorbed within less than 10 nm in Ge during the sub-µs timescale of the laser pulse. This surface layer acts as a heat source, which diffuses in depth over time.

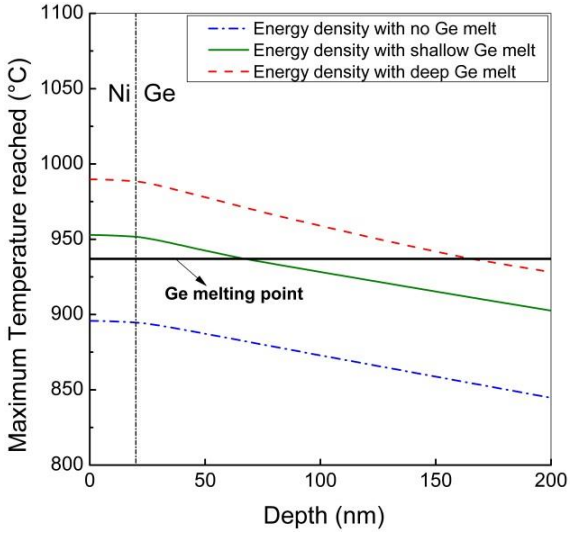


Figure 2.23: Simulated maximum temperature reached as a function of depth for the applied LTA energy densities. The ED values used for simulation are 0.4, 0.45 and 0.5 J/cm² for the non-melt, shallow Ge melt and deep Ge melt, respectively. We acknowledge EXCICO for the modelling work.

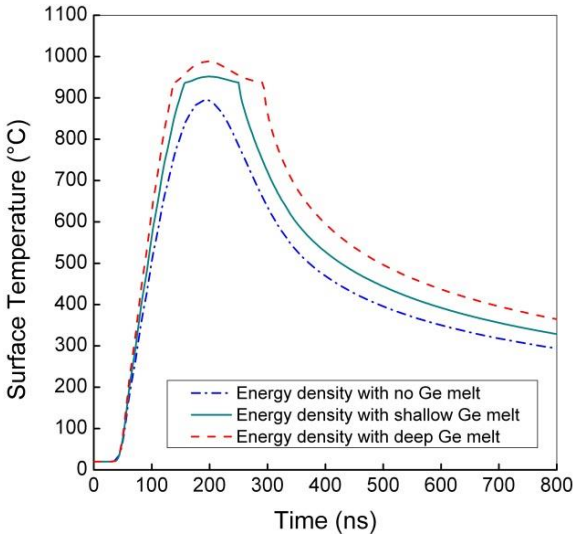


Figure 2.24: Simulated surface temperature as a function of time for the applied LTA energy densities. The ED values used for simulation are 0.4, 0.45 and 0.5J/cm² for the non-melt, shallow Ge melt and deep Ge melt, respectively. We acknowledge EXCICO for the modelling work.

In Figure 2.23 the maximum temperature reached during the process is shown as a function of depth for LTA process conditions corresponding to non-melt, shallow melt and deep melt regimes. The melted depth (where temperature is greater than the Ge melting temperature of 937 °C) increases with the LTA energy density. As it can be seen, the simulated thermal gradient is very high, close to 300 °C/µm, which limits the effect of the laser anneal to the near surface region.

In Figure 2.24, the corresponding surface temperature dynamics are reported. As is shown in the figure, the high temperature regime is sub-µs. Especially, the melting time is typically less than a few hundred ns. Within this timeframe, most of the Ni and Ge inter-diffusion mechanisms are expected to take place in the *liquid* phase, during melt and recrystallization of the Ge and germanide regions. As the melting temperature of Ni is 1455 °C, these simulations indicate that the Ni layer remains in solid form.

The ED values used for simulation are 0.4, 0.45, and 0.5 J/cm² for the non-melt, shallow Ge melt and deep Ge melt, respectively. The corresponding melt depth simulated for 0.4, 0.45, and 0.5 J/cm² are about 0, 50, and 150 nm respectively.

However, the germanide depth extracted from the TEM are much shallower in this ED range (<70nm). This discrepancy may be due to the impact of the NiGe layer optical and thermal properties which change during the process, and are not taken into account dynamically in this simple approach. Moreover, it is possible that diffusion dynamics are slower than the melting and recrystallization dynamics (sub-µs timescale), which would lead to a germanide thickness smaller than the melted depth. More advanced studies would be required to understand the germanide formation mechanisms for such an ultrafast process.

Note, in the conventional RTA case, the entire sample is essentially at the target temperature without significant thermal gradients, and the growth of germanides involves a solid-solid reaction.

Much work has been devoted to understanding the effect of the liquid to solid phase transformation on impurity behaviour and solubility. Distribution coefficients have been explored since the early days of semiconductor processing, and are essentially a measure of solubility. The equilibrium distribution coefficient, k, is defined as the relative tendency of various impurities to dissolve in solid materials. In other words, k is the ratio of concentrations: C_{SOLID}/C_{LIQUID}, at the melting point of the material. In Trumbore's review paper [78], which contains a vast amount of data for impurity solubilities in Si and Ge, $k = C_{SOLID}/C_{LIQUID} = 3\times10^{-6}$ for Ni in Ge. Hence the solubility of Ni in Ge is vastly greater in the liquid Ge phase, compared to the solid Ge phase.

Strictly speaking this value is for equilibrium conditions, but it is reasonable to state for the LTA case here. Ni is in contact with liquid Ge and thus rapidly dissolves into that layer. In effect the liquid Ge consumes the Ni on top very quickly, and the resulting Ni-germanide phase is determined by the ultra-fast reaction quenching.

By changing the ED of the LTA process the surface melt depth can be controlled (Figure 2.23). The result of this is having a different thickness of liquid Ge in contact with the Ni over layer. Consequently the thickness of the obtained germanide layer scales with LTA ED as shown in Figure 2.25.

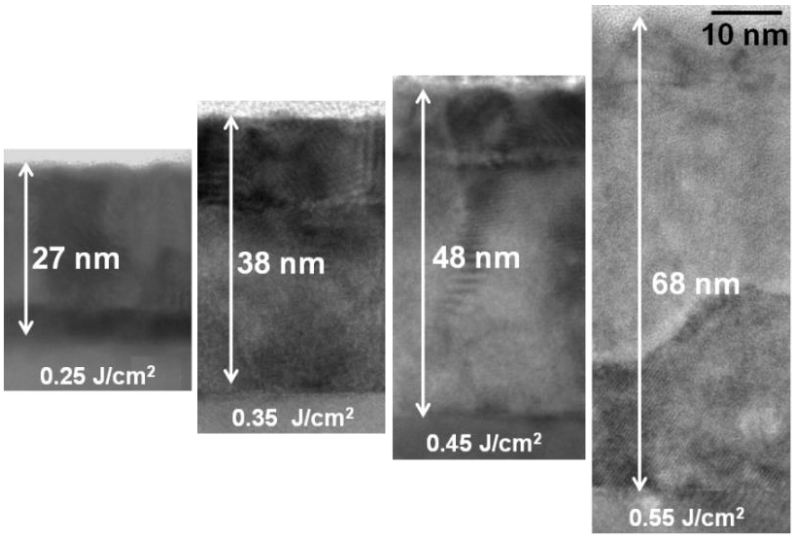


Figure 2.25: XTEM images of Ni-germanide layers obtained at the corresponding laser energy densities.

XRD analysis was carried out to identify crystal phases of the germanide formed during the RTA and also the LTA process.

Figure 2.26 shows XRD diffraction pattern of germanide layer formed by LTA at 0.35 J/cm^2 along with the main Ni_xGe_y crystal phases available in crystal reference patterns. As is seen in the figure it is clearly a complex system.

In order to specify the crystal phases and corresponding indexing of the reflections each XRD data was compared with the reference patterns in the database to find the proper match to each reflection. Figure 2.27 shows XRD patterns of germanide layers formed by RTA at temperatures ranging from 250-450 °C with corresponding indexing of reflections, based on orthorhombic NiGe phases (pbnm

space group, a=5.81, b=5.83, and c=3.42). For reference one unannealed Ge sample was also checked by XRD.

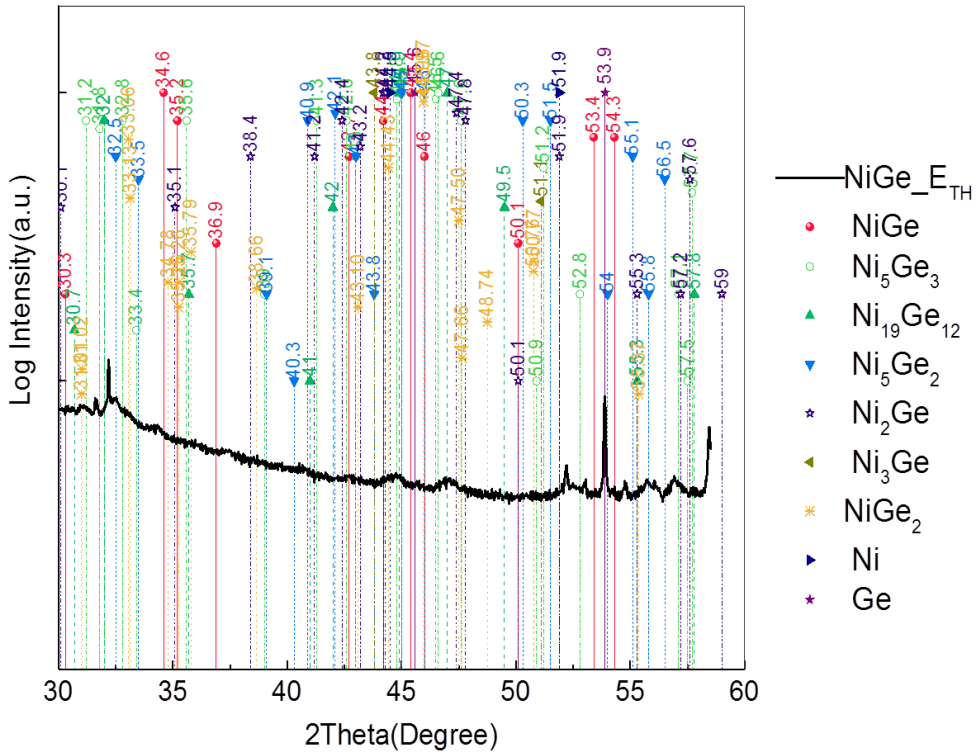


Figure 2.26: X-ray diffraction patterns of germanide layers formed by LTA at 0.35 J/cm^2 with the data base of different crystal phases of the possible NiGe alloy.

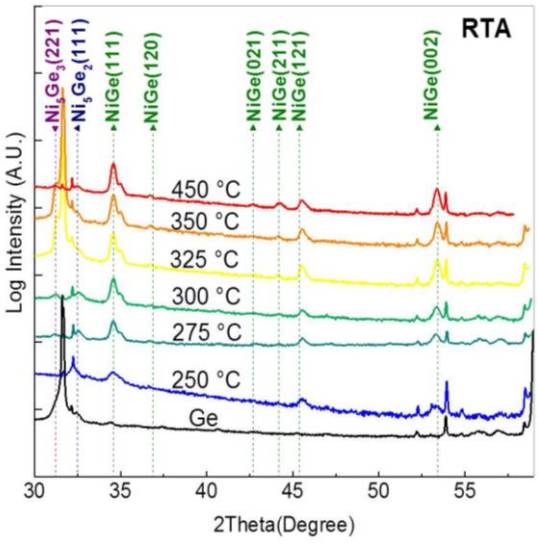


Figure 2.27: XRD patterns of germanide layers formed by RTA at 250- 450°C. For comparison one unannealed Ge sample was also check by XRD.

From the intensities of the RTA samples one can conclude that germanide layers are dominated by the NiGe phase with appearance of Ni-rich germanides such as Ni_5Si_2 and Ni_5Ge_3. The obtained results are in good agreement with the θ-2θ

patterns of the NiGe JCPDS standard [79] and also other published reports on NiGe formation by RTA [41, 75, 80]. Ni-rich germanide phases were also observed during thermal treatment of 50 nm Ni layers on Ge [81].

Figure 2.28 shows XRD patterns for LTA at 0.45 J/cm^2 and RTA at 350 °C samples, with the corresponding indexing of the reflections, based on orthorhombic $NiGe_2$ and NiGe phases ($NiGe_2$ Cmca space group, a = 10.83, b = 5.76 and c = 5.76; NiGe pbnm space group, a = 5.81, b = 5.38 and c = 3.42). $NiGe_2$ phase was reported in XRD analysis of LTA treated samples [76].

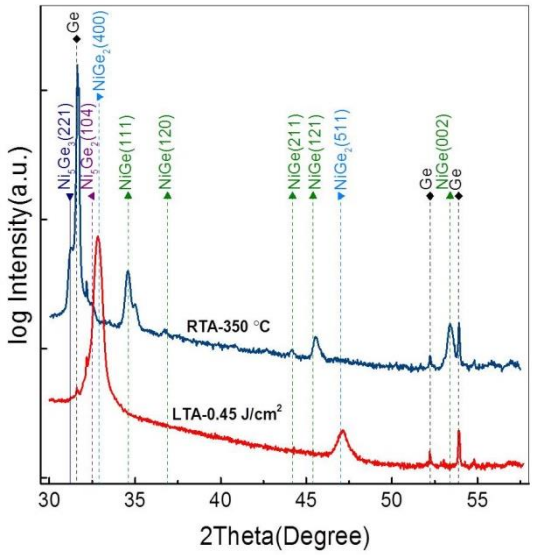


Figure 2.28: XRD patterns of germanide layers formed by LTA at 0.45 J/cm^2 and RTA at 350 °C.

In XRD measurements the intensity of the peaks is influenced by the quality of the measured layer. In RTA samples the germanide is created in the form of relatively large crystalline domains which results in detectable XRD patterns during the measurement. The germanide layers formed by LTA were very thin and polycrystalline. Thus the observed peak were of very small intensity and in some cases broad making it difficult to accurately determine the crystal phase of the germanide layer.

The $NiGe_2$ phase obtained in the LTA process does not appear in the crystal phase diagram of the Ni-Ge system in equilibrium (see Figure 2.29) indicating that $NiGe_2$ phase might have been an non-equilibrium unstable crystal phase in the system.

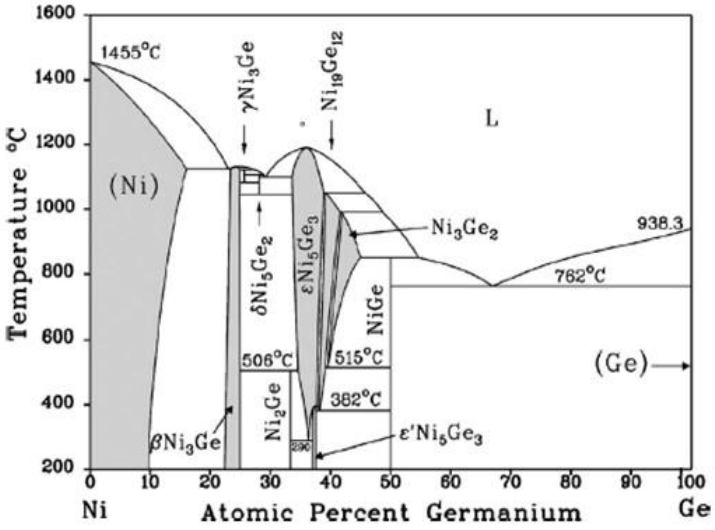


Figure 2.29: Binary phase diagram of the Ni-Ge system. Copyright 2006 American Institute of Physics [82].

2.7.3 Results of the electrical characterization

Using the TLM test structures fabricated, ρ_c of the germanide/n-type Ge interface and the sheet resistance R_{sh} of the underlying P doped Ge layer were then extracted. Approximately 40 TLM structures within each array were electrically measured in order to extract reliable values for ρ_c

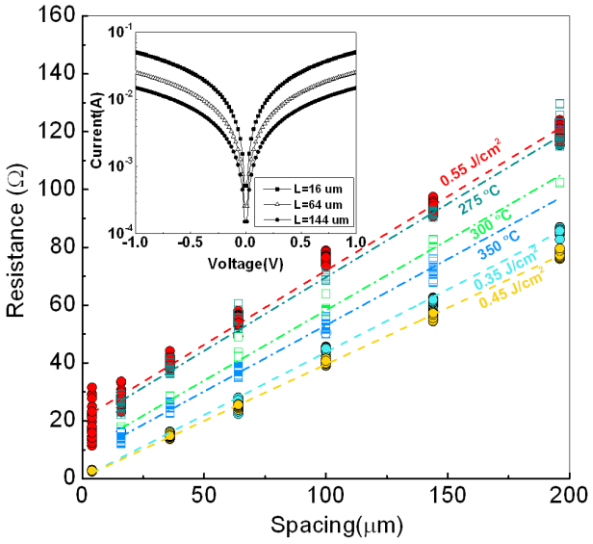


Figure 2.30: Resistance versus contact spacing for LTA and RTA samples. The inset shows I-V characteristics of a typical TLM structure where the germanide contacts were formed by LTA with the energy of 0.45 J/cm^2.

Figure 2.30 depicts the typical output from a TLM measurement. The inset shows current versus voltage as a function of contact spacing of a typical TLM

structure fabricated using LTA (0.45 J/cm^2). The resistance between contacts increases as the spacing increases. In the main part of the Figure 2.30 resistance versus contact spacing is plotted for the germanide formed by RTA at 275°, 300°, 350 °C and LTA at 0.35, 0.45, and 0.55 J/cm^2. As is seen straight lines are fitted to the data. Intercepts of the line with vertical and horizontal axes are used to calculate ρ_c and R_{sh} according to theory in section 2.6.

Table 2.3 shows the results of ρ_c and R_{sh} extracted from all the TLM measurements. In the RTA samples R_{sh} and ρ_c decrease as the formation temperature increases from 275 to 350 °C, except at 325 °C for which we do not have a physical explanation at present. In an overall sense, the RTA samples produce $\rho_c > 10^{-4}\ \Omega.cm^2$.

Table 2.3: R_{sh} and ρ_c values for germanide contacts formed by RTA and LTA.

Contact formation	R_{sh}(Ω/sq)	ρ_c (Ω.cm^2)
275 °C	196.1	6.31×10^{-4}
300 °C	186.0	1.61×10^{-4}
325 °C	216.3	9.57×10^{-4}
350 °C	169.0	1.35×10^{-4}
0.35 J/cm^2	163.6	1.38×10^{-6}
0.45 J/cm^2	147.9	2.84×10^{-7}
0.55 J/cm^2	192.0	8.34×10^{-4}

In general R_{sh} and ρ_c are lower in the LTA samples. The best ρ_c value is $2.84 \times 10^{-7}\ \Omega.cm^2$ obtained for the TLM sample annealed at 0.45 J/cm^2, while $\rho_c = 1.33 \times 10^{-6}\ \Omega.cm^2$ produced by 0.35 J/cm^2 is also a significant result. These ρ_c values are 2-3 orders of magnitude lower than the equivalent RTA cases. It should be stressed again that the only process variable in this experimental work was the germanide formation anneal. It is interesting to see that increasing the LTA energy density to 0.55 J/cm^2 results in higher ρ_c. This could be attributed to the degradation of the interface quality (see Figure 2.22).

Based on previous work we estimate the active doping concentration on the order of $3-6 \times 10^{19}$ cm^{-3}, depending on the amount of P snowploughed by the growing germanide layer, on how much Ge is consumed, and on how much the germanide formation anneal boosts or detracts from the initial activation level.

It is well-known that ρ_c is a strong function of active doping in the substrate below the contact, thus any boost in dopant activation will yield a similar improvement in ρ_c. One might argue in this case for the 0.35 and 0.45 J/cm^2 LTA cases that the LTA is merely improving the P activation which is generating these ρ_c results. Indeed if one looks at Table 2.3, it does seem that the R_{sh} values indicate LTA is a benefit for P activation. However, if ρ_c versus R_{sh} is plotted, as is shown in Figure 2.31, one can immediately see that for a *fixed* R_{sh} LTA can still produce better ρ_c, if the correct energy density condition is selected. The extracted standard deviation for each ρ_c (error bars in this graph) shows that at very low ρ_c the accuracy of the data is reduced.

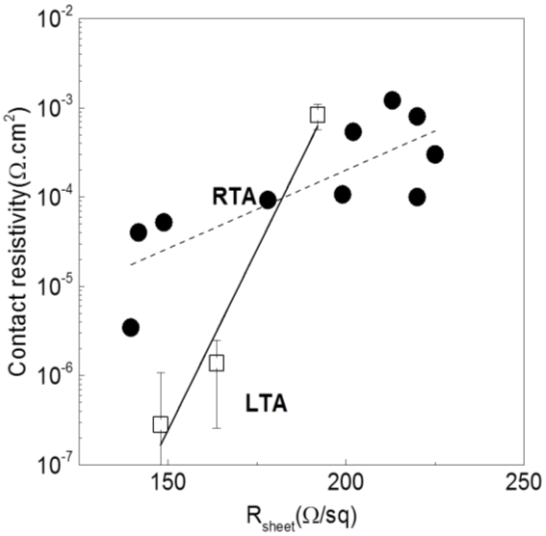


Figure 2.31: ρc versus Rsh for all the samples in this work, as well as those from our previous NiGe on n-type Ge work using RTA (sec 2.6). For a fixed Rsh LTA can produce better ρc, if the correct energy density condition is selected.

Note in Figure 2.31, data points from our previous experiments on germanide formation by RTA are included for completeness [83]. Based on the divergent trend-lines it is argued here that LTA benefits ρ_c not only by boosting dopant activation, but by also improving the quality of the germanide-Ge interface. The latter could be responsible for reduced FLP, as reported by Lim *et al.* [57].

In the final part of this work, thermal stability of the germanide layers is explored. The ultra-short time and highly-localized energy densities of LTA processing may form highly non-equilibrium metastable conditions in the semiconductor materials and substrates. If this is the case thermal budget in the processes that come after the LTA process step, may cause any metastable

condition revert back to a more equilibrium state. In order to evaluate germanide thermal stability one sample prepared at 300 °C RTA and one sample prepared by 0.45 J/cm^2 LTA were subjected to "post-processing" RTA treatments from 100-500 °C. The anneal times were 30 s each. Only one sample was post-processed for both RTA and LTA so one should consider the post-processing thermal-budget in this study as cumulative. Figure 2.32 a) shows the TLM measurements of the LTA sample after post-processing. The slope and intercept of the fitted lines change after each RTA treatment, indicating that R_{sh} and ρ_c are deteriorated. Figure 2.32 b) shows a SEM image taken from the sample after the annealing process where agglomerated NiGe alloy is visible.

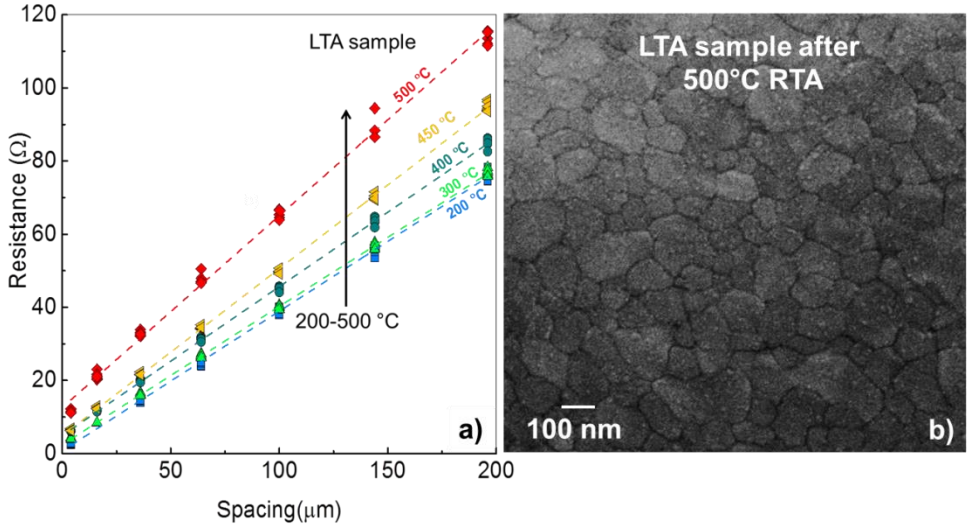


Figure 2.32: a) Resistance versus contact spacing after post-processing treatments. The anneal times were 30 s. b) SEM image of the sample after the annealing process.

Extracted ρ_c results are shown in Figure 2.33. In the LTA sample ρ_c increases gradually, and at 250 °C there is a significant increase in resistivity. By 500 °C the ρ_c value is similar to the RTA cases. In the RTA sample ρ_c shows a slight decrease at 150 °C and then follows an increasing trend. Both samples were inspected by SEM (data not shown), and it was observed at the end of this post-processing anneal sequence that the germanide had agglomerated, which may explain the erratic ρ_c trends for >400 °C post-processing. It is well known that germanide layers annealed at 500 °C become agglomerated [39, 40].

There are various existing methods to alter thermal stability of silicide or germanide layers. Thermal stability of the germanide layer was studied by Park *et*

al. by introducing Ta to the deposited Ni layer. The germanide layers showed a slightly improved stability upon formation of a Ta rich layer on top of NiGe that suppressed agglomeration at temperatures up to 600 °C [84]. Deposition of a thin layer of Pt on top of Ni was used to form $Ni_{1-x}Pt_xGe$ alloys thermally stable up to 550 °C [85]. Adding an intermediate Ti layer either before or after Ni deposition improved the germanide stability due to formation of ternery $Ni_{1-x}Ti_xGe$ near NiGe layer [86]. One recent report highlighted the benefit of co-sputtering Ni and Pt prior to alloy formation [87]. Incorporation of Pd in to NiGe using $Ni_{0.95}Pd_{0.05}$/TiN structure hindered agglomeration and oxidation, hence contact thermal stability was improved [88]. Yb has also been reported to be effective for same purpose [89].

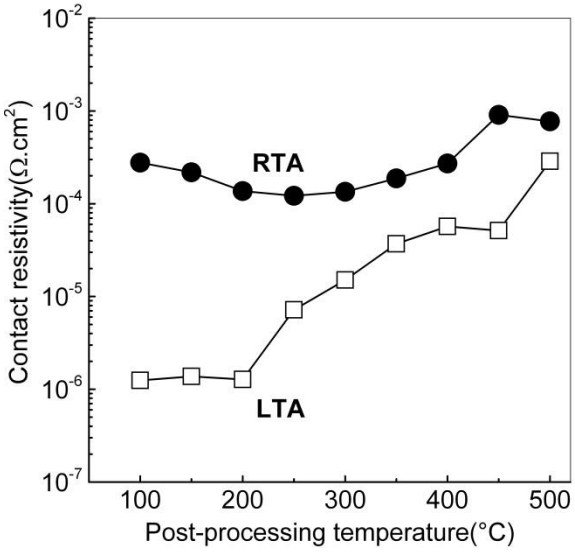


Figure 2.33: ρc versus post-processing RTA treatments. Only one sample was post-processed for RTA and for LTA so one should consider the post-processing thermal-budget as cumulative.

2.8 Conclusion

In this chapter we extracted ρ_c of NiGe on n-type Ge from TLM structures considering different dopants and implant doses. The lowest contact resistivity obtained was 3.46×10^{-6} $\Omega.cm^2$ using a 1×10^{15} cm^{-2} 15 keV phosphorus implant, followed by a 500 °C activation (optimum annealing temperature in terms of activation and diffusion), and a 250 °C NiGe formation anneal. It is shown that higher implant dose leads to lower ρ_c. Also, P and As were compared in terms of R_{sh} and ρ_c, and it was observed that P yields lower R_{sh} and ρ_c. As activation at 500

°C is poor presumably due to unfavourable solubility and tendency to form clusters at this temperature.

Moreover, the quality of germanide contacts formed by state-of-the-art LTA was investigated and compared systematically with RTA. LTA resulted in smoother layers of germanide, mainly NiGe and $NiGe_2$ with some epitaxial relation with the underlying Ge. The germanide-substrate interface was incredibly sharp without any detectable interfacial region or transition zone in HRTEM. Simulations indicated that the LTA melts a surface Ge layer, causing a liquid-solid reaction with the overlying Ni. The best contact resistivity obtained in this study was 2.84×10^{-7} $\Omega.cm^2$. Thermal stability of contacts formed by RTA and LTA was also compared.

Future work in this field should include more ρ_c studies around 250-300 °C formation anneal, also without dopant activation anneal before NiGe formation and investigation of implantation through silicide (germanide) techniques. In case of using LTA to make germanide contacts it is imperative to explore solutions to improve thermal stability of contacts created by this approach.

Chapter 3

N-type Dopant Studies

3.1 Introduction

Indeed many obstacles and challenges need to be addressed before Ge can become a channel material in advanced CMOS technology. Realization of n-type ultra-shallow junctions with highly activated dopants in order to maintain low access resistance is a well-known roadblock in this journey. Meanwhile the relatively small band gap (0.67 eV) of Ge raises difficulties to minimize the leakage current in pn junctions [24]. In fact many people doubt Ge because leakage is too high. In addition, it seems indispensable to come up with practical solutions in order to control Ge desorption and dopant loss. This emphasizes the need for novel techniques and approaches for doping the semiconductor and the subsequent annealing and fabrication steps.

In this chapter we investigate the influence of laser annealing on dopant activation and provide insight into the leakage problem and suggest practical solutions. Then we study F behaviour and its effect as a co implant in Ge. We close this chapter by a short discussion on Ge desorption and its correlation to the dopant loss phenomenon.

3.2 Doping and annealing methodologies

The incredible evolution of CMOS technology over the last decades has been accompanied by the emergence of numerous approaches for introducing impurities into Si and activating them. Among all, ion implantation (at room temperature) is of course the industry most conventional method [90]. Cryogenic implants where the substrate is at very low temperatures e.g. -60 or -100 °C during the implantation process have been proven to provide higher activation levels, more shallow

junctions, as well as lower leakage current. Due to the low temperature process, cryogenic implants cause greater amorphisation so end-of-range (EOR) damage is less.

Another alternative are hot implants reported to be effective upon reduction of implant induced damage during implantation [91-93]. It is well established that specific co-implants such as C, F, and N are beneficial through interactions with interstitials and vacancies that are responsible for dopant diffusion and deactivation during the rapid thermal anneal [18]. Plasma doping is another advanced doping technique which allows high dose applications as well as relatively better conformal doping that is a fundamental requirement for non-planar FinFET architectures [94]. Vapour phase doping has also been used to introduce and activate high concentrations of P and As into Si [95]. Furthermore molecular layer doping is proposed as a novel method enabling conformal non-destructive doping in aggressively scaled semiconductor devices [96]. Spin-on-dopant has also been used for shallow junctions formation in Si [97].

In Ge processing, it can be well said that ion implantation has been the most common technique being used so far. Recently other doping techniques were applied on Ge like gas phase doping [98], plasma doping [99], and molecular layer deposition [100]. Cryogenic B implantation in Ge has been reported to effectively control junction depth and boost the level of activated dopants [58]. Co-implants in Ge have been demonstrated under certain circumstances, however they don't seem to be as effective as in Si [17].

Ge crystal lattice is more likely to be amorphized than Si. So an annealing step is needed to re-grow the damaged crystal, incorporating the impurities in substitutional sites in the lattice, and electrically activate them. This is where the challenge starts. N-type dopants tend to diffuse very quickly via a vacancy-mediated mechanism [101], leading to deep doping profiles. More over these elements exhibit low activation levels compared to p-type dopants. This is not acceptable for what is determined in ITRS roadmap where highly activated dopants ($> 10^{20}cm^{-3}$) and ultra-shallow junctions ~ 10 nm are required for sub-20 nm technology [71].

Using high implant dose in order to achieve high active concentrations is not very straightforward as it results in formation of honey comb voids in the substrate which seem to be stable at temperatures as high as 650 °C [102]. Figure 3.1 a) shows porous Ge surface after P 15 keV, 4×10^{15} cm^{-2} implant followed by laser annealing at 0.66 J/cm^2. Figure 3.1 b) is a TEM image by Kaiser *et al.* showing formation of voids on top of the amorphous region after As 150 keV, $6\times10^{15}cm^{-2}$ implant [103].

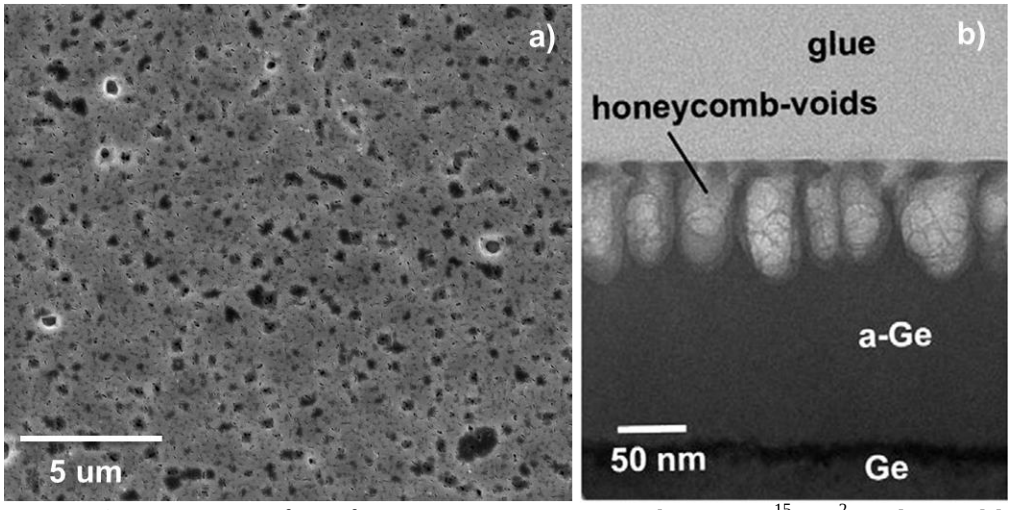


Figure 3.1: a) Porous Ge surface after room temperature P 15 keV, 4×10^{15} cm^{-2} implant and laser thermal anneal at energy density of 0.66 J/cm^2. b) Cross sectional TEM image of the voids after As implant 150 keV, $6\times10^{15}cm^{-2}$. Copyright 2010 American Institute of Physics [103].

Low temperature implants e.g. at 77 K have been shown to eliminate void formation as the vacancies are less mobile and are unlikely to move around and combine with each other. Hot implant also will help to solve this problem due to higher rate point defects recombination [102].

Recently Bao *et al.* reported the formation of Ge pn junctions by laser doping where using spin-on-dopant technique and further laser thermal annealing, P impurities were in-diffused in to the substrate. It is shown that this approach can reduce Ge desorption, and also the junction leakage current compared to ion implantation [104].

Table 3.1 represents a summary of the doping and annealing methodologies that to the best of our knowledge have been applied for Si and Ge processing. In this thesis we discuss some of these techniques and they are highlighted in the table. Having in mind the state-of-the-art techniques being used for processing, and fabrication of Si devices, Ge technology looks quite young and immature. Some of

these methods have never been used in Ge processing e.g. hot implants or are at a very early stage of research e.g. molecular layer doping. Therefore it is imperative to seek new approaches to achieve high activation levels of dopants while maintaining the ultra-shallow junctions in the emerging non-Si based devices.

Table 3.1: A summary of the doping and annealing techniques that have been applied in Si and Ge technology. The areas of interest in this dissertation are highlighted.

Process	Technique
Doping	**Ion implant**
	Cryogenic implant
	Hot implant
	Co-implants
	Plasma doping
	Vapour phase doping
	Spin-on-dopant
	Molecular layer doping
Annealing	**Rapid thermal anneal**
	Solid phase epitaxial regrowth
	Flash lamp anneal
	Laser thermal anneal
	Microwave anneal

The doping process is often followed by an annealing step in order to activate the dopants and repair the crystal damaged of the semiconductor. Again, a large variety of annealing techniques have been explored for Si devices, such as solid phase epitaxial regrowth (minute) [105], flash lamp anneal (millisecond), rapid thermal anneal (second), laser thermal anneal (nano-micro second) [73], and low temperature microwave anneal (seconds-minutes) [106].

3.2.1 Laser anneal activation

Among various annealing techniques that have been developed so far ultrafast laser thermal annealing (LTA) has drawn a lot of interest [107-111]. Providing very limited thermal budgets, LTA has been proven to surpass conventional RTA as it boosts activation levels of the dopants well above the equilibrium limit while suppressing dopant diffusion [69, 73, 111, 112]. This valuable evidence along with achievements in low contact resistance formation [76, 109] proves the efficiency of

this technique. However the impact of LTA on the control of leakage current in Ge junctions is not fully investigated [99].

The aim of this experiment is to systematically compare RTA and LTA with respect to dopant activation and electrical performance of the n+/p junction. Moreover we aim to explore the trade-off between dopant activation and leakage current. In order to fully evaluate these thermal processes we combine a wide range of material characterization with extensive electrical characterization. In this way we explore surface roughness and morphology, crystalline integrity, carrier profiling, sheet resistance and carrier mobility in doped layers, as well as leakage current levels and generation mechanisms.

3.2.2 Experimental procedure

Figure 3.2 shows a summary of the process flow in this experiment. Ge (100) wafers (p-type, 0.059-0.088 Ωcm) received standard cleaning prior to either P or As implant with the dose of 10^{15} cm^{-2} and the energy of 15 keV, and 28 keV respectively. The P implantation amorphized the Ge substrate to a depth of 30-35 nm which for As is 35-40 nm. It is a feature of Ge substrates that the amorphous/crystalline (a/c) interface is not smooth after ion implantation. Following implantation, LTA (single pulse, λ=308 nm) was applied on one set of samples at E_{TH}= 0.55 J/cm^2, E_{TH}+0.25, E_{TH}+0.5, and E_{TH}+0.65 J/cm^2 energy densities in order to cure the crystal damage and electrically activate the dopants. We define the threshold energy E_{TH} as the onset where the Ge surface begins to melt. It is known that changing the energy density changes the melt depth at the Ge surface. Each LTA shot covered an area of 1×1 cm^2 over 158 to 164 ns of exposure time. One P and one As implanted samples were subjected to RTA at 500 °C in N_2 for 3 minutes as a control case. Diodes were subsequently fabricated from P implanted samples. The top contact was formed by evaporation of 20 nm nickel and then patterned by a lift off process. The diodes were isolated from each other by dry etching of a mesa with 600-700 nm height (see Figure 3.11). No germanidation annealing was performed. Ioannou-Sougleridis *et al.* reported enhanced leakage current due to diffusion of Pt atoms in to the depletion region during germanide formation [113].

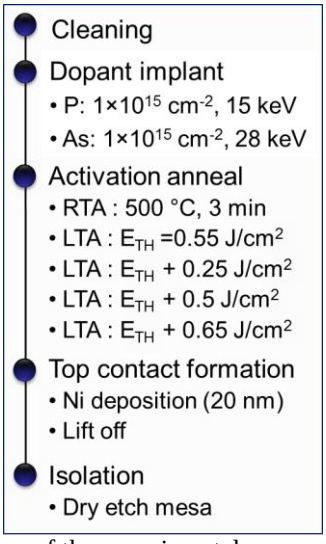


Figure 3.2: summary of the experimental process flow in this work.

The first stage of material characterization involved examination of the surface topography. Atomic Force Microscopy (AFM) was performed in non-contact tapping mode at room temperature on 5×5 μm^2 area for surface examination and surface roughness measurements (RMS) before and after the annealing process. Scanning Electron Microscopy (SEM) was performed on an FEI 650 FEG SEM to inspect the surfaces and test structures. Following this cross-sectional Transmission Electron Microscopy (TEM) was carried out to monitor the crystal integrity using a 200 keV JEOL 2010-HC TEM for the defect analysis, performed under weak beam dark field (WBDF) conditions, and a 200 keV JEOL 2010F for high resolution imaging. For carrier profiling, Secondary Ion Mass Spectrometry (SIMS) was done on a CAMECA IMS 4FE6 system, available at the UMS-CNRS Castaing characterization centre of Toulouse, to obtain the chemical concentration of the dopants, while Electrochemical Capacitance Voltage (ECV) profiling was performed to determine active carrier concentration of the samples. The last stage of material characterization concerned Hall sheet carrier concentration (N_{HS}), mobility (μH), and sheet resistance (R_S) measurements which was done using a microHALL-M300 tool at CAPRES A/S. Several measurements were acquired on each sample for statistical average values.

3.2.3 Results of the material characterization

The samples were initially examined by AFM to inspect the effect of LTA on the surface morphology. After implantation, the RMS was approximately 0.3 nm. As is reflected in the extracted RMS values in Figure 3.3 a), the application of LTA in the partial melt regime (E_{TH} and E_{TH}+0.25 J/cm^2) deteriorated the roughness of the surface. It is known that these energy densities can partially melt the amorphous Ge [73]. At E_{TH}+0.5 and E_{TH}+0.65 J/cm^2 the substrate was melted beyond the amorphous region which resulted in a smooth surface after the LTA process. Figure 3.3 b) and c) show representative AFM images from P implanted samples after E_{TH}+0.25 J/cm^2 and E_{TH}+0.65 J/cm^2 respectively. AFM images from As implanted samples subjected to E_{TH} and E_{TH}+0.5 J/cm^2 are also presented in Figure 3.3 d) and e). From these data, it appears that the higher LTA energy densities are more favorable in order to reduce the roughness of the surface.

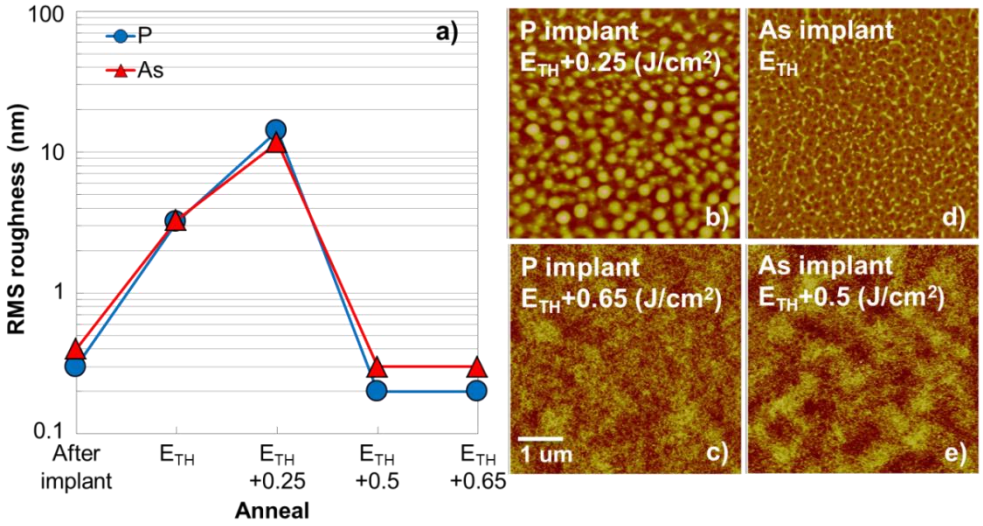


Figure 3.3: a) Surface roughness versus laser energy for P and As samples. Example AFM images of P implanted samples treated by LTA at b) E_{TH}+0.25 J/cm^2 and c) E_{TH}+0.65 J/cm^2.

Representative cross-sectional TEM images of the samples are illustrated in Figure 3.4. Figure 3.4 a) shows the sample after P implantation with the amorphous/crystalline (a/c) interface 35 nm below the surface. Figure 3.4 b) depicts the P implanted sample after E_{TH} LTA. As seen in the WBDF image, the previous amorphous layer is crystallized but stacking faults are also formed (as shown in the high resolution image in the inset) due to poor templated recrystallization. Moreover, the presence of EOR defects at 40 nm below the surface, behind the

previous a/c interface, indicates that the melting arrived just in correspondence of the a/c interface. The same phenomenon was observed by Tsouroutas *et al.* [111]. Figure 3.4 c) shows the P implanted sample subjected to E_{TH}+0.65 J/cm^2 LTA which resulted in apparently defect free crystalline Ge. At this energy Ge is melted beyond the a/c interface.

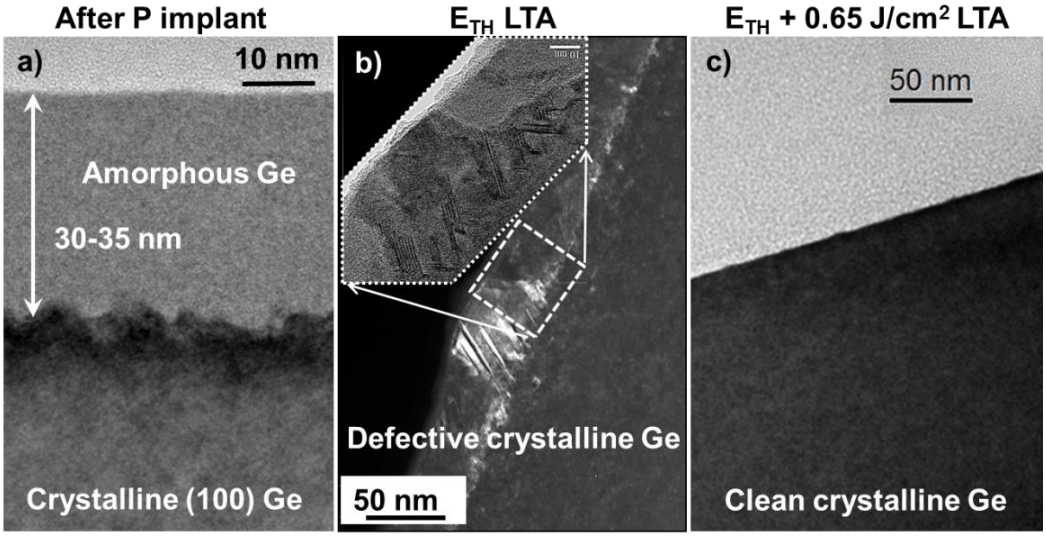


Figure 3.4: Representative TEM images of a) amorphous and crystalline interface in Ge with 30-35 nm amorphous depth after P implant, b) defective crystalline Ge after E_{TH} LTA, and c) crystalline Ge with no visible defects after E_{TH}+0.65 J/cm^2 LTA. We acknowledge Simona Boninelli in MATIS IMM CNR and Fuccio Cristiano in LAAS-CNRS and Univeristy of Toulouse for TEM imaging.

Similar to P case Figure 3.5 illustrates representative cross- sectional TEM images of the As implanted samples before and after the annealing step. Figure 3.5 a) shows as implanted sample after ion implantation with the amorphous /crystalline interface 35-45 nm below the surface. Figure 3.5 b) is an image from the same sample after E_{TH}+0.5 J/cm^2 LTA. In this case the melt-depth is less than the amorphous/crystalline interface leading to polycrystalline Ge and a non-uniform substrate. Figure 3.5 c) shows sample treated with E_{TH}+0.65 J/cm^2 LTA, which created a clean crystalline substrate.

Once again it appears that the higher thermal budget of the high energy density LTA process is desirable, as fewer crystal defects are evident in the TEM images.

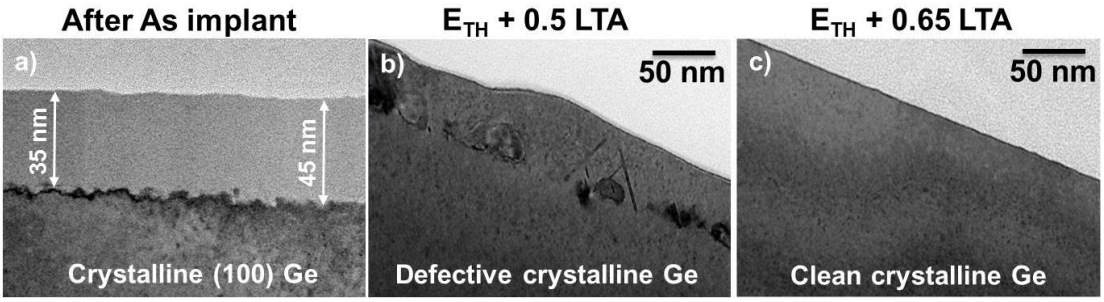


Figure 3.5: Representative TEM images of a) amorphous crystalline interface in the substrate with 35-45 nm junction depth after As implant, b) defective and non-uniform Ge after E_{TH}+0.5 J/cm^2 LTA, and c) clean crystalline Ge after E_{TH}+0.65 J/cm^2 LTA. We acknowledge Simona Boninelli in MATIS IMM CNR and Fuccio Cristiano in LAAS-CNRS and Univeristy of Toulouse for TEM imaging.

Figure 3.6 shows SIMS depth profiles of the P implanted samples subjected to LTA. The a/c interface is shown by a dashed line. The peak on the surface is probably due to a SIMS artefact. From dose integration of the SIMS profiles it was determined that 23-38 % of P out-diffused during the E_{TH} to E_{TH}+0.65 J/cm^2 LTA. Maximum dopant concentration of 2.4×10^{20} cm^{-3} was obtained after LTA at E_{TH}.

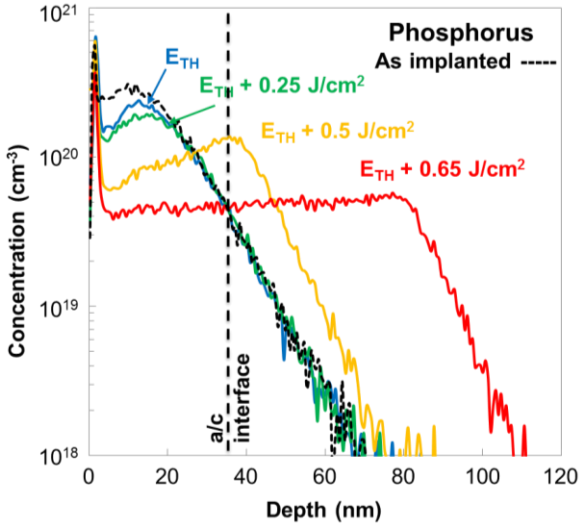


Figure 3.6: SIMS profile of P implanted samples subjected to LTA at energies ranging from E_{TH} to E_{TH}+0.65 J/cm^2.

There is no evidence of redistribution of dopants for the lowest thermal budget cases (E_{TH} and E_{TH}+0.25 J/cm^2). As expected, higher laser energies resulted in a deeper junction and more diffusion of dopants into the substrate. Enhanced redistribution of the dopants in molten Ge created a box-like profile after E_{TH}+0.65 J/cm^2 LTA. In this case the maximum dopant concentration is reduced down to 5.3×10^{19} cm^{-3} due to diffusion.

Dopant loss could be reduced significantly with a careful optimization of the implant conditions, with a much shallower amorphized depth that requires a shallower melting depth and shorter melting time, which subsequently reduces the out diffusion of dopants. Using a capping layer would also help to reduce the dopant loss, hence maximizing the active carrier concentration. An extensive study by Impellizzeri *et al.* on the effect of LTA on activation of B in Ge proved that incorporation of oxygen coming from the native oxide on the Ge surface can impede electrical activation of dopants [114]. This could also be a concern for leakage if oxygen reaches the depletion region of the junction. Comparison of the equilibrium diffusion coefficient for oxygen in Ge [11] with that of for P and As extracted by Chui *et al.* [115] shows that P and As diffuse faster than oxygen in Ge during the annealing process. For the non-equilibrium LTA process we would not expect the oxygen to diffuse faster than the P and As, effectively catching up with the dopants and reaching the depletion region in significant concentration levels.

Figure 3.7 presents active dopant concentration versus depth obtained from ECV measurements for P implanted samples. Comparison of ECV and SIMS profiles for each of the laser energies shows a good agreement between the two techniques (see Figure 3.8). Therefore it appears, within the error bars of the two characterization techniques, all the retained dose of P is activated, with a maximum active concentration of 1.65×10^{20} cm^{-3}, close to the result reported by Mazzocchi *et al.* (1.2×10^{20} cm^{-3}) for P using similar laser energy densities [73]. Using LTA on Sb implanted Ge, Thareja *et al.* also achieved carrier concentrations above 10^{20} cm^{-3} [69].

The observed peak at ~ 35 nm in the E_{TH} LTA is located in the most defective zone of this sample, as found by TEM analysis (cf. Figure 3.4 b) and indicates that the carrier concentration at this depth exceeds the dopant concentration (cf. SIMS profile, Figure 3.6). Similarly to what has already been found during B activation in Si after excimer laser annealing [116], it is therefore suggested that the presence of this ECV peak is attributed to the existing defects rather than to the active dopants. Indeed, the charges measured by ECV are associated to the energy levels distributed in a wide energy range of the bandgap, including those associated to extended defects [117, 118].

Finally, from the ECV profile of the RTA control sample it can be confirmed that RTA resulted in a lower level of active concentration of 2.7×10^{19} cm^{-3} and a deeper junction compared to the LTA samples.

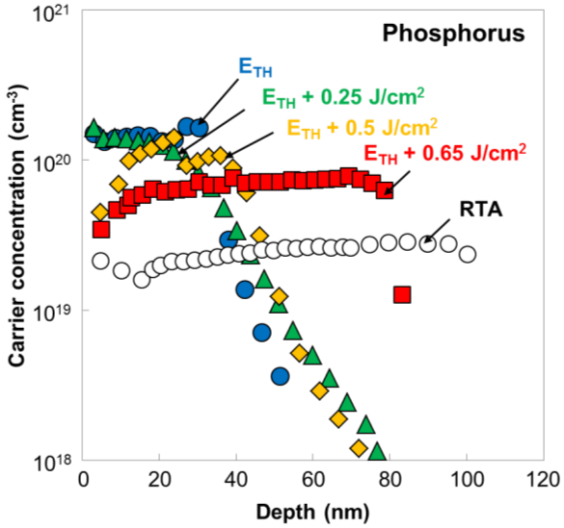


Figure 3.7: Active carrier concentration from P implanted samples obtained by ECV. LTA resulted in higher carrier concentration compared to RTA.

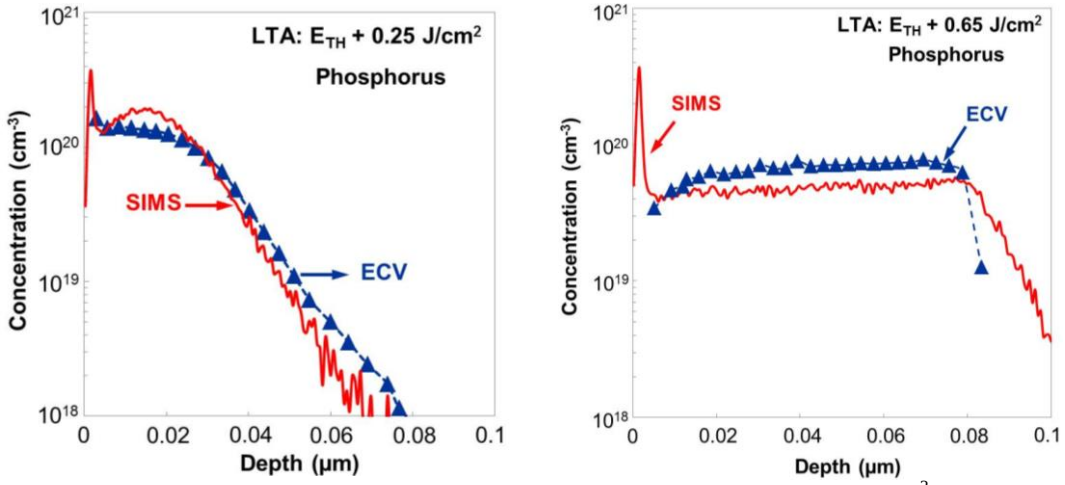


Figure 3.8: SIMS and ECV profile from P implanted samples after a) E_{TH}+0.25 J/cm^2 LTA, and b) E_{TH}+0.65 J/cm^2 LTA.

Figure 3.9 shows SIMS depth profiles of the As implanted samples subjected to LTA. Here the a/c interface lays 35-40 nm below the surface indicated by the dashed line. Almost no redistribution of dopants is observed at E_{TH} LTA.

Dose integration of the SIMS profile at this energy shows no dopant loss during the LTA process. However subsequent LTA energies resulted in 10-20% dose loss. Using ETH+0.65 J/cm$_2$ LTA a box-like profile is formed with the melt depth lying about 80 nm below the surface. Here the plateau concentration is $>10^{20}$ cm^{-3}.

Similar to the P samples no observable defects were formed after the amorphized Ge region (including EOR defects) was fully melted and re-grown.

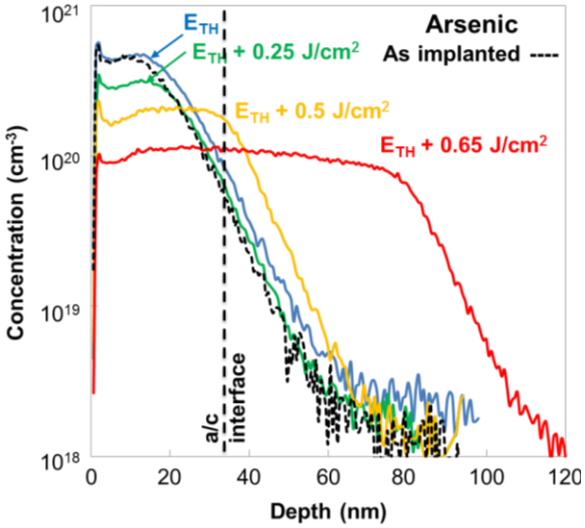


Figure 3.9: SIMS profile of As implanted samples subjected to LTA at energies ranging from E_{TH} to E_{TH}+0.65 J/cm^2.

Active carrier concentration of the As doped samples was also measured by the ECV profiling technique which is shown in Figure 3.10.

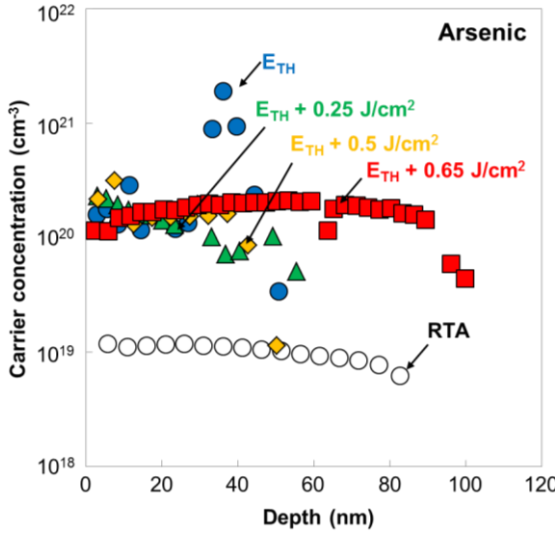


Figure 3.10: Active carrier concentration from As implanted samples obtained by ECV. LTA resulted in higher carrier concentration compared to RTA. The peak in the carrier concentration of the E_{TH} profile is due to the accumulation of defects in the junction not dopants alone.

High active concentrations >10^{20} cm^{-3} were achieved after E_{TH} LTA on As implanted samples with a peak concentration of 10^{21}cm^{-3} at ~35 nm. Several E_{TH} samples were re-measured to confirm these results. Integrated dose of the E_{TH} profile is >10^{15} cm^{-2} indicating that the charge is coming not from the dopant but

from defects at the original a/c interface similar to what previously discussed for the Phosphorus implanted samples (cf. in Figure 3.7).

As was shown for P in Figure 3.4, similar trends were obtained for As resulting from the LTA process. Like the P case, higher laser energies resulted in deeper doping profiles and lower levels of dopant concentration due to diffusion. Again within the error bars of the ECV and SIMS characterization techniques it appears that all the retained dose of As is activated. As a comparison Hellings *et al*. reported 13-26 % activation for As implanted Ge using millisecond laser annealing [108]. ECV characterization on the control RTA sample shows carrier concentration ~ 10^{19} cm^{-3}. Using excimer laser annealing Milazzo *et al.* obtained active carrier concentration of As dopant above 10^{20} cm^{-3} [110].

Table 3.2 shows the mobility and micro Hall Effect measurements on P and As implanted samples after E_{TH}+0.5 and E_{TH}+0.65 J/cm^2 LTA. Higher laser energy in both sets of samples resulted in improved carrier mobility (μ_H) and also lower sheet resistance (R_S). This is consistent with the observations from material studies where the higher laser energy repaired the crystal lattice after the implantation process (see Figure 3.4). Extracted sheet carrier densities with Hall measurements (N_{HS}) is in good agreement with the active integrated concentrations obtained from ECV profiling technique. Active carrier concentration normally increases with increased thermal budget but from these measurements it remains constant.

Table 3.2: Micro Hall effect measurements

Dopant	Anneal (J/cm^2)	μ_H (cm^2/Vs)	N_{HS} (cm^{-2})	Rs (Ω)
P	E_{TH}+0.5	118	5.78×10^{14}	91.8
P	E_{TH}+0.65	161	5.60×10^{14}	69.4
As	E_{TH}+0.5	94	9.01×10^{14}	73.9
As	E_{TH}+0.65	112	8.63×10^{14}	64.5

The observed discrepancy in the extracted values may be associated with the out-diffusion of the dopants during the thermal treatment as well as an almost perfect activation of dopants in both cases. In conclusion from the material analysis, it is apparent that the best choice of LTA condition depends on a number of factors. At low energy density, we observe a diffusion-less high activation of dopants, at a cost of residual defects in the crystal. At high energy density, crystalline integrity is drastically better, while maintaining very impressive levels of carrier concentration.

However care must be taken to optimize the process so as to avoid excessive dopant diffusion.

3.2.4 Results of the electrical characterization on diodes

Although LTA seems to be promising to achieve high activation levels of dopants with no observable defects in the TEM images (Figure 3.4 and Figure 3.5), more evidence on electrical performance of these junctions in terms of leakage current and I_{ON}/I_{OFF} ratio is needed for a clear understanding of the effects of this technique. By making diodes and electrically characterizing them we can study the defects that exist in a pn junction but are not visible in TEM imaging. These defects are responsible for leakage current in the junction.

Figure 3.11 shows a SEM image of the fabricated diode structures. The inset shows a schematic of characterized circular diodes ranging from 100 to 500 µm diameter.

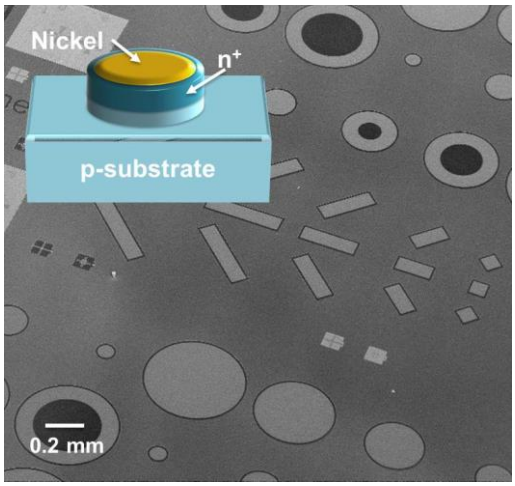


Figure 3.11: SEM image of the diode test structures. The inset shows a schematic of the characterized diodes.

Figure 3.12 depicts I-V characteristics obtained from 500 µm circular diodes processed by LTA and RTA. Due to the similarity in the material characterization trends for P and As implants, we focus on P in the electrical analysis in the remainder of this chapter. The E_{TH} LTA sample shows poor I-V characteristics with very high leakage current and ideality factor n larger than 2. This can be associated to the formation of a defective substrate during the re-crystallization process. Annihilation of defects at higher laser energies (see Figure 3.4) resulted in

improved I-V characteristics. I_{ON}/I_{OFF} ratio > 10^4 was obtained between -1 to 1 V for E_{TH}+0.65 J/cm^2, with n=1.4. Note that smaller dimension diodes produced a higher I_{ON}/I_{OFF} ratio above 10^5 with n= 1.2 (see Figure 3.18).

Significantly, RTA diodes showed ideal behaviour with n =1.03 and I_{ON}/I_{OFF} ratio > 10^6. From the I-V characteristics it can be concluded that there are deep level defects in the n+/p junctions formed by LTA which form generation centres contributing to the leakage current [119]. In the RTA case, on the contrary, long thermal budget cured the defects in the depletion layer and resulted in very low leakage current. Moreover, diffusion of dopants due to the long RTA (as compared to LTA) shifted the junction depth beyond the original defective region within the n+ part of the junction so that the remaining defects (if any) would not be located in the depletion region and have an impact on the leakage current.

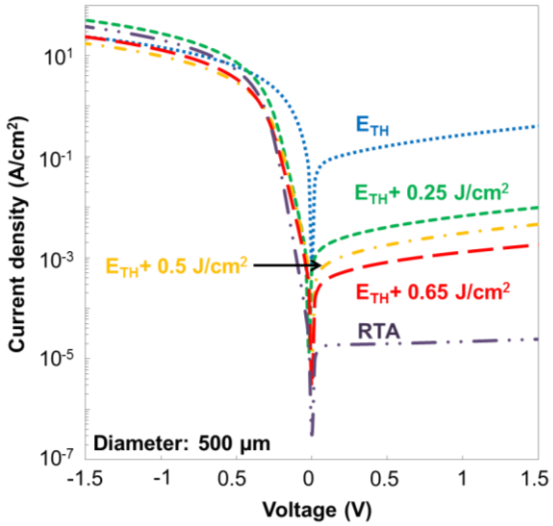


Figure 3.12: Diode I-V characteristics from P implanted samples treated by RTA and LTA (E_{TH} - E_{TH}+0.65 J/cm^2).

As stated earlier I-V measurements were carried out on a large set of diode structures from which perimeter leakage current density (J_P) was extracted using

$$I = P \cdot J_P + A \cdot J_A \qquad (3.1)$$

which becomes:

$$\frac{I}{A} = \frac{P}{A} \cdot J_P + J_A \qquad (3.2)$$

where P and A are perimeter and area of the diode and J_P and J_A are perimeter and area leakage respectively.

To confirm perimeter leakage is not significant Figure 3.13 illustrates leakage current density at 1V versus different perimeter/area ratios for the LTA and RTA diodes. For clarity, data are presented in semi log scale. A straight line can be well fitted to the data in linear scale with the slope of the line corresponding to the perimeter leakage current, according to equation (3.2). It can be confirmed that both RTA and LTA diodes exhibit very low perimeter leakage which is at least 2 orders of magnitude smaller than the area leakage current. The graph also gives good overview of the current density for all types of samples showing improvement in leakage current from E_{TH} to E_{TH}+0.65 J/cm^2 to the RTA diode.

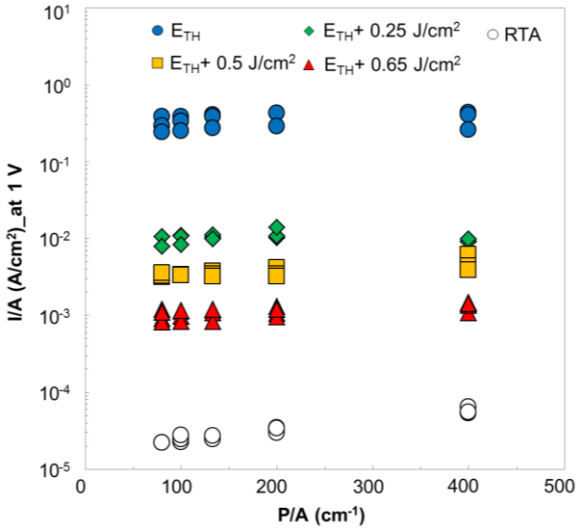


Figure 3.13: Representative perimeter leakage current density at reverse voltage of 1V for different perimeter area ratios for LTA and RTA diodes.

There are different mechanisms responsible in leakage current which are temperature and electric field dependent, and can be classified as Shockley-Read-Hall (SRH) generation/recombination, trap-assisted tunnelling (TAT), band-to-band tunnelling (BBT) and diffusion current [119]. In order to determine the dominant mechanism I-V measurements were carried out at temperatures ranging from -35°C to 100°C in 15°C steps. An activation energy (E_A) was then derived from Arrhenius plots.

Generally speaking, SRH dominated leakage current is more pronounced in the presence of deep level defects in the junction with E_A approximately half of the

band gap. TAT occurs when defects operate as trap levels in the depletion region, causing electrons to be captured and tunnel due to the electric field. E_A around half of the band gap is also expected for TAT. If a high electric field exists in the junction then the most probable mechanism to happen is BBT, as electrons are actuated from valence band in the p-side to the conduction band in the n-side through the depletion region. E_A is approximately 0 eV in this case. For diffusion current, which is proportional to the square of intrinsic carrier concentration, (n_i^2), E_A is close to the band gap [120].

In Figure 3.14 I-V characteristics from 300 µm E_{TH}+0.65 J/cm^2 LTA diode structures at different temperatures are shown. The effect of temperature on diode behaviour was reflected in the ideality factor extracted at each temperature. The inset in Figure 3.14 illustrates variation of n versus temperature with n increasing by temperature.

In these measurements leakage current increased about 3 orders of magnitude at 1V, suggesting that diode behaviour is strongly affected by temperature variations. Meanwhile at low temperatures (from -35°C to room temperature (RT)) leakage current is more dependent on the electric field.

Activation energy for this sample at 1 V was found to be 0.47 eV, which is bigger than half of the Ge band gap. According to theory SRH dominated leakage current is proportional to depletion width which itself is proportional to $V^{0.5}$ [119]. Measurements on the LTA diode revealed that the leakage current is proportional to V^x with $x > 0.5$ for temperatures from -35 to 55 °C and $x < 0.5$ for temperatures from 55 to 100 °C. These results along with extracted E_A values (see Figure 3.16) point out that the leakage mechanisms are dominated by TAT and SRH, respectively.

Figure 3.15 shows representative I-V characteristics obtained from a 300 µm RTA diode. Again temperature measurements were carried out from -35 °C to 100 °C with 15°C increments. Similar to the LTA diode ideality factor was increased by temperature as is shown in the inset. Leakage current was enhanced about 5 orders of magnitude at 1 V due to the temperature change. For this particular sample the current can be categorized in two different regimes in terms of the leakage current behaviour.

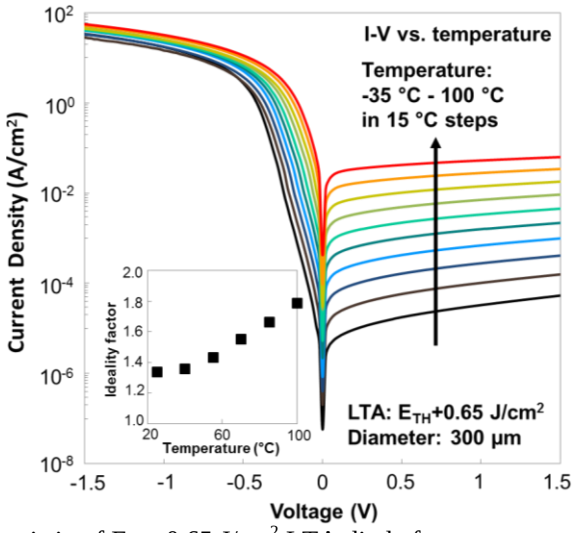


Figure 3.14: I-V characteristic of E_{TH}+0.65 J/cm^2 LTA diode for temperature increments from -35 to 100° C in 15° C steps.

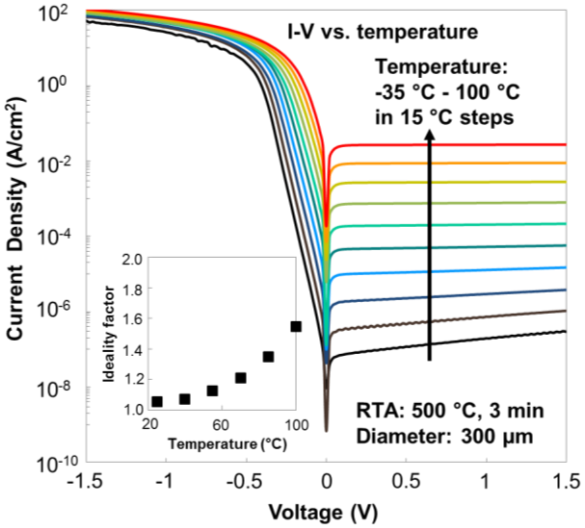


Figure 3.15: I-V characteristic from RTA sample for temperature increments from -35 to 100° C in 15° C steps.

From -35 °C up to 10 °C the leakage current showed electric field dependence whereas it showed weak dependence on the electric field from 25 °C to 100 °C. This difference was also reproduced in the activation energy extraction. The activation energy extraction routine is explained in more detail in Figure 3.17, and is shown for only 2 conditions. Note we performed this analysis on all the diode structures and samples, and this figure shows a representative data sample set.

Figure 3.16 represents reverse current density versus 1/kT from a 300 µm E_{TH}+0.65 J/cm^2 LTA diode for RT to 100°C. Extracted activation energies from the

Arrhenius plots for 0.5 to 2 V are ~ 0.5 to 0.4 eV respectively. The inset shows similar graph for 1V for the RTA sample where the diode behaviour splits into two regimes. Different activation energies at high and low temperatures were also observed by Eneman *et al*. [121].

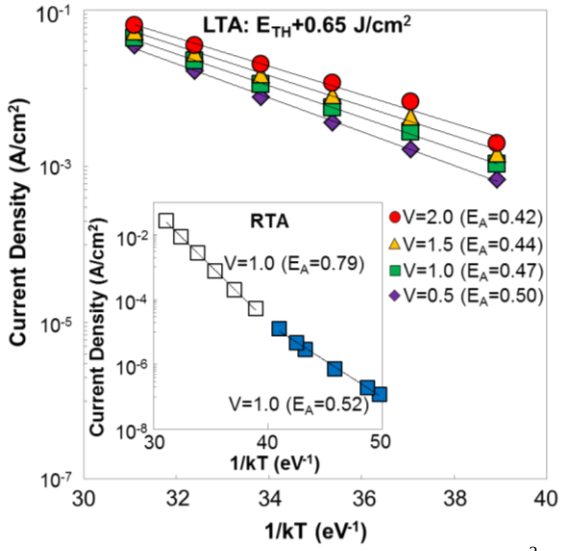


Figure 3.16: Reverse current density versus 1/kT from E_{TH}+0.65 J/cm^2 LTA sample for RT and above. Activation energy is extracted from the slope of the fitted lines. The inset shows current density versus 1/kT for the RTA sample for which different behavior is observed below and above RT.

Below RT the E_A was 0.52 eV suggesting TAT as the main contributor to the leakage current. Interestingly, for the temperatures above RT the extracted E_A was 0.79 eV. Considering voltage independency of the I-V characteristics it could be interpreted that diffusion is dominating the leakage mechanism in this regime with few generation centres in the depletion layer.

Activation energy versus voltage for RTA and LTA samples at RT and above is presented in Figure 3.17. For all LTA samples activation energy is between 0.4 and 0.6 eV. Note that E_A= 0.79 eV (RTA case) is very close to direct band gap (0.8eV) of Ge. This appears to be a surprising result as the indirect band gap of Ge is 0.67 eV.

The reason for E_A > 0.67 eV is not well understood and is currently under investigation. It should be noted that multiple samples and multiple diode structures produced this result. Furthermore we tested our samples on two entirely different probe stations producing the same results. Moreover we repeated the entire experiment and RTA processed diodes still produced E_A > 0.67 eV. The activation

energies for the RTA samples are over 90 meV in excess of what is expected for a perfectly crystalline sample doped at 2.7×10^{19} cm^{-3}. The inset in Figure 3.17 shows the Fermi level versus carrier concentration for Ge, calculated using a 30 band k.p model [122]. At the reported doping concentration the Fermi level and hence the activation energy should lie around 0.7 eV.

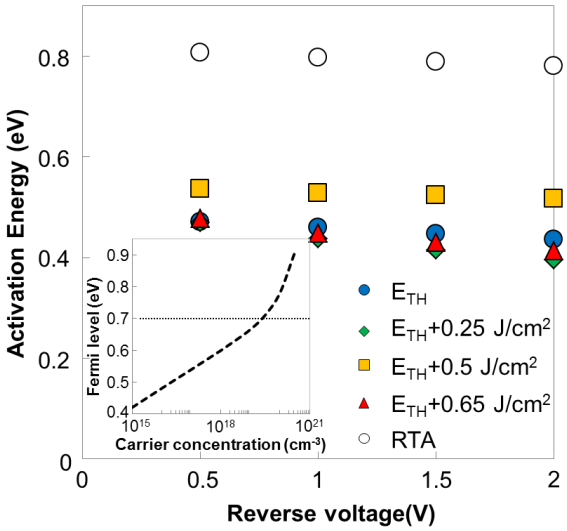


Figure 3.17: Activation energy versus reverse bias extracted from RTA and LTA diodes. The inset shows calculated Fermi level versus carrier concentration in the n-type region, using a 30 band k.p model.

Possible reasons for higher activation energies are: (i) a higher carrier concentration of ~ 10^{20} cm^{-3}, introduced in the process of making the diodes, and (ii) a hybridization of the conduction band with the impurity level at high doping concentration, which may shift the bottom of the conduction band higher in energy. Both these effects would result in an E_A strongly sensitive to doping concentration. However, we saw in our ECV data in Figure 3.7 for RTA processed P implants, that the active concentration was approximately 2.7×10^{19} cm^{-3} which seems to be inconsistent with the first explanation above. We are currently investigating this trend in the experimental data further through advanced theory and modelling.

Figure 3.18 shows the I_{ON}/I_{OFF} ratio versus n extracted from 100-500 µm LTA and RTA diodes. Coloured symbols show the results from LTA diodes, and open symbols show the RTA case. The best I_{ON}/I_{OFF} ratio from LTA samples was obtained from the 100 µm E_{TH}+0.65 J/cm^2 LTA diode with n= 1.3 and I_{ON}/I_{OFF} ratio= 2.4×10^5, which matches the best reported to date for Ge diodes with LTA [69]. RTA diodes exhibit n less than 1.05, with corresponding I_{ON}/I_{OFF} ratio ~ 10^7,

which to the best of our knowledge is the highest obtained for Ge diodes to date. n ~1 indicates that there are few defects in the junction, and the total leakage current is mainly dominated by diffusion current. To benchmark our results the inset shows similar works on Ge that have been reported so far [99, 123-127].

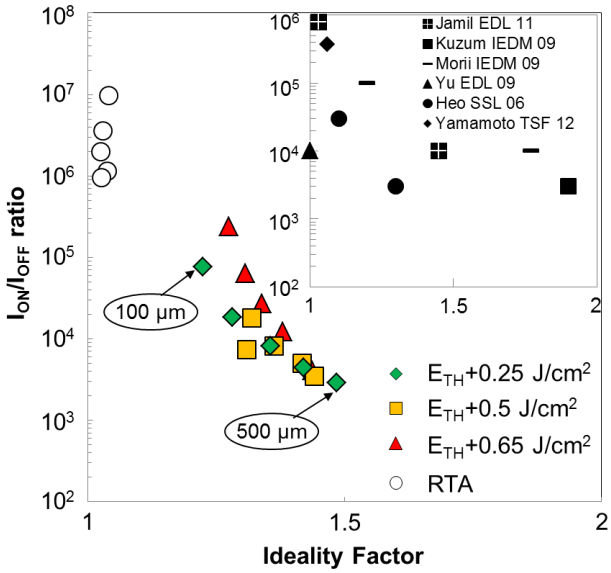


Figure 3.18: I_{ON}/I_{OFF} ratio versus ideality factor for LTA and RTA samples. The inset shows I_{ON}/I_{OFF} ratio for other works published.

Jamil *et al.* used Spin-on-Dopant technique and reported n~ 1.03 and I_{ON}/I_{OFF} ratio~ 10^5-10^6 as compared to conventional ion implantation with n= 1.45 and I_{ON}/I_{OFF} ratio ~ 10^3-10^4 [123]. Kuzum *et al.* achieved n ~ 1.9 and I_{ON}/I_{OFF} ratio ~ 10^3 from NMOS devices with GeO_xN_y dielectrics [124]. Morii *et al*. reported n ~ 1.2 and I_{ON}/I_{OFF} ratio ~ 10^5 from junctions created by Gas Phase Doping and n~ 1.77 and I_{ON}/I_{OFF} ratio ~ 10^4 from phosphorus implanted n+/p junctions [125]. Yu *et al.* compared in-situ doping with ion implantation and reported n ~ 1 and I_{ON}/I_{OFF} ratio = 1.1×10^4 for in-situ doping. For ion implanted samples the I_{ON}/I_{OFF} ratio was ~10^3 [126]. Yamamoto *et al.* fabricated n+/p diodes with n~ 1.06 and I_{ON}/I_{OFF} ratio ~ 3.7×10^5 [127]. Koike *et al.* reported I_{ON}/I_{OFF} ratio ~ 10^6 by two-step P implantation followed by RTA [49]. Heo *et al.* applied plasma doping followed by excimer laser annealing on Ge and obtained n~ 1.1-1.3 and I_{ON}/I_{OFF} ratio ~ 10^3-10^4 [99]. Their ideality factor is better than the value reported in this work but the obtained I_{ON}/I_{OFF} ratio seems to be lower compared to our data. In our case we used ion implant whereas plasma doping was used in the Heo *et al.* work.

This may lead to differences in damage and defect distributions close to the junction, leading to different diode performance. Plasma implant is known to reduce EOR defects and keep the implanted region very shallow (~ 10 nm in [99]). In that case the melting time is probably shorter, thus the dopants out-diffusion is limited. In addition high concentration of P on the surface could act as a capping layer limiting the oxygen incorporation from the native oxide which may result in fewer defects.

There is certainly a trade-off between high levels of carrier concentration and the electrical performance of the n+/p junctions. Figure 3.19 shows the leakage current versus maximum carrier concentration for the RTA and LTA samples.

As is shown in the plot, LTA provides high carrier concentration, which is good for access resistance with trade-off in I_{ON}/I_{OFF}. The opposite is true for RTA technique. From our data it is evident that optimum LTA condition can be found to achieve high carrier concentration with acceptable I_{ON}/I_{OFF} ratios.

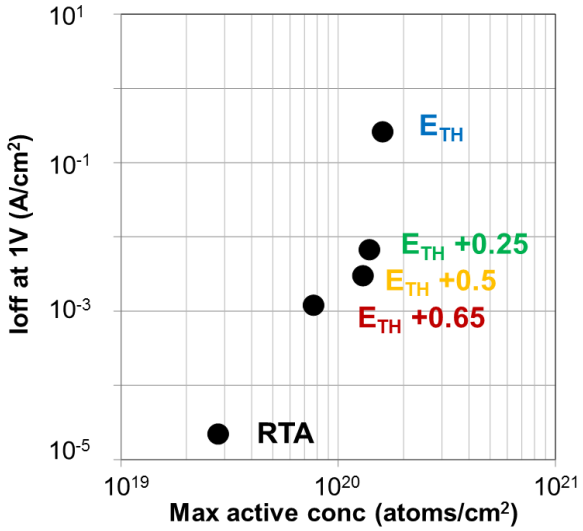


Figure 3.19: Leakage current versus maximum active concentration as a function of the annealing process/energy. This plot clearly shows and the decreasing trend of the leakage current at the cost of lower activation level for the dopants.

3.3 Co-implantation

P and As show concentration dependent diffusivity [59, 115] in extrinsic doping conditions reflected in their box-like doping profile with a flat plateau and sharp drop-off in the tail after RTA. Reducing diffusion might be possible if implant dose

is decreased but that would come with low dopant concentration and high sheet resistance. Since P and As tend to diffuse via a vacancy mediated mechanisms [59, 128] controlling the vacancy population with point defect engineering could help to reduce dopant diffusion.

One solution is using non-dopant impurity co-implants in Ge. It has been shown that C co-implant can help to control B and P diffusion and deactivation [129]. C has been shown to reduce P diffusion both in form of co-implant [73] and molecular-beam-epitaxy [130]. N has also been experimentally demonstrated to suppress P diffusion [131, 132]. F is also considered as a co-implant to control diffusion in Si process [133, 134] either implanted by itself or in form of BF_2.

Note that F exhibits quite unusual behaviour in Si as it does not seem to spend much time in substitutional sites. Looking for impurity solubility and diffusivity of F in Si, one would notice notable absence of F in text books and literature [78, 135]. Jeng *et al.* observed rapid outgassing of F from Si during thermal annealing and attributed that to formation of volatile Si oxyfluoride and Si fluoride on the surface [136]. This can probably be blamed for the difficulty in experimentally extracting F solubility and diffusivity data in crystalline Si. F diffusivity in amorphous Si was extracted at relatively low temperatures by Nash *et al.* [137].

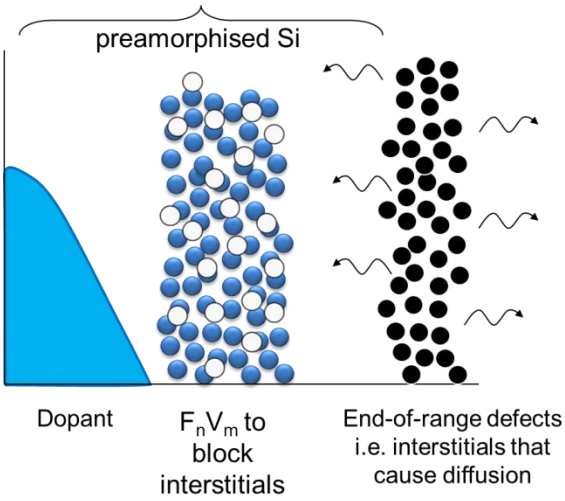


Figure 3.20: Schematic of F role in suppression of B diffusion in Si.

It is known that F has strong electronegativity and if implanted with high concentration in pre-amorphized Si it forms F_nV_m clusters [138] during the recrystallization process. Immobile peaks in SIMS profiles of F in Si often are associated with F-rich clusters. It has been proven that these clusters are effective in

suppression of B deactivation and diffusion [139] as they capture interstitials which will cause the F_nV_m to dissolve [105] resulting in improved thermal stability of SPER-formed junctions as is shown in Figure 3.20.

As proposed by the theoretical calculations in [101] F co-implants might be effective in reducing P diffusion in Ge by forming F_nV_m clusters. These clusters basically occupy the vacancies that P needs to interact with for diffusion into the substrate. Despite promising theoretical studies [140] on F co-implants in Ge, few experimental works have been reported in this area. Jung *et al.* used F ion-implant to passivate vacancy defects in Ge which generate acceptor states in Ge [141].

In this part of the thesis we report our results on the effects of F co-implants in P and As doped Ge.

3.3.1 Experimental procedure

Figure 3.21 depicts the process flow undertaken in this study. Experiments were performed on (100) n-type Ge wafers, with a bulk resistivity of 0.2-0.5 ohm.cm. After a standard clean, wafers received an n-type dopant implant, either P with a dose of 1×10^{15} cm^{-2} and energy of 15 keV, or As with a dose of 1×10^{15} cm^{-2} and energy of 28 keV. In some cases F was implanted with a dose of 1×10^{15} cm^{-2} and energy of either 10 keV which overlays the dopant profiles or 25 keV that is slightly deeper. The first approach puts the F profile in proximity to the dopants. The latter is the typical approach used in Si processes where the projected range of the co-implant is at the depth between the dopant profile and the expected location of the end-of-range defects. All implants were performed at a tilt of 7°, with a native oxide covering the substrate. Wafers subsequently received an RTA in an inert ambient at 600 °C. Anneal times were in the 1-30 s range. Ge substrate loss during RTA is significant, and we expect approximately 0.15 and 4.5 nm to be lost for 1 and 30 s respectively, according to the model of Ioannou *et al*. [142]. It is often common practice to cap Ge substrate during RTA. However covering oxide cap was purposely omitted to determine if there was a link between dopant loss and implant damage.

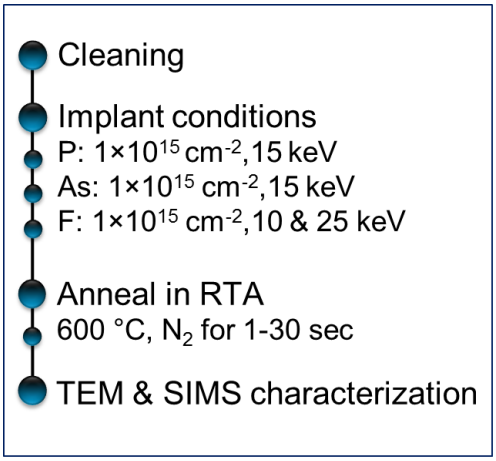


Figure 3.21: Process flow of the experiment.

Secondary-ion-mass-spectrometry (SIMS) was used to characterize the impurity profiles, with Cs^+ primary ions and negative mode for P and As, and with O_2^+ primary ions and positive mode for F. Cross-sectional transmission electron microscopy (XTEM) was also performed on some samples. Bright-field XTEM images were generated to measure the amorphous Ge depth after implant.

3.3.2 Results of the material characterization

The XTEM image in Figure 3.22 shows the sample after a 25 keV F implant, with an amorphized region which is 72 nm deep. A brief theory on ion implantation and point defect is presented in sec 4.2.

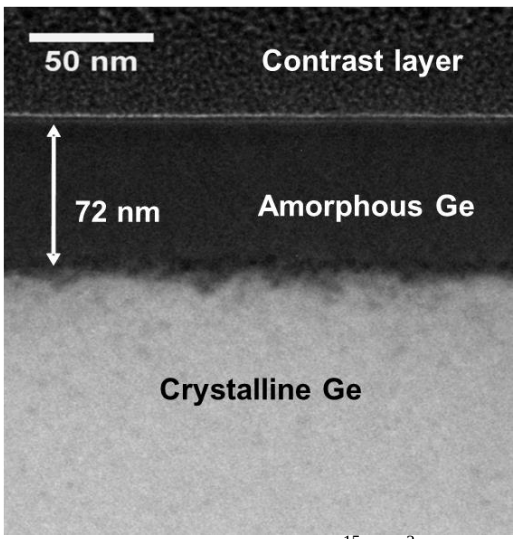


Figure 3.22: A cross-sectional TEM image after the 1×10^{15} cm^{-2} 25 keV F implant. The amorphous Ge depth is approximately 72 nm.

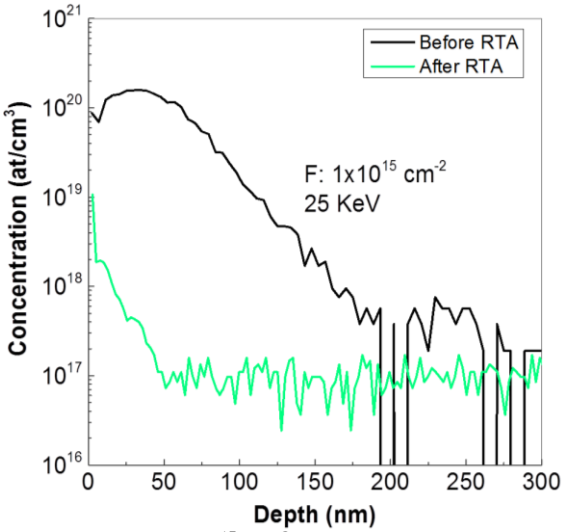


Figure 3.23: SIMS depth profile of F (1×10^{15} cm^{-2} 25 KeV) before and after RTA at 600 °C, 30 sec.

Figure 3.23 represents the chemical concentration of the F implant before and after RTA at 600 °C for 30 s in N_2 confirming F out-diffusion after RTA. SIMS profiles after RTA at 600 °C for 1 sec did not show any F either indicating that F out-diffused after 1 sec anneals (data not shown here).

Figure 3.24 shows SIMS profiles for P after the 600 °C 30 s RTA. The characteristic box-like diffused profile is clearly evident.

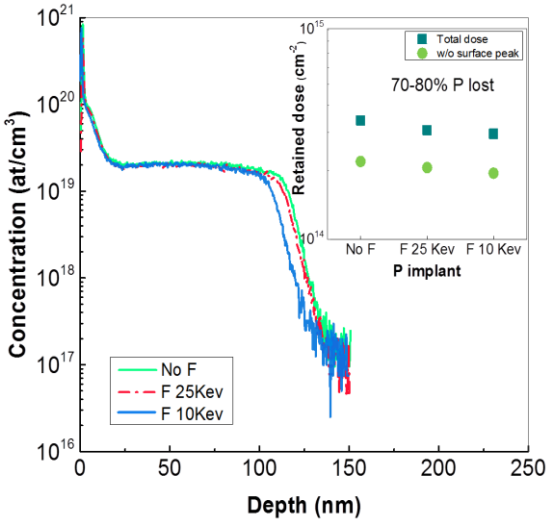


Figure 3.24: P concentration versus depth profiles for a 1×10^{15} cm^{-2} 15 keV implant after a 600 °C 30 s RTA, without F (solid line), with a deep F implant (dashed line), and with an overlaying F implant (dotted line). The retained doses extracted from the SIMS are plotted in the inset, either including the surface peak or assuming a plateau of 2×10^{19} cm^{-3} in the near-surface region.

There is little difference between the P profiles for the different F conditions, as the junction depth (X_j) at a P concentration of 1×10^{18} cm^{-3} is 120-126 nm. The roll-off

of the tail is approximately 10 nm/decade. The retained dose was extracted from the SIMS profiles, and is plotted in the inset. Note there is a 10 % relative error for these values which is standard for SIMS characterization. As the SIMS surface peak may be misleading, we also extracted retained dose assuming the plateau concentration of 2×10^{19} cm^{-3} in the near surface. These levels of dopant loss are consistent with literature. The addition of 10 keV F reduced the retained dose by roughly 12 %.

Figure 3.25 shows SIMS profiles for As after the 600 °C 30 s RTA. A characteristic concentration-enhanced diffusion is observed. X_j at an As concentration of 1×10^{18} cm^{-3} is 165-180 nm. The roll-off of the tail is approximately 20 nm/decade. The resulting retained dose was extracted from the SIMS profiles, and is plotted in the inset. Without the surface peak we extracted retained dose assuming the plateau concentration of 1×10^{19} cm^{-3} in the near surface. The 25 keV F implant has no significant dose loss impact while the 10 keV F implant reduced the dose by approximately 23 %.

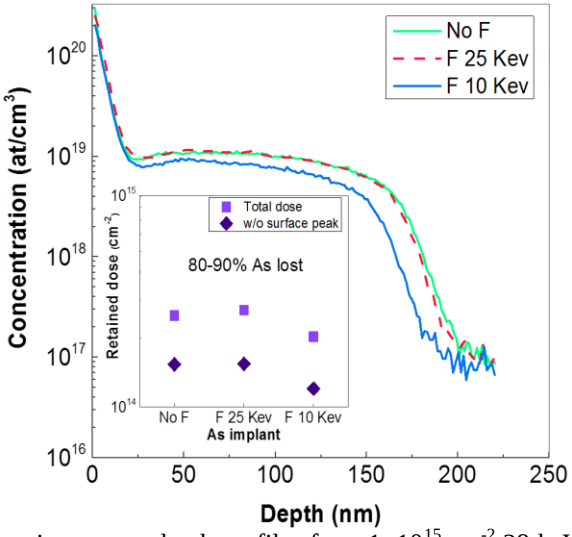


Figure 3.25: As concentration versus depth profiles for a 1×10^{15} cm^{-2} 28 keV implant after a 600 °C 30 s RTA, without F (solid line), with a deep F implant (dashed line), and with an overlaying F implant (dotted line). The retained doses extracted from the SIMS are plotted in the inset, either including the surface peak or assuming a plateau of 1×10^{19} cm^{-3} in the near-surface region.

Clearly F has minimal impact on P and As diffusion in Ge under RTA processing. Both dopants exhibit a strong $(n/n_i)^2$ diffusion dependence, and any subtle differences in X_j can be correlated with differences in retained dose. SIMS analysis was undertaken to profile the F concentration. Curiously, no F (> 5×10^{16}

cm^{-3}) could be found. SIMS of the unannealed samples (c.f. Figure 3.23) clearly showed that F had indeed been implanted. Subsequently, shorter anneals were done on pieces of the 25 keV-F-implanted wafer. Further SIMS analysis showed F had completely outgassed after a 600 °C 5 s RTA, and even after a 600 °C 1 s RTA. Thus the failure of F to impact on P and As diffusion during RTA is because F does not remain in the Ge substrate for a sufficiently long time at these temperatures.

F_nV_m cluster formation in vacancy-rich regions in crystalline Si and in crystalline SiGe has been extensively studied as a function of F implant dose by El Mubarek *et al*. [143, 144]. Increasing the F implant dose increases the concentration of F and vacancies at depths less than the implant projected range, thus increasing the likelihood of F_nV_m cluster formation. However, as shown in Figure 3.22 high F implant doses amorphize the Ge substrate, and assuming vacancy point defects are annihilated upon recrystallization, if F_nV_m clusters are to form in Ge they should do so while the substrate is still amorphous. Future work in this area could explore higher F concentrations ($>3\times10^{20}$ cm^{-3} at least) while being extremely careful to avoid the formation of the characteristic porous sponge-like structure at the Ge surface, common after high-dose or heavily-damaging implants [145].

It is difficult to estimate F diffusivity, as an approximation we use the relation $L=2(D.t)^{½}$, where L is the diffusion length, D is diffusivity, and t is time. For the 25 keV F profile, even if snowplowing sweeps away all the F within the amorphized region, a conservative estimate of F diffusion length is 100 nm. If t=1 s, this gives $D=10^{-10}$ cm^2s^{-1}, which is comparable to some fast-diffusing transition metal diffusivities in Ge at 600 °C [11].

Figure 3.26 shows the temperature dependence of the diffusion coefficient of various foreign atoms in Ge [146].

It was shown that a F co-implant can affect the diffusion of a low dose As (3×10^{13} cm^{-2} dose) implant in certain annealing conditions [147]. A reduction of P (6×10^{13} and 1×10^{15} cm^{-2} dose) diffusion in Ge using F co-implant was recently reported at 400 °C whereas at 450 °C reduced diffusion was only observed for the lower P dose. Upon annealing at 500 °C F showed no impact on diffusion of P [148].

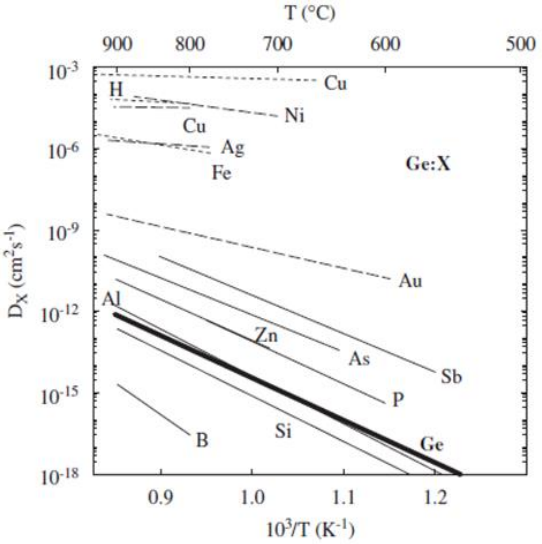


Figure 3.26: Temperature dependence of the diffusion of foreign atoms in Ge in comparison to self-diffusion. The solid lines represent the diffusivity of the substitutionally dissolved elements. hybrid elements(long-dashed lines), i.e. Cu, Au, Ni, and Ag dissolve on both interstitial and substitutional sites[146].

Like in Si, F seems not to reside substitutionally in the Ge lattice for a long time before diffusing away quickly. F solubility data in Ge is also lacking in literature. However, in contrast to Si, F appears not to form stable clusters easily. In the $>10^{20}$ cm^{-3} concentration range F_nV_m clusters form in Si and are stable enough to be characterized after standard RTAs. The rapid departure of F from Ge indicates that F_nV_m clusters in Ge are not very stable, at least in the concentration range of interest in this experiment.

Further work is ongoing in the study of dopant outgassing which will be described in the next section.

3.4 Substrate desorption and dopant outgassing

As was indicated in previous sections (3.2.3 and 3.3) significant amount of dopants were lost during the annealing process. This was more pronounced in RTA treated samples although LTA (especially in P implanted samples) showed some percentage of dopant loss. Dopant loss in Ge has been observed during low-temperature annealing as well.

It is still not quite clear why and how dopant loss/out-gassing happens but in general, it is associated with Ge substrate desorption during the annealing process

[142, 149]. It is suggested that using a capping layer (SiO_2 or Si_3N_4) can help to reduce the out-diffusion although it cannot fully eliminate it. It is shown that Si_3N_4 is more effective to suppress out-gassing compared to SiO_2 [142] essentially due to its density. Ge desorption is undesirable since it causes surface roughness, which eventually leads to degradation of electrical characteristics of the fabricated device.

The aim of this work is to answer the following questions:

1. Is Ge desorption dopant dependent?

2. Does Ge desorption alone account for dopant loss seen in diffusion studies? (or is there another mechanism involved?)

3.4.1 Experimental procedure

Figure 3.27 a) shows a summary of sample preparation process. After a standard clean n-type (100) Ge wafers with a bulk resistivity of 0.2-0.5 Ω.cm received an implant of P with the doses of either 1×10^{14} cm^{-2} (sample B) or 1×10^{15} cm^{-2} (sample C). In order to compare possible effects of implant damage on desorption phenomenon one sample did not receive any implant (sample A).

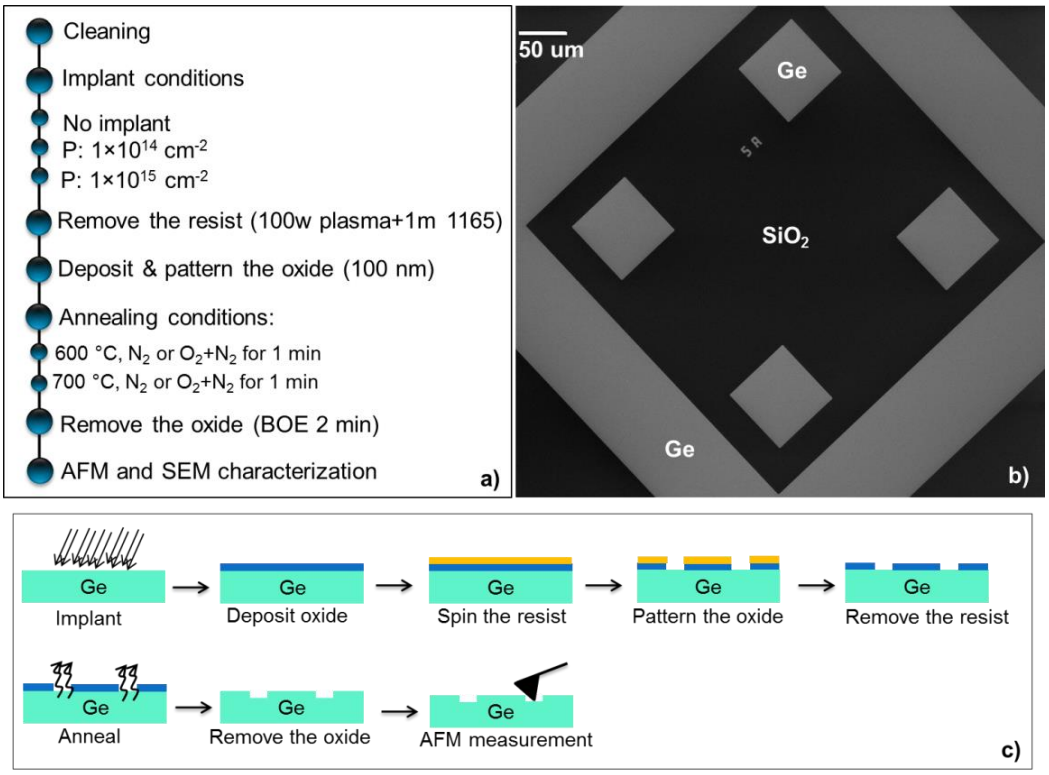


Figure 3.27: a) process flow of the experiment, b) SEM image of the Layout of the test structure. Ge is patterned with SiO_2. c) Schematic of the process flow.

For simplicity we refer to the samples as B and C corresponding to the implant dose they received. A 100 nm thick SiO_2 was deposited by plasma enhanced chemical vapour deposition (PECVD) as the hard mask which was then patterned by lithography (see Figure 3.27 c) leaving some parts of Ge exposed. The photoresist was then removed using 3 min of oxygen plasma followed by 1 min in 1165 solvent which was repeated 3 times. Thereafter the samples were subjected to RTA at 600 or 700 °C for 1 min either in N_2 or N_2 and 10% O_2. As a control case one sample from each set of implanted samples did not receive the RTA. Again corresponding to the implanted dose we name the control samples as control sample A, B and C for no implant, 1×10^{14} cm^{-2}, and 1×10^{15} cm^{-2} dose respectively. The final step was using buffered oxide etch (BOE) to remove the oxide mask for 2-2.5 minutes. The patterned structure is shown in Figure 3.27 c).

We measured step height between covered and uncovered regions as well as surface roughness to determine the amount of Ge substrate loss.

3.4.2 Results of the material characterisation

Initially the samples were visually inspected with SEM. Surface roughness and step height measurements were carried out by AFM in tapping non-contact mode at room temperature on 5×5 μm^2 scanning area. Cross-sectional transmission electron microscopy (XTEM) was also performed to inspect the crystal integrity of the substrate.

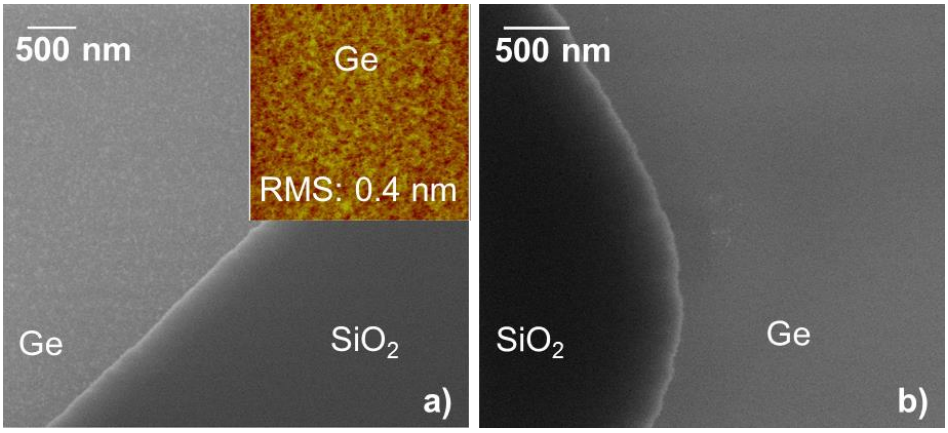


Figure 3.28: SEM image of control samples a) A and b) B before removing the oxide mask. The inset shows an AFM image from the control sample A.

Figure 3.28 shows a representative SEM image from control samples B and C before the hard mask was removed. For both samples after SiO_2 removal surface roughness and step height were approximately 0.4 nm and 4.6 nm respectively.

3.4.2.1 Annealing in N_2 ambient

In Figure 3.29 representative SEM images from a) sample A, b) sample B and c) sample C are shown after being subjected to RTA at 600 °C, for 1 min in N_2. White dots observed in Figures a and b might be due to sample oxidation.

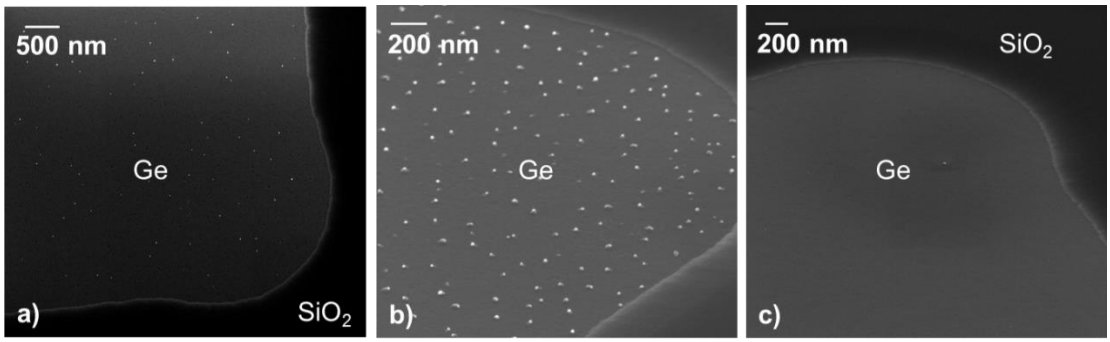


Figure 3.29: SEM images from samples a) A, b) B and c) C after RTA at 600°C, 1 min in N_2.

Similar results were observed after annealing the samples at 700 °C, for 1 min in N_2 expect that there was no oxide left on the surface as it was desorbed at this temperature [150].

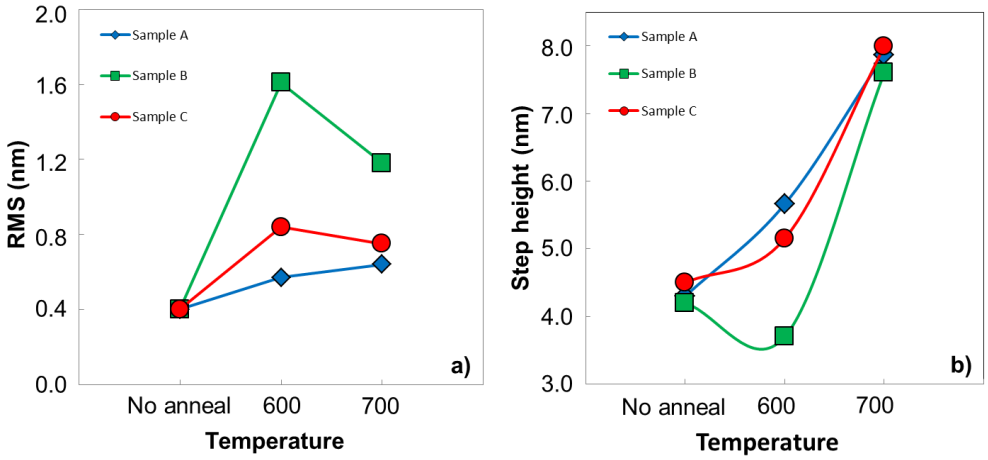


Figure 3.30: a) RMS values and b) step height measurements from samples A, B and C after the RTA treatment. Maximum substrate loss is ~ 4 nm after 700 °C 1 min in N_2.

The graph in Figure 3.30 shows the RMS and step height measurements from the samples annealed at 600 and 700 °C in N_2. We try to analyse the data from

temperature and dose perspectives. With regard to temperature, all sets of samples showed an increased RMS value after they went through RTA treatment.

The sample in group B which are implanted with the lower dose of P exhibit higher roughness compared to group C samples which were implanted with the higher dose of P. The higher RMS value at 600 °C might be related to existence of the small white, germanium oxide, dots on the surface which were desorbed at 700 °C (Figure 3.29) resulting in relatively a smoother surface. Meanwhile the step height measurements showed ~ 4 nm of height difference after RTA at 700 °C.

The aim of this experiment was to investigate the dependency of Ge desorption on the dose of the implant and also the annealing temperature. From these data it appears that the implant dose does not have a significant effect on substrate desorption at least in the scope of this experiment while high temperature annealing can lead to substrate loss only to a very small extent.

Ioannou *et al*. reported significant amount of Ge loss when annealed at different temperatures in N_2 ambient and proposed a desorption model which estimated desorption of approximately 10 nm of Ge after a 600 °C anneal for 1 min [142].

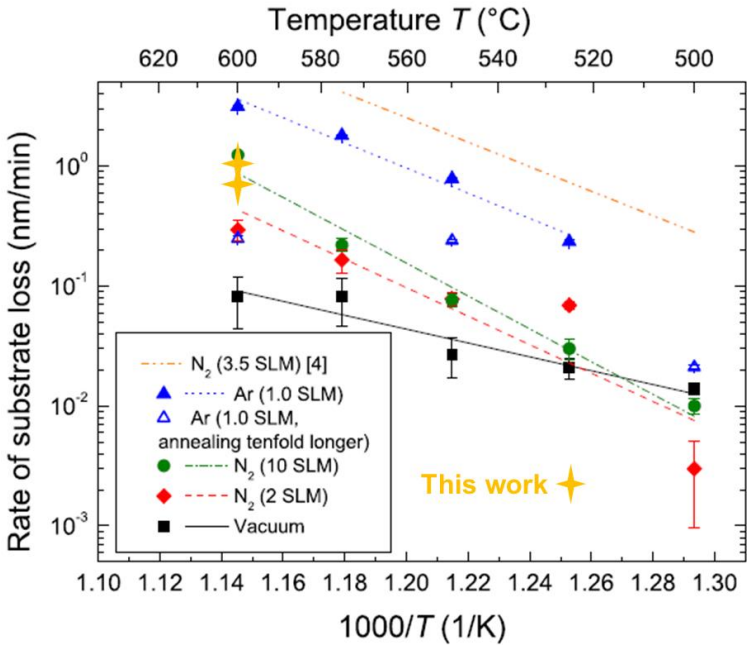


Figure 3.31: Arrhenius plots of Ge substrate loss rate, along with results from Ioannou *et al.* [151]. The obtained substrate loss observed at 600 °C in this study is also included in the graph.

Kaiser *et al.* also studied Ge desorption in different atmospheres (N_2, Ar or vacuum) at temperatures from 500 to 600 °C. They reported around 3 nm substrate loss per min at 600 °C in Ar and observed a noticeable dependence of the rate of Ge loss on the annealing ambient with vacuum ambient more effective to reduce the loss rate [151]. The observed substrate loss at 600 °C in our study seems to be comparable to the reported results in that work as is shown in Figure 3.31.

Referring back to dopant loss issue Figure 3.32 shows the SIMS profile of P. From the measurements it was observed that maximum 4 nm of the Ge substrate is desorbed which corresponds to 30% of the dose in the substrate. In other words if substrate desorption is the main cause for dopant loss then 30% of the dopants are expected to be gone after 600 °C, 30 sec RTA. Nevertheless in our experiment (see 3.3) we observed 70-80% of P dose loss after this annealing treatment which corresponds to approximately 20 nm loss of Ge substrate. So it seems the Ge substrate loss does not account for the dopant loss during the annealing treatments.

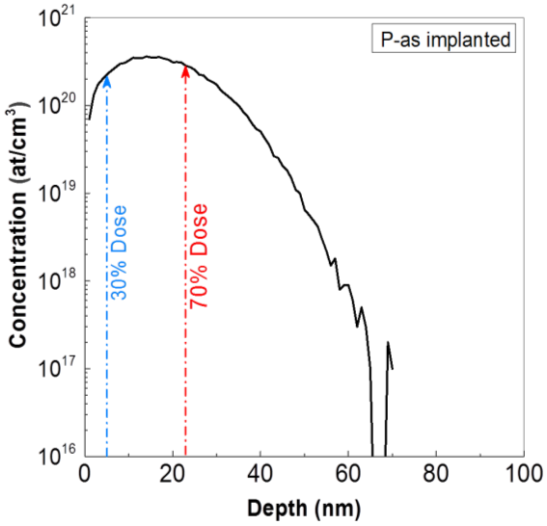


Figure 3.32: SIMS profile of the P implanted sample.

3.4.2.2 Annealing in N_2 and O_2 mix ambient

It is possible that Ge oxidation is engaged in Ge desorption phenomenon. Interestingly the native oxide growth of n-type Ge is faster than p-type Ge, and the oxide is grown layer by layer proven to be atomically flat [152]. It was shown by Oh *et al*. that the native oxide naturally formed in the air is mainly GeO_2 with small amounts of GeO_x (x<2) [153]. Recently Sahari *et al.* grew Ge oxide in the temperatures ranging from 375 to 550 °C and reported an exponential increase in

the oxide thickness above 490 °C due to significant oxygen diffusion in Ge through GeO_2 [154]. Note that GeO_2 is stable up to 1170 °C [155] so, desorption of Ge in the form of GeO_2 is not expected at the temperatures discussed in this thesis.

Ge desorption is perceived to take place in the form of GeO, a successive compound created during/after Ge oxidation at high temperatures [153, 156-158]. Ge oxidation was studies by Oh *et al.* at 450-500 °C RTA in an oxidizing ambient where annealing in N_2 at 500 °C triggered the desorption process [159]. It is suggested that at temperatures 600 °C and above desorption and oxidation are likely to take place at the same time [157, 159]. Kita *et al.* observed oxide thickness reduction from 400 °C [150].

A proposed mechanism for desorption phenomenon is basically decomposition of GeO_2 through a reaction with the underlying Ge substrate leading to formation of GeO [150, 156]. Owing to its temperature-dependent high vapor pressure [154, 157] GeO tends to sublimate at low temperatures. In fact the volatile GeO diffuses through the GeO_2 to the surface and desorbs [160, 161]. Moreover it is shown that along with formation of GeO at the interface loosely bonded Ge atoms are generated that can diffuse to the surface, react with GeO_2 at the surface and reform GeO [158].

In an extensive study on desorption kinetics of GeO from the GeO_2/Ge interface Wang *et al.* suggested that GeO desorption does not occur by a direct-diffusion mechanism. They showed that desorption of GeO is a diffusion limited process depending on the thickness of the oxide layer. They showed that the greater the oxide thickness the higher the desorption temperature. So for an ultrathin GeO_2 (<1nm) desorption temperature is estimated to be around 400°C [162]. Note that in that work the oxide was thermally grown whereas in our experiment only native GeO_2 existed on the sample. Crisman *et al*. found that above 600 °C the growth of germanium oxide is limited by sublimation of GeO from the surface before Ge can be oxidized to GeO_2 [157]. Law *et al.* showed that Ge oxidation is not orientation dependent at and above 550 °C [156]. They reported white deposits on the annealing tool were also and proposed a series of reactions explaining the formation of GeO_2 during the heat treatment [156]

$$Ge_i \rightarrow Ge^{\sigma} \quad \text{(I)}$$

$$Ge^{\sigma} + O_2 \rightarrow GeO_2^{\sigma} \quad \text{(II)}$$

$$Ge^{\sigma} + GeO_2^{\sigma} \rightarrow 2GeO^{\sigma} \quad \text{(III)}$$

$$GeO^{\sigma} \rightarrow GeO_{(g)} \quad \text{(IV)}$$

$$GeO_{(g)} + \frac{1}{2}O_2 \rightarrow GeO_{2(wall)} \quad \text{(V)}$$

where superscript σ refers to material in solid-gas interface, and subscript i denotes the material at GeO_2/Ge interface. As was confirmed by Kita *et al.* loose Ge atoms created during the GeO_2/Ge reaction at the interface diffuse through the oxide to the surface where they react with GeO_2 and reform the volatile GeO which desorbs at the surface in gas form [150]. In presence of O_2 in the annealing ambient it is likely that GeO reacts with oxygen and re-produces GeO_2 which is deposited on the walls of the chamber.

Minimizing the GeO desorption is an open debate since it causes surface roughness, a quite undesired effect that rises difficulties in number of Ge-based device fabrication steps such as formation of low resistance contacts or hi-κ dielectrics. It is suggested that lowering the oxidation temperature to 400 °C can reduce the vapor pressure of GeO and withhold the desorption, as well as high pressure oxidation [160]. Also a capping layer can block the GeO out diffusion [150].

In order to study the effect of oxygen on substrate desorption we annealed one set of samples in an annealing ambient mixed of N_2 and 10% O_2.

Figure 3.33 depicts representative SEM and AFM images from samples A, B, and C after RTA at 600 °C in N_2 and 10% O_2 and after 2-2.5 min BOE treatment for SiO_2 removal. As it can be seen in the image regardless of the implant dose significant amount of Ge is desorbed and large regular facets are formed on the substrate.

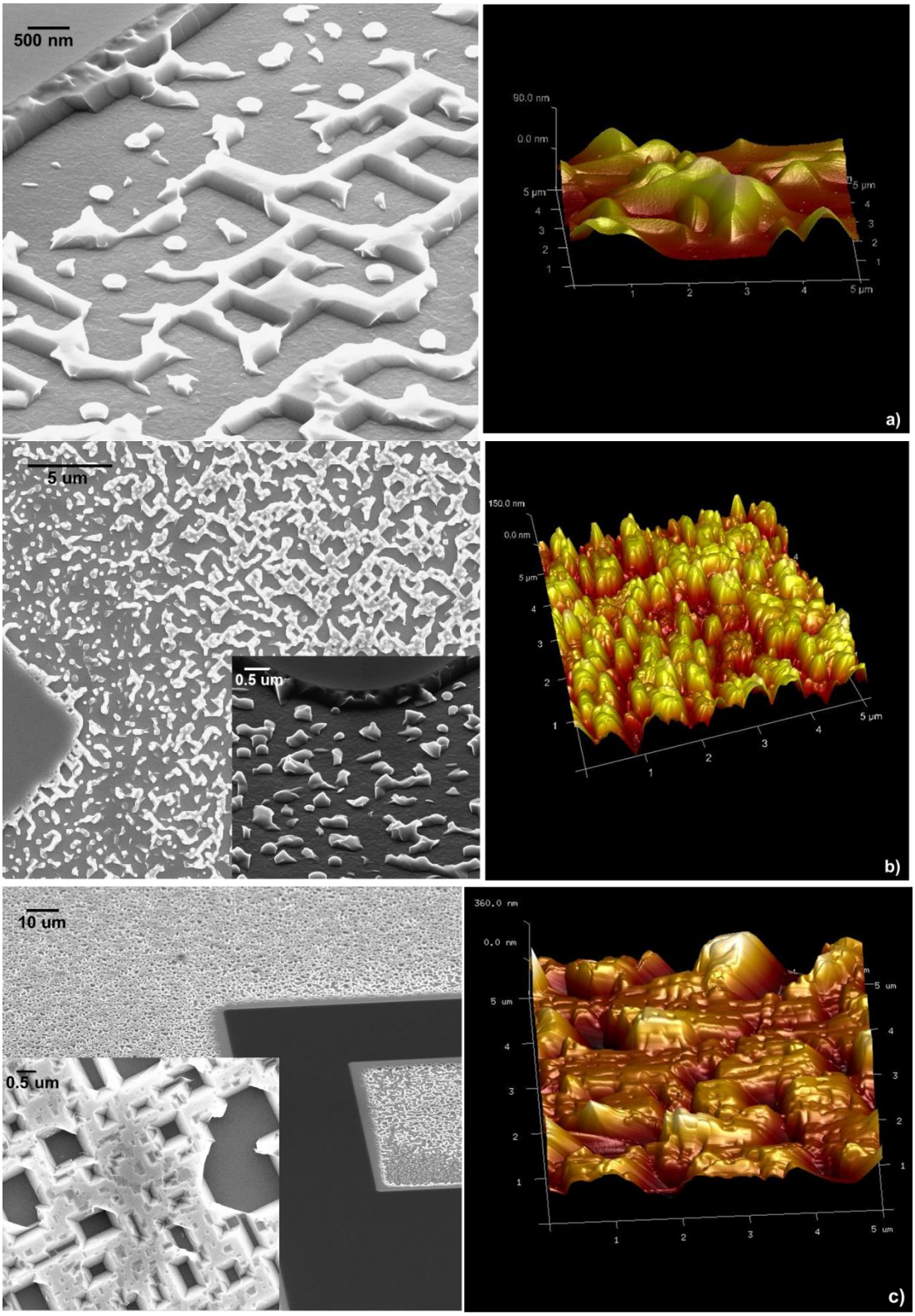


Figure 3.33: SEM image of samples a) A b) B and c) C after 600 °C anneal in N_2 and 10% O_2 ambient, and BOE treatment. Large and deep facets of Ge are formed due to non-uniform desorption of GeO.

In contrast to Si where crystal orientation contributes to the oxidation rate, it was revealed by Law *et al.* that oxidation rate for all three faces of Ge, (100), (110) and (111), is independent of the orientation except at 500 °C where oxidation of the (111) face is more pronounced [156]. The regular facets that were observed in this experiment are probably due to a non-uniform desorption process [162].

By cross-sectional TEM imaging (Figure 3.34) the nature of these regular facets was confirmed to be crystalline Ge with a thin layer of native oxide on top.

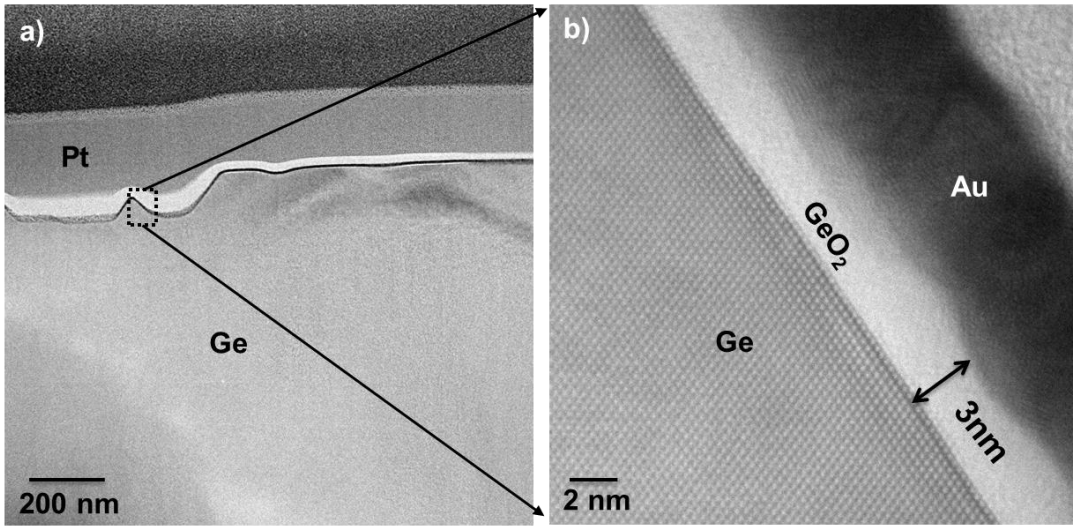


Figure 3.34: a) XTEM image of high implanted sample subjected to 600 °C anneal in N_2 and O_2 ambient, and b) zoomed in view of the interface.

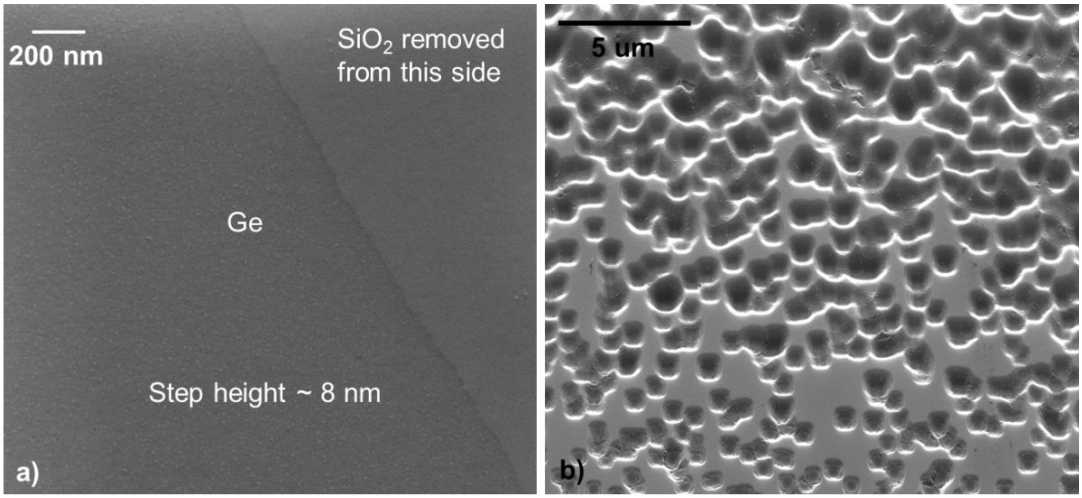


Figure 3.35: SEM images of sample C after a) RTA at 700 °C in N_2, and b) 700 °C anneal in N_2 and 10% O_2.

As a comparison Figure 3.35 shows SEM images from sample C after RTA at a) 700 °C in N_2, and b) N_2 and 10% O_2, where Figure 3.35 a) shows a relatively smooth surface, and Figure 3.35 b) shows a drastically deteriorated surface due to

oxidation and desorption of the Ge substrate. Unlike the results from the 600 °C anneal no facets were observed in the SEM here. In fact GeO is desorbing at a different rate so it looks different after the annealing treatment.

Figure 3.36 shows the corresponding AFM images to Figure 3.35 a) where Ge surface roughness after the annealing treatment and the step height after oxide removal were measured.

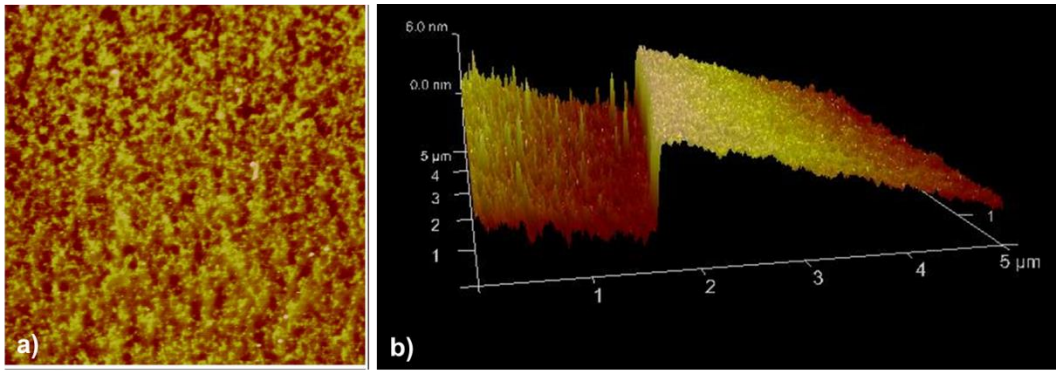


Figure 3.36: a) surface topography and b) step height measurement of sample C after RTA at 700 °C in N_2.

Representative SEM and AFM images taken after RTA at 700 °C in the oxidizing ambient are presented in Figure 3.37 and show a) sample A before oxide removal, b) sample B before oxide removal with the inset showing a zoomed in view of the exposed Ge surface after BOE, and c) sample C before the BOE treatment with the inset showing same sample after BOE. In order to fully remove the oxide BOE treatment for longer than 2 min was required as the SiO_2 became denser and harder to remove after the RTA. Again neither the regular facets nor the oxide is seen in these images. Instead, a damaged and deteriorated surface is created in all groups of samples regardless of the implant conditions. Deep voids are formed due to significant amount of Ge desorption induced by high annealing temperature and the oxidizing ambient.

More importantly, white colour deposits were observed on the covering plate of the RTA tool above the specimen after the oxidation run. As mentioned earlier, there is no chance that Ge could have evaporated in the form of GeO_2 as it is stable at this temperature. This observation can be explained considering the mix N_2 and O_2 annealing ambient in which the gaseous GeO reacts with the oxygen and re-

produces GeO_2 which is deposited on the walls of the chamber. White deposits after annealing were also reported by Law *et al.* [156].

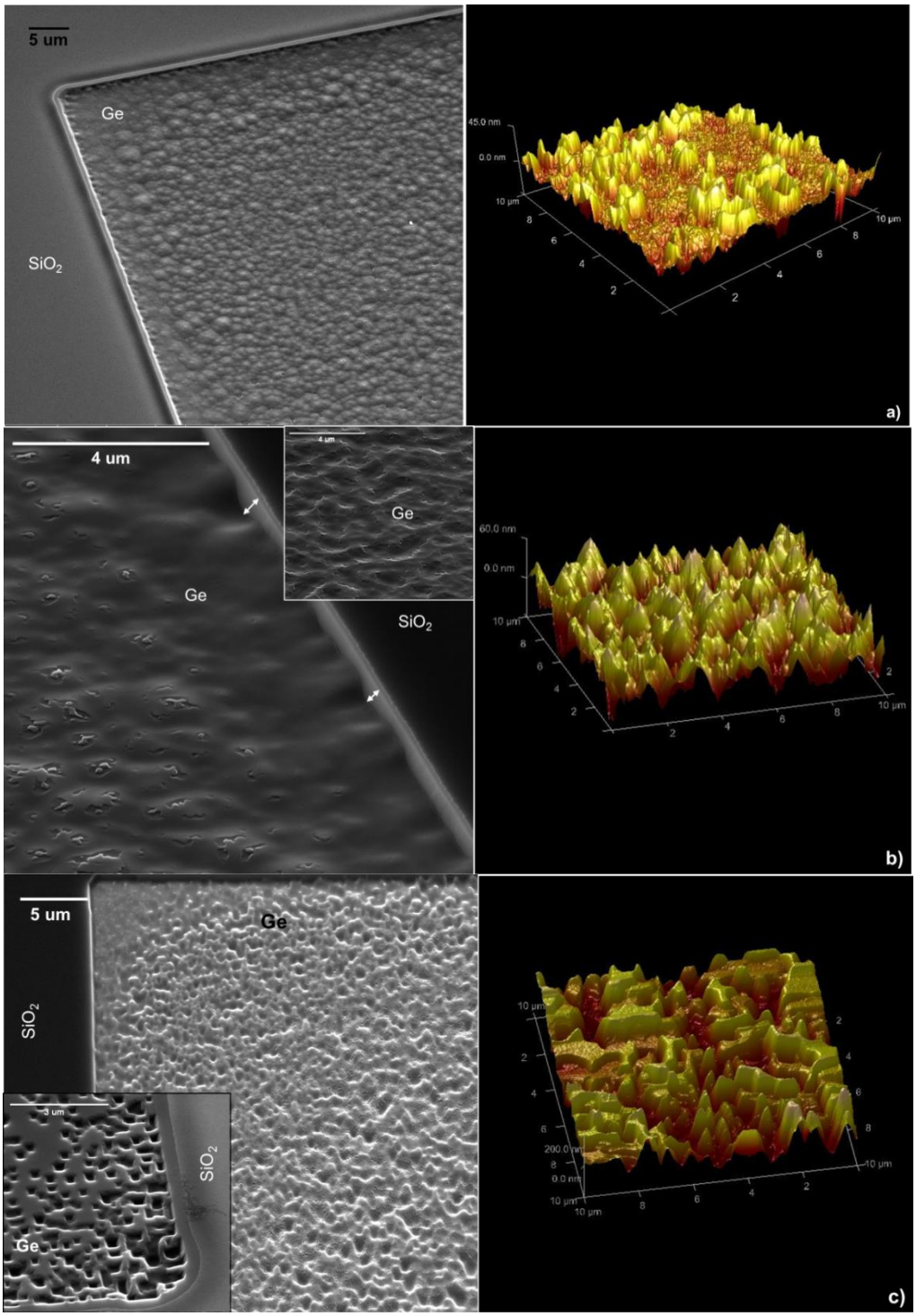


Figure 3.37: SEM and corresponding AFM images from the samples after RTA at 700 °C in N_2 and 10% O_2 showing: a) sample A before the oxide mask was removed, b) sample B before using BOE, with the inset showing a zoomed-in image from the Ge substrate showing a coarse surface caused by desorption, and c) sample C before using BOE. The inset shows a zoomed-in view of the sample after BOE.

Step height measurements were not performed on these samples due to height limits of the AFM measurement tool. However from SEM imaging it was estimated that at least 300 and in some cases more than 500 nm of the substrate was lost.

The primary aim of this experiment was to correlate the Ge substrate desorption with the amount of dopant loss. The oxidation experiment was a complementary test to see the effect of oxygen on Ge during the inevitable high temperature treatments (such as dopant activation) for device fabrication. In fact in order to grow GeO_2 one does not need to go above 500-550 °C. From these data it appears that the implant dose not have a significant effect on substrate desorption at least in the scope of this experiment while high temperature annealing can lead to substrate loss only to a very small extent.

In order to clarify the dopant loss process we carried out residual gas analysis (RGA) using an XPS equipped with a quadrupole and heating stage.

The measurement process is illustrated in Figure 3.38. The quadrupole detects the gaseous materials coming from the Ge substrate as it is heated. As the Ge wafer is heated the gaseous materials come from the surface and can be detected by the quadrupole. The pressure change of the XPS chamber is plotted versus the atomic mass unit of the material at each temperature. The result is a profile for particular atomic mass units, from which one can estimate at what temperature species of interest are out-gassed.

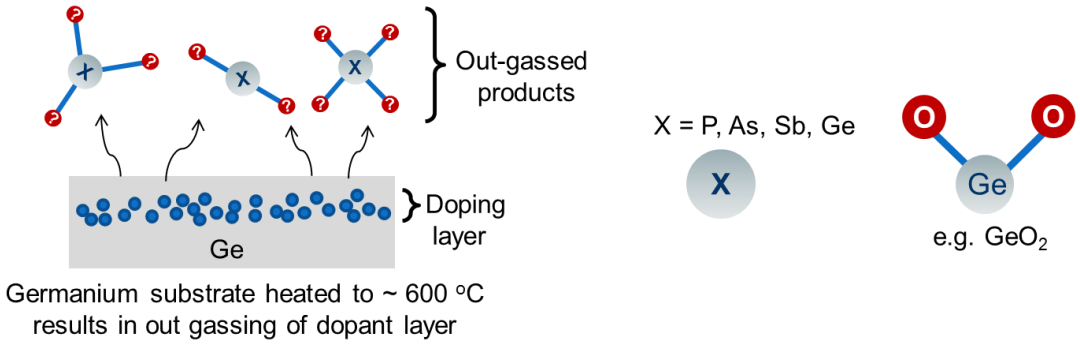


Figure 3.38: Identifying out-gassed products using gas chromatography mass spectrometry.

At this point in time the experiments are ongoing. Data is being collected for a variety of samples including unprocessed Ge and Ge with dopants implanted. We also intend to collect mass spectrometry data from the chamber without a Ge

sample processed as a baseline. Preliminary data indicate that this technique can detect the out-gassing of implants from Ge such as F and P while the concentration of Ge is too low to detect.

3.5 Conclusion

In this chapter a number of dopant related issues in Ge were discussed. First, material and electrical characteristics of n+/p junctions in Ge formed by RTA and LTA process techniques were compared. High carrier concentration (> $10^{20}cm^{-3}$) was accomplished using LTA for activating the dopants and also removal of the crystal damage induced by ion implantation. ECV and Hall Effect data indicate almost 100 % activation of the dose that was retained. Furthermore high quality n+/p junction diodes were demonstrated with I_{ON}/I_{OFF} ratio ~ 10^7 and I_{ON}/I_{OFF} ratio~ 10^5 for RTA and LTA samples respectively. In order to achieve highly activated dopants and high I_{ON}/I_{OFF} ratios more optimization needs to be done to fine tune the LTA process. Also more analysis is required to pinpoint the nature of the mechanism involved in extraction of activation energy greater than 0.67 eV in RTA Ge diodes.

Also, it was proposed that F which is the most common non-dopant co-implant for point defect engineering in Si, is unlikely to be as useful in Ge. We have shown that F has only a minor effect on P and As diffusion, due to extreme F outgassing, which is related to the diffusion, and clustering behaviour of F in Ge. F concentrations in the high 10^{20} cm^{-3} range may be required to create stable F_nV_m clusters, however high implant doses into Ge often risk irreversible substrate damage. Thus, if attempted, care must be taken in that experimental space.

Next, we investigated the correlation between dopant loss and Ge substrate desorption, and conclude that the Ge desorption does not explain the dopant loss mechanism. Annealing in N_2 at 700 °C caused approximately 4 nm of substrate loss per minute. Annealing in O_2 lead to severe surface deterioration and roughening. XPS analysis is ongoing into the study of dopant out-gassing as mass spectrometry can detect species emanating from Ge samples during thermal treatments.

Chapter 4

Fins, Resistors, and Thin Body Devices

4.1 Introduction

The origin of multigate field effect transistors (MugFETs) goes back to 1989 when Hisamato *et al*. reported a new vertical ultrathin MOSFET [163]. Having the advantage of suppression of short channel effects and improved gate control, this new architecture is considered as a solution to the challenge of transistor shrinkage. Yet, development of these devices comes with its own issues like fabrication, doping, and characterization [164]. Figure 4.1 shows configurations of vertical transistors.

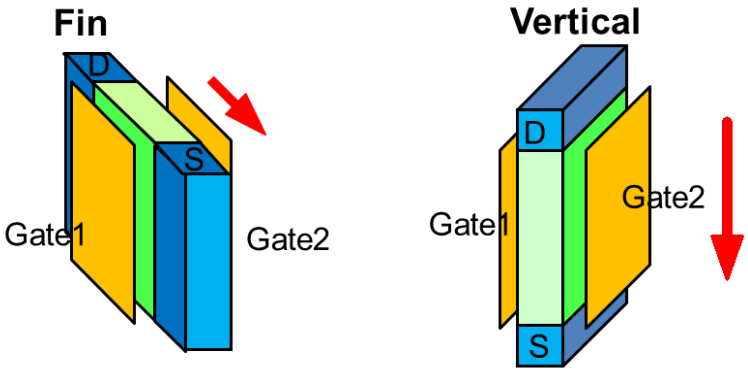


Figure 4.1: Different configurations of vertical transistor.

Doping thin-body features is a difficult task, in order to get the impurity atoms into the structure, activate and prevent them escaping during thermal treatments. A pre-requisite for desirable gate performance in these devices is scaling down the fin widths [165] but this is accompanied by an increase in parasitic source-drain resistance (R_{SD}) [166, 167].

In order to reduce the R_{SD} it is necessary to maintain the crystal integrity of the semiconductor crystal, which is not very straight forward in ion implanted structures. In the case of planar substrates the amorphous layers regrow from bottom to the top during thermal annealing, whereas in case of narrow structures

like fins recrystallization happens from the bottom to the top and also along the edges as is shown in Figure 4.2. Duffy *et al.* reported a problematic solid phase epitaxy (SPE) in thin body Si fins where formation of twin boundary effects and poly crystalline grains deteriorated the re-crystallization mechanism [166].

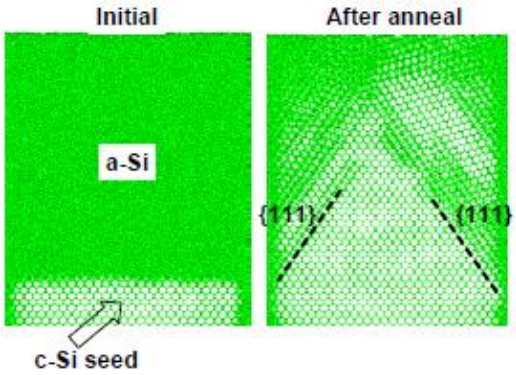


Figure 4.2: Initial and final configurations in a Molecular Dynamic simulation of recrystallization process in thin body Si structure [92].

Lateral SPE (L-SPE) has also been investigated as a method to form Si on insulator (SOI) substrates. In that case the SPE growth front moves laterally over the oxide layer, parallel to the Si surface. In an extensive study by Kunii *et al.* it was shown that during the growth amorphous/crystalline facets form mainly due to the boundary between Si and SiO_2. As is shown in Figure 4.3 a) during vertical growth no facet is formed at the SiO_2 stripe edge. SPE at a short distant from Si/SiO_2 interface is normal and no facet is formed. Figure 4.3 b) shows a lateral growth where the growing layer is bounded by the SiO_2 film and the native oxide layer. It was shown that the facet orientation is determined by the orientation of the crystalline Si seed [168].

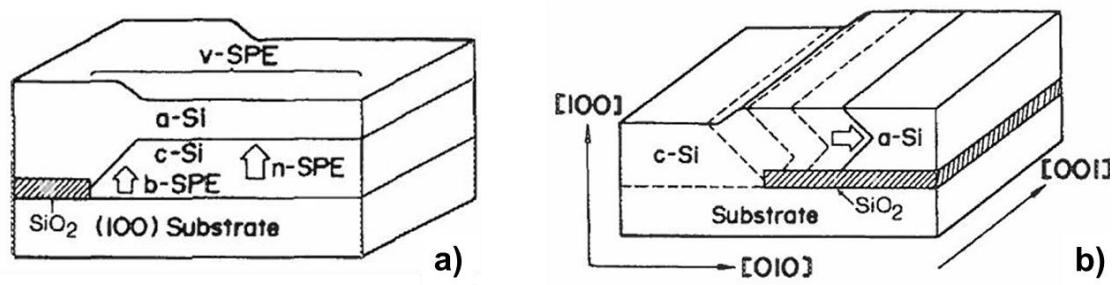


Figure 4.3: Schematic diagram showing a) bounded and normal vertical SPE, and b) lateral growth and bounded SPE. Copyright 1984 American Institute of Physics [168].

Formation of these facets can slow down the SPE and in severe cases there is chance for poly crystalline grains to form which is known as random nucleation growth (RNG).

Another solution to suppress R_{SD} is replacing ion implantation technique with non-destructive conformal doping methodologies.

Several techniques have been proposed for doping Si fin structures such as heated implantation [93], plasma doping [169], atomic layer deposition [170], vapor phase doping [95], molecular layer deposition [171], and self-regulatory plasma doping [172].

Contrary to Si, standard implants can easily amorphise Ge [173] at room temperature. Therefore it is essential to introduce and apply non-destructive doping techniques for Ge fin structures.

In this chapter we study the issues associated with ion implantation in Ge fin structures by looking at simulations of several ion implantation conditions in thin body structures followed by studies on SPE in wide and narrow fin test structures. Subsequently we implement a non-destructive dopant in-diffusion MOVPE-based process to dope the fins, and investigate the electrical properties of P and As doped structures.

4.2 SRIM (The Stopping and Range of Ions in Matter)

In favor of computer-aided design tools, modelling has become a fundamental technique in design, understanding and development of semiconductor devices. It enables the designer to apply varieties of conditions that affect the physical properties and performance of the device, and pick out the most promising fabrication parameters. Several simulation tools can be used to collect and analyze the data and finally fabricate the device. SRIM is modelling software providing a simulation environment to study the ion implantation process and physics which is a conventional and crucial step in making semiconductor devices. For a better understanding some concepts that are frequently used in SRIM software are first explained.

4.2.1 Definitions

The classical transfer of energy between an ion and a stationary atom in the target depends on the mass of both particles and also on the speed and direction of the moving particle. When a moving particle is passing through the material the stationary particle recoils and absorbs the energy and the incident ion gets deflected. Interaction of the ions with the target particles are known as electronic and nuclear collisions as is shown in Figure 4.4. The implant damage is caused by nuclear collisions which can displace the target atoms from their lattice site and the energy lost due to this is called non-ionizing energy loss [174].

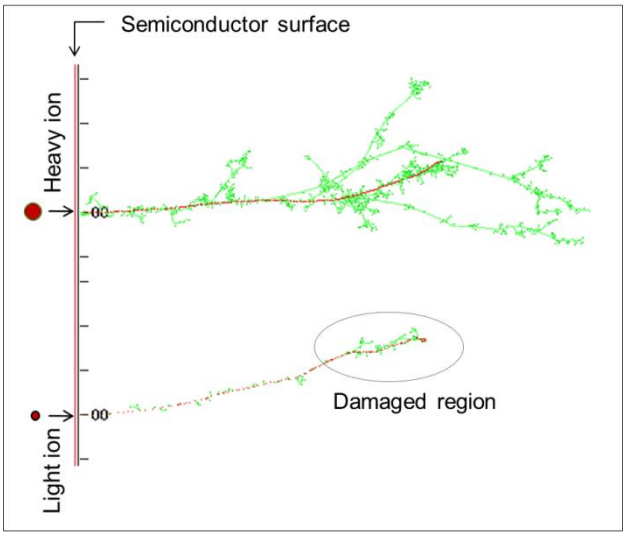


Figure 4.4: Schematic representation of the disorder caused by ion implantation [175]: light ion-increased disorder as the ion penetrates the target, and heavy ion-uniform disorder along the entire ion trajectory.

In order to have better understanding and evaluation of the damage caused by energetic ions, we need to get familiar with definitions below [63]:

- Displacement: The process through which the atom is knocked off the lattice site.
- Vacancy: An empty lattice site caused by displacement (see Figure 4.5).
- Interstitial atoms: Are the incident ions that come to rest in the target, and also the target atoms that are ejected from the lattice site and stop in the solid (see Figure 4.5).
- Displacement Energy: The minimum energy needed to knock a target atom far enough away from the lattice site, so that it will not return back

immediately. This minimum energy can produce a “Frenkel Pair” consisting of a vacancy and an interstitial created when an atom is removed from the lattice site. Frenkel Pair is the fundamental type of damage caused by an ion.

- Lattice Binding energy (LBE): The minimum energy required to break the electronic bonds and remove an atom from the lattice site. Lattice binding energy is smaller than displacement energy, as in this case the atoms are displaced from the lattice site but do not have enough energy to leave the lattice site, and may come back to their previous positions.
- Surface Binding Energy (SBE): Is the energy required to take an atom from the surface of the material. Atoms at the target surface are not bound on one side, and have fewer bonds that should be broken, and it is easier to remove them from the target than if they were in the lattice site. Surface binding energy is an important factor in damage evaluation as it can directly affect the sputtering.
- Final energy of the moving atom: The energy below which the ion is considered to be stopped.

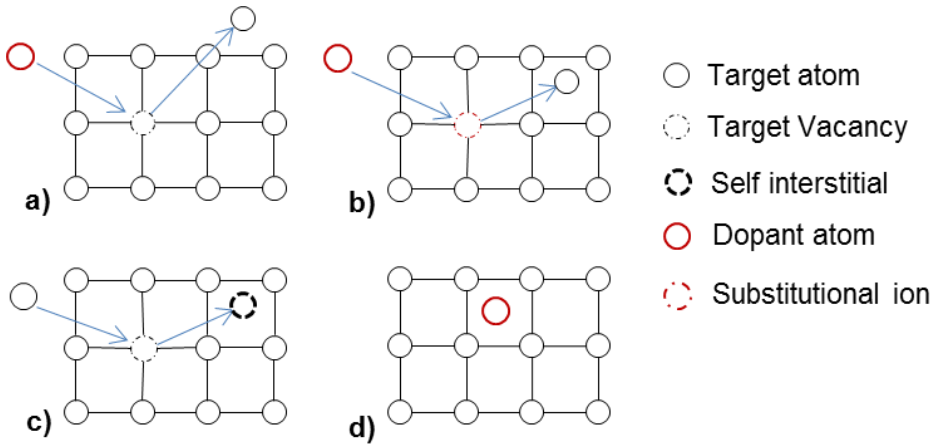


Figure 4.5: a) The incoming ion has knocked out the lattice atom and created a vacancy, b) The incoming ion takes the place of the target atom after giving it enough energy to leave the lattice and becomes a substitutional ion, c) the recoiling target atom, if energetic enough, can collide with other target atoms in the lattice and knock them out. After losing its energy the recoiling atom resides in the lattice and becomes a self-interstitial, d) Eventually, the incoming ion stops in the target and becomes an interstitial.

4.2.2 Modelling of ion implantation in C, Si, Ge and III-V materials

Modelling has been done for three different ions, B, As, and Sb, each with two energy values. The implant angles are 0°, 45°, 60°, 75°, 80°, and 85° in order to

mimic the conditions in a FinFET device. Target materials are Ge, Si, C, GaAs, $In_{0.53}Ga_{0.47}As$, and GaN. The width of the target is 10 nm, and 10000 ions are modelled to generate reliable results. Backscattering, transmission, vacancies created in the target, sputtering and the amount of retained dose are the extracted parameters in this modelling. In Table 4.1 the simulation conditions are summarized.

Table 4.1: Simulation summary carried out in this study.

Target materials	Si	Ge	C	GaAs	InGaA	GaN	SiO_2
Implant species and energies	B	0.5	2 keV				
	As	1 keV	5 keV				
	Sb	2 keV	6 keV				
Implant angles	0°	45°	60°	75°	80°	85°	
Implant ions	10000						
Target material thickness	10 nm						

The species and energies of the ion implants were chosen to reflect typical ultra-shallow junction formation for advanced technologies. Table 4.2 summarizes important parameters as determined in SRIM that affect the features of interest. Energy values shown in the table are the default values taken from SRIM software. As is shown in the table displacement energy and lattice binding energy are considered identical in Si and Ge, although in [176] displacement energy of Ge is reported to be 30 eV. Note that surface binding energy is not known for many substances, and in SRIM it is an estimation of the sublimation energy (SE) of the materials. Atomic density denotes to the number of atoms in one centimeter cube. For example, there are 8 Si atoms in a unit cell which has a volume of 1.6×10^{-22} cm^3, corresponding to the atomic density of 4.96×10^{22} (cm^{-3}).

Figure 4.6 shows a schematic of possible sources of dopant loss during the ion implantation into the fin structures which can be classified as:

- Backscattering: The ions may bounce back from the target after one or more collisions with the stationary atoms.
- Transmission: A number of implanted ions can leave the target from the other side of the fin.
- Sputtering: As a result of ion bombardment an amount of the target material is removed from the target.

Table 4.2: Properties of target materials defined in SRIM [63].

Materials	Density ($g.cm^{-3}$)	Average atomic mass	Atomic density (cm^{-3})	Disp. energy (eV)	LBE (eV)	SBE (eV)
Si	2.329	28.1	4.96×10^{22}	15	2	4.7
Ge	5.323	72.6	4.42×10^{22}	15	2	3.88
C	2.235	12	1.14×10^{23}	28	3	7.41
GaAs	5.318	144.64	4.42×10^{22}	25	3	Ga(2.82) As(1.26)
InGaAs	5.504	259.46	3.98×10^{22}	25	3	In(2.49) Ga(2.82) As(1.26)
GaN	6.1	83.73	8.79×10^{22}	Ga (25) N (28)	3	Ga(2.82) N (2)
SiO_2	2.329*	60.08	2.27×10^{22}	Si (21) O (22)	Si (2.1) O (2.2)	Si(3.1) O(3.2)

* Different values are reported for SiO_2 density. Here we report the values applied in SRIM database.

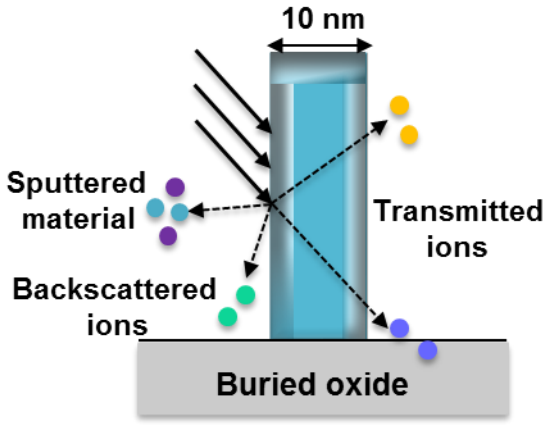


Figure 4.6: Schematic diagram showing the concept of Backscattering, Transmission and Sputtering.

4.2.3 Backscattering

One of the effects of ion implantation is backscattering where the ions are ejected from the target after one or more collisions. Backscattering is affected by the energy and the mass of the ion, the angle of the incident beam, and the density of the target material. In this study impact of different dopants with two different energies is investigated. Figure 4.7 represents bakscattered ions from B 0.5 and 2 keV

implantations. The simulations for Arsenic implants were similar to B, thus are not shown. Figure 4.8 depicts the results for Sb with 2 and 6 keV energies.

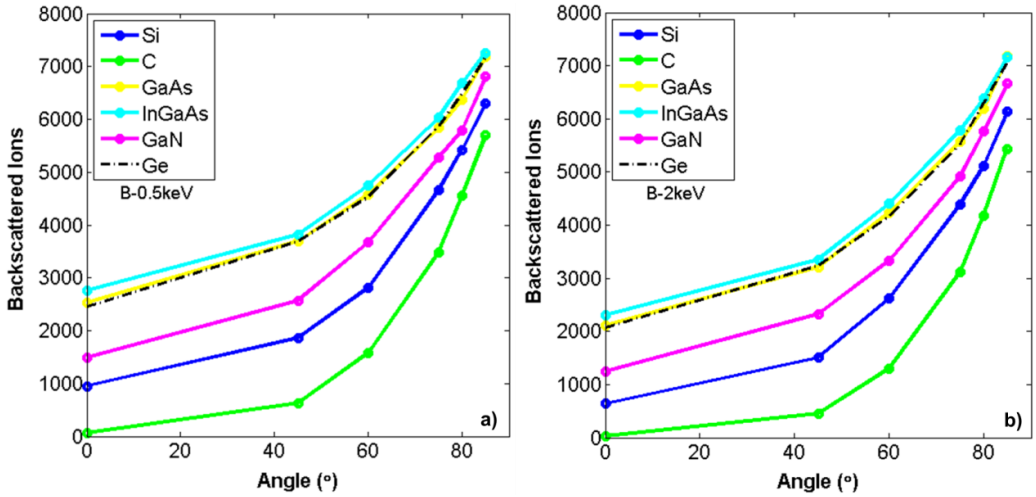


Figure 4.7: SRIM simulations showing backscattered ions from 10000 B ions implanted at a) 0.5 keV and b) 2 keV energy.

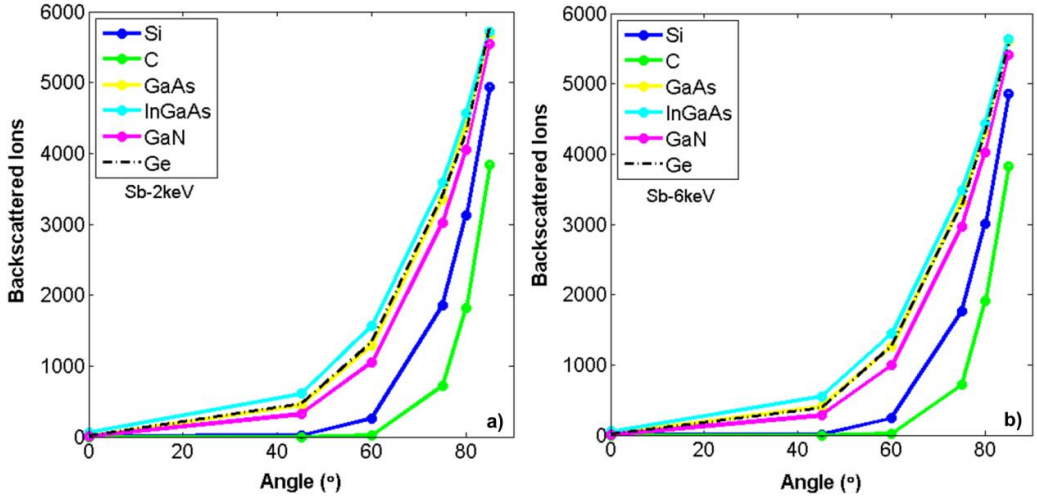


Figure 4.8: SRIM simulations showing backscattered ions from 10000 Sb ions implanted at a) 2 keV and b) 6 keV energy.

In theory, interaction of the ions with a denser material ends in more backscattered ions compared to a material with low density. The trend in the figure justifies this explanation. At the bottom of the plot lies C which is the least dense material, and has the smallest number of backscattered ions. Next, is Si with a slightly greater density and greater number of ions scattered back from the target. GaN is exceptional may be due to the average atomic mass of the material. B atomic mass is close to that of N so it is more likely that the B and N colissions result in displacement of the N atom rather than backscattering of the B ion.

Therefore the total number of the backscattered ions is more than Si and less than Ge target materials.

The average mass of the substrates can be a reasonable answer to this exception, which begins with C as the lighter one, continues with Si, GaN, Ge, GaAs, and ends with $In_{0.53}Ga_{0.47}As$ as the heaviest one. Ge, GaAs, and InGaAs have similar densities and average mass and the backscattering rate in these substrates is similar as well. Backscattering increases as the implant angle changes from 0° to 85°. In fact at bigger implant angles the transverse force of the impinging ion reduces by a cosine factor of the incident angle, and thus it is more likely that ions bounce back after collisions with target atoms.

B 2 keV implant results in a similar graph, where in C lowest number of ions and in $In_{0.53}Ga_{0.47}As$ highest number of ions are backscattered. Comparing the figures one can find out that B 2 keV dopants are less backscattered than B 0.5 keV implants. This, is due to the higher energy of the atoms that enables them to get deeper into the target. Backscattering is also influenced by the properties of the target material. Since B is much smaller that the target atoms e.g. Ge, Ga, In, and As, it is more likely to bounce back in the collision with these atoms and leave the target.

Figure 4.8 shows the results for Sb with 2 and 6 keV energies that are similar to what were obtained in B implantation, however the number of backscattered ions has reduced significantly. For example in C at 0° and 45° no backscattering has happened. Atomic mass of Sb is much higher than atomic mass of B therefore the Sb ions are not easily scattered by the lighter target atoms such as C and Si. However collisions with target atoms with comparable atomic mass units enhances the likelihood of backscattering of Sb ions.

As was observed in B the quantity of backscattered Sb ions enhances by the increased incident angle

Figure 4.9 shows schematic of the implant angles and the effect of the cosine factor which is fading in bigger incident angles.

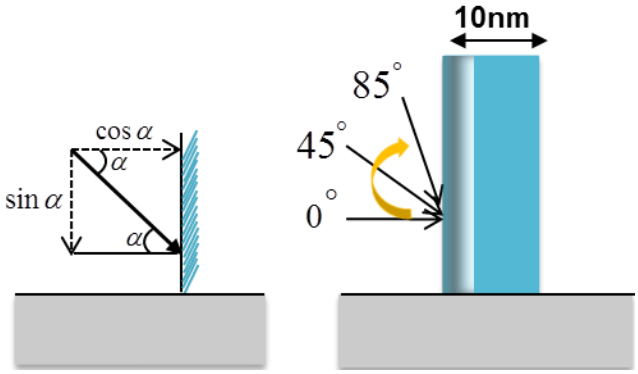


Figure 4.9: Schematic diagram showing the implant angles and the effect of the cosine factor.

From the figures it appears that all the variables strudied in this study can influence the backscattering and are summarized as:

- Target material: a denser material leads to more backscattering.
- Energy and the species of the incident ion: in a particular angle the heavier ions and also those with higher energy are backscattered less than lighter or less energetic ions. For example, in Ge, at any angle B is backscattered more than Sb.
- Implant angle: more ions backscatter from the material surface at bigger implant angles.

4.2.4 Transmission

Transmission or channeling during implantation occurs when some ions pass through the substrate and exit the other side. It should be noted that SRIM assumes the target material is amorphous and therefore crystal channeling effect cannot be included in the simulations. Figure 4.10 and Figure 4.11 depict the simulation results where a decreasing trend of transmission can be observed for higher incident angles.

Regarding Figure 4.10 during B 0.5 keV implantation no transmission occurred in C and GaN which have the highest atomic density values. This is an indication that the ion has more chances to hit the target atoms, lose energy and come to rest with most probably nuclear collision interactions. Much of the same can be said for Si, Ge ,and GaAs. The transmission rate in Ge and GaAs is similar as the density of both materials is similar. $In_{0.53}Ga_{0.47}As$ has the least atomic density among all the

studied materials (see Table 4.2) and show higher transmission of B ions at all the incident angles.

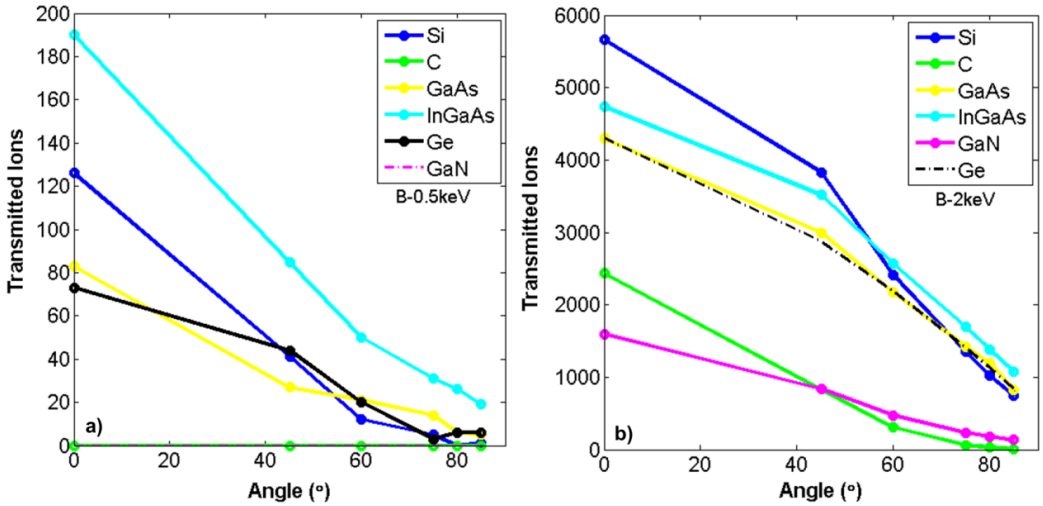


Figure 4.10: SRIM simulations showing transmitted ions from a) B 0.5 keV and b) B 2 keV implants.

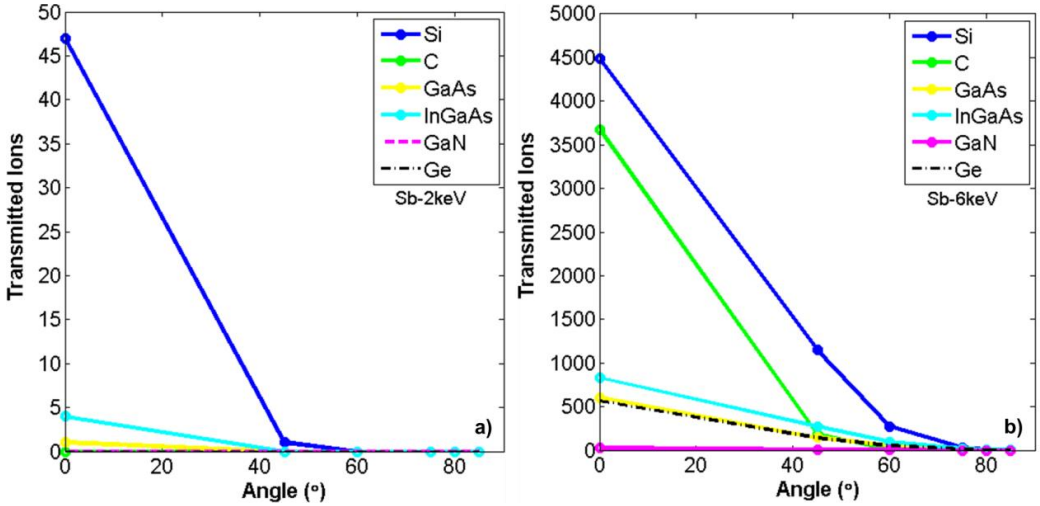


Figure 4.11: SRIM simulations showing transmitted ions from a) Sb 2 keV and b) Sb 6 keV implants.

The considerable amount of B 2 keV ions transmitted through the target materials compared to B 0.5 keV verify that impurities with enough energy and momentum are able to go deeper into the crystal and probably exit the other side.

Oblique angles result in the reduction of the energy of the incident ion by cosine factor of the implant angle, hence less transmission will occur. As is shown in Figure 4.11 a) Sb 2 keV ions pass through only Si and $In_{0.53}Ga_{0.47}As$ at zero angle, and are mostly retained in or backscattered from the other target materials. More ions pass through the substrate when the ion beam is perpendicular to the fin

whereas at oblique implant angles (75, 80, and 85°) Sb ions are either retained in the target material or backscattered from it. Similar trend is observed for Sb 6 keV implant, with C showing the second highest transmission rate. This can be attributed to the low atomic density of the material. Overall from the data it seems that the transmission rate is primarily a factor of density and secondly affected by the atomic density of the target material.

Comparing the Sb implants with B and As for the same implant projected range, it seems that heavier ions are less transmitted than lighter ones. This is due to the lower straggle when using a heaver mass ion during the implant. Overall more transmission happened for:

- Lighter ions
- Smaller implant angles
- Less dense target materials

4.2.5 Retained dose

In Figure 4.12 the retained ions in the substrate after B implant at a) 0.5 keV and b) 2 keV are shown. Retained ions from the lower energy implant follow a decreasing trend at more oblique-angled incidents. As is shown in Figure 4.12 a) the maximum retained dose of B 0.5 keV implant belongs to C where backscattering and transmission rates are very small. It seems that for low energy and light ion implants the best angle in terms of retained dose is the normal incident. The sequence of the substrates in terms of the retained ions is understandable considering the backscattered and transmitted ions at this implant condition as well as properties of the target materials. In fact retained dose is calculated from

$$retained\ dose = implant\ dose - (backscattered + transmitted) \qquad (4.1)$$

For the B 2keV implant the retained dose in the materials is limited by transmission and backscattering below and above 45° implant angle respectively. In Figure 4.12 b) it is observed that for Si the best implant angle is 60° where more ions are retained in the substrate. Similar to B implant at 0.5 keV the best implant angle for Ge, GaAs, GaN and InGaAs is the normal implant.

Figure 4.13 a) shows the retained ions after Sb 2 keV implant. As is shown in the plot most of the ions are retained in the target at 0° and 45° implants, and start a decreasing trend at higher implant angles. For Sb 6 keV the retained dose tend to increase by the incident angle in C and Si until 60°.

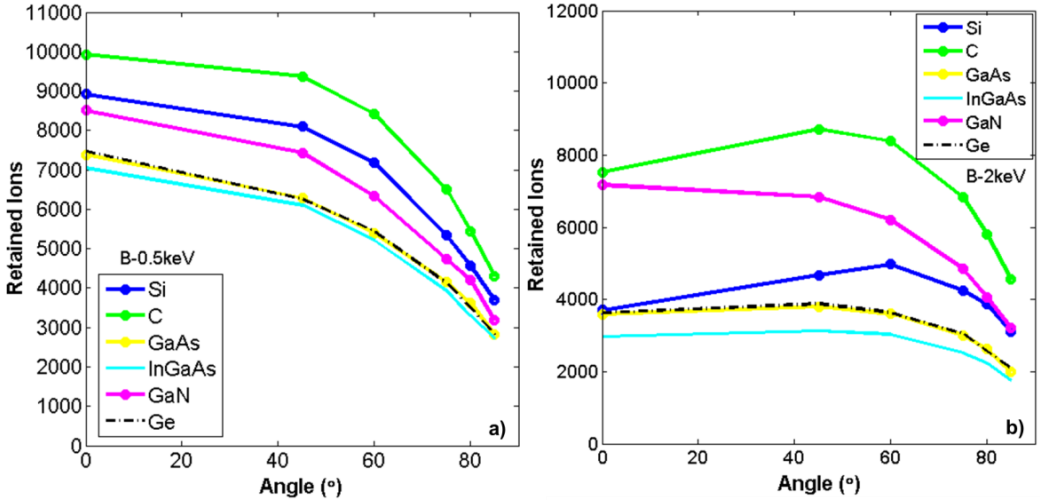


Figure 4.12: Retained ions after B implant at a) 0.5 and b) 2 keV.

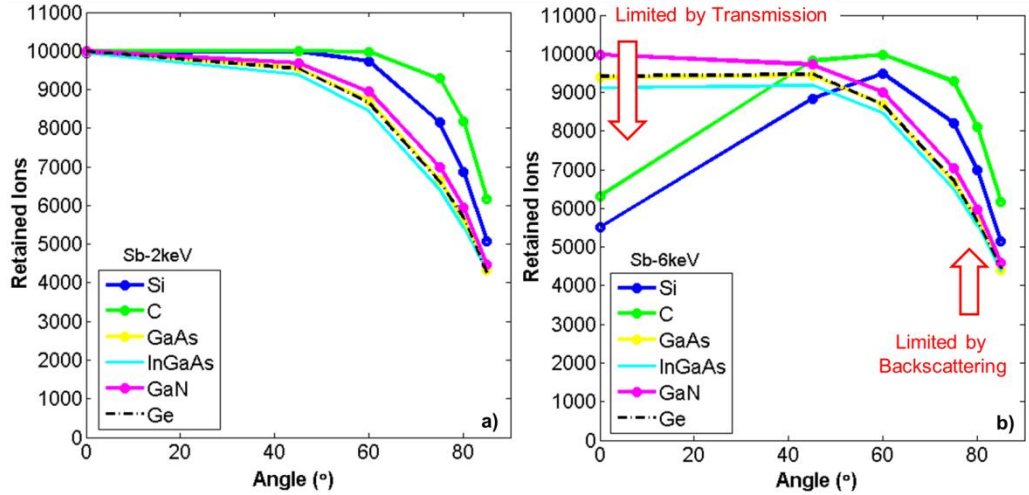


Figure 4.13: Retained ions after Sb implant at a) 2 and b) 6 keV.

Due to high number of backscattered ions at bigger incident angles the retained ions are reduced. However, the retained ions in the other target materials follow a similar trend to Sb 2 keV implant. Similar results were obtained from simulations of B and As implants on Si fin structures by Pelaz *et al.* [92].

Dose retention depends on the angle of incidence. High angle ion implants are equivalent to high number of backscattered, small number of transmitted and retained ions in the targets. At a specific angle the lighter ions are more likely to

leave the target due to transmission and backscattering, therefore heavier ions (Sb) are more suitable for dose retention. Different retained dose will result in different levels of diffusion, since the most common dopants experience the concentration-enhanced diffusion during RTA [177].

Note that in practice in planar structures dopant outgassing can influence the retained dose in the substrate, and could apply to thin body structures as well.

4.2.6 Vacancy

Vacancies are the empty sites generated when the target atoms are moved from the lattice positions. The number of vacancies is affected by the correspondent displacement energy which is the minimum energy required to knock out a target atom far enough from the lattice site so that it will not go back immediately. Vacancies are made when the incoming ion has the energy which is high enough to eject a target atom from the lattice site. If the energy of the recoil atom is still greater than the displacement energy it may create further vacancies by hitting other atoms in the target [63]. Regarding the displacement energies reported in Table 4.2, it is relatively easier to remove atoms from the lattice site in Si, and Ge, compared to III-V materials and also in C. Probably that is the reason for low number of vacancies in C, and high number of vacancies in Si, and Ge after B 0.5 keV (see Figure 4.14).

Figure 4.15 shows the plots from vacancies formed by Sb implants at 2 and 6 keV. The number of vacancies created by each dopant varies by changing the incident angles, and in some cases follows an ascending and then a descending trend. By increasing the angle the normal implant energy is reduced by the cosine factor of the incident angle which means the ions have less energy and thus can generate fewer vacancies.

From the simulations it appears that more vacancies are generated in the following situations:

- Higher mass of the incoming ion
- higher energy of the incoming ion
- low displacement energy of the target material

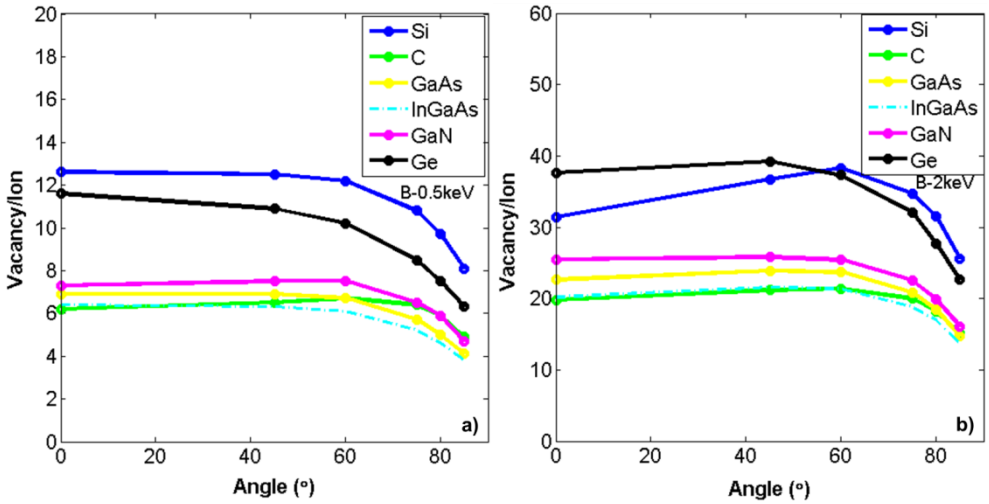


Figure 4.14: SRIM simulations showing the number of vacancies generated after B implant at a) 0.5 keV and b) 2 keV.

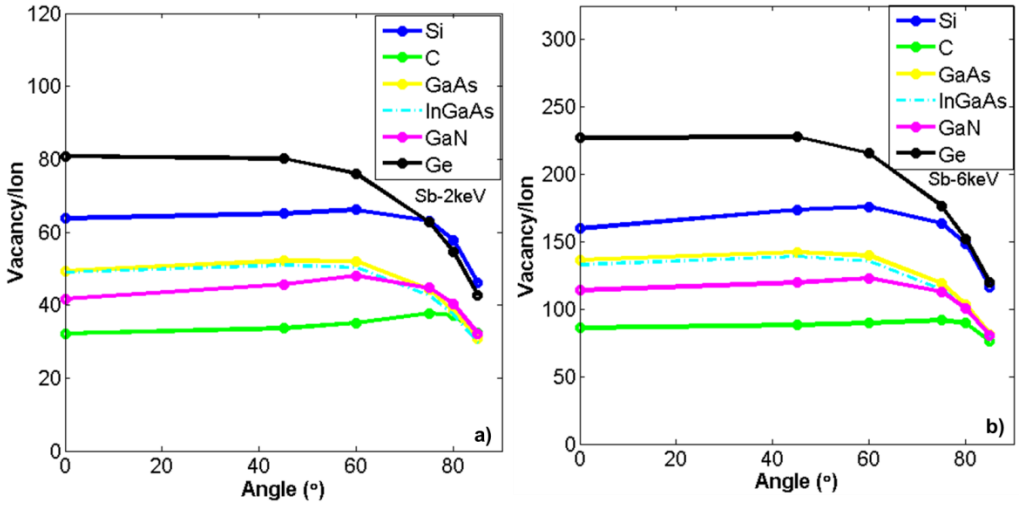


Figure 4.15: SRIM simulations showing the number of vacancies generated after Sb implant at a) 2 keV and b) 6 keV.

4.2.7 Sputtering yield

Removal of the near-surface atoms from the target is called target sputtering. When the energy of the ion is greater than the surface binding energy of the substrate the atoms can be emitted from the surface. "Sputtering Yield" is defined as the mean number of atoms sputtered per incoming ion. LBE and SBE are important parameters in sputtering yield. Sputtering makes the substrate rough and damaged. As a consequence the surface atoms are fastened to the lattice by fewer bonds so the SBE is reduced allowing more target atoms to leave the material. In SRIM calculations this effect is not taken into account so the calculated sputtering yield is

underestimated [63]. Sputtering mostly happens in the nearest layer to the surface but some of the recoil cascade atoms exiting the target might have originated from deeper inside than just the surface. The simulation results for sputtering in B and Sb implants are shown in Figure 4.16 and Figure 4.17 respectively.

In order to get a better overview of the sputtering process, the number of atoms sputtered in each implantation was converted to thickness of the material removed from the target during the process using

$$Sputtered\ \ Width = \frac{Dose\ \left(atoms \cdot cm^{-2}\right) \times Sputtering\ \ Yield}{Atomic\ Density\ \left(atoms \cdot cm^{-3}\right)} \tag{4.2}$$

where the dose is 1×10^{15} cm^{-2}.

Changing the incident angle from 0° to 85° leads to increase and then decrease in the sputtering yield. Referring to Figure 4.7 we know that backscattering follows an ascending trend when the implant angle is changed. It means that at angles bigger that 60°, significant number of ions are lost without having an impact on the target, so the number of ions that have enough energy is decreased, and sputtering is decreased as well. Moreover, at high energies the ion maintains its original direction along a nearly straight flight path, and transfers a little energy near the surface, but transfers much energy close to the surface when travels at grazing incident angles [178]. The influence of the angle on the sputtering is governed by the surface structure of the target.

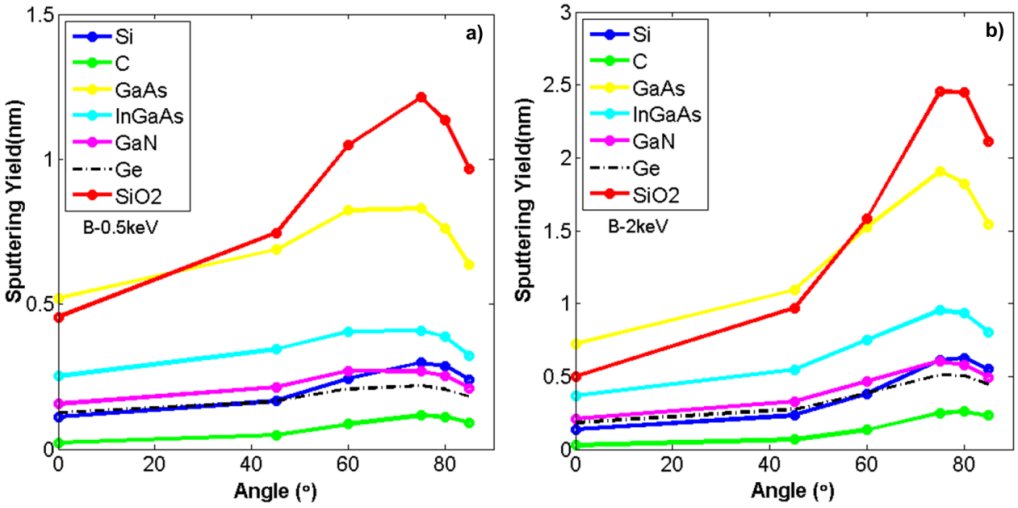


Figure 4.16: Sputtered width after B implant at a) 0.5 keV and b) 2 keV.

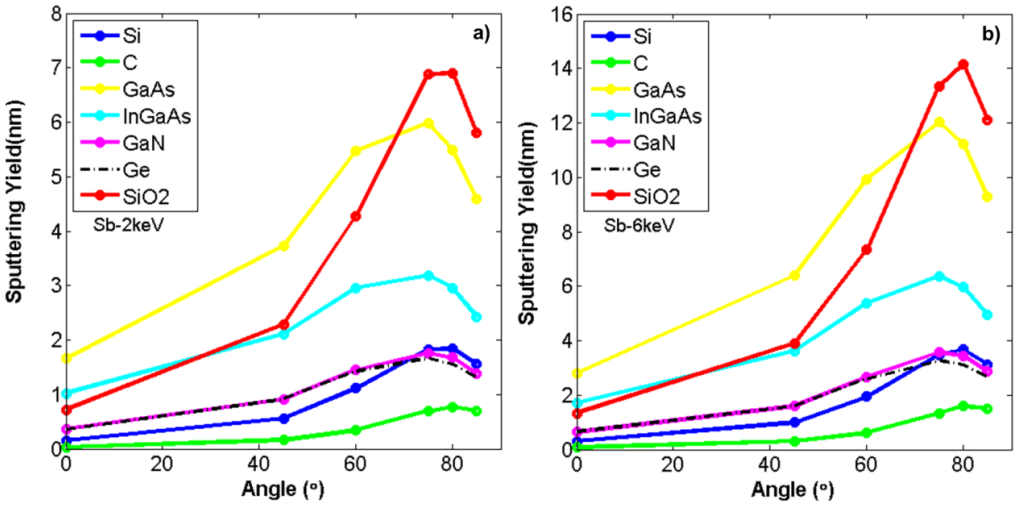


Figure 4.17: Sputtered width after Sb implant at a) 2 keV and b) 6 keV.

SBE in Ge is less than that of in Si and C, which implies that the sputtering in Ge is higher than sputtering in Si, and C. SBE is different for each component in GaAs, In0.53Ga0.47As, and GaN, and is less than Ge, Si, and C (see Table 4.2). Therefore the sputtering yield in these materials is higher than the other materials. Also, sputtering yield in Ge at zero angle is slightly higher than Si which is consistent with the SBE. The simulations on As and B implanted Si fin structures by Pelaz et al. show a similar trend as what was obtained in our study [92]. The high sputtering yield obtained for SiO2 is due to the low atomic density of the material.

Figure 4.17 shows the Sputtering yield after Sb implant. The trend is similar for both energy implants with dramatic increase in the amount of sputtered material at 60° implant angle and above. Again C has the lowest sputtering rate, followed by Si. The sputtering rate for Ge and GaN appears to be very close. Atomic density of the materials together with the number of atoms that are removed from the surface can give a reasonable answer to this result. For example the number of ions that are removed from GaN per incoming ion is approximately twice than that of Ge due to the smaller SBE in GaN.

According to the material properties presented in Table 4.2 the atomic density of GaN is twice the atomic density of Ge, meaning that in a centimeter cube of GaN there are two times more atoms than there are in a centimeter cube of Ge. This would lead to erosion of relatively similar thickness of both materials during the implantation (see equation (4.1)). Same interpretation applies to $In_{0.53}Ga_{0.47}As$, SiO_2, and GaAs.

In practice one option for reducing the amount of sputtered material is using a mask on the target, and it means the amount of energy to get the desired profile of impurities should increase in order to be able to pass the mask and reside at the desired depth. SiO_2 was studied to observe the sputtering rate, and it is shown that SiO_2 itself is sputtered quite quickly.

Looking at the data one can figure out the effect of the dopant on the sputtering yield where heavier ions and higher energy implants have resulted in greater sputtering yield. Implantation in multi-element targets can lead to preferential sputtering. If one of the components is not bound to the lattice as strongly as the other ones then the incoming ion will transfer more energy to it and the ion will be sputtered more, hence the substrate is enriched in the second component. For instance in GaAs, sputtering rate (see Figure 4.18) of As is almost twice the sputtering rate of Ga, which is the consequence of the respective SBEs.

Surface sputtering was recently reported by Kelly *et al.* who investigated the structural transformation in Ge nanowires during ion irradiation, and observed a reduced nanowire diameter from 22 nm to 16 $\pm$ 3 nm , with undulating facets [179].

In conclusion the sputtering yield is more pronounced in materials with

- lower SBE
- lower atomic density

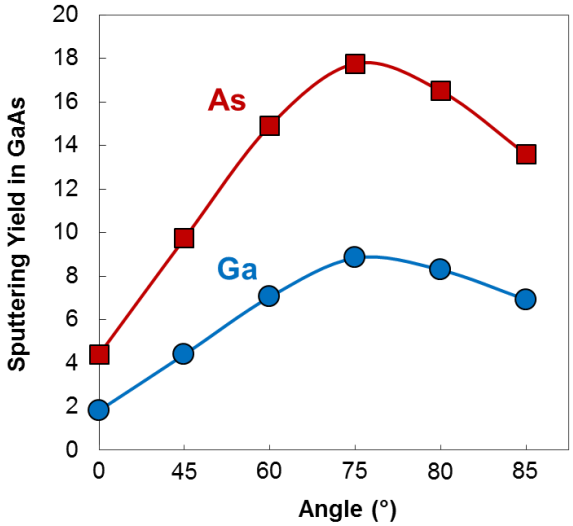


Figure 4.18: Sputtering yield of Ga and As. Sputtering rate of As is twice Ga corresponding to SBE of As which is half of the SBE of Ga.

4.2.8 Limitations of SRIM

In this section we critically analyse the data generated by SRIM. The Ge database is not as complete and mature as Si; hence some of the parameters are taken from Si like displacement energy and LBE. This might affect the results obtained in vacancy and sputtering yield sections.

SRIM code is based on binary collision approximation (BCA) taking into account only the collision between the incoming ion and the closest target atom [180]. Generally the implantation-created damage in the target material is associated with elastic collisions transferring energy to the target atoms which if high enough (> displacement energy) can knock off the atom from lattice site and form Frenkel pairs. Based on extensive studies by Tejido *et al.* [180] BCA underestimate the damage generated in real implantation process, whereas the energy transferred below the threshold displacement energy can impose a significant amount of damage and should be considered in damage calculations. In SRIM the target material in assumed to be amorphous and the effect of damage clusters are not considered in the simulations. Besides, implantation in crystalline substrate cannot be studied using this software.

A comprehensive analysis of the effects of irradiation in thin body structures demands a focused research on modelling adopting various frameworks and simulation techniques which is beyond the scope of this dissertation. The simulations carried out in this work were done in order to gain a general understanding of ion implantation and corresponding effects in thin body structures.

4.3 Recrystallization of thin-body Ge structures

Non-planar thin body structures are proven to be the ultimate architectures for the advanced CMOS devices, and include semiconductor-on-insulator, double or tri-gate, multi-gates and nanowires. From experimental point of view it is still unclear whether Ge FETs can outperform Si FETs or not. However a modelling analysis by Eneman *et al.* showed that n-type Ge FETs can offer better performance than Si due to higher intrinsic mobility, 1.1 times more on the top and 6 times more on the sidewalls of the fins. Electron mobility in Ge shows the highest value at (111)

orientations [181]. Also SiGe S/D is an effective stressor for Ge and can boost the device performance. Meanwhile p-type Ge FETs can beat Si through embedded stressors [182]. Albeit before achieving this breakthrough other known issues with Ge need to be resolved.

4.3.1 State-of-the-art work

In contrast to Si, Ge FinFET devices have been limited to p-type channels, with mostly ion implantation for source/drain doping. The smallest fin width reported to date is 20 nm. Ge p-channel FinFETs with fin widths (W_{fin}) of 130-350 nm were fabricated by Feng *et al.* [183]. Hutin *et al.* demonstrated p-channel MOSFETs with W_{fin} = 30 nm on ultrathin germanium-on-insulator substrates by Ge enrichment technique [184]. Van Dal *et al.* reported scaled p-channel Ge FinFET devices with W_{fin} of 40 nm, fabricated on a Si bulk wafer [21, 185] using Aspect-Ratio-Trapping technique. Liu *et al*. fabricated p-type Ge FinFET devices with W_{fin} = 60-100 nm [186]. Ikeda *et al.* reported p-type Ge nanowire FET devices with W_{fin} = 20 nm [187]. P-channel MUGFET Ge transistors on GeOI with in-situ B doped raised S/D and W_{fin} = ~ 67 nm where reported by Liu *et al.* [188]. Recently a body-tied Ge tri-gate junctionless P MOSFET with a gate length of 120 nm was demonstrated by Che-Wei *et al.* [189].

The reported results on p-channel Ge FETs are promising, however plenty of problems still exist that should be resolved especially for n-type Ge fin structures.

In this section we study the crystal integrity and SPE after ion implantation in wide and narrow n-doped Ge fin test structures.

4.3.2 Experimental procedure

Unimplanted pre-cleaned (100) Ge wafers were patterned using e-beam lithography with various doses ranging from 70 μC/cm^2 to 110 μC/cm^2. At 25 °C, a SF_6 /C_4F_8 plasma process was used for etching. The drawn fin widths were 200, 150, 100, 75, 60, and 50 nm with resulting widths of 150 to 20 nm. Figure 4.19 represents top down view of the test structures with Ge fins running in [110] and [100] directions. SEM imaging was performed to characterize the fins.

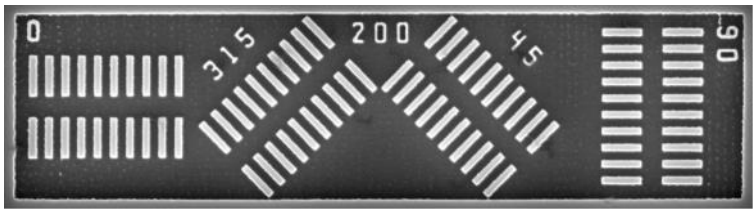


Figure 4.19: SEM image of Ge fin structures patterned in [110] and [100] directions. Fins are 1 µm long and the pitch is 400 nm within each array.

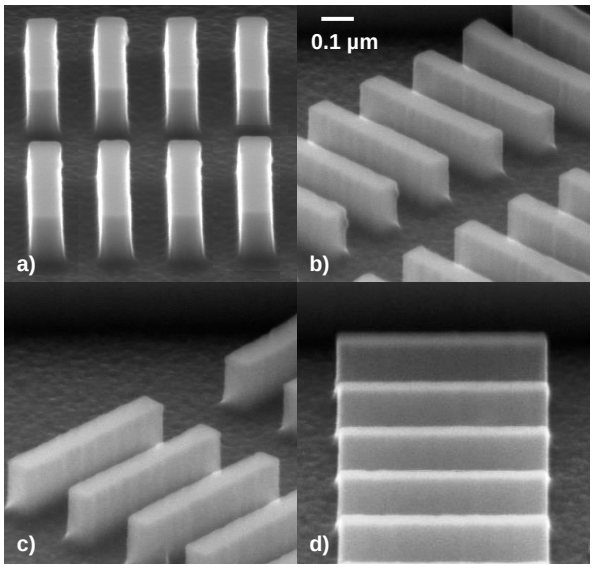


Figure 4.20: Tilted SEM image of germanium fin structures patterned by 90 µC/cm^2 e-beam dose, running in a) and d) [110], b) and c) [100], directions. In this case fin widths are 130-150 nm.

A zoomed in image of the fins is shown from different perspective in Figure 4.20. To study recrystallization phenomena in Ge fins, another sample patterned with 70 and 90 µC/cm^2 doses were subjected to phosphorus implantation at 7º with a dose of 1×10^{15} cm^{-2} and energy of 60 keV. Cross-sectional TEM was carried out using JEOL2100 operated at 200 kV.

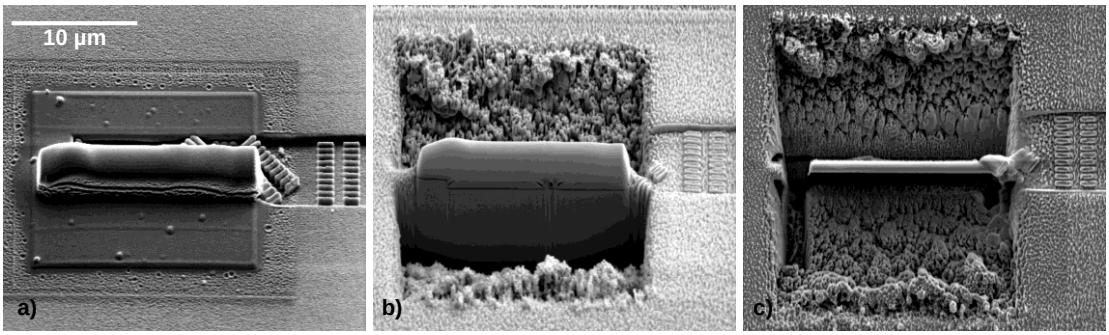


Figure 4.21: SEM image of the sample preparation process including: a) carbon and platinum deposition, b) tilted view during FIB milling, c) plan view of the sample after FIB milling.

For sample preparation which is shown in Figure 4.21 a thin layer of carbon followed by platinum were deposited on the region of interest prior to focused ion beam (FIB) milling processes. Ge fins were studied (i) as implanted (not annealed), (ii) after a 3 min anneal at 400 ºC in N_2. The lowest e-beam dose, 70 µC/cm^2, resulted in thicker fin widths with worse line edge roughness as is shown in Figure 4.22.

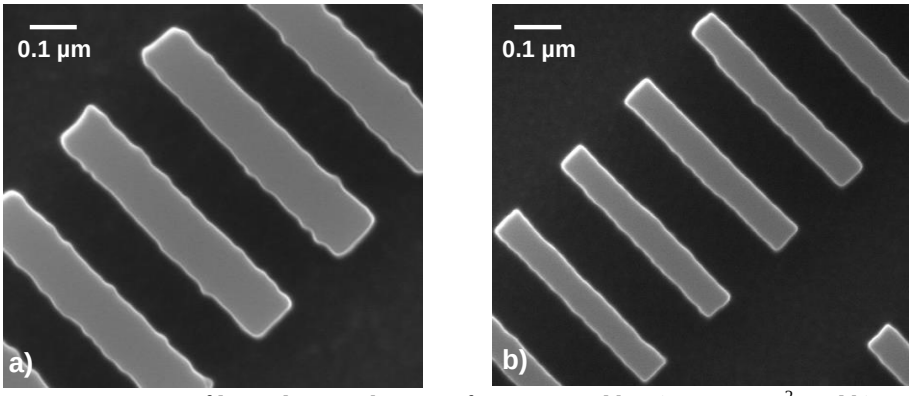


Figure 4.22: Comparison of line edge roughness in fins patterned by a) 70 µC/cm^2, and b) 90 µC/cm^2 e-beam doses.

4.3.3 Amorphisation and Recrystallization

Surface proximity and random nucleation regrowth (RNG) are reported as key challenges in the realization of sub-20 nm wide silicon fins [166]. An equivalent study for Ge is needed for both wide and narrow fins. A schematic of the implant and amorphisation procedure is depicted in Figure 4.23.

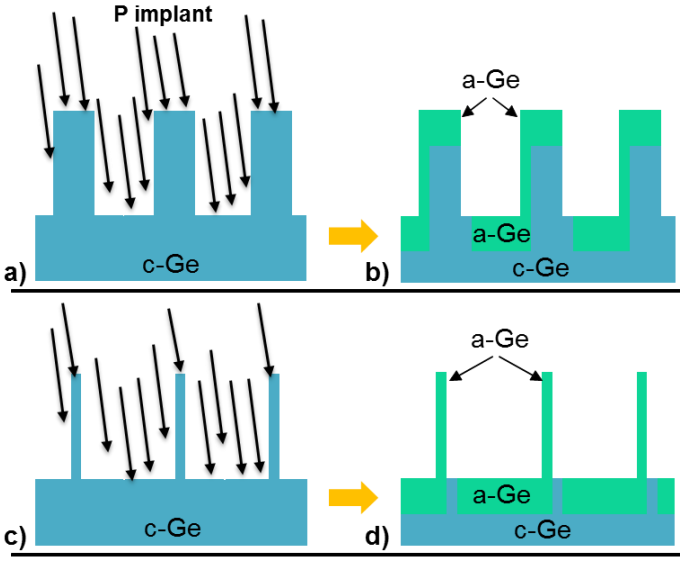


Figure 4.23: Schematic diagram showing a)7° phosphorous implant in wide germanium fins, b) the fins after implant left partially amorphous, c) narrow germanium fins subjected to implant and d) completely amorphous fins after implant.

Figure 4.24 a) shows a TEM image from an array of wide Ge fins where the top 120 nm of the structures was amorphized due to the implantation. In this part of the experiment the fins are approximately 450 nm tall and 105 nm wide. Narrow fins with 20-25 nm width were completely amorphized under the same implant conditions. In the following, bright-field TEM images homogeneous gray regions are amorphous Ge and dark features are defects. The shown images are a representative selection of a larger set of images. The intrinsic Ge recrystallization rate is ~ 2 nm/s for 400 °C anneal [190], therefore after 3 minutes all the Ge is expected to be recrystallized. Fins are partially amorphized on the top and in the trench. Deposited carbon and platinum layers are also seen in the image. Figure 4.24 b) illustrates the fins after a 400 °C 3 min anneal where SPE is complete.

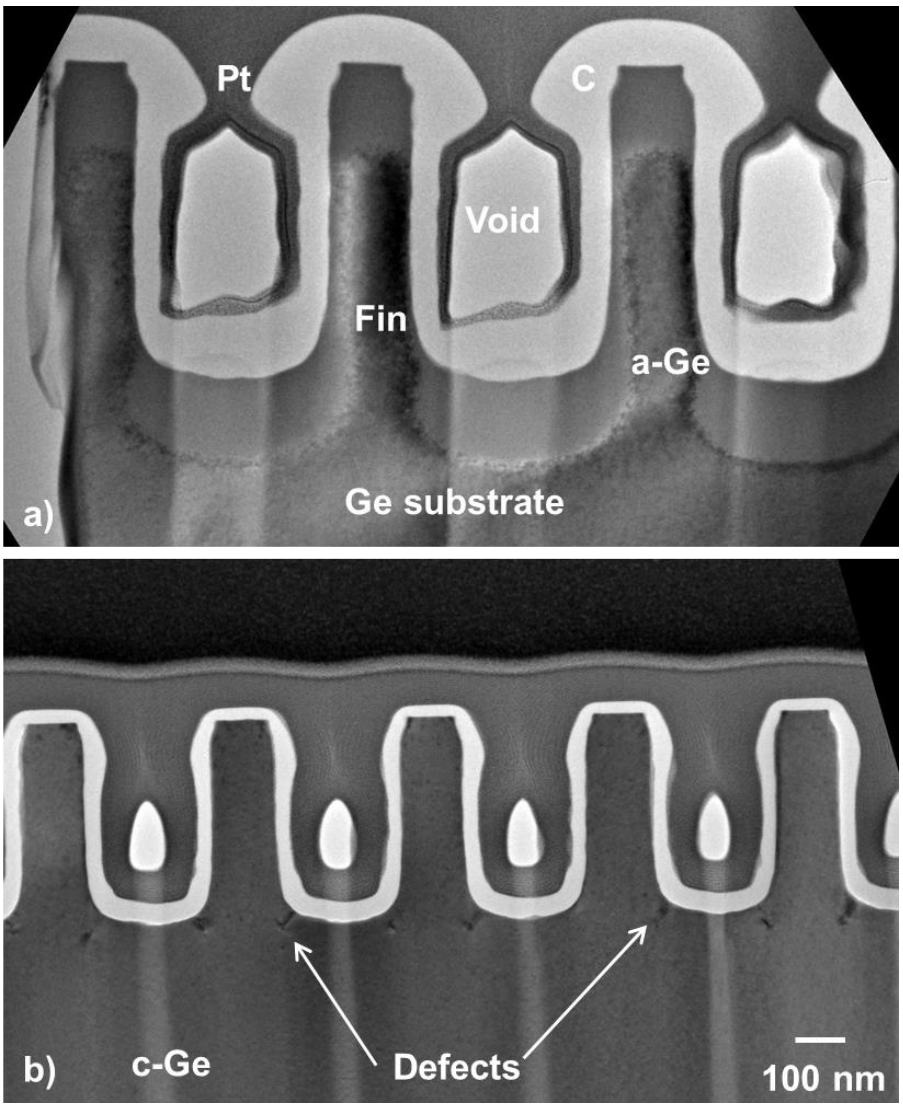


Figure 4.24: XTEM image of Ge fins, a) partially amorphized after implant. b) Although SPE is complete, defects and twin boundaries are generated.

Figure 4.25 is a combination of fins before and after furnace anneal in higher resolution. The stacking faults at the foot of the fins are generated by the intersection of two recrystallization fronts. Further defects are observed in the top 120 nm of the fin that was amorphized. Twin boundaries originating from the sidewalls appear in the top corners of the fin (see Figure 4.25 b) for zoomed in image). Small localized defects are also visible, which are shown in the figure.

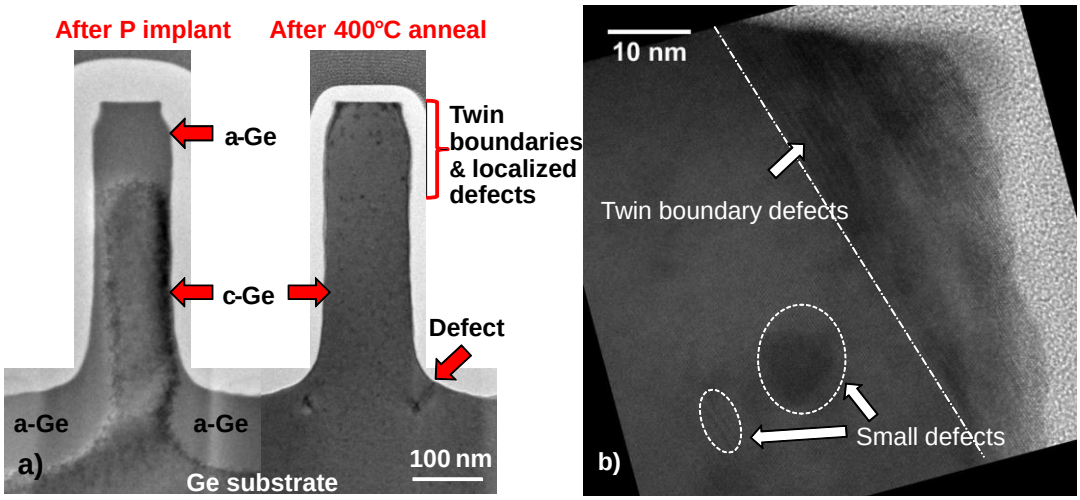


Figure 4.25: a) XTEM image of Ge fin structures showing a fin before and after anneal, with twin boundaries and localized defects on the top and defects at the bottom, b) Cross-section TEM image of fin, showing complete regrowth, with twin boundaries in {111} direction, and defects in the crystal structure.

SPE in planar structures has been studied for Si substrates [191, 192], showing that the growth direction is parallel to the substrate surface with the underneath crystal region being the seed for the regrowth process. On the other hand in 3D structures regrowth proceeds vertically from bottom to the top as well as along the edges of the structure. According to the atomistic model presented by Drosd and Washburn on the physics of recrystallization in Si for each Si atom contributing to the growth process two undistorted bonds with the crystal lattice are required with the angles and lengths as in the crystalline silicon [193]. In the proximity of the fin surface the crystal lattice is interrupted and SPER is retarded due to lack of undistorted bonds [166]. Pelaz *et al*. analyzed damage accumulation and the kinetics of the crystalline to amorphous transition in Si. Their Molecular Dynamic simulations show that IV pairs located close to the surface are more stable than

those in the bulk substrate. So the suppression of I-V recombination near the interfaces, and also the slow regrowth in the {111} direction, causes the formation of twin boundaries and polycrystals in thin-body devices [92] . SPE studies in Ge by Darby *et al*. [194] showed strong dependence of SPE on substrate orientation in Ge with the velocity of [001] direction being 16 times greater than [111] direction.

Narrow fins with 20 to 25 nm width and 400 nm height were also analyzed after undergoing the same implant, and are shown in Figure 4.26.

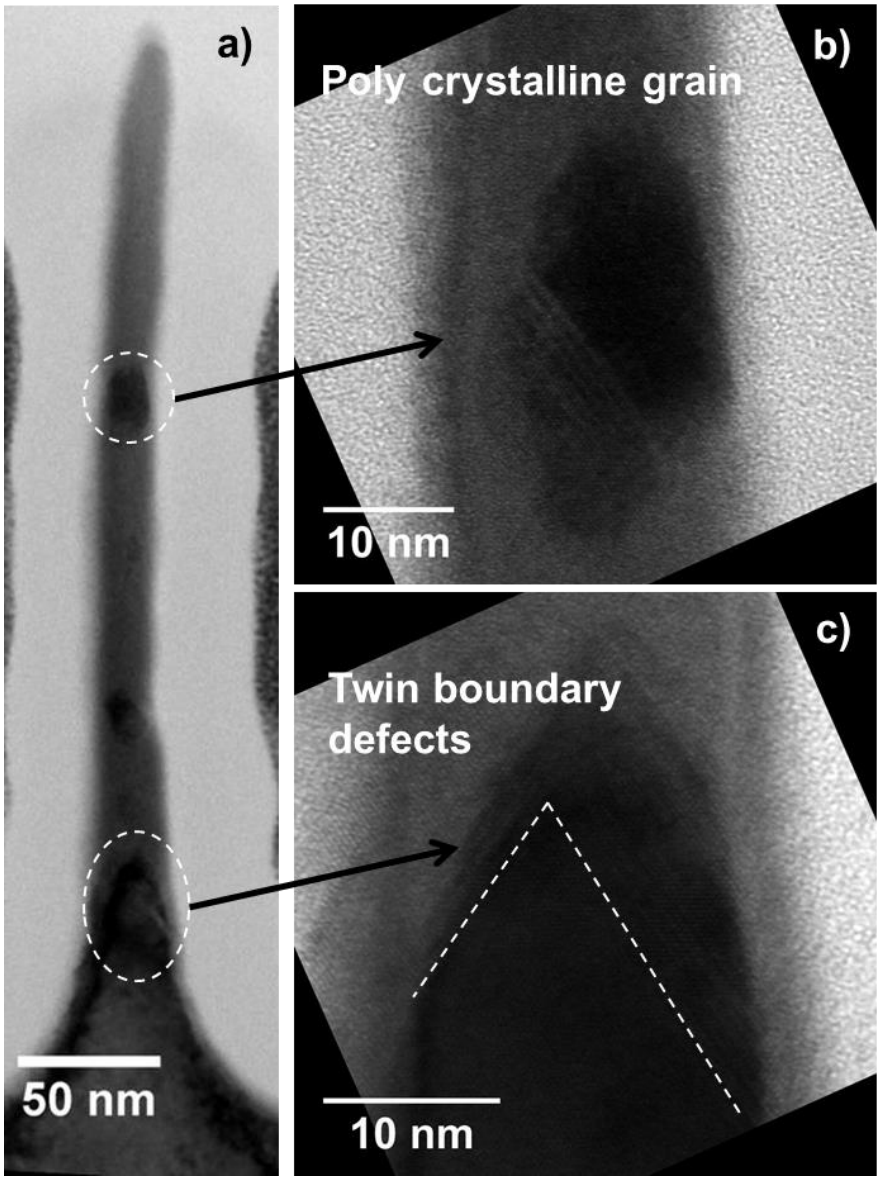


Figure 4.26: a) Narrow fin after 400 °C 3 min anneal. c) Regrowth is incomplete, and b) RNG has occurred.

Unlike the wide ones, SPE was deteriorated in narrow fins due to appearance of the twin boundaries. A clear arrow-head shaped recrystallization front is observed at the

foot of the fin. As is shown in the Figure 4.26 b) RNG occurred and poly-crystalline grains of Ge were also formed. In Figure 4.26 c) twin boundaries are seen. This is similar to the situation in silicon, and is of concern for future Ge FinFET and MugFET applications.

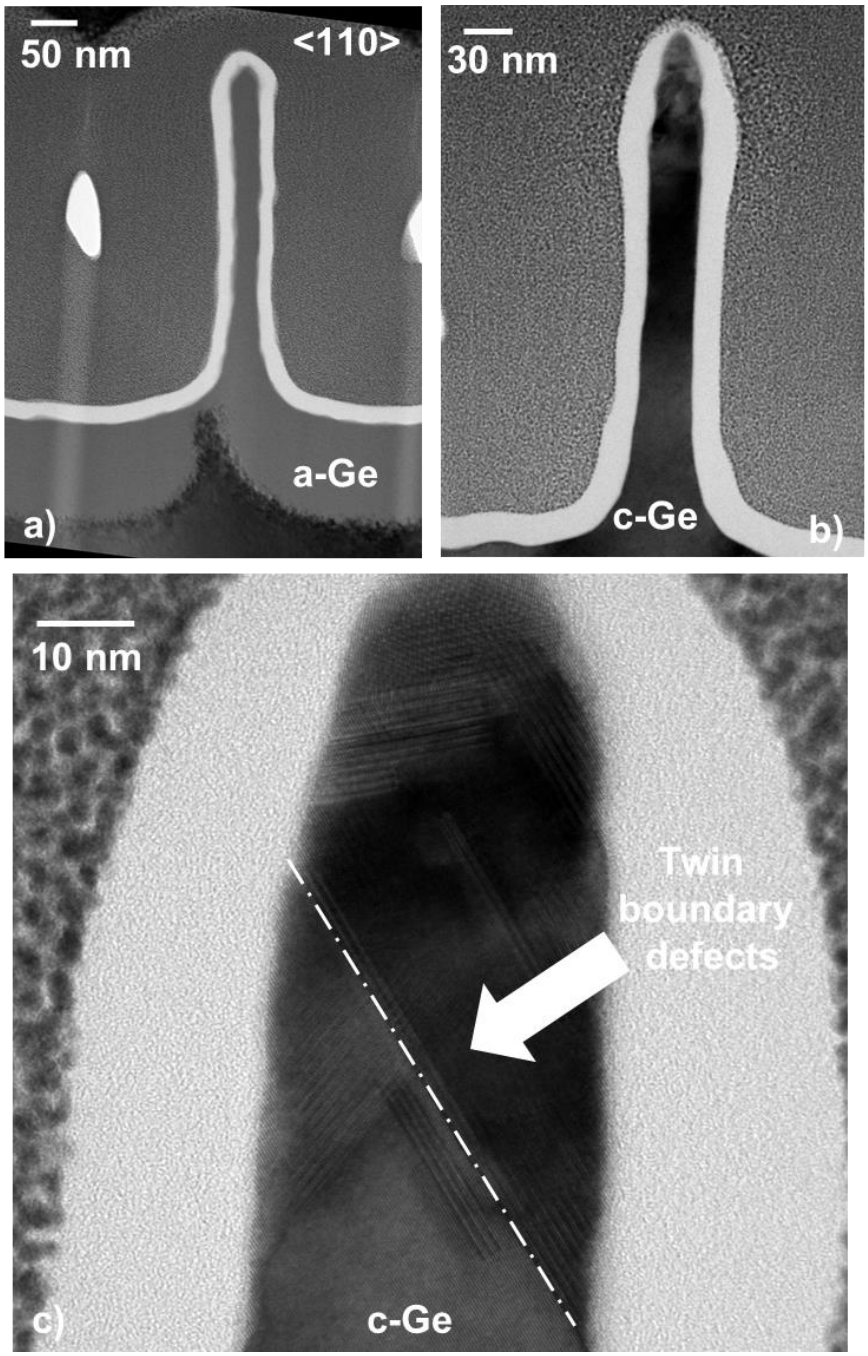


Figure 4.27: a) TEM image of 30 nm size fins after implantation that has amorphized the whole structure, b) a zoomed in image of the fin after RTA tratment, and c) a zoomed in view of the top portion of the structure fin showing the formation of {111} defects

Figure 4.27 shows a 30 nm [110] fin structure which was a) completely amorphized and b) recrystallized after ion implantation and the subsequent annealing process at 600 °C for 1 sec. In this case the fin is fully crystalline with {111} defects only located on top portion of the structure (see Figure 4.27 c)). In some of the structures it was observed that twin boundary defects have detached from side walls. It can be speculated that these defects start to cure from side walls and proceed upwards [195].

Like in Si, SPE appears to be a questionable approach to realize Ge thin body structures due to formation or poly crystalline grains resulting in incomplete or poor recrystallization at low thermal budgets (400 °C). Higher thermal budgets, (600 °C), can entirely crystallize the fins but electrical performance of such devices can be affected due the presence of twin boundary defects on the top of the structure. Therefore, it is essential to develop non-damaging doping techniques in order to prevent high parasitic resistance counteracting the high mobility benefit of Ge material.

4.4 Non-destructive doping of Ge

To date Ge FinFETs have relied on mono-directional ion-implantation for highly doped regions, which is not the perfect approach to achieve a conformal doping [164], that requires the target structure being uniformly coated with a dopant-enriched layer leading to evenly distribution of impurities through a thermal treatment.

Gas-phase and solid-source doping technologies have been around for many years, but there have been recent developments in molecular monolayer doping (MLD) of Si [96] which would be compatible with highly scaled nanowires and fins with aggressively scaled pitches. MLD doping has also been reported for InGaAs nMOSFETs by Kong *et al.* [196].

4.4.1 State-of-the- art work

Regarding in-diffusion of dopants into Ge from a surface, Takenaka *et al.* used a Metalorganic Vapor Phase Epitaxy (MOVPE) system to in-diffuse As into Ge at

500-700 °C [98], and reported maximum active concentrations of 10^{19} cm^{-3}, with the profiles 0.5-1.5 µm deep due to 60 min anneals. The same group demonstrated diode performance that beat their ion implant baseline, correlated with the reduction in crystal defects from the MOVPE approach [125]. Maeda *et al.* succeeded to in-diffuse Sb into Ge at 700 °C using a Sb-doped silicate glass, and reported a 4 µm deep doping profile with maximum chemical concentrations of 5×10^{18} cm^{-3} as well as high I_{ON}/I_{OFF} ratio ~ 1.5×10^{5} from their diodes [197]. Jamil *et al.* performed P in-diffusion from spin-on-dopant source into Ge at 650-750 °C [123]. However the reported Ge FinFET devices are limited to p-type ion implanted structures.

In this section we report application of non-destructive gas phase doping technique to introduce n-type As, and P dopants in fin/nanowire test structures. Nanowire resistors are excellent tools to evaluate and test the effectiveness of a doping technique based on the access resistance characterization.

4.4.2 Experimental procedure

The first part of this work was carried out on unpatterned (100) Ge substrates, with p-type doping concentration in the range of 5-9×10^{16} cm^{-3} according to the supplier information. For the second part of this study undoped (100) germanium-on-insulator (GeOI) substrates were used, with a Ge thickness of 50 nm, for nanowire processing. Samples were cleaned by performing a 10 minute dip in hydrochloric acid (37%) : deionised water in the ratio 27:73, followed by immediately drying with N_2 and loading onto a graphite susceptor within an AIX200-AIX200/4 MOVPE horizontal reactor which, using double purification of the highest commercially available purity precursors, has achieved near Molecular Beam Epitaxy quality III-V material by MOVPE [198]. The samples were heated under a flow of N_2 carrier gas at 80 mbar to 250 °C at which point purified AsH_3 (or PH_3) was also introduced at a flow rate of 50 sccm. The sample temperature was then ramped to the process temperature over 10 minutes, while the flow rate of AsH_3 (or PH_3) into the reactor was linearly increased to 250 sccm, and held at the process temperature for another 20 minutes under a flow of 250 sccm AsH_3 (or PH_3) and N_2 carrier gas. The heating was then switched off to cool down the sample under 100 sccm AsH_3 (or PH_3). The AsH_3 and PH_3 were switched out at 450 and 250 °C

respectively and the sample allowed cooling under N_2 to below 60 °C before it was unloaded from the reactor.

Noted that the reported process temperature is that of a control thermocouple within the body of the graphite susceptor and the actual temperature of the surface is lower. Previous studies using emissivity corrected pyrometry have shown that the sample surface temperature is approximately 590°C at a thermocouple temperature of 650 and 620 °C at a thermocouple temperature of 700 °C.

In order to fabricate Ge nanowires the GeOI substrates were patterned using the Raith e-Line Plus electron beam lithography (EBL) system and high resolution EBL resist known as hydrogen silsesquioxane (HSQ). After EBL exposure, the HSQ resist was developed using an aqueous developer followed by deionised (DI) water rinse [199].

The EBL exposure was a two-step process; the first lithography step was used to expose only the high resolution fin structures and the second step the contact pads for the four probes were exposed. To attain a highly focused beam for the first step, 10 kV beam voltage and 100 µm write-field was chosen. To avoid the large exposure time, the low resolution contact pads were written with 1 kV beam voltage and 400 µm write-field. Figure 4.28 shows a) the process flow and b) a representative SEM image of a 20 nm width Ge nanowire. The patterned nanowires (fins) were 10 µm long with namely 1µm, 300, 100, 80, 70, 60, 50, 40, 30, and 20 nm widths.

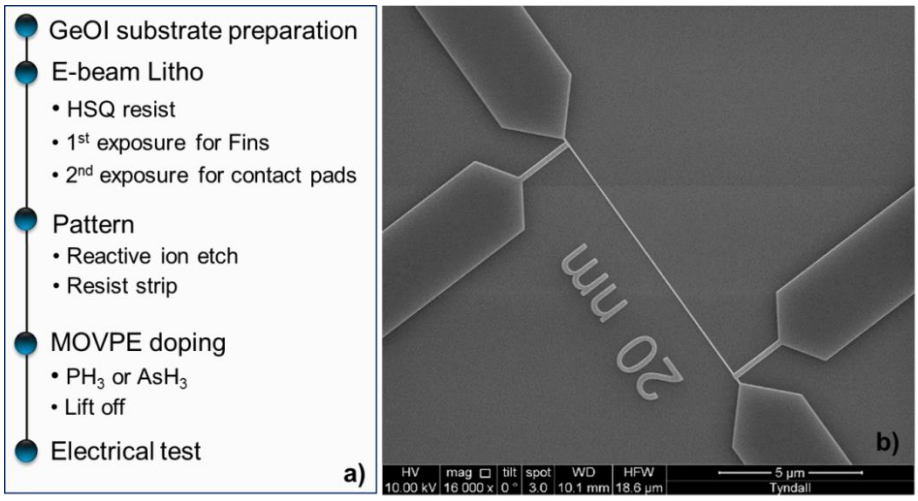


Figure 4.28: a) process flow of the experiment, b) representative SEM image of a 20 nm patterned nanowire.

An exclusive range of characterizations were performed on the samples including AFM for surface inspection, SEM imaging for top-down view of the structures, and cross sectional TEM. SIMS and ECV profiling were done to obtain the chemical and active carrier concentration respectively. XPS was carried out with a VG Scientific Escalab MKII system using Mg X-rays at 1253 eV. Survey scans were performed using a pass energy of 200 eV and core level scans at a pass energy of 20 eV. 4 point probe electrical measurements were done to extract nanowire resistance.

4.4.3 Results of the material characterization

The ECV carrier concentration profile from the P and As doped unpatterned samples is depicted in Figure 4.29. It is well established by ion implantation studies that As diffuses faster than P [61, 115] as we observe in the ECV profiles. As dopants diffused to a depth of approximately 550, and 400 nm during the 700 and 650 °C processes respectively. The flat-topped nature of the As profiles is due to concentration enhanced diffusion [200]. P and As are known to suffer from significant concentration-enhanced diffusion in Ge through the formation of dopant-Vacancy complexes, at concentrations in excess of 2–5×10^{19} cm^{-3} [201].

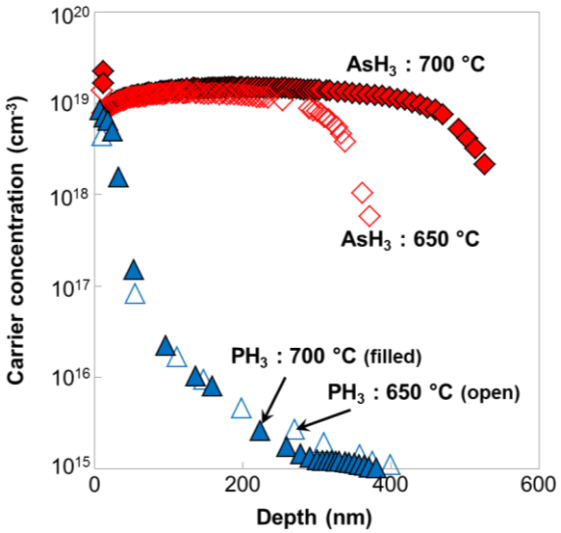


Figure 4.29: Active carrier concentration versus depth extracted by ECV profiling for As and P doped samples. The As-based process resulted in greater dopant integrated dose than the P-based process

In all the samples the peak active carrier profiles are approximately 10^{19} cm^{-3}. Integrating the profiles to extract total active dose yield 3.70×10^{14} and 6.41×10^{14}

cm^{-2} for As in the 650 and 700 °C processes respectively, and total active P doses of 4.91×10^{12} and 1.81×10^{13} cm^{-2} for the 650 and 700 °C processes respectively.

Figure 4.30 shows the SIMS depth profile of As samples with maximum chemical concentrations of approximately 5×10^{19} cm^{-3}, excluding the peak artefact at the surfaces. The profiles match with the ECV data in terms of junction depth. However, integrated dose of the SIMS profile shows higher amount of chemical As than the electrically active As in the ECV profile indicating that not all the dopants are activated during the doping process. Integrating the profiles to extract the total chemical dose yield 6.77×10^{14} and 1.19×10^{15} cm^{-2} for the 650 and 700 °C processes respectively, which are approximately double the electrically active As doses.

It is worth mentioning that SIMS analysis was also performed on the P-doped samples which showed a signal close to the surface, much like that of the ECV profiles, however it did not seem to be reliable data due to the apparent similarity to a SIMS surface artefact.

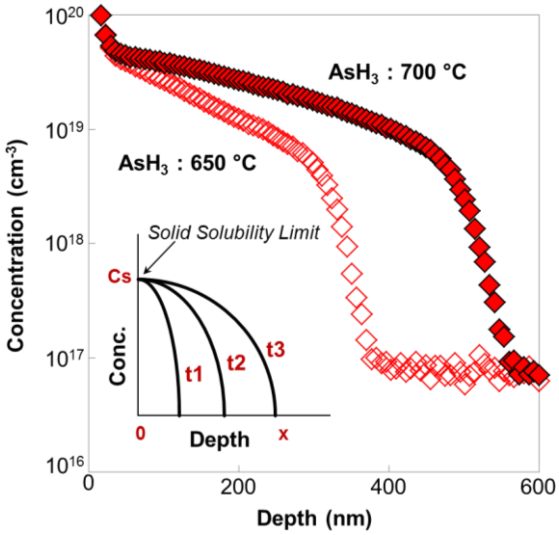


Figure 4.30: Chemical concentration vs depth profiles extracted by SIMS analysis for the unpatterned Ge samples processed by an AsH_3-based method. The higher temperature of processing is more effective at incorporating As, however there is greater diffusion. The inset shows a schematic representation of the time evolution of impurity incorporation in a semiconductor using a chemical predeposition process. The peak concentration is capped by the solid solubility limit at the processing temperature. The profiles get deeper with increasing time.

In this experiment the dopants are introduced from a vapor source which is assumed to provide constant value of surface concentration, and is called chemical predeposition [175]. Here we briefly discuss the underlying theory of the dopants driven-in from the surface.

For the chemical predeposition process the impurity concentration (C) profile is calculated from

$$C_{(x,t)} = C_s erfc\left(\frac{x}{2\sqrt{Dt}}\right) \quad (4.3)$$

where x is the distance from the surface, t is time, C_s is the impurity surface concentration, and D is the impurity diffusivity. The time evolution of the doping profile (for a constant processing temperature) is shown schematically in the inset of Figure 4.30. D is assumed to be constant and the depth of the profile is only dependent on time. The surface concentration remains fixed, since it is limited by solid solubility limit at that processing temperature. Therefore the total quantity of dopants, which is defined as dose, Q, can be described as

$$Q_{(t)} = \int_{\infty} C_{(x,t)} dx \quad (4.4)$$

using these equations the total incorporated dose can be simplified to

$$Q_{(t)} = \frac{2}{\sqrt{\pi}} C_s \sqrt{Dt} \quad (4.5)$$

From ECV and SIMS analysis one can extract the total incorporated dose, Q, as well as C_s the dopant concentration on the surface, so D can be easily calculated for a fixed known processing time (see Table 4.3).

Usually, constant diffusion happens when the dopant concentration is below the intrinsic carrier concentration (n_i) at a processing temperature. Below n_i the diffusion mechanism is dominated by intrinsic diffusivity whereas above ni extrinsic diffusivity dominates the movement fashion of the dopants in semiconductor [59].

Using standards values for concentration-dependent electron mobility provided by Fistul *et al.* [202] sheet resistance was calculated from

$$R_{sheet} = \int_{0}^{\infty} \frac{1}{q \cdot \mu \cdot N \cdot dx} \quad (4.6)$$

where q is electron charge, μ is electron mobility, N stands for dopant concentration and dx represents the junction depth. The extracted values based on the ECV data show much higher sheet resistance for P as compared to As samples, which can be associated to the relatively deep carrier concentration profiles in As samples. The extracted active dose, diffusivity and sheet resistance from ECV and SIMS profiles are summarized in Table 4.3.

In order to confirm the non-destructive effect of the doping process surface topography was carried out on all the samples and showed 0.1-0.2 nm roughness which is close to the roughness of the as-received wafers.

Table 4.3: Extracted data for the unpatterned samples, showing total active dose, R_{sheet}, and diffusivity all extracted from the ECV profiles in Figure 4.29, as well as total chemical dose and diffusivity extracted from the SIMS profiles in Figure 4.30.

Sample	Active dose (at/cm^2)	Diffusivity (cm^2/s)	SIMS dose (at/cm^2)	Diffusivity (cm^2/s)	R_{sheet} (Ω/sq)
P 650 °C	4.91×10^{12}	6.29×10^{-16}	n/a	n/a	3323
P 700 °C	1.81×10^{13}	8.55×10^{-15}	n/a	n/a	937
As 650 °C	3.70×10^{14}	8.93×10^{-13}	6.77×10^{14}	8.31×10^{-14}	55.8
As 700 °C	6.41×10^{14}	2.68×10^{-12}	1.19×10^{15}	2.57×10^{-13}	34.5

In Figure 4.31 we present the extracted diffusivity versus 1000/T (in Kelvin) for the doping conditions used in this experiment, and compare them to the intrinsic diffusivity extracted by Brotzmann *et al.* [59].

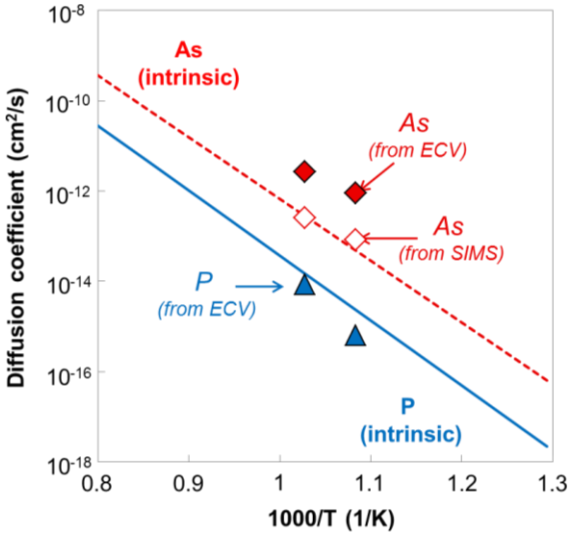


Figure 4.31: Diffusion coefficients vs 1000/T, where T is in Kelvin. The solid trend-line shows the intrinsic P diffusivity, and the dotted trend-line shows the intrinsic As diffusivity. The experimental data from our work is shown as the symbols. Both ECV and SIMS data were used to extract diffusion coefficients here.

The P diffusion coefficients extracted from the ECV analysis lie on the intrinsic diffusivity trend line. The extracted diffusivity values from the As SIMS profiles also show an intrinsic diffusivity for the dopants; however overlaying the extracted diffusivity data from the As ECV profiles with the corresponding trend line show that these dopants diffuse in an extrinsic fashion. It seems reasonable considering the fact that at the processing temperature of our experiment (650-700 °C) n_i is in the range of 3-4×10^{18} cm^{-3} [59], which is below the As concentrations extracted from the ECV profiles (see Figure 4.29).

Figure 4.32 depicts an XPS survey spectra of a Ge sample cleaned by *in-situ* ion etching, a Ge wafer post MOVPE reaction (inset is a core level spectrum in the As 2p region post MOVPE reaction). The survey spectrum of Ge after MOVPE shows large O (532 eV) and C (285 eV) peaks which are due to the native oxide and ambient contamination respectively. These levels are similar to those that one would find in an as-received Ge wafer that has not undergone a cleaning step. Core level examination of the As 2p core region of the spectrum indicates the presence of a small As peak (~0.6 at %). The presence of As on the surface of the wafer after the MOVPE reaction is indicating that there is a constant renewed supply of As during the reaction that stops diffusing in as the temperature of the reactor decreases. It was not possible to positively identify the presence of P due to it being masked by larger Ge peaks that occur at similar binding energies.

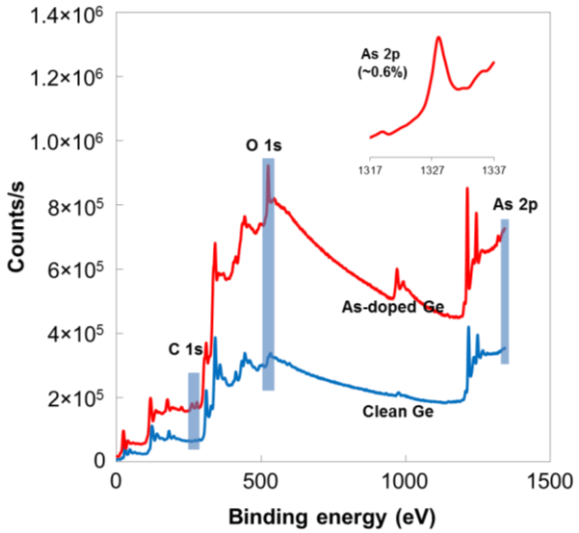


Figure 4.32: An XPS survey spectra of Ge cleaned by in-situ ion etching, and a Ge wafer post MOVPE doping using AsH_3. The inset shows a core level spectrum in the As 2p region post MOVPE reaction.

4.4.4 Results of the electrical characterization

As mentioned earlier the nanowires were exposed to PH_3 at 650 or 700 °C, or to AsH_3 at 650 °C by MOVPE for unpatterned samples. Based on the unpatterned sample analysis of the AsH_3 at 700 °C, this process was considered too coarse for the small nanowires, and was not evaluated in terms of electrical properties.

Figure 4.33 shows representative 4 point probe I-V measurements after PH_3 process at 700 °C. As is shown in the figure the nanowires behave like a resistor with expected linear I-V characteristics that scale for the reduced fin widths.

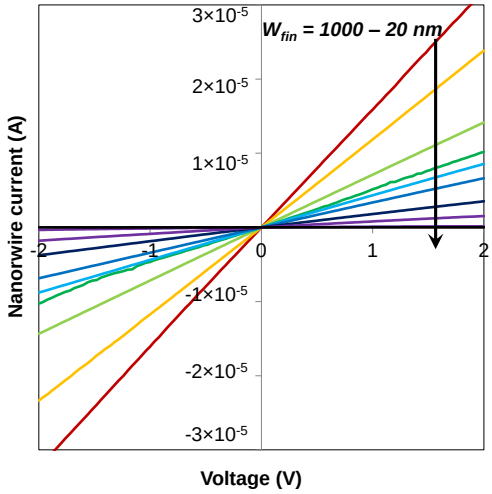


Figure 4.33: Current-voltage characteristics of the Ge nanowires. The current obeys Ohms law, is symmetrical around the origin, and scales with reduced fin width.

In order to validate the effectiveness of the doping process I-V measurements were carried out on one nanowire sample before it was doped. Further analysis of the I-V characteristics was performed in two ways depending on the assumption of where the current flows in the nanowire cross-section. One possibility is that current flows along the edges of the nanowire where the doping concentration is at the highest value on the surface like the P case in this experiment (see Figure 4.29). In this case the electrical width of the device and the fin resistance are calculated from

$$W_{Electrical} = 2H_{fin} + W_{fin} \qquad (4.7)$$

and

$$R = \frac{V}{\left(\frac{I}{W_{Electrical}}\right)} \tag{4. 8}$$

where H_{fin} is the height of the fin and is equivalent to the height of the Ge layer on the GeOI wafer. W_{fin} is to the fin width and varies from 20 nm to 1 um.

In Figure 4.34 the access resistance is plotted versus fin width for all the doped nanowires as well as the data taken from the undoped sample. As is seen in the figure there is a comparable difference (4-5 orders of magnitude) between the resistance of the undoped and doped nanowires, which justifies the efficiency of the MOVPE-based doping technique. Moreover, as the nanowire width is scaled the resistance rises, as expected and reported for Si nanowires and FinFETs [167]. However it seems surprising that the P and As based processes give similar results in the wide nanowires despite the large differences observed in the unpatterned samples. From dopants perspectives it appears that 650 °C PH_3-based process is not high enough as increasing the temperature to 700 °C significantly lowers the resistance. Also the resistance of the 700 °C PH_3-based process matches well with the 650 °C AsH_3-based process except that the resistance increases dramatically for As nanowires at 40 nm width and below where as the PH_3 nanowires can be scaled beyond this point without a sharp increase in the resistance, which makes this method favourable for making scaled features.

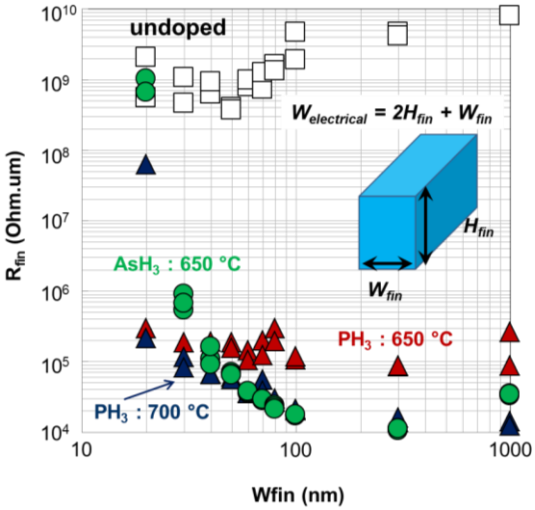


Figure 4.34: Extracted R_{fin} vs W_{fin} for Ge nanowires subjected to PH_3 at 650 and 700 °C, and AsH_3 at 650 °C. W_{fin} on the x-axis refers to the drawn width on the mask.

Another possibility for electrical parameters extraction is considering the current flowing uniformly through the nanowire cross-section analogous to the metal tracks. In this case the applicable equation is as follows

$$R = \rho \frac{L}{A} \tag{4. 9}$$

where ρ is the material resistivity, A is the cross-sectional area, and L is the length of the track, and from these terms we can calculate

$$R_{sheet} = \frac{\rho}{t} \tag{4. 10}$$

where R_{sheet} is the sheet resistance and t is the thickness of the layer.

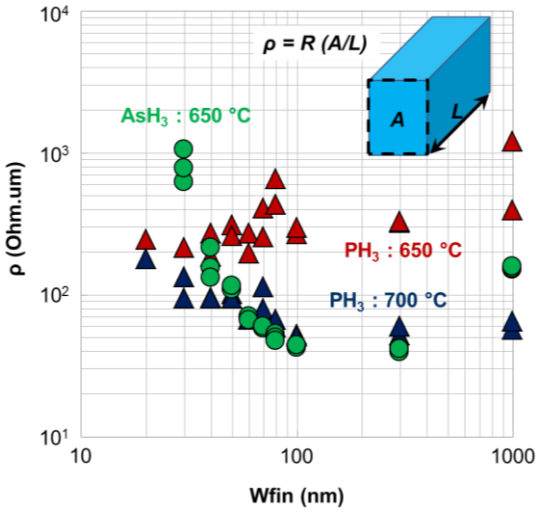


Figure 4.35: ρ vs W_{fin} for Ge nanowires doped at 650 or 700 °C using PH_3, or doped at 650 °C using AsH_3. W_{fin} on the x-axis refers to the drawn width on the mask.

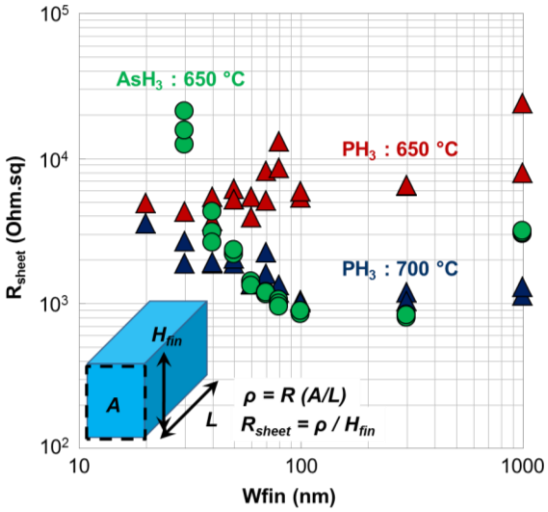


Figure 4.36: R_{sheet} vs W_{fin} for Ge nanowires doped at 650 or 700 °C using PH_3, or doped at 650 °C using AsH_3. W_{fin} on the x-axis refers to the drawn width on the mask.

Figure 4.35 and Figure 4.36 show extracted resistivity and sheet resistance based on the above equations with similar trends observed in the previous analysis in Figure 4.34. Once again 700 °C shows better performance for the P doping process, and the two dopant species produce similar results for wide devices, when the P-based process seems to be a better choice for scaled features.

This is a significant result considering the ECV and SIMS data back in Figure 4.29 and Figure 4.30. Regarding the ECV and SIMS results from unpatterned samples, one might think that the AsH_3 based process would be a better choice, due to the greater dose incorporation. However As may also exhibit greater likelihood of dopant clustering, evident is the differences between the SIMS and ECV data, and may even trap at surfaces more readily, a feature that is reported in As-doped Si [203].

At this point we ought to consider which of the two parameter extraction approaches is more suitable for scaled nanowires and FinFETs. As we scale down to very small dimensions (sub-30 nm) the doping profiles from all sides will tend to overlap, and we are likely to have a uniformly doped structure in cross-section. There comes a point where the device is so small that the volume is essentially uniformly doped and the current flow is throughout the entire cross section of the doped region. Thus in that case it is more appropriate to use the second model for electrical parameter extraction above.

If we assume the fins are uniformly doped then, using the published values for carrier concentration-dependent mobility [115], μ the resistance of the nanowire can be theoretically calculated according to the following equations.

$$\begin{aligned} R &= \rho \frac{L}{A} \\ &= R_{sheet} \cdot t \cdot \frac{L}{A} \\ &= \frac{1}{q \cdot \mu \cdot N \cdot t} \cdot t \cdot \frac{L}{A} \\ &= \frac{L}{q \cdot \mu \cdot N \cdot A} \end{aligned} \qquad (4.\ 11)$$

From these values theoretical expectations for R are calculated and plotted as isolines of constant active concentration alongside the experimental data (simply R=V/I) in Figure 4.37.

From this plot we can see that the 700 °C PH_3 process and the AsH_3 process touch the 3×10^{18} cm^{-3} isoline, while the 650 °C PH_3 process can only touch the 3×10^{17} cm^{-3} isoline. In all cases the active doping levels appear to degrade as the nanowires are scaled. This effect is more pronounced in As-doped structures. It is known that As traps at Si surfaces [203]. This behavior is characterized in Ge using the XPS analysis shown in Figure 4.32. Therefore it appears that surfaces are bad for resistance as the W_{fin} is scaled. P has probably a weaker tendency to trap at the surface or be influenced by the interface. Furthermore, one might think that the overlapping doping profiles originating from the top, left, and right surfaces would lead to greater active concentration and lower resistance. In this case we are probably limited by solid solubility limits of P and As in Ge.

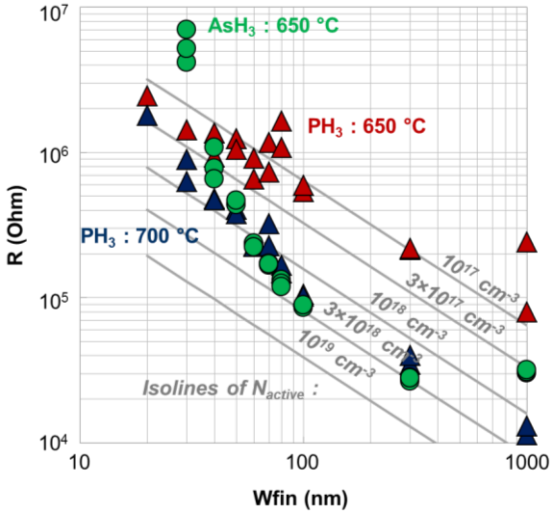


Figure 4.37: R vs W_{fin} for Ge nanowires doped at 650 or 700 °C using PH_3, or doped at 650 °C using AsH_3. R is also calculated based on the assumptions for uniformly doped concentration levels, and carrier concentration dependent mobilities. These calculations are plotted in the form of isoline of constant carrier concentrations, in grey.

As the final characterization step, XTEM analysis of the As-doped nanowires was undertaken to determine if crystal defects had been introduced by this process. Figure 4.38 is a representative TEM image of the samples, in which no visible crystal defects are observed, confirming the non-destructive nature of the process.

Furthermore as the sample temperatures are 650-700 °C during the dopant in-diffusion one would expect a great deal of dynamic annealing, and thus no crystal

damage build-up that could cause the formation of defects. This is in contrast to ion implanted thin-body structures where crystal damage, {111} defects, and poly-crystalline transformation can be a problem with decreasing W_{fin} [166, 204].

Ion implantation is the standard approach in industry for doping semiconductors as it can generate a single ion species with a single energy in a highly controlled fashion. The problems associated with this technique are: a) the induced crystal damage due to the collision of the energetic ions with the target material and b) extremely directional nature of the process resulting in non-conformal doping in non-planar structures. Plasma doping enables formation of more conformal doping profiles than ion implantation but it can cause damage to the substrate as the ions strike the target. In addition there is a chance of implanting multiple species with multiple energies in one doping process which can be troublesome if highly controlled doping processes are required [90, 205]. Conformal doping techniques such as plasma doping may evolve as the ultimate choice for MugFETs and nanowire FETs [206, 207]. The proposed MOVPE approach can be considered as an alternative methodology based on surface in-diffusion, providing non-destructive and conformal doping which is crucial for future non-planar devices.

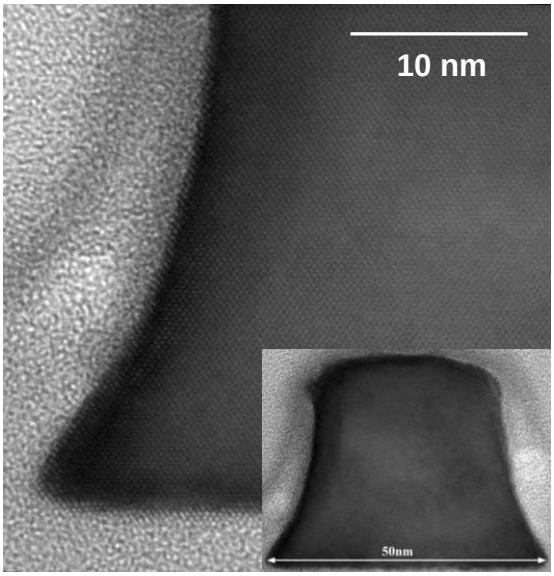


Figure 4.38: Representative XTEM images of a 50 nm wide Ge nanowire structure post MOVPE-doping and post electrical characterisation. No visible crystal defects appear to be present. The drawn width on the mask layout is 40 nm, with a resulting width at half-height of 37 nm

4.5 Conclusion

In this chapter, ion implantation in this body structures was studied using the SRIM simulation software. The amount of ions retained in the structure is determined by the amount of backscattered and transmitted ions which are influenced by the species and energy of the incident ion as well as the implant angle. Furthermore heavy ion implantation at oblique angles would enhance surface sputtering leading to undulating nanowire facets

Ge fins with high aspect ratios were reported on which amorphisation and recrystallization phenomena were studied. In wide fins recrystallization was complete after a 400 °C 3 min anneal resulting in twin boundary defects and stacking faults, whereas in narrow structures due to surface proximity regrowth was incomplete and poly-crystalline grains were formed. The structures were crystalline and the most defects were annihilated after annealing at 600 °C 1 sec.

Moreover we demonstrated a non-destructive dopant in-diffusion process by means of PH_3 and AsH_3 in a MOVPE system above heated substrates. We managed to avoid crystal damage and reduce the access resistance in doped nanowires. Meanwhile the usual degradation of resistance in scaled fin widths was effectively suppressed using a PH_3-based process.

Chapter 5

Summary and future work

Considering its unique properties and high mobility, Ge can be considered a potential replacement or augment for Si. However key bottlenecks like contact resistance, shallow junction formation, dopant diffusion control, and leakage current need to be resolved. This thesis discussed a number of challenging issues in realization of Ge based devices.

5.1 Summary

Formation of low resistive ohmic contacts on n-type Ge is a difficult task. Ohmic contacts on Ge can be formed by different techniques and alloys. NiGe seems to be one of the best candidates due to its low temperature formation, stability, and low resistivity. In this work the effect of impurity concentration, dopant types as well as the annealing techniques on NiGe contacts were studied.

Using a 1×10^{15} cm^{-2} 15 keV phosphorus implant and RTA technique, a low ρ_c of 3.46×10^{-6} $\Omega.cm^2$ was obtained after 250 °C NiGe formation anneal. In addition it was shown that higher implant dose leads to lower ρ_c. It was observed that P yields lower R_{sh} and ρ_c than As. The quality of germanide contacts formed by LTA was investigated and compared systematically with RTA.

LTA resulted in smoother layers of germanide, mainly NiGe and $NiGe_2$ and enhanced the quality of the contact dramatically due to the incredibly sharp germanide-substrate interface without any detectable interfacial region or transition zone. NiGe was formed through a liquid-solid reaction between Ni with the underlying melted Ge layer. The best contact resistivity obtained in this study was 2.84×10^{-7} $\Omega.cm^2$. The contacts made with both annealing techniques showed questionable thermal stability indicating that they have to be modified in a way so that they are stable in subsequent annealing steps during device fabrication.

The atomically flat germanide layers made by LTA with their significantly low ρ_c justified the efficiency of this technique for contact formation. The next step was to evaluate the impact of LTA on implant defects and the junction leakage current. It has already been confirmed by different research studies in Si that LTA activation anneals can boost the level of active dopants and maintain a shallow doping profile.

Therefore a new experiment was carried out, this time using LTA to activate the n-type dopants and cure the crystal damage after ion implantation, which resulted in high carrier concentration (> $10^{20}cm^{-3}$). Material and electrical characteristics of n+/p junctions in Ge formed by RTA and LTA process techniques were compared. From the ECV and Hall Effect data it was concluded that almost 100 % of the retained dose was activated.

Furthermore high I_{ON}/I_{OFF} ratio ~ 10^7 and ~ 10^5 was obtained from RTA and LTA diode samples respectively. The extracted activation energy from RTA diode samples appeared to be greater than 0.67 eV, the indirect bandgap of germanium.

Studies on F which is the most common non-dopant co-implant for point defect engineering in Si proposed that this element is unlikely to be as useful in Ge. In fact it has only a minor effect on P and As diffusion, due to extreme F outgassing. F concentrations in the high 10^{20} cm^{-3} range might be required to create stable F_nV_m clusters, however high implant doses into Ge often risk irreversible substrate damage. Thus, if attempted, care must be taken in that experimental space.

Studies on the correlation between dopant loss and Ge substrate desorption showed that Ge desorption alone does not explain the dopant loss mechanism.

SRIM simulations were carried out to study the effects of ion implantation in 10 nm width thin body structures. It was observed that the retained dose in a nanowire is limited by transmission of ions at normal incident angles whereas is limited by backscattering at oblique implant angles. Surface sputtering could be significant if heavy ions and bigger implant angles are used for implantation.

Substrate desorption, amorphisation and SPE was studied on Ge fins with high aspect ratio. In wide fins recrystallization resulted in twin boundary defects and stacking faults, whereas in narrow structures due to surface proximity regrowth was incomplete and random nucleation growth was observed much like Si. However twin boundary defects appeared to cure more readily in Ge.

Moreover a non-destructive dopant in-diffusion process was demonstrated to dope Ge nanowires where the substrates were subjected to PH_3 and AsH_3 in a MOVPE system. In this technique the crystal damage was avoided thus the access resistance was reduced. Also the usual degradation of resistance in scaled fin widths was effectively suppressed using a PH_3-based process.

5.2 Future work

- Future studies to improve the source and drain contact resistance can be done by NiGe formation without a dopant activation anneal. Implantation through silicide (germanide) technique would be another alternative. Also cryogenic implants can be performed on n-type Ge in order to obtain high dopant activation and subsequently lower the contact resistance. Activation anneal by LTA could also enhance the level of active dopants and help to improve the contacts. Hot implant can also be applied to achieve high levels of dopant activation and suppress the defects. Non-destructive doping techniques such MLD, plasma doping, or MOVPE based doping followed by LTA for contact formation could also be investigated.
- The LTA process for making germanide contacts needs be optimized in order to obtain single crystal phase of NiGe. This could be done possibly by optimizing the deposited Ni thickness.
- Solutions to improve thermal stability of the contacts should be explored. Introducing a third element in germanidation process like Ta, Pt, and Ti could be helpful.
- LTA process optimizations are required for high I_{ON}/I_{OFF} ratios in n+/p junctions while highly activated dopants are maintained.
- Activation anneals done by LTA provide shallow doping profiles with highly activated dopants above the solid solubility limit. There is a good chance that dopants revert back to equilibrium level if subjected to further annealing steps. Therefore it is necessary to examine the thermal stability of such profiles in subsequent heating processes.

- More analysis is required to determine the nature of the mechanism involved in extraction of activation energy greater than 0.67 eV in RTA Ge diodes.
- Dopant loss phenomenon has to be studied in more depth before a proper solution can be proposed. With mass spectrometry this mechanism can be closely inspected.

5.3 Contributions and impact of the work

- Low resistance atomically flat NiGe contacts were formed using LTA technique.
- The effect of LTA on n+/p Ge junctions was studied and I_{ON}/I_{OFF} ratios where obtained. It was shown that there is a tradeoff between dopants activation level and leakage current. An I_{ON}/I_{OFF} ratio ~ 10^7 is achieved in Ge diodes.
- It was shown that F is not efficient for defect engineering in Ge at high temperature.
- It is suggested that substrate desorption is not the sole cause of dopant loss in Ge.
- A non-destructive in-diffusion doping technique was successfully applied to dope Ge nanowires changing resistance and current level by 5 orders of magnitude.

References

[1] W. F. Brinkman, D. E. Haggan, and W. W. Troutman, "A history of the invention of the transistor and where it will lead us," *Solid-State Circuits, IEEE Journal of,* vol. 32, pp. 1858-1865, 1997.

[2] R. G. Arns, "The other transistor: early history of the metal-oxide semiconductor field-effect transistor," *Engineering Science and Education Journal,* vol. 7, pp. 233-240, 1998.

[3] L. Colombo, J. J. Chambers, and H. Niimi, "Gate dielectric process technology for the sub-1 nm equivalent oxide thickness (EOT) Era," *Electrochemical Society Interface,* vol. 16, pp. 51-55, 2007.

[4] G. E. Moore, "Cramming More Components Onto Integrated Circuits," *Proceedings of the IEEE,* vol. 86, pp. 82-85, 1998.

[5] T. R. Halfhill, "The Mythology of Moore's Law: Why Such a Widely Misunderstood "Law" Is So Captivating to So Many," *Solid-State Circuits Society Newsletter, IEEE,* vol. 11, pp. 21-25, 2006.

[6] P. Gelsinger, "Moore's Law- The Genius Lives On," *Solid-State Circuits Society Newsletter, IEEE,* vol. 11, pp. 18-20, 2006.

[7] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *Solid-State Circuits, IEEE Journal of,* vol. 9, pp. 256-268, 1974.

[8] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, T. Yuan, and W. Hen-Sum Philip, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE,* vol. 89, pp. 259-288, 2001.

[9] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature,* vol. 479, pp. 310-316, 2011.

[10] K. L. Wang, K. Galatsis, R. Ostroumov, A. Khitun, Z. Zhao, and H. Song, "Nanoarchitectonics for Heterogeneous Integrated Nanosystems," *Proceedings of the IEEE,* vol. 96, pp. 212-229, 2008.

[11] C. L. S. E. Claeys. (2007). *Germanium-based technologies from materials to devices*. Available: http://site.ebrary.com/id/10172772

[12] E. J. Nowak, "Maintaining the benefits of CMOS scaling when scaling bogs down," *IBM Journal of Research and Development,* vol. 46, pp. 169-180, 2002.

[13] N. G. Tarr, D. J. Walkey, M. B. Rowlandson, S. B. Hewitt, and T. W. MacElwee, "Short-channel effects on MOSFET subthreshold swing," *Solid-State Electronics,* vol. 38, pp. 697-701, 1995.

[14] F. Assaderaghi, P. K. Kop, and H. Chenming, "Observation of velocity overshoot in silicon inversion layers," *Electron Device Letters, IEEE,* vol. 14, pp. 484-486, 1993.

[15] K. Seong-Dong, P. Cheol-Min, and J. C. S. Woo, "Advanced model and analysis of series resistance for CMOS scaling into nanometer regime. I.

Theoretical derivation," *Electron Devices, IEEE Transactions on,* vol. 49, pp. 457-466, 2002.
[16] K. Seong-Dong, P. Cheol-Min, and J. C. S. Woo, "Advanced model and analysis of series resistance for CMOS scaling into nanometer regime. II. Quantitative analysis," *Electron Devices, IEEE Transactions on,* vol. 49, pp. 467-472, 2002.
[17] R. Duffy, M. Shayesteh, and R. Yu, "Processing of germanium for integrated circuits," *Turk. J. Phys,* vol. 38, pp. 463-477, 2014.
[18] R. Duffy and M. Shayesteh, "Novel processing for access resistance reduction in Germanium devices," in *Junction Technology (IWJT), 2014 International Workshop on*, 2014, pp. 1-6.
[19] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *Electron Devices, IEEE Transactions on,* vol. 59, pp. 1813-1828, 2012.
[20] www.intel.com.
[21] M. J. H. van Dal, G. Vellianitis, B. Duriez, G. Doornbos, H. Chih-Hua, L. Bi-Hui, Y. Kai-Min, M. Passlack, and C. H. Diaz, "Germanium p-Channel FinFET Fabricated by Aspect Ratio Trapping," *Electron Devices, IEEE Transactions on,* vol. 61, pp. 430-436, 2014.
[22] B. R. Yates, B. L. Darby, N. G. Rudawski, K. S. Jones, D. H. Petersen, O. Hansen, R. Lin, P. F. Nielsen, and A. Kontos, "Anomalous activation of shallow B+ implants in Ge," *Materials Letters,* vol. 65, pp. 3540-3543, 2011.
[23] G. Hellings, E. Rosseel, T. Clarysse, D. H. Petersen, O. Hansen, P. F. Nielsen, E. Simoen, G. Eneman, B. De Jaeger, T. Hoffmann, K. De Meyer, and W. Vandervorst, "Systematic study of shallow junction formation on germanium substrates," *Microelectronic Engineering,* vol. 88, pp. 347-350, 2011.
[24] K. C. Saraswat, C. Chi On, K. Donghyun, T. Krishnamohan, and A. Pethe, "High Mobility Materials and Novel Device Structures for High Performance Nanoscale MOSFETs," in *Electron Devices Meeting, 2006. IEDM '06. International*, 2006, pp. 1-4.
[25] R. T. Tung, "The physics and chemistry of the Schottky barrier height," *Applied Physics Reviews,* vol. 1, p. 011304 2014.
[26] J. P. Colinge and C. A. Colinge, *Physics of Semiconductor Devices*: Springer, 2005.
[27] G. W. Neudeck, *The PN Junction Diode: Volume II (Modular Series on Solid State Devices)*, 2 ed. vol. 2: Addison-wesley publishing company.
[28] T. Nishimura, K. Kita, and A. Toriumi, "Evidence for strong Fermi-level pinning due to metal-induced gap states at metal/germanium interface," *Applied Physics Letters,* vol. 91, p. 123123, 2007.
[29] T. Nishimura, K. Kita, and A. Toriumi, "A significant shift of Schottky barrier heights at strongly pinned metal/germanium interface by inserting an ultra-thin insulating film," *Applied physics express,* vol. 1, p. 51406, 2008.
[30] A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. K. Evangelou, "Fermi-level pinning and charge neutrality level in germanium," *Applied Physics Letters,* vol. 89, p. 252110, 2006.
[31] D. K. Schroder, *Semiconductor material and device characterization*: Wiley-IEEE Press, 2006.

[32] R. R. Lieten, S. Degroote, M. Kuijk, and G. Borghs, "Ohmic contact formation on n-type Ge," *Applied Physics Letters*, vol. 92, p. 022106, 2008.
[33] T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita, and A. Toriumi, "Proof of Ge-interfacing Concepts for Metal/High-k/Ge CMOS - Ge-intimate Material Selection and Interface Conscious Process Flow," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 697-700.
[34] Y. Zhou, W. Han, Y. Wang, F. Xiu, J. Zou, R. Kawakami, and K. L. Wang, "Investigating the origin of Fermi level pinning in Ge Schottky junctions using epitaxially grown ultrathin MgO films," *Applied Physics Letters*, vol. 96, p. 102103, 2010.
[35] K. Yamamoto, M. Mitsuhara, K. Hiidome, R. Noguchi, M. Nishida, D. Wang, and H. Nakashima, "Role of an interlayer at a TiN/Ge contact to alleviate the intrinsic Fermi-level pinning position toward the conduction band edge," *Applied Physics Letters*, vol. 104, pp. 132109, 2014.
[36] A. M. Roy, J. Y. J. Lin, and K. C. Saraswat, "Specific Contact Resistivity of Tunnel Barrier Contacts Used for Fermi Level Depinning," *Electron Device Letters, IEEE*, vol. 31, pp. 1077-1079, 2010.
[37] S. Gaudet, C. Detavernier, A. Kellock, P. Desjardins, and C. Lavoie, "Thin film reaction of transition metals with germanium," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 24, p. 474, 2006.
[38] D. P. Brunco, B. D. Jaeger, G. Eneman, J. Mitard, G. Hellings, A. Satta, V. Terzieva, L. Souriau, F. E. Leys, G. Pourtois, M. Houssa, G. Winderickx, E. Vrancken, S. Sioncke, K. Opsomer, G. Nicholas, M. Caymax, A. Stesmans, J. V. Steenbergen, P. W. Mertens, *et al.*, "Germanium MOSFET Devices: Advances in Materials Understanding, Process Development, and Electrical Performance," *Journal of The Electrochemical Society*, vol. 155, pp. H552-H561, 2008.
[39] K. Lee, S. Liew, S. Chua, D. Chi, H. Sun, and X. Pan, "Formation and Morphology Evolution of Nickel Germanides on Ge (100) Under Rapid Thermal Annealing," 2004, pp. 55-60.
[40] Q. Zhang, N. Wu, T. Osipowicz, L. K. Bera, and C. Zhu, "Formation and thermal stability of nickel germanide on germanium substrate," *Japanese Journal of Applied Physics part 2 letters*, vol. 44, 2005.
[41] M. Mueller, Q. T. Zhao, C. Urban, C. Sandow, D. Buca, S. Lenk, S. Estévez, and S. Mantl, "Schottky-barrier height tuning of NiGe/n-Ge contacts using As and P segregation," *Materials Science and Engineering: B*, vol. 154-155, pp. 168-171, 2008.
[42] T. Yi, L. Bin, P. S. Y. Lim, and Y. Yee-Chia, "Selenium Segregation for Effective Schottky Barrier Height Reduction in NiGe/n-Ge Contacts," *Electron Device Letters, IEEE*, vol. 33, pp. 773-775, 2012.
[43] T. Nishimura, S. Sakata, K. Nagashio, K. Kita, and A. Toriumi, "Low Temperature Phosphorus Activation in Germanium through Nickel Germanidation for Shallow n+/p Junction," *Applied physics express*, vol. 2, p. 1202, 2009.

[44] M. Koike, Y. Kamimuta, and T. Tezuka, "Modulation of NiGe/Ge Contact Resistance by S and P Co-introduction," *Applied physics express,* vol. 4, p. 021301, 2011.
[45] K. Ikeda, Y. Yamashita, N. Sugiyama, N. Taoka, and S. Takagi, "Modulation of NiGe/Ge Schottky barrier height by sulfur segregation during Ni germanidation," *Applied Physics Letters,* vol. 88, p. 152115, 2006.
[46] K. Gallacher, P. Velha, D. J. Paul, I. MacLaren, M. Myronov, and D. R. Leadley, "Ohmic contacts to n-type germanium with low specific contact resistivity," *Applied Physics Letters,* vol. 100, pp. 022113, 2012.
[47] H. Li, H. H. Cheng, L. C. Lee, C. P. Lee, L. H. Su, and Y. W. Suen, "Electrical characteristics of Ni Ohmic contact on n-type GeSn," *Applied Physics Letters,* vol. 104, p. 241904, 2014.
[48] L. Hutin, C. Le Royer, C. Tabone, V. Delaye, F. Nemouchi, F. Aussenac, L. Clavelier, and M. Vinet, "Schottky Barrier Height Extraction in Ohmic Regime: Contacts on Fully Processed GeOI Substrates," *Journal of The Electrochemical Society,* vol. 156, p. H522, 2009.
[49] M. Koike, Y. Kamimuta, E. Kurosawa, and T. Tezuka, "NiGe/n + -Ge junctions with ultralow contact resistivity formed by two-step P-ion implantation," *Applied Physics Express,* vol. 7, p. 051302, 2014.
[50] H. Miyoshi, T. Ueno, Y. Hirota, J. Yamanaka, K. Arimoto, K. Nakagawa, and T. Kaitsuka, "Low contact resistances using carrier activation enhancement for Germanium CMOSFETs," in *Junction Technology (IWJT), 2014 International Workshop on,* 2014, pp. 1-5.
[51] E. Dubois, G. Larrieu, N. Breil, R. Valentin, F. Danneville, D. Yarekha, G. Dambrine, A. Halimaoui, A. Pouydebasque, and T. Skotnicki, "Recent advances in metallic source/drain MOSFETs," in *Junction Technology, 2008. IWJT '08. Extended Abstracts - 2008 8th International workshop on*, 2008, pp. 139-144.
[52] C. Henkel, S. Abermann, O. Bethge, G. Pozzovivo, S. Puchner, H. Hutter, and E. Bertagnolli, "Reduction of the PtGe/Ge Electron Schottky-Barrier Height by Rapid Thermal Diffusion of Phosphorous Dopants," *Journal of The Electrochemical Society,* vol. 157, pp. H815-H820, 2010.
[53] D. C. S. Dumas, K. Gallacher, R. Millar, I. MacLaren, M. Myronov, D. R. Leadley, and D. J. Paul, "Silver antimony Ohmic contacts to moderately doped n-type germanium," *Applied Physics Letters,* vol. 104, p. 162101, 2014.
[54] J.-R. Wu, Y.-H. Wu, C.-Y. Hou, M.-L. Wu, C.-C. Lin, and L.-L. Chen, "Impact of fluorine treatment on Fermi level depinning for metal/germanium Schottky junctions," *Applied Physics Letters,* vol. 99, pp. 253504, 2011.
[55] Z.-W. Zheng, T.-C. Ku, M. Liu, and A. Chin, "Ohmic contact on n-type Ge using Yb-germanide," *Applied Physics Letters,* vol. 101, p. 223501, 2012.
[56] A. Firrincieli, K. Martens, R. Rooyackers, B. Vincent, E. Rosseel, E. Simoen, J. Geypen, H. Bender, C. Claeys, and J. A. Kittl, "Study of ohmic contacts to n-type Ge: Snowplow and laser activation," *Applied Physics Letters,* vol. 99, pp. 242104, 2011.
[57] P. Shi Ya Lim, D. Zhi Chi, X. Cai Wang, and Y.-C. Yeo, "Fermi-level depinning at the metal-germanium interface by the formation of epitaxial

nickel digermanide NiGe2 using pulsed laser anneal," *Applied Physics Letters*, vol. 101, p. 172103, 2012.

[58] P. Bhatt, P. Swarnkar, F. Basheer, C. Hatem, A. Nainani, and S. Lodha, "High Performance 400 °C p^+/n Ge Junctions Using Cryogenic Boron Implantation," *Electron Device Letters, IEEE*, vol. 35, pp. 717-719, 2014.

[59] S. Brotzmann and H. Bracht, "Intrinsic and extrinsic diffusion of phosphorus, arsenic, and antimony in germanium," *Journal of Applied Physics*, vol. 103, p. 033508, 2008.

[60] R. Duffy, M. Shayesteh, M. White, J. Kearney, and A.-M. Kelleher, "The formation, stability, and suitability of n-type junctions in germanium formed by solid phase epitaxial recrystallization," *Applied Physics Letters*, vol. 96, p. 231909, 2010.

[61] C. O. Chui, L. Kulig, J. Moran, W. Tsai, and K. C. Saraswat, "Germanium n-type shallow junction activation dependences," *Applied Physics Letters*, vol. 87, p. 091909, 2005.

[62] C. Yu-Lin and J. C. S. Woo, "Germanium n+/p Diodes: A Dilemma Between Shallow Junction Formation and Reverse Leakage Current Control," *Electron Devices, IEEE Transactions on*, vol. 57, pp. 665-670, 2010.

[63] http://www.srim.org.

[64] J. Y. Spann, R. A. Anderson, T. J. Thornton, G. Harris, S. G. Thomas, and C. Tracy, "Characterization of nickel germanide thin films for use as contacts to p-channel germanium MOSFETs," *Electron Device Letters, IEEE*, vol. 26, pp. 151-153, 2005.

[65] S.-M. Koh, E. Y. J. Kong, B. Liu, C.-M. Ng, P. Liu, Z.-Q. Mo, K.-C. Leong, G. S. Samudra, and Y.-C. Yeo, "New Tellurium implant and segregation for contact resistance reduction and single metallic silicide technology for independent contact resistance optimization in n- and p-FinFETs," in *VLSI Technology, Systems and Applications (VLSI-TSA), 2011 International Symposium on*, 2011, pp. 1-2.

[66] J. H. J. Oh, Y. –T. Chen, I. Ok, K. Jeon, and S. –H. Lee, "High Specific Contact Resistance of Ohmic Contacts to n-Ge Source/Drain and Low Transport Characteristics of Ge nMOSFETs," *Proceedings of International Conference on Solid State Devices and Materials 2010*, pp. paper P-3-20.

[67] K. Martens, A. Firrincieli, R. Rooyackers, B. Vincent, R. Loo, S. Locorotondo, E. Rosseel, T. Vandeweyer, G. Hellings, B. De Jaeger, M. Meuris, P. Favia, H. Bender, B. Douhard, J. Delmotte, W. Vandervorst, E. Simoen, G. Jurczak, D. Wouters, and J. A. Kittl, "Record low contact resistivity to n-type Ge for CMOS and memory applications," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, pp. 18.14.11-18.14.14.

[68] S. Raghunathan, T. Krishnamohan, and K. C. Saraswat, "Novel SiGe Source/Drain for Reduced Parasitic Resistance in Ge NMOS," *ECS Transactions*, vol. 33, pp. 871-876, 2010.

[69] G. Thareja, J. Liang, S. Chopra, B. Adams, N. Patil, S. L. Cheng, A. Nainani, E. Tasyurek, Y. Kim, S. Moffatt, R. Brennan, J. McVittie, T. Kamins, K. Saraswat, and Y. Nishi, "High performance germanium n-MOSFET with antimony dopant activation beyond $1x10^{20}$ cm^{-3}," in *Electron*

Devices Meeting (IEDM), 2010 IEEE International, 2010, pp. 10.15.11-10.15.14.

[70] S.-L. Cheng, G. Thareja, T. Kamins, K. Saraswat, and a. Y. Nishi, "Electrical Characteristics of Germanium n+/p Junctions Obtained Using Rapid Thermal Annealing of Coimplanted P and Sb " *Electron Device Letters, IEEE*, vol. 32, pp. 608-610, 2011.

[71] www.itrs.net. *The International Technology Roadmap for Semiconductors*.

[72] C. C. Liao, A. Chin, N. C. Su, M. F. Li, and S. J. Wang, "Low Vt gate-first Al/TaN/[Ir_3Si-$HfSi_{2-x}$]/HfLaON CMOS using simple laser annealing/reflection," in *VLSI Technology, 2008 Symposium on*, 2008, pp. 190-191.

[73] V. Mazzocchi, C. Sabatier, M. Py, K. Huet, C. Boniface, J. P. Barnes, L. Hutin, V. Delayer, D. Morel, M. Vinet, C. Le Royer, J. Venturini, and K. Yckache, "Boron and Phosphorus dopant activation in Germanium using laser annealing with and without preamorphization implant," in *Advanced Thermal Processing of Semiconductors, 2009. RTP '09. 17th International Conference on*, 2009, pp. 1-5.

[74] W. Szyszko, F. Vega, and C. N. Afonso, "Shifting of the thermal properties of amorphous germanium films upon relaxation and crystallization," *Applied Physics A*, vol. 61, pp. 141-147, 1995.

[75] M. K. Husain, X. V. Li, and C. H. de Groot, "High-Quality Schottky Contacts for Limiting Leakage Currents in Ge-Based Schottky Barrier MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 56, pp. 499-504, 2009.

[76] P. S. Y. Lim, D. Z. Chi, P. C. Lim, X. C. Wang, T. K. Chan, T. Osipowicz, and Y.-C. Yeo, "Formation of epitaxial metastable $NiGe_2$ thin film on Ge(100) by pulsed excimer laser anneal," *Applied Physics Letters*, vol. 97, pp. 182104, 2010.

[77] X. Gao, J. Andersson, T. Kubart, T. Nyberg, U. Smith, J. Lu, L. Hultman, A. J. Kellock, Z. Zhang, C. Lavoie, and S.-L. Zhang, "Epitaxy of Ultrathin $NiSi_2$ Films with Predetermined Thickness," *Electrochemical and Solid-State Letters*, vol. 14, pp. H268-H270, 2011.

[78] F. A. Trumbore, "Solid Solubilities of Impurity Elements in Germanium and Silicon," *Bell System Tech. J*, vol. 39, p. 205, 1960.

[79] "JCPDS diffraction file 07-0297 (NiGe)".

[80] D. R. Gajula, D. W. McNeill, B. E. Coss, H. Dong, S. Jandhyala, J. Kim, R. M. Wallace, and B. M. Armstrong, "Low temperature fabrication and characterization of nickel germanide Schottky source/drain contacts for implant-less germanium p-channel metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters*, vol. 100, pp. 192101, 2012.

[81] F. Nemouchi, D. Mangelinck, C. Bergman, G. Clugnet, P. Gas, and J. L. Labar, "Simultaneous growth of Ni_5Ge_3 and NiGe by reaction of Ni film with Ge," *Applied Physics Letters*, vol. 89, pp. 131920, 2006.

[82] S. Gaudet, C. Detavernier, C. Lavoie, and P. Desjardins, "Reaction of thin Ni films with Ge: Phase formation and texture," *Journal of Applied Physics*, vol. 100, p. 034306, 2006.

[83] M. Shayesteh, C. L. L. M. Daunt, D. O'Connell, V. Djara, M. White, B. Long, and R. Duffy, "NiGe Contacts and Junction Architectures for P and

As Doped Germanium Devices," *Electron Devices, IEEE Transactions on,* vol. 58, pp. 3801-3807, 2011.

[84] K. Park, B. H. Lee, D. Lee, D.-H. Ko, K. H. Kwak, C.-W. Yang, and H. Kim, "A Study on the Thermal Stabilities of the NiGe and Ni_{1-x} Ta_x Ge Systems," *Journal of The Electrochemical Society,* vol. 154, pp. H557-H560, 2007.

[85] O. Nakatsuka, A. Suzuki, A. Sakai, M. Ogawa, and S. Zaima, "Impact of Pt Incorporation on Thermal Stability of NiGe Layers on Ge(001) Substrates," in *Junction Technology, 2007 International Workshop on*, 2007, pp. 87-88.

[86] S. Zhu, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Enhanced thermal stability of nickel germanide on thin epitaxial germanium by adding an ultrathin titanium layer," *Applied Physics Letters,* vol. 91, p. 051905, 2007.

[87] K. Min-Ho, S. Hong-Sik, Y. Jung-Ho, L. Ga-Won, O. Jung-Woo, P. Majhi, R. Jammy, and L. Hi-Deok, "Thermally Robust Ni Germanide Technology Using Cosputtering of Ni and Pt for High-Performance Nanoscale Ge MOSFETs," *Nanotechnology, IEEE Transactions on,* vol. 11, pp. 769-776, 2012.

[88] Z. Ying-Ying, O. Jungwoo, H. In-Shik, Z. Zhong, S.-G. Li, S.-Y. Jung, P. Kee-Young, S. Hong-Sik, C. Won-Ho, K. Hyuk-Min, L. Wei-Yip, P. Majhi, R. Jammy, and L. Hi-Deok, "Thermal Immune NiGermanide for High Performance Ge MOSFETs on Ge-on-Si Substrate Utilizing $Ni_{0.95}Pd_{0.05}$ Alloy," *Electron Devices, IEEE Transactions on,* vol. 56, pp. 348-353, 2009.

[89] Y.-Y. Zhang, J. Oh, S.-G. Li, S.-Y. Jung, K.-Y. Park, H.-S. Shin, G.-W. Lee, J.-S. Wang, P. Majhi, H.-H. Tseng, R. Jammy, T.-S. Bae, and H.-D. Lee, "Ni Germanide Utilizing Ytterbium Interlayer for High-Performance Ge MOSFETs," *Electrochemical and Solid-State Letters,* vol. 12, pp. H18-H20, 2009.

[90] A. Renau, "(Invited) Recent Developments in Ion Implantation," *ECS Transactions,* vol. 35, pp. 173-184, 2011.

[91] L. Eriksson, J. A. Davies, N. G. E. Johansson, and J. W. Mayer, "Implantation and Annealing Behavior of Group III and V Dopants in Silicon as Studied by the Channeling Technique," *Journal of Applied Physics,* vol. 40, pp. 842-854, 1969.

[92] L. Pelaz, R. Duffy, M. Aboy, L. Marques, P. Lopez, I. Santos, B. J. Pawlak, M. v. Dal, B. Duriez, T. Merelle, G. Doornbos, N. Collaert, L. Witters, R. Rooyackers, W. Vandervorst, M. Jurczak, M. Kaiser, R. Weemaes, J. v. Berkum, P. Breimer, *et al.*, "Atomistic modeling of impurity ion implantation in ultra-thin-body Si devices," *Electron Devices Meeting*, pp. 1-4, 2008.

[93] M. Togo, Y. Sasaki, G. Zschatzsch, G. Boccardi, R. Ritzenthaler, J. W. Lee, F. Khaja, B. Colombeau, L. Godet, P. Martin, S. Brus, S. E. Altamirano, G. Mannaert, H. Dekkers, G. Hellings, N. Horiguchi, W. Vandervorst, and A. Thean, "Heated implantation with amorphous Carbon CMOS mask for scaled FinFETs," in *VLSI Technology (VLSIT), 2013 Symposium on*, 2013, pp. T196-T197.

[94] K. Han, S. Tang, T. Rockwell, L. Godet, H. Persing, C. Campbell, and S. Salimian, "A novel plasma-based technique for conformal 3D FINFET

doping," in *Junction Technology (IWJT), 2012 12th International Workshop on*, 2012, pp. 35-37.
[95] S. Takeuchi, N. D. Nguyen, F. E. Leys, R. Loo, T. Conard, W. Vandervorst, and M. Caymax, "Vapor Phase Doping with N-type Dopant into Silicon by Atmospheric Pressure Chemical Vapor Deposition," *ECS Transactions,* vol. 16, pp. 495-502, 2008.
[96] J. C. Ho, R. Yerushalmi, Z. A. Jacobson, Z. Fan, R. L. Alley, and A. Javey, "Controlled nanoscale doping of semiconductors via molecular monolayers," *Nat Mater,* vol. 7, pp. 62-67, 2008.
[97] B. Hartiti, A. Slaoui, J. C. Muller, R. Stuck, and P. Siffert, "Phosphorus diffusion into silicon from a spin-on source using rapid thermal processing," *Journal of Applied Physics,* vol. 71, pp. 5474-5478, 1992.
[98] M. Takenaka, K. Morii, M. Sugiyama, Y. Nakano, and S. Takagi, "Gas Phase Doping of Arsenic into (100), (110), and (111) Germanium Substrates Using a Metal–Organic Source," *Japanese Journal of Applied Physics,* vol. 50, p. 010105, 2011.
[99] S. Heo, S. Baek, D. Lee, M. Hasan, H. Jung, J. Lee, and H. Hwang, "Sub-15 nm n+/p -Germanium Shallow Junction Formed by PH3 Plasma Doping and Excimer Laser Annealing," *Electrochemical and Solid-State Letters,* vol. 9, pp. G136-G137, 2006.
[100] B. Long, G. A. Verni, J. O'Connell, J. Holmes, M. Shayesteh, D. O'Connell, and R. Duffy, "Molecular Layer Doping: Non-destructive Doping of Silicon and Germanium," This work was presented in IIT 2014 in Portland, Oregon.
[101] A. Chroneos and H. Bracht, "Diffusion of n-type dopants in germanium," *Applied Physics Reviews,* vol. 1, p. 011301, 2014.
[102] G. Impellizzeri, S. Mirabella, A. Irrera, M. G. Grimaldi, and E. Napolitani, "Ga-implantation in Ge: Electrical activation and clustering," *Journal of Applied Physics,* vol. 106, p. 013518, 2009.
[103] R. J. Kaiser, S. Koffel, P. Pichler, A. J. Bauer, B. Amon, A. Claverie, G. Benassayag, P. Scheiblin, L. Frey, and H. Ryssel, "Honeycomb voids due to ion implantation in germanium," *Thin Solid Films,* vol. 518, pp. 2323-2325, 2010.
[104] Y.Bao, K. Sun, N. Dhar, and M. C. Gupta, "Germanium p-n Junctions by Laser Doping for Photonics/Microelectronic Devices," *Photonics Technology Letters, IEEE,* vol. 26, pp. 1422-1425, 2014.
[105] R. Duffy, "Metastable Activation of Dopants by Solid Phase Epitaxial Recrystallisation," in *Subsecond Annealing of Advanced Materials*. vol. 192, W. Skorupa and H. Schmidt, Eds., ed: Springer International Publishing, 2014, pp. 35-56.
[106] Y.-J. Lee, "Dopant activation by microwave anneal," in *Junction Technology (IWJT), 2011 11th International Workshop on*, 2011, pp. 44-49.
[107] J. Huang, N. Wu, Q. Zhang, C. Zhu, A. A. O. Tay, G. Chen, and M. Hong, "Germanium n+/p junction formation by laser thermal process," *Applied Physics Letters,* vol. 87, p. 173507 2005.
[108] G. Hellings, E. Rosseel, E. Simoen, D. Radisic, D. H. Petersen, O. Hansen, P. F. Nielsen, G. Zschätzsch, A. Nazir, and T. Clarysse, "Ultra shallow arsenic junctions in germanium formed by millisecond laser annealing," *Electrochemical and Solid-State Letters*, vol. 14, pp. H39-H41, 2011.

[109] M. Shayesteh, K. Huet, I. Toque-Tresonne, R. Negru, C. L. M. Daunt, N. Kelly, D. O'Connell, R. Yu, V. Djara, P. B. Carolan, N. Petkov, and R. Duffy, "Atomically Flat Low-Resistive Germanide Contacts Formed by Laser Thermal Anneal," *Electron Devices, IEEE Transactions on,* vol. 60, pp. 2178-2185, 2013.

[110] R. Milazzo, E. Napolitani, G. Impellizzeri, G. Fisicaro, S. Boninelli, M. Cuscunà, D. De Salvador, M. Mastromatteo, M. Italia, A. La Magna, G. Fortunato, F. Priolo, V. Privitera, and A. Carnera, "N-type doping of Ge by As implantation and excimer laser annealing," *Journal of Applied Physics,* vol. 115, p. 053501, 2014.

[111] P. Tsouroutas, D. Tsoukalas, I. Zergioti, N. Cherkashin, and A. Claverie, "Modeling and experiments on diffusion and activation of phosphorus in germanium," *Journal of Applied Physics,* vol. 105, p. 094910, 2009.

[112] K. L. Pey, K. K. Ong, P. S. Lee, Y. Setiawan, X. C. Wang, A. T. S. Wee, and G. C. Lim, "Formation of Silicided Hyper-Shallow p+/n- Junctions by Pulsed Laser Annealing," *ECS Transactions,* vol. 11, pp. 379-394, 2007.

[113] V. Ioannou-Sougleridis, S. F. Galata, E. Golias, T. Speliotis, A. Dimoulas, D. Giubertoni, S. Gennaro, and M. Barozzi, "High performance n+/p and p+/n germanium diodes at low-temperature activation annealing," *Microelectronic Engineering,* vol. 88, pp. 254-261, 2011.

[114] G. Impellizzeri, E. Napolitani, S. Boninelli, G. Fisicaro, M. Cuscunà, R. Milazzo, A. L. Magna, G. Fortunato, F. Priolo, and V. Privitera, "B-doping in Ge by excimer laser annealing," *Journal of Applied Physics,* vol. 113, p. 113505, 2013.

[115] C. O. Chui, K. Gopalakrishnan, P. B. Griffin, J. D. Plummer, and K. C. Saraswat, "Activation and diffusion studies of ion-implanted p and n dopants in germanium," *Applied Physics Letters,* vol. 83, pp. 3275-3277, 2003.

[116] G. Fisicaro, L. Pelaz, M. Aboy, P. Lopez, M. Italia, K. Huet, F. Cristiano, Z. Essa, Q. Yang, E. Bedel-Pereira, M. Quillec, and A. L. Magna, "Kinetic Monte Carlo simulations of boron activation in implanted Si under laser thermal annealing," *Applied Physics Express,* vol. 7, p. 021301, 2014.

[117] C. Nyamhere, A. Venter, F. D. Auret, S. M. M. Coelho, and D. M. Murape, "Characterization of the E(0.31) defect introduced in bulk n-Ge by H or He plasma exposure," *Journal of Applied Physics,* vol. 111, p. 044511, 2012.

[118] C. Nyamhere, F. Cristiano, F. Olivie, Z. Essa, E. Bedel-Pereira, D. Bolze, and Y. Yamamoto, "Electrical characterisation and predictive simulation of defects induced by keV Si+ implantation in n-type Si," *Journal of Applied Physics,* vol. 113, p. 184508, 2013.

[119] R. Duffy, A. Heringa, V. C. Venezia, J. Loo, M. A. Verheijen, M. J. P. Hopstaken, K. van der Tak, M. de Potter, J. C. Hooker, P. Meunier-Beillard, and R. Delhougne, "Quantitative prediction of junction leakage in bulk-technology CMOS devices," *Solid-State Electronics,* vol. 54, pp. 243-251, 2010.

[120] R. Duffy and A. Heringa, "Characterisation of electrically active defects," *physica status solidi (c),* vol. 11, pp. 130-137, 2014.

[121] G. Eneman, O. Sicart i Casain, E. Simoen, D. P. Brunco, B. De Jaeger, A. Satta, G. Nicholas, C. Claeys, M. Meuris, and M. M. Heyns, "Analysis of

junction leakage in advanced germanium P+/n junctions," in *Solid State Device Research Conference, 2007. ESSDERC 2007. 37th European*, 2007, pp. 454-457.

[122] M. El Kurdi, G. Fishman, S. Sauvage, and P. Boucaud, "Band structure and optical gain of tensile-strained germanium based on a 30 band k·p formalism," *Journal of Applied Physics,* vol. 107, p. 013710, 2010.

[123] M. Jamil, J. Mantey, E. U. Onyegam, G. D. Carpenter, E. Tutuc, and S. K. Banerjee, "High-Performance Ge nMOSFETs With n^+-p Junctions Formed by "Spin-On Dopant"," *Electron Device Letters, IEEE,* vol. 32, pp. 1203-1205, 2011.

[124] D. Kuzum, A. J. Pethe, T. Krishnamohan, and K. C. Saraswat, "Ge (100) and (111) N- and P-FETs With High Mobility and Low-*T* Mobility Characterization," *Electron Devices, IEEE Transactions on,* vol. 56, pp. 648-655, 2009.

[125] K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, "High-Performance GeO_2 /Ge nMOSFETs With Source/Drain Junctions Formed by Gas-Phase Doping," *Electron Device Letters, IEEE,* vol. 31, pp. 1092-1094, 2010.

[126] H.-Y. Yu, S.-L. Cheng, P. B. Griffin, Y. Nishi, and K. C. Saraswat, "Germanium *In Situ* Doped Epitaxial Growth on Si for High-Performance n^+/p- Junction Diode," *Electron Device Letters, IEEE,* vol. 30, pp. 1002-1004, 2009.

[127] K. Yamamoto, T. Yamanaka, R. Ueno, K. Hirayama, H. Yang, D. Wang, and H. Nakashima, "Source/drain junction fabrication for Ge metal-oxide-semiconductor field-effect transistors," *Thin Solid Films,* vol. 520, pp. 3382-3386, 2012.

[128] M. Naganawa, Y. Shimizu, M. Uematsu, K. M. Itoh, K. Sawano, Y. Shiraki, and E. E. Haller, "Charge states of vacancies in germanium investigated by simultaneous observation of germanium self-diffusion and arsenic diffusion," *Applied Physics Letters,* vol. 93, p. 191905, 2008.

[129] C. I. Li, R. Liu, M. Chan, T. F. Hsiao, C. L. Yang, and S. F. Tzou, "Control of Source and Drain Extension Phosphorus Profile by Using Carbon Co-Implant," in *Advanced Thermal Processing of Semiconductors, 2007. RTP 2007. 15th International Conference on*, 2007, pp. 127-130.

[130] S. Brotzmann, H. Bracht, J. L. Hansen, A. N. Larsen, E. Simoen, E. E. Haller, J. S. Christensen, and P. Werner, "Diffusion and defect reactions between donors, C, and vacancies in Ge. I. Experimental results," *Physical Review B,* vol. 77, p. 235207, 2008.

[131] E. Simoen, A. Satta, A. D'Amore, T. Janssens, T. Clarysse, K. Martens, B. De Jaeger, A. Benedetti, I. Hoflijk, B. Brijs, M. Meuris, and W. Vandervorst, "Ion-implantation issues in the formation of shallow junctions in germanium," *Materials Science in Semiconductor Processing,* vol. 9, pp. 634-639, 2006.

[132] E. S. A. Satta, B. Van Daele, T. Clarysse, G. Nicholas, W. Vandervorst, W. Anwand, W. Skorupa, T. Peaker, V. Markevich, "Junction Formation In Ge By Ion Implantation," *Proceedings of INSIGHT,* 2007.

[133] H. A. W. El Mubarek and P. Ashburn, "Reduction of boron thermal diffusion in silicon by high energy fluorine implantation," *Applied Physics Letters,* vol. 83, pp. 4134-4136, 2003.
[134] P. López, L. Pelaz, R. Duffy, P. Meunier-Beillard, F. Roozeboom, K. van der Tak, P. Breimer, J. G. M. van Berkum, M. A. Verheijen, and M. Kaiser, "Si interstitial contribution of F+ implants in crystalline Si," *Journal of Applied Physics,* vol. 103, p. 093538, 2008.
[135] P. Pichler, *Intrinsic Point Defects, Impurities, and their Diffusion in Silicon*. NewYork: Springer, 2004.
[136] S. P. Jeng, T. P. Ma, R. Canteri, M. Anderle, and G. W. Rubloff, "Anomalous diffusion of fluorine in silicon," *Applied Physics Letters,* vol. 61, pp. 1310-1312, 1992.
[137] G. R. Nash, J. F. W. Schiz, C. D. Marsh, P. Ashburn, and G. R. Booker, "Activation energy for fluorine transport in amorphous silicon," *Applied Physics Letters,* vol. 75, pp. 3671-3673, 1999.
[138] M. Diebel and S. T. Dunham, "*Ab Initio* Calculations to Model Anomalous Fluorine Behavior," *Physical Review Letters,* vol. 93, p. 245901, 2004.
[139] N. E. B. Cowern, B. Colombeau, J. Benson, A. J. Smith, W. Lerch, S. Paul, T. Graf, F. Cristiano, X. Hebras, and D. Bolze, "Mechanisms of B deactivation control by F co-implantation," *Applied Physics Letters,* vol. 86, p. 101905, 2005.
[140] A. Chroneos, R. W. Grimes, and H. Bracht, "Fluorine codoping in germanium to suppress donor diffusion and deactivation," *Journal of Applied Physics,* vol. 106, p. 063707 2009.
[141] W.-S. Jung, J.-H. Park, A. Nainani, D. Nam, and K. C. Saraswat, "Fluorine passivation of vacancy defects in bulk germanium for Ge metal-oxide-semiconductor field-effect transistor application," *Applied Physics Letters,* vol. 101, p. 072104, 2012.
[142] N. Ioannou, D. Skarlatos, C. Tsamis, C. A. Krontiras, S. N. Georga, A. Christofi, and D. S. McPhail, "Germanium substrate loss during low temperature annealing and its influence on ion-implanted phosphorous dose loss," *Applied Physics Letters,* vol. 93, p. 101910, 2008.
[143] H. A. W. El Mubarek, J. M. Bonar, G. D. Dilliway, P. Ashburn, M. Karunaratne, A. F. Willoughby, Y. Wang, P. L. F. Hemment, R. Price, J. Zhang, and P. Ward, "Effect of fluorine implantation dose on boron thermal diffusion in silicon," *Journal of Applied Physics,* vol. 96, pp. 4114-4121, 2004.
[144] H. A. El Mubarek, M. Karunaratne, J. M. Bonar, G. D. Dilliway, Y. Wang, P. L. F. Hemment, A. F. Willoughby, and P. Ashburn, "Effect of fluorine implantation dose on boron transient enhanced diffusion and boron thermal diffusion in $Si_{1-x}Ge_x$," *Electron Devices, IEEE Transactions on,* vol. 52, pp. 518-526, 2005.
[145] L. Romano, G. Impellizzeri, M. V. Tomasello, F. Giannazzo, C. Spinella, and M. G. Grimaldi, "Nanostructuring in Ge by self-ion implantation," *Journal of Applied Physics,* vol. 107, p. 084314, 2010.
[146] H. Bracht and S. Brotzmann, "Atomic transport in germanium and the mechanism of arsenic diffusion," *Materials Science in Semiconductor Processing,* vol. 9, pp. 471-476, 2006.

[147] G. Impellizzeri, S. Boninelli, F. Priolo, E. Napolitani, C. Spinella, A. Chroneos, and H. Bracht, "Fluorine effect on As diffusion in Ge," *Journal of Applied Physics*, vol. 109, p. 113527, 2011.
[148] H. A. W. El Mubarek, "Reduction of phosphorus diffusion in germanium by fluorine implantation," *Journal of Applied Physics*, vol. 114, p. 223512, 2013.
[149] A. Chroneos, "Effect of germanium substrate loss and nitrogen on dopant diffusion in germanium," *Journal of Applied Physics*, vol. 105, p. 056101 2009.
[150] K. Kita, S. Suzuki, H. Nomura, T. Takahashi, T. Nishimura, and A. Toriumi, "Direct Evidence of GeO Volatilization from GeO 2 /Ge and Impact of Its Suppression on GeO_2/Ge Metal–Insulator–Semiconductor Characteristics," *Japanese Journal of Applied Physics*, vol. 47, p. 2349, 2008.
[151] R. J. Kaiser, S. Koffel, P. Pichler, A. J. Bauer, B. Amon, L. Frey, and H. Ryssel, "Germanium substrate loss during thermal processing," *Microelectronic Engineering*, vol. 88, pp. 499-502, 2011.
[152] S. K. Sahari, H. Murakami, T. Fujioka, T. Bando, A. Ohta, K. Makihara, S. Higashi, and S. Miyazaki, "Native Oxidation Growth on Ge(111) and (100) Surfaces," *Japanese Journal of Applied Physics*, vol. 50, p. 04DA12, 2011.
[153] J. Oh and J. Campbell, "Thermal desorption of Ge native oxides and the loss of Ge from the surface," *Journal of Electronic Materials*, vol. 33, pp. 364-367, 2004.
[154] S. K. Sahari, A. Ohta, M. Matsui, K. Mishima, H. Murakami, S. Higashi, and S. Miyazaki, "Kinetics of thermally oxidation of Ge(100) surface," *Journal of Physics: Conference Series*, vol. 417, p. 012014, 2013.
[155] D. Schmeisser, R. D. Schnell, A. Bogen, F. J. Himpsel, D. Rieger, G. Landgren, and J. F. Morar, "Surface oxidation states of germanium," *Surface Science*, vol. 172, pp. 455-465, 1986.
[156] J. T. Law and P. S. Meigs, "Rates of Oxidation of Germanium," *Journal of The Electrochemical Society*, vol. 104, pp. 154-159, March 1, 1957 1957.
[157] E. E. Crisman, Y. M. Ercil, J. J. Loferski, and P. J. Stiles, "The Oxidation of Germanium Surfaces at Pressures Much Greater Than One Atmosphere," *Journal of The Electrochemical Society*, vol. 129, pp. 1845-1848, 1982.
[158] K. Kita, S. K. Wang, M. Yoshida, C. H. Lee, K. Nagashio, T. Nishimura, and A. Toriumi, "Comprehensive study of GeO_2 oxidation, GeO desorption and GeO_2-metal interaction -understanding of Ge processing kinetics for perfect interface control," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.
[159] J. Oh and J. C. Campbell, "Thermal desorption of Ge native oxides and loss of Ge from the surface," *Materials Science in Semiconductor Processing*, vol. 13, pp. 185-188, 2010.
[160] C. H. Lee, T. Tabata, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "Ge/GeO_2 Interface Control with High-Pressure Oxidation for Improving Electrical Characteristics," *Applied Physics Express*, vol. 2, p. 071404, 2009.
[161] K. Kita, C. H. Lee, T. Nishimura, K. Nagashio, and A. Toriumi, "Control of Properties of GeO2 Films and Ge/GeO2 Interfaces by the Suppression of GeO Volatilization," *ECS Transactions*, vol. 19, pp. 101-116, 2009.

[162] S. K. Wang, K. Kita, C. H. Lee, T. Tabata, T. Nishimura, K. Nagashio, and A. Toriumi, "Desorption kinetics of GeO from GeO2/Ge structure," *Journal of Applied Physics*, vol. 108, p. 054104, 2010.
[163] D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, "A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET," in *Electron Devices Meeting, 1989. IEDM '89. Technical Digest., International*, 1989, pp. 833-836.
[164] W. Vandervorst, J. L. Everaert, E. Rosseel, M. Jurczak, T. Hoffman, P. Eyben, J. Mody, G. Zschätzsch, S. Koelling, M. Gilbert, T. Poon, J. del Agua Borniquel, M. Foad, R. Duffy, and B. J. Pawlak, "Conformal Doping of FINFETs: a Fabrication and Metrology Challenge," *AIP Conference Proceedings*, vol. 1066, pp. 449-456, 2008.
[165] N. Lindert, L. Chang, Y.-K. Choi, E. H. Anderson, L. Wen-Chin, K. Tsu-Jae, J. Bokor, and H. Chenming, "Sub-60-nm quasi-planar FinFETs fabricated using a simplified process," *Electron Device Letters, IEEE*, vol. 22, pp. 487-489, 2001.
[166] R. Duffy, M. J. H. V. Dal, B. J. Pawlak, M. Kaiser, R. G. R. Weemaes, B. Degroote, E. Kunnen, and E. Altamirano, "Solid phase epitaxy versus random nucleation and growth in sub-20 nm wide fin field-effect transistors," *Applied Physics Letters*, vol. 90, p. 241912, 2007.
[167] M. J. Van Dal, G. Vellianitis, R. Duffy, G. Doornbos, B. Pawlak, B. Duriez, L.-S. Lai, A. Y. Hikavyy, T. Vandeweyer, M. Demand, E. Altamirano, R. Rooyackers, L. Witters, N. Collaert, M. Jurczak, M. Kaiser, R. G. Weemaes, and R. Lander, "Material Aspects and Challenges for SOI FinFET Integration," *ECS Transactions*, vol. 13, pp. 223-234, 2008.
[168] Y. Kunii, M. Tabe, and K. Kajiyama, "Amorphous-Si/crystalline-Si facet formation during Si solid-phase epitaxy near Si/SiO2 boundary," *Journal of Applied Physics*, vol. 56, pp. 279-285, 1984.
[169] Y. Sasaki, C. G. Jin, H. Tamura, B. Mizuno, R. Higaki, T. Satoh, K. Majima, H. Sauddin, K. Takagi, S. Ohmi, K. Tsutsui, and H. Iwai, "B_2H_6 plasma doping with "in-situ He pre-amorphization"," in *VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on*, 2004, pp. 180-181.
[170] B. Kalkofen, A. A. Amusan, M. Lisker, and E. P. Burte, "Investigation of oxide thin films deposited by atomic layer deposition as dopant source for ultra-shallow doping of silicon," *Microelectronic Engineering*, vol. 109, pp. 113-116, 2013.
[171] J. O'Connell, B. Long, R. Duffy, G. P. McGlacken, and J. D. Holmes, This work was presented in 2014 MRS spring meeting, San Francisco, California.
[172] Y. Sasaki, K. Okashita, K. Nakamoto, T. Kitaoka, B. Mizuno, and M. Ogura, "Conformal doping for FinFETs and precise controllable shallow doping for planar FET manufacturing by a novel B_2H_6/Helium Self-Regulatory Plasma Doping process," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1-4.
[173] T. E. Haynes and O. W. Holland, "Damage accumulation during ion implantation of unstrained $Si_{1-x}Ge_x$ alloy layers," *Applied Physics Letters*, vol. 61, pp. 61-63, 1992.
[174] A. Chilingarov, D. Lipka, J. S. Meyer, and T. Sloan, "Displacement energy for various ions in particle detector materials," *Nuclear Instruments and*

Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 449, pp. 277-287,.
[175] S. Wolf and R. N. Tauber, "Silicon Processing for the VLSI Era vol. 1: Process technology, 1986," ed: Lattice Press.
[176] R. Wittmann and S. Selberherr, "A study of ion implantation into crystalline germanium," *Solid-State Electronics*, vol. 51, pp. 982-988, 2007.
[177] R. Duffy, G. Curatola, B. J. Pawlak, G. Doornbos, K. van der Tak, P. Breimer, J. G. M. van Berkum, and F. Roozeboom, "Doping fin field-effect transistor sidewalls: Impurity dose retention in silicon due to high angle incident ion implants and the impact on device performance," *Journal of Vacuum Science & Technology B*, vol. 26, pp. 402-407, 2008.
[178] J. F. Ziegler, J. P. Biersack, and M. D. Ziegler, *SRIM : the stopping and range of ions in matter*. Chester, Md.: SRIM Co., 2012.
[179] R. A. Kelly, J. D. Holmes, and N. Petkov, "Visualising discrete structural transformations in germanium nanowires during ion beam irradiation and subsequent annealing," *Nanoscale*, vol. 6, pp. 12890-12897, 2014.
[180] I. S. Tejido, *Multiscale Modeling of Dopant Implantation and Diffusion in Crystalline and Amorphous Silicon*, 2010.
[181] H. Yokoyama, Y. Ohta, K. Toko, T. Sadoh, and M. Miyao, "Growth-Direction Dependent Rapid-Melting-Growth of Ge-On-Insulator (GOI) and its Application to Ge Mesh-Growth," *ECS Transactions*, vol. 35, pp. 55-60, 2011.
[182] G. Eneman, D. P. Brunco, L. Witters, B. Vincent, P. Favia, A. Hikavyy, A. De Keersgieter, J. Mitard, R. Loo, A. Veloso, O. Richard, H. Bender, S. H. Lee, M. Van Dal, N. Kabir, W. Vandervorst, M. Caymax, N. Horiguchi, N. Collaert, and A. Thean, "Stress simulations for optimal mobility group IV p- and nMOS FinFETs for the 14 nm node and beyond," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 6.5.1-6.5.4.
[183] J. Feng, R. Woo, S. Chen, Y. Liu, P. B. Griffin, and J. D. Plummer, "P-Channel Germanium FinFET Based on Rapid Melt Growth," *Electron Device Letters, IEEE*, vol. 28, pp. 637-639, 2007.
[184] L. Hutin, C. Le Royer, J.-F. Damlencourt, J. M. Hartmann, H. Grampeix, V. Mazzocchi, C. Tabone, B. Previtali, A. Pouydebasque, M. Vinet, and O. Faynot, "GeOI pMOSFETs Scaled Down to 30-nm Gate Length With Record Off-State Current," *Electron Device Letters, IEEE*, vol. 31, pp. 234-236, 2010.
[185] M. J. H. van Dal, G. Vellianitis, G. Doornbos, B. Duriez, T. M. Shen, C. C. Wu, R. Oxland, K. Bhuwalka, M. Holland, T. L. Lee, C. Wann, C. H. Hsieh, B. H. Lee, K. M. Yin, Z. Q. Wu, M. Passlack, and C. H. Diaz, "Demonstration of scaled Ge p-channel FinFETs integrated on Si," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 23.25.21-23.25.24.
[186] L. Bin, G. Xiao, Z. Chunlei, H. Genquan, C. Hock-Chun, L. Moh-Lung, L. Jie, L. Yongdong, H. Jiangtao, N. Daval, C. Veytizou, D. Delprat, N. Bich-Yen, and Y. Yee-Chia, "Germanium Multiple-Gate Field-Effect Transistors Formed on Germanium-on-Insulator Substrate," *Electron Devices, IEEE Transactions on*, vol. 60, pp. 1852-1860, 2013.

[187] K. Ikeda, M. Ono, D. Kosemura, K. Usuda, M. Oda, Y. Kamimuta, T. Irisawa, Y. Moriyama, A. Ogura, and T. Tezuka, "High-mobility and low-parasitic resistance characteristics in strained Ge nanowire pMOSFETs with metal source/drain structure formed by doping-free processes," in *VLSI Technology (VLSIT), 2012 Symposium on*, 2012, pp. 165-166.

[188] L. Bin, Z. Chunlei, Y. Yue, C. Ran, G. Pengfei, Z. Qian, E. Y. J. Kong, N. Daval, C. Veytizou, D. Delprat, N. Bich-Yen, and Y. Yee-Chia, "Germanium Multiple-Gate Field-Effect Transistor With In Situ Boron-Doped Raised Source/Drain," *Electron Devices, IEEE Transactions on*, vol. 60, pp. 2135-2141, 2013.

[189] C. Che-Wei, C. Cheng-Ting, T. Ju-Yuan, C. Pang-Sheng, L. Guang-Li, and C. Chao-Hsin, "Body-Tied Germanium Tri-Gate Junctionless PMOSFET With In-Situ Boron Doped Channel," *Electron Device Letters, IEEE*, vol. 35, pp. 12-14, 2014.

[190] A. Claverie, S. Koffel, N. Cherkashin, G. Benassayag, and P. Scheiblin, "Amorphization, recrystallization and end of range defects in germanium," *Thin Solid Films*, vol. 518, pp. 2307-2313, 2010.

[191] H. Ishiwara, H. Yamamoto, S. Furukawa, M. Tamura, and T. Tokuyama, "Lateral solid phase epitaxy of amorphous Si films on Si substrates with SiO2 patterns," *Applied Physics Letters*, vol. 43, pp. 1028-1030, 1983.

[192] M. Sasaki, T. Katoh, H. Onoda, and N. Hirashita, "Lateral solid phase epitaxy of Si over SiO2 patterns and its application to silicon-on-insulator transistors," *Applied Physics Letters*, vol. 49, pp. 397-399, 1986.

[193] R. Drosd and J. Washburn, "Some observations on the amorphous to crystalline transformation in silicon," *Journal of Applied Physics*, vol. 53, pp. 397-403, 1982.

[194] B. L. Darby, B. R. Yates, I. Martin-Bragado, J. L. Gomez-Selles, R. G. Elliman, and K. S. Jones, "Substrate orientation dependence on the solid phase epitaxial growth rate of Ge," *Journal of Applied Physics*, vol. 113, p. 033505, 2013.

[195] R. Duffy, M. Shayesteh, B. McCarthy, A. Blake, M. White, J. Scully, R. Yu, A.-M. Kelleher, M. Schmidt, N. Petkov, L. Pelaz, and L. A. Marqués, "The curious case of thin-body Ge crystallization," *Applied Physics Letters*, vol. 99, pp. 131910, 2011.

[196] E. Y. J. Kong, G. Pengfei, G. Xiao, L. Bin, and Y. Yee-Chia, "Toward Conformal Damage-Free Doping With Abrupt Ultrashallow Junction: Formation of Si Monolayers and Laser Anneal as a Novel Doping Technique for InGaAs nMOSFETs," *Electron Devices, IEEE Transactions on*, vol. 61, pp. 1039-1046, 2014.

[197] T. Maeda, Y. Morita, and S. Takagi, "High Electron Mobility Ge n-Channel Metal–Insulator–Semiconductor Field-Effect Transistors Fabricated by the Gate-Last Process with the Solid Source Diffusion Technique," *Applied Physics Express*, vol. 3, p. 061301, 2010.

[198] V. Dimastrodonato, L. O. Mereni, R. J. Young, and E. Pelucchi, "AlGaAs/GaAs/AlGaAs quantum wells as a sensitive tool for the MOVPE reactor environment," *Journal of Crystal Growth*, vol. 312, pp. 3057-3062, 2010.

[199] R. Duffy, M. Shayesteh, K. Thomas, E. Pelucchi, R. Yu, A. Gangnaik, Y. M. Georgiev, P. Carolan, N. Petkov, B. Long, and J. D. Holmes, "Access resistance reduction in Ge nanowires and substrates based on non-destructive gas-source dopant in-diffusion," *Journal of Materials Chemistry C*, vol. 2, pp. 9248-9257, 2014.

[200] A. N. Larsen, K. K. Larsen, P. E. Andersen, and B. G. Svensson, "Heavy doping effects in the diffusion of group IV and V impurities in silicon," *Journal of Applied Physics*, vol. 73, pp. 691-698, 1993.

[201] G. Hellings and K. De Meyer, "Source/Drain Junctions in Germanium: Experimental Investigation," in *High Mobility and Quantum Well Transistors*. vol. 42, ed: Springer Netherlands, 2013, pp. 7-26.

[202] V. I. Fistul, M. I. Iglitsyn, and E. M. Omel'yanovskii, "Mobility of Electrons in germanium strongly Doped with Arsenic," *Soviet Physics-Solid State*, vol. 4, p. 784, 1962.

[203] C. Steen, A. Martinez-Limia, P. Pichler, H. Ryssel, S. Paul, W. Lerch, L. Pei, G. Duscher, F. Severac, F. Cristiano, and W. Windl, "Distribution and segregation of arsenic at the SiO_2/Si interface," *Journal of Applied Physics*, vol. 104, p. 023518, 2008.

[204] R. Duffy, M. J. H. Van Dal, B. J. Pawlak, N. Collaert, L. Witters, R. Rooyackers, M. Kaiser, R. G. R. Weemaes, M. Jurczak, and R. Lander, "Improved fin width scaling in fully-depleted FinFETs by source-drain implant optimization," in *Solid-State Device Research Conference, ESSDERC 2008. 38th European*, 2008, pp. 334-337.

[205] G. Zschatzsch, Y. Sasaki, S. Hayashi, M. Togo, T. Chiarella, A. K. Kambham, J. Mody, B. Douhard, N. Horiguchi, B. Mizuno, M. Ogura, and W. Vandervorst, "High performance n-MOS finFET by damage-free, conformal extension doping," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 35.36.31-35.36.34.

[206] E. Tutuc, J. Appenzeller, M. C. Reuter, and S. Guha, "Realization of a Linear Germanium Nanowire p−n Junction," *Nano Letters*, vol. 6, pp. 2070-2074, 2006.

[207] H. Schmid, M. T. Björk, J. Knoch, S. Karg, H. Riel, and W. Riess, "Doping Limits of Grown in situ Doped Silicon Nanowires Using Phosphine," *Nano Letters*, vol. 9, pp. 173-177, 2008.