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Title	Effect of low temperature RF plasma treatment on electrical properties of junctionless InGaAs MOSFETs
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Publication date	2019-03-02
Original Citation	Gomeniuk, Y. V., Gomeniuk, Y. Y., Rudenko, T. E., Okholin, P. N., Glotov, V. I., Nazarova, T. M., Djara, V., Cherkaoui, K., Hurley, P. K. and Nazarov, A. N. (2019) 'Effect of low temperature RF plasma treatment on electrical properties of junctionless InGaAs MOSFETs', ECS Journal of Solid State Science and Technology, 8(2), pp. Q24-Q31. doi: 10.1149/2.0181902jss
Type of publication	Article (peer-reviewed)
Link to publisher's version	10.1149/2.0181902jss
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Download date	2026-11-06 23:19:20
Item downloaded from	https://hdl.handle.net/10468/10204



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Effect of Low Temperature RF Plasma Treatment on Electrical Properties of Junctionless InGaAs MOSFETs

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Abstract

In this paper, we study the effect of low-temperature RF plasma treatment in forming gas ($10\%H_2+90\%N_2$) on the electrical characteristics of junctionless MOSFETs with *n*-$In_{0.53}Ga_{0.47}As$ channel and an Al_2O_3 gate dielectric. The impact of plasma power density on the device parameters is investigated. It is found that RF plasma annealing with a low power density (0.5 W/cm^2) at 150°C for 10 min provides substantial improvement of source/drain contacts resistance and the carrier mobility resulting in a considerable increase of the on-state current and transconductance. It also improves the subthreshold slope and reduces the fixed positive charge in Al_2O_3 under the gate, shifting the threshold voltage towards positive values. It is demonstrated that non-thermal factors play a principle role in modification of electrical properties of the JL MOSFETs under RF plasma treatment. Such treatment may be an efficient tool for the improvement of the performance of the advanced MOSFETs with III-V channel materials.

This was Paper 1464 presented at the Seattle, Washington Meeting of the Society, May 13-17, 2018.

Introduction

The junctionless (JL) device concept for silicon-on-insulator MOSFETs was introduced by Colinge et al. in 2010,[1] demonstrating considerable gains in terms of process simplicity when compared to conventional inversion-mode MOSFETs. The JL device architecture is particularly well suited to III-V channel materials. Firstly, a high body doping concentration (N_d), being the key requirement for JL MOSFETs, is less problematic for $In_{0.53}Ga_{0.47}As$ than it is for Si. Indeed, the bulk electron mobility in Si is ≤100 cm^2/V·s at $N_d = 1\times10^{19}$ cm^{-3},[2] while in $In_{0.53}Ga_{0.47}As$ the bulk mobility is ~2500 cm^2/V·s at a similar N_d level.[3] Moreover, the JL architecture allows to obviate the difficulties associated with implantation[4,5] or regrowth techniques[6] generally used to form the source/drain (S/D) regions of III-V inversion-mode MOSFETs and to improve the thermal budget. Recently, tri-gate JL MOSFETs with the InGaAs channel have been demonstrated.[7,8] A major concern for these devices is found to be a high S/D resistance (R_{SD}). The formation of good Ohmic S/D contacts requires device annealing at temperatures ≥300°C that could lead to unintentional diffusion of In atoms into the gate dielectric. In this work, low-temperature RF plasma

treatment (RFPT)[9] is proposed to form S/D contacts and improve the performance of JL $In_{0.53}Ga_{0.47}As$ MOSFETs. In our previous publications it has been shown that RF plasma treatment is efficient in reducing the density of fixed positive charges in SiO_2 layers and interface traps at the Si-SiO_2 interface,[9-11] annealing radiation-induced and ion implantation defects in metal-insulator-semiconductor (MIS) structures,[12,13] structural ordering and recrystallization of thin amorphous semiconductor layers,[14,15] low-temperature activation of implanted doping impurities in Si and Ge.[15-17] In this paper, we report that low-temperature RF plasma treatment in forming gas (10%H_2+90%N_2) can significantly improve the electrical characteristics of *n*-$In_{0.53}Ga_{0.47}As$ JL MOSFETs with an Al_2O_3 gate dielectric. In particular, it provides substantial reduction of S/D resistances, an increase of the electron mobility, resulting in the strong increase of the on-state current and transconductance, reduction of the effective positive charge in the Al_2O_3 gate dielectric, and improvement of the subthreshold slope.

Experimental

A structure consisting of a highly Si-doped ($N_d = 2\times10^{18}$ cm^{-3}) 32-nm-thick *n*-$In_{0.53}Ga_{0.47}As$ layer on a 500-nm-thick Zn-doped *p*-$In_{0.52}Al_{0.48}As$ ($N_a = 8\times10^{15}$ cm^{-3}) barrier was grown by metal organic vapour-phase epitaxy (MOVPE) on a p^+-InP wafer. Schematic representation and transmission electron microscopy image of the resulting heterostructure is illustrated in Figure 1 (a). In order to form a channel for the JL devices, the $In_{0.53}Ga_{0.47}As$ layer was thinned using a 10% H_2O_2/10% HCl digital wet etching process to achieve channel thickness of 20 nm. A gate enclosed device layout was employed to simplify the fabrication process flow. The main steps of the $In_{0.53}Ga_{0.47}As$ junctionless *n*-MOSFET fabrication process are illustrated in Figures 1(b-e)). A surface passivation in 10% $(NH_4)_2S$ for 30 min[18] was performed before atomic layer deposition (ALD) of an 8.5-nm-thick Al_2O_3 gate oxide. A Pd gate was formed by e-beam evaporation and lift-off. No S/D implantation and no selective epitaxial growth were used to reduce the S/D resistance. The Al_2O_3 on the S/D contact areas was etched in dilute HF. The S/D contact formation was carried out by e-beam evaporation of a Au/Ge/Au/Ni/Au stack and lift-off.

The samples used in this study were not subjected to any post-fabrication thermal anneal; instead the fabricated samples were exposed to the RF (13.6 MHz) plasma treatment in forming gas (10% H_2 + 90% N_2) during 10 min with additional heating of the sample holder to 150°C. Plasma power density was varied from 0.5 to 1.75 W/cm^2. Temperature of the samples during RF plasma treatment did not exceed 250°C.[9] In order to distinguish between thermal and non-thermal effects of the RFPT in some cases the treatment was performed in the same process for two chips - one from the side of metal electrodes (top side) and another from the side of p^+-InP substrate (back side).

Figure 2 (a) shows a schematic view of the gate-enclosed junctionless MOSFET architecture, where r_g, r_s, r_g^{in} and r_g^{out} are the drain, source, gate inner and gate outer radii, respectively. The MOSFETs being investigated had the gate length $L_g=r_g^{out}-r_g^{in}$ of 40, 60 and 80 μm with a 10-μm separation between the gate and source and drain contact pads. The devices with large L_g values were used for avoiding short-channel effects when investigating the impact of RF plasma treatment on the electrical properties of InGaAs JL MOSFETs.

Layout of the circular transmission line (CTL)[19] which was used for measurements of sheet resistance of *n*-$In_{0.53}Ga_{0.47}As$ layer and of specific contact resistance of S/D contacts is shown in Figure 2 (b). Current-voltage (*I-V*) characteristics of JL MOSFETs and CTL were measured by Agilent 4156C precision semiconductor parameter analyzer. Most measurements were performed with grounded outer electrode and electrically isolated (floating) substrate to avoid a parasitic effect of a leakage current through the buried *p-n* junction. This regime corresponds to zero current through the substrate. In some cases, to determine properties of the buried *p-n* junction and the effect of plasma treatment, the substrate was grounded.

Results and Discussion

Effect of RF plasma treatment on sheet resistance and specific contact resistance. - The specific contact resistance, ρ_c, is the parameter used to characterize metal/semiconductor interface, which is independent on the geometry of the contact. Measurements of the specific contact resistance and sheet resistance of the semiconductor film were carried out using simplified two-contact CTL technique.[19-21] Test structures consisted of inner circular contact pads with radius *r* of 100 μm separated from the surrounding outer contact of larger area with different gap spacings *d* of 16, 24, 32, 40, 48, 64, 80 and 96 μm (see Figure 2 (b)). The outer radius of semiconductor film ring not covered by metallization is then $R = r + d$. The total resistance between two contacts separated by a circular gap is given by:[22]

$$R_t = \frac{R_{sh}}{2\pi} \times \left[\ln\left(\frac{R}{r}\right) + L_t\left(\frac{1}{R} + \frac{1}{r}\right)\right], \qquad (1)$$

where R_{sh} is the sheet resistance of the semiconductor film, *r* and *R* represent the radius of the inner and outer contacts, respectively, and L_t is the transfer length. The total resistance measured for different spacing is plotted as function of $\ln(R/r)$ and approximated by a straight line. The slope of this line is equal to $R_{sh}/2\pi$, and the intercept with the Y axis at $\ln(R/r)=0$ is $R_{sh} \cdot L_t/\pi r$, giving L_t. Then the specific contact resistance, ρ_c, can be found from the equation:

$$L_t = \sqrt{\frac{\rho_c}{R_{sh}}} \qquad (2)$$

First we checked an absence of the possible effect of the buried *p-n* junction degradation, which may occur after the plasma treatment, on the measurement results. I_{sub}-*V* characteristic of the buried *p-n* junction (where I_{sub} is the current through the *p-n* junction into the substrate) was measured together with *I-V* characteristic of the element of CTL. The circuit diagram of the measurements is presented in Figure 3 (a). When the substrate and the outer electrode of CTL (see Figures 2 (b) and 3 (a)) are grounded a good rectifying I_{sub}-*V* characteristic is observed (Figure 3 (b)). I_{sub} current through the buried *p-n* junction is several orders of magnitude smaller than the measured current between contacts of CTL almost in the whole voltage range, and the *I-V* characteristics of CTL with grounded substrate and electrically isolated substrate match exactly in the range of the inner contact voltage from -0.5V to +1 V (Figure 3 (b), inset). The total resistance of the structure was determined in the range with minimum leakage current where *I-V* characteristics for grounded and isolated substrate

electrode coincide. In this case the error in determination of the film and contact resistance has to be rather small.

Figures 4 (a)-(c) show the current-voltage characteristics measured on CTL structures with different spacing and electrically isolated substrate before and after RFPT for the 20 nm InGaAs film. It can be seen in Figure 4 (a) that *I-V* characteristics of the initial sample are strongly non-linear due to presence of a rectifying barrier between metal and semiconductor after metallization. The strong asymmetry of the *I-V* curves is due to different areas of the two contacts. At positive voltage the current is limited by the higher resistance of the reverse connected diode of the small inner contact, and is substantially lower than at negative voltage of the same magnitude, when the limiting contact has much larger area and, respectively, lower resistance. In the case of non-linear current-voltage characteristics we determined for further evaluations the resistance of the test structure as a reciprocal of the maximum differential conductance (d*I*/d*V*). After RF plasma annealing from top side with power density of 0.5 W/cm^2 at 150°C the current-voltage characteristics (Figure 4(b)) become absolutely linear reflecting the conversion of the rectifying contacts into Ohmic ones. After RF plasma annealing from back side at the same treatment regime the level of currents is approximately the same as in the initial sample and the contacts remain evidently non-Ohmic (Figure 4 (c)). Figure 4 (d) illustrates the procedure of extracting of sheet resistance and contact resistivity from the CTL measurements. The slope of the approximating straight line leads to R_{sh}, and from the intercept the value of the specific contact resistivity ρ_c can be determined. One can see that after RFPT from top side with plasma power density of 0.5 W/cm^2 both sheet resistance and contact resistance are reduced dramatically. Sheet resistance of the 20-nm-thick film reduces from ≈330 kΩ/sq to about 2 kΩ/sq after RFPT at 0.5 W/cm^2. Specific contact resistivity also falls by more than two orders of magnitude after such treatment. After the RFPT from back side the contact resistivity and sheet resistance are changed insignificantly.

Comparison of the results obtained after RFPT of the structures treated from top side and back side indicates that strong non-thermal effects occur during the plasma treatment from top side. Indeed at top-side RFPT the following factors affect subsurface layers of the structure[9]: thermal heating; low-energy ion and electron bombardment; x-ray and UV irradiation combining with alternating RF electric field; protons as catalyst of defect transformation. Under RF plasma treatment from the back side, the main factors that influence the studied layers are temperature, soft x-ray irradiation, and alternating electric field. Thus, a decrease of specific contact resistivity after RFPT from top side is probably attributable to low-energy ion and electron bombardment of the multilayer contact structure during plasma exposure, resulting in the formation of Ohmic contacts due to reduction of the potential barrier at the metal/semiconductor interface. It should be noted that Schottky barrier height reduction on n-GaAs at low-energy ion bombardment was previously observed by a number of authors.[23-25]

Reduction of the sheet resistance of uncoated *n*-InGaAs film under N_2/H_2 plasma exposure from top side can be attributed to surface nitridation, resulting in suppression of Ga oxides and As oxides and formation of Ga-N bonds at the surface, which strongly reduces the interface trap density,[26,27] and hydrogen passivation of bulk and surface defects.[25,28-31] However, hydrogen in III-V semiconductors also is known to passivate (or deactivate) shallow dopants, specifically Si, which reduces the free carrier concentration in the semiconductor layer.[25,28-30] The latter effect is temperature-dependent and reversible, since a temperature increase brings

about the dopant reactivation.[25,28-30] This allows explaining the hump on the dependence of the sheet resistance on the plasma power density (see Figure 5). Figure 5 illustrates also the variation of specific contact resistivity with the RF plasma power density. Specific contact resistivity reaches the lowest values at plasma power density 0.75 W/cm^2 and increases with further increasing power density, which can be attributed to the ion bombardment damage.

Effect of RF plasma treatment on transfer characteristics of JL MOSFETs n-InGaAs channel and ALD Al_2O_3 gate dielectric. - Figure 6 shows drain current (I_d) versus gate voltage (V_g) transfer characteristics measured as the drain voltage (V_d) varied from 10 mV to 50 mV on the 40-μm-gate-length *n*-InGaAs JL MOSFET before and after RF plasma treatment at a low plasma power density P=0.5 W/cm^2. The drain current values in Figure 6 are normalized to the effective gate width-to-length ratio, $(W/L)_{eff}$, which for a gate-enclosed transistor with annular gate is expressed as:[32]

$$\left(\frac{W}{L}\right)_{eff} = \frac{2\pi}{\ln\left(r_g^{out} / r_g^{in}\right)}, \qquad (3)$$

where r_g^{out} and r_g^{in} are gate outer and gate inner radii, respectively.

As is seen from Figure 6, RF plasma treatment from top side results in the shift of the $I_d(V_g)$ - characteristics towards positive values, which is indicative of the reduction of the fixed positive charge in the gate dielectric. The threshold voltage (V_{th}) evaluated by the second derivative method[33] before and after plasma treatment at the plasma power density of 0.5 W/cm^2 is, respectively, -0.49 V and 0.05 V. This V_{th} shift is attributable to the reduction of an equivalent density of fixed positive oxide charge at the Al_2O_3/ *n*-$In_{0.53}Ga_{0.47}As$ interface in the gated area by ~2.8×10^{12} /cm^2. The reduction of positive charge is consistent with what is observed with a standard forming gas anneal in a 5% H_2 / 95% N_2 ambient at 350 °C for 30 minutes.[34] Another consequence of RF plasma treatment is a decrease of the inverse subthreshold slope (*SS*) from 190 mV/dec to 150 mV/dec, which can be attributed to the reduction of the interface trap density (D_{it}) from ~1.1×10^{13} /cm^2·eV to 7.5×10^{12}/cm^2·eV. However, the most remarkable result of RF plasma treatment is significant increase (approximately by two orders of magnitude) of the on-state current, I_{ON}, which is evidently related to reduction of the S/D contact series resistance, since initial samples were not subjected to any post-metallization processing and RF plasma was used for contact annealing. The on-to-off current ratio (I_{ON}/I_{OFF}) after plasma annealing at the plasma power density P=0.5 W/cm^2 is ≈1.7×10^5.

It is worth to note that RFPT from back side does not increase the I_{ON}/I_{OFF} ratio in comparison with the initial device and even slightly deteriorates the subthreshold slope (see Figure 6). The first effect is due to the absence of reduction of the S/D contact series resistance; and the second one reflects the increase of the interface trap density and/or of surface potential fluctuations. At the same time the shift of the $I_d(V_g)$ - characteristic (about 0.45V) towards positive values is observed as a result of reduction of fixed positive oxide charge in the Al_2O_3 gate dielectric. The value of the shift is similar (a bit smaller) to that after RFPT from top side, and it is possible to conclude that in this case the same mechanisms of charge annealing can

take place. As it was mentioned before the main factors affecting the gate dielectric and InGaAs film at RF plasma treatment from back side are temperature, RF electric field and soft x-ray irradiation. Combination of the last two factors results in strong electron and hole injection from the semiconductor and from the metal gate into the gate dielectric leading to recombination-enhanced processes of fixed positive change neutralization and defects annealing in the dielectric.[35]

Figures 7(a)-(c) illustrate the impact of the plasma power density on the threshold voltage shift ΔV_{th}, the inverse subthreshold slope *SS*, as well as the on-current and on-to-off current ratio. on the plasma power density. It can be seen that the threshold voltage shift tends to increase with power density (Figure 7(a)). Increasing the plasma power density from 0.5 W/cm^2 to 1.75 W/cm^2 has only a minor effect on *SS* (Figure 7(b)), however, it strongly decreases I_{ON} and I_{ON}/I_{OFF} ratio (Figure 7(c)), which can be explained by both degradation of the mobility and an increase of the parasitic S/D resistance.

Effect of RF plasma treatment on electron mobility and source-drain series resistance in InGaAs JL MOSFETs. **-** The carrier mobility was evaluated using the Y-function methodology and the split *C-V* method. According to the approach developed in[36] for heavily doped Si layers, the drain current in JL MOSFET in volume conduction region with considering the parasitic S/D resistance, R_{SD}, can be written as:

$$I_d = \frac{W}{L} \cdot C_{ox} \cdot \frac{\mu_{vol}}{1+\theta_1\left(V_g - V_0\right)} \cdot \left(V_g - V_0\right) \cdot V_d , \qquad (4)$$

where W and L are the gate width and length, respectively, C_{ox} is the gate dielectric capacitance, μ_{vol} is the carrier mobility in the volume of the semiconductor layer assumed to be uniform across the film thickness, V_g is the gate voltage, V_0 is a characteristic gate voltage, which provides full depletion of the film, V_d is the drain voltage, and θ_1 is the coefficient considering R_{SD}:

$$\theta_1 = R_{SD} \cdot \mu_{vol} \cdot C_{ox} \cdot \frac{W}{L} \ . \qquad (5)$$

From (4) one can obtain:

$$Y_{vol} = \frac{I_d}{\sqrt{g_m\left(V_g\right)}} = \sqrt{\frac{W}{L} \cdot C_{ox} \cdot \mu_{vol} \cdot V_d} \cdot \left(V_g - V_0\right), \qquad (6)$$

where the effect of R_{SD} is eliminated. From (6) it follows that the slope of the $Y_{vol}(V_g)$ dependence yields the value of μ_{vol} being unaffected by the S/D series resistance. Thus the procedure for the extraction of μ_{vol} in JL MOSFETs is similar to that in the conventional Y-function technique used for extracting low-field mobility, μ_0, in inversion-mode MOSFETs.[37] The S/D series resistance R_{SD} is involved in the coefficient θ_1, which is obtainable from the slope of $1/\sqrt{g_m}$ versus V_g dependence:[38]

$$\frac{1}{\sqrt{g_m(V_g)}} = \frac{1+\theta_1\cdot(V_g - V_0)}{\sqrt{C_{ox}\cdot\frac{W}{L}\cdot\mu_{vol}\cdot V_d}}. \qquad (7)$$

In the case of the transistor with annular gate, the ratio W/L in equations (4)-(7) should be replaced by the effective gate width-to-length ratio $(W/L)_{eff}$ given by eq. (3).

Since the physical meaning of the threshold voltage in JL MOSFETs is the transition from the full depletion regime to partially depletion regime, we can consider $V_0 \approx V_{th}$. The range of V_g corresponding to volume conduction regime in JL MOSFETs (between the threshold voltage V_{th} and flat band voltage V_{FB}) is usually identified from the positions of the two peaks of the second derivative of the drain current versus gate voltage characteristics, d^2I_d/dV_g^2.[39] However, in the case of relatively high series resistance, the second peak in the d^2I_d/dV_g^2 curves, associated with the transition to the surface accumulation regime, is not pronounced,[40] as in our case. The V_g range corresponding to volume conduction can be estimated as follows:

$$\Delta V_g = V_{FB} - V_{th} \approx \frac{q\cdot N_d\cdot t_{InGaAs}^2}{2\cdot\varepsilon_{InGaAs}} + \frac{q\cdot N_d\cdot t_{InGaAs}}{C_{ox}}, \qquad (8)$$

which for our device parameters is ≈0.8 V.

Figure 8(a) shows $Y_{vol} = I_d / \sqrt{g_m}$ versus gate voltage overdrive (V_g-V_{th}) obtained at V_d=50 mV on the 40-μm-gate-length JL MOSFETs before and after RF plasma treatment with various plasma power densities. It is clearly seen that plasma annealing, especially at a low power density, results in the strong increase of the slope of the linear region of the Y-function compared to that for the initial sample, suggesting that RF plasma treatment increases the carrier mobility in the $In_{0.53}Ga_{0.47}As$ film. The extracted mobility values obtained for the initial sample and after RF plasma treatment with different plasma power densities are presented in Figure 8(b). The value of μ_{vol} obtained for the initial sample is ≈90 cm^2/V·s, whereas after plasma annealing with a low plasma power density (P=0.5 ÷ 1 W/cm^2) it is ≈1300 cm^2/V·s. This is attributable to RF plasma-assisted annealing of bulk and surface defects in the $In_{0.53}Ga_{0.47}As$ film, due to a cooperative effect of the RF field, the X-ray radiation, and the induced wafer temperature, resulting in the recombination-enhanced defect reactions in metal-insulator-semiconductor structures.[35,40] An increase of the plasma power density from 1.25 W/cm^2 to 1.5 W/cm^2 results in the significant mobility degradation, which is explainable by the creation of new defects (Figure 8 b), resulting from the increase of the intensity of X-ray and UV radiation accompanying RFPT.[35]

Plotted in Figure 9(a) are $1/\sqrt{g_m}$ versus ($V_g - V_{th}$) characteristics obtained on the InGaAs JL MOSFETs with L_g=40 μm before and after RF plasma treatment at two different plasma power densities, 0.5 W/cm^2 and 1 W/cm^2. Larger slope of the $1/\sqrt{g_m}$ curve above V_{th} for the initial sample suggests larger S/D series resistance. The obtained results for R_{SD} in the initial

sample and after RF plasma treatment at different plasma power densities are presented in Figure 9(b). As follows from Figure 9(b), plasma treatment at P=0.5 W/cm^2 results in the considerable (by two orders of magnitude) reduction of R_{SD}, namely, from 14.4 kΩ in the initial sample to 140 Ω after RF plasma anneal, which agrees well with results for the contact resistance. It should be noted that in the devices with a given geometry the source/drain parasitic resistance R_{SD} is determined not only by the contact resistance, but also it includes the resistance of the n-$In_{0.53}Ga_{0.47}As$ film outside of the Pd gate between the gate and source and drain regions (see Figure 2). Therefore, one would expect that the treatment, which reduces the fixed positive charge in Al_2O_3, can increase R_{SD} and thereby reduce I_{ON} due to a decrease or removal of accumulation in the non-gated regions of the n-$In_{0.53}Ga_{0.47}As$ film, as it was observed in the case of H_2/N_2 thermal anneal reported in Ref. 42. However, the effect of RF plasma is most likely not the same for the insulator/semiconductor systems with and without metal gate.

An increase of the plasma power density from 0.5 W/cm^2 to 1.25 W/cm^2 results in the gradual increase of R_{SD}; further increase of plasma power sharply increases R_{SD}. This can be explained by the defect formation in the InGaAs film with an increase of the energy of incident bombarding ions.

Using combined drain current and gate-to-channel capacitance (C_{gc}) versus V_g measurements, we evaluated the effective electron mobility for plasma power density of 0.5 W/cm^2, which provides the best results in terms of I_{ON}, μ_{vol} and R_{SD}. The extraction of the effective electron mobility (μ_{eff}) was performed on the test MOSFETs with channel length of 100 and 150 μm. The C_{gc}-V_g characteristic used for the extraction of μ_{eff} is shown in Figure 10(a). Resulting μ_{eff} is presented in Figure 10(b) as a function of the average carrier concentration N_{aver} in the $In_{0.53}Ga_{0.47}As$ film, where N_{aver} was obtained by dividing the total carrier density N_{tot} by the film thickness, $N_{aver}= N_{tot} /t_{InGasAs}$, and N_{tot} was obtained by integrating the measured $C_{gc}(V_g)$ curve. Using a value of a flat-band capacitance (C_{FB}) of 0.61 μF/cm^2, obtained from Poisson-Schrödinger simulations, we extracted for a given plasma power density a flat-band voltage V_{FB} of 0.71 V and electrically active doping concentration in the $In_{0.53}Ga_{0.47}As$ film (N_d) of 1.3×10^{18}/cm^3 (Figure 10(a)). As is seen from Figure 10(b), the maximum value of μ_{eff} for a given plasma power density is ≈1500 cm^2/V·s, whereas at flat-band conditions it is ≈1430 cm^2/V·s. The obtained results for μ_{eff} agree well with the corresponding μ_{vol} value extracted by the Y-function method.

Conclusions

In summary, we investigated the effects of the RF plasma treatment in the forming gas (10%H_2+90%N_2) on the characteristics of $In_{0.53}Ga_{0.47}As$ channel MOS transistors with an Al_2O_3 gate dielectric and having a junctionless layout. We have demonstrated that RF plasma treatment at 150-200°C for 10 min with a low power density (~0.5 W/cm^2) allows one to anneal effectively the source/drain contacts to the InGaAs film decreasing the contact resistance by more than two orders of magnitude without degradation of buried p-n junction. Moreover, RF plasma treatment provides strong enhancement of the carrier mobility in the $In_{0.53}Ga_{0.47}As$ film, which together with reduction of the source/drain resistance results in the dramatic increase of the on-current. It was found also that RFPT reduces the built-in positive charge in the dielectric layer shifting the threshold voltage to positive values. It was

demonstrated that non-thermal factors play a principle role in modification of electrical properties of the JL MOSFETs under RFPT. RF plasma treatment was proven to be an effective technique for formation of source/drain contacts and for improvement of the performance of the $In_{0.53}Ga_{0.47}As$ JL MOSFETs, and more generally could be applicable to reduction of source/drain resistance in 3D sequential integration.

Acknowledgments

The authors acknowledge the financial support of the EU Horizon 2020 programme, through the project ASCENT (grant agreement 654384), and of Science Foundation Ireland through the project INVEST (15/IA/3131).

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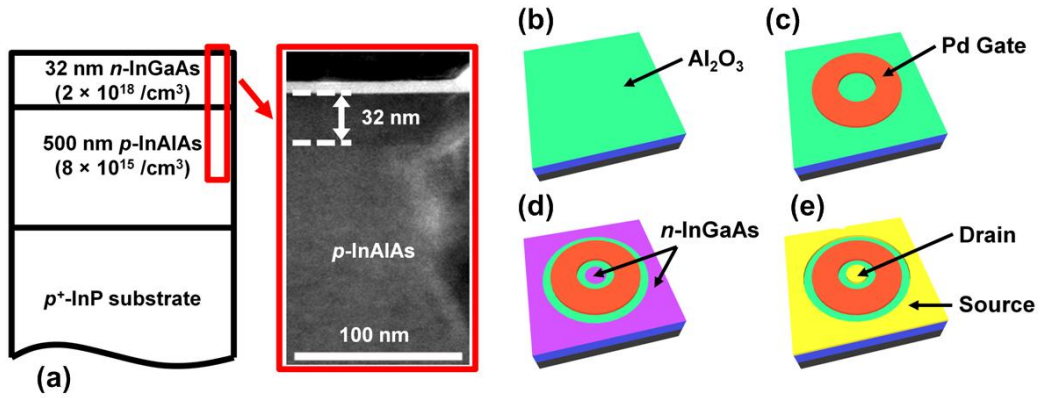


Figure 1. (a) Cross-section schematic and transmission electron microscopy image of the MOVPE grown *n*-$In_{0.53}Ga_{0.47}As$ (32 nm)/*p*-$In_{0.52}Al_{0.48}As$ (500 nm)/p^+-InP wafer structure. The $In_{0.53}Ga_{0.47}As$ Junctionless *n*-MOSFET fabrication process flow including (b) $(NH_4)_2S$ passivation and atomic-layer deposition of Al_2O_3, (c) Pd gate lift-off, (d) S/D contact opening and (e) NH_4OH treatment and S/D contact formation and lift-off.

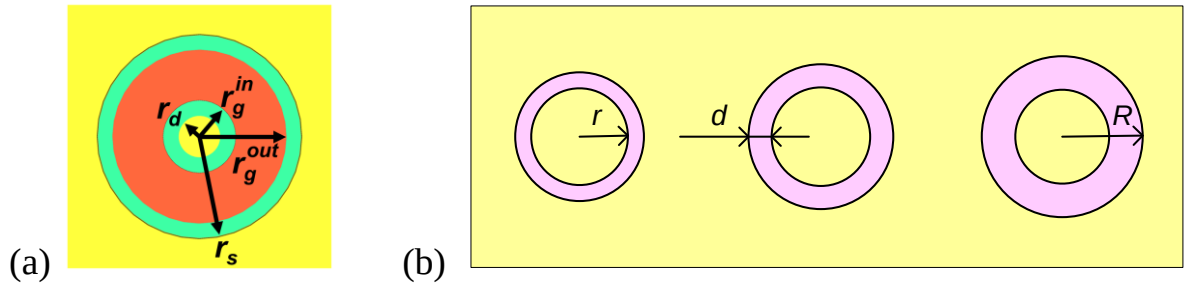


Figure 2. (a) Schematic representation of a gate-enclosed junctionless MOSFET architecture, where r_d, r_s, r_g^{in}, and r_g^{out} are the drain, source, gate inner and gate outer radii, respectively. (b) Layout of circular transmission line, r=100 μm, d varies from 16 to 96 μm.

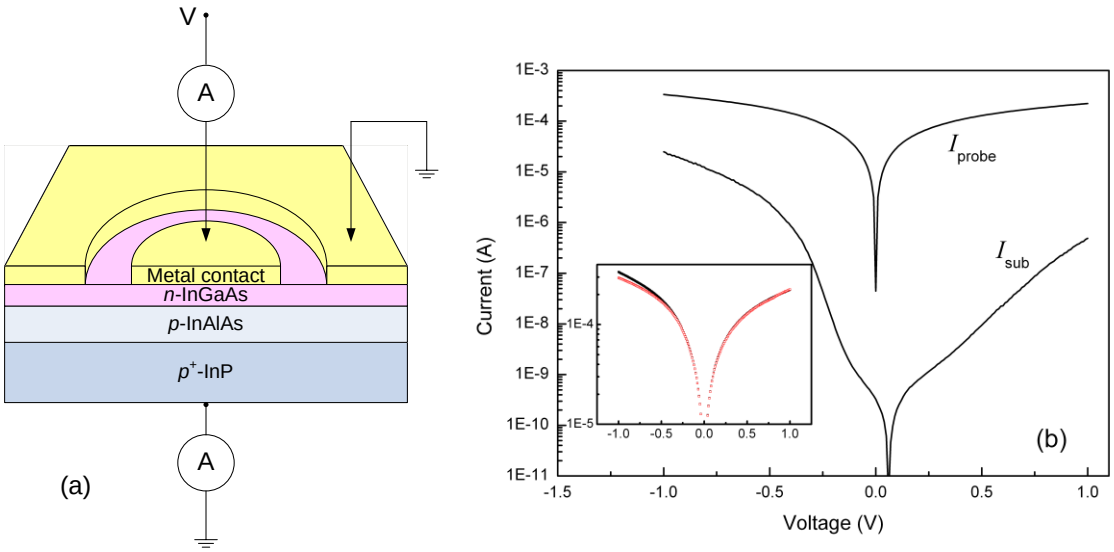


Figure 3. (a) Circuit diagram of CTL measurements. (b) *I-V* characteristics between metal contacts (I_{probe}) and between the central contact and the substrate (I_{sub}). Inset shows in larger scale I_{probe} measured with grounded (black dots) and isolated (red dots) substrate.

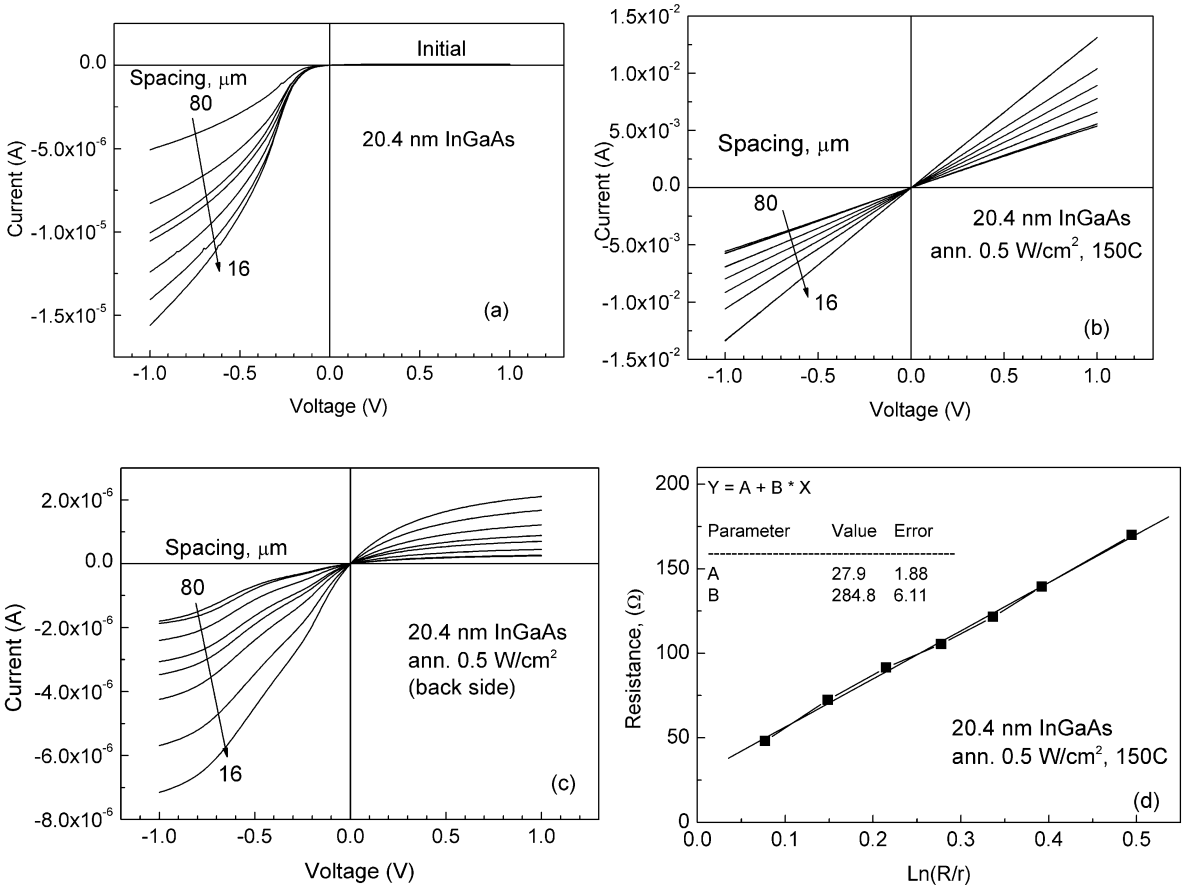


Figure 4. *I-V* characteristics of circular contacts in CTL before treatment (a), after RF plasma treatment (0.5 W/cm^2; 150°C; 10 min) from top side (b) and after RFPT from back side (c). (d) Plot of total resistance vs. ln(*R*/*r*) after RFPT.

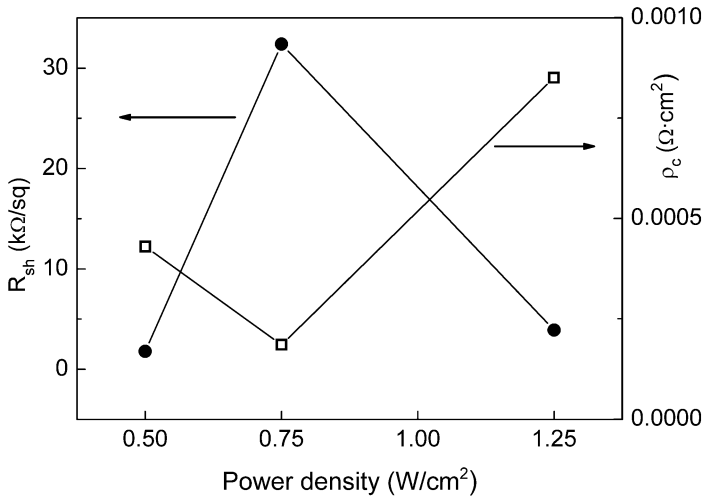


Figure 5. Dependence of the sheet resistance of the InGaAs film (dots) and specific contact resistance (open squares) on plasma power density.

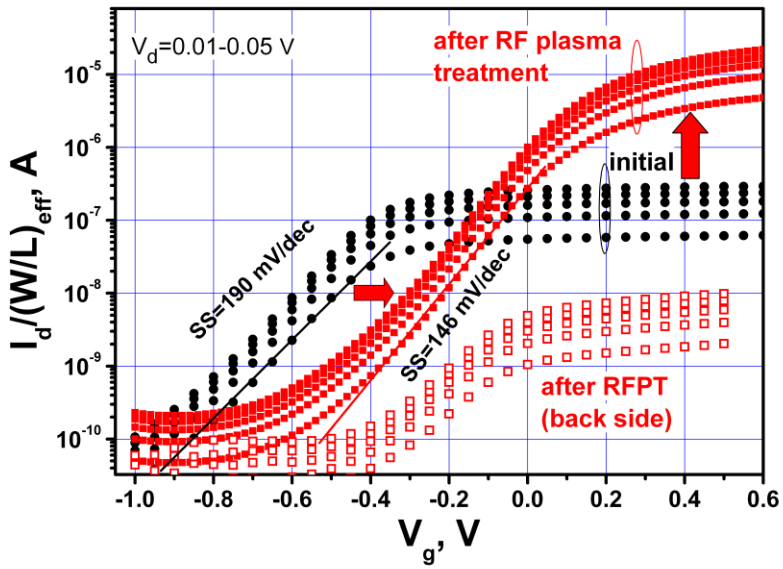


Figure 6. Transfer (I_d -V_g) characteristics measured at different values of V_d varied from 10 mV to 50 mV on the 40-μm-gate-length *n*-InGaAs JL MOSFET before and after RF plasma treatment with plasma power density P=0.5 W/cm^2.

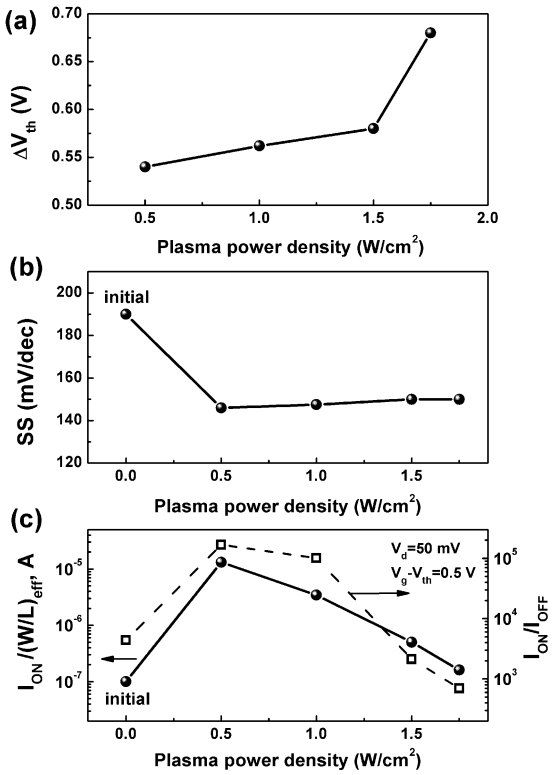


Figure 7. The threshold voltage shift ΔV_{th} (a), the inverse subthreshold slope *SS* (b), and the on-current I_{ON} and on-to-off current ratio I_{ON}/I_{OFF} (c) as a function of the RF plasma power density in $In_{0.53}Ga_{0.47}As$ JL MOSFETs (L_g=40 μm, V_d=50 mV). The data in Figure 6(c) are obtained at V_g-V_{th}=0.5 V, where V_{th} values are evaluated by the second derivative drain current method.

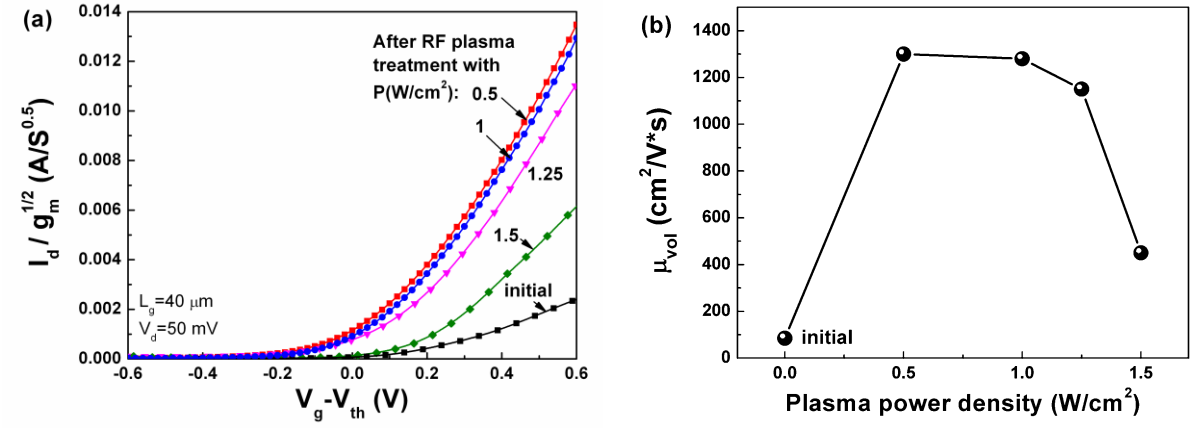


Figure 8. (a) Y-function plotted versus gate voltage overdrive in the range of volume conduction obtained at V_d=50 mV on $In_{0.53}Ga_{0.47}As$ JL MOSFETs (L_g=40 μm) before and after RF plasma treatment with various plasma power densities and (b) the extracted carrier mobility μ_{vol} as a function of RF plasma power density

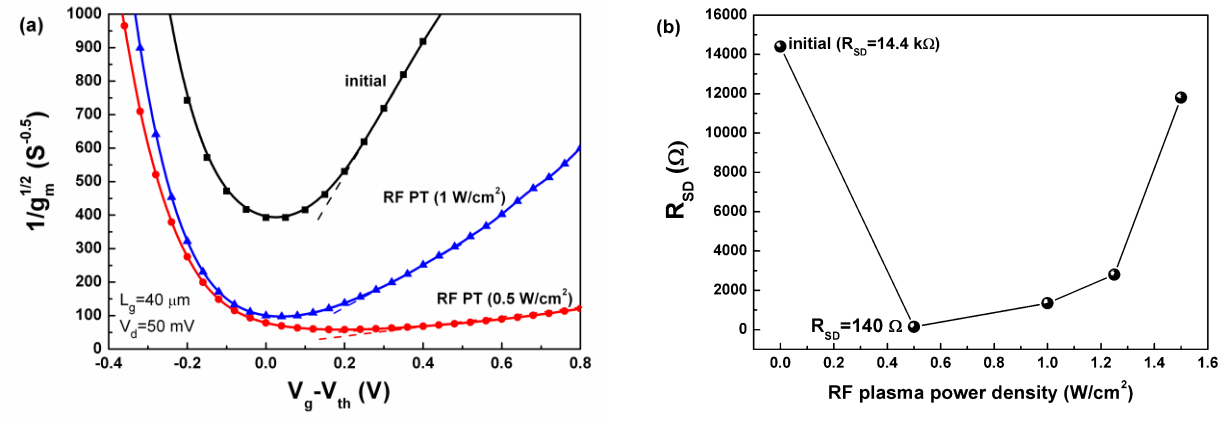


Figure 9. (a) $1/\sqrt{g_m}$ versus gate voltage overdrive obtained on $In_{0.53}Ga_{0.47}As$ JL MOSFETs before and after RF plasma treatment with plasma power densities of 0.5 W/cm^2 and 1 W/cm^2 (L_g=40 μm, V_d=50 mV); (b) the extracted source/drain series resistance R_{SD} as a function of RF plasma power density.

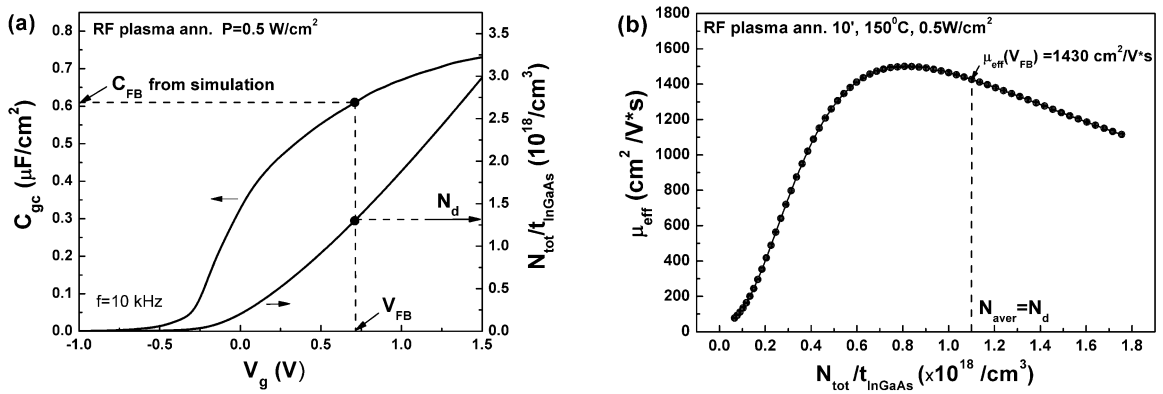


Figure 10. (a) The C_{gc}-V_g characteristic measured at f=10 kHz in the JL $In_{0.53}Ga_{0.47}As$ MOSFET after RF plasma treatment with P=0.5 W/cm^2 (left axis), and the average electron concentration in the $In_{0.53}Ga_{0.47}As$ film obtained by integrating the C_{gc}-V_g curve and dividing by the film thickness (right axis). (b) The effective electron mobility μ_{eff} versus the average electron concentration in the $In_{0.53}Ga_{0.47}As$ film.