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Monolayer doping of bulk and thin body Group IV semiconductors

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Declaration

This is to certify that this is my own work and has not been submitted for another degree at University College Cork or elsewhere. All references are acknowledged in the contents of the text. I have read and understood the terms and conditions outlined by University College Cork with regards to plagiarism.

Michael Noel Kennedy

ABSTRACT

The turn of the new year from 2019-2020 has brought us into a new decade with an unforeseen worldwide halt to what was previously considered “normal” life, due to a virus (coronavirus-19) with dimensions measured by scanning electron microscopy (SEM) to be in the nanometre range. This has emphasized the importance for the general public of acknowledging particles and materials in this nanometre range which cannot be seen without electron microscopy. Some of the technology being used to fight these viruses, such as ventilators, operate using electronics which contain semiconductor materials. Since the mid 1900 s the size of these electronics has decreased while doubling their quantity of transistors in line with Moore’s law. This has allowed for increased performance with lower power consumption. Scaling of metal-oxide-semiconductor field effect transistors (MOSFETs) has progressed from the original micrometre range to current sub-10 nm dimensions, while also moving from planar to 3-dimensional (3-D) architectures. However, increasing difficulty has been found with these new and reduced material dimensions. All fabrication processes are stressed, but doping has particularly found limitations in this region. High concentrations of dopant atoms are required at increasingly shallow depths, while maintaining the crystalline integrity of the planar or 3-D doped substrate. Traditional methods of introducing these dopant atoms, such as ion implantation, have found difficulty with damage production and conformality on state-of-the-art applications. Monolayer doping, which is a method of semiconductor doping through chemical functionalisation of the target substrate with the required dopant-containing molecules, has shown promise as an alternative method for this state-of-the-art doping.

The aim of this thesis is to study the potential of monolayer doping for application to materials used in current and future transistor devices.

Chapter 1 acts as an introduction to the work which is discussed in this thesis. A brief history of transistor development is outlined to give context to the main application where MLD has been proposed as a solution. The use of transistors in every day electronic devices and their continued development towards smaller sizes and improved power and performance has led to the requirement for alternative doping methodologies. The traditional technique for doping, beam-line implantation is discussed with its issues on current device sizes and architectures outlined. Alternative doping methods such as plasma doping, and in-situ doping are also discussed with both the positives and negatives associated with each technique outlined. MLD has been proposed as a novel alternative with potential to conformally dope these nanostructures with no crystalline damage. The advantages of MLD are outlined with a detailed discussion on how the technique has developed since its inception in 2008. A number of limitations do remain when considering MLD as a viable industry alternative to more traditional doping techniques. These limitations are discussed and are addressed by the work later described in chapters 3-6. A number of fundamental properties associated with diffusion doping are also described which are necessary for a complete understanding of the work described in this text.

Chapter 2 describes the experimental methods involved with each work described in the following work chapters. Various functionalization methods used with each substrate type and dopant type are outlined in detail. A brief and general description of the MLD surface functionalisation process is also provided.

Chapter 3 outlines extensive testing of phosphorus MLD processing which was first optimized on blanket silicon wafers and then transferred to SOI and nanowire test structures. Characterization of P-MLD doped blanket wafers with SiO_2 capping with ECV and SIMS demonstrated that P diffusion into the silicon lattice was being inhibited and not following the expected limited source diffusion model. It was theorized that surface oxidation which results from the functionalization process is leading to this inhibited diffusion. Application of P-MLD to SOI both represented the first of this kind in literature and acted as a confirmation of previous blanket results. Electrical results on scaled SOI down to 4 nm film thickness, and nanowires demonstrated that MLD is capable of doping these advanced applications but requires increased carrier concentrations to compete with beam-line implantation.

Chapter 4 both provides solutions to some of the issues seen in the previous chapter and demonstrates a novel approach to doping Si with As. P-MLD processing which has been developed and extensively examined in the previous chapter to show an activation limit at 2×10^{19} cm^{-3} has been tested with silicon nitride capping and demonstrates increased activation levels approaching the target 1×10^{20} cm^{-3}. Results have been demonstrated with ECV and validation of total chemical concentrations via SIMS. Previous work on the use of nitride capping in the field of ion implantation has demonstrated that it has better “blocking” properties to prevent dopant out-diffusion, than oxide caps. It is theorized that this effect also leads to improved dopant incorporation from P-MLD. Application of this processing to nanostructures did not prove successful due to issues with cap addition and removal processes. These results are also outlined. Further work was carried out on planar Si to develop an As-MLD

process using a relatively safe As precursor of Arsanillic acid with tethering by aggregation methodology. A successful approach was determined to be through click chemistry with activation levels of $\approx 3 \times 10^{19}$ cm^{-3} demonstrated with a 5×10^{18} cm^{-3} junction depth of 19 nm. This also represents an order of magnitude increase on previous arsenic doping of Si with MLD through click chemistry (previous high = 2×10^{18} cm^{-3}). Control of active dose, max carrier concentration and junction depth has been shown through varied annealing parameters.

Chapter 5 discusses the application of a new functionalization method with As-acid to Ge substrates. Ge substrates are notoriously difficult to work with due to their unstable oxide layer. In this study a Cl-terminated Ge surface was utilized as a building block for functionalization with As-acid through a nucleophilic substitution reaction. XPS analysis showed that annealing in a vacuum environment was necessary for attachment of the As-acid molecule with monolayer formation assessed through re-oxidation of the Ge 3d signal. DFT calculations determined that binding of the As-acid molecule to Ge via a di-dentate configuration was preferential compared to the mono-dentate and tri-dentate forms. Surface analysis with AFM during the MLD process demonstrated good surface quality with a minimal impact on roughness values. Active carrier concentrations from this As-MLD of $\approx 2\times10^{19}$ cm^{-3} represent the highest seen for As-MLD on Ge (2x previous record values), and are what has been recorded in literature as the electrically active limit through conventional RTA. Active carrier concentration values were validated through sheet resistance measurements. This study also demonstrated that incorporated dopant dose can be controlled in MLD via molecule size with comparison made between As-acid and the

previously used triallylarsine showing that the smaller As-acid molecule is capable of packing more dose on the Ge surface.

Chapter 6 outlines the application of P-MLD to SiGe, which is another potential channel material for use in future advance logic technology nodes. Thin films of strained SiGe on Si were epitaxially grown with varied concentrations of Ge (18, 30 and 60 %). Applying high temperature thermal treatments to SiGe has the potential to develop defects as a result of strain relaxation. A detailed material characterization SiGe film properties using AFM and XTEM was carried out to determine what anneal temperatures each SiGe content could sustain during MLD. XPS and angle resolved XPS were used to identify the actual bulk and surface Ge compositions present in each SiGe sample in order to tailor reaction conditions for chemical functionalization. Dopant profiling of the resulting MLD doped SiGe was carried out with SIMS and determined that phosphorus incorporation decreases for increasing mole fraction of Ge, when the RTA temperature is a fixed amount below the melting temperature of each alloy.

Chapter 7 presents the conclusions gained from the work in this thesis and also expands on what future possibilities there are for MLD on an academic research and industrial application setting.

List of commonly used Abbreviations

2-D - two dimensional

3-D - three dimensional

3,4-DCB – 3,4 Dichlorobut-1-ene

ABAPE – Allylboronic acid pinacol ester

ABF – Ammonium hydrogen difluoride

ADP - Allyldiphenylphosphine

AFM – Atomic force microscopy

ALD – Atomic layer deposition

APT – Atomic probe tomography

As -Arsenic

As-azide – Arsenic Azide

B - Boron

C - Carbon

CMOS – Complementary metal oxide semiconductor

C-TLM – Circular transmission line method

CVD – Chemical vapour deposition

DCM - Dichloromethane

DFT – Density functional theory

DHEM – Differential hall effect measurement

DLTS – Deep level transient spectroscopy

DPP – Diethyl-1-propylphosphonate

ECV – Electrochemical capacitance voltage

FET – Field effect transistor

FIBDD – Focused ion beam directed deposition

GAA – Gate all around

Ge - Germanium

GP-MLD – Gas phase monolayer doping

IC – Integrated circuit

MLCD – Monolayer contact doping

MLD – Monolayer doping

MOVPE – Metal organic vapour phase epitaxy

ODPA – Octadecyl phosphonic acid

P - Phosphorus

PBE – Perdew-Burke-Ernzerhof

PEALD – Plasma enhance atomic layer deposition

PLAD – Plasma doping

PMMA – Poly methyl methacrylate

RBS – Rutherford backscattering spectroscopy

RCA – Radio corporation America

RF – Radio frequency

RMS – Root mean square

RSF – Relative sensitivity factor

RTA – Rapid thermal anneal

Sb – Antimony

SEM – Scanning electron microscopy

Si - Silicon

SiGe – Silicon-Germanium

SIMS – Secondary ion mass spectrometry

SNR – Signal to noise ratio

SOI – Silicon-on-insulator

SRP – Spreading resistance profiling

STM – Scanning tunneling microscopy

TAA - Triallylarsine

T-BAG – Tethering by aggregation

TDD – Threading dislocation density

TEM – Transmission electron microscopy

TOF-SIMS – Time of flight secondary ion mass spectrometry

VLS – Vapour liquid solid

WCA – Water contact angle

Xj – Junction depth

XPS – X-ray photoelectron spectroscopy

XTEM – Cross sectional transmission electron microscopy

Acknowledgments

Some studies have shown that the average attention span of a human has dropped from 12 seconds in the year 2000, to 8 seconds in 2018, which coincides with the development of technology such as smartphones. Given that the aim of this thesis is to further advance research in this area it would be ironic if I were to write a long winded acknowledgment section which would run well beyond the measured attention span of which we are all now capable.

I never thought when I was beginning my undergraduate studies in UCC that I would spend most of the next decade at the university and enjoy such successful studies in collaboration with many fantastic individuals of which I will name a few. An incalculable amount is owed to my supervisor Dr. Brenda Long for introducing me to the world of postgraduate research in 2016 and guiding me through the doctoral process while helping all of her students to grow in every aspect of their lives. Without a doubt, I will be forever grateful for everything you have done for me. Whether it was discussing championship soccer or dopant diffusion there is no doubt that every conversation with Dr. Ray Duffy was enjoyable and a fantastic learning experience. The original CONDUCT research project which Brenda, Ray and I worked on from 2016 merged into CONDUCT 2 with the addition of Nikolay, Margarita, Fintan, John and Luke. Each and every one of you were a pleasure to work with and I appreciate how great of a contribution you have made to the work in this text. I am especially grateful for the work which Luke and I collaborated on in the Kane. I have no doubt in my mind that you will be a fantastic scientist in the years to come. A special mention

must also be made to Dan O' Connell, for all of the fantastic processing which he carried out in Tyndall over the course of both projects. The work of both CONDUCT projects would not have been possible without the funding of Enterprise Ireland and Applied Materials.

The School of Chemistry in UCC has provided a great platform for postgraduate studies. I appreciate the help from all staff members that I encountered over my time in the school. Prof. Justin Holmes guided the school over my postgraduate term while also guiding each of us students, whether it was in a conference room or just over coffee, thank you Justin. I promised that I would keep this short, so one final group remains that directly helped in completing my postgraduate studies and must be given a mention. To Shane, Will, Alex G, Eadaoin, Alex L, Giuseppe and all of the other postgraduate students, that are too many to mention, thank you for being such a great bunch to work with.

Dedication

My Family

CHAPTER 1
Introduction

1.1 Abstract

The year 2020 signals the start of a new decade and in the advanced logic industry it represents the progression from the 7 nm technology node to the 5 nm technology node. Moore's Law scaling of transistors has become increasingly challenged over the past decade by ever decreasing dimensions and performance requirements. The current roadmap for transistor development states that we are in the "more Moore" era where extreme scaling will further test Moore's law. New requirements for power, performance, chip area and cost will be the key metrics involved in gauging the success of semiconductor research and development for this field. Device architectures have successfully moved to finFETS from planar, but now require further advancement to gate-all-around (GAA) structures to maintain scaling and transistor properties advancement. These technology changes are demanding improved processing in all aspects of integrated circuit (IC) fabrication. Semiconductor doping remains a vital component of device processing for these advanced logic applications. Conventional doping methods such as ion implantation struggle to provide conformal and damage free doping of current 3-dimensional (3-D) nanostructures. Alternative doping methods such as plasma doping (PLAD), in-situ doping, atomic layer deposition (ALD) and metal organic vapour phase epitaxy (MOVPE) are being tested with varying degrees of success. Monolayer doping (MLD) is another method which is suitable for doping of nanostructures. MLD, by its nature is conformal and allows precise control over dopant diffusion and concentration, with no crystalline damage.

Work on MLD to date by a number of research groups worldwide, such as the Javey group in Berkeley, Dan group in Michigan/Shanghai, and Napolitani group in Padova, is outlined in this chapter. This technique has been applied to a variety of different materials, from silicon (Si) and germanium (Ge) to III-Vs with demonstrations of different dopant types and surface functionalization strategies. Specific consideration is given to achieving high active carrier concentrations with ultra-shallow diffusion, as these requirements are necessary for advanced logic applications. Particular deficiencies in the literature are noted and are addressed in the work Chapters 3-6 in this thesis. These areas include the achievement of active carrier concentrations greater than 2×10^{19} atoms cm^{-3} using phosphorus MLD (P-MLD) on Si, development of alternative methods of carrying out arsenic MLD (As-MLD) on Si, and the application of P-MLD and As-MLD to Ge and silicon-germanium (SiGe) alloys.

.

1.2 General concepts

1.2.1 What is doping?

Doping is the process of adding impurities to intrinsic semiconductors to alter their conductivity. Semiconductor materials have a small band gap in comparison with insulators and therefore the addition of small amounts of impurities leads to a dramatic increase in their conductivity. Both trivalent (*e.g.* boron) and pentavalent (*e.g.* phosphorus) elements are used to dope Group IV semiconductors such as Si and Ge. When an intrinsic Group IV semiconductor is doped with a trivalent or Group III impurity it becomes a p-type semiconductor. As an example, individual Si atoms in a crystalline Si substrate are bonded to four neighbouring Si atoms through their four

valence electrons. When a boron (B) atom is added, it replaces a Si atom in the lattice and since it contains one less valence electron it is considered as adding a hole to the lattice. The “p” in p-type doping denotes “positive”, which means the semiconductor is rich in holes or positively charged ions. Alternatively, when an intrinsic Group IV material is doped with a pentavalent or Group V impurity, such as phosphorus (P), we get an n-type semiconductor, where “n” stands for “negative” as P contains an extra valence electron.

1.2.2 Transistor development

Transistors are semiconductor devices that are used for both amplifying and switching electronic signals and electronic power. Their ability to act as “on” and “off” switches is most commonly related to use in IC technology involved in most modern-day electronics. **Figure 1.1** shows a schematic of an n-type metal oxide semiconductor field-effect transistor (MOSFET) resulting from impurity doping. In this example the substrate is p-doped and contains two heavily n-type doped regions known as the source and drain. The flow of charge between the source and drain, through the channel, is determined by the gate properties in combination with the dielectric layer. Depending on whether a sufficient voltage is applied to the gate, the system will either be in the “on” or “off” state, as shown in the schematic.

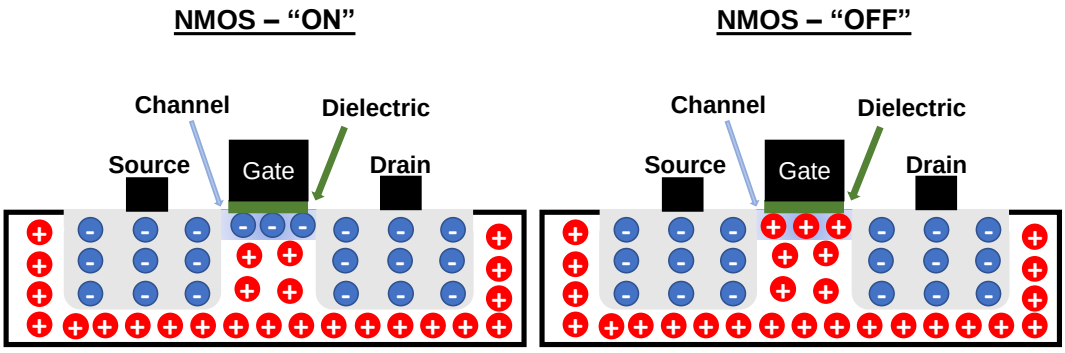


Figure 1.1: Schematic of planar n-type MOSFET (NMOS). NMOS – "ON" on the left depicts a channel where flow of the electrons has been allowed. NMOS – "OFF" on the right depicts a channel where the flow of electrons has not been allowed. This switching between ON and OFF states is controlled by the gate.

The dimensions of transistors have scaled over the past 50 years in accordance with Moore's law with the number (of transistors) on a chip roughly doubling every 2 years. The original planar device structure has progressed, with scaling, to the currently used Fin and silicon-on-insulator (SOI) structures. Although SOI preceded Fin's, the most commonly used structure today is the Fin structure. Both demonstrate quality electrostatics, but it is possible that economic factors have driven the success of Fins over SOI, as they are considered cheaper to produce. To give an example of the quantity of transistors in a single device, an iPhone 11 which was released in 2019 contains approximately 8.9 billion. This equates to roughly 1.2 transistors for every person in the world (world population 2017 ≈ 7.53 billion), all contained in one phone.

Over the past decade there have been many claims that this continued transistor scaling was not sustainable. Moore's law scaling is being pushed to the limit but current roadmaps show that the "more Moore" era will continue through to 2025.[1, 2] Cloud

computing and the requirement for “instant data” have pushed computing to the edge with a need for ultra-low-power devices that remain “always-on” while also being of high performance to enable the generation of data instantly. The International Roadmap for Devices and Systems 2018 (IRDS-2018) outlined the key aspects for continued device scaling over the near- and long-term future. Targets are set for key parameters of power, area and cost that will all decrease significantly, while performance will increase every 2-3 years in order to maintain a “more Moore” scaling. In terms of device architecture there is a predicted transition from current technology to a GAA structure in the near-term, which is depicted in **Figure 1.2** (up to 2025).

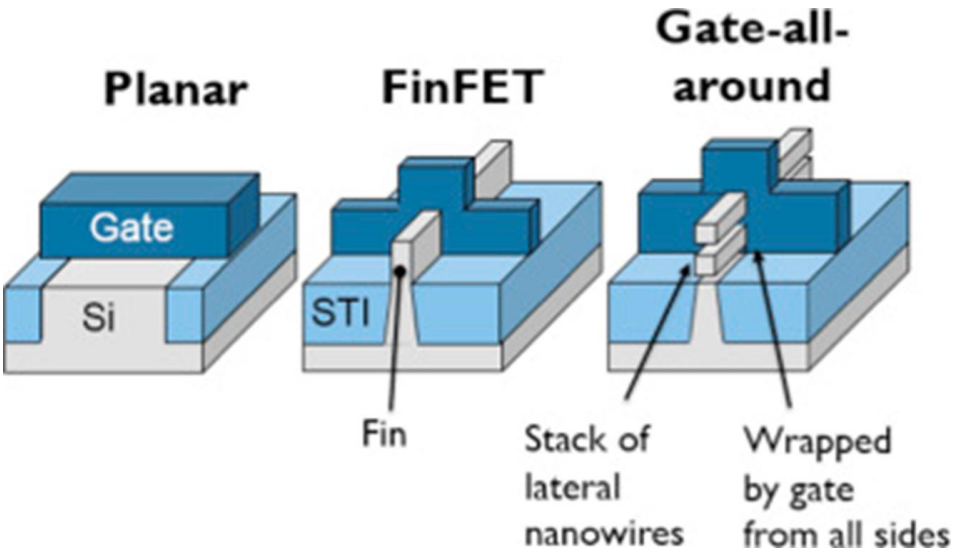


Figure 1.2: Transistor architectures have transitioned from planar to finFET to maintain Moore’s law. Gate-all-around structures (GAA) are scheduled for implementation before 2025 in what is known as the “More Moore era”. [3] STI in this figure refers to shallow trench isolation.

It is likely that Si will remain the backbone of the semiconductor industry into this “more Moore” era, as we move towards the development of GAA devices. However,

it is probable that alternative materials will be introduced, alongside Si, to create high-mobility channels. SiGe, Ge and III-V's, for example, are possible alternatives as they provide increased drive current due to their increased electron and hole mobility when compared with standard Si.[4] It is predicted by the IRDS-2018 that channel material for logic applications will move to SiGe in 2020 and then to Ge from 2025.

1.3 State of the art in semiconductor doping

1.3.1 Beam-line ion implantation

Semiconductor doping has traditionally been carried using a technique known as beam-line (BL) ion implantation. Given that this approach has been the most common method of implantation it will simply be referred to as ion implantation from here on. This is an approach where the semiconductor surface is bombarded with ions of the desired atom, whether it be an n-type dopant for Si such as P or arsenic (As), or a p-type dopant such as B or indium (In).

The concept of ion implantation was developed through the 1940s and 50s finally resulting in it being brought to market in the 1960s. A pivotal moment was the filing of a patent in 1954 by William Shockley of Bell laboratories. He described ion implantation as a process that could alter the conductivity of a Group IV semiconductor material by bombarding it with atoms from a Group III or V element with sufficient energy to enable it to enter the crystal lattice. This process causes amorphization of the implanted region which, Shockley realised, could be recrystallized through thermal treatments during which the impurity atoms are

incorporated into the crystal lattice causing a change in electrical properties.[5] Ion implantation has been extensively studied and optimised over the course of the last 50 years. Companies such as Texas Nuclear and IPC, which were the forerunners of the implantation industry, have through mergers and terminations transformed into the modern-day industry leaders of Applied Materials, Axcelis Technologies and Nissin Ion Equipment.[6]

Although ion implantation has been a fundamental process in transistor development to its current state, its limitations are evident when the process is applied to sub 10 nm 3-D nanostructures. These include irreparable crystal damage, poor conformality and difficulty achieving ultra-shallow junctions. Control of the depth at which dopant atoms are located after implantation is impacted both by the initial ion bombardment step and the subsequent thermal treatment for recrystallization/activation purposes. Production of ultra-shallow junctions is vitally important to modern devices given that device dimensions are in the sub 10 nm regime. Source and drain regions of complementary metal oxide semiconductor (CMOS) devices require high, ultra-shallow doping levels to minimize junction leakage as the gate length decreases. A junction in this case is defined as the depth from the semiconductor surface where the concentration of intentionally introduced electrons (n-type doping) is equal to the concentration of holes which are intrinsic to the substrate. When attempting to implant dopant atoms at ultra-shallow depths, an extremely low implant energy is required. This causes a major problem as ion-ion repulsion (spreading of the ion beam) at low energies limits the tool's ability to transport and manipulate ions.[7] Several solutions have been proposed, such as deceleration [8] or molecular ion implantation,[11] which may satisfy the current requirements for device fabrication but will likely struggle to meet

future demands, due to decreasing dimensions and 3-D architectures.[9, 10] As mentioned above, during the implantation process the crystal structure of the semiconductor is damaged, resulting in an amorphous implant region which is supersaturated with point defects, and has to be repaired through a thermal treatment. However, this thermal treatment, post implantation, has been found to result in enhanced dopant diffusion through a process known as transient enhanced diffusion which makes it difficult to attain ultra-shallow diffusion depths through standard ion implantation and thermal annealing.[11] Co-implantation with species such as fluorine, for B doping of Si, has shown some success in reducing dopant diffusion during the thermal anneal step.[12] Advanced annealing techniques such as laser annealing and flash lamp annealing (FLA) have also demonstrated shallower diffusion depth and increased activation levels when used in combination with ion implantation.

The ion implantation process also struggles to adapt to non-planar surfaces such as finFETs, which are currently in the sub 10 nm regime. When applying ion implantation to these smaller 3-D devices the crystal damage caused is much more difficult to reverse if it is possible at all. If the Fin is completely amorphized it has been found that defective recrystallisation occurs, as shown in **Figure 1.3**.[13] Even when the Fin is not completely amorphized the regrowth process may take place at different velocities, between the bulk and the sidewall, resulting in a large number of twin defects leading to limited drive current while also impacting resistivity. This results in higher junction leakage and parasitic resistance problems.[14] The use of "hot" implantations has been studied in an attempt to prevent the amorphization of the substrate. It was found, however, that this approach led to increased channelling, due to the lack of amorphization, and therefore deeper dopant profiles, which is counterproductive

considering the requirement for ultra-shallow.[15] When considering finFET devices with a narrow Fin pitch, the directional nature of ion implantation will lead to a shadowing effect which limits both control of dose and dopant positioning this results in non-conformal doping.[16]

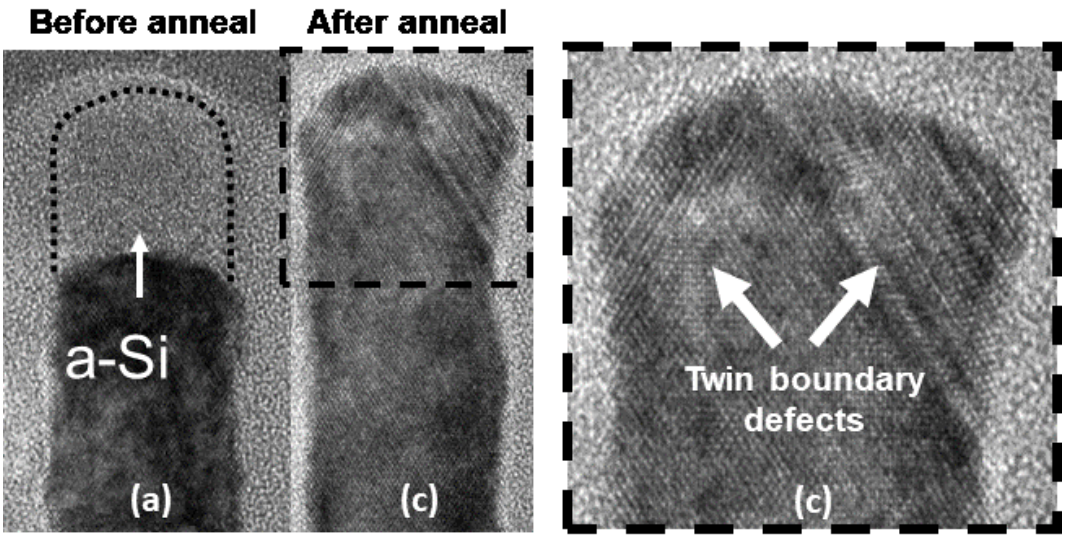


Figure 1.3: Cross-section transmission electron microscopy images of an ion implanted Fin structure before (a) and after (c) thermal annealing. Visible twin defects remain after thermal treatment. Adapted with permission from reference 13, Applied Physics Letters, AIP Publishing (2007).

1.3.2 Plasma doping

As was previously stated, some of the main downsides associated with ion implantation are crystal damage (amorphization), non-conformality and difficulty producing ultra-shallow junction depths (Xj). Through years of research and development plasma doping (PLAD) has been found as a viable alternative which is capable of addressing some of these issues.

PLAD is an adaptation of ion implantation, where a dopant-containing gaseous precursor is energized into a plasma by a radio frequency (RF) source. The required dopant ions are then extracted from the plasma by applying a voltage to the substrate and targeting them into a semiconductor wafer.[7] The voltage applied determines the implantation depth which enables ultra-shallow junction formation. This is considered to be one of the main advantages of PLAD as it produces ultra-shallow junctions much more quickly than ion implantation. Although PLAD is based on a relatively simple concept it is challenging as it relies on a number of secondary processes(deposition, resputtering, in diffusion, etc.).[17] These secondary processes are a result of neutral atoms from the plasma depositing on the target substrate followed by their interaction with incident ions that may cause them to re-sputter to other locations on the substrate. During subsequent activation anneals the deposited neutral atoms are also capable of in-diffusion into the substrates crystal lattice.

Lee *et al.*, carried out a study on the amorphization caused by ion implantation and compared it with plasma doping.[18] They claim that plasma doping produces considerably less damage than ion implantation due to the lower energies required for the incorporation of dopant ions. However, although there is less damage from this technique, it will still lead to the presence of defects after recrystallization with similar consequences to those described with ion implantation.

The ability of PLAD to uniformly dope non-planar structures is critical to its success in device fabrication in the future. Some of the earliest work examining this topic was carried out by Mizuno *et al.*,[19] they successfully doped the vertical sidewall of a trench

capacitor using PLAD. Even at this extremely early stage in the development of the technique, this group managed to achieve a thinly doped region (30-50 nm deep) at the relatively low processing temperature of 120 °C. However, when looking at more recent 3-D device architectures with more densely packed structures such as finFets, PLAD has encountered difficulties producing conformal doping.[20]

PLAD has also been found to result in high levels of dopant trapping at the SiO_2:Si interface,[21] This effect is worsened when using heavier dopant atoms, Kim *et al.* compared plasma doping using P and As on a set of finFET structures. Through use of atomic probe tomography (APT), they found that the majority of dopant atoms were segregated along the boundary of the Si substrate. They discovered that using heavier As ions resulted in more surface damage and led to increased surface oxidation.

1.3.3 *In-situ* chemical vapour deposition doping

Chemical vapour deposition (CVD) is a commonly used method for producing thin semiconductor films on bulk substrates. It involves the growth of a film of the required substance in either monocrystalline, polycrystalline or amorphous forms,[22-25] when the bulk substrate is exposed to a vapour containing the required mixture of precursors which react with or decompose onto the substrate surface.[24]

In-situ doping of these CVD films is a very complex process. Introducing another component in the vapour phase to the growth mixture inevitably leads to the possibility of more chemical interactions taking place.[26] This issue can sometimes be resolved through examination of the mechanisms and fine-tuning of process parameters *e.g.* gas

flow, chamber pressure. The main issue when considering CVD as a rival to ion implantation is the lack of uniformity and control over the location of the dopant atoms in the grown films.[27]

CVD has also been demonstrated as a method with potential for growing nanostructures such as nanowires.[23, 27] Doping of Group IV nanowires during the growth process is usually carried out by introducing phosphine (PH_3) or diborane (B_2H_6) gas precursors which decompose and dissolve into the liquid growth seed used in vapour-liquid solid growth (VLS).[28] This mechanism of *in-situ* doping has been found to severely impact the growth rate of nanowires and some reports claim that it completely inhibits nanowire growth when using high ratios of phosphine to silane, or arsine to silane.[29, 30] It has also been found that dopant incorporation during the growth process does not result in uniform doping throughout the 3-D nanowire structure with increased levels found in the sidewalls.[27] Negative impacts on nanowire morphology, such as nano-faceting, have also been observed when introducing B as the dopant molecule with diborane precursor.[31, 32]

1.3.4 Spin-on doping

Spin-on doping is a technique most commonly used for doping of Si solar cells.[33, 34] It may also have applications for doping of CMOS and other electronic devices.[35] This doping technique is regarded as a low-cost and simple method for non-destructive semiconductor doping.[36] In its simplest form, spin-on doping utilizes sol-gel processing techniques to coat the semiconductor wafer with a dopant source. **Figure 1.4** provides a general outline of the spin-on-doping process for semiconductor wafers. This initially involves the coating of the target substrate with a solution, usually

containing the dopant atom incorporated in monomer molecules which are Si based, such as phosphosilicates. This solution is then cured, at a relatively low temperature in comparison to later dopant diffusion/activation anneals, to "solidify" into a gel through solvent evaporation and polymerization. Finally, samples are annealed to diffuse the dopant atoms into the Si substrate.[35, 37] Numerous publications have investigated the application of spin-on doping to Si and Ge substrates with dopant species varying from P, Sb and Ga.[38-44]

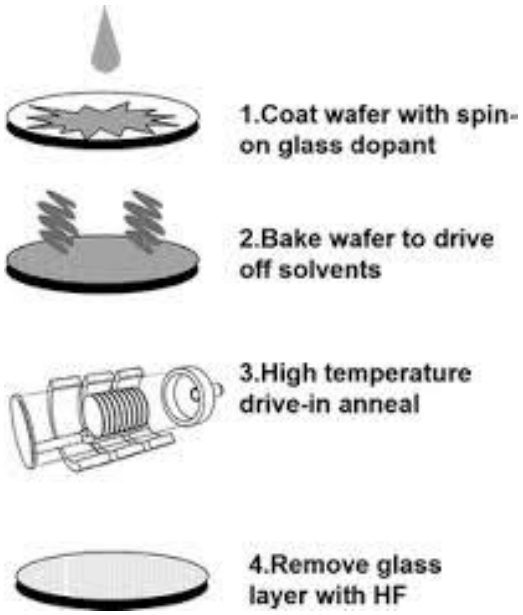


Figure 1.4: A general spin-on-doping process outline. Reprinted with permission from reference 45 MEMS Reference Shelf, vol 1. Springer (2011). [45]

Some of the downsides of spin-on doping include its lack of uniformity, and poor dose control over large areas.[36] Another major disadvantage when comparing spin-on doping to other rival techniques is that the removal of the spun-on layer is relatively difficult, often leaving an undesirable residue. Hoarfrost *et al.*,[35] proposed an approach which they believed would resolve some of these issues. They spun-on a solution of dopant-containing organic polymers and carried out the same processing steps used in

spin-on doping. As expected, the organic polymer film burned off during rapid thermal annealing (RTA) and they believe that the resulting deposit can be easily removed through wet chemical treatments providing a solution to conventional spin-on doping's major issue. This approach appears to be promising but still lacks the uniformity of MLD. Traditional spin-on doping does not have the required characteristics to be of use for doping of modern electronic devices, as it will be difficult to conformally cover arrays of tightly pitched 3-D nanostructures. Further work will have to be done on variations of this process for it to have an impact on the industry.

1.3.5 ALD and Gas phase MOVPE

Atomic layer deposition (ALD) is another technique that is widely recognised as a possible alternative to implantation for future doping applications.[46, 47] It is a gas phase deposition method which consists of sequential, self-saturating surface reactions. The required chemicals are introduced into the reaction chamber in what is known as a "pulse" to react with the surface followed by a "purge" to remove the excess gas and prevent gas phase reaction with the chemical involved in the next pulse-purge steps. The main advantage associated with ALD is its ability to conformally coat surfaces of complex geometry, whether they are planar or 3-D, with controlled layer formation. However, this often requires high cost processing with long times which lead to a low throughput. Further development of ALD using plasma sources, referred to as plasma enhanced atomic layer deposition (PEALD), will enable lower operating temperatures than those used in standard atomic layer deposition. Work by Baik *et al.*, has shown that PEALD in combination with flash lamp annealing can lead to high ($> 10^{20}$ cm^{-3}) incorporation levels of n-type dopants in Ge.[48]

Metal organic vapour phase epitaxy (MOVPE) has also been used as a method of gas phase doping with the potential for conformal doping of 3-dimensional nanostructures. In general, MOVPE is used as a gas phase technique for growth of semiconductor layers. It is capable of operating at temperatures in excess of 1000 °C. The adaptation of this tool for group IV semiconductor doping has been pioneered by the Tyndall National Institute. This system is capable of utilizing highly toxic gases such as arsine and phosphine at elevated temperatures allowing for effective doping (**Figure 1.5**).[49, 50] However, maintaining control of the dose using MOVPE is difficult due to simultaneous deposition and diffusion of dopants into the substrate at the elevated processing temperatures used.

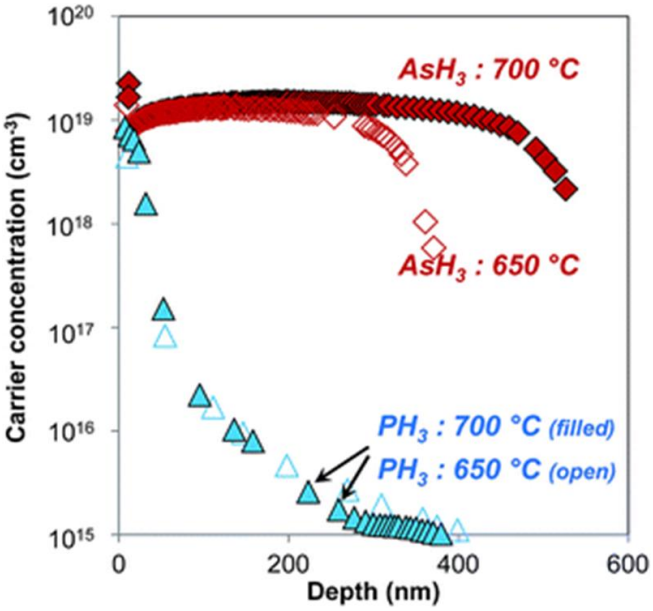


Figure 1.5: Example of work by Duffy *et al.*, doping Ge with As and P through MOVPE. Activation results shown are measured with electrochemical capacitance voltage profiling. Reprinted with permission from reference 50, Journal of Materials Chemistry C, Royal Society of Chemistry (2014).[50]

1.4. Monolayer doping

1.4.1 Background

Monolayer doping is a doping technique which was pioneered by Javey *et al.* that provides a solution to problems encountered with ion implantation.[51] It has the potential to produce ultra-shallow junctions with minimal crystal damage to the substrate. As was previously stated, one of the major problems facing the semiconductor doping industry in the coming years is the ability to conformally dope tightly pitched arrays of 3-D structures, such as finFET's, and non-line-of-sight doping, e.g. for GAA devices. MLD has shown great promise in this area.[52]

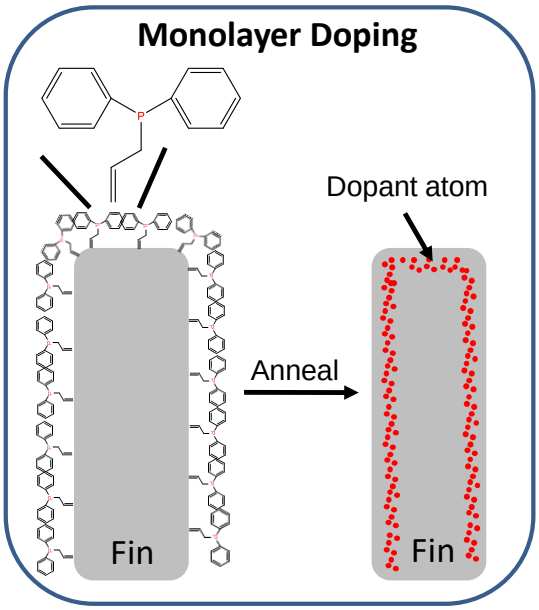


Figure 1.6: Schematic depicting the application of monolayer doping to a Fin structure., © 2014 IEEE

The process in its simplest form involves the chemical reaction of a molecule containing the target dopant atom to what is usually a hydrogen terminated Si surface (formed through a short dip in hydrofluoric acid). A suitable MLD molecule will contain the required dopant atom while also containing a reactive functionality intended for interaction with the semiconductor surface. It is also important that the remaining functional groups of the molecule are "un-reactive" and will not polymerise or lead to multilayer formation. These properties promote a self-limiting monolayer formation which is of course for MLD. In most studies surface functionalisation step is followed by the application of a capping layer to promote in-diffusion of the target atom into the substrate through thermal annealing, and subsequent capping layer removal.[53]

Due to the self-limiting nature of the reaction between the dopant molecule and the Si surface it is possible to apply a consistent and repeatable dopant dose. Long et al,

demonstrated the relationship between surface dose and resultant carrier concentrations after doping, if dopants were confined within the dimensions of Fins or nanowires.[52] The work in **figure 1.7** shows that it is possible to achieve carrier concentrations in excess of $1x10^{20}$ atoms cm^{-3} for sub-10 nm fin width or nanowire diameter, with surface dose values $\leq 1x10^{14}$ atoms cm^{-2}. A dose of $2x10^{14}$ atoms cm^{-2} would in this case be satisfactory to achieve carrier concentrations greater than $1x10^{20}$ atoms cm^{-3} for dimensions up to 20 nm. For example, allyldiphenylphosphine (ADP) which is a P-MLD precursor has dimensions (shown in **figure 1.7**) that would equate to a maximum achievable dose value of $2x10^{14}$ atoms cm^{-2}. Decreasing the size of the dopant molecule provides a possible route towards achieving the same levels of incorporation as seen with ion implantation.

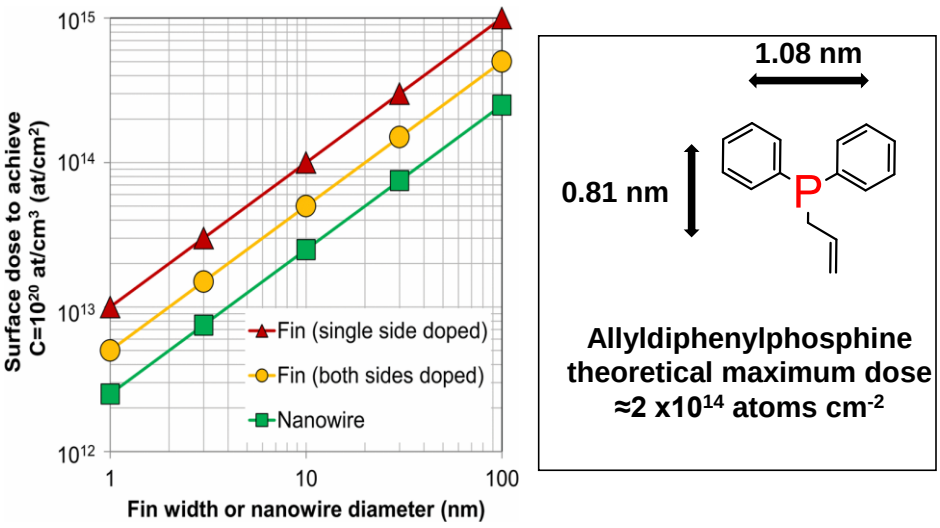


Figure 1.7: The graph represents work by Long et al where they estimated the relationship between Fin/nanowire dimensions and the required surface dose to achieve carrier concentrations in excess of $1x10^{20}$ atoms cm^{-3}. Adapted with permission from reference 52, © 2011 IEEE

1.4.2 MLD development

1.4.2.1 Phosphorus and Boron MLD

The majority of MLD publications to date have dealt with variations of P and B doping of Si. In this section we will discuss some of the state-of-the-art MLD processing and characterization developed by groups worldwide for P and B MLD on Si. O'Connell *et al.* previously summarized MLD literature up to 2016 in a comprehensive review article.[36] In the following sections the work up to 2016 will be noted and progress since this date will be examined in detail.

When reviewing MLD it is important to note and describe the pioneering work that was carried out by Javey *et al.* to introduce the topic to the world of academic research in 2008.[51, 53] They developed methods of P-MLD and B-MLD through the use of diethyl-1-propylphosphonate (DPP) and allylboronic acid pinacol ester (ABAPE), respectively, as dopant precursors. Chemical concentrations which may not all be electrically active, measured by secondary ion mass spectrometry (SIMS), of the resulting doped Si exceeded 1×10^{20} atoms cm^{-3} for both dopant types and demonstrated sub 50 nm Xj at 5×10^{18} atoms cm^{-3} . These publications provided the basis for further work on the topic which would be carried out by multiple groups worldwide to refine and optimize MLD processing.

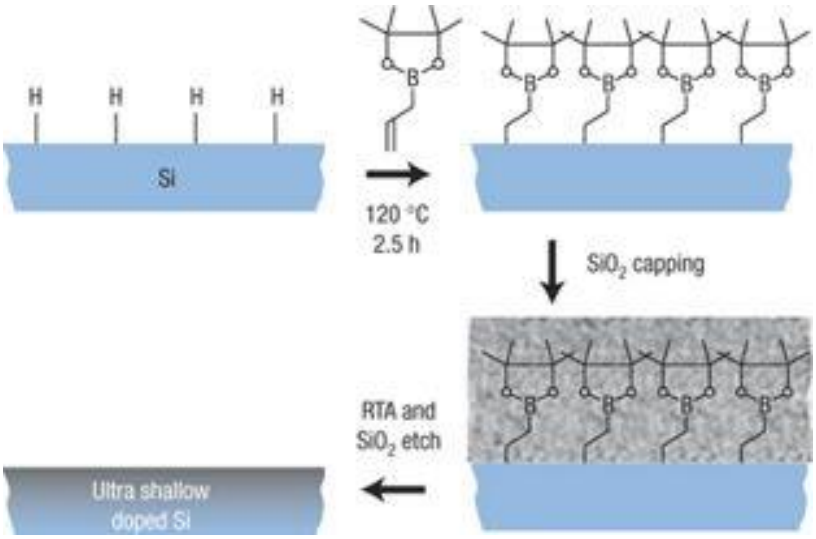


Figure 1.8: B- and P-MLD was pioneered by Ho *et al.*, with an example of the B-containing monolayer functionalisation procedure depicted. Reprinted by permission from reference 51, Nature Materials, Springer Nature (2008).

Standard MLD is a liquid phase process that is used to form the surface monolayer. Taheri *et al.*,[54] have developed a method known as gas phase monolayer doping (GP-MLD). A modified ALD apparatus was utilised to carry out these gas phase functionalisation reactions. This alternative to standard MLD also allows doping of 3-dimensional nanoscale architectures without having to consider wetting factors which can hinder nanowire doping. This gas-phase method was combined with a 1000 °C anneal for time periods of spike (no hold time at the maximum anneal temperature) and 10 second, respectively. They achieved carrier concentrations above 1 x 10^{20} atoms cm^{-3} total incorporated dopant atoms as measured by SIMS which are shown in **Figure 1.9**. The surface concentration of B using a spike anneal in Si was 7.5 $\times 10^{20}$ atoms cm^{-3} with an Xj of 3.5 nm (at 5 $\times 10^{18}$ atoms cm^{-3}). These values are at the limit of SIMS characterization but do represent some of the potential that MLD processing has for ultra-shallow doping.

Localized doping is a key feature of ion implantation with which MLD is striving to compete with. Through the use of nano-lithography, it has been shown by Taheri *et al.* *that* MLD is capable of selectively doping specific regions on the Si surface, *et al.* using a pattern of 2 µm poly methyl methacrylate (PMMA) resist squares. After application of this resist they carried out GP-MLD and removed the resist. Demonstration of localized doping was confirmed through conductive atomic force microscopy (AFM). Voorthuijzen *et al.*,[55, 56] had previously ventured into the area of localized doping via MLD. These publications also demonstrate that MLD is capable of integration into a variety of process schemes, as dopant monolayer functionalization was demonstrated both before and after nanolithography steps.

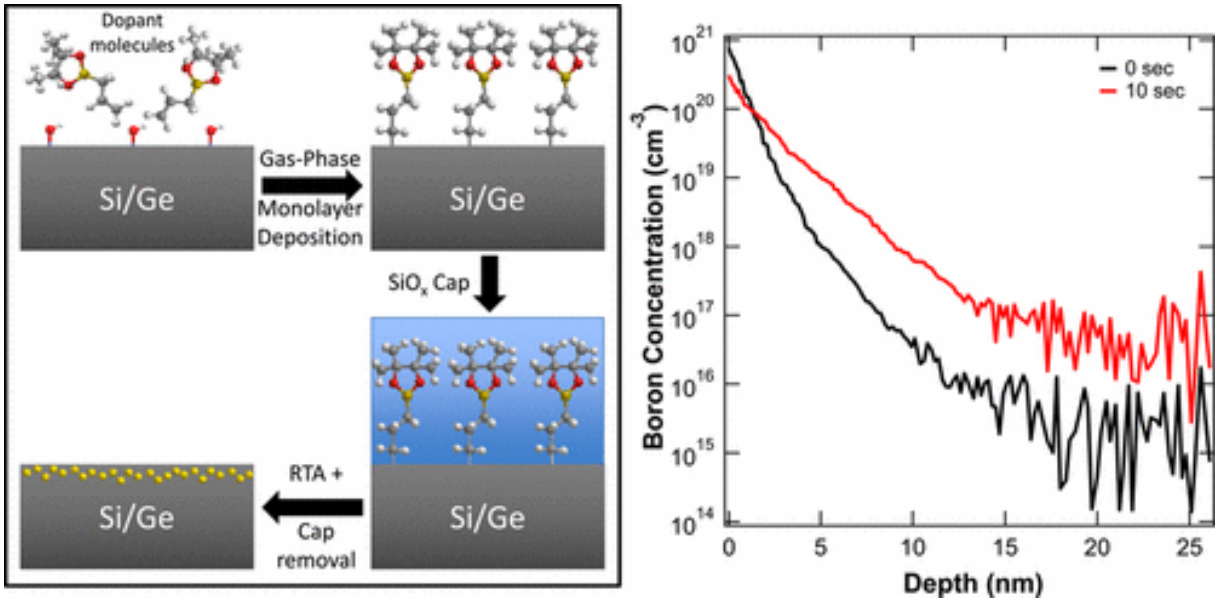


Figure 1.9: Taheri *et al.* developed a method for gas phase MLD which they applied to Si and Ge substrates with SIMS data showing high chemical incorporation of dopants at ultra-shallow depths. Reprinted with permission from reference 54 by Taheri *et al.* Copyright (2017) American Chemical Society.

Significant effort has been put into understanding whether capping layers are necessary for optimal dopant incorporation with MLD. Addition and removal of a SiO_2 capping layer involves several process steps which are beneficial to circumvent if possible. Caccamo *et al.*, carried out a detailed study into the impact of capping layer variation on the resultant dopant incorporation from MLD on Si.[57] They utilized a P containing dopant molecule (diethyl-1-propyl phosphonate) with a variety of SiO_2 deposition methods for capping layer addition and made a comparison with a sample where no cap was applied. Using spreading resistance profiling (SRP) for analysis of active carrier concentration profiles they determined that CVD capping with SiO_2 resulted in the highest maximum active carrier concentration values of 2×10^{19} atoms cm^{-3} and greatest total dose incorporation.

Monolayer contact doping (MLCD) is a variation of MLD where the target Si substrate is contacted with a second Si substrate, which has previously been functionalized with the dopant molecule, and thermally annealed. This thermal treatment induces diffusion of the dopant atom into both target and donor substrates, while also providing energy for activation.[58, 59] The main advantage of this method is the ability to carry out the MLD process without the use of capping layers. Hazut *et al.*, demonstrated that MLCD using a variety of P precursors (diphenylphosphine oxide, triphenylphosphine oxide, and tetraethylmethylenediphosphonate) resulted in total chemical concentration values (by SIMS) approaching the solid solubility levels of P incorporation at $\approx 5 \times 10^{20}$ atoms cm^{-3}. When applied to Si nanowires, the measured electrical resistance led to the conclusion that a maximum active carrier concentration of $\approx 1 \times 10^{19}$ atoms cm^{-3} was achieved. A further novel contribution made by Hazut *et al.*, was to develop a method of doping nanowires with both n and p-type dopants in a single step to produce parallel

p-n junctions.[60] This study once again demonstrated maximum active carrier concentrations of $\approx 1 \times 10^{19}$ atoms cm^{-3} for P doped nanowires which were measured through scanning tunnelling microscopy (STM).

Veerbeek.*et al* [61] examined the use of MLCD and an MLCD/MLD combination for the doping of highly porous nanowires, which would have had a large surface area due to the increased porosity. They reported MLCD dose values an order of magnitude higher than those they achieved using MLD and the same reaction conditions. In this study a relatively large carborane molecule (1-triethoxysilyl-2-methyl-carborane), which contains 10 B atoms, was synthesized with the aim of increasing the possible dose available for doping. This area of dose control is an important topic for MLD. Tailoring the size of the molecular precursor should, in theory, enable a wide range of doses to be introduced. Possibly the most significant demonstration of this precursor tailoring to date has been by Wu *et al.*, where macromolecules containing P were chemically bound to Si with the aim of controlling single dopant atom placement in the target crystalline lattice.[62, 63] This control of single dopant atoms is extremely challenging for other doping techniques and, with its potential application to quantum computing, could prove to be a breakthrough application for MLD processing.[64, 65]

Hazut *et al.*[66] also pioneered a variation of MLD known as remote monolayer doping which has the ability to selectively dope regions of a substrate. Photolithography processing was used to pattern a photoresist mask which is applied to the target substrate. This enabled determination of areas which are selectively doped. A donor substrate is functionalized with the dopant atom source. These substrates are then

brought into contact, in a similar manner to MLCD, and through thermal processing it is capable of selectively doping areas of the target substrate. Characterisation of the MLD doped substrates was carried out with false colour scanning electron microscopy (SEM), sheet resistance measurements, and SIMS.

As was previously discussed, incorporation of dopant atoms during nanowire growth has proven difficult as it has been shown to result in defective growth. Puglisi *et al.*, demonstrated that nanowires which had been grown via CVD could be doped following growth by MLD.[67] Electron microscopy analysis showed that, after MLD, the nanowire structures were not damaged and had no visible defects. SRP analysis of active carrier concentrations on a planar sample which had also been doped via the same MLD processing demonstrated max active carrier concentration levels $\approx 1 \times 10^{19}$ atoms cm^{-3}.

Carbon (C) contamination of electronic devices would cause an issue as it would negatively impact electrical properties due to C-dopant defect formation resulting in deactivation of the dopant atoms. When selecting a dopant molecule, it is possible to minimize this issue but not completely remove it. All dopant molecules used in MLD contain an organic shell composed of C and possibly other elements. During thermal treatments, these elements are also capable of diffusing into the Si substrate. Several studies have been carried out to investigate the impact of C (and other elements) contained in these molecules on the activation of dopants introduced via MLD, with varied conclusions as discussed below. For example, it was reported by Shimizu *et al.*,[68] using APT, that C and O contamination are restricted to the first few nanometres

of Si (≈ 2-3 nm) and they proposed that the removal of these layers would solve the issue.

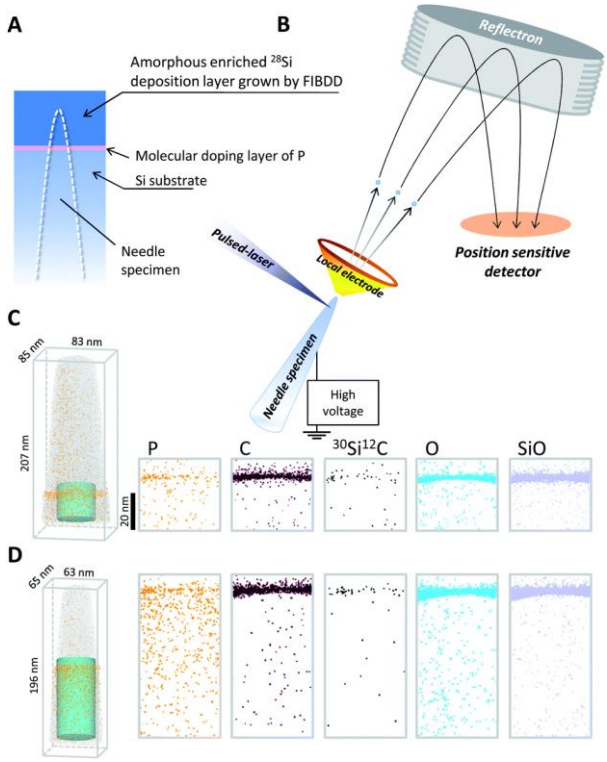


Figure 1.10: APT analysis of P-MLD doped Si was conducted by Shimizu *et al*. Through elemental mapping they determined that the majority of C and O contaminants, introduced by MLD, were confined within ≈ 2 nm of the surface. Reprinted with permission from reference 68, Nanoscale (2014).

Gao *et al.*,[69] have investigated the impact of introducing C into Si during P-MLD processing with deep level transient spectroscopy analysis (DLTS) of the resulting defects. They determined that up to 20% of P atoms were electrically deactivated by C or oxygen (O) related defects. In a further publication Gao *et al.*,[70] proposed a method of removing these C related defects via post MLD annealing processes. They proposed the use of "longer" anneals at relatively low temperatures (up to 400 °C) to remove the C-related defects. Although relatively low temperatures are used for these thermal treatments, they are for time periods greater than two minutes which would

both slow throughput and lead to an additional step in MLD processing which could be seen as a negative industrially. A recent report by Zhi *et al.*, also proposes a thermal pyrolysis method for reducing the impact of C contamination on P-MLD samples.[71] This fundamental issue of C incorporation during MLD processing will continue as a point of contention when considering the process as a viable alternative to implantation industrially.

Further to this work on P-MLD, Gao *et al.*, studied the impact of C and related defects on B-MLD.[72, 73] Utilizing the same characterization methods as previously used on P-MLD doped samples they determined that B-MLD, with ABAPE, does not suffer from the same degree of dopant deactivation. Up to 99 % of B was found to be active with 1 % deactivated through binding with O impurities which form majority hole traps. The C defects which caused issues with P-MLD samples were found to have no negative impact on B-MLD samples as they only captured electrons and did not interact with the hole population introduced from B doping.

The impact of surface states on MLD was studied by Park *et al*.[74, 75] In this study they examined different crystal orientations, crystallinities and surface defects using B-MLD with ABAPE as a dopant precursor. They found that (100) Si functions as a more efficient surface state for MLD compared to (110) Si which they deduced was a result of the lesser reaction sites available on the (110) surface for termination with the ABAPE molecule. SIMS profiles demonstrated high surface carrier concentrations greater than $\approx 1\times10^{20}$ atoms cm^{-3} for both states. The accuracy of SIMS in this surface region is heavily dependent on calibration and is always in question.

Developing novel applications for MLD should enable greater industrial application of this methodology. He *et al.* has recently proposed P-MLD as a means of doping Si for phototransistors.[76, 77] This form of transistor relies on exposure to light for operation and is commonly used in state-of-the-art photonic applications. Through the use of P-MLD, they produced Si nanowires with a core P-N junction, which they characterized with SEM, TEM, SIMS and electrical measurements. It was determined in this study that P-MLD enables the formation of highly repeatable phototransistors which is promising for commercialisation purposes.

Although, planar and nanowire Si functionalization have been the main test methods of MLD, it has also been applied to nanoparticles. Mathey *et al.*,[78] demonstrated that B-MLD could be applied to nanoparticles while also introducing the concept of a self-capping molecule (**Figure 1.11**). In this study a set of molecules (Tris(2-hydroxyphenyl)methane-borate tetrahydrofuran adduct and Phenanthro[9,10-d][1,3,2]dioxaborole) were used that contained relatively large terminal functional groups which acted as a capping layer to promote diffusion into the target substrates. Removal of the capping step from MLD would be beneficial from the commercial and throughput perspectives. The underlying issue with capping is the requirement for deposition methods that will also conformally coat tightly pitched nanostructures. This could potentially lead to a situation in future device dimensions where it would be possible to produce conformal dopant monolayer coverage while not being able to conformally cap the sample. Therefore, it is imperative that alternative methods for promoting diffusion into the substrate or capping are explored. Tzaguy *et al*., have also recently used SiO_2 nanoparticles as a target for B-MLD dopant attachment.[79]

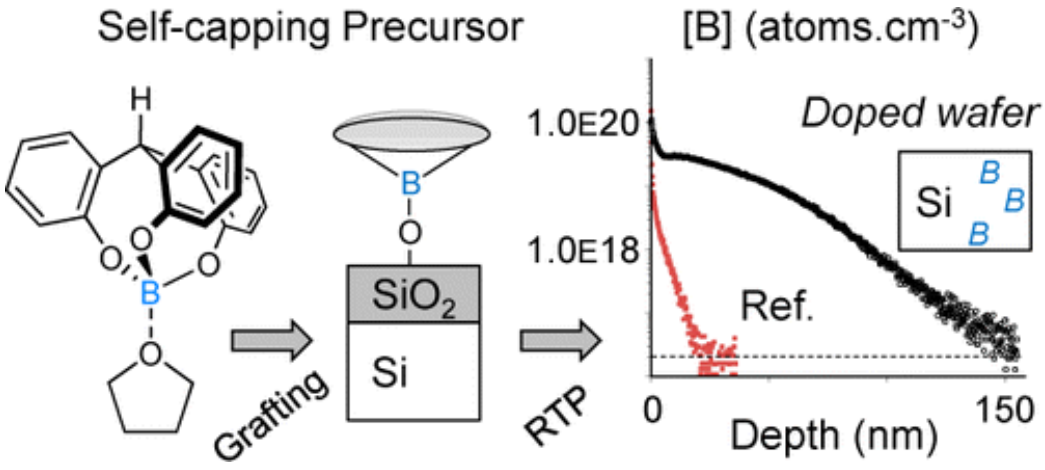


Figure 1.11: Mathey *et al.*, both demonstrated that MLD is applicable to nanoparticles and developed a self-capping precursor approach for B-MLD. Reprinted with permission from reference 78 © American Chemical Society (2015)

1.4.2.2 Application of MLD to alternative dopant and substrate types.

When surveying the landscape of MLD literature it is quite obvious that publications on the use of alternative n-type dopants for Si are sparse. To date there have only been three publications related to As and three related to antimony (Sb) doping of Si and Ge. There are a number of reasons as to why there is such a disparity between the work involving P/B and As/Sb/others. The toxicity of As and Sb precursors is well recorded, with most academic research set-ups unsuitable for their use due to safety concerns. There are also issues with reactivity of As- or Sb precursors. To the best of the authors knowledge there are no commercially available As- or Sb- molecules which contain the allyl (R-C=CH_2) functional group capable of reacting with Si and Ge through the most commonly used reaction types of hydrosilylation/hydrogermylation. Therefore, alternative reaction types are required for the attachment of these precursors in MLD.

O'Connell *et al.*[80] synthesized a triallylarsine (TAA) molecule which they used to dope Si nanostructures down to 20 nm in width, finding a maximum decrease in resistivity of 7 orders of magnitude after doping. O'Connell *et al.* further developed a click chemistry approach for attaching an arsenic azide (As-azide) molecule to a H-terminated Si surface. Given that the As-azide would not directly attach to the Si-H surface they initially formed a dialkyne monolayer on the Si through thermal hydrosilylation. The follow up reaction between the As-azide and the dialkyne monolayer is referred to as the "click" step. Click reactions are defined as a means of generating substances by joining smaller modular units. This both demonstrated a novel functionalization method and provided a new method for As-MLD.[81] This study demonstrated low activation levels of As after MLD processing with maximum carrier concentrations of $\approx 2\times10^{18}$ atoms cm^{-3} measured with electrochemical capacitance voltage profiling (ECV). The authors proposed that these low dopant levels would have application in "devices where low defect densities are required to minimise dark currents such as high operating temperature detectors and low-capacitance photodiodes for electron detection".

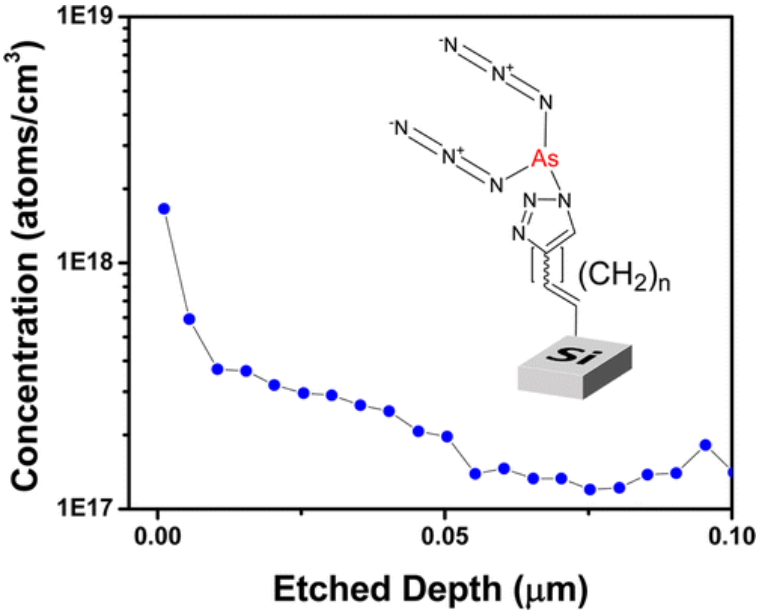


Figure 1.12: O'Connell introduced the concept of click chemistry to MLD surface functionalisation. The graph shows ECV active carrier concentration values from this method of As-MLD with As-azide precursors. Reprinted with permission from reference 81 © American Chemical Society (2015).

The application of MLD to other substrate types, such as planar Ge and nanowires, has proven to be a high interest topic of research in recent years. Long *et al.* also used TAA as an As-MLD precursor and developed As-MLD on blanket Ge wafers showing a maximum active dopant concentration level of 6 $\times 10^{18}$ atoms cm^{-3}.[52, 82] Due to the material properties of Ge (melting point = 938 °C) it is not suited to RTA temperatures above 700 °C. It was theorized that this 6 $\times 10^{18}$ atoms cm^{-3} mark represented a solubility limit of As for Ge via MLD.

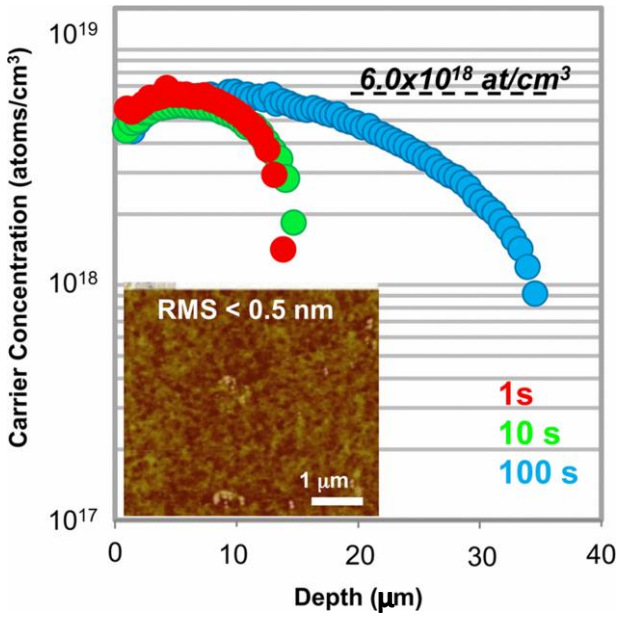


Figure 1.13: ECV analysis of active carrier concentrations achieved through As-MLD with TAA on Ge substrates by Long *et al.* © 2014 IEEE

Further work with n-type doping of Ge was conducted by Sgarbossa *et al.*,[83] who successfully carried out MLD with Sb using a metallic source and gas phase processing. They determined that the unstable nature of Ge-oxide enabled the formation of a controlled Sb-O-Ge layer with a consistent dose measured through Rutherford backscattering spectroscopy (RBS) measurements. This study also provided a demonstration of the potential for use of laser annealing with MLD. They demonstrated that Sb incorporation and activation was limited to values approaching solid and electrically active solubility limits when utilising conventional annealing tools ($\approx 2\times10^{18}$ atoms cm^{-3}) but could be increased to values considerably greater than this using laser annealing ($\approx 1\times10^{20}$ atoms cm^{-3}). Sgarbossa *et al.*,[84] also attempted to carry out P-MLD on Ge substrates, using DPP and octadecyl phosphonic acid (ODPA), but found their precursors to be unsuitable for complete release and activation of the dopant atom into the substrate during conventional RTA. Thorough x-ray

photoelectron spectroscopy (XPS) analysis did, however, show that P monolayers had been formed on the Ge surface during the functionalization procedure. Using laser annealing they achieved incorporation of the P dopants into the Ge sample with total chemical P incorporation of $\approx 3 \times^{19}$ atoms cm^{-3}, measured by SIMS. Alphazan *et al.*, also successfully carried out MLD on Ge using Sb-containing precursors.[85]

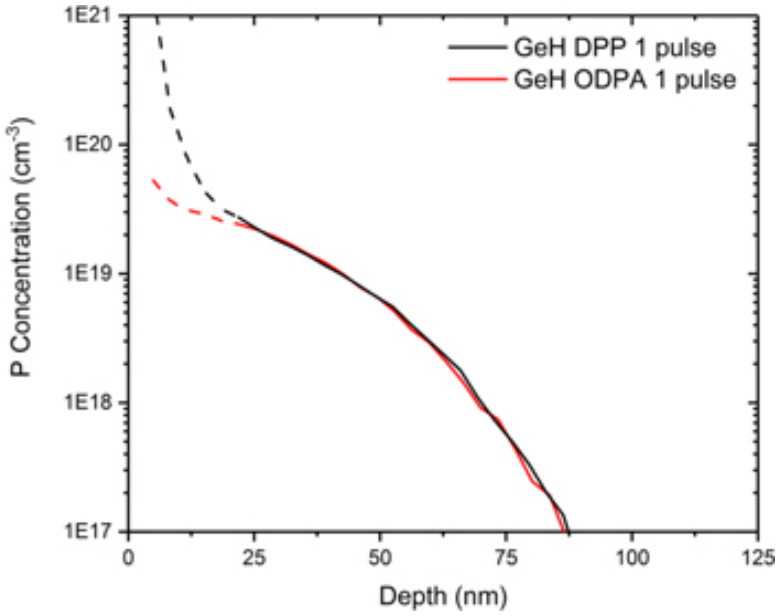


Figure 1.14: SIMS profiling of P doped Ge through the use of laser annealing with MLD. This work, by Sgarbossa *et al.*, demonstrates the potential for use of advanced annealing techniques in combination with MLD. Reprinted with permission from reference 83 © Nanotechnology, IOP Publishing Ltd (2018)

These publications have shown that advanced annealing technology has the potential to achieve ultra-high activation levels of dopants in combination with MLD. Flash lamp annealing, which is another advanced annealing technique, remains un-probed as a method of incorporating MLD dopants (**Figure 1.15**). Achieving sufficient thermal budget for activation while minimizing diffusion remains the aim of ultra-shallow junction formation with this type of doping.

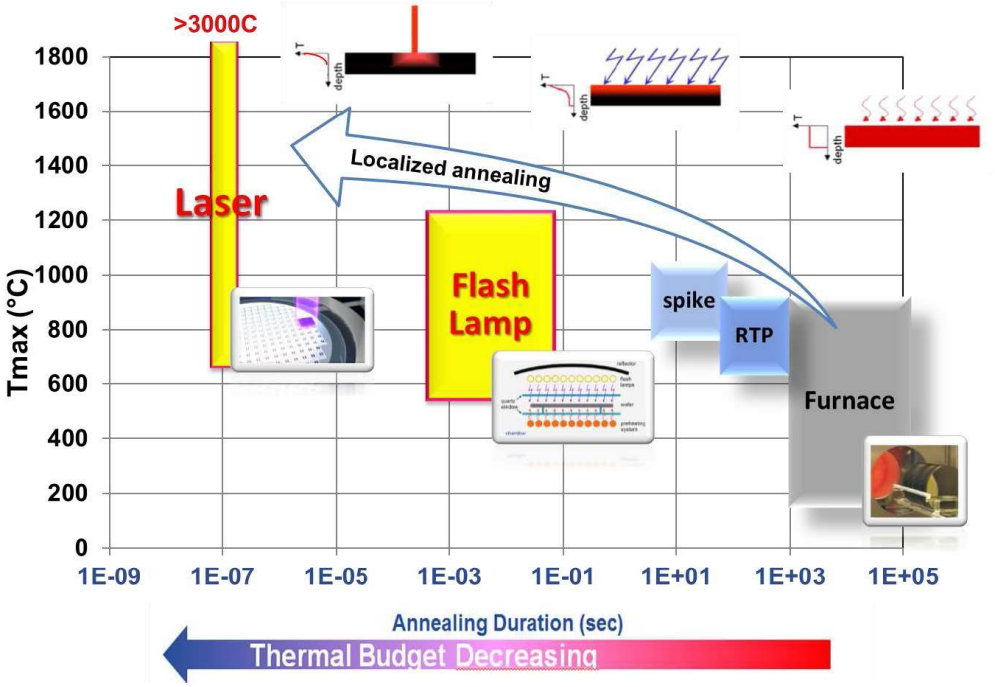


Figure 1.15: Huet *et al.* depicted the ability of advanced annealing techniques for operation at reduced thermal budgets and anneal times. Reprinted with permission from ECS Transactions, The Electrochemical Society (2019).[86]

Modelling and simulations of surface chemistry reactions enable elucidation of the mechanisms by which the dopant containing molecules in MLD bind to the semiconductor surfaces. Longo *et al.* have contributed a number of publications detailing computational analysis of MLD binding and molecular decomposition mechanisms.[87-90] Combing density functional theory (DFT) calculations with experimental results, they have examined phosphonic acid and arsonic acid MLD on H-terminated Si. It was determined that the maximum achievable coverage through functionalization with alkyl phosphonic acids is 2/3 due to steric constraint forces. These studies also examined the binding configurations of arsonic and phosphonic acids to Si and determined whether they would favourably bind in the mono-dentate, di-dentate or tri-dentate configurations. In a further study by the Longo group they

examined the possibility of combining As and P doping through MLD.[91] They determined that this combination of dopant atoms would lead to interesting possibilities when tuning MLD processing but would require a complicated functionalization process that has not yet been reported.

Though we will not go into details here, MLD processing has also been developed for use on InGaAs and GaAs substrates with dopant types varying from Si to sulphur.[92-96] There is potential for application of MLD to other III-V materials such as GaN in the future.

1.4.3 Limitations of MLD

Monolayer doping can be considered a relatively new means of doping semiconductor materials. Although there has been a considerable amount of research carried out on the topic over the past twelve years there is a great deal that has yet to be learned.

The aim of this thesis is to address some of the limitations associated with MLD on substrate types and materials which have both immediate and future viability in the area of transistor fabrication (Si, Ge, and SiGe). **Figure 1.16** graphically demonstrates the methodology used when addressing these points. Initial development of P- and As-MLD on blanket Si enabled the use of characterisation methods such as ECV, AFM and XPS which was beneficial before application to novel substrate types, such as SOI and nanowires, as these characterisation methods would not be viable on these substrates. Material and electrical characterisation of SOI and nanowires demonstrate

the viability of MLD on state-of-the-art applications. Further transfer of the MLD process to SiGe and Ge introduced novel materials to the library of MLD capabilities.

Increasing carrier concentrations to values approaching solid solubility levels in Si for P doping has proven difficult for multiple groups worldwide. This thesis reports on the strenuous efforts made to do so. Application of MLD to SiGe and SOI had not previously been shown until this work. As was previously mentioned, CMOS channel material for logic applications should transition to SiGe followed by Ge in the period from 2020-2025 in accordance with the IDRS-2018.

Direct functionalisation strategies to realise MLD on Si and Ge surfaces were limited to hydrolysilylation/hydrogermylation until the development of a "click chemistry" method by O'Connell *et al.*,[81] which allowed for attachment of either As or P precursors to linker molecules. It would be hugely beneficial if new strategies for the functionalization of Ge and Si could be developed, not only for MLD but also for the growing range of applications for these chemically modified materials (e.g. sensing, solar. etc). With respect to MLD it would potentially enable the use of smaller dopant precursors which would in turn enable higher dose incorporation. A novel method for direct functionalisation of Ge, which may have potential for direct Si functionalisation, has also been developed. This chemical reaction has been transferred from previously known wet chemical synthesis to surface chemistry. The application to Ge has enabled a controlled increase in dose compared with previous MLD work and shown electrically active levels of As that agree with literature values for the electrical activation limit through RTA.

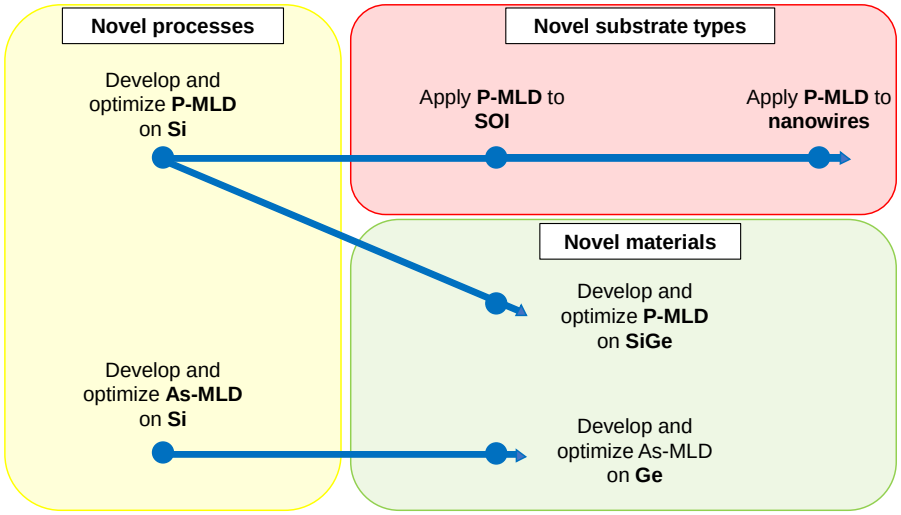


Figure 1.16: The methodology used in this work was to develop and optimize processes on blanket Si and then transfer to novel substrate types (SOI and nanowires) or novel materials (SiGe and Ge).

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CHAPTER 2

Characterization and experimental method

2.1 Electrochemical capacitance-voltage profiling

Precise measurement of active carrier concentration profiles in semiconductors is a difficult task. Some of the most commonly used methods for acquiring these profiles are through SRP, differential hall-effect measurement (DHEM), and ECV. The WEP CONTROL CVP 21 profiler, which is an ECV tool, has been used in this study for measurement of active carrier concentrations in Si and Ge. ECV involves sequential measurement and etch steps to provide profiles of carrier concentration (atoms cm^{-3}) vs depth (nm). This method involves the contacting of an electrolyte with the semiconductor surface to form a Schottky-like contact (shown in **Figure 2.1**), which contains a depletion zone. The controlled modification of this depletion region is fundamental to the ECV technique. The electrolyte used varies with the material being analysed. Ideally the electrolyte chosen will not etch the semiconductor through chemical means without application of charge. Ammonium hydrogen difluoride (ABF) is used for Si, and 4,5-Dihydroxy-1,3-benzenedisulfonic acid disodium salt (Tiron) is used for Ge.

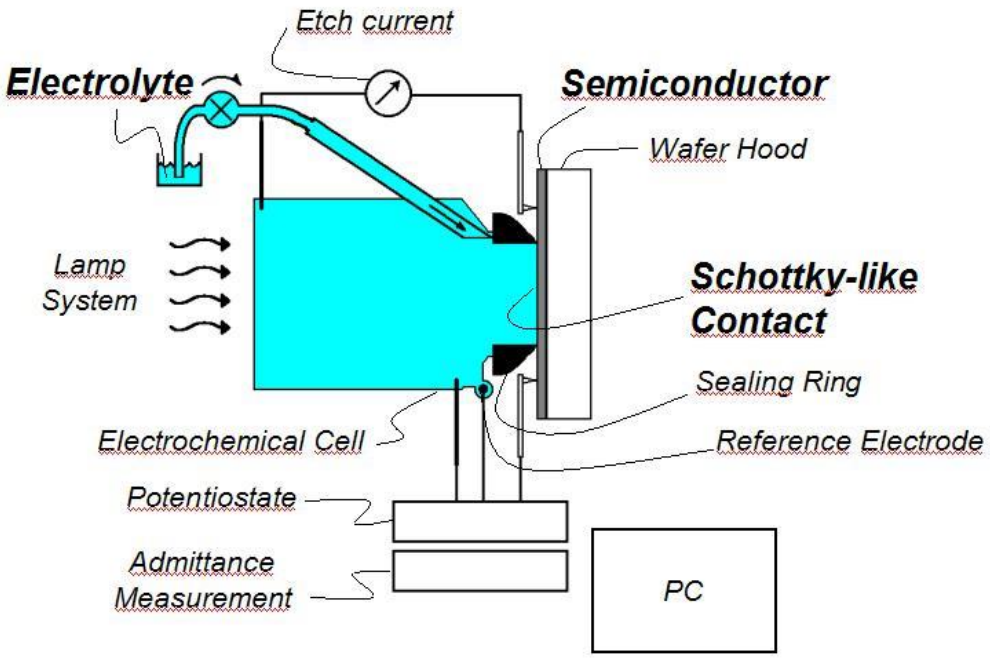


Figure 2.1: Measurement setup of WEP CONTROL CVP 21 ECV profiler. Reproduced with permission from WEP.

The mechanism by which Si is etched is based on the movement of holes. The CVP 21 profiler etch mechanism operates by the movement of holes to the semiconductor surface atoms followed by dissolution of the surface atom into the electrolyte. Therefore, etch conditions vary between dopant type, since hole concentrations are plentiful at the surface of p-type doped samples but not in n-type doped. P-type samples are etched by applying a positive potential to the semiconductor and a negative potential to the electrolyte. N-type doped samples require either, voltage etching, or the use of light, to induce movement of holes to surface. For n-type doped Si with high surface carrier concentration levels $>5x10^{18}$ cm^{-3} (typical for MLD), an increased voltage etching is used to induce a breakdown of the Schottky interface, allowing dissolution of the surface Si. Final etch depth and width were monitored after characterization by a profilometer to calibrate results.

To assess carrier concentrations in the doped semiconductor substrate, the width of depletion layer in the Schottky-like contact is modulated by changes in the applied voltage. This change in depletion layer width, both, slightly alters the capacitance of the region, and the quantity of charge at the edge of the layer. Capacitance is evaluated by using an admittance analyser which operates in a four-wire method. Considering the series and parallel resistance of the setup, the capacitance is calculated from this admittance value. The CVP 21 profiler automatically translates the calculated capacitance into an active carrier concentration value through the Mott Schottky equation shown below.

$$N = \frac{-2}{e\varepsilon_r\varepsilon_0 A^2 . \frac{d(\frac{1}{C^2})}{dV}}$$

N= carrier concentration

E = electron charge

ε_o = vacuum permittivity

ε_r = relative permittivity of the semiconductor material

A = measurement area

C = Capacitance of the depletion zone

dV = Change in external voltage applied

Carrier concentration measurement from ECV has an associated error value which is used as a means of ensuring accurate characterisation. This error value is calculated with each ECV data point through analysis of the linearity of the $1/C^2$ curve. At each measurement point $1/C^2$ is calculated at varied voltages. In theory this $1/C^2$ versus voltage curve should be linear and if so, the error value will be zero. The extent to which this curve deviates from linear defines the measurement error value.

It is important to highlight that carrier concentration determined from this equation is dependent on the measurement area (A). This is defined by the area of the sealing ring and also requires knowledge of the surface roughness of the material being analysed. An area factor adjustment can be made for rough samples where RMS values are high and will impact the resulting calculation. Therefore, it is essential that ECV measurements are reported with the corresponding sample topology through AFM or SEM for example. Traps and surface states also lead to inaccuracies when carrying out ECV analysis.

In this study ECV measurement of Si samples was carried out using 0.1 M ammonium hydrogen difluoride (ABF) as electrolyte. This solution was considered "fresh" for 48 hours and was disposed after this time period. Etch steps of 1 nm, 2 nm, 5 nm were carried out depending on profile depth and measurement error for carrier concentration was monitored to maintain below 10 % at all times.

A 0.1 M Tiron solution was used as an electrolyte for Ge samples. Start voltage (for measurement) and etch voltage were modified when using Tiron to -0.2 V and 0 V respectively. Due to the deeper diffusion of MLD dopants used in Ge the etch steps were modified to 2 nm, 5 nm, 10 nm and 20 nm. Increased relaxation time periods of 30 seconds were used to maintain carrier concentration error levels below 10 % at all times.

ECV characterisation of SiGe is not included in this thesis, due to issues with its application to this substrate type. While the physical properties of both pure materials are well defined, the combination is not the same extent. As previously mentioned, the

electrolyte used for Si differs to that of Ge, and the ε_r factor which is fundamental to the carrier concentration evaluation also varies between Si and Ge. For these reasons, ECV on SiGe is a considerably trickier proposition than Si and Ge. ECV also encounters issues when applied to SOI. The close proximity of the insulator layer (buried oxide) leads to errors in both etching and measurement steps which rely on the application of voltage to the substrate. This phenomenon occurred within ≈ 20 nm of the insulator layer and therefore made substrates such as the 13 nm SOI unsuitable for analysis.

2.2 Atomic force microscopy

AFM is a commonly used technique for measuring surface topology of semiconductor substrates. It also has a wide variety of other applications ranging from cell biology to piezoelectric materials. It operates by scanning an atomically sharp tip, which is connected to a cantilever, across a surface and monitoring any deflections caused by interactions between the surface and the tip with lasers and photodiodes. These deflections can then be translated into spatial maps for the analysed area with respect to height or phase of the surface.

AFM images in this study were taken on a Veeco multimode microscope using non-contact tapping mode. A 3-sided silicon tip with radius of 7 nm, and height of 15 µm, was used for all measurements. In general, scanning parameters used were a Z-limit of 1 µm, frequency of 0.3 Hz, and a scan area of 3 µm x 3 µm. The Z-limit corresponds to the height of the AFM cantilever from the sample surface while the frequency relates to the speed at which the tip scans.

2.3 X-ray photoelectron spectroscopy

XPS is a fundamental technique for the characterization of organic based monolayers on semiconductors. It provides quantitative analysis of elemental compositions and chemical states at the semiconductor surface. Spectra are obtained by irradiating the target material with X-rays and measuring the resulting electrons that are released with a specific kinetic energy that is later translated to binding energy.

In this study two separate XPS spectrometers were used for data collection and analysis. All data described in Chapter 3, unless otherwise specified, was acquired on an Oxford Applied Research Escabase XPS system. All other XPS data presented in Chapters 4, 5 and 6 was acquired on a Kratos ULTRA spectrometer. The Kratos Ultra tool allowed for increased measurement resolution and was used for this purpose. It is important to note that no direct comparisons have been made between data acquired from different tools.

The Oxford Applied Research Escabase XPS system was equipped with a CLASS VM 100 mm mean radius hemispherical electron energy analyzer with a triple-channel detector arrangement in an analysis chamber with a base pressure of 5.0×10^{-10} mbar. Survey scans were acquired between 0-1400eV with a step size of 0.7 eV, a dwell time of 0.3 s and a pass energy of 50eV. Core level scans were acquired at the applicable binding energy range with a step size of 0.1 eV, dwell time of 0.1 s and pass energy of 20 eV averaged over 10 scans. A non-mono-chromated Al kα X-ray source at 200 W power was used for all scans. All spectra were acquired at a take-off angle of 90° with respect to the analyser axis and were charge corrected with respect to the C 1s photoelectric line by rigidly shifting the binding energy scale to 284.8 eV. Data were

processed using CasaXPS software where a Shirley background correction was employed.

The Kratos Ultra spectrometer was operated with the following conditions. Sample temperature was kept between 20 and 30 °C with a mono-chromated Al K α source used. Pass energies of 160 eV for survey spectra and 20 eV for core regions were used with steps of 1 eV (survey) and 0.05 eV (narrow regions). Dwell times were 50 ms (survey) and 100 ms (regions) while 12 sweeps were carried out during survey spectra, and for core region analysis from 5 to 40 sweeps were used.

Core level analysis for Si examined the Si 2p, P 2s, N 1s, C 1s, and As 2p. Characterisation of Ge focused on the Ge 3d, C 1s, O 1s and As 2p core regions while Si 2p and Ge 3d were used for SiGe.

2.4 Secondary ion mass spectrometry

SIMS is considered a backbone of the dopant profiling industry. It is capable of quantitative analysis of elemental composition from the target substrate. SIMS operates by sputtering the target sample with a focused primary ion beam, while collecting and analysing the resulting secondary ions which are emitted. Two operation modes of SIMS are used known as static and dynamic modes. Static SIMS, which is also commonly referred to as time-of-flight SIMS (TOF-SIMS), is a version of the technique which is only capable of analysing the top 1-2 nm of the sample. Whereas dynamic SIMS is a technique used for measuring total chemical concentration with depth in a substrate. This depth measurement is carried out by calibrating the sputter rate of the incident focused ion beam and using a quadrupole mass spectrometer for

analysis of the secondary ions. It is generally accepted that this form of dynamic SIMS requires a ≈ 2 nm region at the sample surface to sufficiently reach equilibrium of the sputter process and acquire meaningful results. This top 2 nm is often regarded as a surface artefact. The more useful of these SIMS modes for MLD purposes is dynamic mode as it allows for total chemical concentration of dopant atoms such as As or P to be measured with depth in the semiconductor sample. It also has the ability to measure the C which has been introduced to the sample from MLD. Correlating SIMS results with ECV allows for comparison of total incorporated dopant with the electrically active dopant concentration and therefore leads to calculation of ionization %.

In this study SIMS data was acquired on a Phi Adept 1010 using a 0.5–1 keV Cs+ bombardment with negative ion detection. All SIMS characterisation was carried out by the Evans Analytical Group and utilised the relevant calibration processes.

2.5 Electron microscopy

Transmission electron microscopy (TEM) and scanning electron microscopy (SEM) are used as a means of acquiring high resolution images of semiconductor surfaces and cross-sectional views of either 3-dimensional or planar substrates. These forms of microscopy are considerably more powerful that traditional microscopy.

For structural analysis, FEI's Dual Beam Helios Nanolab 600i system with a Ga ion beam was used to obtain cross-sectional samples. Electron beam C, electron beam Pt, and ion beam C were used as protective layers. Lamellas were thinned and polished at

30 kV 100 pA and 5 kV 47 pA, respectively. JEOL 2100 HRTEM operated at 200 kV in the Bright Field mode using a

Gatan Double Tilt holder was used for cross sectional transmission electron microscopy (XTEM) imaging.

2.6 Hall-effect measurements

Silicon-on-insulator substrates are extremely suitable for hall effect measurements due to their electrically isolated silicon layer which is of known dimensions. Room temperature Hall effect measurements carried out in this study were performed using a controllable electromagnet in a LakeShore Model 8404 Hall effect measurement system (HMS) with dc and ac magnetic field capability in the range of ±1.7 T for dc, and of 1.2 T RMS (ac, 50/100 mHz), respectively. The ac magnetic field mode works in combination with a high-resolution lock-in amplifier that filters out all dc error components and uses phase analysis to remove ac error components. As a consequence, the ac results are generally more accurate that the dc results. Fitted with a high-resistance unit, the HMS can deal with many material systems that have low mobility, high resistivity and low carrier concentrations. As well as Hall effect measurements, the HMS also performs checks for ohmic behaviour and four-point resistivity measurements, and combines all-current/fieldreversal techniques, optimisation methods and averaging between all geometries to remove most major error components and obtain an accurate Hall voltage assessed against the signal-to-noise (SNR) accuracy obtained. [1] For all samples assessed in this work, the coupon size is ca. 1 cm × 1 cm with four pressure probe metal contacts placed in the corners of the coupon, thus creating a van der Pauw structure. [2] The Hall factor (*h*f) is set to

unity and the ac frequency is 100 mHz. We assume a uniform thickness with a uniform response across the material thickness. Moreover, the material is assumed to not have a dominant interlayer to be isolated electrically. If thickness-dependent properties are reported, we assume the thickness reported is correct.

2.7 Sheet resistance measurement

Sheet resistance measurements were carried out using a Lucas labs 302 four-point probe with a Keithley power supply. This characterization provided a means of verifying ECV data for active carrier concentration profiles.

2.8 Water contact angle (WCA) measurements

WCA measurements were carried out using an Ossila contact angle goniometer and analysis of the resulting angles was also carried out on the Ossila software. A water droplet volume of 5 µL was used for all measurements. Although this technique can be used for quantitative analysis of monolayer formation, this was not the case in this work. WCA was used as a supplemental technique to qualitatively analyse the semiconductor surface terminations.

2.8 General MLD procedure

All MLD procedures detailed in this thesis follow the same general outline, which involves four steps. The initial step 1) is to clean the substrate with appropriate

chemical solvents, such as IPA or acetone. This removes carbonaceous material which could cause issues with later processing. The clean semiconductor surface is then altered in step 2) by termination with, either H in the case of Si, or Cl for Ge. To produce these terminated surfaces the samples are dipped in dilute solutions of hydrofluoric and hydrochloric acid, respectively. Step 3) is where the dopant containing monolayer is chemically bound to the substrate. This involves reaction of the P- or As- molecule with the H- or Cl- terminated substrate followed by solvent cleaning to remove any physisorbed molecule. Characterisation with XPS, WCA, and AFM provides valuable insight the effectiveness of each of steps 1-3. The chemically bound, monolayer functionalised sample can then be processed with capping and annealing in step 4) which results in a doped sample suitable for characterisation with ECV, SIMS, etc. This brief outline of the MLD procedure is meant as an introduction to the technique and a more detailed functionalisation procedure is provided with each Chapter 3-6.

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CHAPTER 3

Monolayer doping of silicon: development of phosphorus doping on planar, silicon-on-insulator and nanowire substrates

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Adapted from the following presentation and publications. As a result, sections such as introduction and abstract may contain repeating concepts. A comprehensive authorship contribution section is provided in **Chapter 8**:

Results section 3.4.1 – 3.4.2.1.6

Kennedy, N; Holmes, J.D; Duffy, R; Long,B. "Critical analysis of phosphorus monolayer doping in silicon" **European Materials Research Society (EMRS) Fall Meeting 2017, 18th-21st September 2017, Warsaw, Poland.**

Kennedy, N; Duffy, R; Eaton, L; O'Connell, D; Monaghan, S; Garvey, S; Connolly, J; Hatem, C; Holmes, J.D; Long, B**. Beilstein Journal of Nanotechnology, 2018, 9: 2106-2113**

Results section 3.4.2.1.7

MacHale, J; Meaney, F; **Kennedy, N**; Eaton, L; Mirabelli, G; White, M; Thomas, K; Pelucchi, E; Petersen, D; Lin, R; Petkov, N; Connolly, J; Hatem, C; Gity, F; Ansari, L; Long, B; Duffy, R. **Journal of Applied Physics, 125, 225709, (2019)**

Results section 3.4.3

Duffy, R; Ricchio, A; Murphy, R; Maxwell, G; Murphy, R; Piaszenski, G; Petkov, N; Hydes, A; O'Connell, D; Lyons, C; **Kennedy, N**; Sheehan, B; Schmidt, M; Crupi, F; Holmes, J.D; Hurley, P; Connolly, J; Hatem, C; Long, B**. Journal of Applied Physics, 123 125701 (2018).**

3.1 Abstract

This chapter outlines the application of phosphorus monolayer doping (P-MLD) to silicon (Si) ubstrates through covalent binding of ADP via a hydrosilylation reaction. Extensive examination of various processing parameters such as reaction time and temperature were carried out on blanket wafers. The resulting dopant profiles were characterised with ECV measurements and the topology with AFM. Surface analysis with XPS of P-MLD functionalized samples both provided evidence of monolayer formation and showed that oxidation during MLD processing was present even with stringent efforts to prevent it. It has been theorized herein, that the presence of this oxide and the use of SiO_2 capping, impacts diffusion of P atoms into the Si substrate. This is most likely due to the P being trapped in the oxide layer or at the oxide to silicon interface, due to the significantly lower diffusivity of P in SiO_2 than Si with an apparent activation barrier at $\approx 2 \times 10^{19}$ atoms cm^{-3}. Optimized P-MLD process conditions from Si blanket studies were then applied to SOI substrates which represents the first demonstration of this kind in literature. Hall effect and circular transmission line method (C-TLM) testing, confirmed results found on blanket wafers that P-MLD on SOI also produces doping levels (10^{19} atoms cm^{-3}) which are an order of magnitude lower than beam-line (BL) ion implantation reference samples (10^{20} atoms cm^{-3}). A follow up study focused on the impact of decreasing SOI film thickness to sub-10 nm dimensions where it was found that the incorporation and activation of dopants was problematic in this size regime. Finally, this P-MLD process was applied to fabricated nanowire structures. This study agreed with all previous testing on SOI and blanket with P-MLD demonstrating resistivity values that equate to active carrier concentrations in the 10^{19} atoms cm^{-3} range. XTEM demonstrated the gentle nature of

MLD with no visible defects seen in the doped nanowire sample. In comparison, implant recrystallized nanowires were noticeably defective.

3.2 Introduction

Aggressive device scaling, towards sub-10 nm dimensions, has resulted in a number of techniques, such as ion implantation for doping, being deemed detrimental to future device production. Semiconductor substrates require doping (the addition of impurity atoms) to reduce their resistivity and enable their use in electronic devices such as MOSFET's (Metal-oxide semiconductor field effect transistors). Traditionally, *ex-situ* doping was carried out using beam-line ion implantation, however this suffers from several downsides when used on sub 10 nm structures with 3-D architectures .[1, 2] The main issues with ion implantation are the crystal damage it induces which cannot be annealed out of sub-10 nm structures and its inability to conformally dope 3-D structures due the directional nature of the ion beam. The introduction of this crystal damage has major negative consequences. Short channel effects (SCE's) become more profound with reduced device dimensions and when combined with crystal damage, leads to high leakage current which results in elevated power consumption.[2, 3] Ion implantation engineers have devised several methods to counter these issues, such as hot implantation, with only moderate success.[4, 5] Therefore, it is essential for future device scaling that a means of damage-free, conformal doping is developed. Monolayer doping (MLD) has the potential to succeed in achieving this.

MLD was pioneered by Javey *et al*. in 2008 and has subsequently been used to dope multiple substrate types such as Si, germanium (Ge), III-V's and others.[6-13] MLD involves the attachment of organic molecules, containing dopant atoms, to a surface

which can then be diffused into the substrate. **Figure 3.1** shows a schematic version of the steps involved in an MLD process. The most commonly examined reaction for attaching dopant-containing molecules to Si is hydrosilylation, where a molecule containing an allyl group is chemically bound to a hydrogen-terminated (H-terminated) Si substrate.[14] A capping layer is then applied to the sample followed by thermal treatment to promote diffusion of the dopant atoms into the Si substrate while also providing enough energy to activate them in the crystal lattice.

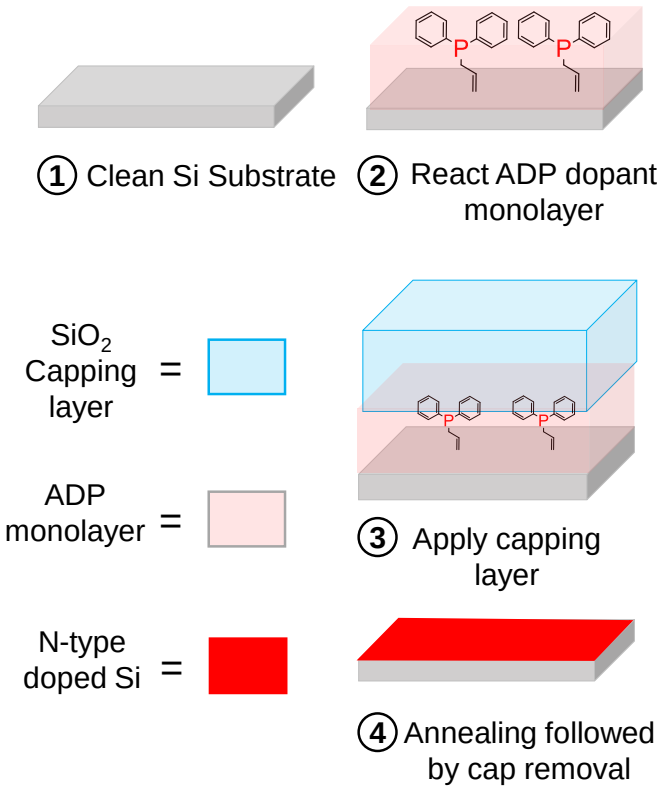


Figure 3.1: Schematic depicting MLD processing applied to Si wafers which were cleaned and H-terminated with HF (step 1), followed by monolayer formation with ADP (step 2). After monolayer formation the samples were capped with a sputtered SiO2 capping layer (step 3) and annealed in a RTA resulting in a shallow n-type doped Si after cap removal (step 4).

This chapter will initially describe the application of P-MLD to blanket Si as there are several characterisation techniques that can be used on bulk substrates (*e.g.* ECV, SIMS, AFM and XPS) that could not be applied to nanostructures. When the optimal process parameters (*e.g.* reaction and annealing conditions) have been established on blanket wafers they can then be transferred to thinned down SOI and nanowire substrates.

Si transistors encounter difficulties when scaled past 10 nm due to SCE and significant leakage current which increases their power consumption. SOI and finFETs are two means of device scaling which are currently being pursued by the electronics community. Planar, fully depleted SOI (FD-SOI) has been used to provide a more cost-effective scaling mechanism than finFET alternatives. Although initial wafer cost is higher for SOI compared to bulk Si, which is used to fabricate finFETs, the required masking and etching needed for Fin production is both complex and expensive. Ultra-thin body SOI is known to be high speed, with both low power consumption and parasitic capacitance.[15] SOI doping has applications in a variety of fields including electronics, thermoelectric, photovoltaics and others. It is show in this chapter that MLD is capable of damage free source/drain doping of planar SOI. At the time of writing this thesis this is the only demonstration of MLD on SOI substrates.

The final part of this chapter describes the application of P-MLD to Si nanowires. Given that the ultimate goal for semiconductor doping technology is to provide a solution that will conformally dope GAA structures with high active carrier concentrations at shallow depths, it is vitally important that nanowire test structures are utilized for MLD testing.[16]

3.3 Experimental methods

3.3.1 General procedure for Si functionalization with ADP

Glassware used in all following experimental sections were cleaned prior to use with multiple semiconductor grade solvent washes and piranha (5:1 solution of sulfuric acid: hydrogen peroxide) cleaning.

Samples were degreased through sonication in acetone for 120 seconds followed by a dip in 2-propanol and drying under a stream of nitrogen. Samples were then placed in a 2% HF solution for a period of 10 seconds to provide a H-terminated surface. Following this HF treatment, the Si samples were dried under a stream of nitrogen and promptly placed under inert conditions in the Schlenk apparatus to prevent re-oxidation. A solution of ADP in mesitylene (100 μL in 5 mL) was degassed using multiple freeze–pump–thaw cycles followed by transfer to the reaction flask containing the hydrogen-terminated Si sample. This reaction flask was connected to a condenser that enabled reflux conditions during the 3-hour heating period. After this 3-hour reaction period the samples were removed and sonicated in 2-propanol for 120 seconds followed by drying under a stream of nitrogen and storage in a glovebox. Upon removal from this glovebox, samples were promptly capped with a 50 nm layer of sputtered SiO_2 using an Oxford sputter system. RTA was carried out followed by cap removal. A dilute solution of buffered-oxide-etch (BOE) was used for cap removal.

3.3.2 SOI fabrication process

Nominally undoped SOI wafers of 66 nm (thickness of the surface Si layer) were prepared as a starting point for all SOI development, with a 145 nm buried oxide layer. These 66 nm wafers were thinned to all other used dimensions by controlled oxidation followed by stripping of the oxide layer. Dry thermal oxidation was carried out in a Thermco 9000 series horizontal furnace at 1000 °C. Oxide stripping was carried out with a Seimtool Spray Acid Tool (SAT) using ozone gas, hydrofluoric acid, and ammonium hydroxide. Each cycle resulted in the removal of approx. 1 nm of Si. Final thickness values were characterized with TEM and film continuity was also examined using AFM.

3.3.3 Nanowire fabrication process

The nanowire fabrication for characterization of all MLD processing presented here is reproduced from the publication by Duffy *et al* of which the author of this thesis is a co-author.[17]

The starting substrates for this fabrication were nominally undoped (100) SOI with a Si thickness of 30 nm or 66 nm on 145 nm of SiO_2. For nanowire processing, the SOI substrates were patterned using the Raith VOYAGER electron beam lithography (EBL) system with a beam energy of 50 keV and the high-resolution EBL resist hydrogen silsesquioxane (HSQ, XR1541, 2%) from Dow Corning. The substrates were firstly degreased by ultrasonicating them in acetone and isopropyl alcohol (IPA) solvents. After drying the substrates, HSQ resist was spun at 4000 rpm to achieve 15 nm resist thickness. In another set, 6 nm thick layers were prepared by diluting the resist to 1%. Spin coating was performed at 4500 rpm. The EBL exposure was a two-

step process, namely a low current set-up pattern for the high-resolution nanowires structures, and in the second step, in a high current set-up, the contact pads were exposed. This was done to decrease the total exposure time while maintaining the high resolution required for the nanowires. After the EBL exposure, the substrates were developed in NaCl (4%)and NaOH (1%) solutions for 4 min followed by 15 s rinse in deionised (DI) water and a second 15 s rinse in DI water in a second beaker. The samples were etched in an Oxford Instruments System 100 ICP etcher operating in the Reactive Ion Etch (RIE) mode. The etch chemistry was a Cl2/N2 gas mixture at flows of 20 and 40 sccm, respectively, with a process pressure of 10 mTorr and a RF power of 80W yielding a DC bias of 220 V. The sample temperature was controlled at 20 C with helium gas backside cooling with the sample mounted on a Si carrier wafer using KrytoxVR vacuum oil. Real time etch depth monitoring of the SOI film layer was achieved using an Intellemetrics LEP500 laser reflection system.

A UV lithography-based process was used to pattern the Ti/Au metal contact pads, based on a lift off technique. The steps are as follows: bake the sample in a hexamethyldisilazane(HMDS) primer vapour oven at115 C, spin on Micro Chem LOR3A lift-off resist at 3000 rpm for 50 s, hot-plate bake at 150 C for 3 min, spin on HMDS at 3000 rpm, spin on Micro Chem S1805 imaging resist at 3000 rpm, hot-plate bake at 115 C for 2min, align and expose in a Karl Suss MA1006 aligner for 4.5 s, exposure dose¼45 mJ/cm2, develop for 1min in Microposit 319 developer, rinse in DI water for 1min and blow dry with N2, immerse in dilute HF (25:1) for 5 s, rinse in DI water and blow dry with N2, load in a Temescal FC2000 e-beam evaporator and pump system to >5

107Torr, expose to Ar plasma for 20 s to improve metal to metal adhesion, evaporate

Ti:Au (10:150nm), lift-off resist and excess metal in Microposit R1165 resist remover at 90 C for 1 h, and finally rinse in DI water and blow dry with N_2.

Accurate control of Si contact pad and nanowire dimensions enabled the extraction of resistivity which was used as a means of direct comparison between MLD, implantation and MOVPE doping.

3.3.4 Characterization methods

A variety of methods were used for characterization of MLD on blanket Si, SOI and nanowire structures. These methods are extensively detailed in Chapter 2. Surface topology was assessed with AFM. Dopant profiling was carried out with SIMS and ECV. Surface chemistry analysis was undertaken with XPS. Hall effect and micro 4-point probe were used on SOI for further analysis of MLD doping.

3.4 Results and Discussion

3.4.1 Optimization of process conditions on blanket silicon

P-MLD was initially optimized on blanket Si. As previously mentioned, blanket Si enabled characterization techniques such as ECV, AFM, XPS, and SIMS to be used which would not have been possible on 3-D substrates. Given that the P-MLD process contained a large number of variable processing parameters, it was determined that a systematic approach to changing individual variables and monitoring the resultant active carrier concentrations (as determined by ECV) along with surface topology (through AFM), would best suit optimization. The following sections describe this

optimization process addressing a number of variables: (1) hydrosilylation reaction conditions, (2) annealing conditions and (3) capping layer.

3.4.1.1 Optimization of hydrosilylation reaction conditions

3.4.1.1.1 Reaction time

The reaction time was varied (1 → 3 → 15 hours) at a fixed reaction temperature of 165 °C, the boiling point of the solvent used in this process (mesitylene). Standard MLD processing was carried out on all samples and the carrier concentrations of all the samples was then measured using ECV (**Figure 3.2.**). It is clear that changing the reaction time had no impact on the incorporated dopant dose which is the same for all reaction times (dose = 4.7×10^{13} atoms cm^{-2}), suggesting that monolayer formation has been completed in the 1-hour reaction and no further ADP binding occurs during the longer reaction times. Previous MLD literature shows that reaction times for complete surface functionalisation can be as low as 10 minutes.[6] Decreasing reaction times is seen as a positive when considering MLD as an industrial alternative to current doping technologies as it leads to greater throughput.

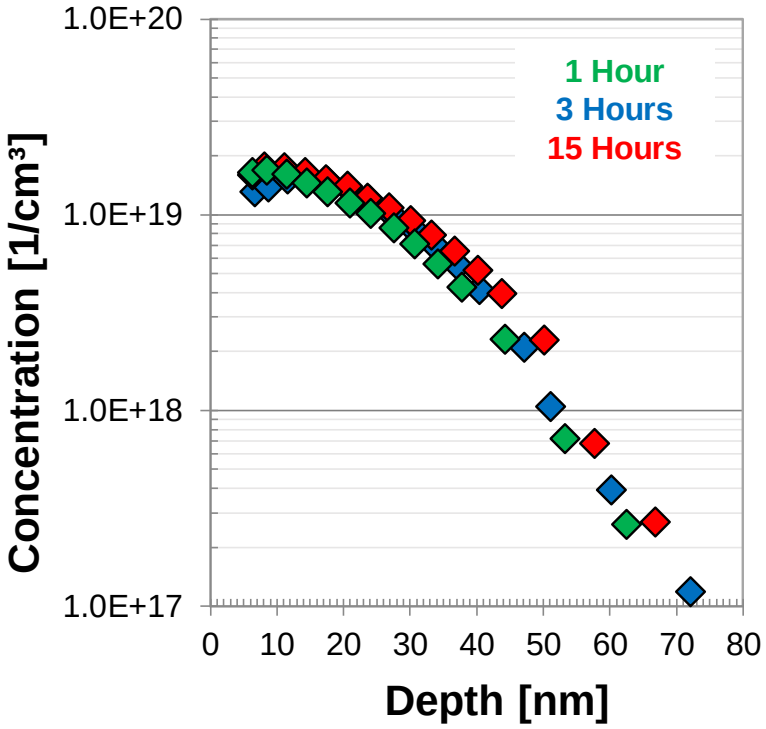


Figure 3.2*:* ECV plot of active carrier concentrations using bulk Si samples to analyse the impact of reaction time with a fixed reaction temperature of 180 °C. A 50 nm sputtered SiO_2 cap and 1050 °C 5 second anneal was used for all samples

3.4.1.1.2 Reaction temperature

A variation of reaction temperature (80 →120 →165°C) with a fixed reaction time of 3 hours was carried and the results were again probed using ECV (**Figure 3.3**). As mesitylene was used as the reaction solvent the highest temperature the reaction could be carried out at was its boiling point (*i.e.* 165°C). The Arrhenius equation below defines the dependence of a chemical reaction rate constant on the temperature of the reaction:

$$k = Ae^{((-Ea)/(kB.T))}$$

where k is the reaction rate constant, A is the pre-exponential factor, E_a is the activation energy for the reaction, kB is the Boltzmann constant and T is the reaction temperature.

This well-known equation demonstrates an exponential relationship between the reaction rate constant and the temperature used. ECV data gives a demonstration of this reliance with lower carrier concentrations seen when the reaction is carried out at temperatures of 80 °C and 120 °C. At reflux, the results, as measured by ECV lead to higher dose incorporation, indicating that there was better coverage of ADP at this temperature.

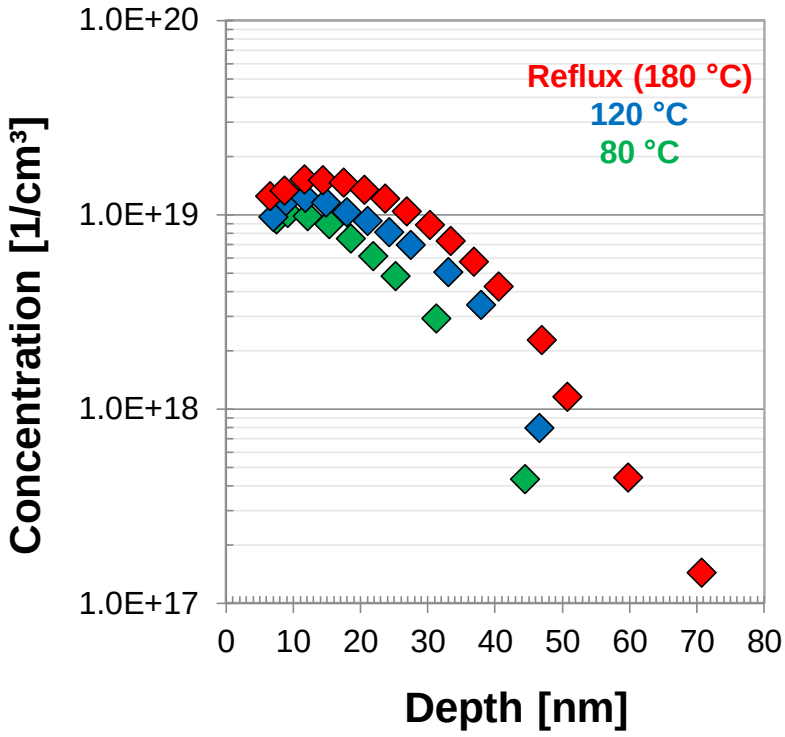


Figure 3.3: ECV plot of active carrier concentrations using bulk Si samples to analyse the impact of reaction temperature with a fixed reaction time of 3 hours. A 50 nm sputtered SiO_2 cap and 1050 °C 5 second anneal was used for all samples

3.4.1.1.3 Molecule concentration

The concentration of ADP was changed (0.01 →0.10 →1.00 mol L^{-1}) to see if this would have an impact on the final coverage, as tested by dose incorporated. This test was carried out at constant time and temperature (reflux ≈165 °C for 3 hours). The

ECV curves in **Figure 3.4** demonstrate that there is little or no reliance on the concentration of the molecule for the resulting activation levels in the concentration window that was tested.

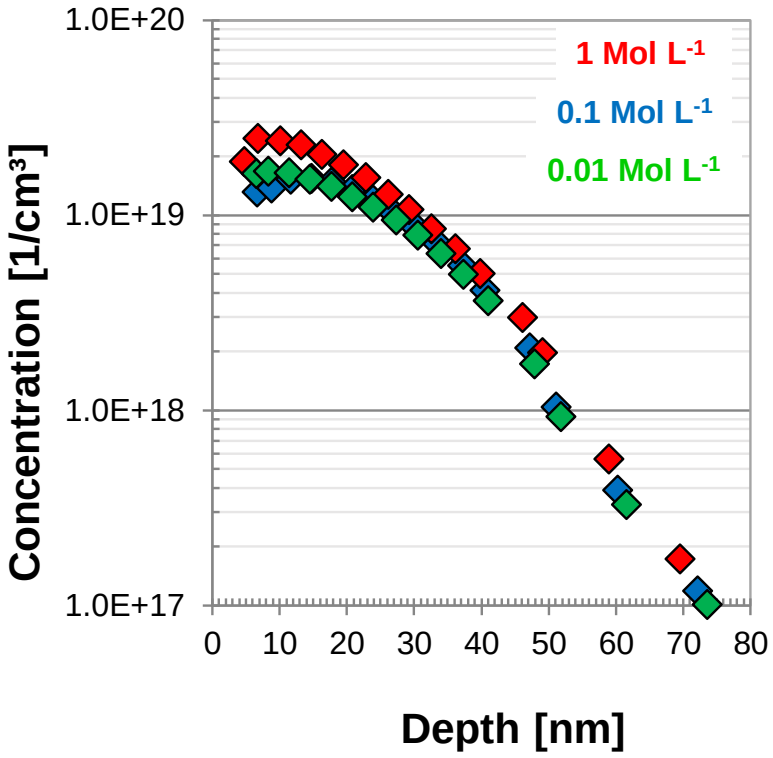


Figure 3.4: ECV plot of active carrier concentrations using bulk Si samples to analyse molecule concentration variation during functionalization. A 50 nm sputtered SiO_2 cap and 1050 °C 5 second anneal was used for all samples

3.4.1.2 Optimization of annealing conditions

3.4.1.2.1 Annealing temperature

MLD can be described as a limited source diffusion method of doping. To further probe the diffusion properties of P-MLD, a series of RTA temperature and time skews were conducted. The samples were characterised by ECV and validated using SIMS. While ECV gives the concentration of activated dopant, SIMS will give the total chemical concentration of in-diffused dopant. **Figure 3.5** shows that both SIMS and

ECV measure maximum concentration levels of $\approx 2 \times 10^{19}$ atoms cm^{-3}, when the top 2 nm of SIMS data is disregarded. Decreasing the RTA temperature leads to the expected drop in diffusion/activation of P dopant atoms. The maximum RTA temperature used in this study of 1100 °C shows that there is increased diffusion when compared with an annealing temperature of 1050 °C but no increase in maximum activation levels.

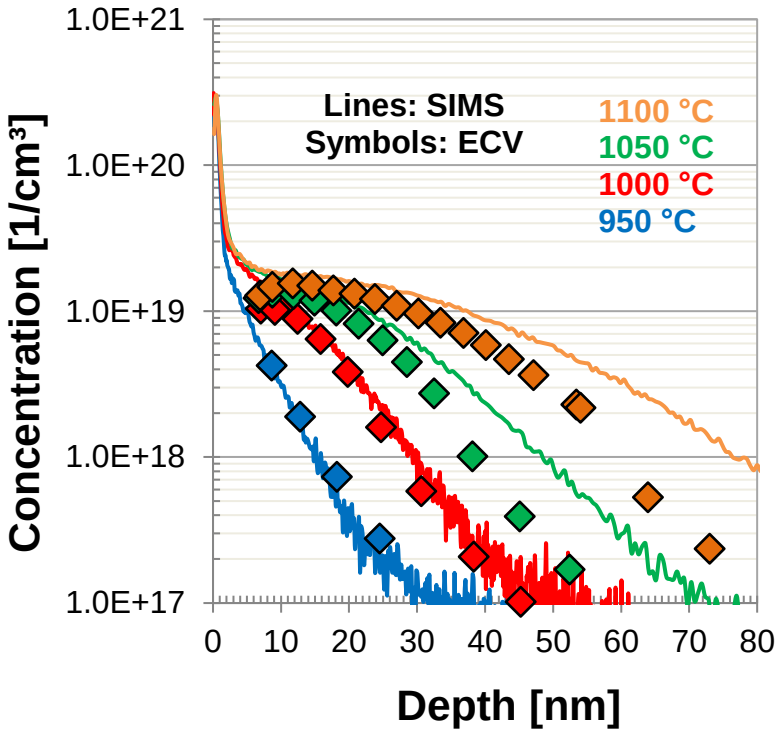


Figure 3.5: SIMS and ECVS plots of P-MLD doped samples with a SiO_2 capping layer. RTA time has been kept constant at 5 seconds while temperature has been varied from 950 – 1100 °C.

From the data shown in **Figure 3.5** it was possible to compare the total chemical dose (SIMS) and total active dose (ECV). Dose values from both characterisation methods were calculated through integration of the area under each dopant profile. This allowed the calculation of the percentage of P which has been ionized into substitutional

positions and activated in the semiconductor lattice, relative to total P incorporated. Trends shown in **Table 3.1** demonstrate that temperatures above 1000 °C lead to increased ionization of P dopant atoms. Increasing the anneal temperature leads to an increase in the achievable active carrier concentration which may in itself explain why a greater percentage of P is ionized at higher anneal temperatures. However, it is also possible that C-related defects that are known to deactivate P dopants, are removed with higher anneal temperatures. This is further be probed in section 3.4.1.2.2 where RTA time is varied.

RTA time (°C)	SIMS dose excluding top 2 nm (cm^{-2})	ECV dose (cm^{-2})	Ionization %
950	1.3×10^{13}	5.25×10^{12}	40.4
1000	3.1×10^{13}	1.76×10^{13}	56.8
1050	5.21×10^{13}	3.1×10^{13}	59.5
1100	8.25×10^{13}	5.15×10^{13}	62.4

Table 3.1: Calculation of ionization % from P-MLD doping with SiO_2 cap, a 5 second anneal time, and varied anneal temperatures

3.4.1.2.2 Annealing time

Variation of the RTA time at a constant temperature of 1050 °C allowed for further examination of the diffusion properties of P. The plots shown in **Figure 3.6** do not follow the expected trend of limited source diffusion but instead shows more similarity with constant source diffusion. Once again, the maximum concentration values are seen at $\approx 2 \times 10^{19}$ atoms cm^{-3} in both the SIMS and ECV data. The annealing time of

100 seconds is sufficient to incorporate the maximum surface dose value of 2×10^{14} atoms cm^{-2} but shows significant diffusion of dopants into the bulk of the semiconductor. This indicates that the shorter anneal times do not represent sufficient thermal budgets to incorporate the total dose. This represents a form of "hourglass diffusion" whereby some inhibiting factor appears to be preventing the achievement of increasing dopant concentration levels and matching the expected limited source diffusion.

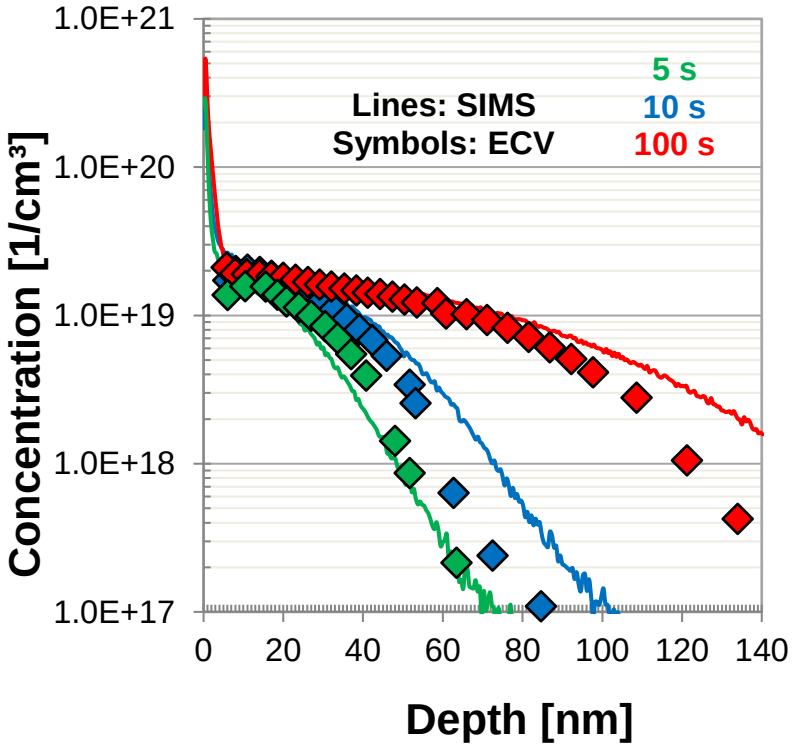


Figure 3.6: SIMS and ECVS plots of P-MLD doped samples with a SiO_2 capping layer. RTA temperature has been kept constant at 1050 °C while varying time from 5-100 seconds.

Looking at the total dose values incorporated during the 100 second anneal provide information about the coverage of ADP achieved. Materials studio modelling of its molecular dimensions estimate a molecular footprint of ≈ 1.1 x 0.8 nm. Estimating

maximum "ideal" surface coverage with this size leads to a value of $\approx 1.5 \times 10^{14}$ atoms cm^{-2} which agrees with findings from SIMS and ECV.

RTA time	SIMS dose excluding top 2 nm (cm^{-2})	ECV dose (cm^{-2})	Ionization %
5 seconds	5.21×10^{13}	3.1×10^{13}	59.5
10 seconds	9.9×10^{13}	6.7×10^{13}	67.5
100 seconds	1.8×10^{14}	1.3×10^{14}	71.1

Table 3.2: Calculation of ionization % from P-MLD doping with SiO_2 cap, 1050 °C anneal temperature, and varied anneal times

The ionization % trend also provides insight into the activation process of P dopants introduced from MLD. There is an increase in the ionization % of P dopants with increasing annealing time from 5 seconds up to 100 seconds. Two scenarios may explain this increase in ionization. 1) It has been found by Gao *et al*, [18] that longer low temperature anneals prove successful in lowering the impact of carbon contamination on the activation of P from MLD. Although this case does not represent low temperature conditions it is possible that a similar effect has been seen. 2) Both ECV and SIMS struggle to characterize the near surface region (top ≈2 nm). With increasing depth of diffusion, it would be expected to improve the accuracy of the measurement. It is possible that the 5 second data point suffers from this inaccuracy to a greater extent than the 10 and 100 second anneals.

3.4.1.3 Necessity of capping layer?

3.4.1.3.1 Carrier profiling

Tests were carried out to determine whether a capping layer was necessary, to achieve higher dopant incorporation, for MLD using standard processing conditions but with and without an SiO_2 capping layer. **Figure 3.7** clearly shows that when a capping layer is used the maximum active carrier concentration is an order of magnitude higher then when no cap is used. It is presumed that in the absence of a capping layer that much of the ADP monolayer is lost to the annealing chamber.

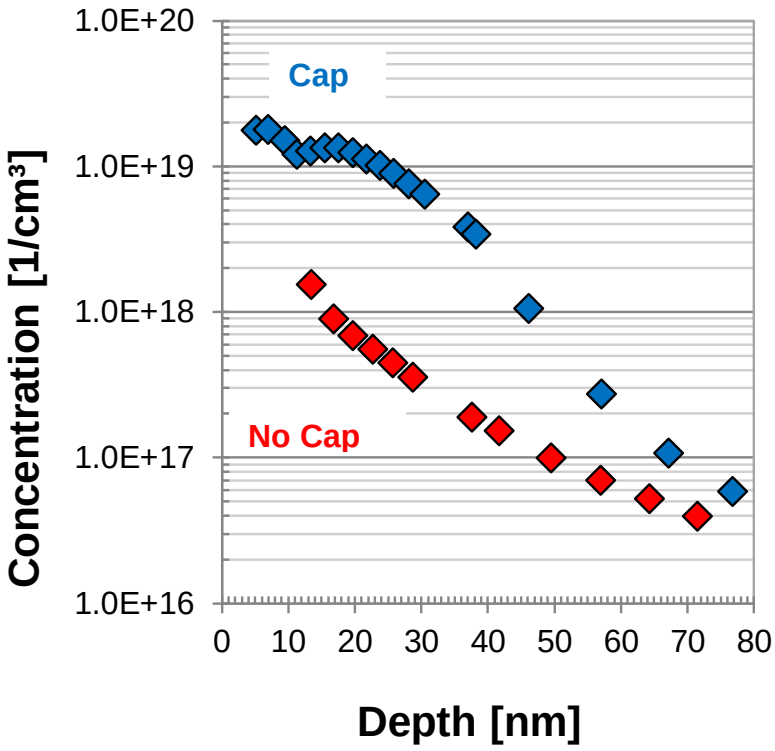


Figure 3.7: Electrochemical capacitance-voltage profile showing the impact of applying a SiO_2 capping layer for the duration of the annealing process. Both samples were annealed at 1050 °C for 5 seconds.

3.4.1.3.2 AFM analysis

AFM was used to evaluate the impact of the various MLD processing steps on surface roughness. This is a critical issue to consider, as MLD is designed for sub-10 nm structures, where any appreciable increase in surface roughness could destroy the structures or at least severely hamper their performance. Increased surface roughness can also impact processing such as metallisation which would be subsequent to doping in device processing Root mean squared (RMS) is used as an indication of the surface roughness value across the 3x3 μm measurement area. **Figure 3.8** shows surface quality of the blanket Si wafers after each MLD processing step. Initial as-received samples show high quality with an RMS value less than 0.1 nm. Cleaning the samples with IPA and acetone does not affect the RMS which indicates that the cleaning and sonication step does not cause any damage. Prior to functionalisation the native oxide must be removed by treating with HF. **Figure 3.8 (c)** shows a negligible increase in the surface roughness. Finally, after undergoing all the processing steps of MLD the RMS value of 0.29 nm demonstrates the gentle nature of the process. To compare this value to previous literature, the TAA MLD process developed my O'Connell *et al* showed an increase in RMS from 0.1 nm to 2 nm.[26]

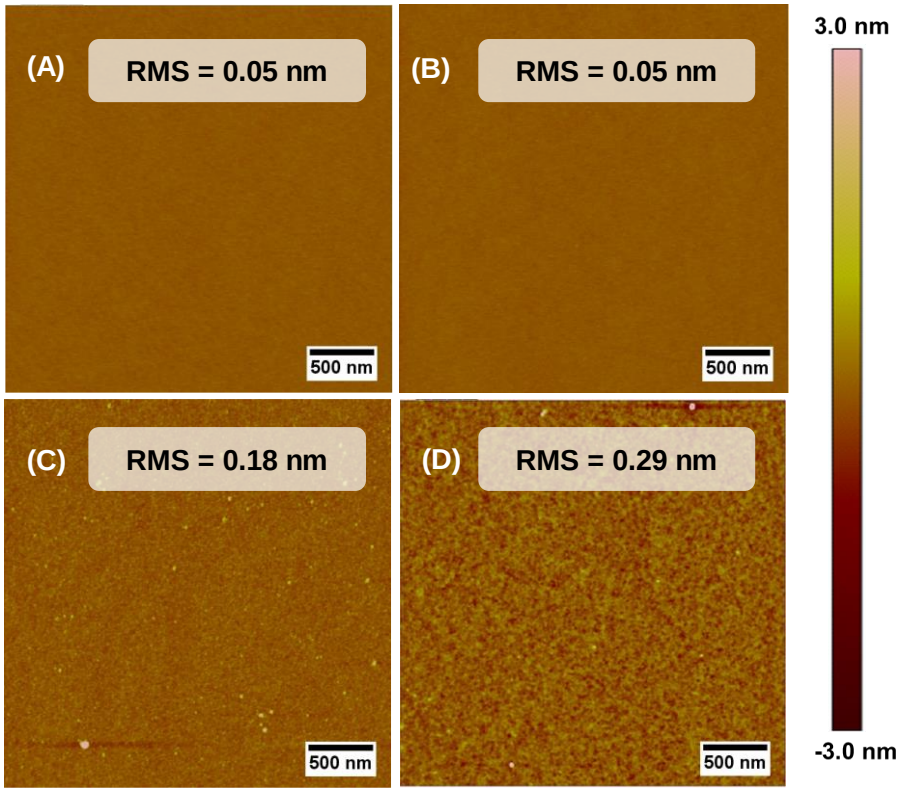


Figure 3.8: Atomic force microscopy of (A) as received Si (B) chemically cleaned Si (C) hydrofluoric acid dipped Si and (D) fully processed Si after P-MLD

3.4.2 Application to SOI

The optimised process for P-MLD on blanket Si was transferred to two SOI substrates, 13 and 66 nm thicknesses. These samples were analysed using AFM, XPS, ECV and Hall-effect as outlined in the following sections. A further study on SOI thickness down to sub-5 nm values was conducted with a brief summary outlined below. **Figure 3.9** provides a general schematic for P-MLD processing on SOI with a similar process flow to what was shown on blanket Si.

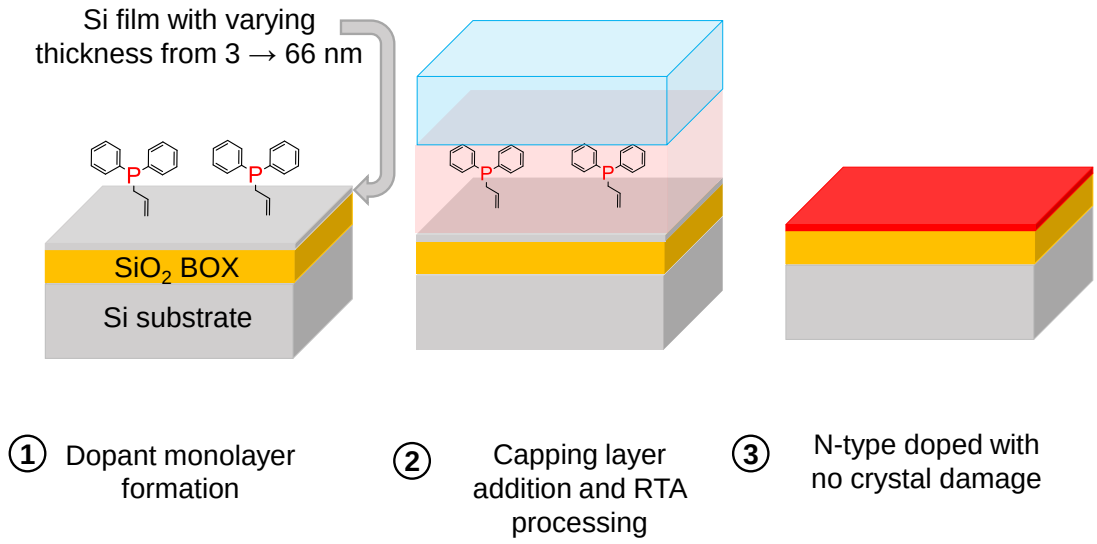


Figure 3.9*:* General schematic depicting P-MLD processing on SOI. SOI wafers were comprised of Si thicknesses varying from 3 → 66 nm, over a SiO_2 buried oxide layer (BOX) which is atop a Si substrate.

3.4.2.1 Material Characterization

3.4.2.1.1 AFM analysis

P-MLD processing was initially carried out on 66 nm SOI. AFM analysis of the starting SOI substrate and samples post-MLD processing follow a similar trend, as expected, to what was seen on blanket Si wafers (**Figure 3.10**) with a slight increase in surface roughness after all the processing steps have been completed.

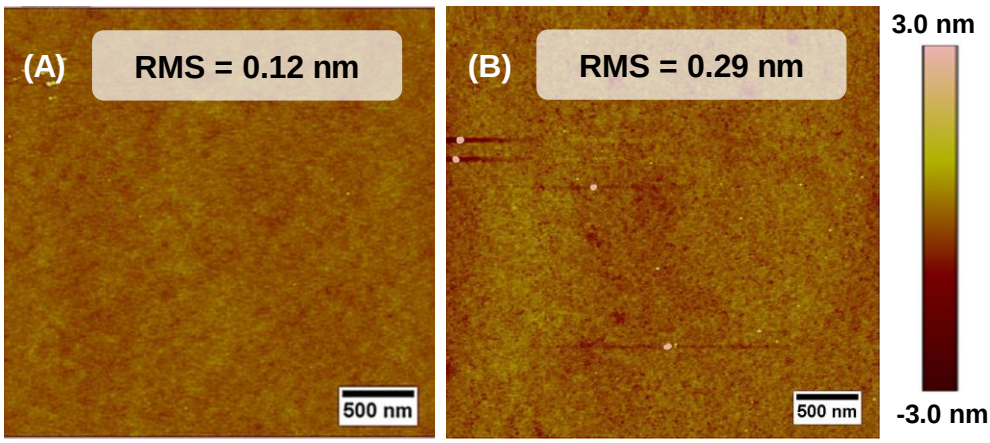


Figure 3.10*:* AFM images of (A) as received SOI and (B) SOI after P-MLD processing

3.4.2.1.2 ECV analysis of P-MLD doped 66 nm SOI

Active carrier concentration levels, as measured by ECV, shown in **Figure 3.11,** approach 2×10^{19} atoms cm^{-3} which correlate with results seen during the initial tests carried out on bulk substrates. ECV encounters difficulty when approaching the insulator layer of the SOI sample due to the voltage etching mechanism employed on n-type doped Si. Applying a voltage near the insulator layer becomes problematic and prevents uniform etching and analysis in this region as the etching mechanism near insulator layers is known to have faster etching rates at the edges of the etch pit than in the centre. This phenomenon, which occurs in the ≈ 15 nm approaching the insulator layer, makes the 13 nm substrates unsuitable for ECV analysis. A more detailed description of ECV characterisation and the issues when applying the technique to SOI is provided in Chapter 2 section 2.1. For this reason, Hall Effect measurements were employed to determine carrier concentration levels of thinner SOI layers.

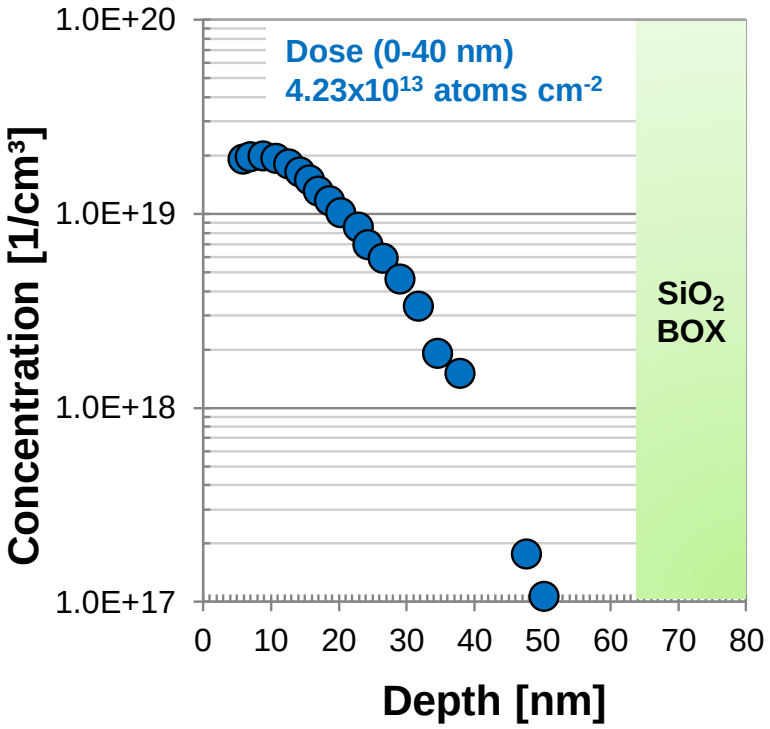


Figure 3.11: ECV plot of active carrier concentrations in a 66 nm SOI after MLD using a 50 nm sputtered SiO_2 cap and a 1050 °C 5 second anneal

3.4.2.1.3 Electrical characterisation of P-MLD doped SOI using Hall-effect measurements.

A summary of the key data found from Hall-effect analysis is shown in **Table 3.3.** Sheet carrier concentration (CC) values, from AC mode, are virtually the same for both the 13 and 66 nm substrates. This is due to the overall dose available being limited by surface coverage of the ADP dopant molecule. Consistent dose values produced by MLD are desirable when compared with fluctuations seen using other techniques. However, the volume of the 13 nm samples is significantly less than the 66 nm sample which leads to a higher carrier concentration (CC,n) which is a very positive outcome

(concentration = dose/thickness). As a result of this increased carrier concentration the mobility drops which is as expected for Si.

Property	Units	66 nm sample	13 nm sample
Mobility μH	$cm^2/(V.s)$	125.72	61.79
Sheet CC	$1/cm^2$	$2.3x10^{13}$	$2.26x10^{13}$
CC, n	$1/cm^3$	$3.49x10^{18}$	$1.74x10^{19}$

Table 3.3: Hall-effect data from 66 nm and 13 nm MLD doped SOI

3.4.2.1.4 XPS characterization

MLD is a surface diffusion technique meaning that the dopant source is applied to the surface of the substrate and requires further thermal treatment to both promote diffusion into this substrate and to electrically activate. Although this process sounds trivial, there are numerous issues which can arise and prevent the movement of the dopant into the target area. In the case of Si doping one of the most prominent issues is SiO_2 formation at the surface. P diffuses through SiO_2 at a rate significantly slower than through Si.[19, 20] The quoted nitrogen ambient diffusivity value for P in Si (intrinsic = 3.85 cm^2 s^{-1}) is at least 20 times higher than the value associated with P in SiO_2 (Phosphosilicate glass = 0.185 cm^2 s^{-1}).[21] Although it has been shown that H-terminated Si re-oxidizes relatively slowly when stored at room temperature in air, the elevated temperatures required for MLD processing carried out in the liquid phase enhances this re-oxidation.[9] Therefore, precautions are taken to ensure minimal possibility of re-oxidation, solvents are thoroughly degassed, and processing is carried out in a nitrogen environment using a Schlenk line. **Figure 3.12** shows XPS analysis

of the Si 2p signal which is used to evaluate SiO_2 presence via the shoulder at ≈ 103 eV. The pass energy used in this study demonstrates a classical asymmetric peak for the overlapping Si $2p_{1/2}$ and Si $2p_{3/2}$ orbitals both of which represent elemental Si. In this set of samples (A) is as received Si, (B) freshly HF dipped (T = 0 hours) and (C) Si which has been HF dipped and stored in ambient conditions for four days (T = 96 hours). It is evident that treating the sample with HF removes the SiO_2, clear by the absence of a peak at 102.5 eV, but storage in ambient results in re-oxidation of this surface to a condition similar to that of the as-received sample.

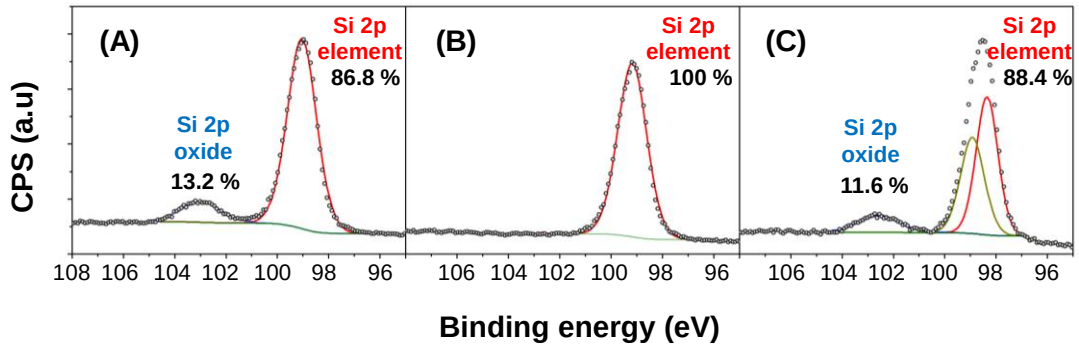


Figure 3.12: Si 2p signal from XPS of (a) as-received (b) HF treated dipped (c) HF dipped t = 96 hours left in ambient

XPS analysis of samples during the P-MLD functionalization process, shown in **Figure 3.13**, indicates that surface oxidation had taken place during the functionalization step even with the diligent removal of all possible drivers of this oxidation. It is possible to surmise that even this small amount of SiO_2 has the ability to inhibit P diffusion into the Si substrate. The stability of this monolayer functionalized sample is evidenced by the fact that the there is no change, within experimental error, in the amount of SiO_2 over 96-hour period of exposure to ambient conditions.

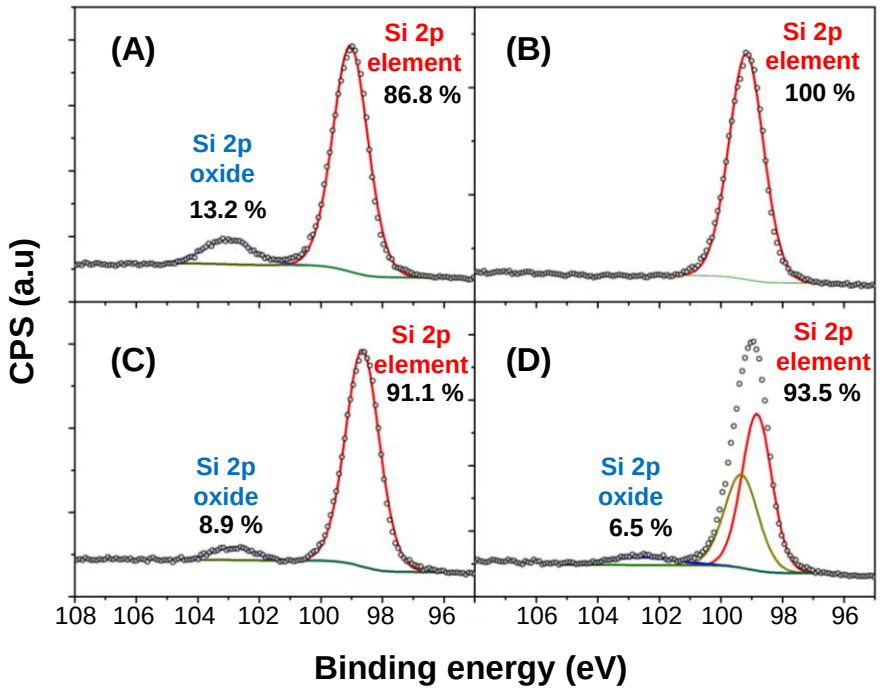


Figure 3.13*:* Si 2p signal from XPS of (a) as-received (b) hf dipped (c) ADP functionalised t= 0 hours and (d) ADP functionalised t = 96 hours

3.4.2.1.5 Angle resolved XPS characterisation of ADP on Si.

A higher resolution XPS tool (details in Chapter 2 section 2.3) was used for angle-resolved XPS (AR XPS) of ADP functionalised Si samples. This enables a direct method to observe the presence of P, which has previously been used by Gao *et al.*,[22] in the ADP monolayer.

Figure 3.14 shows AR-XPS analysis of P on as-received Si and ADP functionalized Si for P-MLD. The as received sample shows no significant change in peak shape when moving from 0 ° to 75 ° take off angle as in theory there should be no overlayer covering the Si substrate. The ADP functionalized sample does show an evolution of the P 2s signal when moving from 0 ° to 75 ° take off angle with a higher peak seen than the Si plasmon peak in the 75 ° spectra. Increasing the take-off angle leads to a

more surface sensitive analysis and therefore it goes as expected that the surface P containing monolayer makes up a larger contribution of this signal.[22]

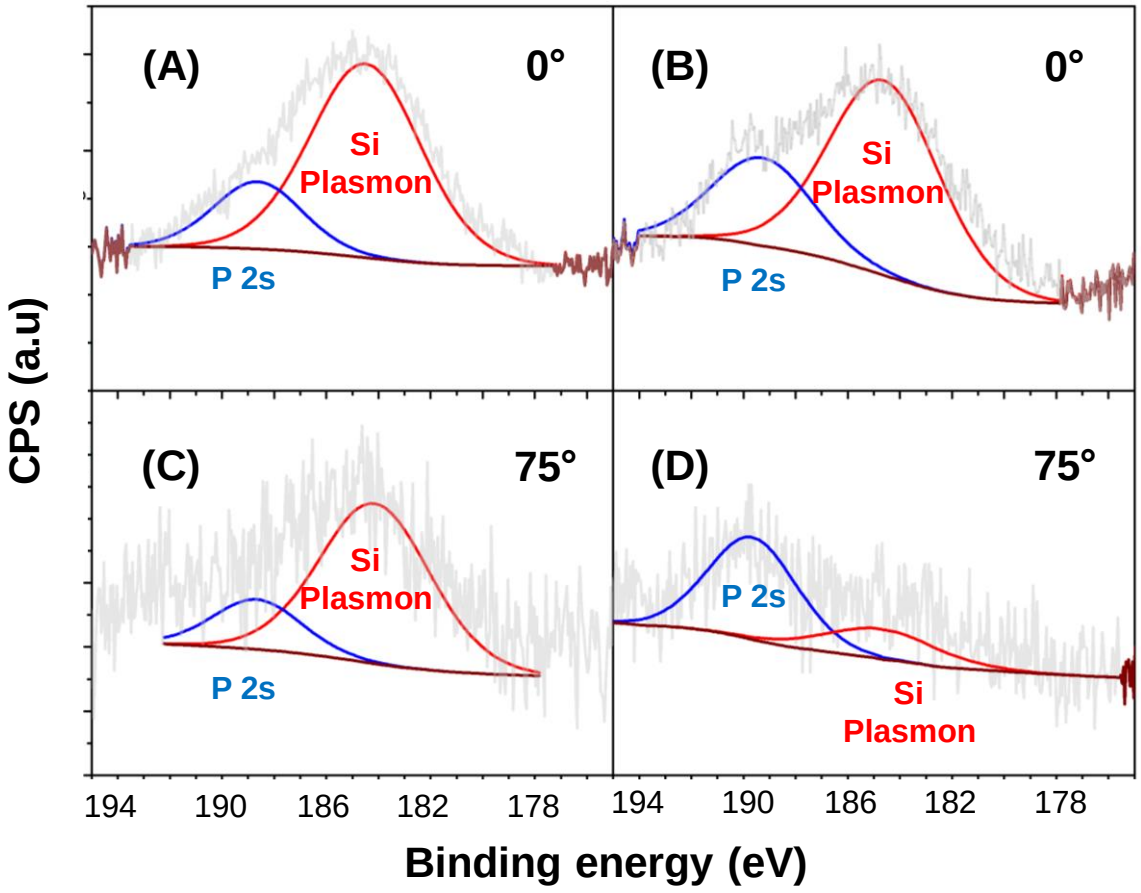


Figure 3.14: AR XPS analysis of P presence after ADP functionalization. (A) and (C) are as-received Si at 0 ° and 75 ° respectively. (B) and (D) are ADP functionalized Si at 0 ° and 75 ° respectively.

3.4.2.1.6 Interface trapping of dopants analysed with SIMS

66 nm SOI, which had undergone MLD, was further examined using SIMS to assess the chemical concentration of dopant that had been achieved. Data shown in **Figure 3.15** correlates well with Hall-effect and ECV shown previously, with P concentration levels of $2x10^{19}$ atoms cm^{-3} from 2 nm onwards, indicating that all the dopant that has been driven in has been electrically activated. The maximum levels of dopant found from SIMS were in the first 2 nm with values approaching 3×10^{20} atoms cm^{-3}. One

possible reason for these elevated values may be dopant trapping by SiO_2 during the annealing process. The surface oxidation found after functionalization (**Figure 3.13**), and use of SiO_2 as a capping layer, have the potential to inhibit diffusion into the substrate. Other research groups,[8, 9] working on P diffusion doping using a variety of techniques have also seen limitations at $2x10^{19}$ atoms cm^{-3}. This leads us to believe that the presence of SiO_2 near the sample surface may be inhibiting the in-diffusion of the P dopant atoms.

The final noteworthy aspect of this SIMS profile is the peak seen at the Si/insulator interface. A spike in P concentration is seen showing that it may also be trapped at this point in the substrate. This build up at the interface can be explained by the fact that there is slower diffusion of P in SiO_2 when compared to Si. A similar feature has previously been seen with ion implantation on SOI substrates.[23] Previous work by Mastromatteo *et a*l,[24] examining P implantation of Si nanocrystals embedded into SiO_2 attributed a similar P peak to interface effects. In order to attain a more detailed understanding of this interface peak a more comprehensive study of this back interface would have to be undertaken.

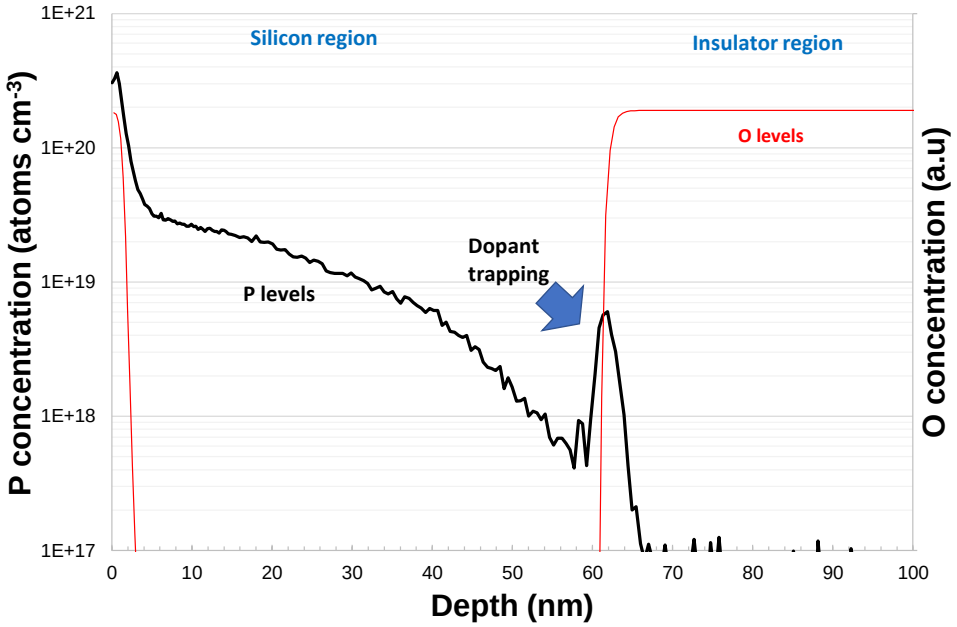


Figure 3.15: Secondary ion mass spectrometry analysis of P-MLD doped 66 nm SOI substrate. Blue line – P concentration. Red Line – O concentration.

3.4.2.1.7 Further work on SOI

A further extensive study was carried out to determine the impact of decreasing SOI thickness on conductivity. This study benchmarked P-MLD processing versus rival doping technologies, beam-line implantation, and MOVPE gas phase doping. Beam line implantation conditions used were a P 2keV energy, 1 x10^{15} atoms cm^{-2} dose, 7° tilt angle, at room temperature.

The standard wet chemistry P-MLD processing was also applied to the substrates shown below in **Figure 3.16** for this study. A novel functionalization method through the vapour phase was also demonstrated as part of this study.

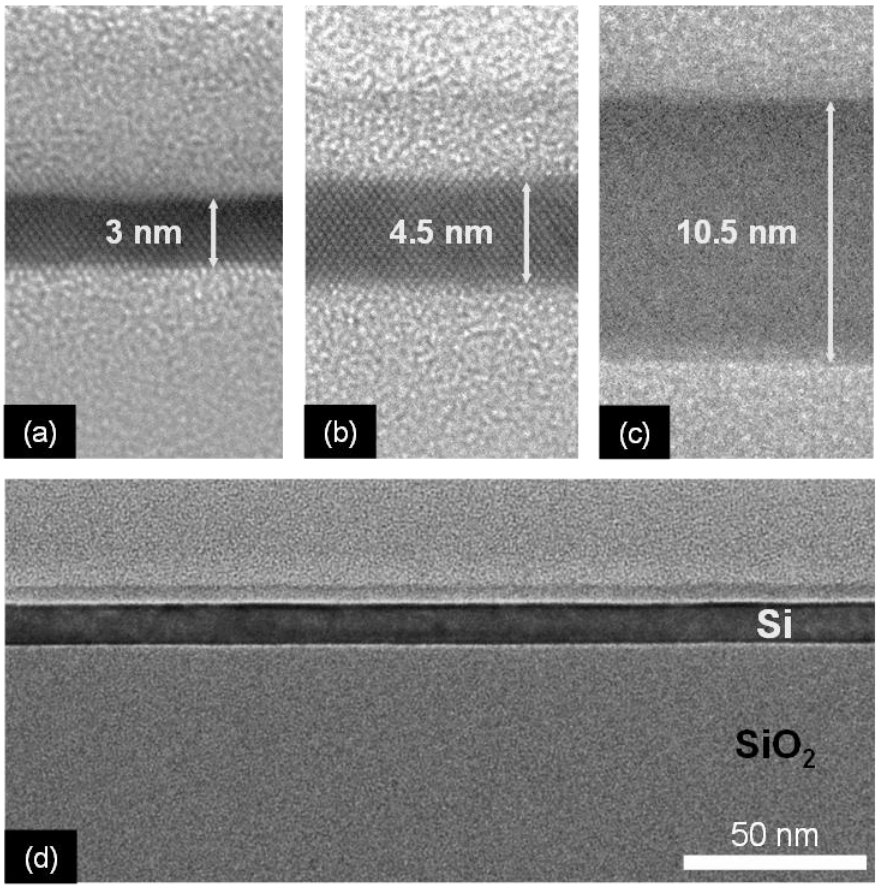


Figure 3.16: Cross-section transmission electron microscope images of SOI with film dimensions shown down to 3 nm. Image (dff) also shows a wider view of the buried oxide layer

MLD doped samples were electrically characterized by means of C-TLM and micro-4-point probe which provide complementary analysis to hall effect used in the previous work.

C-TLM data shown in **Figure 3.17** compares MLD with the rival doping methods at SOI thickness down to the 3 nm mark. Resistivity values for MLD are higher than those seen in beam-line implanted samples which is as expected given that activation values from ECV show that P-MLD does not exceed 2 $x10^{19}$ atoms cm^{-3} whereas beam-line approaches $1x10^{20}$ atoms cm^{-3}. Favourable resistivity values were documented for MLD in comparison to MOVPE doping with arsine which also

requires further development before being capable to rival implant for industry applications. This further highlights the need for MLD to overcome the 2 x10^{19} atoms cm^{-3} barrier in order to compete industrially.

This study also demonstrated that achieving measurable resistance values below SOI film thickness of 4.5 nm proves difficult for all doping methods, which provides evidence to the theory that dopant incorporation in sub 5 nm dimensions may require alternative methodology. This roadblock may be overcome by future annealing or dopant delivery methods.

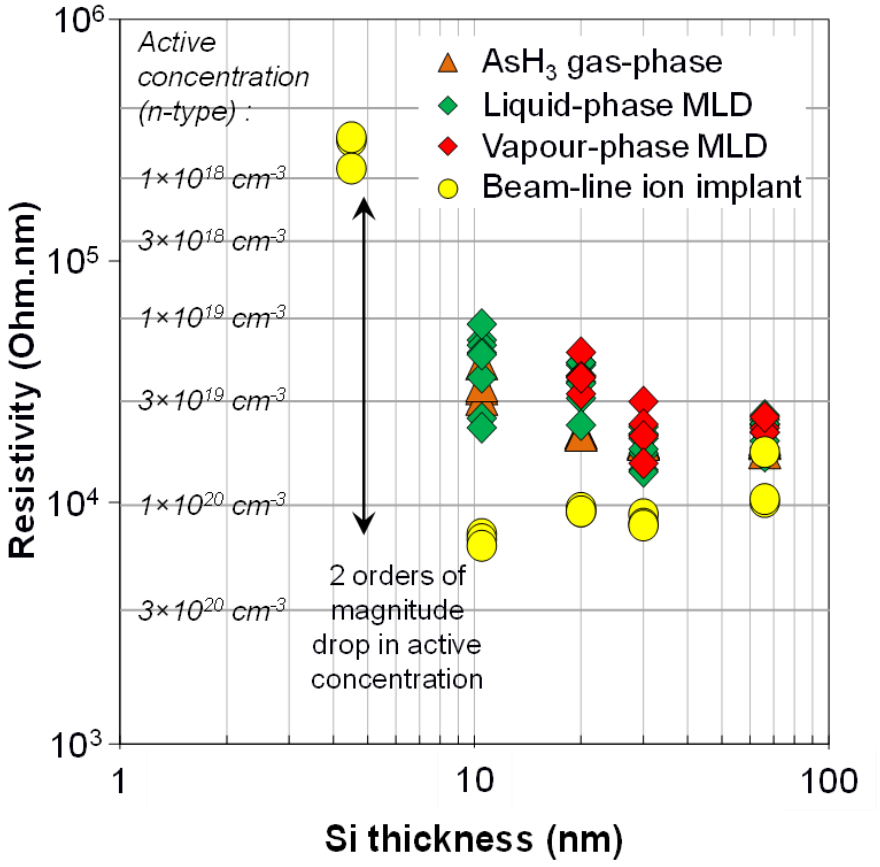


Figure 3.17*:* Resistivity vs SOI thickness for P-MLD with an SiO_2 cap and 1050 °C 5 second RTA. Rival doping techniques beam line implant, and MOVPE gas phase doping, are also analysed and compared.

3.4.3 Application to Nanowires

Nanowire structures provide a test structure which enable development of processes for future GAA devices. They are a valuable method of assessing whether MLD is capable of competing with rival doping technologies. This section demonstrates the application of MLD to nanowire substrates, with material characterisation using SEM and XTEM, followed by electrical characterisation. The optimized P-MLD processing parameters developed on blanket Si were applied to the nanowire samples used in this study. **Figure 3.18** depicts the P-MLD on Si nanowire process flow with (1) monolayer formation followed by (2) capping and RTA and (3) cap removal after which a conformally doped nanowire structure with no crystal damage is produced.

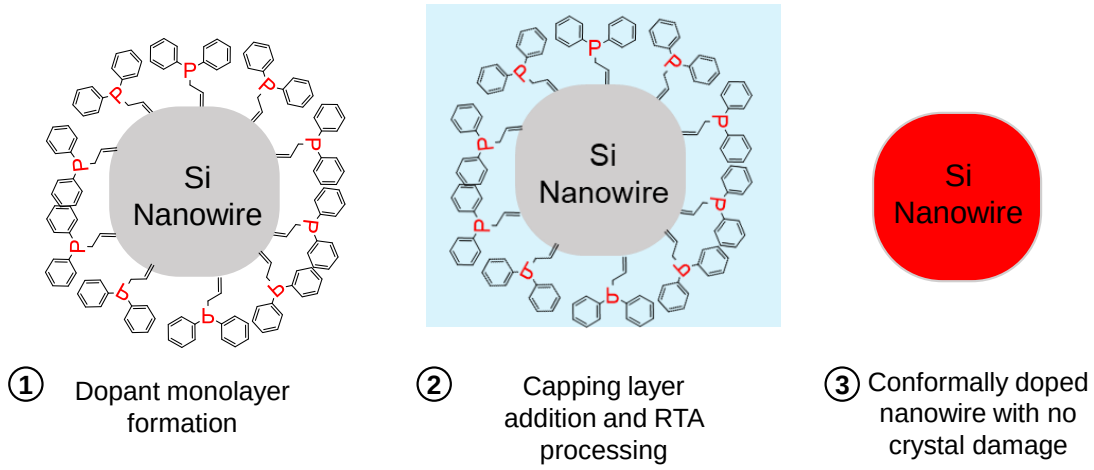


Figure 3.18: General schematic depicting P-MLD processing on nanowires.

3.4.3.1 Material characterisation of test structures

3.4.3.1.1 Scanning electron microscopy

Development on blanket structures is a useful method of optimizing a process for transfer to 3-D structures. Current logic devices utilize either SOI or high aspect ratio finFET architectures with an emphasis on research and development to produce

solutions for future GAA structures. In order to fully understand the applicability of P-MLD to current and future logic solutions it was essential that 3-D structures in the form of nanowires were examined. Examining these nanoscale 3-D structures proves difficult from a metrology perspective with standard tools for planar Si becoming redundant (ECV, AFM etc). SIMS of nanowires has previously been shown but suffer from a number of effects which bring into question the accuracy of the technique. [25]

A typical SEM of a nanowire test structure used in this study is shown below in the **Figure 3.19**. This consists of two metal contact pads deposited on two contact sections of the Si structure which are linked by the Si nanowires. Test structures were fabricated for this study with a variety of widths, lengths and spacing. This allowed for extraction of contact resistance and nanowire resistance with the ultimate aim of calculating resistivity. A detailed methodology for nanowire fabrication has previously been described in publication and in section 3.3.3 of this thesis.[17]

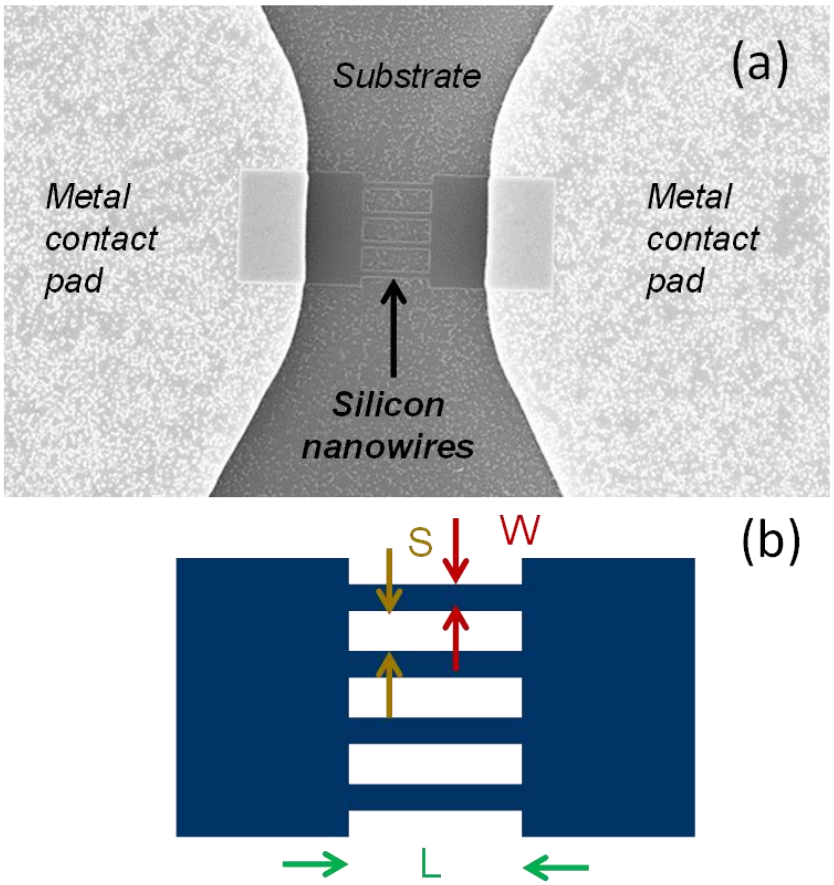


Figure 3.19: (A) Scanning electron microscopy image of a typical nanowire test structure used in this study. (B) Schematic describing the nanowire dimensions which were varied across the 196 test structures per sample. S = spacing, W = width and L = length.

3.4.3.1.2 XTEM

TEM analysis of samples which had been doped through the respective doping technologies gives evidence of the non-destructive nature of MLD which is contrasted by the destructive nature of ion implantation. Shown in **Figure 3.20**, extensive crystal defects remain after RTA in the implanted sample. The top corners of the implanted fin also show the physical impact that implant has on fin dimensions. This sputtering caused by the high energy incident P ions has rounded the fin corners, which has not occurred in the gentler MLD processing.

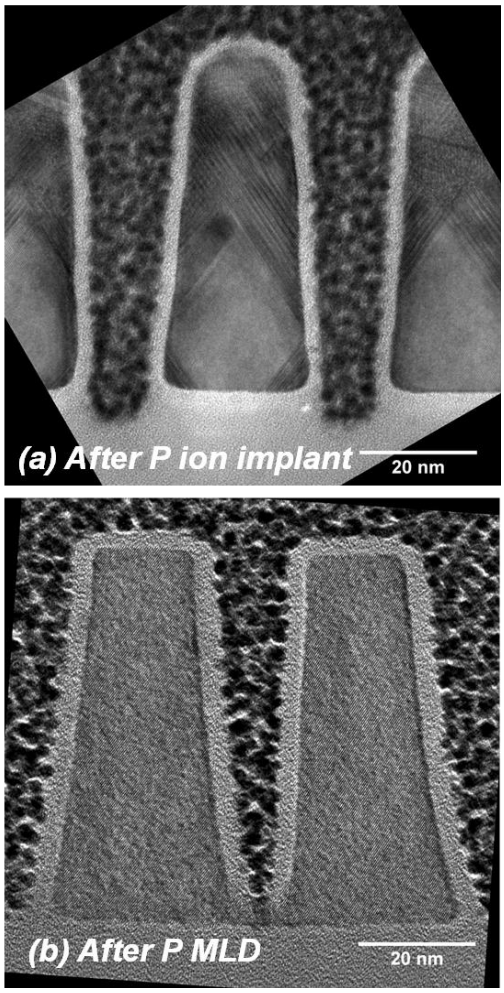


Figure 3.20: Cross section transmission electron microscopy images of nanowires doped by (a) ion implantation and (b) MLD. Crystalline defects are evident in the P-implant sample which are not seen in the MLD sample.

3.4.3.1.3 Carrier profiling of reference blanket samples

Similar to the work on SOI, a reference beam-line ion implanted sample was used to provide a comparison for MLD data. ECV data shown in **Figure 3.21** demonstrates, that on blanket Si, beam-line implanted samples show significantly higher activation levels than the P-MLD samples.

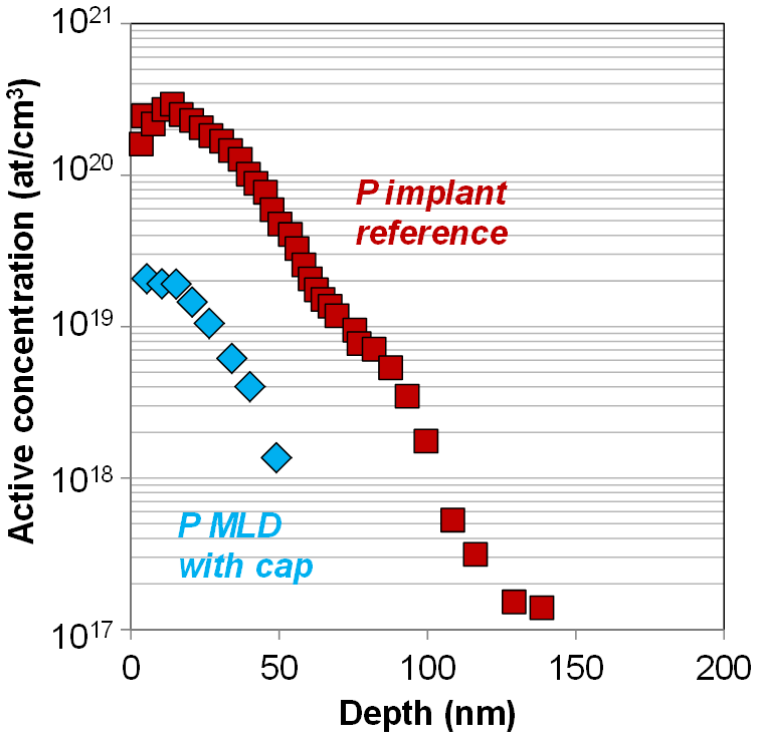


Figure 3.21: Electrochemical capacitance-voltage profiling comparison of the P implant reference sample with a P-MLD doped sample used for this study

3.4.3.1.4 Electrical characterisation of nanowire test structures

P-MLD processing which had been developed on blanket Si was applied to these nanowire structures as described in the experimental section. A further variable which was probed in this study was the use of an additional RCA clean prior to the hydrofluoric acid dip. This clean has commonly been used in the semiconductor industry to remove organic contaminants and particles. Although this clean has proven beneficial for the semiconductor industry it was found that when utilized with MLD and nanowire devices that it led to significant device loss. **Figure 3.22** shows that when using an RCA clean with or without a subsequent capping layer the resulting devices are more likely to have higher total resistance than the scenarios where no RCA clean was carried out.

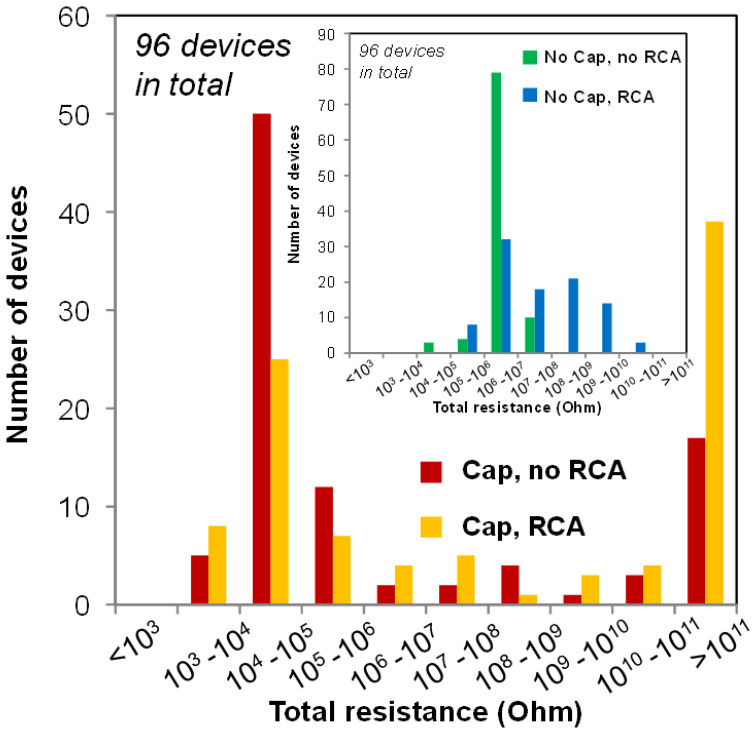


Figure 3.22: Number of devices versus total resistance in P-MLD nanowire devices. Variations in cap and the use of an RCA clean are indicated

The quantity of devices in the 10^3 – 10^5 Ohm range is considerably larger when utilizing a capping layer. This confirms results which had previously been shown on blanket Si that using a capping layer is necessary to achieve optimal doping results though MLD. For these reasons it was decided that P-MLD with a capping layer and no RCA clean would be taken as the optimal process for comparison with the P beam-line implant reference. The conditions for the P implant reference for this study were a 3keV energy, 4×10^{15} cm^{-2} dose at a tilt angle of 45 °.

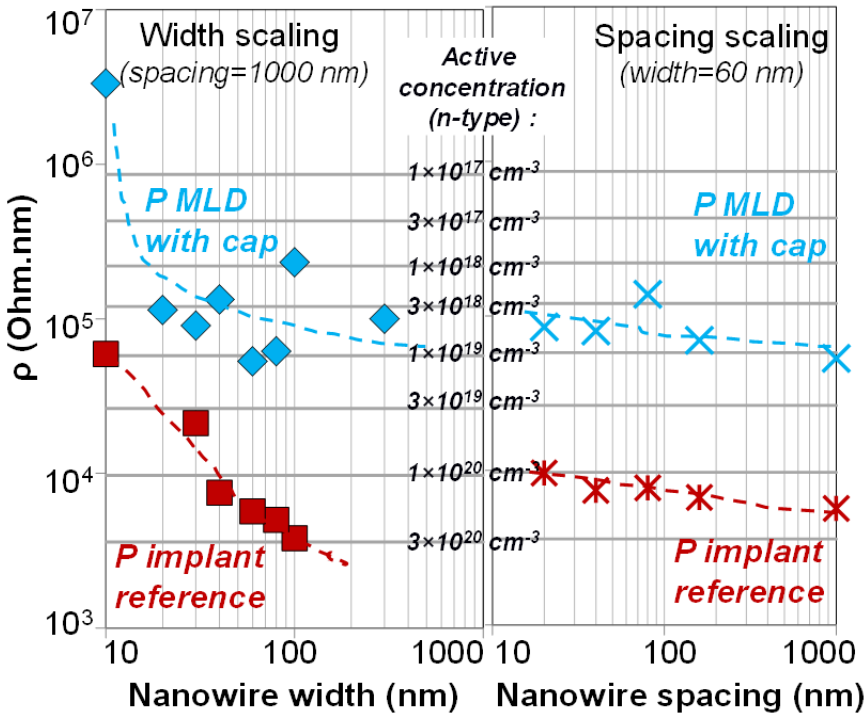


Figure 3.23: ECV plot of active carrier concentrations using bulk Si samples to analyse molecule concentration

Resistivity values from MLD and beam-line implant doped nanowires of various widths and spacings are shown in **Figure 3.23**. This data confirms previous findings on blanket Si and SOI that P-MLD produces doping levels an order of magnitude lower than beam-line implantation which is seen in the resulting higher resistivity values of MLD samples. It is noticeable that MLD does not suffer from the same rate of increase in resistivity, with decreasing nanowire width that is seen in the P implant data set. Nanowire spacing down to 20 nm does not make a significant impact on the resistivity of either data set.

3.5 Conclusions and Outlook

The work in this chapter has provided a detailed understanding of P-MLD on Si substrates. Initial process development carried out on blanket Si determined the impact of various reaction and fabrication process steps on the resulting dopant incorporation/activation. A diffusion barrier related to presence of SiO_2 has been proposed as the reason for limitations seen at the 2 x10^{19} atoms cm^{-3} mark for P from MLD. The presence of this SiO_2 has been shown to occur during functionalization even with stringent efforts to utilize inert conditions. Further studies were carried out on SOI and nanowires to validate MLD as a doping technology with comparison to beam-line implantation. This study on SOI represents the first application of MLD to these substrates. Both substrate types demonstrated similar findings with MLD showing higher resistivity values than the beam-line implant reference sample. This correlates with ECV findings on blanket wafers which show activation levels in P implanted samples to be an order of magnitude (10^{20} atoms cm^{-3}) higher than MLD samples (10^{19} atoms cm^{-3}). In order for MLD to compete with implantation as an industrial alternative it is vital that higher activation levels are achieved. An outlook was taken from these findings that alternative methods of limiting SiO_2 presence would have to be found through functionalization or capping. It was also theorized that developing MLD methodology to incorporate arsenic as an alternative n-type dopant may allow for increased dopant incorporation. Chapter 4 describes efforts to push the limits of MLD on Si by addressing these points.

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Kennedy, M. N. 2020. Monolayer doping of bulk and thin body group IV semiconductors. PhD Thesis, University College Cork.

Please note that Chapter 4 (pp. 123-159) is unavailable due to a restriction requested by the author.

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CHAPTER 5

Monolayer doping of germanium with arsenic: A new chemical route to achieve optimal dopant activation

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Adapted from the following presentation and publications. As a result, sections such as introduction and abstract may contain repeating concepts. A comprehensive authorship contribution section is provided in **Chapter 8**:

Kennedy, N; Garvey, S; Maccioni, B; Eaton, L; Nolan, M; Duffy, R; Meaney, F; Kennedy, M; Holmes, J.D; Long, B. **Langmuir, (2020), 36, 34, 9993–10002**

5.1 Abstract

Reported here is a new chemical route for the wet chemical functionalization of germanium (Ge), whereby arsanilic acid is covalently bound to a chlorine (Cl) terminated surface. This new route is used to deliver high concentrations of arsenic (As) dopants to Ge, via monolayer doping (MLD). Doping, or the introduction of Group III or Group V impurity atoms into the crystal lattice of Group IV semiconductors, is essential to allow control over the electronic properties of the material to enable transistor devices to be switched on and off. MLD is a diffusion-based method for the introduction of these impurity atoms via surface bound molecules which offers a non-destructive alternative to ion implantation, the current industry doping standard, making it suitable for sub-10 nm structures. Ge, given its higher carrier mobilities, is a leading candidate to replace Si as the channel material in future devices. Combining the new chemical route with the existing MLD process yields active carrier concentrations of dopants ($>1 \times 10^{19}$ atoms/cm^3), that rival those of ion implantation. It is shown that the dose of dopant delivered to Ge is also controllable by changing the size of the precursor molecule. XPS data and DFT calculations support the formation of a covalent bond between the arsanilic acid and the Cl terminated Ge surface. AFM indicates that the integrity of the surface is maintained throughout the chemical procedure and ECV data shows carrier concentrations of 1.9×10^{19} atoms/cm^3 corroborated by sheet resistance measurements.

5.2 Introduction

The dimensions of CMOS components, *i.e.* transistors, have decreased over the decades from being in the order of micro to nano-metres in accordance with the prediction of Moore's law.[1, 2] The aggressive scaling down of transistors has placed demands on the engineering required to keep up with this, calling for dramatic alterations to the architectures of the devices as well as the processes such as doping, deposition, and lithography.[3, 4]

Ge is the most likely material to be used, together with Si, to improve the performance of future transistors. It offers the advantages of increased (2.7 time) electron and (4 time) hole mobility over Si[5] and their similarity (both are Group 4 elements) means it can be seamlessly integrated into a CMOS fabrication process utilising the same infrastructure. Alternative channel materials, such as III-Vs, would require new costly infrastructure and are considerably more expensive to produce and process than Ge.

One of the most fundamental processes in transistor fabrication is the introduction of impurity atoms into the semiconductor to allow them to function as switching devices. Beam-line based ion implantation has long been the industry leading method of carrying out semiconductor doping.[6] This is a process which involves bombarding the structure with dopant ions, a side effect of which is crystal damage. Larger and planar structures can be annealed at high temperature to restore the crystal integrity. However, in dimensions approaching sub-10 nm, ion implantation induces damage that cannot be reversed by annealing.[7] Furthermore, the directional nature of beam-

line implantation has significant issues when applying the technique to tightly pitched arrays of nanostructures. The nanostructures in these arrays create shadows which can lead to non-conformality, giving high variability in device characteristics, and poor dopant incorporation into the sidewalls.[8, 9] To address the issue of crystal damage, implantation development has moved from room temperature towards high temperature conditions known as hot implantation.[10-12] However, these do not address the issue of shadowing and non-conformality for arrays of nanostructures. An alternative to ion implantation, plasma doping, has been developed to address problems with directionality and crystal damage, but still has conformality issues.[13, 14] Nonetheless, with further device scaling, novel methods will be required for these advanced doping applications where ideally the solution will be capable of producing minimal crystal damage and a conformal doping without the directionality constraints.

Monolayer doping (MLD), first reported in 2008,[15] is a diffusion based, and therefore non-destructive method, for introducing dopants and has the potential to deliver conformal doping of nanostructures without issues of directionality. MLD is a deposition doping technique in which a controllable dose is provided through a self-limiting surface adsorbed monolayer of organic molecules containing the dopant atom. The self-limiting nature of monolayer formation allows for a controlled dose which is defined by the size of the molecular precursor. The dopant atoms are transported into the target structure via diffusion during an annealing step which causes the adsorbed molecule to decompose releasing the dopant. While, MLD has been well studied and used to dope Si,[16-23] silicon-germanium alloys,[24] and III-V's[25, 26] it has been less studied for Ge doping.[27-29]

Finding new methods to non-destructively dope Ge to the required dopant concentration is imperative given the use of Ge not only as the channel material in FETs, but also in other devices, which requires doping concentrations typically on the order of 1×10^{19} atoms/cm^3. The application of MLD to Ge doping with As is challenging but is worth investigating due to the controllable As diffusion and high solubility in Ge, while the diffusion of both boron and phosphorus (via MLD using conventional annealing) is too slow to achieve any meaningful doping.[30] Sgarbossa *et al* showed useful results for antimony (Sb) doping achieving a concentration of ~3×10^{18} atoms/cm^3 using conventional annealing.[28, 31] However when laser annealing was employed record levels of Sb (~1×10^{20} atoms/cm^3) activation were achieved and successful P (~2×10^{19} atoms/cm^3) incorporation was also produced. However, despite these high doping concentrations, we have to remember that laser annealing involves melting the surface of the semiconductor and is therefore not suitable for processing nanostructures as they would lose their structural integrity.

As-MLD in germanium has not been studied to the same extent as other n-type dopants, likely due to the toxicity of the traditional molecular precursors. Previous work in the area of As-MLD also required synthesis of As precursors as there was no commercially available molecule which can undergo the hydrogermylation reaction. This reaction had to this point, been the most consistent means of producing a chemically bound, self-limiting, monolayer for MLD.[32] However, large amounts of toxic waste are generated, which is dangerous and expensive to dispose of. Also, the

synthesised precursors were prone to oxidation therefore extremely difficult to work with.[27, 33-36]

There is huge interest in chemical functionalisation of semiconductors. By modifying the surface of Si or Ge it is possible to control its functionality with applications that extend well beyond MLD such as photovoltaics, [37] electroactivity [38] and biointerfacing [39] for example. Loscutoff and Bent comprehensively reviewed the topic of organic functionalization of Ge in 2006.[40] They acknowledged that wet chemical functionalization methods on Ge were limited, with only three viable wet chemistry methods 1) hydrogermylation 2) thiolation and 3) Grignard reaction.

With the above discussion in mind, the present study describes a novel route for chemical functionalisation of Ge and represents a significant advancement in the field as it is transferrable to a broad range of materials. This new route, adapted to permit controlled doping of Ge substrates with As, is summarised in **Figure 5.1.** Furthermore, we also demonstrate, by comparing with existing data, that the As dose can be finely controlled by controlling the size of the adsorbed molecular precursor, while first principles simulations elucidate the binding mode of the precursor to the Ge substrate. Finally, we demonstrate for the first time on Ge that the maximum limits of electrically active arsenic has been achieved by MLD making it a truly viable alternative to other more destructive, less conformal, techniques, such as ion implantation.

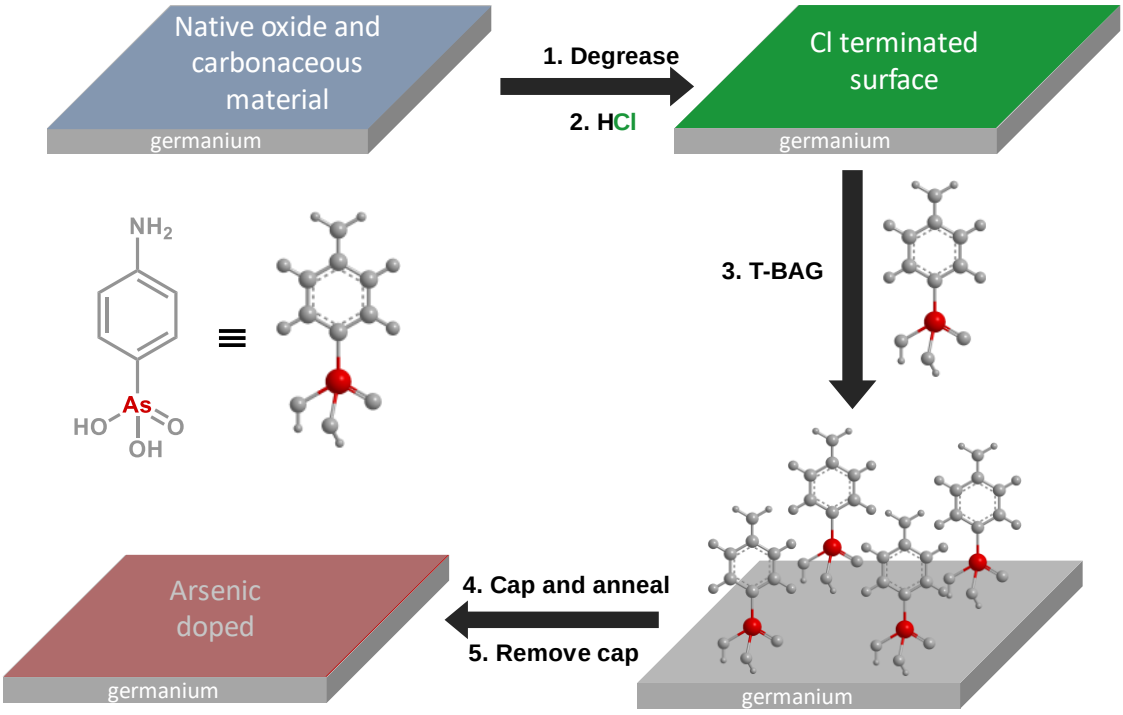


Figure 5.1: Illustration of the novel chemical functionalisation procedure using arsanilic acid on a Cl terminated Ge surface.

5.3 Experimental

5.3.1 Functionalisation process for As-MLD on Ge

All chemicals were purchased from Sigma-Aldrich and used as received. Planar p-type Ge wafers (100) with intrinsic carrier concentrations of ~ 1×10^{16} atoms/cm^3 were diced into 1 cm^2 samples for MLD processing. Carbon contamination and debris from the dicing process was cleaned by sonicating in acetone for 2 minutes followed by a dip in 2-propanol (IPA) with drying under a stream of nitrogen. Chlorine termination was produced by placing the Ge samples into a solution of 10% HCl for 10 minutes. Once a hydrophilic-like Cl terminated Ge surface was achieved a subsequent nitrogen dry was carried out in an effort to remove any traces of the HCl solution. Samples

were then placed in a solution of 0.007 g / 50 ml arsanilic acid in suitable solvent which after testing was chosen to be dichloromethane (≥99.9%). This solution was left to evaporate and once done, a physisorbed arsanilic acid residue remained on the samples. Chemical binding of the arsanilic acid monolayer was carried out through the T-BAG method which required annealing at 140 °C in a vacuum oven for a period of 10 hours. [41] Once this chemisorption step was complete a final clean was carried out to remove the excess physisorbed material. A 2-minute sonication in methanol followed by a further dip in methanol and nitrogen drying was used to remove this physisorbed material. A sputtered SiO_2 capping layer was used to promote dopant diffusion into the semiconductor substrate during annealing. Capping layers were deposited prior to annealing which was done in a RTA system at temperatures from 400-700 °C and times varying between 1-100 seconds. The capping layers were then removed using a dilute solution of BOE. This process was refined to ensure minimal surface damage to both planar and non-planar samples.

5.3.2 Characterisation methods

ECV, AFM, XPS, WCA, and Rs measurements were carried out through the methods detailed in **Chapter 2**. XPS analysis in this Chapter used the Kratos Ultra tool.

5.3.3 Density functional theory modelling of As-acid binding

The adsorption mechanism of arsanilic acid on a model Cl-terminated Ge surface, which prevents reconstruction of the Ge (100) surface and is consistent with Cl-

termination of Ge used in the experiments, has been studied using DFT. In particular our investigation focuses on determining the adsorption of arsanilic acid on Cl-terminated Ge (100) surface. All DFT calculations of geometry and electronic structure have been performed within DFT using the generalized gradient approximation (GGA) as implemented in the Vienna Ab Initio Software Package (VASP.5.4.1) program.[42, 43] The core-valance electron interactions are described by potentials constructed with the projector augmented-wave (PAW) method[44]; the following valance electron configurations are used Ge $4s^2$ and $4p^2$, As $4s^2$ and $4p^3$, C $2s^2$ and $2p^4$, O $2s^2$ and $2p^2$, N $2s^2$ and $2p^3$ and H 1s. The exchange-correlation energy was evaluated with the Perdew-Burke-Ernzehof (PBE) approximation to the exchange-correlation functional.[45] In all calculations, the cutoff energy is 420 eV, the energy is converged when the difference between successive steps is less than 10^{-4} eV and the forces are converged when they are below 0.02 eV/Å. Given the supercell dimensions, we use Γ-point sampling for the Brillouin zone integrations.

The Ge (100) surface is described by a 3D periodic surface slab composed of 4 Ge-atomic layers with a 2x2 surface supercell expansion; this gives eight atoms in the outermost layer of the surface. The two faces of the Ge surface are separated by a vacuum region of 40 Å and the top and bottom layers are passivated with one Cl per surface Ge atom. Ionic relaxations are performed with the atoms belonging to the two bottom Ge-layers constrained while the other atoms were allowed to relax with no symmetry constraints.

To investigate the interaction of arsanilic acid on the Cl-terminated Ge (100) surface we have calculated the adsorption energies (E_{ads}) using the following expression:

$$E_{ads} = E_{molecule\text{-}Ge+Cl} + nE_{HCl} - E_{Ge+Cl} - E_{molecule}$$

where E_{Ge+Cl} and $E_{molecule\text{-}Ge+Cl}$ are the total energies of the Cl-termianted Ge surface and with the arsanilic acid adsorbed. *n* is the number of HCl removed from the system during adsorption, E_{HCl} is the energy of a gas phase HCl molecule and $E_{molecule}$ is the energy of the isolated arsanilic acid, all computed using the same technical parameters and set-up of the previous systems. Given the magnitude of the adsorption energies found, we do not include van der Waals interactions in the adsoprtion calculations, as these will not lead to any significant change in the adsorption energies.

5.4 Results and Discussion

5.4.1 Surface characterisation of monolayer formation

Kary et al,[46] outlined in their patent from 1957, a solution based method of forming arsono-siloxane molecules which involved the reaction of a halosilane with an arsonic acid through a nucleophilic substitution reaction. Nucleophilic substitution is a commonly used strategy in organic chemistry. It involves the attack of a nucleophile to a target carbon molecule which contains a suitable leaving group with an inversion of the stereochemistry. In theory this stereochemistry inversion would not be possible on crystalline substrates. Interestingly, Si has shown an alternative trend to carbon when undergoing these nucleophilic substitution reactions with no inversion in stereochemistry.[47] The T-BAG method of chemically binding a monolayer to a crystalline substrate has previously been demonstrated as a successful method of attaching phosphonic acid monolayers to Si oxide by Chabal *et al*.[41] In this chapter we

have employed this nucleophilic substitution strategy, combined with the T-BAG method as a novel method of Ge functionalization.

Figure 5.1 illustrates the reaction procedure for arsanilic acid with the Ge surface. The first steps involved degreasing the sample by sonicating in acetone to remove carbonaceous material and its termination using chlorine (Cl). Cl termination of Ge has been well described in literature with reports showing that a dip in a dilute solution of hydrochloric acid serves to both remove the native oxide and Cl-terminate the surface with minimal roughening of the Ge substrate.[48] WCA measurements were carried out to determine the change in the hydrophobicity of the surface as an indication of the Cl-termination. WCA values of as-received Ge were ~ 60° with this value decreasing to ~ 35-40°, as expected, as Cl terminated surfaces are known to be hydrophilic.

The functionalisation procedure outlined in the experimental section was carried out on these Cl-terminated samples with the aim of chemically binding a monolayer of arsanilic acid to the Ge surface. One of the key findings from previous T-BAG literature is that the presence of humidity prevents the formation of a covalent bond. In order to minimise humidity, this reaction was carried out in a vacuum oven. After the vacuum oven anneal, the Ge substrate was sonicated in methanol to remove any physisorbed species. A control sample which had undergone annealing in a standard oven and the same post-anneal cleaning procedure was also prepared. An XPS study of these samples, as well as an as-received and Cl terminated Ge wafer was carried out. **Figure 5.2** shows the survey spectra XPS data, highlighting the region around

1326 eV where the As 2p peak can be seen. This data clearly shows that the As 2p peak is only present on the sample (pink line) which has undergone the vacuum oven annealing step. This finding agrees with the previous T-BAG literature in showing that vacuum is essential for the covalent binding of the monolayer. The absence of an As 2p peak on the sample that was annealed in a standard oven would suggest that the sonication of the sample post-anneal in methanol is effective for the removal of non-covalently bound (physisorbed) arsanilic acid molecules. Quantification of the As on Ge is not currently possible via XPS as the As 3d peak overlaps with a Ge plasmon while the As 2p has no known relative sensitivity factor (R.S.F).

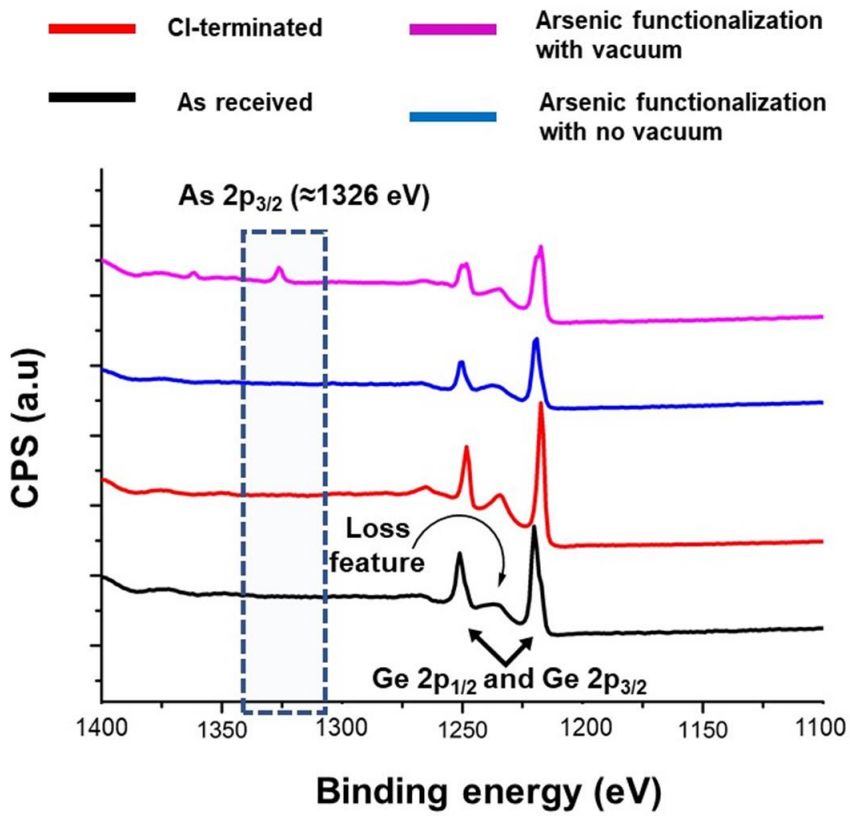


Figure 5.2: XPS survey spectra of as received and Cl terminated Ge and arsanilic acid functionalised Ge, annealed at 140 ^{o}C for 10 hours, with and without a vacuum.

Complete XPS survey spectra are shown in **Figure 5.3** with data analysis in **table 5.1**. Peaks are indicated for Ge 3d, C 1s, O 1s and As 2p. Quantification of the Ge 3d and C 1s components enabled an understanding of carbon (C) content after each process. A degree of C contamination is noted on the as-received sample. This content increases to approximately the same value for Cl-terminated and As functionalised with no vacuum samples. It is possible that some of the solvents (acetone, ipa, etc.) used in processing are still present on the Ge surface in these samples and lead to this increase. The As functionalised with vacuum sample both demonstrates the presence of the As 2p peak and a significant increase in C 1s %. This is as expected given that monolayer formation with As-acid would lead to the introduction of 1 x As and 6 x C atoms per molecule. The peak at 1070 eV in the As functionalised with no vacuum sample is likely a sodium related contamination which can result from manual handling during processing and is deemed inconsequential.

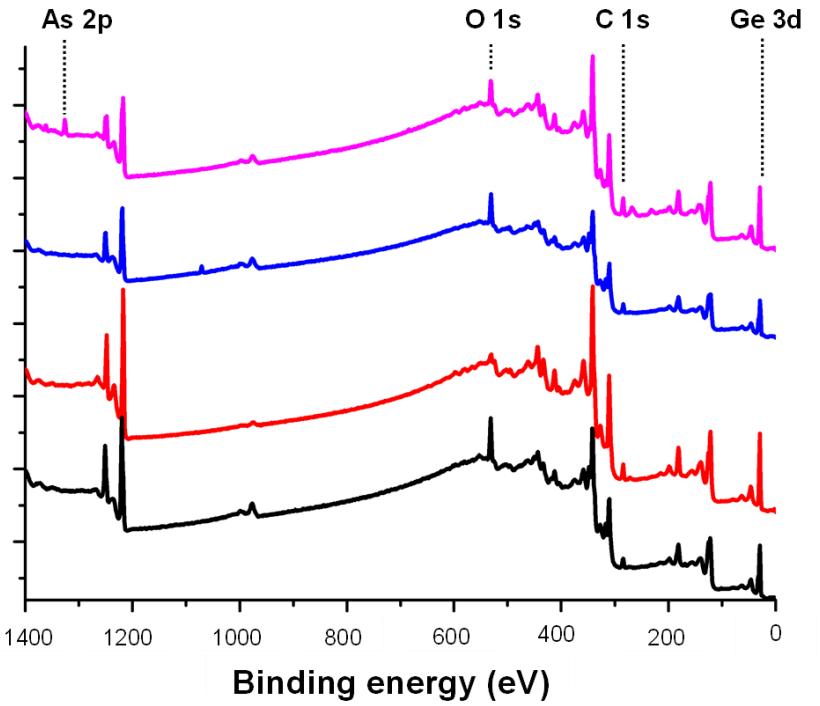


Figure 5.3: Survey spectra analysis of as-received Ge (black), Cl-terminated Ge (red), As functionalised with no vacuum Ge (blue), and As functionalised with vacuum Ge (pink).

	Ge 3d %	**C 1s %**	**Core level area ratio Ge 3d: C 1s**
As-rec	76.8	23.2	4.62:1
Cl-terminated	71.2	28.8	3.75:1
As functionalised with no vacuum	71.1	28.9	3.32:1
As functionalised with vacuum	64.8	35.2	2.91:1

Table 5.1: Comparison of Ge and C content from As-MLD on Ge samples.

Core level spectra of As 2p and As 3d peaks from the As MLD with vacuum sample are shown in **Figure 5.4**. Two distinct peaks are noted in the As 2p signal. The shoulder peak at ≈ 1323 eV (blue) represents As in a +3 or +1 oxidation state while the peak at ≈ 1326.5 eV (red) represents As in a +5 oxidation state which is the

expected positioning from As-acid binding. It is possible that the shoulder peak represents As-acid which has decomposed during the functionalization procedure and now occupies this alternative oxidation state. It is also known that As has a tendency to decay under X-rays from the +5 to the +3 oxidation state and may result in this shoulder artefact.

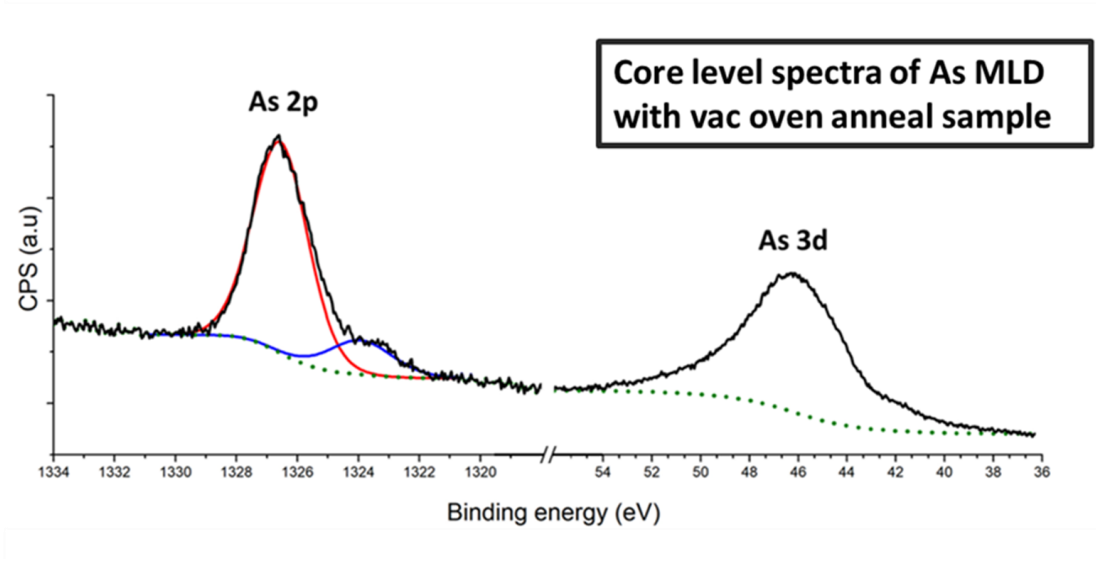


Figure 5.4: Core level XPS spectra of As 2p and As 3d from As-acid functionalized Ge where a vacuum oven anneal was used

Analysis of the core level Ge 3d signal analysed by XPS is shown in **Figure 5.5.** After HCl treatment of the Ge samples it can been seen that there is a significant reduction in the oxide component of the Ge 3d signal at ~33 eV. The sample which has undergone functionalization and annealed in the absence of a vacuum, has returned to a condition similar to the as-received Ge. Under ambient conditions the re-oxidation process would have been much slower, however the elevated temperature combined with humidity, in the absence of a vacuum, promotes this oxidation. The sample which has undergone functionalization with a vacuum oven anneal shows a small growth in

the peak at ~33eV. It is noted that after 1 week (t = 168 hrs) the contribution from this peak remains the same indicating that the monolayer functionalized sample is stable.

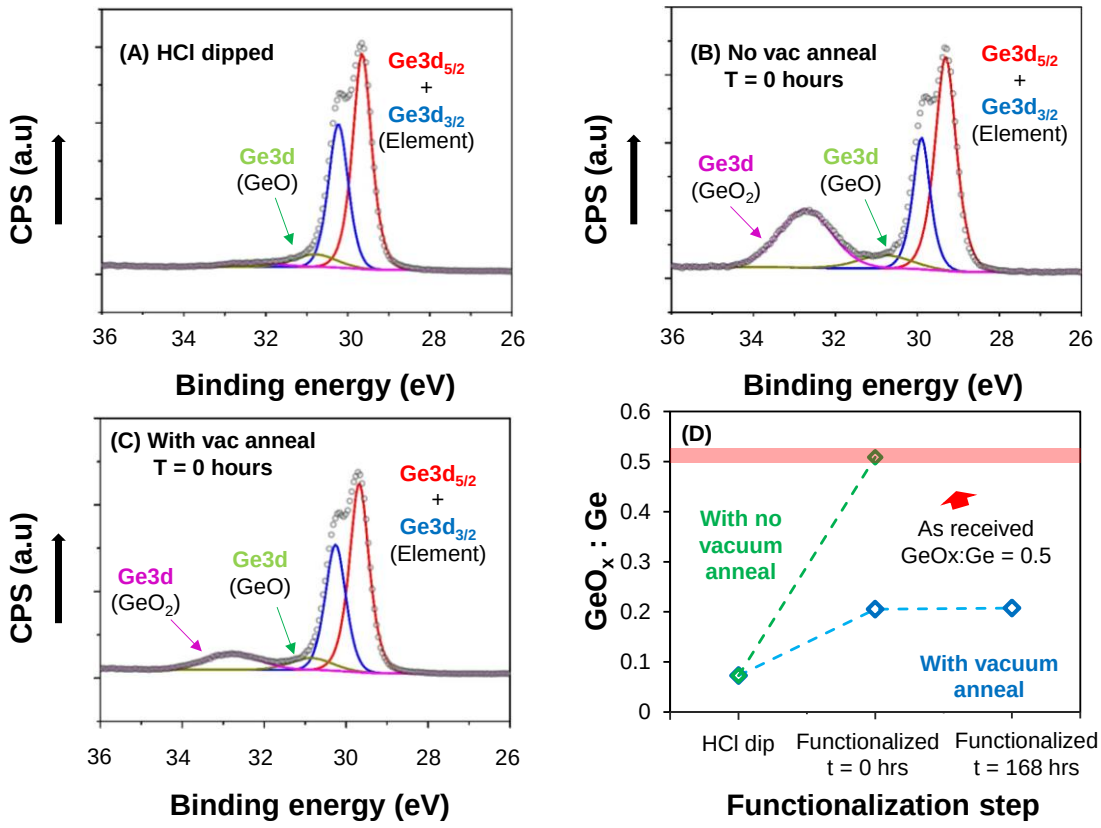


Figure 5.5: XPS analysis of the Ge 3d peak for (A) Cl terminated (B) Arsanilic acid functionalised annealed in the absence of vacuum and (C) Arsanilic acid functionalised annealed in the presence of vacuum and (D). Analysis of GeOx:Ge over time for the arsanilic acid functionalised samples with and without a vacuum anneal. t= 0 hours represents samples analysed immediately after completion of the monolayer grafting process while t= 168 hours represents a sample which has undergone the grafting process and has subsequently been stored for 168 hours in ambient conditions before analysis.

5.4.2 Theoretical calculations of molecule binding

We use first principles DFT to model the adsorption of the arsanilic acid molecule to a model Ge substrate to determine the preferred binding mode of the molecule. **Figure**

5.6 shows a schematic of the adsorption process and identifies three likely binding modes, two through the acid group, using two oxygen sites (removing two surface Cl atoms) or one oxygen site (removing one surface Cl atom) and the third through the amino group, removing one surface Cl atom.

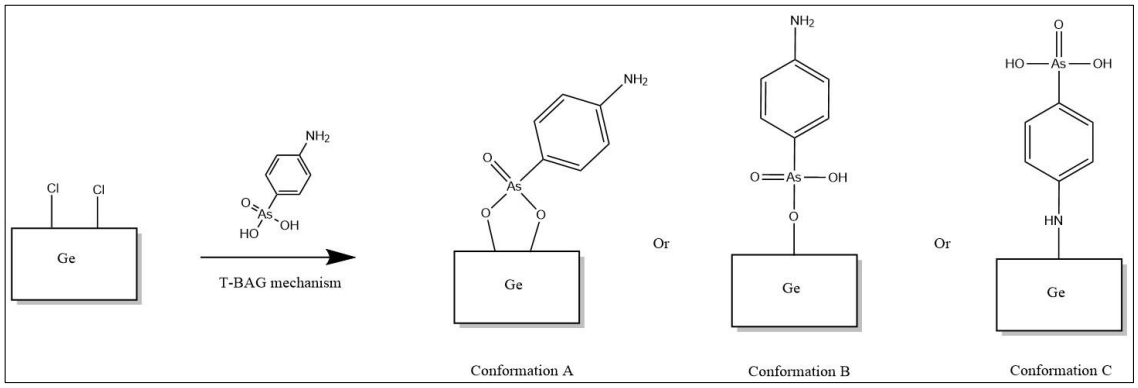


Figure 5.6: Possible surface binding conformations of the As-acid molecule to the Ge surface

Figure 5.7 shows the atomic structure of the Cl-terminated Ge(100) surface and relaxed adsorption structures for the three adsoprtion modes described above. The computed adsorption energies are -4.97 eV for Configuration A, -5.70 eV for Configuration B and -3.66 eV for Configuration C. Therefore the arsanilic acid molecule can in principle adsorb at Ge (100) in all three configurations, with loss of HCl. However, we note that configuration B, in which one oxygen atom from the acid group initially binds to one Ge atom in the (100) surface, relaxes so that adsorption takes place through two oxygen atoms in the molecule. These oxygen atoms each coordinate to different surface Ge atom (inset of Figure 5.6(c)). In the other adsorption modes the interaction is through two oxygen atoms in the acid group (Configuration A) or the nitrogen atom in the amino group (Configuration C). In addition, in configuration B, the phenyl ring tilts relative to the Ge surface.

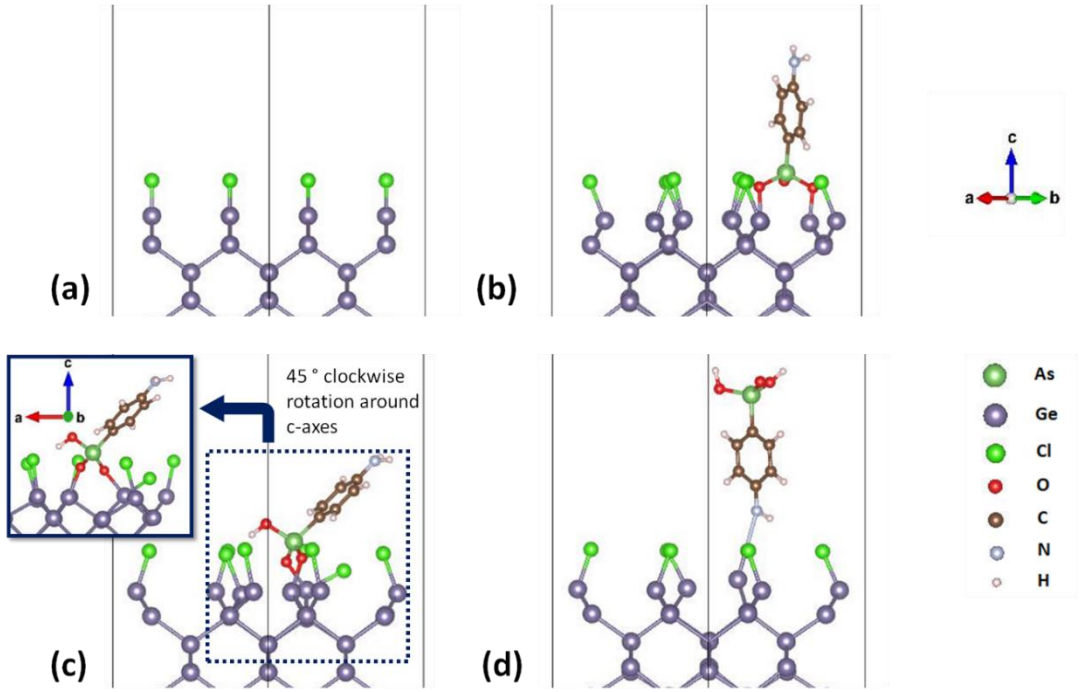


Figure 5.7: Atomic structure of **(a):** Cl-terminated Ge (100) surface, **(b):** relaxed adsorption structure of arsanilic acid in Configuration A, **(c):** relaxed adsorption structure of arsanilic acid in Configuration B and **(d):** relaxed adsorption structure of arsanilic acid in Configuration C. In panel **(c)** we also show a rotated view so that the As-O-Ge bonds can be seen.

In Configuration B, one Ge atom maintains a Ge-Cl bond, with a Ge-O distance of 1.93 Å. The second Ge-O distance is 1.92 Å and the As-O distances are 1.74 Å. Finally, the distance from As to the hydroxyl oxygen that does not bind to the surface, As-OH, is 1.75 Å. During the relaxation the As-O distances in the molecule increase by 0.09 Å and 0.06 Å for those oxygen binding to Ge and decrease by 0.05 Å for the As-OH bond. This change in metal-oxygen distances is consistent with the strong adsorption energy.

In Configuration A, the Ge-O distance involving the initially unprotonated oxygen is 1.86 Å , while for the other oxygen it is 2.01 Å. The O-As distances are 1.65 Å for oxygen that forms the double bond with As and 1.80 Å for the oxygen binding to the

surface. Finally, in the least stable configuration, Configuration C, the Ge-N distance is 3.71 Å and the interaction is clearly weaker and we do not expect this binding mode to be of importance in the MLD process.

Finally, we note that after adsorption and ionic relaxation, surface Ge and surface terminating Cl atoms are distorted away from their initial positions in the Cl-terminated Ge (100) surface. For example we see a clear tilting of the surface terminating Cl atoms.

5.4.3 Material characterisation after MLD

5.4.3.1 AFM analysis of surface topology

As-MLD functionalized samples were capped with 50 nm of sputtered SiO_2. It has previously been shown that the deposition of a capping layer is essential in the MLD process to optimise the diffusion of the dopant atoms from the surface into the bulk of the target semiconductor.[16, 34] Following capping, the samples were annealed using an RTA system and prepared for characterization by removing the cap using a dilute BOE solution. AFM imaging of samples after each processing step, shown in **Figure 5.8**, was carried out to monitor the surface roughness. Initial starting Ge (Fig 6. A) shows a high-quality surface with a roughness value of 0.26 nm. A slight increase in surface roughness is noted after the MLD processing steps with a final roughness of 0.55 nm. This increase in surface roughness is considered suitable for transfer to nanostructured Ge as it remains within ± 0.3 nm of the initial starting value. If roughness values were to increase significantly after MLD processing on blanket samples one would envisage, that given the dimensions of current and future nanostructured Ge, there would be the potential for structure damage and even complete structure loss.

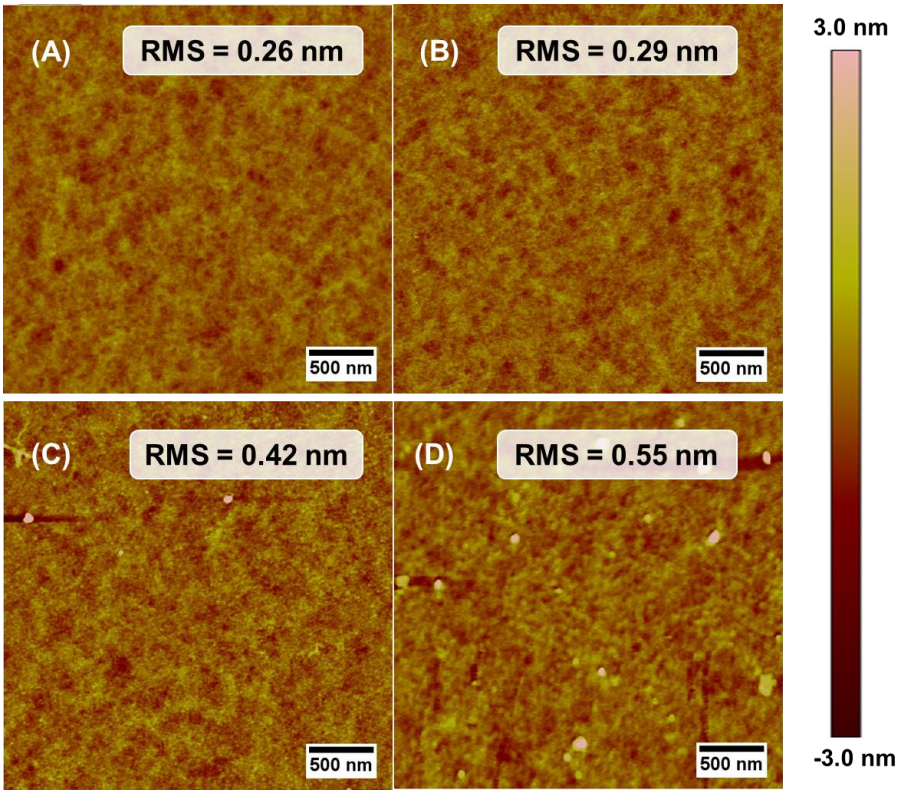


Figure 5.8: AFM of (a) cleaned (b) Cl-terminated (c) functionalized with vac oven anneal and (d) post MLD and cap removal Ge.

5.4.3.2 Dopant profiling and sheet resistance measurements

Active carrier concentration values from As-MLD doped Ge are shown in **Figure 5.9** where the RTA time was varied while maintaining a constant temperature of 650 °C. Using a conventional RTA system this is the maximum temperature permitted (~2/3 of melting temperature) for Ge as it has a melting point of 938.12 ^{o}C. The maximum carrier concentration for the first 8-10 nm shows values between 3×10^{19} and 4×10^{19} atoms/cm^3. Surface artefacts are known to impact on the accuracy of the initial surface data point measured through ECV and lead to this data point often being disregarded when quoting maximum carrier concentrations. Maximum carrier concentration values after this surface point of $> 1 \times 10^{19}$ atoms/cm^3 represent the highest values

seen to date with As-MLD. Previously, the maximum carrier concentration of As-MLD on Ge was approximately half of this at 6×10^{18} atoms/cm^3.[27] The solid solubility and maximum electrically active limits of arsenic in Ge have not been as widely reported on as the corresponding values for Si. Chui et al [49], reported that the maximum electrically active limit of As is 3.5×10^{19} atoms/cm^3 for Ge doped through implantation and activated with a 500°C RTA. Their study also noted that RTA temperatures above 600 °C lead to considerable As diffusion with a concurrent decrease in the maximum electrically active dopant levels to ~ 2×10^{19} atoms/cm^3. Other reports of As activation in Ge have placed the maximum activation level in a range between 1-3 $\times 10^{19}$ atoms/cm^3. [50-55] Duffy *et al* [56], have reported maximum activation limits in this 2×10^{19} atoms/cm^3 region for Ge doped with As through a gas phase source using RTA temperatures above 600 °C. Miyoshi *et al*, reported a maximum activation value with a form of microwave plasma doping at 4.3×10^{18} atoms/cm^3. [57] Analysis of the shape of the plots in **Figure 5.9** shows that they have box like profiles as have been seen in other As diffusion doping studies which are consistent with concentration enhanced diffusion.[58]

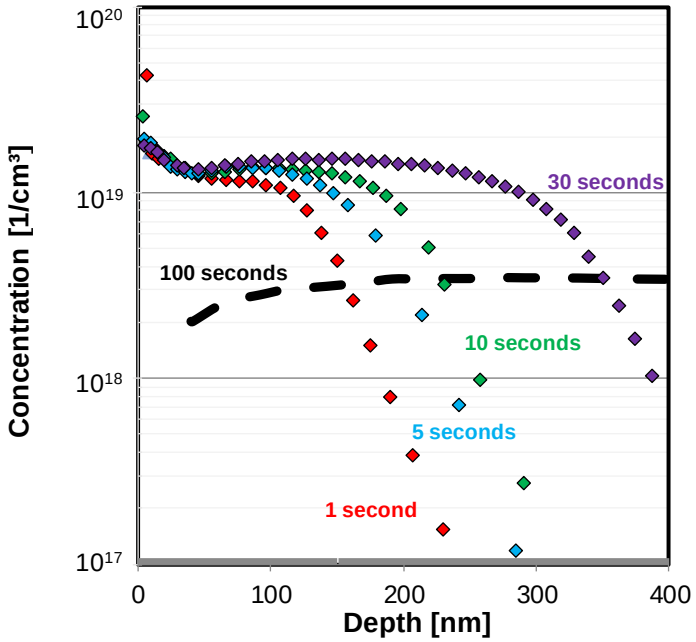


Figure 5.9: ECV profiling of active carrier concentrations in Ge samples after arsenic MLD processing. RTA time has been varied with all samples receiving a 50 nm sputtered SiO_2 cap and 650 °C RTA

Monolayer doping by nature is a limited source diffusion method of doping. Further indirect evidence of monolayer formation is provided through analysing the incorporated dose values from the ECV data. **Table 5.2** shows that dose values plateau at ~ 4×10^{14} atoms/cm^2. Profiles match the theory of limited source diffusion.[59] Between 30 seconds and 100 seconds the complete surface dose is incorporated and dopants which were situated close to the sample surface diffuse further into the bulk using a 100 second anneal.

Validation of the ECV data was attained from sheet resistance (Rs) measurements of the MLD doped blanket Ge samples. Through the formula outlined previously by Duffy *et al*,[56] it was possible to translate carrier concentration profiles from ECV to a

theoretical Rs value which was then compared to the experimentally determined value. The correlation between the theoretical and experimentally measured Rs is shown in **Table 5.2** with reasonable agreement between the values, which corroborates the ECV data.

RTA time	**Dose (**atoms/cm^2**)**	**Sheet resistance (Ohm/sq)**	
		Theoretical (ECV)	**Measured value**
1 second	1.7×10^{14}	101	99
5 seconds	2.3×10^{14}	79	72
10 seconds	2.8×10^{14}	70	60
30 seconds	4.5×10^{14}	46	40
100 seconds	4.2×10^{14}	25	10

Table 5.2: Total activated dose values in Ge from As-MLD with variations in RTA time using a 650 °C RTA. Sheet resistance values of selected samples were measured and compared to theoretical values to validate ECV data

The impact of varying RTA temperature on dopant incorporation/activation is shown in **Figure 5.10** and **table 5.3,** with a fixed time of 10 seconds. Increasing maximum carrier concentrations are observed with increasing RTA temperature up to 650 °C. In comparison to implantation, MLD has additional thermal budget requirements for molecule decomposition and drive-in to the crystalline lattice. Therefore, it is reasonable that the trend in activation requires a sufficiently high temperature value for these budget requirements to be met. A similar observation has been made with P-MLD on Si which is described in Chapter 3. Decreased activation levels are observed in the 700 °C sample. A similar trend has previously been noted in work by Camacho-Aguilera et al, where they were doping Ge with delta-P layers. [60] They encountered a temperature limitation whereby maximum carrier concentrations were limited by

dopant out diffusion. It is possible that this data represents another example of this type of phenomenon. It is also worthwhile noting that RTA temperature provides a degree of control over the resulting Xj achieved from MLD. Although maximum activation levels in the 550 °C sample are lower than the 650 °C at ≈ 5.5 $\times 10^{18}$ $cm^{-3,}$ it does demonstrate extremely shallow diffusion from MLD with a 5 $\times 10^{18}$ cm^{-3} Xj of just 15 nm.

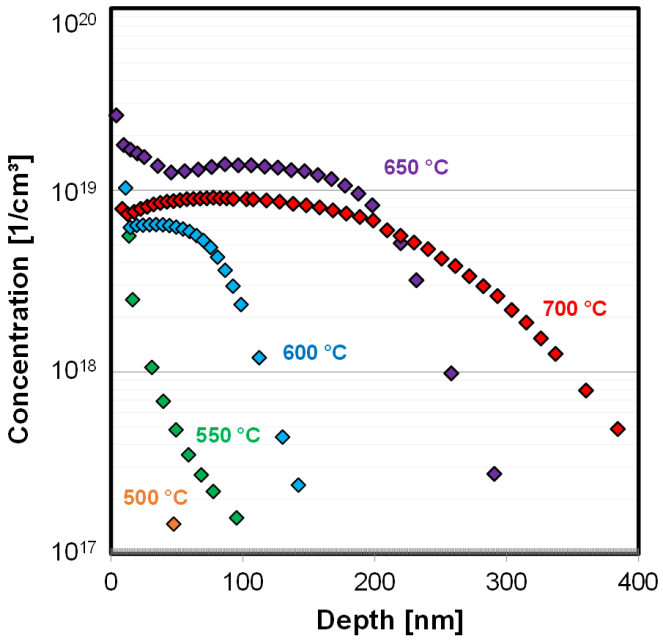


Figure 5.10: ECV profiling of active carrier concentrations in Ge samples after arsenic MLD processing. RTA temperature has been varied with all samples receiving a 50 nm sputtered SiO_2 cap and a 10 second RTA

RTA temperature (°C)	**Dose (**atoms/cm^2**)**
500	8.6×10^{11}
550	1.2×10^{13}
600	6.1×10^{13}
650	2.5×10^{14}
700	2.1×10^{14}

Table 5.3: Total activated dose values in Ge from As-MLD with variations in RTA temperature using a 10 second RTA.

5.4.3.3 Theoretical dose estimation and comparison

The pioneering work of Ho *et al* demonstrated the ability of MLD to provide controlled dopant doses to semiconductor materials, by the variation of dopant-containing molecule.[15] Since then, a number of studies have found success in controlling dose through MLD, such as those by Ye et al and Perego et al.[61, 62] These studies have all focused on the application of phosphorus and boron MLD to silicon.

A rudimentary method of estimating the quantity of the arsanilic acid molecules which can pack onto the Ge surface, is to model the dimensions of the molecule, assume a spherical shape and calculate the maximum coverage on a semiconductor surface in a 2-dimensions (see **Figure 5.11**). Modelling work was carried out using Materials Studio© software. TAA which was used for previous As-MLD studies on Ge has a calculated diameter of 0.94 nm which translates to a theoretical "ideal" dose of ~ 1.5 $\times$ 10^{14} atoms/cm^2.[27, 34] Previous experimental work using TAA incorporated a maximum dose of 2 $\times$ 10^{14} atoms/cm^2. By comparison, arsanilic acid was calculated to have a diameter of 0.46 nm. An approximate maximum dose of ~ 6 $\times$ 10^{14} atoms/cm^2 was calculated from this 2-dimensional "ideal" packing scenario. Experimentally it was determined from ECV that an active dose of ~ 4 $\times$ 10^{14} atoms/cm^2 was incorporated. This corresponds with to approximately 70% of what could have been achieved with ideal packing. There are two reasons why 100% of the potential dose was not incorporated. The first being that the packing of the molecules was not ideal

and spaces on the surface of Ge were present which were too small to incorporate a molecule, therefore full coverage was not achieved. The second is that some of the As from the molecules attached to the surface got trapped at the interface or in the capping layer. In reality it is probably a combination of both but a theoretical study to determine what the optimal packing could be for such molecules will be pursued in future studies. This provides an experimental validation of the theory, that changing size of the footprint of the dopant-containing molecule, between As-acid and TAA, allows for controlled adjustment of dose from 2×10^{14} atoms/cm^2 to 4×10^{14} atoms/cm^2. It is important to note that this approach for modulating dose, between As-acid and TAA, does require different monolayer reaction strategies. Further advancement of As-MLD on Ge by functionalisation with larger and smaller dopant-containing molecule sizes will allow for greater ability to tune the incorporated dose through MLD.

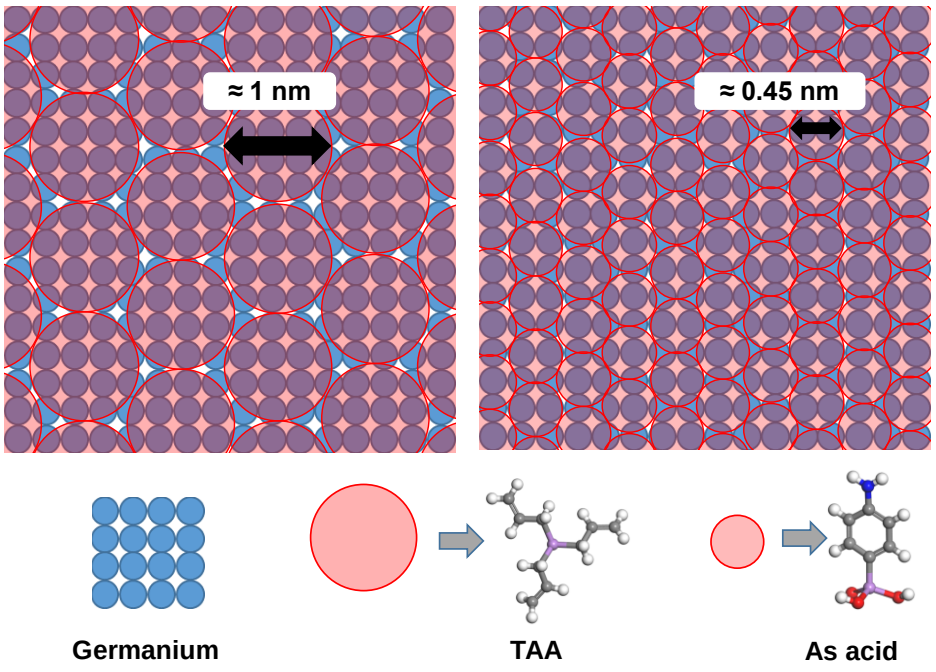


Figure 5.11: 2-dimensional depiction of packing density for arsenic MLD precursor arsanilic acid As acid) and a comparison with previously used TAA

5.4.3.4 Diffusion co-efficient calculation and comparison with literature

Dose values determined from ECV where the RTA temperature was varied (**Figure 5.9**) were used to calculate the diffusion co-efficient of arsenic introduced through MLD. These values are compared to previous literature where ECV was used. The methodology for calculating diffusion co-efficient has previously been outlined in the study of phosphorus doping of silicon-germanium.[24] **Figure 5.12** demonstrates the increase in diffusion co-efficient with increasing RTA temperature. Our data shows some correlation with the previous As-MLD literature where triallylarsine was used as a dopant source.[27] Duffy et al, utilized a gas source (AsH_3) method for As diffusion and activation in Ge which shows lower diffusivity than results from arsanilic acid-MLD. [56] Temperature ramp rates of the annealing tools are likely to differ between each study, and the inclusion of additional elements such as carbon and nitrogen impacting diffusivity of As, may account for the difference in the diffusion co-efficient. All data sets have diffusion co-efficients which are in the extrinsic doping regime.

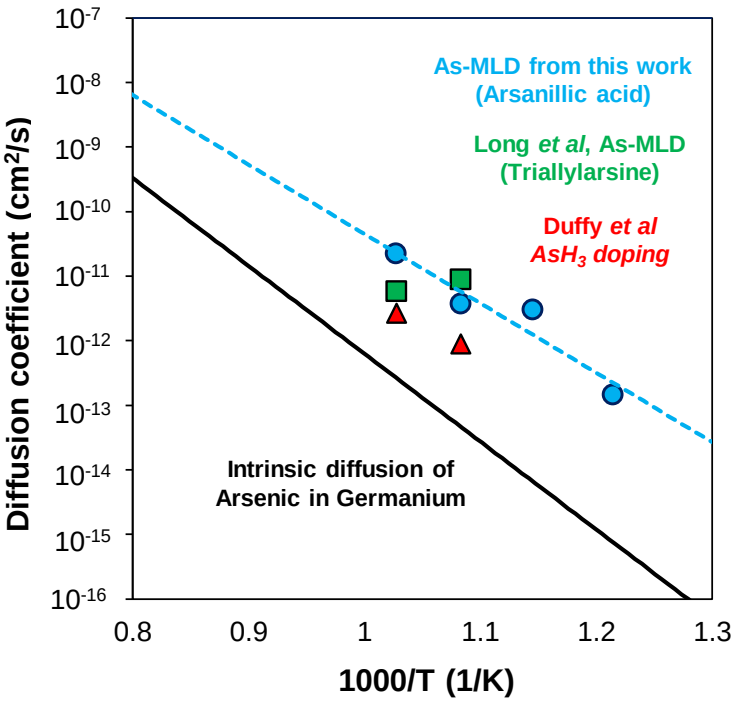


Figure 5.12: Diffusion co-efficient vs 1000/T, where T is in Kelvin. A black solid line is used to show intrinsic As diffusivity, red markers to show the previous work of Duffy et al, and blue markers to indicate As-MLD data from this work. Diffusion co-efficient from Duffy et al, and this work have been calculated from ECV.

With the aim of potential doping processes to decrease annealing temperatures, while maintaining or improving active carrier concentrations and minimizing diffusion depth, it is evident that MLD requires alternative methods of delivering dopant atoms into target substrates with reduced thermal budgets. Utilizing tools such as laser and flash lamp annealing have shown promise for producing greater than solid solubility limit levels of dopants in Ge. [31, 63-65] Further studies into the combination of MLD with these advanced annealing techniques are important to demonstrate the true of potential of this doping methodology.

5.5 Conclusions and outlook

A new chemical route for functionalising Ge has offered the opportunity to controllably dope nanostructured Ge using As via monolayer doping, which overcomes many of the issues associated with ion implantation and permits a record As doping level to be achieved. It involves the functionalisation of Cl terminated Ge with a commercially available arsenic containing molecule, arsanilic acid. By applying this new chemical route we have demonstrated a simple, non-destructive approach for conformal doping of Ge producing n-type doping levels, rivalling beam-line implantation, which matches previously shown active solubility limits of arsenic (approx. 2×10^{19} atoms/cm^3) when using RTA temperatures greater than 600 °C. These active carrier concentrations are two times higher than what was the previously assumed limit of As-MLD on Ge and for the first time is at dopant levels that allow the use of Ge as the channel material in transistor devices. We demonstrate that anneal time allows control over the depth of diffusion of the arsenic dopants in Ge. By calculating the molecular footprint of the arsanilic acid and comparing it to that of triallylarsine used in a previous study we propose that the molecular footprint be tuned (i.e. increasing or decreasing the size of the molecule) to control the dose of dopant that is delivered to Ge. Finally, the discovery of this new chemical functionalisation route significantly advances the field of surface functionalisation with implications for many potential applications and a broad range of materials.

5.6 References

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CHAPTER 6

MLD on silicon-germanium alloys: A balancing act between phosphorus incorporation and strain relaxation

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Adapted from the following presentation and publications. As a result, sections such as introduction and abstract may contain repeating concepts. A comprehensive authorship contribution section is provided in **Chapter 8**:

Kennedy, N; Duffy, R; Mirabelli, G; Eaton, L; Petkov, N; Holmes, J.D; Hatem, C; Walsh, L; Long, B. **Journal of Applied Physics 126, 025103 (2019)**

6.1 Abstract

This chapter presents the application of monolayer doping (MLD) to silicon-germanium (SiGe). This study was carried out for phosphorus dopants on wafers of epitaxially grown thin films of strained SiGe on silicon with varying concentrations of Ge (18, 30 and 60 %). The challenge presented here is achieving dopant incorporation while minimising strain relaxation. The impact of high temperature annealing on the formation of defects due to strain relaxation of these layers was qualitatively monitored by XTEM and AFM prior to choosing an anneal temperature for the MLD drive-in. Though the bulk SiGe wafers provided are stated to have 18, 30 and 60 % Ge in the epitaxial SiGe layers it does not necessarily mean that the surface stoichiometry is the same and this may impact the reaction conditions. XPS and AR-XPS were carried out to compare the bulk and surface stoichiometry of SiGe to allow tailoring of the reaction conditions for chemical functionalization. Finally, dopant profiling was carried out by SIMS to determine the impurity concentrations achieved by MLD. It is evident from the results that phosphorus incorporation decreases for increasing mole fraction of Ge, when the RTA temperature is a fixed amount below the melting temperature of each alloy.

6.2 Introduction

Device sizes for electronic applications have been aggressively scaled down over the past 50 years, pushing the limits of what was capable by introducing new materials such as high-k dielectrics,[1] and new device architectures such as FinFETs,[2] for example. Regardless, in recent times device dimensions have approached a critical point where silicon, the cornerstone of the semiconductor industry, struggles to achieve the performance gains as scaling continues. In this context, other high mobility materials, such as SiGe, are being investigated to assess their potential.[3] Currently, low mole fraction (MF) SiGe is being used as a stress enhanced carrier mobility booster[4] and is considered to be a viable candidate for a channel material in MOSFETs.[5-7] Recently, the 7-nm technology node solution has also been proposed with integration of SiGe p- and strained-Si n-MOSFETs, showing the feasibility of SiGe devices in future devices.[8] However, there are no reports of chemical functionalization of SiGe in literature, and only a few reports of *ex-situ* doping SiGe[9, 10] when compared to silicon.

For thin-film homogeneous strained or relaxed SiGe with >50 % Ge-content there is little available experimental data on processing such as dopant diffusion and activation, contact formation, or on *in-situ* doping and selective epitaxial growth on surfaces with different crystal orientations. Very recently, publications have emerged on high-Ge content SiGe for solar cell applications.[11-13]

Doping of future technology devices fabricated either from thin-films or 3-D structures could prove difficult for ion implantation, which has been the most commonly used *ex-situ* doping technique during the device miniaturization drive until

this point.[14, 15] High energy ion beams induce damage (amorphization) into these structures which prove difficult to remove, if at all.[16] Possibly the most critical flaw of ion implantation is the lack of conformality seen when doping 3-D structures such as fins or nanowires. Due to the directionality of the technique it struggles to equally dope both the top and sidewalls of these structures.[17] A number of alternative *ex-situ* doping methods have been proposed and developed to offer solutions to the problems encountered with ion implantation such as PLAD,[18] spin-on-doping,[19] and solid-source-diffusion.[20] However, these techniques also suffer from crystal damage or lack of dose control. Doping SiGe *in-situ* has been studied for many years[21-23] and is the current trend in certain technology applications. Furthermore a boost in dopant activation by using a laser anneal after the growth of the *in-situ* doped epi layer has shown to be beneficial in source/drain contact regions.[24] However for alternative applications, or other parts of the transistor, epitaxy may not be suitable due to design or space restrictions.

Monolayer doping (MLD) has been developed as a method to produce ultra-shallow junctions (USJ's) without crystal damage, while also conformally doping 3-D substrates.[25-27] It has already been demonstrated on a variety of semiconductors including Si,[28-34] Ge,[35-37] and a number of III-V materials.[38] **Figure 6.1** depicts the MLD procedure on SiGe. The key step involves functionalization of the target surface through the bonding of a dopant molecule (in this case ADP) to form a self-limiting monolayer where the quantity of dopant molecules present is determined by the molecule size and also defines the dose. Once monolayer formation is complete the samples are capped with an oxide layer to prevent desorption and promote diffusion of the dopant atoms into the substrate during thermal treatments. After thermally

treating the samples the capping layer can be removed to leave a uniformly doped substrate whether it be planar or 3-D. This chapter will examine the application of phosphorous MLD to SiGe alloys ranging from low Ge content 18 %, to high Ge content 60 % aiming to understand if this novel doping technique can effectively dope these substrates. There are two main challenges associated with doping SiGe by MLD 1) How to chemically functionalize the SiGe with dopant-containing molecules (i.e. will the reactivity of the surface atoms to the molecules be like silicon or germanium?) and 2) How to avoid strain relaxation of the non-buffered SiGe layers during the dopant drive-in annealing step?

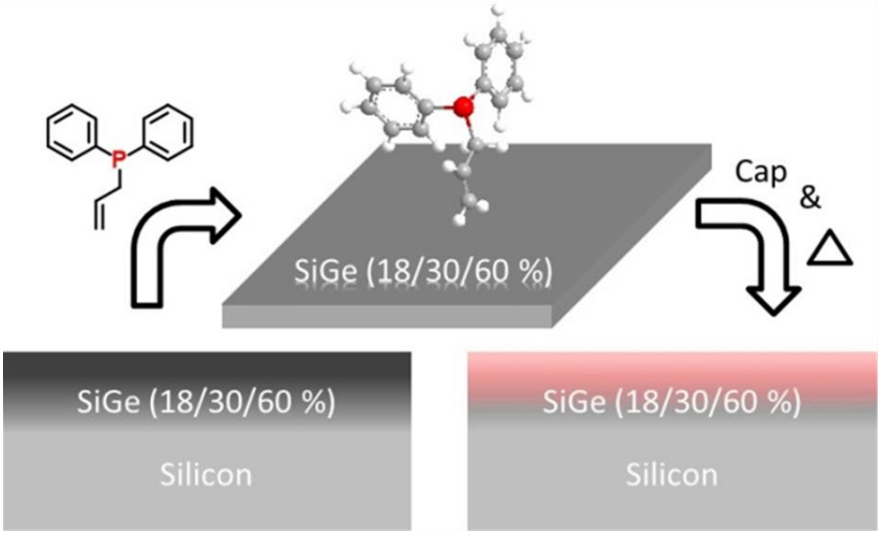


Figure 6.1: Summary of MLD procedure on SiGe

6.3 Experimental methods

6.3.1 SiGe wafer growth and surface functionalisation method

Thin films of strained SiGe were grown on a 300 mm Applied Materials epitaxy system on silicon substrates with germanium contents of 18, 30 and 60 % respectively. The thickness of these films was inspected with cross sectional transmission electron microscopy (X-TEM). All chemicals were purchased from Sigma Aldrich. 1×1 cm samples were cut from the starting SiGe wafers and cleaned by sonicating in acetone (≥99.8 %) for 2 minutes, followed by a rinse in isopropyl alcohol (IPA-99.9 %) and drying under a stream of nitrogen. Samples were hydrogen terminated by dipping in 2 % hydrofluoric acid (HF) for 10 seconds and placed under nitrogen in a Schlenk line to prevent re-oxidation. A 0.1 M solution of allyldiphenylphosphine (ADP-95 %) in mesitylene (98 %) was degassed and transferred into the reaction flask containing the H-terminated samples. This reaction flask was heated to 180 °C for 3 hours to allow for optimal monolayer formation on the SiGe surface. Samples were then removed and sonicated in IPA for 1 minute followed by a further IPA rinse and drying under a stream of nitrogen to remove any physisorbed dopant molecule. Functionalized samples were stored under nitrogen until capping with 50 nm sputtered SiO_2. RTA was carried out at a variety of temperatures and times which are specified for each result. The SiO2 capping layer was then removed by dipping in a 25:1 BOE solution until a hydrophobic H-terminated surface was produced.

6.3.2 Characterisation methods

XTEM, SIMS, XPS, and AFM characterisation which were carried out in this work are extensively outlined in **Chapter 2**. The Kratos Ultra tool was used for XPS analysis.

6.4 Results and Discussion

6.4.1 Material characterisation of SiGe for MLD processing

6.4.1.1 TEM analysis of starting SiGe substrates

Figure 6.1 broadly describes the process of doping SiGe by MLD. ADP was chosen as a source of phosphorus for these experiments for two reasons; (1) it contains the C=C functionality which reacts with both Ge and Si with an assumption being made that it will also react with SiGe and (2) its remaining functional groups are phenyl rings which are highly unreactive thereby inhibiting multilayer formation.

Epitaxially grown SiGe with varying concentrations of Ge were used in this study. As-received, the amount of Ge in the SiGe wafers provided was stated to be 18, 30 and 60 %. Representative XTEM images are show in **Figure 6.2**. Though chemical reactions on Si and Ge are similar there are variations in reactivity between the two materials. For example, the reaction of an alkene with hydrogen terminated Si will occur in solution when heated to 180 ^{o}C but under these same conditions it will not

react with Ge. Either much higher temperatures (> 220 ^{o}C) or UV light are required for the reaction between an alkene and Ge to proceed. [35, 36]

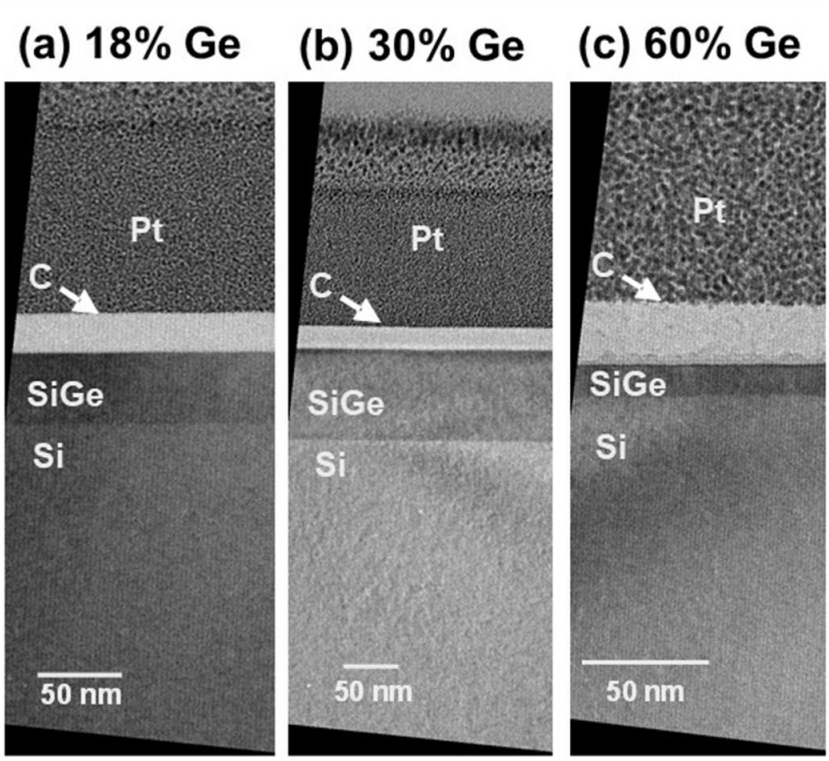


Figure 6.2: XTEM of as-received SiGe (a) 18% Ge (b) 30% Ge and (c) 60% Ge

6.4.1.2 Determination of SiGe content with XPS analysis

Though the bulk SiGe wafers provided are stated to have 18, 30 and 60 % Ge in the epitaxial SiGe layers it does not necessarily mean that the surface stoichiometry is the same as the bulk. The surface stoichiometry is important as it may impact the chosen reaction conditions for the chemical functionalization. In order to assess if surface stoichiometries differ to the bulk, an angle-resolved XPS study was carried out. **Table 6.1** show the measured stoichiometries for each sample.

Sample ID	Measured stoichiometry	Measured stoichiometry (60°)
SiGe18	$Si_{0.86}Ge_{0.14}$	$Si_{0.88}Ge_{0.12}$
SiGe30	$Si_{0.67}Ge_{0.33}$	$Si_{0.69}Ge_{0.31}$
SiGe60	$Si_{0.35}Ge_{0.65}$	$Si_{0.35}Ge_{0.65}$

Table 6.1: The experimentally measured surface stoichiometries of the epitaxial SiGe. The measured stoichiometries are reported for take-off angles of 90 and 60 degrees. The measured stoichiometries are calculated from the areas of the Si *2p* and Ge *3d* XPS core levels, normalized using the appropriate relative sensitivity factors.

The measured stoichiometries are 14, 33 and 65 % for XPS with a take-off angle of 90° which corresponds to a sampling depth of 9.1 nm for the Ge 3d peak and 8.8 nm for Si 2p peak.[39] Those measured for the XPS with a take-off angle of 60° were 12, 31 and 65 %, where the sampling depth is halved when compared with samples measured with a take-off angle of 90° and thus are more surface sensitive. With a commonly specified error range of +/- 10 % it can be concluded that the surface and bulk stoichiometries do not differ drastically.

6.4.1.3 Packing density calculation of ADP on SiGe

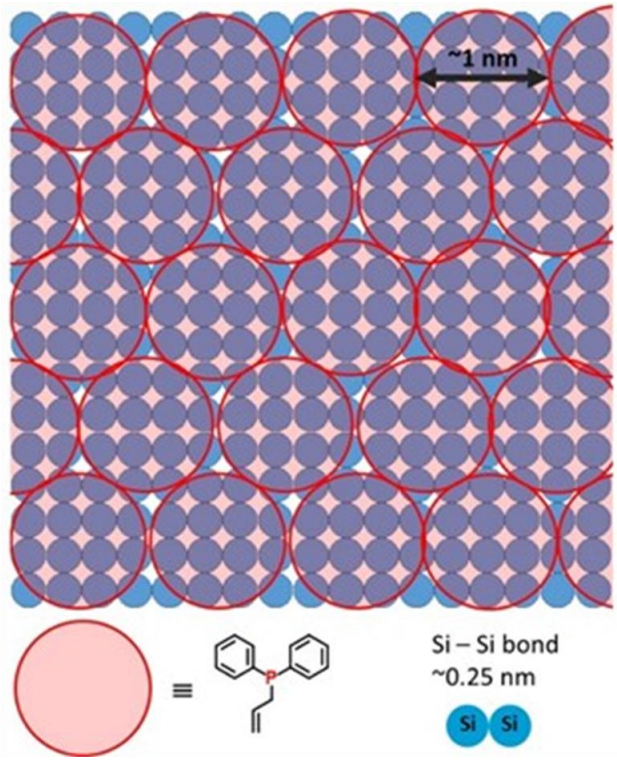


Figure 6.3: Illustration showing the approximate footprint of the molecule, ADP, on the surface of Silicon

Figure 6.3 shows roughly how much space the ADP will take up on the surface of a substrate in an ideal packing scenario. It is important to note that effects such as steric constraints may impact this packing and lead to a situation where less molecules are packed on the semiconductor surface. For the purposes of illustration, the surface depicted is silicon. Given that ADP has an approximate molecular footprint of 1 nm^2 and that the Si-Si bond length in crystalline Si is roughly 0.25 nm about 1 in 16 Si atoms (or ~6 % of the surface atoms) will have a molecule bonded to them. An assumption is made here that these calculations will be very similar for the SiGe substrates. Though these calculations and the illustration in **Figure 6.3** are for

indication only, when combined with the XPS data we are satisfied that we can treat the SiGe surface, from a chemical reactivity point of view, as if it were silicon. It should be noted that the authors recognize that though the chemical reactivity of Si and Ge are well established [28, 29, 36, 37]there is no available data on the reactivity of SiGe.

6.4.1.4 Characterisation of SiGe after high temperature RTA

The selection of the drive-in anneal temperature is a critical part of this experimental set-up. Si melts at 1416 °C, while Ge melts at 938 °C, and alloys of SiGe melt at temperatures between those extremes, depending on the % Ge content. Another consideration is that the epitaxial SiGe is strained and heating to high temperatures will cause strain relaxation. XTEM and AFM were carried out on SiGe 30 % to assess the impact of annealing at high temperature. The standard annealing temperature for MLD on Si is 1050 °C. [26, 32] Before anneal, the substrates show no obvious crystal defects in cross-section or in the AFM analysis (representative images in **Figure 6.4a**). Post-anneal at 1050 °C, it is obvious the SiGe layer has been degraded (**Figures 6.4b**). For example, there is extensive crosshatching in the AFM. Crosshatching occurs as a result of misfit dislocations having formed at the SiGe:Si interface. These misfit dislocations are an indication of the strain relaxation which can also be seen in the XTEM which contains a noticeably defective SiGe:Si interface. Furthermore, a stacking fault is visible in **Figure 6.4b** resulting in a kink or step-like feature at the surface where it terminates.

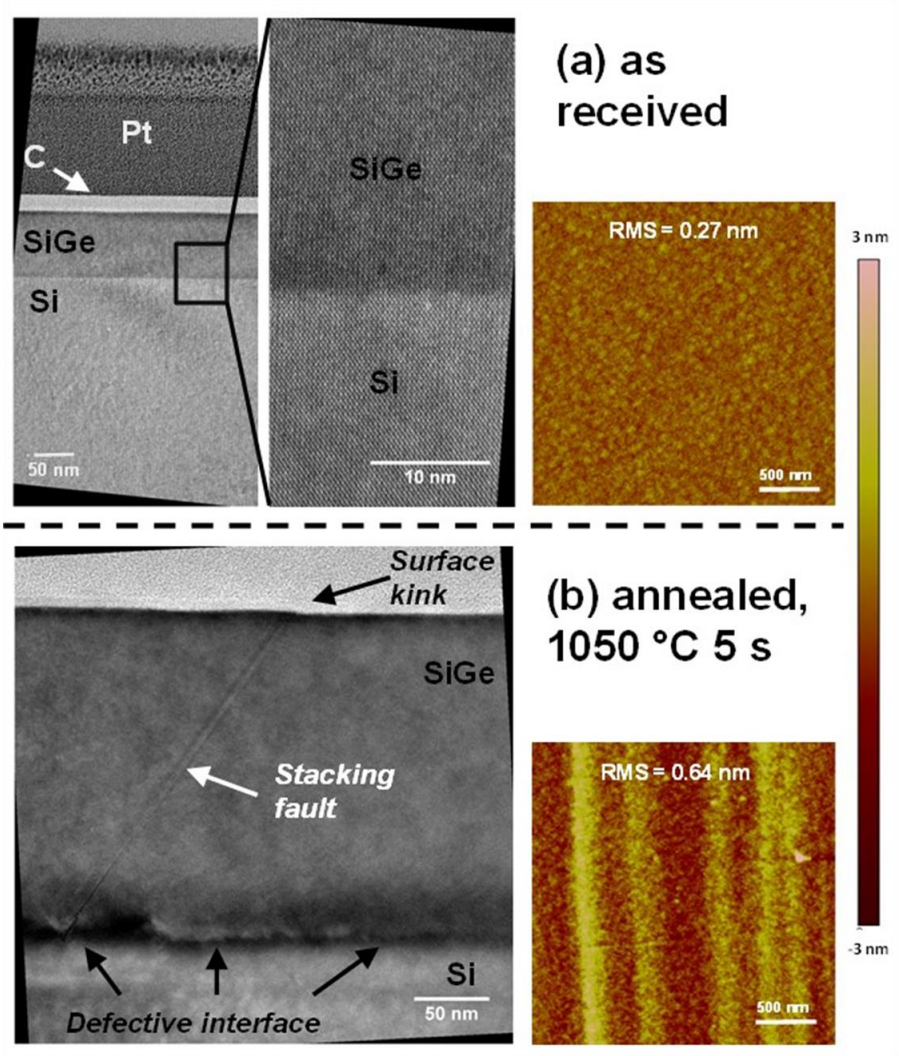


Figure 4: XTEM and AFM of as-received SiGe 30 % (top row) and SiGe 30 % after annealing at 1050 °C for 5 seconds (bottom row).

Due to this degradation it is assumed that a 1050 °C RTA used for Si cannot be applied to Ge, and thus we are unable to apply a constant RTA temperature across all the SiGe alloys studied here. Instead we have chosen an RTA temperature at a fixed amount below the melting temperature of each material, in accordance with **Figure 6.5**. As 1050 °C is routinely used for P in-diffusion into Si,[34] we used this as our basis for a constant T_{melt} - T_{RTA} (1416-1050 °C) value[56,57]. The RTA temperatures for 18, 30, and 60 % Ge content SiGe are thus 935, 835 and 685 °C respectively.

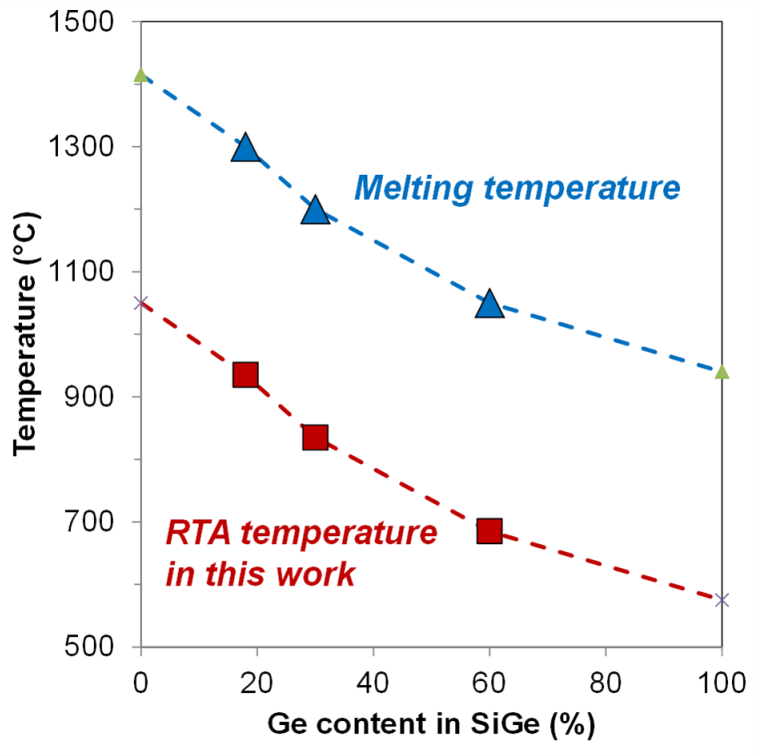


Figure 6.5: Melting temperature of SiGe as a function of Ge content. The dopant drive-in RTA was chosen to be a constant value below the melting temperature, also plotted here.[56,57]

6.4.2 Application of MLD to SiGe

6.4.2.1 AFM analysis of surface topology

Figure 6.6 shows AFM images of all SiGe samples before and after MLD processing. Samples before MLD show that the surface topology is very uniform, with RMS values <0.3 nm. MLD processing leads to a small increase in all RMS values which is to be expected with wet chemistry processing and cap addition/removal possibly leaving residue on the sample surface. Disregarding these residues due to processing which are clearly present on the 18 and 60 % after MLD, all surfaces are of good quality. Though not quantified it is clear that crosshatching can be seen in both the 30 and 60 % samples which is an indicator of the onset of strain relaxation. [40, 41]

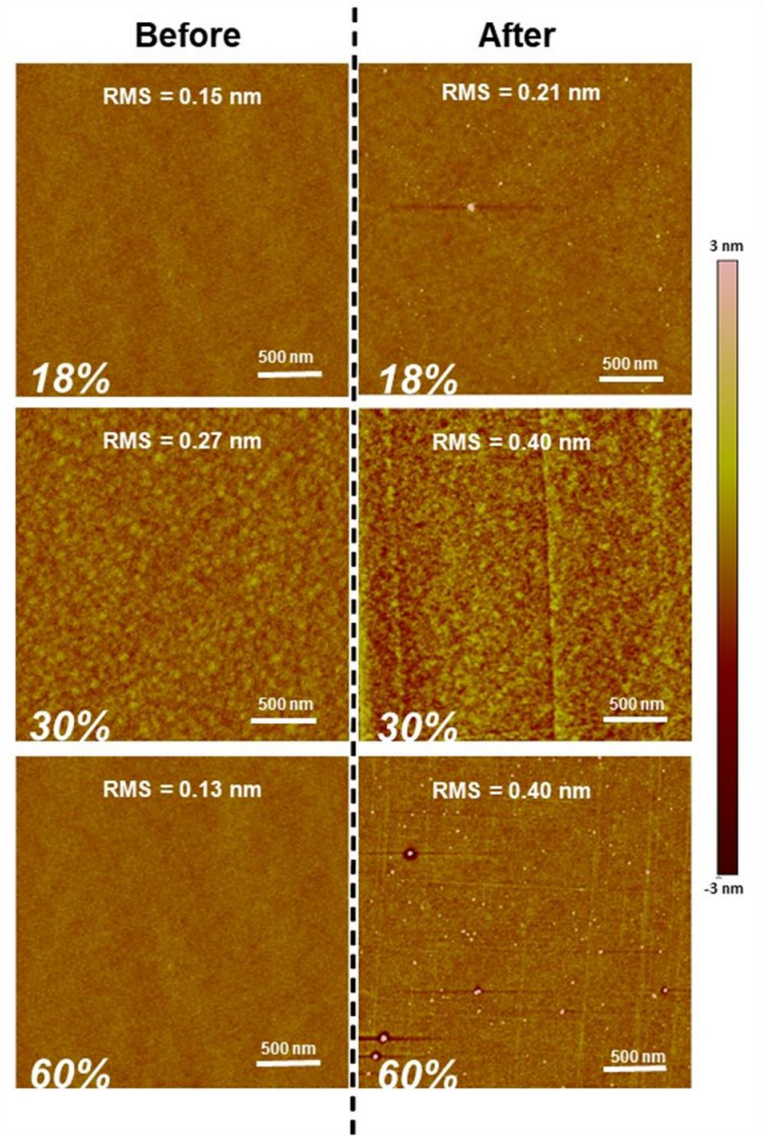


Figure 6.6: AFM before (left column) and after MLD (right column) of (a) 18% SiGe (b) 30% SiGe and (c) 60 % SiGe

The impact of MLD on SiGe sample quality was further probed using X-TEM. **Figure 6.7** shows images of SiGe 30 % before and after MLD. It is clear from these images that P-diffusion into the SiGe30 sample does not lead to any crystalline damage at the temperature used in this study. This agrees with numerous other studies which demonstrate MLD as a non-destructive doping technique. [26,42] The SiGe:Si interface in **Figure 6.7** does not show any evidence of defects which leads us to believe that the small amount of crosshatching seen in AFM after MLD is not of concern.

6.4.2.2 TEM analysis of crystal quality

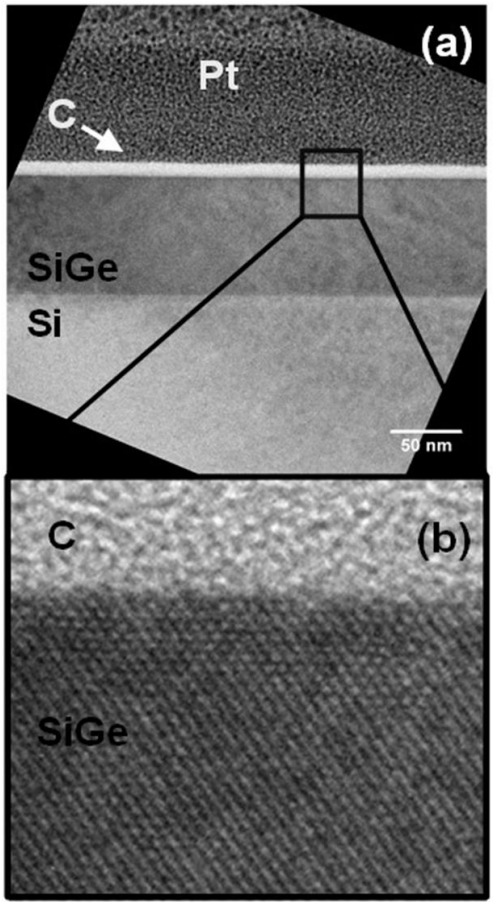


Figure 6.7: (a) XTEM of SiGe30 after MLD (b) Magnified region showing smooth interface and crystalline SiGe.

If defect formation as a result of strain relaxation of the SiGe layer was not considered problematic it would be possible to utilize higher anneal temperatures up to those seen in **Figure 6.4** (1050 °C). These higher anneal temperatures would theoretically enable higher in-diffusion and activation of the P dopant atoms. Previous studies on silicon have found that optimal RTA temperatures for P in-diffusion and activation were somewhere in the region of 1000-1100 °C.[26, 32] Another approach which may have the potential to reduce the probability of nucleating defects at the Si/SiGe interface seen

at higher anneal temperatures (**Figure 6.4**) is the use of buffer layers. These buffer layers include a gradual increase in germanium content which leads to a smaller lattice mismatch than what is seen in samples where high Ge content SiGe has been grown directly on Si. Alternative annealing methods such as laser annealing have also been shown to work effectively in combination with ion implantation to dope strained SiGe layers. [43] Combining laser annealing and MLD may prove to be a more suitable means than RTA, of achieving highly doped SiGe layers while maintaining the strained nature of the SiGe layer.

6.4.2.3 Dopant profiling with SIMS

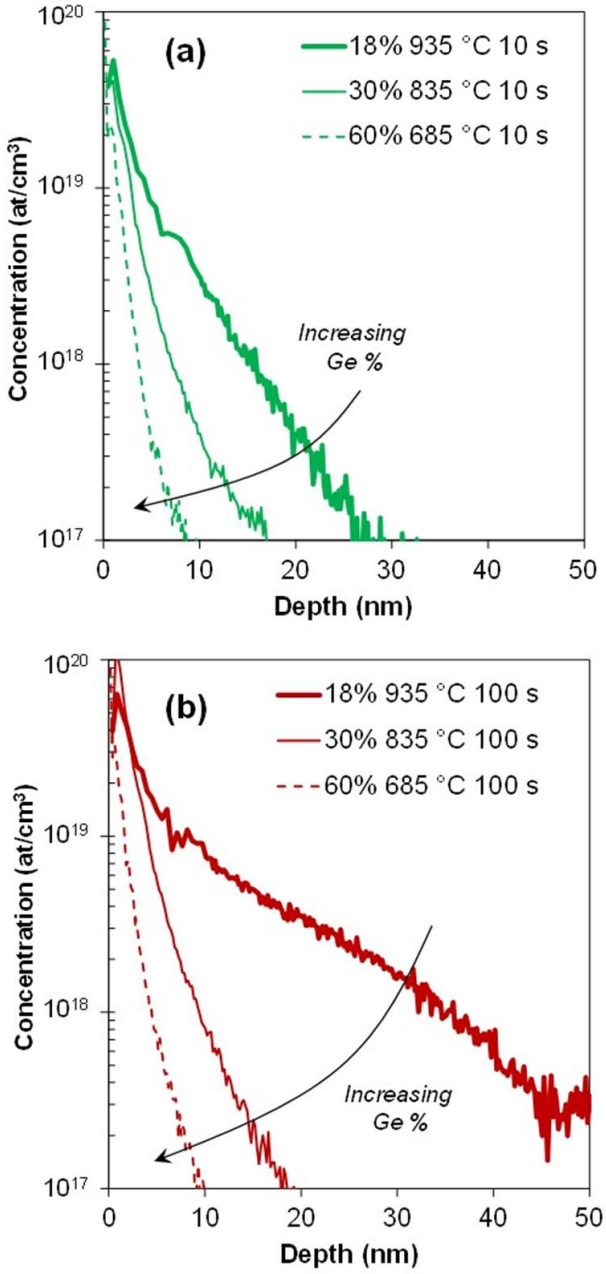


Figure 6.8: SIMS of P-MLD doped SiGe with concentration of 18 %, 30 % and 60 % with respective annealing temperatures of 935, 835, and 685 °C at annealing times of (a) 10 s (b) 100 s

Figure 6.8 shows SIMS analysis of the concentration of P versus depth for the SiGe samples doped using MLD. From both **Figure 6.8a** and **6.8b** we note that less P diffusion occurs as the Ge content increases, again within the experimental framework

of a constant T_{melt} - T_{RTA}, as the profiles for 18 % Ge content SiGe are deeper than those in 30 % Ge content SiGe, which are again deeper than those in 60 % Ge content SiGe. The longer anneal time produced more diffusion, which is consistent with theory, as dopant diffusion lengths are proportional to $\sqrt{t}$, where t is anneal time.[44] Based on the TEM images of the as-received SiGe layers, the dopant profiles in **Figure 6.8** are all contained within the SiGe layers, for the most part, and have not diffused into the underlying Si substrate.

6.4.2.4 Analysis of diffusion co-efficient and discussion

Figure 6.9 shows P-diffusivity (D) in SiGe as a function of Ge content, at the specific temperatures used for the drive-in anneal. The blue points are data extracted from our experiments, while the black points are the data we could find in literature for similar temperatures and material compositions.[45-49] . The two blue points represent values extracted from the two annealing times, namely 10 and 100 s, as shown in **Figure 6.8.**

Note that the literature value temperatures and Ge content correspond to the experimental data we have in this work. In the literature, phosphorus D is presented as a function of 1/kT, and so for the specific content (e.g. 18% Ge) we could read off the D value for the corresponding temperature in this work (e.g. 935 °C). Overall the values extracted from our data correspond with the trends previously reported in literature. D drops with increasing Ge content and decreasing RTA temperature when using a constant T_{melt} - T_{RTA}.

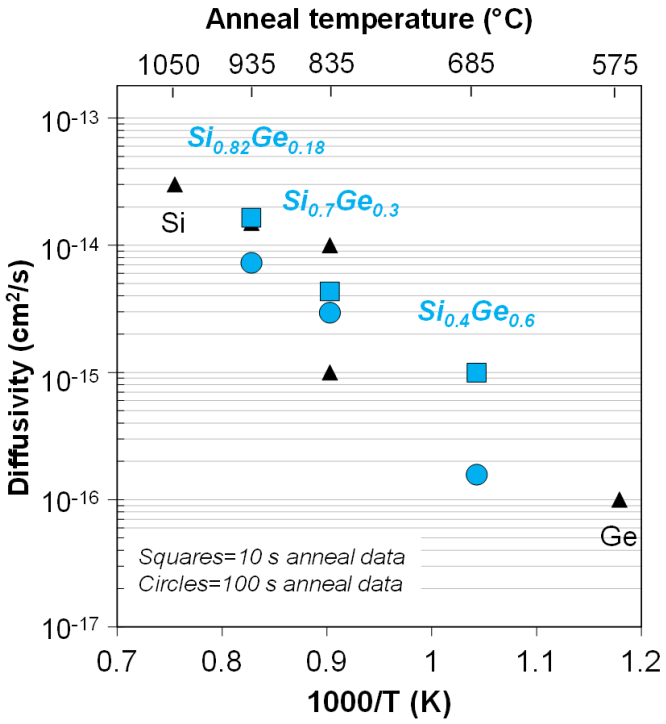


Figure 6.9: Phosphorus diffusivity in SiGe versus 1000/T extracted from our experiments (blue symbols) as well as literature values (black symbols). In this case T is the temperature of the drive-in anneal, which was kept at a constant value below the melting temperature of the material.

The method for extracting D for in-diffused doping profiles is now briefly summarized. The impurity concentration (C) profile for a chemical pre-deposition process has the form

$$C_{(x,t)} = C_s erfc\left(\frac{x}{2\sqrt{Dt}}\right) \qquad (1)$$

where x is the distance from the surface, t is time, C_s is the impurity surface concentration, and D is the impurity diffusivity. If D is constant, the depth of the profile depends only on time, and the surface concentration remains fixed as this is

limited by solid solubility limit at that processing temperature. If the total quantity of dopant is defined as dose, Q, then this can be described as

$$Q_{(t)} = \int_0^\infty C_{(x,t)} dx \qquad (2)$$

Using these two equations, the total incorporated dose can be simplified as

$$Q_{(t)} = \frac{2}{\sqrt{\pi}} C_s \sqrt{Dt} \qquad (3)$$

Using the SIMS analysis in **Figure 6.8**, Q and C_s can be extracted. Knowing the experimental processing time, t, means D is the only unknown, and thus can be calculated.

Factors that affect changes in dopant diffusivity in semiconductors include the relative dominance of interstitial-mediated or vacancy-mediated diffusion mechanisms, point defect populations, lattice strain, presence or absence of threading dislocations and their density, and finally the dose or supply of dopant. P diffusion in Si is predominantly interstitial-mediated,[50, 51] while P diffusion in Ge is vacancy-mediated.[45, 52] It is not clear presently at what point along the Ge % content axis where it changes from one mechanism to the other. From the evidence in **Figure 6.9** diffusivity changes quite linearly rather than reaching a toggle point or falling off a cliff, so probably the switch from interstitial or vacancy mediation is gradual.

Note that this is a simplified model for the purposes of our discussion, although it is well-known as a surface-source in-diffusion model. The system under study is very complicated considering the changing alloy composition will affect diffusion mechanisms, probability of dopant-point defect pairing, intrinsic concentrations of

those point defects, both charged and uncharged, as well the presence of strain and extended defects. It is not the aim of this work to go in depth into the changing diffusion mechanisms, as it would be another quite-substantial work. Furthermore, we have not explicitly considered a dependence of D on phosphorus concentration in this surface-source in-diffusion model, mainly as concentration enhancement effects usually arise at concentrations approaching or above 10^{20} at./cm^3 and we are below those concentrations in this work. Nevertheless, it is important to note that we have benchmarked our results with existing reports, and the data appear consistent.

The influence of strain should also be mentioned as these SiGe layers are grown directly on a Si substrate, without a strain-relaxed-buffer (SRB). Pakfar *et al.* modelled the effects of strain and Ge content on point defect population in SiGe,[53] which drive a change in dopant diffusivity. For P it was found that the effect of stress counterbalances the Ge chemical effect on interstitials, and thus the change in diffusivity is minimized. Note, we should state again that it was not the aim of this work to explore strain as one of the variables here, but rather to explore the choice of RTA temperature in the trade-off between successful dopant incorporation while avoiding epitaxial layer structural relaxation. Given the 2 orders of magnitude change in D as a function of RTA temperature, that is a dominant variable here.

As seen in the TEM and AFM data, with high thermal budgets threading dislocations will form in order to relax the strained layer. The threading dislocation density (TDD) will affect the diffusivity if the material is extremely defective as these defects could form preferential pathways for P atoms to diffuse.[54] However the data presented in **Figure 6.6** and **6.7** show that the TDD is less for the RTA temperatures considered in

Figure 6.8 and **6.9** than for the standard anneal temperature of 1050 ^{o}C. Although overall the TDD should not have a strong bearing on the conclusions in this work we cannot conclusively state that the trend in SIMS profiles in **Figure 6.8** are not contributed to by the TDD.

Finally, Si and Ge inter-diffusion has been modelled by Zechner and Zographos,[55] which may locally affect the SiGe composition close to the SiGe-Si interface. The change in Ge % content will have a knock-on effect on point-defect populations and hence point-defect mediated dopant diffusion, as discussed earlier. For the study here, namely in-diffusion from the top surface, the back interface of the SiGe (away from the source of the dopant) should only have a minimal effect on the dopant drive-in.

6.5 Conclusions and Outlook

This chapter has outlined the application of MLD to SiGe showing both the advantages of this form of doping and some of the issues which must be overcome for future use. Ultra-shallow doping has been achieved with phosphorus dopant atoms to levels currently in the region of 2×10^{19} atoms/cm^{-3}. Doping levels in excess of 1×10^{20} atoms/cm^{-3} are required for working devices and the authors are working on combining MLD with advanced annealing processes (e.g. laser annealing) to achieve these values. Diffusivity levels found during this study agree with values from literature for P diffusion in strained SiGe. Strain relaxation is a major issue when applying high thermal budget treatments to epitaxially grown SiGe/Si substrates. In this study we have optimized RTA temperatures for low to high Ge content SiGe samples to produce maximum doping levels without introducing strain relaxation into

the substrates. More advanced annealing methods or the use of buffer layers would allow for greater dopant incorporation while maintaining the strained nature of the SiGe layer.

6.5 References

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CHAPTER 7

Conclusions and Future Perspectives

7.1 Conclusions

The “more Moore” era has meant progression into the 7 nm and 5 nm technology nodes for logic device applications. Extreme demands are placed on all industries linked to integrated circuit technology for development of processes which are suitable for these dimensions. Transistor structures have developed from planar to 3-D finFets and are expected to move to gate-all-around structures in the next 5 years. These 3-D structures add complexity to doping strategies with a solution required that will have dose control, conformality, and no crystalline damage while maintaining high active carrier concentrations and ultra-shallow Xj. Although physical dimension scaling of CMOS is still progressing it is also necessary that power, performance and cost are concurrently improved. In order to make these improvements the channel material used is expected to change from Si to SiGe and then to Ge by 2025. Developing doping solutions which are capable of doping these materials without impacting their structural integrity is also of vital importance. This is where MLD has potential to provide an alternative option to traditional doping techniques.

Chapter 1 outlined why doping is necessary and what structure types this type of processing is being currently applied to and the future aims. The current state-of-the-art technologies for semiconductor doping are reviewed with the advantages and dis-advantages of each technique outlined. MLD has been proposed as an alternative

method of semiconductor doping and a comprehensive review of its development and current situation is provided. The majority of work to date on MLD has focused on P and B doping of Si with novel variations allowing for gas-phase MLD and non-contact MLD. Further work where alternative substrate types and alternative dopant types are also outlined. The volume of published work to date on MLD demonstrates that the technique is both popular and effective at producing nanoscale doping.

Chapter 2 described in detail the characterization methods that are used in the work that follows. An emphasis is placed on ECV, XPS, SIMS and AFM as they provide the backbone of the surface functionalization and doping results from MLD.

Chapter 3 described a systematic study carried out on P-MLD of Si substrates. This represents the first application of MLD to SOI and nanowire dimensions approaching what is used in current CMOS technology. Blanket Si results demonstrated a limitation on maximum active carrier concentration at $\approx 2 \times 10^{19}$ cm^{-3} through ECV and SIMS analysis. This result was validated through Hall-effect on SOI substrates. XPS analysis demonstrated that a degree of oxidation was present after functionalization of the Si surface with the P containing molecule. It was theorized that this SiO_2 presence and the use of an SiO_2 cap leads to limited incorporation of the P dopant atoms. The P-MLD process developed on blanket Si was transferred to SOI with film dimensions ranging from 66 nm to as low as 3 nm. C-TLM and µ-4pp analysis of these MLD doped substrates once again demonstrated resistivity values that equated to $\approx 2 \times 10^{19}$ cm^{-3} which are an order of magnitude lower than those from implantation. It was notable that all doping methodologies used struggled to achieve measurable resistance

values in sub 5 nm SOI which provides evidence to the theory that traditional impurity doping may struggle in this region. Further work on nanowire structures with P-MLD processing demonstrated that dopant activation levels were once again in this $\approx 2 \times 10^{19}$ atoms cm^{-3} region. However, this study did demonstrate the gentle nature of MLD showing no crystalline damage in nanowire substrates imaged by XTEM after doping whereas implanted samples showed noticeable defects which could not be removed with thermal treatments.

Chapter 4 showed how MLD on Si could be advanced through alternative cap types and changing dopant species. Sputtered Si_3N_4 capping was used to achieve activation levels approaching 10^{20} atoms cm^{-3} with P-MLD processing on blanket Si. ECV and SIMS demonstrated that Xj could also be tuned using RTA conditions with this capping approach. Surface roughness was monitored with AFM and showed only a minor increase after MLD with Si_3N_4 capping. A methodology for doping Si with As was then developed using As-acid as a dopant precursor. Click chemistry using 3,4 DCB as a click molecule proved relatively successful with maximum activation levels of 3×10^{19} atoms cm^{-3} demonstrated with a 5×10^{18} atoms cm^{-3} Xj of just 19 nm.

Chapter 5 described a novel method functionalizing Ge with As-acid through reaction with the Cl-terminated surface. XPS and DFT calculations were used to support formation of a covalent bond between the As-acid molecule and the Cl terminated Ge surface. DFT calculations suggest that the As-acid molecule will initially bind with one oxygen atom from the acid group attaching to one Ge atom in the (100) surface. This configuration then relaxes so that adsorption takes place through two oxygen

atoms in the molecule. The calculated adsorption energy of this configuration is -5.7 eV, with bond lengths decreasing after relaxation, that are consistent with strong adsorption. AFM demonstrated that Ge topology remains intact after each step of MLD processing. Active carrier concentrations analysed with ECV after MLD showed levels $\approx 2\times10^{19}$ atoms cm^{-3} which represent the maximum achieved concentrations through doping with conventional annealing. These values are twice as high as what was previously reported as the limit of As MLD on Ge. ECV results were validated with sheet resistance measurements. A control of Xj was once again demonstrated via MLD with variation of RTA time and temperature. Dose calculation from experimental and theoretical work show that As-acid, due to its smaller dimensions, provides an increased dose in comparison to the previously used triallylarsine.

Chapter 6 described the application of MLD to another prospective channel material in future CMOS devices, which was SiGe. This study initially focused on the material properties of the SiGe substrates with XPS and angle resolved XPS carried out to probe the relative composition of the SiGe films. The understanding of surface and bulk stoichiometries was essential for determining reaction conditions for functionalization. Further material studies with XTEM and AFM examined the ability of these SiGe films to withstand high temperature thermal treatments required for MLD dopant drive-in. These properties were taken into account when carrying out P-MLD processing and doping results were probed with SIMS. Results found demonstrated that phosphorus incorporation decreases for increasing mole fraction of Ge, when the RTA temperature is a fixed amount below the melting temperature of each alloy.

7.2 Future Perspectives

This thesis has systematically studied the application of P-MLD to planar and 3-D Si demonstrating carrier concentrations $\approx 2 \times 10^{19}$ atoms cm^{-3} which are suitable for channel doping in current and future node CMOS. Chapter 4 demonstrated that increased carrier concentrations approaching 10^{20} atoms cm^{-3} are achievable with P-MLD using a Si_3N_4 cap. These levels and higher are required for more heavily doped regions of the CMOS such as source and drain. Application of this methodology to nanostructures did not prove successful with cap addition and removal processes requiring optimization. To carry this work on for a future study, it would be interesting to optimize the Si_3N_4 cap addition and removal process from nanostructures followed by further electrical analysis. The use of capping materials has proven essential to MLD processing for optimal dopant incorporation/activation and therefore it is vitally important that MLD development coincides with the development of cap deposition and etch methodologies. The ability of MLD to conformally dope GAA structures in a non-line of sight manner should also be analysed and developed as this area is of significant concern to implantation. Further nanowire studies which include APT could prove the ability of MLD for this application.

The work carried out in Chapter 4 developing a method of As-MLD through the use of As-acid has shown the potential to develop new chemistries involving alternative dopant types. There is significant potential to further advance the functionalization work carried out with As-acid. Utilizing gas-phase chlorine reactors or systems capable of plasma formation with chlorine would potentially enable the formation of a Si-Cl surface which may be capable of carrying out the direct attachment of As-acid

in a similar manner to what is seen on Ge. As-acid provides a smaller MLD precursor option in comparison to triallylarsine and enables greater packing density and resultant dose. When considering MLD as an alternative to implantation for producing highly doped CMOS components it is reasonable that the only way is down when looking at molecule dimensions.

It is also possible that the click chemistry approach developed to functionalize Si with As-acid will allow for the formation of a mixed As/P monolayer. Some initial work on this topic has been carried out. but extensive development of this approach is required. Formation of mixed dopant monolayers allows for fine-tuning dopant properties such as diffusion and activation. Spectroscopy analysis of the resulting defects from each process would further benefit the field of MLD.

MLD on Ge is not as advanced as work on Si with publications limited to Sb, As and P. The work described in Chapter 5 demonstrates a novel functionalization method which is capable of introducing active dopant levels at the limit of RTA. To further this study, it would be interesting to process As-acid functionalized Ge with flash lamp annealing and laser annealing tools. It is possible that these tools will allow for higher activation levels to be achieved than what is seen with RTA.

A potential avenue for MLD development and application over the next decade is the area of quantum computing. This field requires the accurate placement of single dopant atoms which is not easily attainable through implantation. The development of molecular precursors for MLD that span a wide range of dimensions would enable

precise control of this dopant placement. Current work in this area has been carried out to develop extremely large molecules and it will likely prove a hot topic of research in the near future.

CHAPTER 8

Appendix

8.1 List of Publications

8.1.1 Work related to this thesis

Authorship contribution

Values shown in superscript with each author name correspond to the description shown below and give a general outline of the individual author contribution. Authorship contribution provided here is to the best of the author of this texts knowledge and is only for the papers related to this thesis.

1. Conceptualization
2. Modelling
3. Experimental – sample preparation
4. Experimental - characterisation
5. Data interpretation
6. Writing – Original drafts
7. Writing – Review
8. Funding acquisition

2018:

- Phosphorus monolayer doping (MLD) of silicon on insulator (SOI) substrates

Kennedy, N [1,3,4,5,6,7]; Duffy, R [1,5,6,7,8]; Eaton, L [3]; O'Connell, D [3]; Monaghan, S[4,5,7]; Garvey, S [4,5]; Connolly, J [8]; Hatem, C [8]; Holmes, J.D [8]; Long, B [1,5,6,7,8]. Beilstein Journal of Nanotechnology, 2018, 9: 2106-2113

- Diagnosis of phosphorus monolayer doping in silicon based on nanowire electrical characterisation

  Duffy, R [1,4,5,6,7,8]; Ricchio, A; Murphy, R; Maxwell, G; Murphy, R; Piaszenski, G; Petkov, N; Hydes, A; O'Connell, D; Lyons, C; **Kennedy, N [1,3,4,7]**; Sheehan, B; Schmidt, M; Crupi, F; Holmes, J.D; Hurley, P; Connolly, J; Hatem, C; Long, B [1,5,6,7,8]. Journal of Applied Physics, 123 123701 (2018).

2019:

- Monolayer doping of silicon-germanium alloys: a balancing act between phosphorus incorporation and strain relaxation

  Kennedy, N [1,3,4,5,6,7]; Duffy, R [1,5,6,7,8]; Mirabelli, G [4,]; Eaton, L [3]; Petkov, N [4,5]; Holmes, J.D [8]; Hatem, C [8]; Walsh, L [4,5,6,7]; Long, B [1,5,6,7,8]. Journal of Applied Physics 126, 025103

- Exploring conductivity in ex-situ doped Si thin films as thickness approaches 5 nm

  MacHale, J [1,3,4,5,6,7,]; Meaney, F [1,3,4,5,6,7]; **Kennedy, N [3,4,5]**; Eaton, L [3]; Mirabelli, G; White, M; Thomas, K; Pelucchi, E; Petersen, D; Lin, R; Petkov, N; Connolly, J; Hatem, C; Gity, F; Ansari, L; Long, B [1,5,7,8]; Duffy [1,4,5,6,7,8], R. Journal of Applied Physics, 125, 225709, (2019)

2020:

- Monolayer doping of germanium with arsenic: a new chemical route to achieve dose control and optimal dopant activation

  Kennedy, N [1,3,4,5,6,7]; Garvey, S [4,5]; Maccioni, B [2,5,6,7]; Eaton, L [1,3,4]; Nolan, M [2,5,6,7]; Duffy, R [1,5,7]; Meaney, F [1,4,7]; Kennedy, M [4,5]; Holmes, J.D [7]; Long, B [1,5,6,7]. Langmuir, (2020), 36, 34, 9993–10002

8.1.2 Other co-authored publications and conference papers

2018:

- Monolayer doping and other strategies in high surface-to-volume ratio silicon devices

  Duffy, R; **Kennedy, N**; Mirabelli, G; Galluccio, E; Hurley, P; Holmes, J.D; Long, B. 2018 18th International Workshop on Junction technology.

- AsH_3 gas phase ex situ doping of 3D silicon structures

  Duffy, R; Thomas, K; Galluccio, E; Mirabelli, G; Sultan, M; **Kennedy, N**; Petkov, N; Maxwell, G; Hydes, A; O'Connell, D; Lyons, C; Sheehan, B; Schmidt, M; Holmes, J.D; Hurley, P; Pelucchi, E; Connolly, J; Hatem, C; Long, B. Jorunal of Applied Physics, 124 (4) : 045703

- Electrical evaluation of ion implant, liquid, and gas sources for doping of ultra-thin body SOI and Si Nanowire structures

MacHale, J; Meaney, F; Sheehan, B; Duffy, R; **Kennedy, N**; Long, B. 22nd International Conference on Ion Implantation Technology (IIT)

- Tertiarybutylarsine damage-free thin-film doping and conformal surface coverage of substrate-released horizontal Si nanowires
  Meaney, F; Thomas, K; MacHale, J; Mirabelli, G; **Kennedy, N**; Connolly, J; Hatem, C; Petkov, N; Long, B; Pelucchi, E; Duffy, R. Applied Surface Science, Volume 508, April 2020, 145147.

- RF Plasma Monolayer Doping of Si Nanowires
  Nazarov, A; Gomeniuk, Y; **Kennedy, N**; Glotov, V; Okholin, P; Long, B; Nazarova, T, Duffy, R. 2019 IEEE 9th International Conference Nanomaterials: Applications & Properties (2019)

8.1.3 Conference presentations

2017:

- Critical analysis of phosphorus monolayer doping in silicon
  Kennedy, N; Holmes, J.D; Duffy, R; Long, B. European Materials Research Society (EMRS) Fall Meeting 2017, 18th-21st September 2017, Warsaw, Poland.

2018:

- Monolayer doping: A novel functionalization method through the vapour phase

Kennedy, N; Holmes, J.D; Duffy, R; Long, B. 22nd International Conference on Ion Implantation Technology (IIT 2018), 16th- 21st September 2018, Wurzburg, Germany.

8.1.4 Internship undertaken

- January-July 2019 at Applied Materials, Gloucester, Massachusetts, USA.