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The impact of forming gas annealing on the electrical characteristics of sulfur passivated $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) metal-oxide-semiconductor capacitors

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The impact of forming gas annealing on the electrical characteristics of sulfur passivated $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) metal-oxide-semiconductor capacitors

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This study reports the impact of forming gas annealing (FGA) on the electrical characteristics of sulfur passivated, atomic layer deposited Al_2O_3 gate dielectrics deposited on (110) oriented *n*- and *p*-doped $In_{0.53}Ga_{0.47}As$ layers metal-oxide-semiconductor capacitors (MOSCAPs). In combination, these approaches enable significant Fermi level movement through the bandgap of both *n*- and *p*-doped $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs. A midgap interface trap density (D_{it}) value in the range $0.87 - 1.8 \times 10^{12}\,cm^{-2}eV^{-1}$ is observed from the samples studied. Close to the conduction band edge, a D_{it} value of $3.1 \times 10^{11}\,cm^{-2}eV^{-1}$ is obtained. These data indicate the combination of sulfur pre-treatment and FGA is advantageous in passivating trap states in the upper half of the bandgap of (110) oriented $In_{0.53}Ga_{0.47}As$. This is further demonstrated by a reduction in border trap density in the *n*-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs from $1.8 \times 10^{12}\,cm^{-2}$ to $5.3 \times 10^{11}\,cm^{-2}$ as a result of the FGA process. This is in contrast to the observed increase in border trap density after FGA from $7.3 \times 10^{11}\,cm^{-2}$ to $1.4 \times 10^{12}\,cm^{-2}$ in *p*-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs, which suggest FGA is not as effective in passsivating states close to the valence band edge. *Published by AIP Publishing.*
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Due to the fundamental scaling limits of Si complementary-metal-oxide-semiconductor (CMOS),[1] innovations based around new materials and device architectures are required to facilitate improvements in transistor performance, and extend the logic device and more than Moore roadmaps. The first of these innovations has seen the device architecture evolving to become non-planar in the form of tri-gate metal-oxide-semiconductor field-effect-transistors (MOSFETs) and fin field-effect-transistors (FinFETs),[2] which have become the mainstream in CMOS since the 22 nm technology node. Future scaling, beyond critical geometries of 10 nm, will require the introduction of high-mobility channels to sustain performance at reduced supply voltages.[3] III-V compound semiconductors have garnered significant interest due to their superior electron transport properties in this regard.[3] This has led to a number of non-planar device demonstrations, including InGaAs FinFETs and nanowire MOSFETs, on (100)-oriented substrates.[4–6] In these devices, the gate stack is formed over both the top and sidewalls of the fin/wire, with the latter having (110) or (111) surface orientations. As such, passivation techniques to engineer a high quality gate stack on a variety of surface orientations are essential to realising high performance non-planar InGaAs-channel devices.

Numerous approaches including sulfur-based chemical cleans,[7,8] As_2 capping and decapping,[9] trimethylaluminum (TMA) pre-dosing,[10] cyclic plasma (H_2 or N_2) and TMA exposures,[11,12] and AlN interface control layer[13] have been explored to passivate InGaAs (100) surfaces prior to atomic layer deposition (ALD) of high-*k* gate dielectrics. Of these surface preparation methods, ammonium sulfide ($(NH_4)_2S$), a wet chemical treatment, has demonstrated interface trap density (D_{it}) below $10^{12}\,cm^{-2}eV^{-1}$ around the mid-gap energy.[14] Wet sulfur treatment has also been reported to be an effective passivation technique on InGaAs (111) surfaces, resulting in an interface quality comparable to that achieved on sulfur-treated InGaAs (100) surfaces.[15] In the case of InGaAs (110) surfaces, D_{it} in the order of $2 - 4 \times 10^{12}\,cm^{-2}eV^{-1}$ was achieved for surfaces prepared by means of cyclic atomic H cleaning and TMA pre-dosing.[16] However, as yet, there has been no exploration into the effectiveness of wet sulfur treatments on InGaAs (110) surfaces. It is therefore timely to observe the impact of this sulfur-based approach to the interface between Al_2O_3 grown by ALD and (110)-oriented *n*- and *p*-type $In_{0.53}Ga_{0.47}As$ and in addition to evaluate the role of forming gas annealing (FGA), which has been widely used to lower D_{it} in both SiO_2/Si[17] and high-*k*/InGaAs (100)[18] systems.

Wafers comprising of *p*-type Be-doped ($4 \times 10^{17}\,cm^{-3}$) and *n*-type Si-doped ($4 \times 10^{17}\,cm^{-3}$) $In_{0.53}Ga_{0.47}As$ (110) layers with a thickness of 200 nm grown by molecular beam epitaxy (MBE) on p^+ and n^+ InP (110) substrates, respectively, were used in this study. Samples from both wafers were initially degreased for 1 min each in acetone, methanol, and isopropanol. Following treatment in $(NH_4)_2S$ (10% in deionised H_2O) for 20 min at room temperature (~295 K), samples were transferred to the ALD chamber within ~3 min after removal from the sulfur solution. Films of Al_2O_3, with a nominal thickness of 8 nm, were grown by

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ALD at 300 °C using alternating pulses of TMA and H_2O precursors, with TMA being the first pulse in the process. Metal-oxide-semiconductor capacitors (MOSCAPs) were fabricated by electron-beam evaporation of Pt/Au through a shadow mask for gate contacts, and completed with Au/Zn/Au or Au/Ge/Ni/Au ohmic contacts to the back of the *p*- and *n*-type samples, respectively. Post-metallisation FGA was performed in a H_2/N_2 (5%/95%) ambient for 30 min at 350 °C. Electrical measurements were performed on-wafer in a microchamber probe station (Cascade, Summit 12971B) in a dark, electrically shielded environment using an impedance analyser (Agilent E4980A).

Fig. 1 shows the room temperature frequency-dependent (1 kHz to 1 MHz) capacitance-voltage (*CV*) characteristics of sulfur passivated *p*- and *n*-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs before and after FGA. A qualitative assessment of the samples prior to FGA reveals a larger frequency dispersion in the accumulation region of the *p*-type (110) MOSCAP, akin to that observed in $In_{0.53}Ga_{0.47}As$ (100) MOSCAPs.[7] The observed dispersion is ascribed to the tunnelling of carriers into electrically active, near interface border traps in the oxide,[19–21] and fast interface states.[22,23] The larger frequency dispersion in the depletion region of the *p*-type MOSCAP also suggests a higher density of interface traps in the lower half of the bandgap. Following FGA, the frequency dispersion in accumulation and depletion is marginally improved for the *p*-type MOSCAP. Notably though the *CV* response is seen to plateau as the gate bias is increased to more positive voltages as shown in Fig. 1(c). This behaviour is consistent with a genuine minority carrier response in inversion as opposed to a defect-dominated response.[24] The transition frequency, defined as the capacitance in inversion that is half way between the highest capacitance measured at low frequency and the lowest capacitance measured at high frequency, and for which the frequency scaled measured conductance (G_m/ω) is also a maximum, provides a measure of the minority carrier response time (τ_R).[24] For the *p*-type MOSCAP after FGA, G_m/ω (not shown) is at a maximum at a transition frequency of 3 kHz, from which τ_R is estimated as 0.25 ms. This value is comparable with a τ_R of ~1 ms reported on MBE grown InGaAs (100), for which inversion was observed.[25,26] In the case of the *n*-type MOSCAP, the frequency dispersion in accumulation and depletion and the *CV* stretch-out are noticeably reduced following the FGA treatment. These observations can be interpreted as reduced D_{it} in the bandgap as a consequence of the FGA process.

For quantitative analysis, D_{it} distributions of the MOSCAPs pre- and post-FGA were determined using a temperature modified version[7] of the combined high-low frequency *CV* method.[24] In this approach, the low-frequency capacitance measurement was obtained at 100 Hz at room temperature while the high frequency measurement of 1 MHz was obtained at a reduced temperature of –50 °C to minimise the interface defect response to allow for a more accurate estimation of D_{it}. It is further crucial to obtain an accurate estimate of the oxide capacitance (C_{ox}) as this has a direct bearing on the accuracy of the extracted D_{it}. Often C_{ox} is deduced from the maximum accumulation capacitance, which is prone to error due to the effects of density of states and charge quantisation in the semiconductor[27] which is compounded by interface states and border traps.[14,22,23] An alternative is to calculate C_{ox} based on the dielectric constant (k) and physical dielectric thickness obtained from transmission electron microscopy. This can also be erroneous given the uncertainty of the k-value of Al_2O_3, reported to be between 7 and 9 in literature, resulting in an assumed value of the dielectric constant to be used in the calculation. In addition, there could be an interfacial transition region between the InGaAs and the Al_2O_3, whose dielectric constant is not known. Instead, here we derived the value of C_{ox} for each sample by comparing the experimental and modelled *CV* curves. The modelling was based on the work of

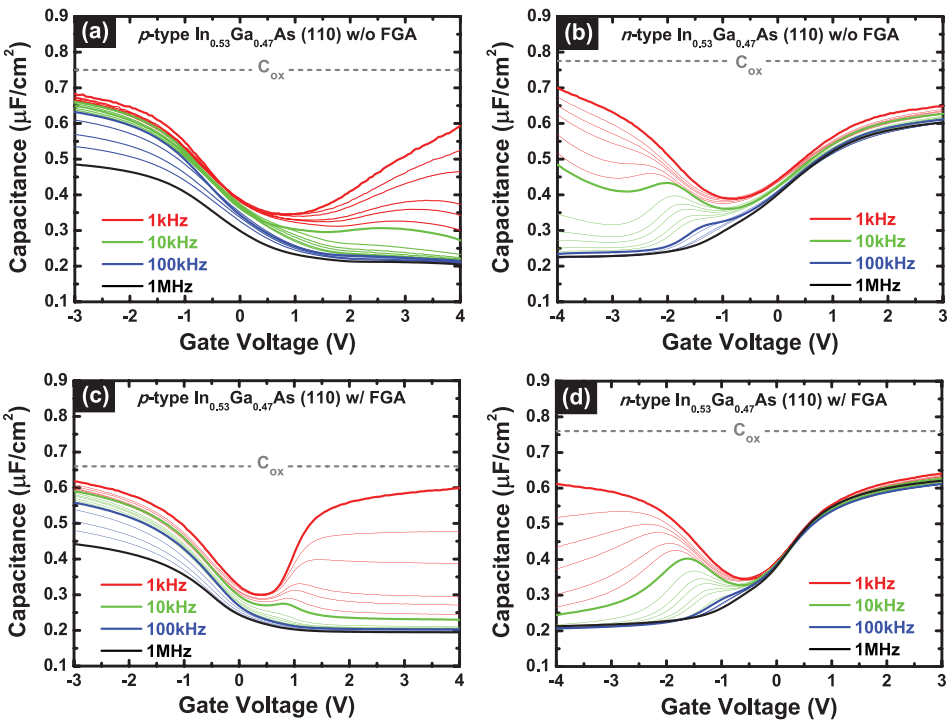


FIG. 1. Multifrequency (1 kHz to 1 MHz) room temperature *CV* responses of Au/Pt/Al_2O_3/$In_{0.53}Ga_{0.47}As$ (110) MOSCAPs: (a) *p*-type and (b) *n*-type before FGA, and (c) *p*-type and (d) *n*-type after FGA. The C_{ox} values derived from a comparison between experimental and modelled *CV* curves are indicated as horizontal lines.

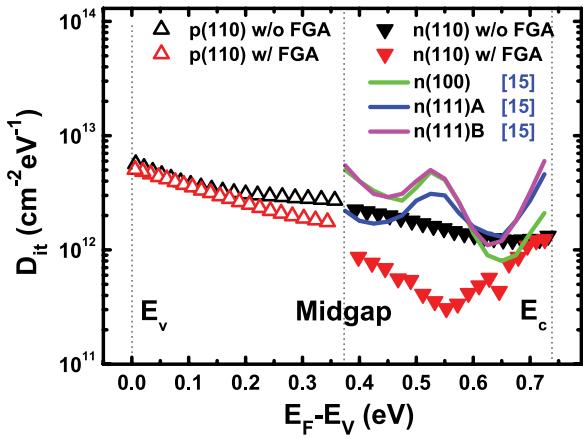


FIG. 2. Extracted D_{it} profiles of *p*- and *n*-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs before and after FGA. For comparison, the D_{it} distributions of sulfur passivated *n*-type $In_{0.53}Ga_{0.47}As$ (100), (111) A and (111B) surfaces from Ref. 15 are shown.

Engel-Herbert *et al.*,[28] and the obtained C_{ox} values are indicated as horizontal lines in Fig. 1. Fig. 2 shows the D_{it} distributions of the *p*- and *n*-type MOSCAPs before and after FGA as a function of the surface potential (ψ) determined from the Berglund integral.[29] As the surface potential for the flatband voltage (V_{fb}) is known, i.e., $\psi(V_{fb}) = 0$, the integral was split into two parts: one integrating from flatband to accumulation and the other from flatband to weak inversion. The flatband voltage used in the integral, and in subsequent analysis, was based on the flatband capacitance calculated using the value of C_{ox} derived from the aforementioned technique. From the extracted profiles, the midgap D_{it} of the *p*- and *n*-type (110) samples before (and after) FGA are estimated to be 2.7×10^{12} (1.8×10^{12}) $cm^{-2}eV^{-1}$ and 2.2×10^{12} (8.7×10^{11}) $cm^{-2}eV^{-1}$ respectively. Furthermore, the trap density close to the conduction band is reduced by almost an order of magnitude after the FGA treatment, resulting in a D_{it} of 3.1×10^{11} $cm^{-2}eV^{-1}$. For comparison, the D_{it} profiles of sulfur passivated *n*-type $In_{0.53}Ga_{0.47}As$ (100) and (111) MOSCAPs[15] are plotted in Fig. 2. It is notable that D_{it} distributions in the upper half of the bandgap are comparable between the different surface orientations of $In_{0.53}Ga_{0.47}As$.

In addition to D_{it}, the impact of FGA on the border trap response of samples was analysed by means of hysteresis exhibited in the *CV* characteristics.[30] The *CV* hysteresis responses were measured at room temperature starting from inversion and sweeping towards accumulation, followed by sweeping back towards inversion. To minimise the contribution of D_{it} to the *CV* responses, the bi-directional sweeps were performed at a high frequency measurement of 1 MHz.[7] Shown in Fig. 3(a) and 3(b) are the bi-directional *CV* sweeps for the *p*- and *n*-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs, respectively, obtained under increasing maximum gate bias in accumulation (V_{max}) before and after FGA. The *CV* hysteresis is derived from the difference in V_{fb} between the upward and downward sweep of a measurement. A linear increase in the *CV* hysteresis with increasing V_{max} is noted from the insets of the figures, suggesting an increase in the trapped charge density as the Fermi level is moved

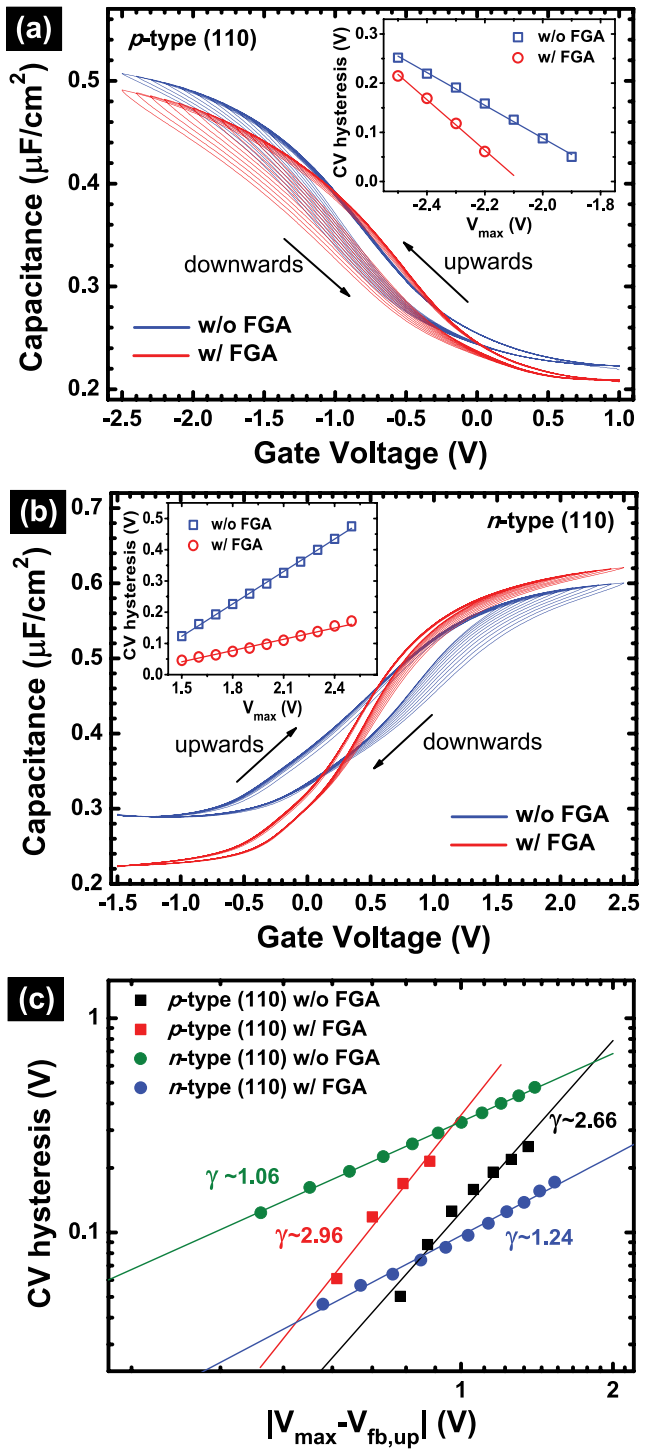


FIG. 3. Bi-directional 1 MHz *CV* sweeps recorded at room temperature for (a) *p*-type and (b) *n*-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs, before and after FGA, using the same starting gate bias in inversion and increasing maximum gate bias in accumulation (V_{max}), with plots of *CV* hysteresis as a function of V_{max} shown in the insets, and (c) *CV* hysteresis as a function of $|V_{max} - V_{fb,up}|$ plotted in log-log scale for *p*- and *n*-type $In_{0.53}Ga_{0.47}As$ (110) samples, before and after FGA.

towards the band edges. For both *p*- and *n*-type samples, the FGA treatment results in a reduction in the *CV* hysteresis. In the case of the *p*-type sample, the reduction in hysteresis after the FGA treatment becomes more pronounced with decreasing V_{max}. This is in marked contrast to the *n*-type sample for which the FGA treatment results in a significant reduction in *CV* hysteresis with increasing V_{max}. From the

log-log scale plot of Fig. 3(c), it is further observed the CV hysteresis follows a power-law of $|V_{max} - V_{fb,up}|$ (where $V_{fb,up}$ is the flatband voltage of the upward measurement sweep) for all samples. The voltage acceleration factor (γ), marked in the plot, is given by the exponent of the power-law dependence and is found to improve for both *p*- and *n*-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs after FGA. The steeper voltage acceleration is indicative of a narrower border trap distribution (assuming a normal distribution), which can be seen as a projection of improved reliability at lower operating voltages.[31] The level of charge trapping in the samples can be quantified as

$$N_t = \frac{C_{ox} \times \Delta V}{q}, \quad (1)$$

where N_t is the trapped charge density (cm^{-2}), ΔV is the *CV* hysteresis, and q is the electronic charge. For a valid comparison between the samples, N_t must be obtained under the same electric field across the oxide.[30] This means ΔV in Eq. (1) should be evaluated at the same value of $|V_{max} - V_{fb,up}|$. If $|V_{max} - V_{fb,up}|$ is taken as 1.1 V, the trapped charge density before (and after) FGA is estimated to be 7.3×10^{11} (1.4×10^{12}) cm^{-2} for the *p*-type MOSCAP and 1.8×10^{12} (5.3×10^{11}) cm^{-2} for the *n*-type MOSCAP. It is noted that *CV* hysteresis measured at 1 MHz does not capture all border traps, as in practical devices, border traps exist into the oxide, and the density can vary with depth into the oxide, as well as with energy.[32] In a *CV* sweep, the fast traps, which can respond at frequencies up to the low GHz range, would have emitted the trapped charge just as the reverse sweep is initiated. In addition, a significant quantity of charge is lost during the reverse *CV* sweep. As a consequence, the trapped charge measured from *CV* hysteresis only samples a certain portion from the total population of border traps, whose time constants are comparable to, or longer than, the time associated with the *CV* sweep. However, it remains a useful approach to explore how the border traps with long time constants vary with FGA.

This study shows that in combination, a wet sulfur pre-treatment prior to atomic layer deposition of Al_2O_3 together with a post-metal deposition FGA, enables significant Fermi level movement through the bandgap of (110) oriented *n*- and *p*-doped $In_{0.53}Ga_{0.47}As$ MOSCAPs. Quantitatively, a midgap D_{it} value in the range $0.87 - 1.8 \times 10^{12}\,cm^{-2}eV^{-1}$ is obtained from both the *p*- and *n*-type samples studied. Close to the conduction band edge, a D_{it} value of $3.1 \times 10^{11}\,cm^{-2}eV^{-1}$ is obtained. These data are in agreement with previous reports from (100) and (111) oriented *n*-doped $In_{0.53}Ga_{0.47}As$ MOSCAPs, indicating the combination of sulfur pre-treatment and FGA is advantageous in passivating trap states in the upper half of the bandgap. This is further demonstrated by a reduction in border trap density in the *n*-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs from $1.8 \times 10^{12}\,cm^{-2}$ to $5.3 \times 10^{11}\,cm^{-2}$ as a result of the FGA process, as determined from *CV* hysteresis trapped charge at a bias of 1.1 V beyond the flatband voltage. This is in contrast to the observed increase in border trap density after FGA from $7.3 \times 10^{11}\,cm^{-2}$ to $1.4 \times 10^{12}\,cm^{-2}$ for similar bias stress conditions in *p*-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs, which suggest FGA is not as effective in passsivating states close to the valence band edge.

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