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The Structural and Electrical Characterization of a $HfErO_x$ Dielectric for MIM Capacitor DRAM Applications

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Abstract

Hafnium Erbium Oxide ($HfErO_x$) thin films were formed using Atomic Layer Deposition. The effect of using different Hf:Er pulse ratios on the electrical and structural properties of the $HfErO_x$ thin films (~9nm) in metal-insulator-metal (MIM) capacitor structures have been investigated and comparisons made between as-deposited and annealed samples. We report the stabilisation of the higher dielectric constant (k) tetragonal/cubic phase by optimising the Hf:Er pulse ratio. The dielectric properties post thermal anneal at 500^{o}C were studied. A leakage current in the order of ~1 x 10^{-8} (A/cm^2) at a voltage of 1V and a capacitance equivalent thickness of ~1.4nm have been achieved post thermal annealing at 500^{o}C

1. Introduction

Metal-insulator-metal (MIM) capacitors play an essential role in dynamic random access memory (DRAM) and logic applications [1, 2]. With the on-going scaling of the minimum device dimensions of logic and memory devices, the choice of the dielectric incorporated into these MIM capacitors is critical [3]. Currently, the semiconductor roadmap requires film properties to be superior to those of silicon nitride in two distinct areas. First, the leakage current must be in the order of 10^{-8} A/cm^2 and secondly a capacitance equivalent thickness (CET) in the sub-nanometer range is required. To achieve these demanding dielectric targets high dielectric constant (high-*k*) thin films must be used, and an increasing amount of research activity is now focussed on the integration of different high-*k* materials to achieve the target values for optimum dielectric constant and leakage current density [3,4].

Hafnium Oxide (HfO_2) is now used as a gate dielectric [5] for logic CMOS due to its high dielectric constant, chemical and thermal stability and the resulting low gate current leakage. Erbium is a rare earth element which has been used in laser applications because of its optical properties but has found only limited use in semiconductor devices [6] as well as MOS Structures [7]. It has been shown that doping HfO_2 with rare earth elements can reduce the leakage current and increase the *k* value in Metal Insulator Silicon (MIS) capacitors [8]. High-*k* films have been deposited on silicon substrates using physical vapor deposition (PVD) [9] but recently Weimer et al. have fabricated MIS structures with Er doped (~15%) HfO_2 thin films using Atomic Layer Deposition (ALD) [10]. In this paper we examine Er doped HfO_2 films containing a range of different Hf to Er ratios

deposited by ALD and incorporated into MIM structures for potential DRAM applications. Structural characterization of the $HfErO_x$ films have been performed using transmission electron microscopy (TEM) and X-ray diffraction (XRD). Capacitance-voltage and current-voltage analysis have been used to electrically access the different $HfErO_x$ MIM structures.

2. Experimental and Sample Details

The MIM layers were deposited onto an n-type Si (100) wafer with n+ type As surface doping (~$5x10^{19}$ cm^{-3}). TiN (10nm) was deposited by metal organic chemical vapour deposition (MOCVD) and $HfErO_x$ films of varying Hf:Er pulse ratios were deposited by ALD in a ASM Pulsar 2000, hot wall cross flow reactor, at a deposition temperature of 325^oC using bis(methylcyclopentadienyl)methoxymethyl hafnium (HfD-04, SAFC Hitech), tris(2,2,6,6-tetramethyl-3,5-heptanedionato) erbium, ($Er(thd)_3$, SAFC Hitech), and Ozone as precursors. The samples were formed with nominal Hf:Er pulse ratios of 1:1, 4:1 and 8:1. The samples were given a Rapid Thermal Anneal (RTA) in a Jipelec Jetfirst 150 system for 60s in N_2 (1000-mbar pressure) at 500^oC. Blanket un-annealed and annealed samples were used for comparative physical measurements. Test structures were then fabricated to replicate a DRAM MIM Capacitor structure using a lithography and lift off process, with a range of top metal areas from 400 μm^2 to $1.6x10^5$ μm^2. The top metal electrode consisted of Ti(10nm) and Al(200nm) formed in sequence using e-beam deposition. The metals used to form the upper and lower electrodes are all CMOS compatible and meet current industrial standards [11].

Samples for TEM examination were made using the H-bar technique [12] and milled to electron transparency in an FEI 200 workstation. Final milling was performed at a beam current of 11pA. The samples were examined at 200eV using a range of microstructural characterization techniques in a JEOL2010. The XRD system used was PANalytical X'Pert Pro MPD X-ray diffractometer with CuK_{α} radiation. 1° incident angle and detector scan mode was used for the running conditions. Current Voltage (I-V) and Capacitance Voltage (C-V) measurements were carried out using a HP4156B precision Semiconductor Parameter Analyser and a HP4284A precision LCR meter respectively. All electrical measurements were taken from a wafer at 25^{o}C in a micro-chamber probe station (Cascade Micro-tech model Summit 12561B) in a dry air environment.

3 Experimental Results

3.1 TEM Analysis

TEM was used to assess the layer microstructure and the thickness of the as-deposited samples. Figures 1(a), 1(b) and 1(c) show typical regions of the capacitor structure for which the Hf:Er ratios are 1:1, 4:1 and 8:1 respectively. The 25nm amorphous oxide formed below the TiN electrode was found to be heavily As doped and to be characteristically inhomogeneous containing a number of different sub-layers consistent with the locally variable As doping. The TiN bottom electrode which was found to be similarly irregular has a low density band at its center whilst exhibiting the formation of more localised regions that extend into the underlying As doped oxide to depths of up 18nm. The as-deposited $HfErO_x$ layers were found to be crystalline, in agreement with Böscke et al [13] who made similar observations for HfO_2 films deposited at thicknesses

greater than 7nm.The thickness and grain size of the $HfErO_x$ layers are shown in Table 1 as a function of the Hf:Er ratios. As the Er concentration is reduced, the thickness of the dielectric layer remain almost constant but the grain size increases as is evident in Fig 1. Table 1 also shows that the grain size of the $HfErO_x$ increases upon annealing. Given that the layer thickness of the $HfErO_x$ films are constant as a function of the Hf:Er pulse ratio, within experimental limitations, any significant capacitance changes can be attributed to changes in the *k* value of the dielectric.

3.2 XRD Analysis

The XRD data for the as-deposited samples are shown in Figure 2 for which there are a number of differences as a function of the Hf:Er layer concentration. The 8:1 Hf:Er samples exhibit two distinct peaks corresponding to the monoclinic HfO_2 phase at 2θ 28.5^o and the tetragonal/cubic HfO_2 phase at 2θ 30.5^o [13]. The 1:1 Hf:Er and 4:1 samples by comparison show only one peak, at 2θ 30.5^o thus indicating that the monoclinic phase which has been suppressed with increasing erbium concentration. The addition of erbium also leads to a slight shift of the diffraction peak at 2θ 30.5^o towards the (222) plane of the Er_2O_3 cubic phase at 2θ 29.5^o [14]. This shift of the cubic/tetragonal peak seen in the 1:1 sample could be due to the large erbium content resulting in the presence of the cubic phase of pure Er_2O_3. The presence of cubic Er_2O_3 phase within the dielectric could explain the lower *k* value of the 1:1 sample compared with the 4:1 sample. Moreover, the monoclinic phase was not detected in the Hf:Er 1:1 sample yet the measured capacitance was comparable to the Hf:Er 8:1. As the Er_2O_3 content in HfO_2 is increased, the $HfErO_x$ film *k* value will be reduced as the contribution of the pure ErO_2 (*k* of Er_2O_3 ~ 12-14) to the overall film dielectric constant will be more significant.

3.3 Electrical Characterisation

Figure 2 shows the C-V response for the $HfErO_x$ MIM structure with a Hf:Er ratio of 8:1 following an RTA anneal (area=$1x10^4um^2$) at 500^{o}C. The measurement frequency was ranged from 1 kHz to 1MHz and the oscillation level was 0.05V. The capacitance was measured using both the Cs-V (Series) and Cp-V (parallel) modes, and Figure 3. illustrates the effect of the ac signal frequency and the equivalent circuit mode.

Before discussing the multi-frequency capacitance voltage (C-V) response, it is important to note the difference observed between the C-V characteristics in the series and the parallel modes. A perfect capacitor will yield identical C-V characteristics irrespective of the mode employed. However, when the measured capacitor presents resistive components due to resistance in series or leakage through the dielectric, this will cause divergence of the two measurement modes. When measured in Cp-V mode, a capacitor with a significant series resistance component will exhibit a strong dispersion with the measurement frequency i.e. the measured capacitance will significantly decrease at high frequency (100kHz-1MHz). The Cs-V mode should cancel the series resistance effect and the extracted capacitance should be frequency independent. Figure 3 shows the Cs-V mode applied to these capacitors reduces the dispersion with frequency but it is not totally cancelled which indicates the presence of other resistive (possibly frequency dependent) components contributing to the overall impedance of the MIM capacitor under test. Nevertheless, the Cs-V and Cp-V measured at 1 kHz are identical suggesting that the resistive components have been minimised when using at the lowest measurement frequency (1 kHz). In addition to the frequency dispersion, the CV characteristic is asymmetric and this behaviour is more pronounced at low frequency.

The asymmetry in the CV could be related to the form of the bottom electrode. The TiN making up the bottom electrode has been deposited on a highly doped oxide layer formed as a result of the substrate doping process. The CV data was obtained using the Si substrate as the bottom electrode. This structure could behave as a non ideal MOS structure in series with the MIM capacitor under study and cause the observed asymmetry. Due to the non ideal nature of the test structure used in this study, all the following discussion and analysis is based on the capacitance values measured at 0V and a measurement frequency of 1kHz, where the series and parallel circuit modes yield the same capacitance value. Similar measurement conditions were used in a recent study [15]. Figure 4 summarises the CV characteristics (measured at 1 kHz) for the three pulse ratios investigated in this study. The C-V plots show that there is very little difference in the capacitance between the Hf:Er pulse ratios of 1:1 and 8:1. In addition, the thermal anneal can be seen to have no significant impact on the capacitance values. However, when the Hf:Er pulse ratio is 4:1, the capacitance value increases significantly but reduces slightly following the post deposition anneal. The capacitance for the Hf:Er 4:1 sample was measured down to 200Hz and no further significant increase in capacitance was observed.

Figure 5 summarises the current density for all the samples. The measurements were carried out at 25^{o}C, a long integration time was used and a delay time of 5 seconds was applied. The data shows that for the as deposited Hf:Er 1:1 and Hf:Er 8:1 samples, the leakage current at 1V is approx 10^{-9} A/cm^2. At the same voltage the Hf:Er 4:1 sample has a leakage current of 10^{-8} A/cm^2. The leakage current of the Hf:Er 1:1 sample deteriorates significantly after anneal to 10^{-4} A/cm^2. Conversely, the Hf:Er 8:1 and 4:1 samples maintain similar leakage currents post annealing (in the range 10^{-8}-10^{-9} A/cm^2).

The final aspect of this study was to explore the capacitance equivalent thickness (CET) values extracted from the C-V data for the as deposited and post thermal anneal samples. Figure 6 shows the measured CET and extracted *k* values for all the samples. The CET for the Hf:Er 1:1 and the Hf:Er 8:1 samples are generally similar ranging from 1.8nm to 1.9nm for the as-deposited layer and changing only marginally after anneal. The CET for the 4:1 sample is the lowest of all the samples for the as-deposited and annealed samples, it was found to be 1.4nm and 1.5nm respectively. After annealing all samples exhibited an increase in the standard deviation of the CET values measured over a large number of sites across the sample. In light of this fact the 1:1 and the 8:1 samples were subsequently annealed to 550^{o}C and the standard deviation of the CET was again found to increase. The *k* values for each of the samples are also shown in Figure 5; the *k* values were calculated by using the physical thickness of the dielectric which was determined by TEM (See Table 1). The Hf:Er 4:1 samples have highest *k* values (24-26) than either their 1:1(18-21) or 8:1(18-22) counterparts. The *k* value for the Hf:Er 4:1 sample is however lower than that reported by Wiemer et al. [10] although it should be noted a much lower annealing temperature has been used in the present study. The higher annealing temperature (900^{o}C) used by Weimer et al. may influence the *k* value but would clearly not be suitable for some MIM capacitor applications due to the low melting temperature of the Al. This difference in $HfErO_x$ *k*-values could also be attributed to the different substrates which may be influencing the crystallinity and hence the *k* value of the films. The films investigated in this paper were deposited on TiN as opposed to SiO_2 for the films in ref 10.

Conclusion

We have demonstrated the formation of $HfErO_x$ films by ALD for MIM capacitor DRAM applications. We have demonstrated that the incorporation of Er into HfO_2 can lead to an increase in the *k* value of the oxide. The XRD data shows that Er tends to inhibit formation of the monoclinic HfO_2 phase which is likely to result in higher *k* value. The Hf:Er 4:1 pulse ratio seems to provide the optimal Er content for cubic/tetragonal phase stabilisation without increase in pure Er_2O_3 influence. In addition, the Hf:Er 4:1 pulse ratio films exhibit current leakage values of ~$1x10^{-8}A/cm^2$ at V=1V and has a CET of ~1.4nm. In addition, both CET and leakage current are maintained after thermal annealing at 500^oC. This low leakage figure, low CET and good thermal stability make $HfErO_x$ a promising material for MIM capacitors in future DRAM applications.

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Table 1

Hf:Er Pulse Ratio	Condition	Grain Size (nm)	Thickness (nm) (+/-0.5nm)
1:1	As Deposited	5-7	9
4:1	As Deposited	5-10	9
	500ºC Anneal	20	8.5
8:1	As Deposited	6-15	9
	500ºC Anneal	15-25	9.5

Table 1 Grain size and layer thickness measurements of the as-deposited and annealed HfErOx films formed with different pulse ratios

Figures

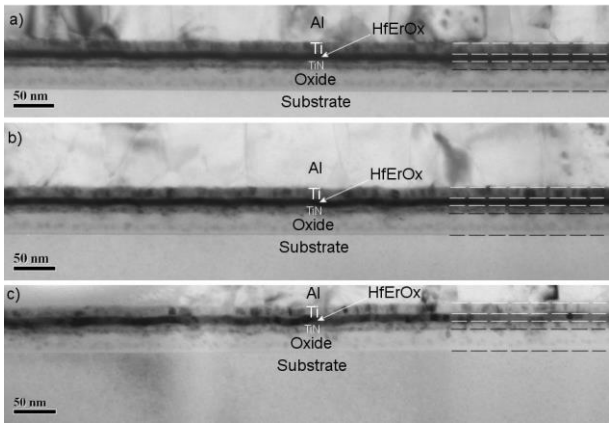


Fig. 1 Bright field TEM micrograph of the as-deposited structures with Hf:Er pulse ratios of a) 1:1 b) 4:1 and c) 8:1.

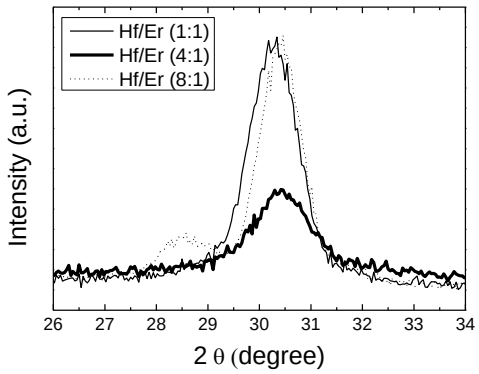


Fig. 2 XRD Data for the as deposited samples with different Hf:Er pulse ratios.

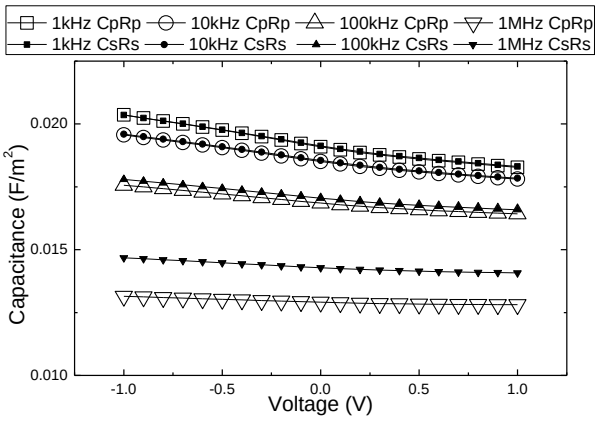


Fig. 3 C-V response for a $1x10^4$ μm^2 $HfErO_x$ (8:1) device following an RTA at 500°C. The frequency of these measurements was varied from 1kHz to 1MHz. The C-V was measured in the parallel and series modes and shows identical characteristics at low frequency.

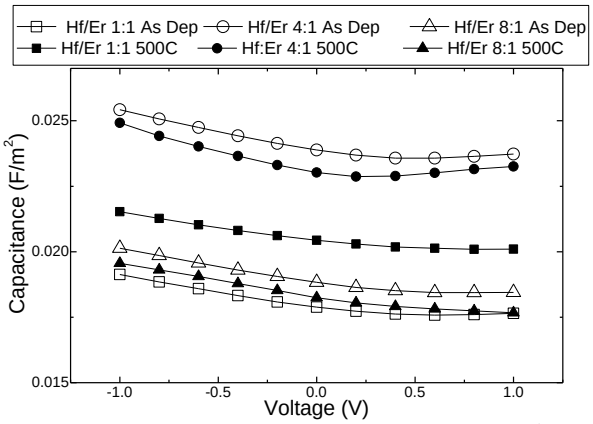


Fig. 4 C-V response measured on a $1x10^4$ μm^2 device at 1kHz, with various Hf:Er pulse ratios, as deposited and after an RTA of 500^{o}C. The highest capacitance density is achieved with the 4:1 Hf:Er pulse ratio.

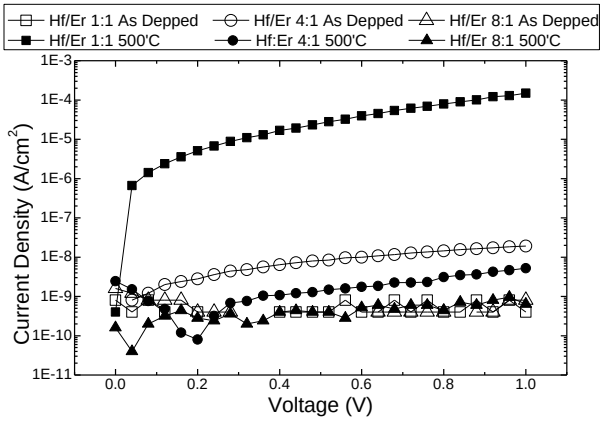


Fig. 5 Current Density (J-V) plots for a $2.5x10^3$ μm^2 device of various Hf:Er pulse ratios, as deposited and with an RTA of 500ºC.

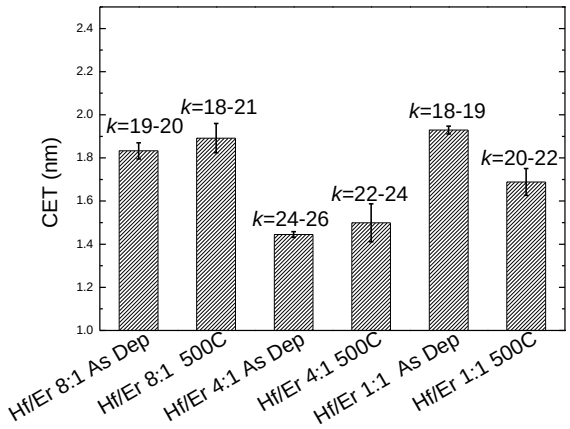


Fig. 6 CET and *k* values extracted from C-V responses at 1 kHz and at V = 0 on a 1 x 10^4 um^2 device.