University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

PUSHING THE LIMITS OF kT/C NOISE IN DELTA-SIGMA MODULATORS

Spyridon Kalogiros[1], Gerardo Salgado[1], Colin Lyden[2], Kevin McCarthy[3], and Ivan O'Connell[2]
[1]Microelectronic Circuits Centre Ireland, Tyndall National Institute, Cork, Ireland
[2]Analog Devices International, Cork, Ireland
[3]University College Cork, Department of Electrical and Electronic Engineering, Cork, Ireland
email: spyridon.kalogiros@umail.ucc.ie

Abstract

Thermal noise, which is sampled and aliases in-band in discrete-time systems, limits the achievable performance of switched-capacitor noise-shaping Analogue-to-Digital Converters (ADCs). While the performance of such ADCs has advanced significantly over the last 20 years, as quantified by the Schreier Figure-of-Merit (FoM_S), the theoretical limit of 192 dB remains unchallenged. Over that period, the envelope of ADC performance has advanced from a FoM_S of 163 dB 20 years ago, to 186 dB today, with a rate of advancement, corresponding to ADC performance, which is doubling every 1.6 years. However, this rate of advancement has started to slow in recent years. This work will review some of the recent advancements in relation to reducing the thermal noise in switched-capacitor Delta-Sigma Modulators. In addition, this chapter will address many of the challenges associated with breaking the 192 dB FoM_S performance barrier.

1. Introduction to kT/C noise

Sampled thermal noise plays a crucial role in the performance of switched-capacitor ADCs, significantly degrading their Signal-to-Noise Ratio (SNR) performance, and it has been a field of research study for decades. To study its origins, the fundamental sampling circuit has to be considered, which consists of a MOSFET device biased in the deep triode region operating as a switch, and thus, it can be replaced by an equivalent resistor, R_{on}, driving a sampling capacitor, C, in series:

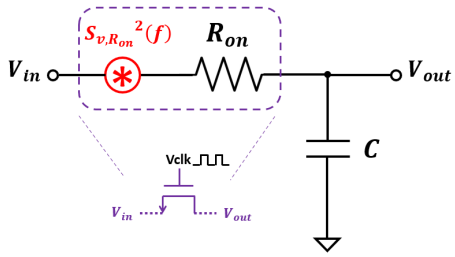

Figure 1 *Sampling equivalent circuit to study sampled thermal noise*

Illustrated in Figure 1, $S_{v,Ron}$ is the power spectral density of the equivalent resistance's thermal noise source. Noise that arises from the random motion of carriers within a conductor is typically called thermal noise due to its temperature dependence. Its spectral power density is given by:

$$S_{v,R_{on}}{}^2(f) = 4kTR_{on}\,, \tag{1}$$

where k is Boltzmann constant (1.380649×10^{-23} m^2 kg s^{-2} K^{-1}); T is the absolute temperature, in Kelvin; and R_{on} is the equivalent on-resistance of the MOS device. In order to calculate the total mean squared noise voltage, which in switched-capacitor circuits is determined by the sampling capacitor, Parseval's theorem could be used [1]. The total mean squared noise voltage is the product of $S_{v,Ron}$ and the equivalent noise bandwidth (ENBW) of the circuit, and is given by:

$$\overline{v_n{}^2} = S_{v,R_{on}}{}^2(f) * ENBW\,, \tag{2}$$

where:

$$ENBW = \int_0^\infty \left|\frac{1}{1+j2\pi fR_{on}C}\right|^2 df\,. \tag{3}$$

For a single pole system, equation (3) becomes as follows [1]:

$$ENBW = \frac{1}{4R_{on}C}\cdot \tag{4}$$

Substituting Equation (4) into (2) results in:

$$\overline{v_n{}^2} = 4kTR_{on} * \frac{1}{4R_{on}C}\cdot \tag{5}$$

The resulting noise voltage from (5) is the following:

$$\sqrt{\overline{v_n{}^2}} = \sqrt{\frac{kT}{C}}\,. \tag{6}$$

The existence of kT/C noise fundamentally limits the SNR performance of a switched-capacitor circuit. This limitation can be evident in the SNR equation below, considering the signal power of a sinusoidal-type input signal, with amplitude V (in Volts), and the power of *kT/C* noise [2]:

$$\mathrm{SNR} = \frac{\mathrm{V}^2/2}{\mathrm{kT/C}}. \tag{7}$$

By introducing values to the capacitor logarithmically from 10 fF to 10 pF, the resulting kT/C noise voltages can be calculated, as shown in Table 1 below.

Capacitor	$\sqrt{\mathbf{kT/C}}$ Noise
10 fF	640 μV
100 fF	200 μV
1 pF	64 μV
10 pF	20 μV

***Table 1**: kT/C noise voltage values for 10 fF-10pF capacitor sizes*

If an input signal with an amplitude of 1 V is considered, by sweeping the SNR from 20 dB to 140 dB with a step of 20 dB, the capacitor values that are needed to achieve each value of SNR are shown in Table 2 [2] below.

SNR (dB)	C (pF)
20	0.00000083
40	0.000083
60	0.0083
80	0.83
100	83
120	8300
140	830000

***Table 2**: Capacitor values for a given SNR performance*

While it's relatively easy to achieve performances at the range of 60-80 dB, very high capacitor values are required to achieve performances from 100 dB and beyond, which is very difficult to be integrated in silicon.

From (6) it is evident that the resistance R_{on} has been eliminated from the calculation of *kT/C* noise voltage value, but when its Power Spectral Density (PSD) is plotted in the frequency domain, R_{on} impacts both the bandwidth and the magnitude. A lower resistance increases the bandwidth (BW) and decreases the maximum noise voltage. The total integrated noise in any case remains the same. This is visualized in Figure 2.

Thermal noise when sampled in switched-capacitor circuits folds back and aliases from higher to lower frequencies, increasing the resultant in-band noise. This

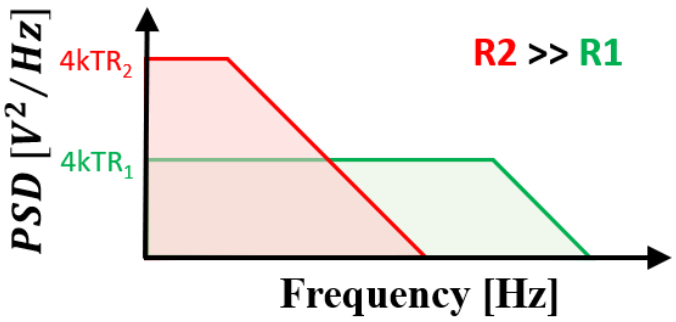

Figure 2 *Power spectral density of kT/C noise vs R_{on} resistance*

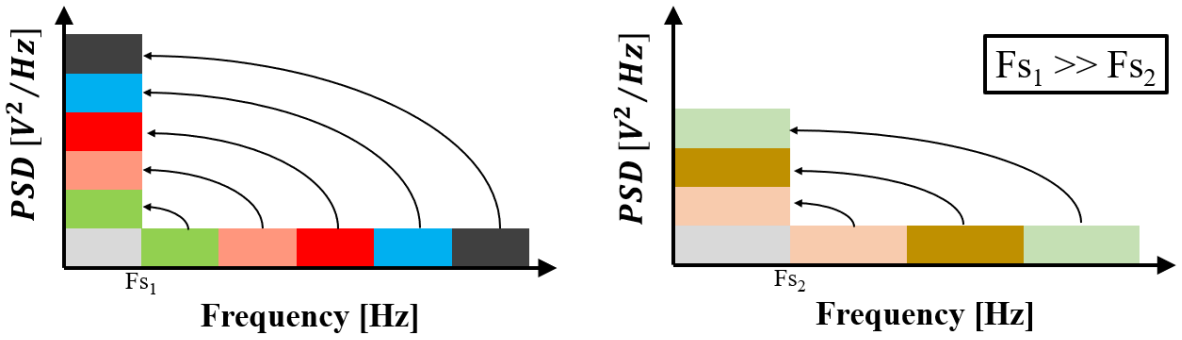

Figure 3 *In-band aliasing of thermal noise due to sampling*

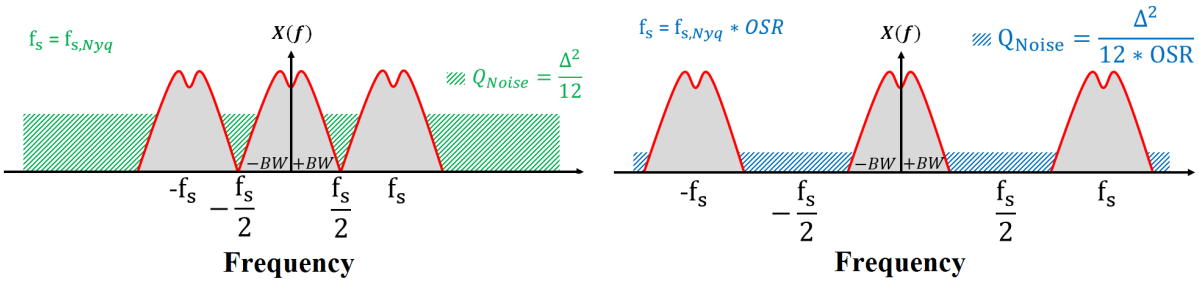

Figure 4 *(a) Noise floor in Nyquist-rate sampling (b) Noise floor with oversampling with an oversampling ratio of OSR*

amount depends on the existing total integrated noise, which is set primarily by the capacitor size. As the sampling frequency becomes smaller, more in-band noise is generated. Figure 3 visualizes the noise aliasing.

The oversampling technique is a key aspect of oversampling ADCs, like Delta-Sigma Modulators, to further improve their SNR performance, compared to their Nyquist-rate counterparts. Sampling at rates higher than two times the Nyquist frequency, $f_{s,Nyq}$ (where $f_{s,Nyq}$=2*BW), moves the signal aliases higher in frequency and significantly reduces the overall quantisation noise (Q_{Noise}) floor [2]. Figure 4 illustrates the case of noise reduction with oversampling. On this figure, parameter Δ stands for the total number of quantisation steps.

2. Introduction to the FoMs and current State-of-the-Art trends

Delta-Sigma Modulators are characterized as noise-limited systems. Their performance is broadly benchmarked (in dB) by the Schreier Figure-of-Merit (FoM_S), which is the most appropriate Figure-of-Merit to be taken into account in the case of benchmarking noise-limited ADCs. Firstly, it includes a noise quantity in its calculation, and secondly, it captures most accurately the quadruplication of the consumed power per added bit [3]. The mathematical expression of FoM_S is given by [3]:

$$\mathrm{FoM_s(dB)} = \mathrm{SNDR(dB)} + 10\log\left(\frac{\mathrm{BW}}{\mathrm{P}}\right), \tag{8}$$

where SNDR is the Signal-to-Noise and Distortion Ratio, BW is the bandwidth of the input signal (in Hz) and P the total power consumption (in W). The FoM_S can be visualized in the energy per conversion vs SNDR plot of the State-of-the-Art, in Figure 5 [4]. The red line on the plot indicates the FoM_S frontier and is associated with an increase by four of the power per added bit in noise-limited converters, whereas the green dashed line illustrates the frontier for technology-limited converters, benchmarked using the Walden FoM (FoM_W), [3] and associated with a doubling of the power per added bit.

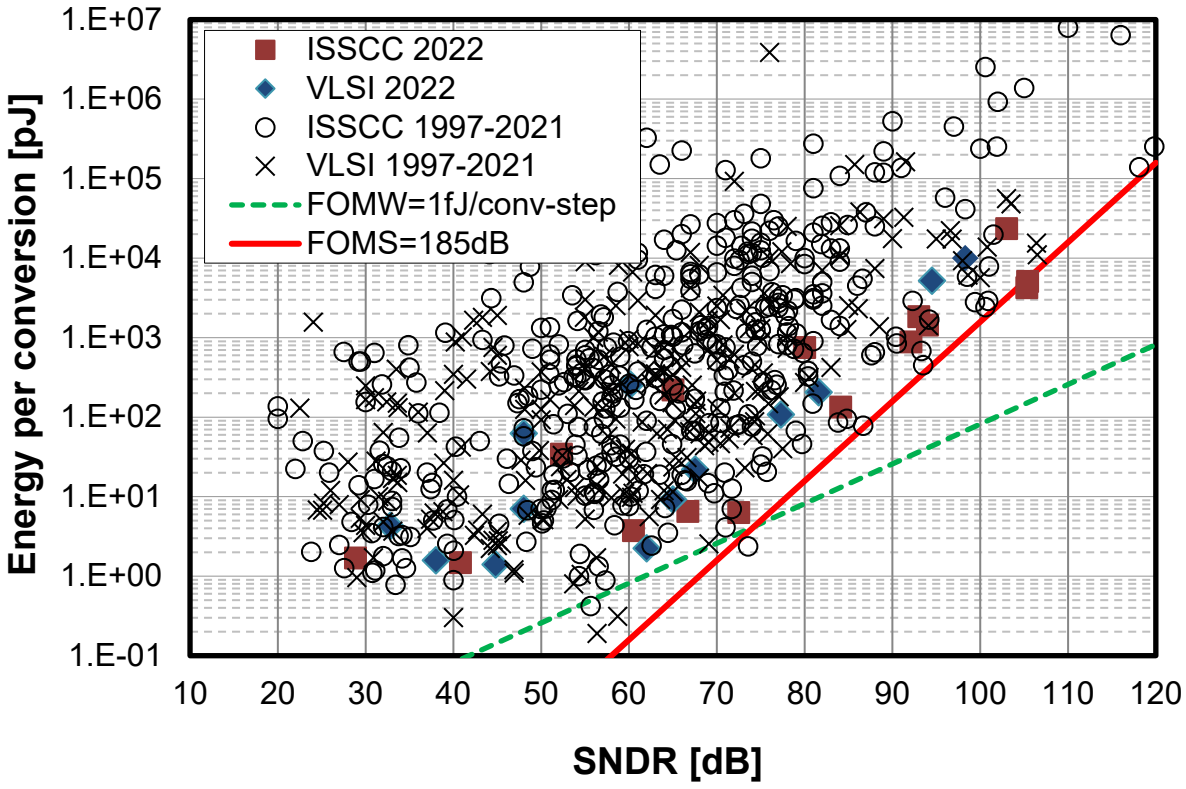

Figure 5 *Energy per conversion vs SNDR State-of-the-Art plot [4]*

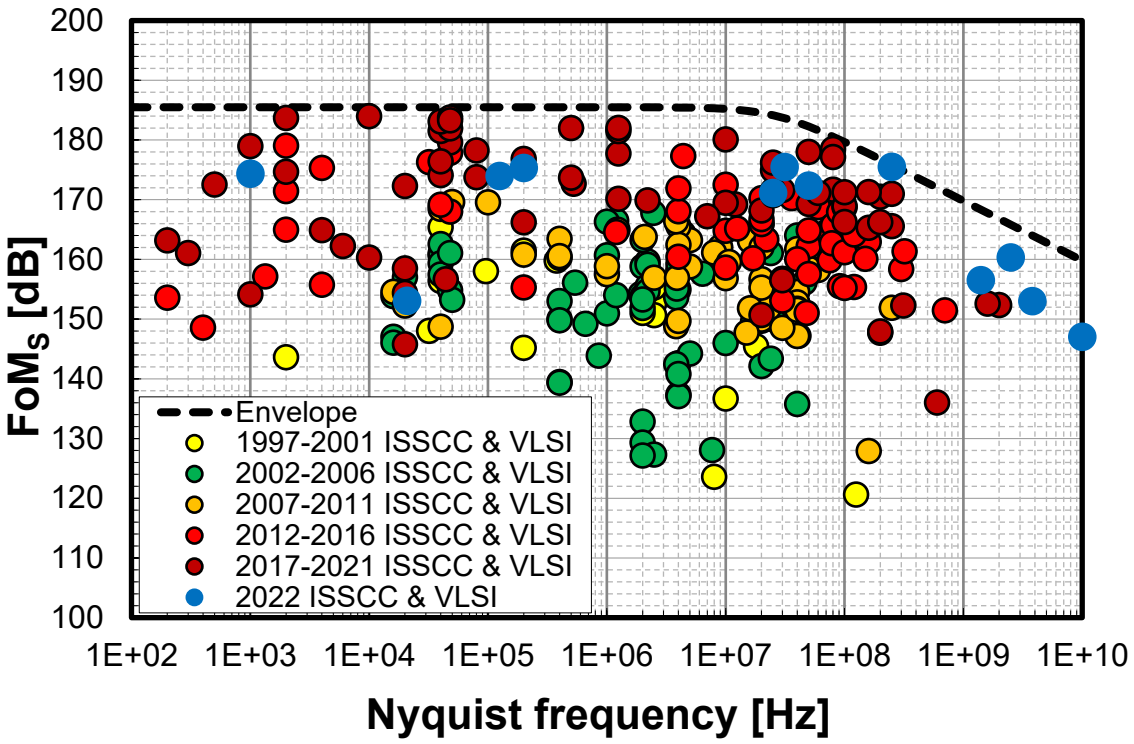

Figure 6 *FoM$_S$ vs Nyquist frequency State-of-the-Art plot [4]*

Another representation of the FoM$_S$ is shown in Figure 6, where the FoM$_S$ for the State-of-the-Art is plotted versus the Nyquist frequency, categorized in groups of 5 years advancement, apart from those of 2022 [4].

The rate of improvement indicates that there is an advancement of 1 dB in the FoM$_S$ per year [3, 5, 6]. However, there is a fundamental limitation for this advancement, which is going to be analyzed in the next section of this work [3, 5].

3. The 192 dB FoMS boundary

Alongside with the expression in (8), *kT/C* noise from (6) leads to the derivation of a FoM$_S$ boundary for ADCs. The first quantity to derive this is the energy per conversion, E_{conv}, shown also in the Y axis of Figure 5, which is given by:

$$E_{conv} = {}^{P}/_{f_{s,Nyq}}, \tag{9}$$

where P is the dissipated power (in W), and $f_{s,Nyq}$ the Nyquist frequency (in Hz). The minimum power for circuits that are capable to handle rail-to-rail signal voltages, which is also linked to the *kT/C* noise presence, is given by [8]:

$$P_{min} = 8kT * f_{s,Nyq} * SNR\,. \tag{10}$$

Combining the equations (9) and (10), the minimum energy it takes to drive a sampling capacitor is obtained as follows [3, 7-10]:

$$E_{conv,min} = 8kT * SNR\,. \tag{11}$$

Based on the Nyquist frequency, $f_{s,Nyq}$, which is equal to 2*BW, the FoM_S from (8) can be rewritten as:

$$FoM_s(dB) = SNDR(dB) + 10\log\left(\frac{f_{s,Nyq}}{2P}\right). \tag{12}$$

By assuming an ideal situation where SNDR = SNR with no distortion [3], expression (12) can be rewritten using (9) as:

$$FoM_s(dB) = SNR(dB) + 10\log\left(\frac{1}{2E_{conv,min}}\right). \tag{13}$$

By substituting the minimum energy from (11) to (13), the FoM_S now becomes:

$$FoM_s = SNR(dB) + 10\log\frac{1}{16kT*SNR}. \tag{14}$$

By applying logarithmic rules, (14) can be rewritten as:

$$FoM_s = SNR(dB) + 10\log 1 - 10\log(16kT) - 10\log(SNR), \tag{15}$$

which can be further simplified to:

$$FoM_s = -10\log(16kT)\,, \tag{16}$$

or, equivalently, 192 dB in approximation, at room temperature (T = 300° K). A more realistic approach to this boundary could be a number between 186 and 188 dB, since the 192 dB limitation considers only sampling energy [3] and ideal circuits. The 192 dB limitation can be shown on the State-of-the-Art FoM_S of Figure 7 [4].

4. kT/C noise cancellation: Previous work

A lot of research has been conducted in order to reduce *kT/C* noise in switched-capacitor circuits. The work in [1] proposes a sampling circuit for image sensors

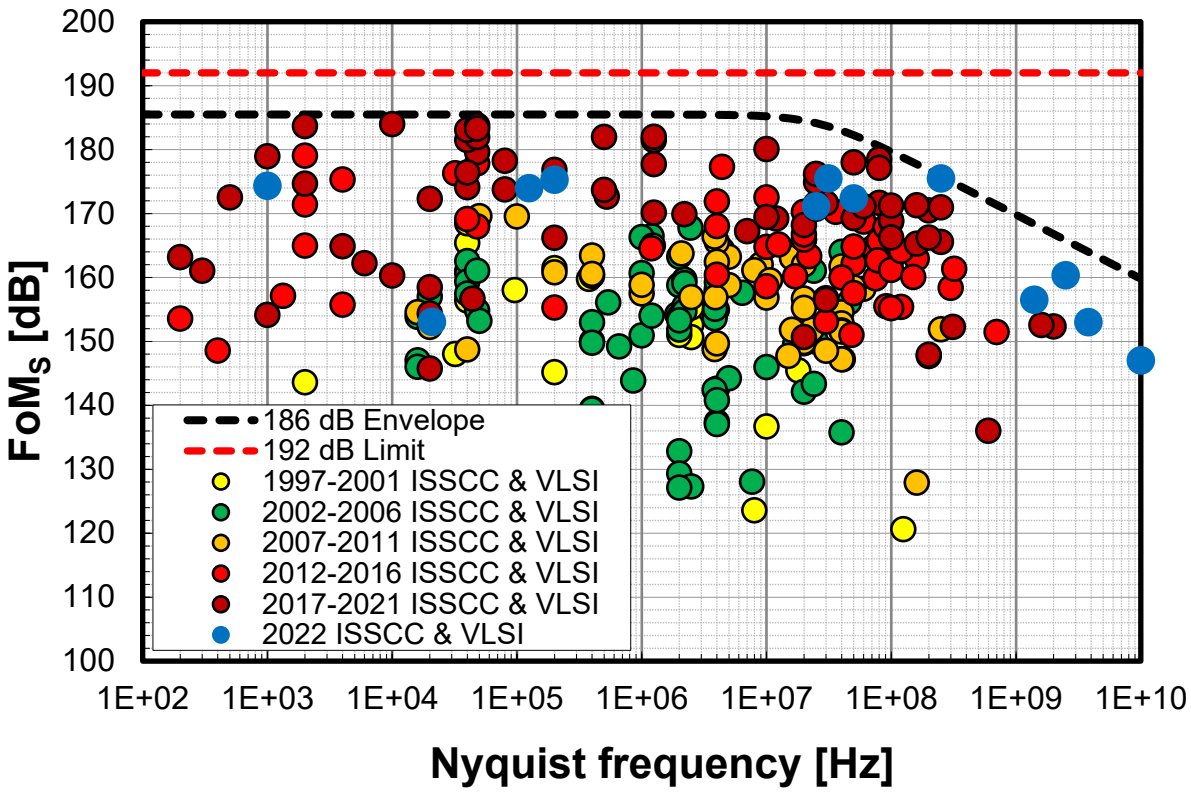

Figure 7 *FoM$_S$ vs Nyquist frequency State-of-the-Art plot with the 192 dB FoM$_S$ limit [4]*

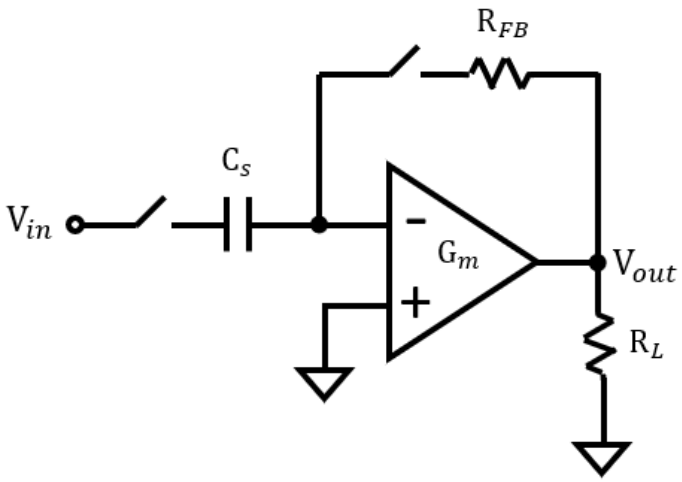

Figure 8 *Circuit from [1] for the reduction of sampled thermal noise*

that breaks the relationship between the dominant noise source and the impedance which limits the noise bandwidth, in order to reduce sampled thermal noise. This circuit is illustrated in Figure 8.

The feedback configuration with a transconductance amplifier, G_m, and a relatively high resistor, R_{FB}, performs the noise reduction by decoupling thermal noise density and bandwidth. Resistors R_{FB} and R_L, alongside with the

transconductance amplifier, form a new system with an effective transconductance $G_{m,eff}$, which is the G_m of the amplifier multiplied with the resistive divider formed by the two resistors. Eventually, the total sampled *kT/C* noise is attenuated by $1/(G_{m,\,eff}*R_{FB})$. However, the need for active elements in order to beat *kT/C* noise substantially increases the power consumption and the FoM_S is not improved.

Another useful circuit for the purpose of beating *kT/C* noise in Successive Approximation Register (SAR) ADCs is proposed in [11]. In conventional SAR ADCs, the sampled *kT/C* noise is directly added on the input signal, significantly degrading the SNR performance. The work in [11] proposes the addition of a capacitor C_2 and a switch controlled by phase φ_2, placed after the pre-amplifier. Figure 9 illustrates this idea.

This added circuitry, alongside with the clocking scheme of phases φ_1 and φ_2, practically cancels the *kT/C* noise imposed by capacitor C_1 and introduces *kT/C* noise only from capacitor C_2, which is attenuated by the gain of the pre-amplifier, since the capacitor is placed after this block.

However, the additional pre-amplifier here has to drive a large capacitive load and a large capacitor C_2, as it has to fully settle for each bit conversion. This configuration significantly reduces sampled thermal noise, but due to increased power consumption the FoM_S is not advanced.

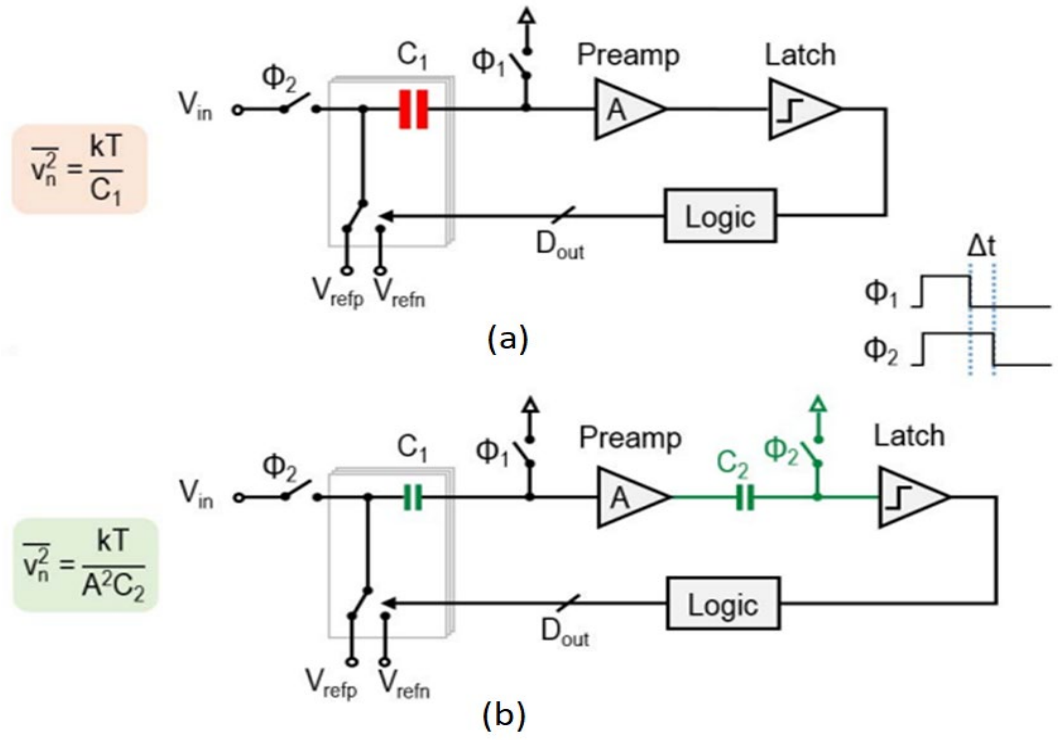

Figure 9 *(a) Conventional SAR ADC with bottom-plate sampling and comparator pre-amplifier (b) SAR ADC with kT/C noise cancellation [11]*

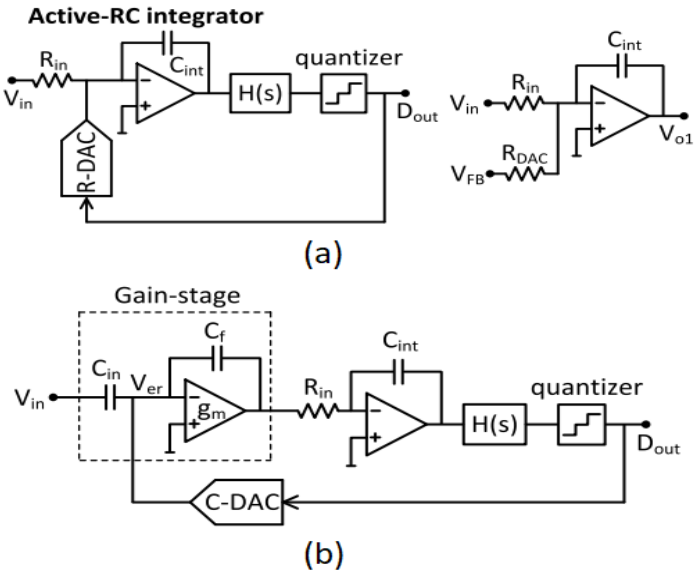

Figure 10 *(a) CTDSM with RC integrator front-end (b) CTDSM with Capacitive-Gain Amplifier (CGA) front-end [12]*

An interesting approach on cancelling *kT/C* noise has been introduced in [12] and is depicted in Figure 10. Traditionally, in Continuous-Time Delta-Sigma Modulators (CTDSMs), the power required to drive the input and the Digital-to-Analogue Converter (DAC) is larger than the power of the first integrator's operational amplifier (opamp). Consequently, a large amount of power is burnt at the resistance R_{in} of the first integrator, as shown in Figure 10(a). The loading of the first integrator should be reduced, and the transconductance that sets the noise density should be different than the one that sets the signal's bandwidth.

To alleviate the above issues, a Capacitive-Gain Amplifier (CGA) stage, with an input capacitor, C_{in}, and a feedback capacitor, C_f, is added before the first integrator of the CTDSM, as shown in Figure 10(b). With the existence of this, the "power x noise" tradeoff is significantly reduced by a factor of 18.1, from 29.5kT to 1.62kT. Due to the absence of *kT/C* noise from the input, the capacitors of that stage can be made small, and the power consumption is therefore dominated by the opamp used for the CGA stage. The closed-loop gain of the CGA block is given by C_{in}/C_f, and it is selected to a value that ensures a proper error signal (V_{in}-V_{DAC}) swing for the rest of the blocks in the loop-filter of the modulator.

The CGA block dramatically changes the noise performance of such a modulator, and it can be adapted to modulators which consist of switched-capacitor filters also. To operate properly, the feedback signal has to precisely track the input signal, and that enables larger gains to be applied with better noise performances. It not only improves the *kT/C* noise performance but advances the FoM_S. In the following section the operation of this block and its benefits will be discussed.

5. Delta-Sigma Modulators: General Overview

Before introducing the CGA stage and analyzing its benefits, this section revises the basics of Delta-Sigma Modulators. Such a system is considered as a closed-loop system like the one in Figure 11. It contains the input X(s), a loop-filter with a number of integrators according to its order which has a transfer function H(s), the output signal W(s), and the additive quantisation noise source Q(s) to approximate the behavior of a quantiser. Finally, the output signal Y(s), which is fed back to the system is subtracted from the input signal providing to the loop-filter a quantisation error signal as an input. By applying basic algebra rules, the output Y(s) is given by [13-15]:

$$Y(s) = W(s) + Q(s). \tag{17}$$

Moreover, the output of the loop-filter, W(s), can be further derived as:

$$W(s) = H(s) * \big(X(s) - Y(s)\big). \tag{18}$$

By substituting W(s) from (18) into (17), the output Y(s) becomes:

$$Y(s) = H(s) * \big(X(s) - Y(s)\big) + Q(s). \tag{19}$$

This equation can be further derived as follows:

$$Y(s) = \frac{H(s)}{1+H(s)} X(s) + \frac{1}{1+H(s)} Q(s). \tag{20}$$

Equation (20) contains two main quantities, the Signal Transfer Function (STF), multiplied by the input X(s), and the Noise Transfer Function (NTF), multiplied by the quantisation noise Q(s), the two main transfer functions of a Delta-Sigma Modulator loop. The former has a low-pass characteristic for the input signal, and the latter a high-pass characteristic for the quantisation noise, introducing the noise-shaping feature of the modulator. If an integrator is used, with a transfer function of H(s) = 1/s, the STF becomes equal to 1/(s+1) and the NTF becomes equal to s/(s+1) [13-15].

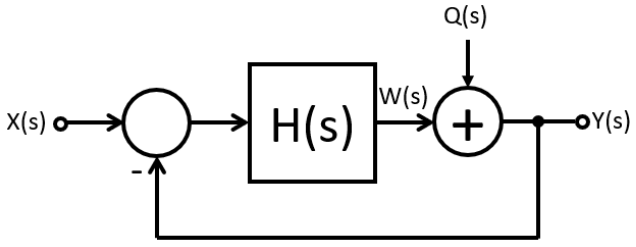

Figure 11 *s-domain model of a Delta-Sigma Modulator*

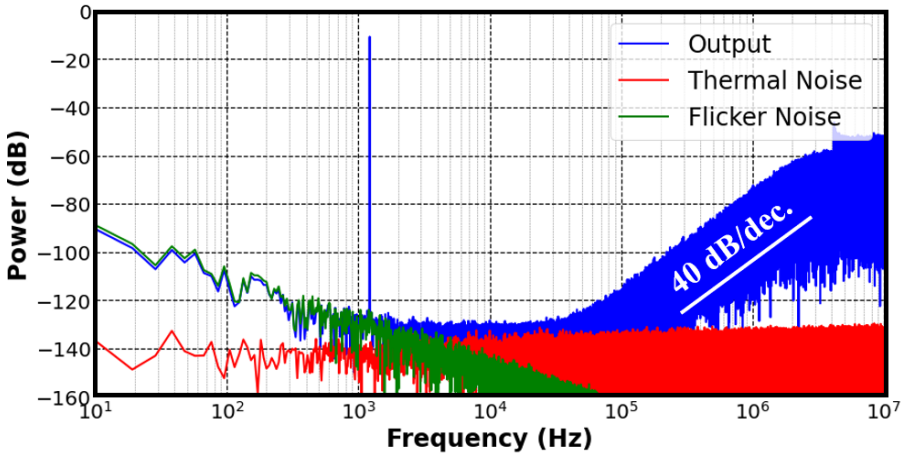

Figure 12 *PSDs of output signal, flicker and thermal noise of the second-order Delta-Sigma Modulator in [16]*

The noise-shaping feature can be observed when looking at the output of the modulator, Y(s), in the frequency domain. The work in [16] presents the output spectrum of a synthesized single-bit second-order Delta-Sigma Modulator, with the existence of flicker and thermal noise. Here, the two types of noise form a noise corner. This introduces a roll-off characteristic to the output spectrum at low frequencies due to the flicker noise, and a noise floor characteristic at mid-range frequencies due to the thermal noise (Figure 12). At higher frequencies, the noise-shaping takes place, depending on the order of the modulator. A first-order modulator introduces 20 dB/dec. noise-shaping. Then, for every increase by one in the order of the modulator, the noise shaping increases by 20 dB/dec. [13-16].

6. Introducing CGA Stage to Delta-Sigma Modulators

In a generic Delta-Sigma modulator, like the one in Figure 13(a), the dominant noise sources, seen as input-referred, are the in-band thermal noise voltage from the DAC and the in-band thermal noise voltage from the first integrator of the loop-filter. The input thermal noise, thus, can be derived as follows:

$$V_{th,in} = \sqrt{V^2_{th,\ DAC,\ In-Band} + V^2_{th,\ Int1,\ In-Band}}\ . \tag{21}$$

The input-referred noise voltages from the subsequent integrators of the loop-filter are divided by the product of gains of the preceding integrators, and thus, are significantly attenuated. The in-band noise voltage of the first integrator, in the case of a switched-capacitor circuitry implementation, is the following:

$$V_{th,\ Int1,\ In-Band} = \sqrt{\frac{kT}{C_{in,Int1} * OSR}}, \tag{22}$$

where $C_{in,Int1}$ the integrator's input capacitance and OSR the oversampling ratio.

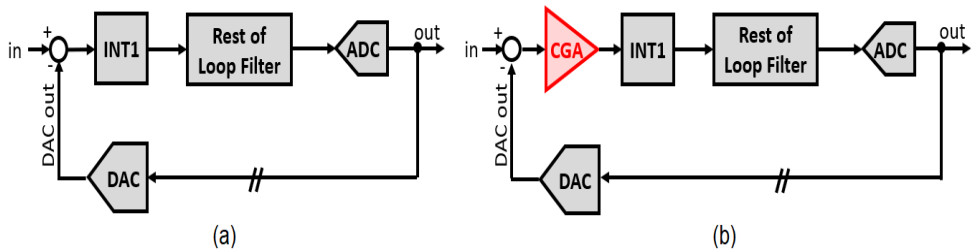

Figure 13 *(a) Delta-Sigma Modulator with no CGA (b) Delta-Sigma Modulator with CGA to provide gain and attenuate the input referred noise of the subsequent circuits.*

By applying a gain stage upfront, before the first integrator and directly after the formation of the quantisation error signal, as shown in Figure 13(b), the dominant noise sources change [12]. Thermal noise voltage from the CGA block becomes now the dominant noise source. However, the noise of the first integrator, as seen input-referred, is attenuated by a factor equal to the gain of the added CGA block. The input-referred noise voltage in this case can be derived as follows:

$$V_{th,in} = \sqrt{\mathbf{V^2_{th,\ CGA,\ In-Band}} + V^2_{th,\ DAC,\ In-Band} + \left(\frac{1}{\mathbf{G_{CGA}}} * V_{th,\ Int1,\ In-Band}\right)^2}\ . \quad (23)$$

The addition of this gain stage up-front plays a critical role for the SNR and FoM_S improvement. That will be analytically explained in the following sections.

7. Theoretical analysis of the CGA Stage

A CGA stage, like the one proposed in [12], is depicted in Figure 14(a). A second branch for a DAC input has been added to illustrate the feedback signal's input, and also a parasitic capacitor, C_{par}, related to parasitics such as metal in real silicon implementations. Also, a resistance R_B is added which sets the bias voltage of the opamp. The ideal transfer function of this block is given by the following [12]:

$$V_{out} = -\left(V_{in}\frac{C_{in}}{C_f} + V_{dac}\frac{C_{dac}}{C_f}\right). \quad (24)$$

However, a more realistic form can be derived, considering non-idealities like the finite DC gain and the dominant pole of the opamp. The opamp can be modelized as a single-pole system with a transfer function, A(s), given by [17-18]:

$$A(s) = \frac{A_0}{1+{}^{s}/_{\omega_0}}\ , \quad (25)$$

where A_0 is the DC gain of the opamp and ω_0 its dominant pole, in radian frequency.

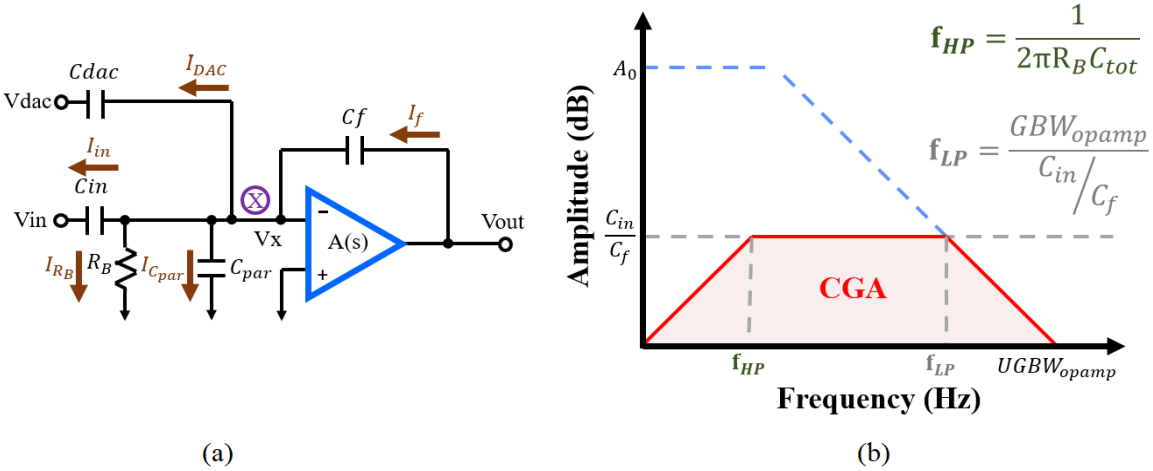

Figure 14 *(a) CGA block (b) Associated transfer function characteristic*

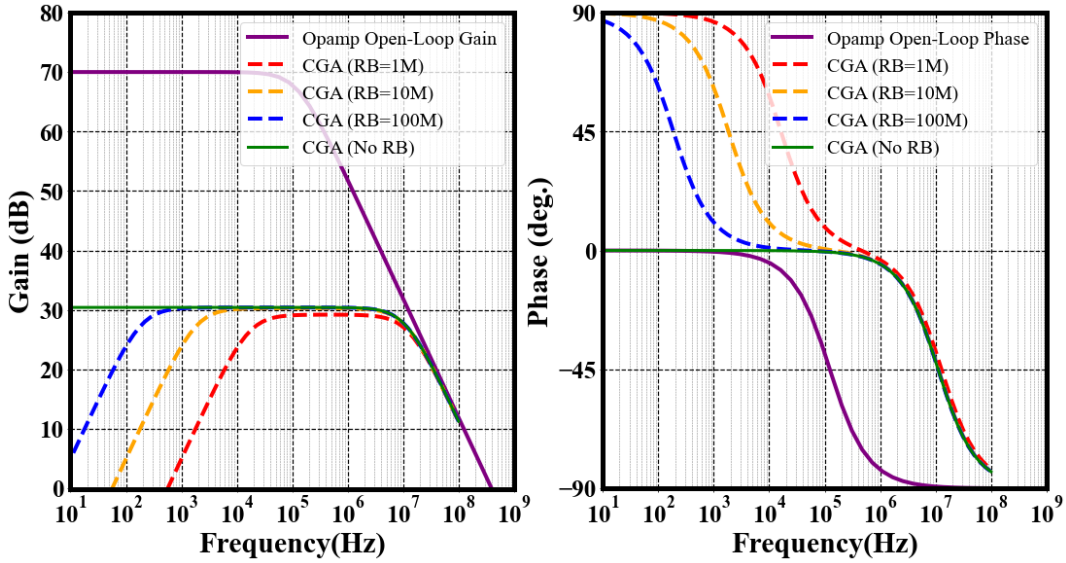

Figure 15 *Behavioral simulation of CGA transfer function with varying R_B (a) CGA gain bode plot (b) CGA phase bode plot*

By applying Kirchhoff's Current Law (KCL) at node X of Figure 14(a), the current, I_f, is equal to the sum of currents I_{in}, I_{DAC}, I_{RB} and I_{Cpar} (or equivalently $I_f = I_{in} + I_{DAC} + I_{RB} + I_{Cpar}$), thus:

$$[V_{out}(s) - V_X]sC_f = [V_X - V_{in}(s)]sC_{in} + [V_X - V_{DAC}(s)]sC_{DAC} + \frac{V_X}{R_B} + V_x sC_{par}. \quad (26)$$

The output voltage, V_{out}, can be further derived as V_X*A(S), and thus, the voltage at node X is given by:

$$V_X = \frac{V_{out}(s)}{A(s)} = \frac{V_{out}(s)}{\frac{A_0}{1+s/\omega_0}}. \quad (27)$$

By using equation (27) to replace V_X, equation (26) now becomes:

$$\left[V_{out}(s)-\frac{V_{out}(s)}{\frac{A_0}{1+s/\omega_0}}\right]sC_f=\left[\frac{V_{out}(s)}{\frac{A_0}{1+s/\omega_0}}-V_{in}(s)\right]sC_{in}+\left[\frac{V_{out}(s)}{\frac{A_0}{1+s/\omega_0}}-V_{DAC}(s)\right]sC_{DAC}+\frac{\frac{V_{out}(s)}{\frac{A_0}{1+s/\omega_0}}}{R_B}+\frac{V_{out}(s)}{\frac{A_0}{1+s/\omega_0}}sC_{par}. \quad (28)$$

By further rearranging equation (28) in order to derive the transfer function, $V_{out}(s)/V_{in}(s)$, it becomes as follows:

$$V_{out}(s)=-\frac{sA_0V_{dac}C_{dac}+sA_0V_{in}C_{in}}{s^2\left(\frac{C_f}{\omega_0}+\frac{C_{dac}}{\omega_0}+\frac{C_{in}}{\omega_0}+\frac{C_{par}}{\omega_0}\right)+s\left(A_0C_f+C_f+C_{dac}+C_{in}+C_{par}+\frac{1}{\omega_0R_B}\right)+\frac{1}{R_B}}. \quad (29)$$

The transfer function characteristic of (29) is shown in Figure 14(b) and has three main spectral areas of interest. Initially, it has a 20 dB/dec. high-pass characteristic due to the formation of a high-pass filter from the existence of C_{in} and R_B. A high-pass filter pole is therefore formed at f_{HP}, and the response thereafter becomes flat. At higher frequencies, the opamp with a DC-gain of A_0 rolls-off the CGA gain until its Unity-Gain Bandwidth (UGBW) frequency. At f_{LP}, the point where the opamp response crosses the CGA's characteristic, another CGA pole f_{LP} (low-pass) can be calculated and it is shown on Figure 14(b).

A slight modification of the CGA block can be also implemented without the existence of the resistor R_B, since there are circuitry mechanisms that can provide a stable bias voltage for the opamp, like the case of a switched-capacitor DAC. In this case, the transfer function of (29) can be further simplified as:

$$V_{out}=-\frac{A_0V_{dac}C_{dac}+A_0V_{in}C_{in}}{s\left(\frac{C_f}{\omega_0}+\frac{C_{dac}}{\omega_0}+\frac{C_{in}}{\omega_0}+\frac{C_{par}}{\omega_0}\right)+\left(A_0C_f+C_f+C_{dac}+C_{in}+C_{par}\right)}. \quad (30)$$

The poles f_{HP} and f_{LP} of the CGA transfer function characteristic in Figure 14(b) can be precisely calculated by solving the second-order equation of the denominator in equation (29). By applying basic algebra in order to find the roots of this equation, they are extracted as follows:

$$f_{HP}=\left|\frac{-A_0C_f\omega_0-C_{tot}\omega_0-\frac{1}{R_B}+\omega_0\sqrt{A_0{}^2C_f{}^2+C_{tot}{}^2+\frac{1}{\omega_0{}^2R_B{}^2}+2A_0C_fC_{tot}+\frac{2A_0C_f-2C_{tot}}{\omega_0R_B}}}{2C_{tot}}\right|, \quad (31)$$

Parameter	Description	Value
f_s	Sampling frequency	6.25 MHz
V_{in}	Input voltage	1 V
V_{DAC}	DAC input voltage	1 V
C_{in}	Input capacitor	500 fF
C_{DAC}	DAC capacitor	60 fF
G_{CGA}	CGA closed-loop gain (C_{in}/C_f)	30
C_f	Feedback capacitor	C_{in}/G_{CGA}
C_{par}	Parasitic capacitor	20 fF
C_{tot}	Total capacitance	$C_{in}+C_{DAC}+C_f+C_{par}$
GBW	CGA opamp gain bandwidth	$10*f_s$
$A_{0,\,min}$	CGA opamp minimum DC-gain	70 dB
$f_{pole,\,Hz}$	CGA opamp dominant pole frequency	$GBW/A_{0,\,min}$
$f_{pole,\,rad}$	CGA opamp dominant pole radial frequency	$2\pi f_{pole,\,Hz}$

Table 3 *Parameter values for the behavioral simulation of CGA transfer function*

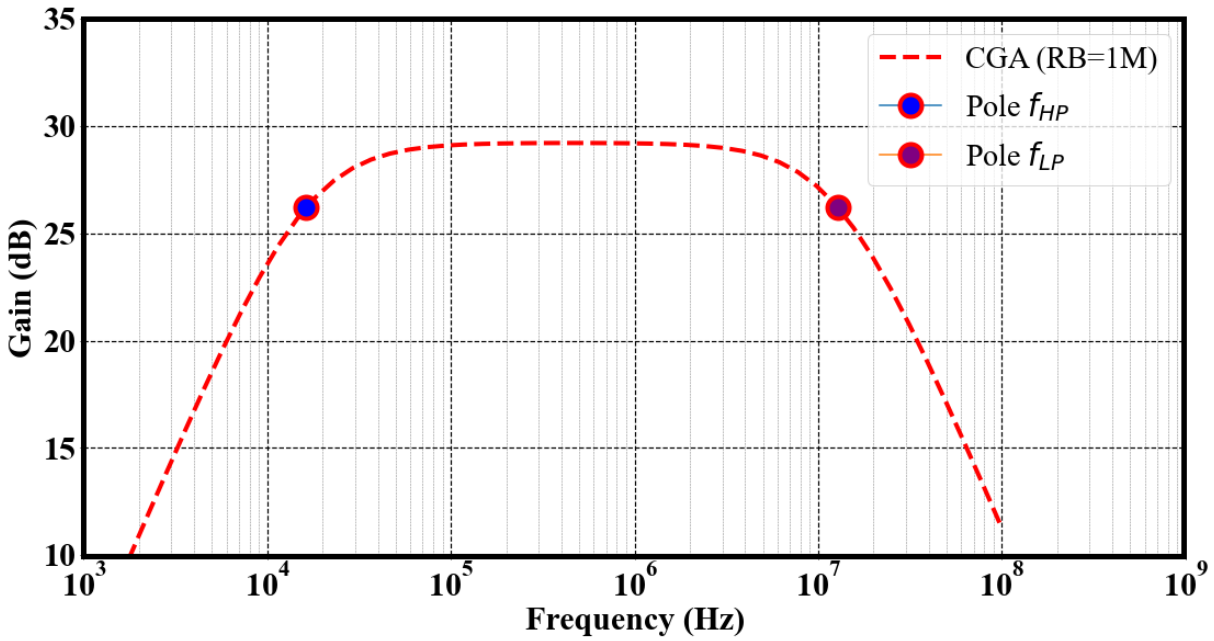

Figure 16 *Verification of CGA f_{HP} and f_{LP} poles*

$$f_{LP} = \left| \frac{-A_0 C_f \omega_0 - C_{tot}\omega_0 - \frac{1}{R_B} - \omega_0 \sqrt{A_0{}^2 C_f{}^2 + C_{tot}{}^2 + \frac{1}{\omega_0{}^2 R_B{}^2} + 2A_0 C_f C_{tot} + \frac{2A_0 C_f - 2C_{tot}}{\omega_0 R_B}}}{2C_{tot}} \right| . \quad (32)$$

Figure 15 shows the behavioral simulation with gain and phase bode plots of the CGA block's transfer function from (29), while the R_B resistance is varied logarithmically, from 1 MΩ to 100 MΩ, which in turn alters the pole f_{HP}. The bigger the resistor R_B, the lower the pole f_{HP} becomes. Also, the case of a zero R_B

is plotted, where there is no pole formed. The opamp bode and phase plots are also shown to illustrate how opamp contributes to the CGA gain roll-off at higher frequencies. Table 3 summarizes the parameter values for the setup of this behavioral simulation.

Figure 16 illustrates the simulated poles f_{HP} and f_{LP}, given the parameters of Table 3, as they are calculated using equations (31) and (32). They appear on the spectrum very precisely, at - 3dB from the maximum closed-loop gain of the CGA characteristic, with $R_B = 1M\Omega$.

8. Impact of the CGA on the SNR performance of Delta-Sigma Modulators

The SNR for a Delta-Sigma Modulator can be generally calculated (in dB) as follows:

$$\mathrm{SNR(dB)} = \mathrm{P_{sig.}(dBFS)} - \mathrm{V_{n,tot}(dB)}\,, \tag{33}$$

where $P_{sig.}$ is the signal power, in dBFS, and $V_{n,tot}$ the total input-referred noise voltage, in dB. The signal power, $P_{sig.}$, can be calculated (in dBFS) as follows:

$$\mathrm{P_{sig.}(dBFS)} = 10\log\left(\frac{\mathrm{A^2}/2}{\mathrm{A^2_{FS}}/2}\right), \tag{34}$$

where A is the amplitude of the input signal (in Volts) and A_{FS} the full-scale amplitude (in Volts).

The total input-referred noise voltage, $V_{n,tot}$, is given by:

$$\mathrm{V_{n,tot}(dB)} = 20\log\left(\sqrt{\mathrm{N_Q}^2 + \mathrm{N_{th}}^2}\right), \tag{35}$$

where N_Q is the total quantisation noise voltage and N_{th} the total input-referred thermal noise voltage. Those are calculated as follows [13-15]:

$$\mathrm{N_{Th}} = \sqrt{\left(\frac{\sqrt{\frac{4\mathrm{kTC_{dac}}}{\mathrm{OSR}}}}{\mathrm{C_{in}}}\right)^2 + \left(\sqrt{\frac{4\mathrm{kT\gamma BW}}{\mathrm{G_{m,CGA}}}}\right)^2 + \frac{1}{\mathrm{G_{CGA}}}\left(\sqrt{\frac{4\mathrm{kT}}{\mathrm{C_{in,Int1}}*\mathrm{OSR}}}\right)^2}, \tag{36}$$

$$\mathrm{N_Q} = \frac{10^{\frac{\mathrm{N_Q(dB)}}{10}}}{\sqrt{\mathrm{BW}}}, \tag{37}$$

Parameter	Description	Value
A	Input signal amplitude	0.7 V
A_{FS}	Full-scale amplitude	1.2 V
BW	Input signal bandwidth	100 kHz
Nfft	Number of total frequency bins	4096016
NBW	Noise bandwidth	1/Nfft
OSR	Oversampling ratio	32
Δ	Quantisation steps	64
L	Modulator order	3
$G_{M,CGA}$	CGA opamp transconductance	10 μS
$C_{in,Int1}$	Integrator 1 input capacitor	500 fF
γ	Transistor technological parameter	2/3

Table 4 *Rest of parameter values for the behavioral simulation of total input-referred noise voltage in a Delta-Sigma Modulator with CGA block*

where:

$$N_Q(\text{dB}) = 10\log10\left(\frac{\text{BW}}{\text{NBW}}\right) + 10\log10\left(\sqrt{\frac{\Delta^2}{12\pi(2L+1)}\left(\frac{\pi}{\text{OSR}}\right)^{2L+1}}\right). \quad (38)$$

Thermal noise voltage from the DAC is the first quantity in the square root of equation (36). It is calculated as the thermal noise charge of the DAC capacitor, divided by the oversampling ratio, OSR, to keep the in-band quantity, and this result is divided by the input capacitor of the CGA, C_{in}, in order to get the equivalent *kT/C* noise voltage, multiplied by the C_{DAC} capacitance, which can provide noise scaling according to its size compared to C_{in}. The second quantity in the square root of (36) is the thermal noise voltage from the opamp [18]. The third quantity is the in-band thermal noise voltage of the first integrator in the loop filter [13-15], divided by the gain of the CGA, as seen in-band.

The effect of CGA block on the overall SNR and FoM_S performance is shown on Figure 17(a). By sweeping the CGA closed-loop gain logarithmically from 1 to 1000, the improvement on the SNR and FoM_S is observed. Further improvement occurs when input signals with larger amplitudes are applied. The best performance improvement occurs when the CGA gain is in the range between 2 and 200. Further increase beyond 200 does not contribute to better SNR and FoM_S performances, as the SNR stabilizes. However, for very high CGA gain numbers beyond 200, a very large C_{in} capacitance is required to provide a reasonable size of C_f, provided that the CGA closed-loop gain is given by C_{in} / C_f. Thus, the difficulty to integrate large capacitances in real silicon implementations sets a limit to the maximum usable CGA gain.

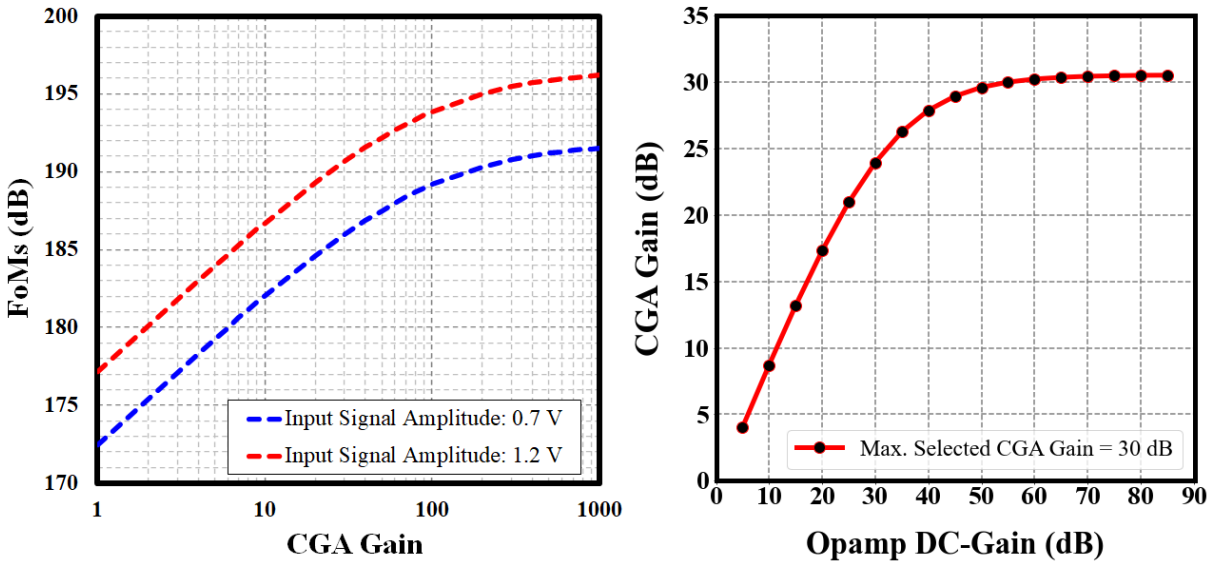

Figure 17 *(a) FoM$_S$ vs CGA gain (b) CGA gain vs opamp DC-gain*

Moreover, by sweeping the DC-gain of the opamp in the CGA, and by keeping the CGA closed-loop gain to 30 dB, the minimum DC-gain of the opamp for which the maximum closed-loop gain is achieved can be found, and in the present behavioral simulation it is 70 dB, as shown in Figure 17(b). This is critical for optimum design purposes. The values of the parameters for the equations (33-38), and with which the results of Figure 17 were extracted, are listed in Table 4, in addition to the parameters which are already shown in Table 3.

Shown in equation (36), the existence of CGA block significantly reduces the thermal noise voltage from the first integrator, seen as input-referred. Thus, the CGA block becomes the dominant thermal noise voltage source. That explains the SNR and FoM$_S$ improvement, observed in Figure 17(a). In order to approach FoM$_S$ performances of 186 dB and higher, a quantisation error amplification by at least 10, according to Fig. 17(a), has to be introduced before the loop-filter. The amplification requirement for a targeted performance gets lower when input signals with higher amplitudes are applied. Due to this amplification process, the DAC feedback signal has to precisely track the input signal, providing in that way a very small quantisation error to the CGA stage.

9. Conclusions

The ongoing demand for power-efficient ADCs is ever more present, driven by rapidly increasing energy costs and the need to minimize self-heating in deep sub-micron nodes. The efficiency of noise-limited ADCs in particular, like Delta-Sigma Modulators, is benchmarked by the FoM$_S$, and its rate of advancement has slowed in the recent years. While the theoretical FoM$_S$ limit of 192 dB will most

likely result in a practical of 186-188 dB, recent publications have begun to approach it and in two cases match these numbers [19, 20]. However, to exceed these numbers, new architectures will be required, whereby the quantisation error signal is amplified prior to sampling. This approach is necessary to reduce the impact that sampling has on wide-band thermal noise sources and can pave the way for future ADCs to achieve FoMs of 190 dB and greater.

References

[1] R. Kapusta, H. Zhu and C. Lyden, "Sampling Circuits That Break the kT/C Thermal Noise Limit," in IEEE Journal of Solid-State Circuits, vol. 49, no. 8, pp. 1694-1701, Aug. 2014.

[2] M. Pelgrom, “Analog-to-Digital Conversion”, Third Edition (Springer International Publishing, 2017).

[3] B. Murmann, "The Race for the Extra Decibel: A Brief Review of Current ADC Performance Trajectories," in IEEE Solid-State Circuits Magazine, vol. 7, no. 3, pp. 58-66, Summer 2015.

[4] Murmann, ADC performance survey 1997–2022[Online]. http://web.stanford.edu/~murmann/adcsurvey.html.

[5] M. Keller, B. Murmann, Y. Manoli, Analog-Digital Interfaces, NANO-CHIPS 2020, Springer, 2010, pp. 93-116.

[6] B. Murmann, M. Verhelst, Y. Manoli, Analog-to-Information Conversion, NANO-CHIPS 2030, Springer, 2020, pp. 275–292.

[7] B. Murmann, “A/D converter trends: Power dissipation, scaling and digitally assisted architectures,” in Proc. IEEE Custom Integrated Circuits Conf., 2008, pp. 105–112.

[8] C. C. Enz and E. A. Vittoz, "CMOS low-power analog circuit design," Emerging Technologies: Designing Low Power Digital Systems, 1996, pp. 81-82.

[9] E. A. Vittoz, "Future of analog in the VLSI environment," IEEE International Symposium on Circuits and Systems, 1990, pp. 1372-1375 vol. 2.

[10] B. J. Hosticka, “Performance comparison of analog and digital circuits,” Proc. IEEE, vol. 73, no. 1, pp. 25–29, 1985.

[11] J. Liu, X. Tang, W. Zhao, L. Shen and N. Sun, "A 13-bit 0.005-mm2 40-MS/s SAR ADC With kT/C Noise Cancellation," in IEEE Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3260-3270, Dec. 2020.

[12] H. Chandrakumar and D. Marković, "A 15.2-ENOB 5-kHz BW 4.5- μ W Chopped CT ΔΣ -ADC for Artifact-Tolerant Neural Recording Front Ends," in IEEE Journal of Solid-State Circuits, vol. 53, no. 12, pp. 3470-3483, Dec. 2018.

[13] S.Pavan, R. Schreier, G. C. Temes, “Understanding Delta-Sigma Data Converters”, Second Edition, IEEE Press, Wiley, 2017.

[14] J. de la Rosa, “Sigma-Delta Converters : Practical Design Guide”, Second Edition, IEEE Press, Wiley, 2018.

[15] S. Norsworthy, R. Schreier, G. Temes, “Delta-Sigma Data Converters: Theory, Design and Simulation”, IEEE Press, Wiley, 1997.

[16] S. Kalogiros, G. Salgado, K. McCarthy and I. O’Connell, "Behavioral Modeling of Low-Frequency Noise in Switched-Capacitor Circuits Using Python," 2022 20th IEEE Interregional NEWCAS Conference (NEWCAS), 2022, pp. 446-449.

[17] K. Martin and A. Sedra, "Effects of the op amp finite gain and bandwidth on the performance of switched-capacitor filters," in IEEE Transactions on Circuits and Systems, vol. 28, no. 8, pp. 822-829, August 1981.

[18] B. Razavi, “Design of Analog CMOS Integrated Circuits”, New York, USA, McGraw Hill, Second Edition, 2017.

[19] S. -E. Hsieh and C. -C. Hsieh, "A 0.4V 13b 270kS/S SAR-ISDM ADC with an opamp-less time-domain integrator," 2018 IEEE International Solid - State Circuits Conference - (ISSCC), 2018, pp. 240-242.

[20] J. Steensgaard, R. Reay, R. Perry, D. Thomas, G. Tu and G. Reitsma, "A 24b 2MS/s SAR ADC with 0.03ppm INL and 106.3dB DR in 180nm CMOS," 2022 IEEE International Solid- State Circuits Conference (ISSCC), 2022, pp. 168-170