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High-speed Electro-absorption Modulator Assisted by Iron Doping for Micro-Transfer-Printing Integration

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***Abstract*—A high-speed lumped-element electro-absorption modulator designed for micro-transfer-printing onto silicon has been tested. The modulators use an iron doped layer to reduce the parasitic capacitance of the devices after transfer-printing, which is beneficial for achieving high bandwidth for heterogeneous integration applications with silicon photonics.**

Keywords—Modulator, heterogeneous integration, micro transfer printing, high-speed photonics

I. Introduction

Developments on promising large scale heterogeneous integration technologies such as micro-transfer-printing (MTP) have received wide interests over the past few years. Beyond the scope of published research, an electro-absorption modulator (EAM) based on the Quantum Confined Stark Effect (QCSE) with optimized ultra-low capacitance is ideal for demonstrating the potential of high-speed applications using MTP as a large scale photonic integration solution [1]. Due to the incompatibility between transfer printing and many high speed device processing techniques, adopting an iron doped layer in the EAM design is proposed in this work as a solution to overcome integration challenges for high-speed performance brought by MTP processing.

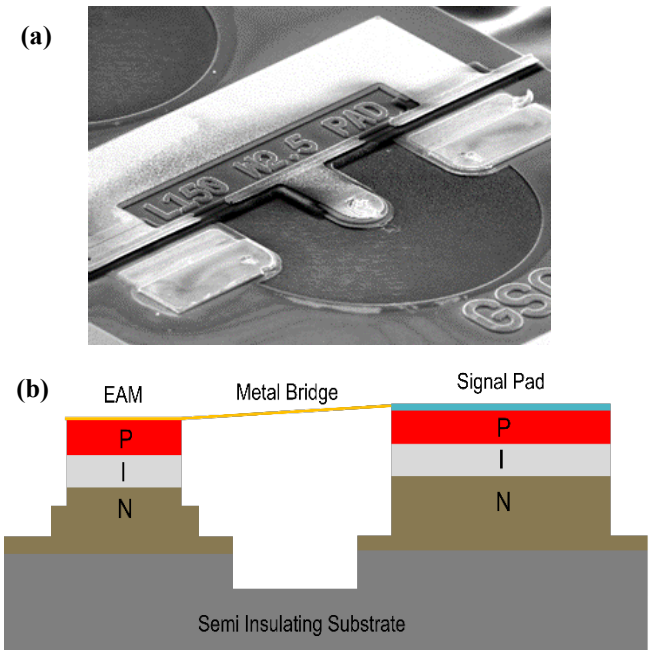


Figure. 1. (a) SEM of a fabricated high-speed EAM Structure (b) Schematic of a cross-section from the structure

II. High-Speed EAM Design and MTP Processing

The high-speed EAM utilizes a customized in-house InP based epitaxy with 12 quantum wells of 9 nm width. The designed working wavelength is 1310 nm for its original monolithic integration purposes and the speed performance is optimized by a high-speed contact pad scheme which has minimized total parasitic capacitance down to below 10fF [2]. As Fig. 1 shows, the monolithically integrated high-speed EAM is fabricated on a semi-insulating substrate to minimize device parasitic capacitance.

For successful MTP photonic integration of the high-speed EAM, as indicated by Fig. 2, the device epitaxy incorporates an extra 400nm InGaAs and 100nm AlInAs bi-layer sacrificial design necessary for MTP coupon release, and in addition, in order to make sure the speed from a heterogeneous integrated high-speed EAM via MTP works on par with a monolithically optimized and fabricated device, the parasitic capacitance of the transfer printed EAM also has to be minimized, namely keeping the overall influence of the potential extra parasitic capacitance generated from MTP processing as small as possible. Therefore, a customized iron doped InP layer with tested resistivity higher than 10^8 Ω-cm is added in the epitaxy design for mitigating negative influences of extra coupled parasitic capacitance on device bandwidth after the transfer printing process.

The fabrication process realized such high-speed EAMs ready for MTP as shown in Fig. 3(a) with high yield. The releasing of the fabricated coupons from the source wafer involves a chemical undercut processing of the InGaAs/AlInAs layer using FeCl3:H2O (1:2) solution [3]. Once the release is completed, the coupons are ready to be transfer-printed onto silicon targets. As an example, Fig. 3(b) shows a series of EAMs with different lengths successfully printed on silicon using a thin BCB adhesion layer. After removing the remained tether photoresist layer on the transfer-printed EAM, the device was prepared and ready for subsequent characterizations as indicated in Fig. 3(c).

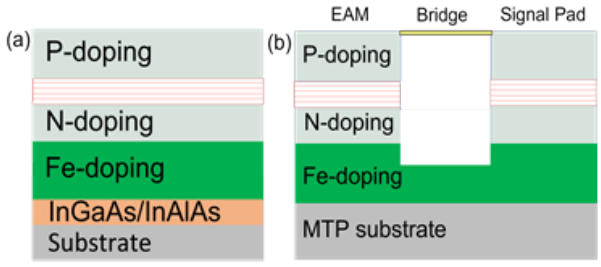


Figure. 2. (a) Epitaxy stack of the MTP compatible EAM (b) Cross-section schematic of a high-speed EAM after MTP

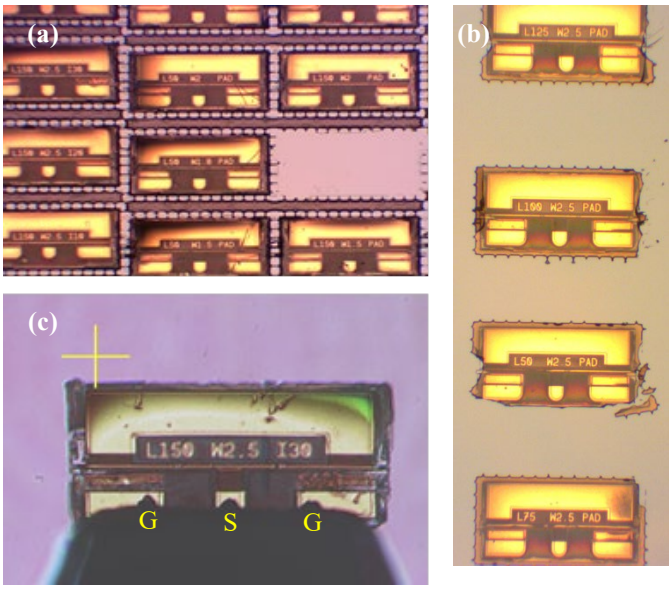


Figure. 3. (a) Fabricated high-speed EAM coupons for MTP (b) Transfer-printed coupons with various EAM lengths (c) A transfer-printed EAM coupon on silicon under S11 characterization

III. S11 Characterization and Simulated S21 Bandwidth

Transfer printed EAMs and calibration structures with and without the iron doped layer were tested using a vector network analyzer (VNA) to measure S11 response as shown in Fig. 4. The reflected RF signal measured through port 1 of VNA from the calibration structures of the signal pad, metal bridge, and the EAM are extracted to fit into an inductor-resistor-capacitor equivalent circuit model to study the effect of parasitic capacitance on the device bandwidth [2]. The signal pad parasitic capacitance from the transfer-printed EAM using iron doping has been found to be as low as 5.3fF which is nearly the same as the 5fF capacitance from a high-speed EAM fabricated on semi-insulating wafer, whereas the lowest pad parasitic capacitance of a transfer-printed EAM without using iron doping was found to be 21.39fF.

Preliminary S11 testing results suggest using iron doping could reduce device parasitic capacitances after MTP, reaching a measured complex impedance close to EAMs fabricated on a semi-insulating wafer. The 3dB bandwidth from simulated S21 response based on the equivalent circuit model of transfer-printed EAMs with and without the iron doped layer are shown in Figure 5, indicating a clear advantage of using an iron doped layer to maintain its high bandwidth. More MTP EAMs for heterogeneous integration are in progress which have been designed to achieve improved facet formation for optical edge coupling and overall transfer-printing yield. Upon completion, experiments to characterize the bandwidth of the transfer-printed EAMs could be completed via S11 and S21 measurements.

IV. Conclusion

This work presents a promising way for photonic devices in MTP integration to maximize high-speed performance by using

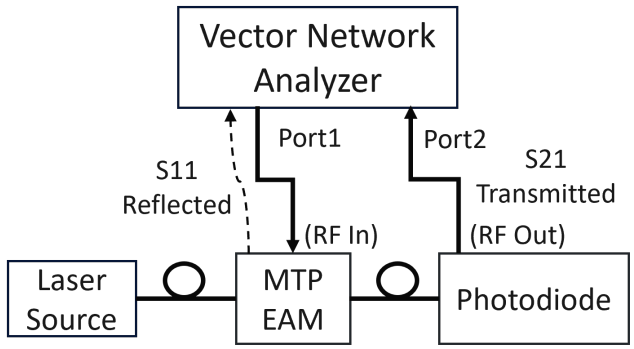


Figure. 4. Schematic of measurement setup for S11 and S21 characterizations of MTP EAM

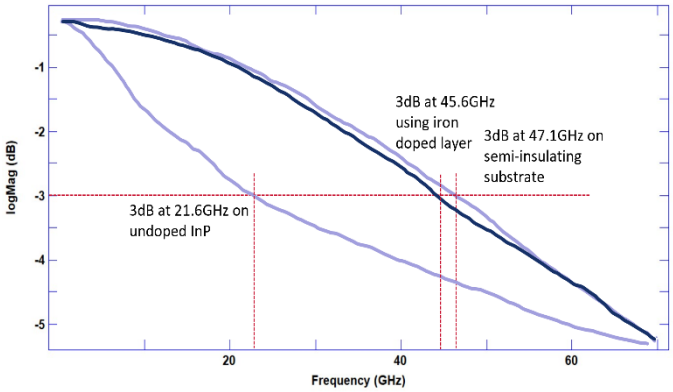


Figure. 5. Simulated S21 for monolithically fabricated EAM and transfer-printed EAM using and without using iron doping

an iron doping layer in the device design. The high-speed EAMs have been successfully transfer-printed and characterized to demonstrate effective reduction of parasitic capacitances using iron doping. Edge coupling of such transfer-printed EAMs to silicon photonic chips is planned in the next step along with comprehensive characterizations of the transfer printed EAMs high-speed performance.

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