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**DEPARTMENT OF ELECTRICAL AND ELECTRONICS
ENGINEERING
NATIONAL UNIVERSITY OF IRELAND, CORK**

NANOWIRES FOR 3D SILICON INTERCONNECTION – LOW TEMPERATURE COMPLIANT NANOWIRE- POLYMER FILM FOR Z-AXIS INTERCONNECT

A thesis submitted in accordance with the requirements for the degree of

Doctor of Philosophy

Jing Tao

April 2016

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Declaration

I, Jing Tao, certify that this thesis is my own work and has not been submitted for another degree, either at University College Cork or elsewhere on the basis of the work submitted in this thesis.

Jing Tao

Abstract

Semiconductor chip packaging has evolved from single chip packaging to 3D heterogeneous system integration using multichip stacking in a single module. One of the key challenges in 3D integration is the high density interconnects that need to be formed between the chips with through-silicon-vias (TSVs) and inter-chip interconnects. Anisotropic Conductive Film (ACF) technology is one of the low-temperature, fine-pitch interconnect method, which has been considered as a potential replacement for solder interconnects in line with continuous scaling of the interconnects in the IC industry. However, the conventional ACF materials are facing challenges to accommodate the reduced pad and pitch size due to the micro-size particles and the particle agglomeration issue. A new interconnect material - Nanowire Anisotropic Conductive Film (NW-ACF), composed of high density copper nanowires of ~ 200 nm diameter and 10-30 μm length that are vertically distributed in a polymeric template, is developed in this work to tackle the constraints of the conventional ACFs and serves as an inter-chip interconnect solution for potential three-dimensional (3D) applications.

The main focus of this PhD work is to design, fabricate and characterize the NW-ACF material and to apply the NW-ACF to form interconnects to prove the NW-ACF concept. Commercial ion-track etched membranes with nominal pore diameter of 200 nm were used as nanoporous polymeric templates to fabricate the NW-ACF. Template-based electrodeposition method was employed to obtain a high filling ratio of copper nanowires in the template under optimized electrodeposition parameters. By employing a long-time deposition process, we allowed a continuous copper overgrown layer to form on the template surface and by mechanically stripping this overgrown layer, the NW-ACF with the controlled nanowire length (same as the pore length) and residue-free surfaces can be obtained. SEM, DSC, TGA and DMA analysis were performed to characterize the structural and thermal properties of the NW-ACF material. Thermocompression bonding was carried out to form the NW-ACF interconnects with: 1) indium coated Ti/Cu/Si substrates, and 2) fine-pitch test die with Cu-In bond pads. The effects of bond pad size, bonding temperature and force on the formed interconnects were investigated. The results show that under the optimized bonding conditions, the NW-ACF can form an ultra-small interconnection (at $10 \times 10 \mu\text{m}^2$ pad area) with an ultra-low interconnection resistance (0.03-0.04 Ω per interconnect), which is the best fine-pitch capability reported so far in the literature for the nanowire based interconnects. The contact mechanism of the nanowire formed interconnects was understood by STEM, EDS and XRD analysis. The penetration contact mode of the nanowire to In surface and the interdiffusion of Cu and In atoms in such contact are confirmed. The viability of NW-ACF bonding to Au bumpless die has also been verified and the results show a superior DC and thermal performance of the NW-ACF interconnects as compared to a commercial particle-based ACF. High frequency performance of the NW-ACF interconnects was also studied and shows good RF transmission properties, which is comparable to that of the solder-bump interconnects. Finally, the reliability tests of the NW-ACF interconnects have been completed under 1100 thermal shock cycles and 800 hours of high temperature and humidity test and the typical failure mechanisms were understood.

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List of Publications

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Author's Contribution

In Publication A, the author planned the experimental work together with co-authors, performed the experimental work and wrote the manuscript with the help of the co-authors.

In Publication B, the author planned the experimental work together with co-authors, performed the experimental work with the help of Tyndall fab for wafer fabrication, discussed the experiment results and wrote the manuscript with the help of the co-authors.

In Publication C, the author planned the experimental work together with co-authors, performed the experimental work independently, discussed the experiment results and wrote the manuscript with the help of the co-authors.

In Publication D, the author planned the experimental work together with co-authors, performed the experimental work independently, discussed the experiment results and wrote the manuscript with the help of the co-authors.

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In Publication F, the author wrote the manuscript with the help of the co-authors, based on the work of Publication A to D.

Publication G, is a joint paper together with researchers from Stokes Institute and Villanova University. A part of experiment work (thermal diffusivity measurement) was performed the author. The results was discussed with the co-authors and manuscript was written by E. Dalton and with the help of the other co-authors.

In Publication H, a part of experiment work (S-parameters of lossy Si substrate) was performed the author. The results was discussed with the co-authors and manuscript was written by L. Floyd with the help of the other co-authors.

Glossary of Abbreviations and Symbols

1D	one-dimensional
2D	two-dimensional
2.5D	2.5-dimensional (mainly refer to interposer technology)
3D	three-dimensional
ACA	anisotropic conductive adhesive
ACF	anisotropic conductive film
AFM	atomic force microscopy
BEOL	back-end of line
BGA	ball-grid-array package
BCB	benzocyclobutene
BOE	buffered hydrofluoric acid
CNT	carbon nanotube
CMP	chemical mechanical polishing
CVD	chemical vapor deposition
CMOS	complementary metal-oxide semiconductor
C4	controlled collapse chip interconnection
DRIE	deep reactive ion etch
DI	deionized
DNA	deoxyribonucleic acid
D2D	die-to-die
D2W	die-to-wafer
DSC	differential scanning calorimetry
DBI	direct bonding interconnect
DC	direct current
DIP	dual-in-line package
DMA	dynamic mechanical analyser
ECA	electrical conductive adhesive
ECD	electrochemical deposition or electrodeposition
ECP	electrochemical plating
EDS	energy-dispersive X-ray spectroscopy
FEOL	front-end of line

GSG	ground-signal-ground
HT/HH	high temperature and humidity
OH	hydroxyl
I/O	input/output
IC	integrated circuit
IMCs	intermetallic compounds
JCPDS	Joint Council for Powder Diffraction Studies
kgf	kilogram force
KGDs	known good dies
μbump	micro-bump
MEMS	microelectromechanical systems
MCM	multi-chip modules
NEE	nanoelectrode ensemble
NW-ACF	Nanowire Anisotropic Conductive Film
NCA	non-conductive adhesive
NCF	non-conductive Film
NCP	non-conductive paste
NW	nanowire
PDA	personal digital assistant
PR	photoresist
PVD	physical vapor deposition
PC	polycarbonate
PET	polyethylene terephthalate
PI	polyimide
AAO	porous alumina membranes
PCB	printed circuit board
RF	radio frequency
RDL	redistribution lines
RMS	root mean square
ROM	rule-of-mixture
SEM	scanning electron microscope
STEM	scanning transmission electron microscope
S-parameter	scattering- parameter
SPE	silicon packaging efficiency

SLID	solid-liquid interdiffusion
SMUs	source/monitor units
SiP	System in Package
ITRS	Technology roadmap for Semiconductors
CTE	thermal expansion coefficient
TIM	thermal interface material
T/S	thermal shock
TCB	thermocompression bonding
TGA	thermogravimetry analyser
TMA	thermomechanical analysis
TSV	through silicon via
UBM	under bump metallurgy
VNA	vector network analyser
WLP	wafer-level packaging
W2W	wafer-to-wafer
XRD	X-ray diffraction

Chapter 2

T_g	glass transition point
R_c	contact resistance
ρ	electrical resistivity
N	number of conduction paths
E	elastic modulus
ν	Poisson's ratio
F	contact force
D	diameter
φ_0	Fermi level
K	dielectric constant
$R_{\text{constriction}}$	constriction resistance
$R_{\text{tunnelling}}$	tunnelling resistance
R_{circle}	circle resistance
R_{ring}	ring resistance

V_f	volumetric factor of the fiber
E_m	Young's modulus of the matrix
E_f	Young's modulus of the fiber
G_m	matrix shear modulus
M^{n+}	metal species
M_s	metal adatom
E_{eq}	equilibrium potential of the solution
η	overpotential

Chapter 3

V-t	potential-time
\emptyset	real filling ratio
V_{Cu}	volume of Cu nanowire
V_T	total volume of template including the pore volume
W_1, W_2	film weight before and after electrodeposition
ρ_{Cu}	density of copper
H	thickness of film
S	surface area of the sample being weighed
C_p	heat capacity
$\tan \delta$	tangent delta
R_{Cu-In}	resistance of Cu-In multilayer
R_{NW}	resistance of the nanowires
$R_{Contact}$	contact resistances
ρ_{Cu-In}	resistivity of Cu-In multilayer (including IMC)
L	effective length (thickness of Cu-In layer)
S	cross-section area (bonding area)
ρ_{NW}	resistivity of Cu nanowire
L	length of nanowire
D	diameter of the nanowire
n	number of the nanowires per bonding area

Chapter 4

V	voltage
I	current
I_{leak}	leakage current
Z_0	characteristic impedance
S_{11}	reflection coefficient
S_{21}	transmission coefficient
R	series resistance per unit length
L	series inductance per unit length
C	shunt capacitance per unit length
G	shunt or leakage conductance per unit length
γ	propagation constant
f	frequency
R_{leak}	resistance induced by the low resistivity Si
C_{ox}	capacitance induced by the low resistivity Si
C_{NW}	capacitance induced by nanowires
T_{j_max}	maximum junction temperature
Θ_{TIM}	total thermal impedance
Θ_{c1}, Θ_{c2}	contact impedances
BLT	bond line thickness

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Chapter 1 Background and Motivation

1.1 Evolution of Electronic Packaging

Nowadays, people are living in a world with electronics proliferating into all aspects of their lives including transportation, communication, energy, medical and health. Cars, trains and planes rely on electronic systems to control, operate and communicate. Patients are diagnosed and medically treated using electronic instruments which can perform imaging, manipulation and vibration functions. In the information era we are living in, the innovations from mobile products such as smart phones, PDAs to massive network infrastructures and cloud computing provide the possibility of global connectivity in a fast and convenient way. However, none of these electronic devices and systems can be applied in their field use without the use of electronic packaging, which is the final manufacturing process which transforms semiconductor devices into functional products.

The functions that electronic packaging provide are [1]:

- Electrical connections for signal transmission, power input and voltage control;
- Thermal dissipation;
- Physical and mechanical protection from environment.

There are packaging interconnect hierarchy levels defined by Japan JISSO Technology Roadmap Group to explain the chip to packaging levels [2]: Level 1 – **Electronic Element**, refers to a bare die/wafer or discrete component (resistor, capacitor, inductor, transistor, diode, fuse, etc.) with metalized terminals or termination ready for mounting; Level 2 - **Electronic Package**, refers to an Individual Electronic Element or Elements in a container which protects the contents to assure the reliability and provides terminals to interconnect the container to an outer circuit; Level 3 – **Electronic Module**, refers to a functional block which contains Individual Electronic Elements and /or Electronic Packages, to be used in a next level assembly. Fig. 1.1 schematically illustrates three package/interconnect levels with an example of two stacked silicon die in a package assembled on the printed circuit board (PCB). In the example, the silicon die represent the electronic elements in Level 1. In Level 2, the electronic package is formed by stacking the silicon dies on the substrate with die attach material, electrically connecting the die to the substrate with wire bonding and encapsulating

the die and Au wires in a mold to provide the physical and mechanical protection from the environment. In Level 3, the electronic package is assembled to the PCB with solder ball interconnects to form the electronic module.

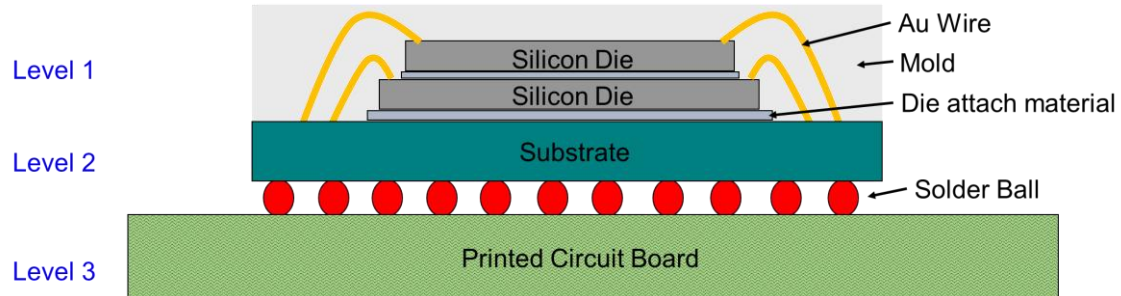


Figure 1.1 Schematics showing three package/interconnect hierarchy levels.

The single-chip package was the earliest developed packaging technology where a single chip was connected to the substrate using wire-bonding and flip-chip technology and then encapsulated in molding material. With different substrate types, such as lead frames and rigid laminate substrates, various package types have been developed such as dual-in-line package (DIP) and ball-grid-array package (BGA) to form the through-hole or surface-mount components for the next level of PCB and module assembly. For a traditional single-chip package, the silicon packaging efficiency (SPE), which is defined as the area of silicon divided by the total substrate area, is only 10-25% [3].

To meet the requirements of portable consumer markets with the driving factors of small size, thickness, weight, and better performance, wafer-level packaging (WLP) has been developed to perform integrated circuit (IC) packaging process steps at the wafer level. Wafer-level chip-scale packaging WLCSP, also known as fan-in package, was developed to minimize the package size to $1.2 \times$ of the die size [4]. On the other hand, the fan-out WLP die technology was developed by reconstituting and embedding the chips in an epoxy compound to expand the area available for interconnect redistribution and to form fine pitch interconnection at reasonable cost [5]. With WLP, SPE can be increased to ~80%.

With the driving factors of system miniaturization, technology integration and performance enhancement with a reduced overall cost, multiple die and/or passive components were proposed to be integrated in one package. Early approaches to integrate multiple die had been achieved by multi-chip modules (MCM), where the multiple die are placed side by side on ceramic substrate with polymer-copper wiring [6]. Later, people utilized the third dimension to vertically stack die or packages. This leads to 3D packaging

approaches or System in Package (SiP). SiP is defined as a combination of multiple active electronic components of different functionality, assembled in a single unit that provides multiple functions associated with a system or sub-system [2]. This chip or package stacking configuration greatly reduces the package area. With SiP, SPE can reach higher than 100%.

Although SiP has been able to integrate most of the functional devices in a system with a reasonably low cost, the interconnections between the functional devices are only achieved by wiring the individual chips to the substrates. Thanks to the through-silicon-via (TSV) technology [7], the vertical interconnection between the die can be directly formed with the minimum interconnect length. 3D integration [8-10] based on TSVs and inter-chip wiring has become the most advanced package technology nowadays with the main advantages being:

- Multifunctionality - functional combination of dissimilar components including processor, memory, radio frequency (RF), sensors, power and microelectromechanical systems (MEMS) devices can be integrated in one system package. The example of 3D integration of MEMS/IC system has been given by Ramm et al. [8].
- Increased performance - compared with two-dimensional (2D) technology or 3D packaging, 3D integration with TSVs can achieve much better system performance due to the much shorter interconnects between the functional devices. Shorter interconnects result in a lower interconnect resistance and capacitance and therefore low time/RC delay.
- Increased data bandwidth - 3D integration allows a larger number of input/output (I/Os) as compared to 3D packaging and the number of I/Os is proportional to the data bandwidth of the integrated system [11].
- Reduced power - conventional wire-bonded interconnects consume a large portion of power budget in a chip due to high parasitic losses and 3D interconnects with TSVs can reduce the power dissipation associated with interconnects by 80% and reduce the system power dissipation by 35-55% [3].
- Small form factor - due to the shortest interconnect distance and multiple die stacking, 3D integration has the highest SPE with the package size reduction in both height, length and width directions.
- Reduced packaging - compared to single-chip package and 3D package, 3D integration reduces the package steps for individual ICs, i.e. the interconnection can be made directly between die instead of from die to substrate.
- Increased yield and reliability - 3D integration yield and reliability are greatly dependent on the bonding processes to stack the devices with different backend-of-line layers. By

adopting the die-to-die (D2D) and die-to-wafer (D2W) stacking with known good dies (KGDs), the assembly yield can be improved [12].

- Flexible heterogeneous integration and reduced overall cost - heterogeneous integration of different functional devices increase the diversification of the system and with the technology development and production volume ramp-up, the overall cost will eventually decrease.

Generally, electronic packaging has evolved from the single-chip package to WLP, SiP and 3D IC integration by pursuing smaller form factor, increased functionality, better system performance and reduced overall cost. The trend of the package evolution is illustrated in Fig. 1.2 [13] with respect to the year the technology was introduced to the market. 3D IC and heterogeneous integration, as one of the most updated and sophisticated packaging technologies, is attracting more and more attention in both academic and industrial fields.

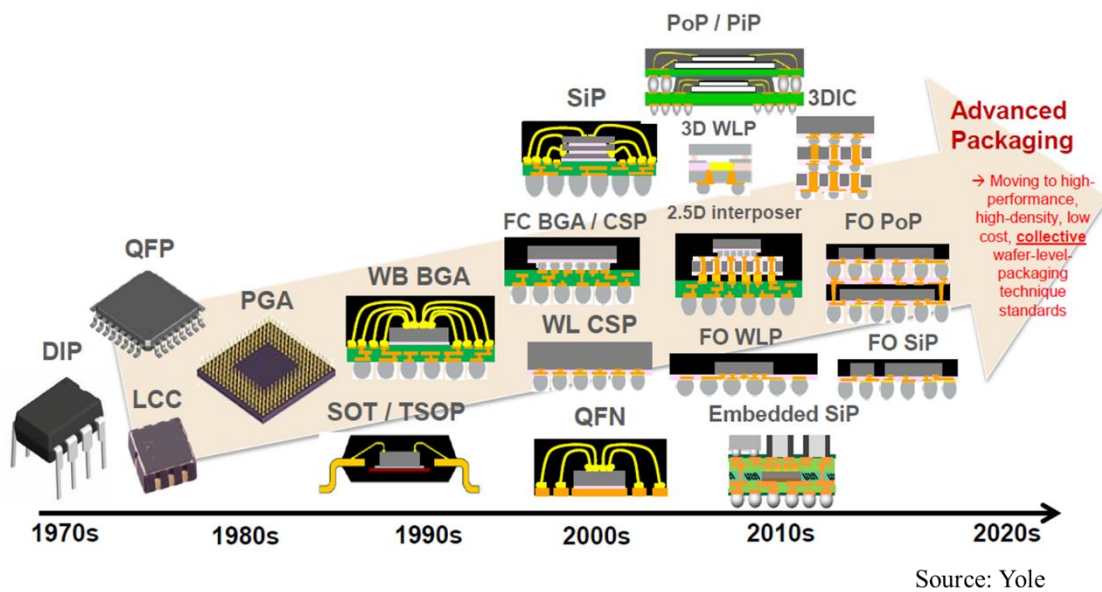


Figure 1.2 Semiconductor chip packaging market evolution [13].

1.2 Conventional Interconnection Methods and New Approaches for 3D Integration

1.2.1 Through Silicon Vias (TSVs)

Through Silicon Via (TSV) technology [14] is the most important enabling technology for 2.5D/3D IC integration. TSV is defined as a galvanic connection between the two sides of

a Si wafer that is electrically isolated from the substrate and from other TSV connections [15]. The concept of TSVs for wafer-level 3D integration was introduced in 1999 by Infineon based on the “via-last” process [16]. The name relates to the order of the TSV process with respect to the device wafer fabrication process, which also applies to “via-first” and “via-middle” processes. The three via sequences refer to fabrication of TSVs before the Si front-end of line (FEOL) device fabrication processing (“via-first”), after the Si FEOL device fabrication processing but before the back-end of line (BEOL) interconnect process (“via-middle”), after or in the middle of the Si BEOL interconnect process from back side or front side (“via-last”). Fig. 1.3 shows the schematic of the TSV formation process based on “via-first”, “via-middle” and “via-last” [17].

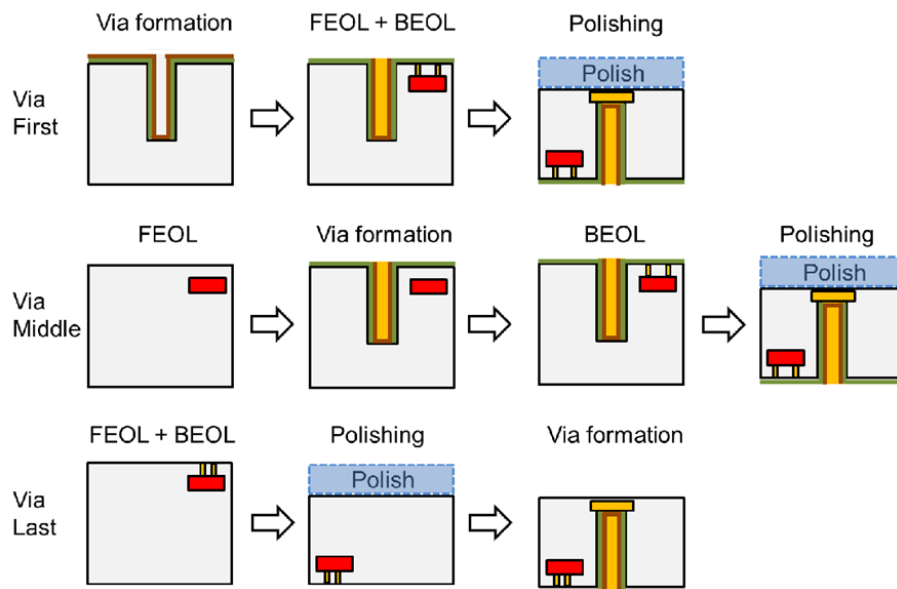


Figure 1.3 Schematics showing the three main approaches for TSV fabrication: Via First, Via Middle and Via Last [17].

The major processes to form TSVs are illustrated in Fig. 1.4 [14], which are:

- Patterning process with lithography mask.
- Deep Si etching using deep reactive ion etch (DRIE) /BOSCH Process [18] to form high aspect ratio via holes.
- Photoresist and wafer cleaning process.
- TSV liner deposition which uses high temperature thermal oxide deposition or low-temperature chemical vapor deposition (CVD) process [19] to electrically isolate the TSV connections from the Si substrate.

- e) TSV barrier deposition using physical vapor deposition (PVD) [20] to avoid migration of TSV metal into the Si, and Cu seed layer deposition [21] for Cu TSVs formation.
- f) TSV metal filling process using electrochemical plating (ECP) of Cu [21] or other types of conducting materials (aluminium or tungsten).
- g) Chemical mechanical polishing (CMP) for removal Cu overburden for Cu TSVs [22].
- h) TSV capping deposition if needed.

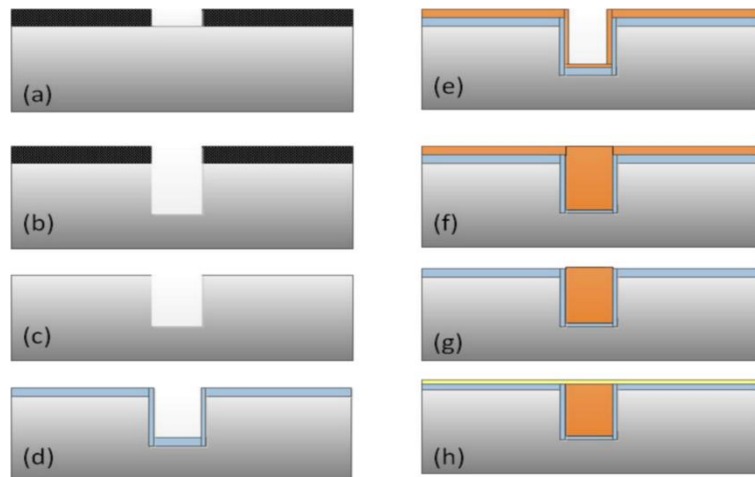


Figure 1.4 Major process modules in TSV formation [14]. (a) TSV mask lithography, (b) deep Si etch, (c) photoresist and wafer cleaning, (d) liner oxide deposition, (e) barrier metal and Cu seed sputtering, (f) Cu ECP, (g) Cu CMP, and (h) TSV capping deposition

Wafer thinning is an important process step to form TSVs in the thinned wafer (“via-last”) or to reveal the TSV nails after TSV formation (“via-first, middle or last”) before the wafer backside process. The key process for wafer thinning is temporary bonding of the device wafer to a carrier substrate (glass or wafer) for mechanical grinding and thin wafer handling [23, 24]. If the TSVs are already formed in the wafer, a wafer backside process sequence is performed to form the passivation layer, redistribution lines (RDL) and bumping [25, 26]. After the backside process, the die/wafers containing TSVs are ready for 3D stacking, where the electrical interconnections are formed between different device layers or an interposer. Various interconnect methods are under development, among which metal-to-metal or direct metal/oxide bonding methods [27, 28] have been developed for wafer-to-wafer (W2W) stacking; while copper-tin (Cu-Sn) based solid-liquid interdiffusion (SLID) [29, 30] or Cu/Sn micro-bump technologies [26, 31] are prevalent bonding technologies for D2D and D2W

stacking with the TSVs. TSV technology combined with Cu-Sn micro-bumps has been successfully demonstrated by Xilinx for their commercial 28nm technology FPGA product and the representative SEM images of the TSV and micro-bump are shown in Fig. 1.5 (a) and (b), respectively [32].

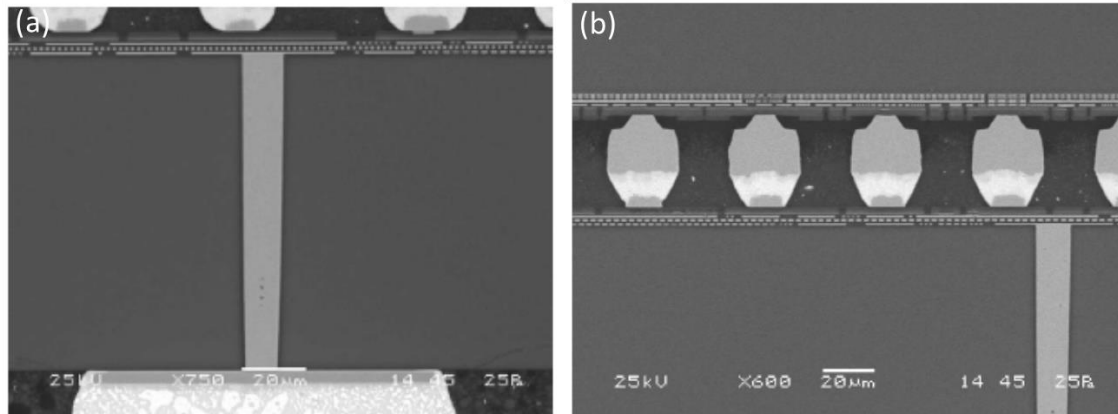


Figure 1.5 2.5D integration demonstrated by Xilinx and cross-sectional SEM images showing (a) the TSV in 2.5 interposer and (b) the Cu-Sn micro-bumps [32].

1.2.2 Micro Bumps (μ bump)

For D2D and D2W stacking, the industry is currently focused on micro-pillar or micro-bump interconnect methods because this technology combines the advantages of high throughput and compatibility with the conventional flip chip interconnect methods [12]. Flip chip technology with solder balls is a face-down assembly technique originally developed by IBM and called C4 (controlled collapse chip interconnection) in the 1960s to electrically connect individual die to a substrate [33]. Compared with wire bonded interconnects [34], flip chip interconnects have the advantages of higher number of I/Os, better electrical performance due to the shorter interconnection length and a faster processing time due to all interconnects being bonded in a single step.

Associated with flip chip technology, there are bumping techniques that need to be performed depending on the requirements. There are different approaches of bumping techniques such as stud bumping, solder bumping, plated solder bumping and adhesive bumping [35, 36]. Among them, flip chip technology based on solder balls /bumps is the most developed interconnect method for package-to-board, chip-to-package and die-to-die/wafer technologies. Fig. 1.6 shows the solder ball/bump based flip chip interconnect at

different interconnect levels at which the solder ball sizes are gradually reduced. For BGA packages to electrically connect to PCB, the solder balls have a diameter of 200 μm and a ball pitch of 500 μm . While at chip-to-substrate interconnect level, the land pitch of solder ball interconnects will reach <100 μm pitch by the year 2017 for cost-performance package type (CPU, GPU, processor) [12]. For the die-to-die/wafer interconnect level in 3D integration, the stressing interconnect pitch size is steadily decreasing below 50 μm [26, 31]. With an ever decreasing pitch size, the conventional soft solder balls technology is challenged due to the spherical geometry of the balls, the decreasing of the standoff height and expanding of the solder width after reflow [37]. The alternative solutions proposed are copper pillar bumps [38], which have a non-reflowable copper pillar base and a reflowable solder cap, as well as Cu/Sn micro-bumps [39] consisting of an under bump metallurgy (UBM) layer and an electroplated solder layer, as illustrated in Fig. 1.6. Compared with a traditional solder ball, there is a reduced volume of solder in a μbump and during bonding, the greatest portion of solder transforms into intermetallic compounds (IMCs) due to interdiffusion with the base metal.

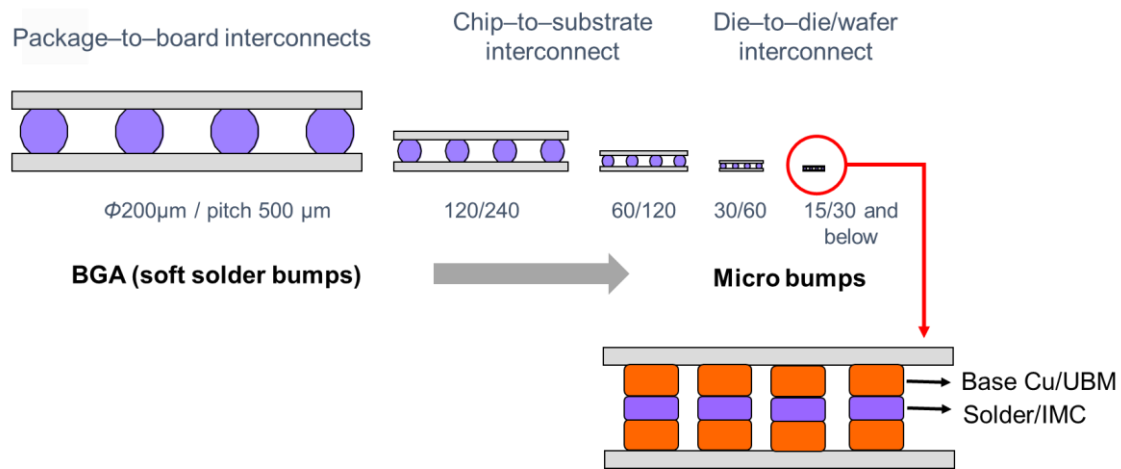


Figure 1.6 Geometrical roadmap of flip chip solder ball/bump interconnects.

In 2010, ITRI reported the Cu/Ni/SnAg μbump technology for 3D chip stacking at 30 μm pitch [40, 41], stressing the influence of process parameters and underfill material on the reliability of the μbump . For the bumping processes, the difficulties lie in bumping defects such as bridge bump, missing bump and variations in bump height. Meanwhile, due to the difficulty of removing flux residue within the narrow gap, plasma treatment had to be used to remove Sn oxides before assembly. To diminish the solder squeezing problem, thermo-compression bonding process with gap control (by optimizing the bonding parameters) is

applied to form a good joint. After solder joint formation, underfill dispensing is needed to protect μ bumps from thermal and mechanical stresses. Fine-gap filling capability of the underfill material is necessary to achieve a high dispensing yield with no voids. The main fracture mechanisms of the μ bump joints are crack propagation along the interface between solder and the formed intermetallic compounds (IMCs) and in the interface of Cu UBM/Al trace, as shown in Fig. 1.7 (a) and (b), respectively [41]. Underfill cracking can also happen due to the degradation of adhesion strength between the underfill and passivation layer. Thermo-mechanical stress caused by local thermal expansion coefficient (CTE) mismatch between the UBM, solder, IMC and underfill is another reliability issue of these μ bump interconnects which needs to be addressed for high temperature processes [42].

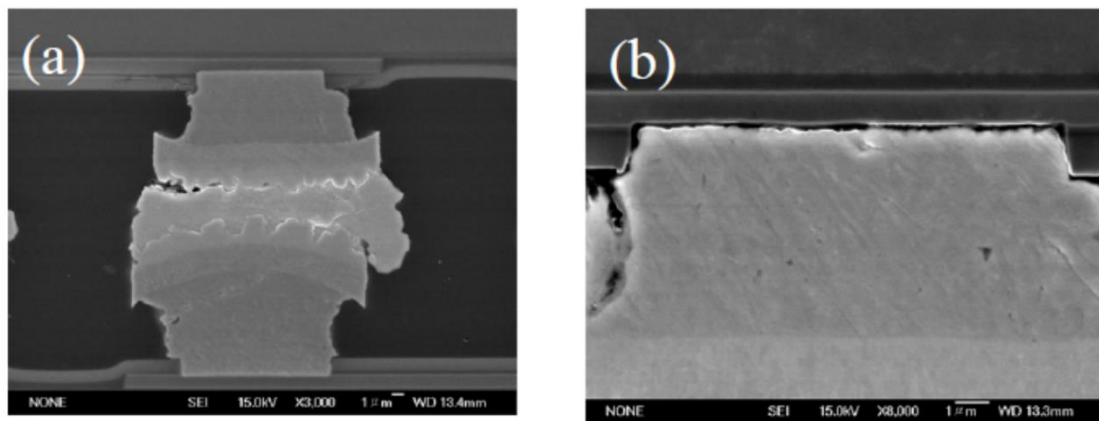


Figure 1.7 Typical failure mechanisms of the μ bump (a) the crack propagated along the interface between solder and Ni₃Sn₄ IMC and (b) the crack in the interface of Cu UBM/Al trace [41].

1.2.3 Cu-Cu Direct Bonding

With 3D integration, heterogeneous devices including complementary metal-oxide semiconductor (CMOS) devices (e.g. logic, memory, etc.) and non-CMOS devices (e.g. MEMS, sensors, etc.) need to be stacked on top of each other. For the temperature sensitive non-CMOS devices, a high bonding process temperature ($> 300\text{ }^{\circ}\text{C}$) can cause damage to the devices and influence their performance. Meanwhile, the die/wafer warpage needs to be minimized during the die stacking processes to ensure high bonding yield. It is reported that the μ bump and underfill processes with a typical process temperature of $250\text{ }^{\circ}\text{C}$ can cause a significant warpage of 2.39 mil ($\sim 60\text{ }\mu\text{m}$) during the chip stacking process [32]. Although

low-temperature solder interconnection such as eutectic Sn-Bi can be a feasible solution to reduce chip/board warpage and has been developed to form a small size bump (22 μm width) [43], the solder is only applied for Si to organic substrate interconnection at a relatively large pitch size (500 μm) [44] and there is no report available for its application for D2D interconnection. Other solutions for low-temperature interconnection processes are in demand for 3D integration.

Ziptronix has developed wafer-level direct bonding interconnect (DBI) by direct Cu-Cu and oxide bonding at room temperature using copper CMP process after the BEOL Cu damascene process, followed by 125 $^{\circ}\text{C}$ post annealing [28]. LETI/STMicroelectronics have developed a similar approach using direct hydrophilic Cu-Cu bonding at room temperature, atmospheric pressure, and ambient air [45]. A post annealing process of 200 $^{\circ}\text{C}$ is also required. The main challenge presented by these processes is that in the area of surface preparation, where a very flat surface roughness (root mean square, RMS, roughness lower than 0.5 nm) and particle-free hydrophilic surface have to be prepared before bonding. Researchers in the University of Tokyo have successfully applied a surface activated bonding (SAB) method for Cu-Cu direct bonding at room temperature without any annealing steps [46]. A bumpless interconnect with 6 μm pitch Cu electrodes has been realized at room temperature using the SAB method, as shown in Fig. 1.8 [46]. However, the whole bonding process has to be carried out under an ultrahigh vacuum condition ($<10^{-5}$ Pa) and this makes these processes very expensive for mass production.

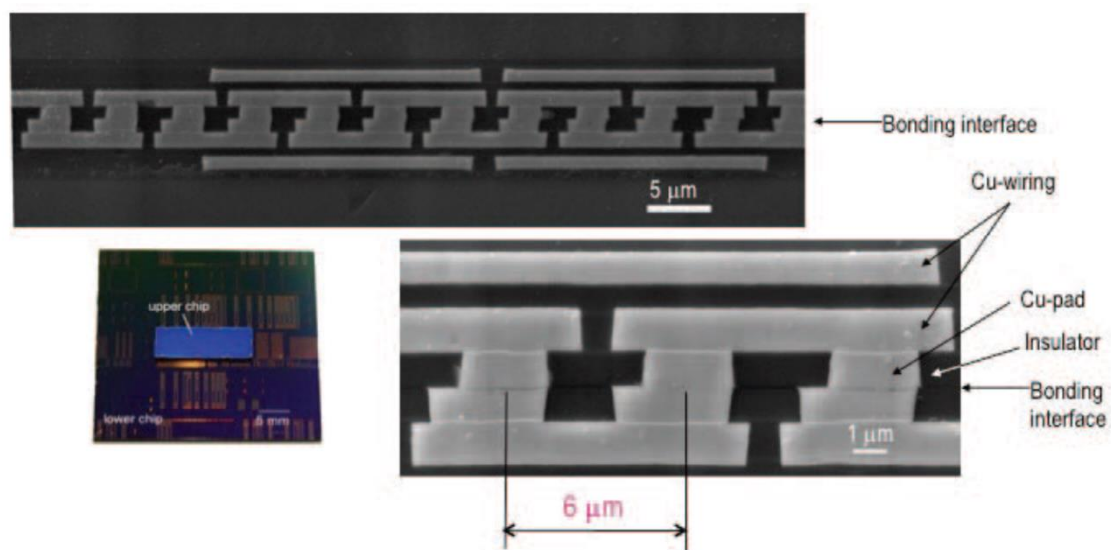


Figure 1.8 Cu bump-less interconnects of 6 μm pitch bonded by SAB at room temperature [46].

1.2.4 Adhesive based 3D Interconnect Methods

1.2.4.1 Nonconductive Film (NCF) based Interconnects

Adhesive bonding is a low-temperature, low-cost method that is applied for wafer-to-wafer bonding before TSV formation. The main advantages of adhesive bonding include the insensitivity to surface topography, the low bonding temperatures (between room temperature and 450 °C, depending on the polymer adhesive), the compatibility with standard CMOS integrated circuit wafers and the ability to join different types of materials [47]. However, the adhesives used for die/wafer level bonding can only mechanically join two bonding surfaces together, but they do not provide electrical connections. For bumped die/wafers, pre-applied underfill materials and nonconductive film (NCF) can be deposited or laminated on the bumped surface of die/wafers before thermo-compression bonding is performed. When the adhesives are squeezed out of the bump area under heat and pressure, the bumped metal or solder can be joined together to form the electrical connections [48-50]. This pre-applied underfill material solves the problem of capillary fill processes when the occurrence of voids and long underfill times might be needed to fill the narrow gap in fine-pitch interconnects. However, this technology still requires a bumping process with a relatively large bump height and one of the reliability concerns is that underfill residue can be trapped between the pads in the formed joints and induce voids and open joints [51].

1.2.4.2 Anisotropic Conductive Adhesive (ACA) Technology

Anisotropic conductive adhesive (ACA), is a Z-axis interconnect material which can provide direct electrical connection between the two bonding surfaces. The electrical connection is provided by the conductive fillers embedded in the adhesive matrix; while the X-Y insulation is maintained due to the insulation of the individual conductive particles. ACAs have been considered as a potential replacement for the soldered interconnects [52] and have been widely used as a flip-chip interconnect technology for chip-to-substrate packaging applications, especially in the display industry [53-56]. The potential to apply ACA material for W2W bonding has been demonstrated by incorporating micro-size metal coated polymer balls into BCB material [57]. The main advantages of ACAs are fine-pitch capability (for flip-chip application), lower processing temperature (< 200 °C, which makes it also applicable to bond flex substrates), less environmental impact (no flux process), reduced cost (elimination of underfilling) and decreased IMC reliability concerns.

Conventional ACAs have spherical conductive particles of 3-15 μm in size, which are randomly dispersed throughout a polymer matrix with a filling ratio of 5-20%. This results in unidirectional electrical conduction when the film is compressed and when the particles form an interconnection between the bond pads. Fig. 1.9 shows schematic of the flip-chip interconnects formed by the conventional particle-based ACA between the IC and the substrate. The electrical connection is formed by the trapped conductive particles between the opposite bond pads and the electrical insulation in X-Y plane is maintained due to the highly dispersed particles in the polymer.

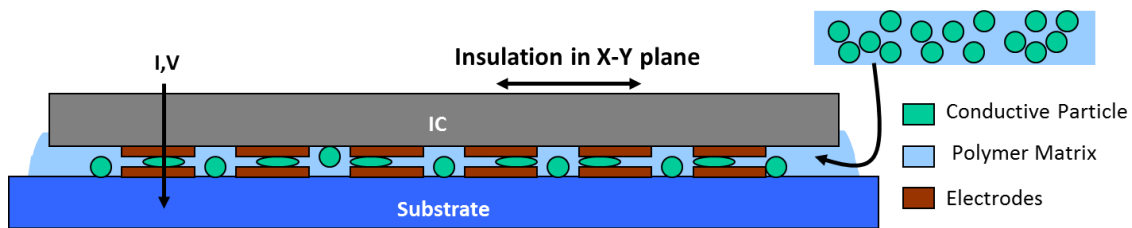


Figure 1.9 Schematic showing the flip-chip interconnects formed by the particle-based ACA between the IC and the substrate; the spherical particles are trapped and deformed to make connection between the opposite pads.

However, the limitations of conventional ACAs are that, particle size cannot be smaller than 2-3 microns to achieve an adequate bondline thickness and a much higher density of these smaller particles is needed to achieve the required electrical conductivity between pads. Meanwhile, high density particles face agglomeration problems during the fabrication of the ACAs as well as the bonding process and this can cause short-circuiting in the X-Y plane [58]. For conventional ACAs, the electrical connection is formed by physical contact of the particles to the metal surfaces, and thereby, an unstable contact resistance can arise due to a loss of compressive force and this also increases as a result of delamination [59].

As a more promising alternative, Nanowire Anisotropic Conductive Film (NW-ACF) which is composed of a polymer matrix and high density vertical metallic nanowires has been developed and demonstrated for die-to-die interconnection [60]. Fig. 1.10 shows the concept of the NW-ACF as the interconnection between the IC and substrate. The high aspect ratio nanowires can act as the vertical conductors to electrically connect the opposite bonding pads with the wire ends; while the polymer matrix provides the mechanical strength of the interconnects. Compared with the particle-based ACAs, the NW-ACF has the intrinsic

advantages of finer pitch size (nano-scale conductors) and lower contact resistance (high density nanowires). Furthermore, the particle agglomeration and co-planarity issues experienced by the conventional ACAs are expected to be diminished by using NW-ACF due to the less mobility and structural compliance of the high aspect ratio nanowires. The NW-ACF has been successfully demonstrated for die-to-die bonding at a minimum pad/pitch size of 10/30 μm with a low contact resistance $\sim 40\text{ m}\Omega$ per pad [61]. The feasibility of the NW-ACF to interconnect with the non-soldered Au bumpless pads (pad height $< 1\text{ }\mu\text{m}$) has also been verified [62].

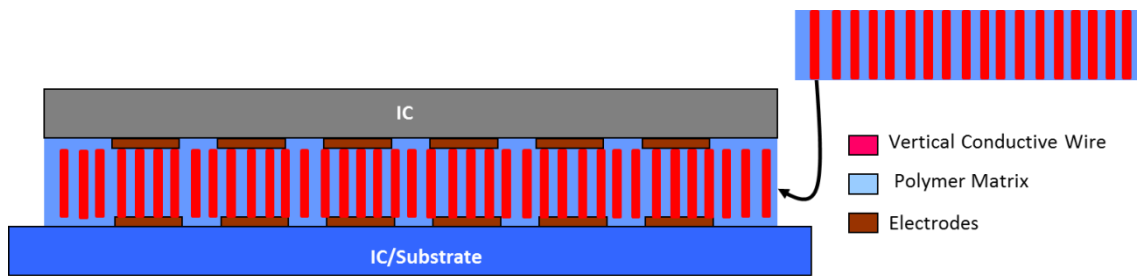


Figure 1.10 Schematic showing NW-ACF as the interconnects between the IC and substrate.

1.2.5 Comparison of the 3D Interconnect Methods

Table 1.1 compares the different interconnection technologies for 3D stacking, including Cu-Cu direct bonding, Cu/Sn μ bump, conventional ACF and NW-ACF. Among them, Cu-Cu direct bonding and solder μ bump are existing technologies which have been applied for 3D interconnection. Despite the ultra-fine pitch capability, the technologies are limited by process cost or high process temperature and the related reliability issues. On the other hand, ACF technologies can be recognized as a low-temperature, fine-pitch interconnect method applied for chip-to-substrate and D2D applications. As compared to the particle-based ACF that is limited by the applicable pad/pitch size due to the micro-size conductors, NW-ACF with nanowires orderly distributed in the polycarbonate matrix has shown its potential as an ultra-fine pitch interconnect method. As a proof-of-concept development, polycarbonate (PC) matrix is so far the most suitable commercially available template for material development. The reliability property of the NW-ACF associated with the polycarbonate template can be further improved if other polymeric templates are available beyond the state-of-art.

Table 1.1 Comparison of interconnection technologies for 3D stacking.

	Solder μbump ^[31, 41, 42]	Cu-Cu Direct Bonding ^[28, 45, 46]	Particle-based ACF	NW-ACF
Applications	3D interconnect	3D interconnect	Chip-to-substrate, D2D	D2D 3D integration
Companies /Institutes	RTI International (2010), ITRI (2011)	LETI (2008), Uni. of Tokyo (2008), Ziptronix (2009)	Hitachi (commercial ACF) (evaluated in this work)	Tyndall (evaluated in this work)
Interconnect Methods	Cu-Ni/Au-SnAg, Cu-Sn	Cu-Cu (bumpless)	Adhesive based, Ni/Au coated particles	Adhesive based, Cu-NW
Minimum Pitch Size (μm)	10	6	80	30
Minimum Pad Size (μm)	4	3	40	10 (to date)
Process Temperature	300 °C (N ₂ purging)	< 200 °C or RT	190 °C	220 °C
Process Time	180 s	30 s or post-annealing, 30 min	lamination time + 5-30 s bonding time	60 s
Bonding Force	5 MPa	64 MPa	16 MPa	29 MPa
Contact Resistance (Ω)	0.07	0.08	0.09 (Cu-In pads)	0.03 (Cu-In pads)
Bond strength	20-30 MPa	> 20 MPa	20 MPa	5-10 MPa*
Reliability Issue	Intermetallic compounds (IMC) growth	N.A.	Polymer degradation	Polymer delamination and degradation*
Specific Requirements	UBM, Wafer bumping, Underfill	Surface treatment, CMP, Vacuum environment	Lamination process	N.A.
Process complexity/ Cost	Medium	High	Low	Low

* Values/issues can be improved by using a different polymer system.

1.3 Research Objectives

The evolution of electronic packaging has led towards 3D system integration in order to address the ever-continuing product needs of miniaturization, increased performance and multifunction capability for next generation ICs. One key technology for enabling 3D integration is 3D die stacking where two or more dies are stacked on top of each other with vertical interconnections. Such high density vertical interconnections only become viable by using TSVs and the chip-to-chip interconnects. According to the International Technology roadmap for Semiconductors (ITRS) roadmap 2012 [15], the predicted contact pitch for TSV dies/wafers at the global interconnect level are 10 μm by using solder micro-bump technology and 5 μm by using metal-to-metal thermocompression bonding in the coming years 2015-2018. However, both technologies face many challenges. For micro-bump technology, the challenges include process difficulties of wafer bumping and underfill process with the decreasing bump size and the reliability issues associated with the intermetallic compounds and under bump metallization, as described in chapter 1.2.2. Moreover, the temperature of the soldering process is more than 250 $^{\circ}\text{C}$, which can result in high thermal stress in the devices to cause the warpage and non-planarity issues and also impact the thermal budget of the processing, particular for the multi-technology node-stacking processes. While for metal-to-metal thermocompression (TC) bonding, the challenges are the expensive wafer processing infrastructure and the bonding equipment required for the mass production. Therefore, developing the interconnect methods, which can provide ultra-fine pitch capability, low processing temperature and a low cost is very important and is highly demanded in all aspects of 3D integration.

The objectives in this work are to develop and prove the concept of a novel nanowire anisotropic conductive film (NW-ACF) material for application in ultra-fine pitch interconnection with a low-temperature thermocompression bonding process. Fig. 1.11 (a) shows the proposed fabrication of the NW-ACF material with a template synthesis method and (b) the concept of TSV/NW-ACF bonding for potential 3D integration applications. In this work, the single metal is deposited in the nano-porous template to form the NW-ACF and the NW-ACF bonding between the fine-pitch Si test die is demonstrated to prove the concept.

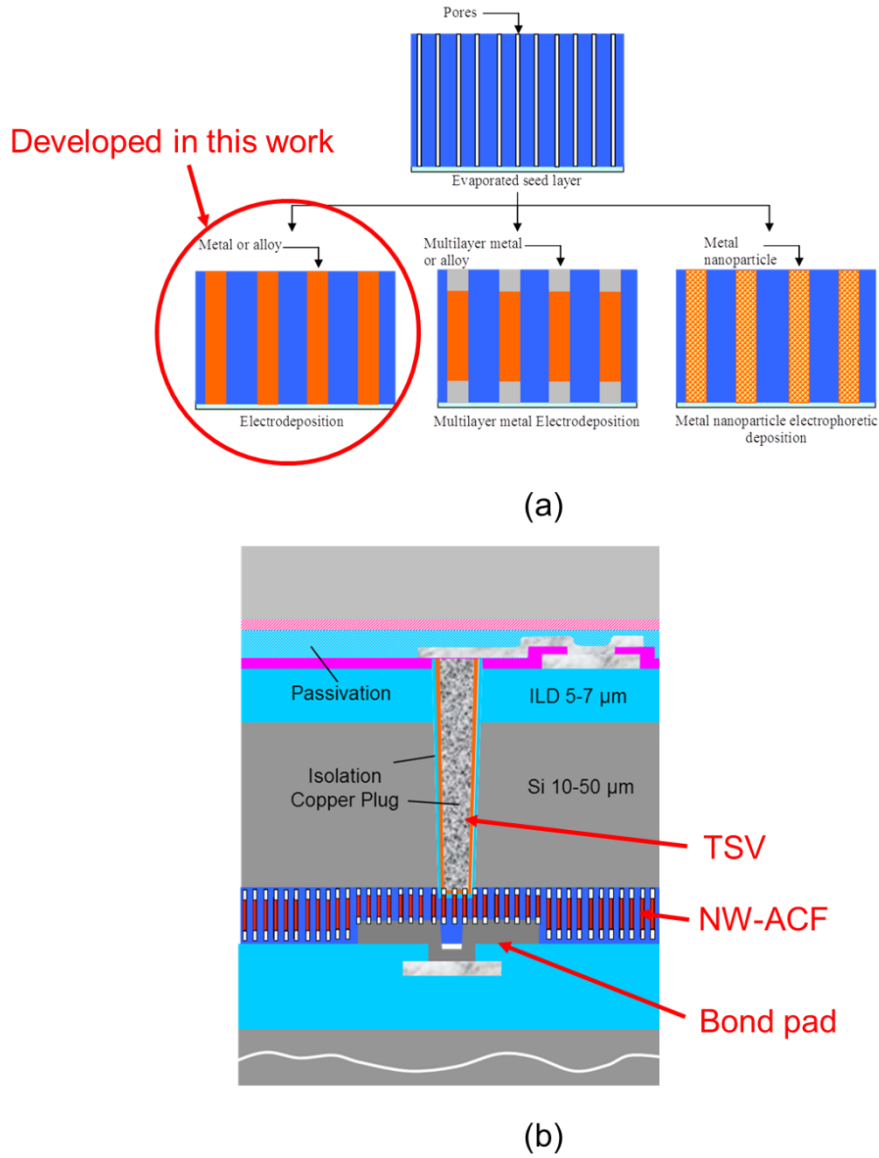


Figure 1.11 Schematics showing (a) proposed fabrication of the NW-ACF material and (b) the potential application of the NW-ACF for 3D TSV integration.

To fulfil the objectives, the main tasks of this research work include:

- i. Fabrication of NW-ACF using Cu electrochemical deposition (ECD) technique through nanoporous templates; structural and thermal characterization of the NW-ACF material [60].
- ii. Bonding experiment and electrical/mechanical characterization of the NW-ACF interconnects with a Cu-In metallized die [60].
- iii. Test chip design and test wafer fabrication for the evaluation of NW-ACF for fine-pitch applications [63].

- iv. Characterization of the fine-pitch capability of the NW-ACF with the designed test chips [61, 64].
- v. Understand the effect of bonding parameters on the NW-ACF interconnect properties [64, 65].
- vi. A feasibility study of the NW-ACF bonding with the Au bumpless pads and a comparative study with the particle-based ACF [62].
- vii. High frequency characterization of the NW-ACF interconnects and a comparative study with the solder-bump interconnects.
- viii. Thermal characterization of the NW-ACF interconnects using thermal impedance test and a comparative study with the particle-based ACF.
- ix. Reliability assessment of the NW-ACF interconnects and failure analysis of the electrically failed samples.

1.4 Thesis Outline

This thesis is organized in six chapters, and the general content of each chapter can be summarized as below:

In Chapter 1, electronics packaging evolution and the key technologies in 3D integration are introduced. A comparison is made between the existing and potential interconnection technologies for 3D integration and the research objectives are elucidated.

In Chapter 2, a literature review is performed on the various ACA/ACF technologies, including particle dispersed ACAs, vertical wire ACFs and nanowire ACF, with emphasis on ACA/ACF material constituents, processing, conduction principles, failure mechanisms and applications.

The experiments associated with NW-ACF fabrication, structural and thermal characterizations of the NW-ACF material are described in Chapter 3. The structural and thermal properties of the fabricated NW-ACF material are studied using scanning electron microscope (SEM) analysis and various thermal characterization techniques including differential scanning calorimetry (DSC), thermogravimetry analyser (TGA) and dynamic mechanical analyser (DMA). The bonding and electrical properties of the NW-ACF are investigated using unpatterned In finished Ti/Cu/Si die. An interconnection resistance model is given and the major contributions to the total resistance are discussed. The contact mechanism of the nanowires to the bonding surface is studied by SEM, scanning transmission

electron microscope (STEM), energy-dispersive X-ray spectroscopy (EDS) and X-ray powder diffraction (XRD) analysis. The bonding structure is studied by bonding interface analysis and the mechanical strengths of the NW-ACF interconnects are obtained by die shear test.

From the fine-pitch application perspective, test chip modules are designed containing daisy chain, 4-point and insulation test structures with four pad /pitch variations. In Chapter 4, the test chip structure and the test wafer fabrication using 4-mask lithography fabrication process are described. Three NW-ACFs based on different templates are bonded with fine-pitch test die with Cu-In bond pads and the template related open/short failures are screened out. The effects of bonding parameters are studied and the bonding mechanism under the optimized bonding temperature is explained. The mechanical behaviours of the nanowire bending under a varying bonding force are understood. Meanwhile, the feasibility study of the NW-ACF interconnects bonding with Au bumpless pads is carried out. The electrical results are compared with a commercial particle-based ACF. High frequency performance of the NW-ACF interconnects is evaluated based on S-parameter measurement and the RLCG parameters are extracted and compared to the results of solder-bump interconnects. To compare the thermal performance of the NW-ACF to the particle-based ACF, the thermal impedance measurement is performed and the results are discussed with the thermal impedance model.

As a potential reliable interconnect solution, the mechanical and reliability properties of the NW-ACF interconnects are critical for future material development and applications. In chapter 5, the mechanical strength and the fracture mode of the NW-ACF interconnects are studied by conducting die shear test and fracture surface analysis. The reliability assessments of the NW-ACF interconnects are carried out with thermal shock test and high temperature and humidity test. The electrical failures and mechanical degradation under the respective environmental acceleration conditions are studied. As compared to a commercial particle-based ACF, the failure mechanism associated with the polymer matrix system of the current NW-ACF material is addressed.

In Chapter 6, a summary of the current work presented in the thesis and its novelty as well as suggestions for future works that will be necessary to develop and apply the NW-ACF for D2D and 3D applications are provided.

Chapter 2 Development Trends of Anisotropic Conductive Adhesive (ACA) Technologies

2.1 Introduction

Anisotropic conductive adhesives/films (ACAs/ACFs) are composite materials comprised of electrically conductive fillers in a non-conductive adhesive base. There are mainly two types of the ACAs [66]: 1) a homogeneous mixture of conductive fillers and the adhesive, and 2) the conductive fillers distributed in an orderly fashion in the adhesive base. The commercial particle dispersed ACAs belong to the first type of ACAs and are the most developed ACA technology with wide applications for chip-to-substrate packaging particularly in the display industry. As a mature material and technology, there are extensive studies towards material constituents, fabrication methods, bonding processes, conduction mechanism and applications. The advantages of particle dispersed ACAs are: fine-pitch capability, lower processing temperature, less environmental impact, reduced cost and decreased intermetallic reliability concerns. However, the limitations of these materials are that the applicable pad/pitch size may not fulfill the ultra-fine pitch ($< 50\ \mu\text{m}$) requirements such as for 3D interconnection and also the open/short failures could occur due to the unpredictable number of trapped particles in the interconnection and the occurrence of particle agglomeration in the small pad gap. Vertical wire ACFs belong to the second type of ACAs and they have been developed in the patterned adhesive matrix as a Z-axis interconnect solution for even finer pitch size applications. Compared to particle-dispersed ACAs, the vertical-wire ACFs have a higher density of conductors in the interconnection and also eliminate the particle agglomeration problem. However, the vertical wires with diameters smaller than $< 1\ \mu\text{m}$ can no longer be fabricated by lithographic patterning. To obtain nano-size conductors for ultra-fine pitch interconnection, nanowire ACF based on template synthesis method has been proposed and developed. The unique fabrication techniques and early researches on nanowires properties and applications will be introduced.

2.2 Commercial Particle Dispersed ACAs

Conventional particle dispersed ACAs are composed of conductive particles with a volume fraction of 5-10% and the adhesive matrix in which the particles are uniformly dispersed [67-69]. The conductive particles are so dispersed that they do not cause any direct metallic contact before pressure is applied. The Z-axis electrical conduction is only formed after the particles are pressed to contact between the electrodes of the chips and/or substrates. Meanwhile, the X-Y insulation is maintained due to the fact that the particles are still isolated from each other by the insulating polymer material. The mechanical interconnection is formed by hardening the thermosetting polymer or solidifying the thermoplastic polymer after a heating process.

2.2.1 Types of Conductive Particles

2.2.1.1 Solid Metal Particles

There are many inventions and patents that propose new and versatile conductive fillers to be used in ACA materials. In 1978, Fujita et al. [70] patented the solid metal particles which are composed of reduced Ag powder, Au powder, Pd/Ag powder, Ni powder, and In powder, with a volume fraction of $< 30\%$ and a diameter equal to the thickness of the adhesive film. They also claimed that by incorporating insulating particles with a smaller diameter that the non-conductivity in the lateral direction is improved. Solid fibrils type fillers were patented by Shin-Etsu Polymer Co. Ltd in 1986 [71]. The fibrils have a length of $\leq 300\ \mu\text{m}$ and an aspect ratio of ≥ 3 . These are dispersed in the film-like adhesive base with a volume fraction of 2-20%. The fibrils are dispersed in the orientation that is being substantially parallel to the surface of the film adhesive, which requires two or more layers of fibrils to be stacked to form the vertical conduction paths. Examples of the conductive fibrils are metallic wires and whiskers such as aluminium, copper and tungsten.

2.2.1.2 Metal-coated Polymer-core Particles

The conductive particles comprising polymeric core material coated with a thin metal layer was patented by Hitachi Company in 1988 [72]. The polymeric core material can be polystyrene, epoxy, acrylonitrile-butadiene rubber, polyimide or polyester. The range of the average particle size is preferably from 0.5 to $300\ \mu\text{m}$. Either too small ($< 0.5\ \mu\text{m}$) or too big

(> 300 μm) particle size can easily result in electrical open or short. Because of the elastic polymeric core material used, these particles are easy to deform and the contact area between particles or between a particle and a conductor surface is greatly increased, as compared to the point contact formed by solid metal particles that arise because of the material rigidity. This core material has an electrically conductive thin metallic or metal layer coated on almost its whole surface with a thickness of 1/5 to 1/1000 of the particle size (diameter). The metal coating could be Au, Ag, Ni, Ni/Au, Cu/Ni and many others. The techniques used to coat the thin metal layer onto the spherical polymeric particles include vapor deposition, sputtering, plating, etc. Among these, the electroless plating method has been experimented with to make metal layer such as Ni, Cu, Au, Ni/Au and Ni/Cu on the polymeric core material. Meanwhile, the adhesiveness between the metallic thin layer and the polymeric core material can be improved by surface activating methods, such as plasma treatment, using coupling agents and chelating agents.

2.2.1.3 Conductive Particles with Insulating layer

The other type of the spherical conductive particles is composed of either a solid metal sphere or metal coated polymer core spheres with an insulating layer on the surface, which was patented by the Casio company in 1993 [73]. The insulating layer consists of a material which is broken under heat and pressure when parts of the layer are brought into contact with the connection surfaces; while the insulating layer of the particles in the planar direction are not broken and remain as they were. The advantage of using an additional insulating layer on the particles is that the electrical insulation in the planar direction is not compromised by increasing the filler concentration. The insulating layer could be a resin material with a low melting temperature, or non-conductive micro-powders which couple with the surface of the conductive particles. Fig. 2.1 illustrates the structures of the three types of spherical conductive particles which are solid metal particle, metal-coated polymer-core particle and the conductive particles with an insulating layer.

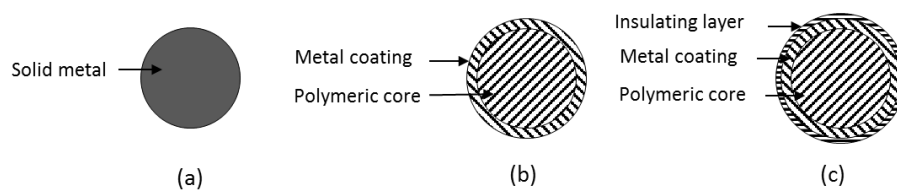


Figure 2.1 Schematics of the three types of sphere particles in ACAs, (a) solid metal particle, (b) metal-coated polymer-core particle and (c) the conductive particle with an insulating layer.

2.2.2 Polymer Matrixes

2.2.2.1 Materials and Formulation

Both thermosetting and thermoplastic polymer can be used as the adhesive matrix. Epoxy, cyanate ester, silicone, polyurethane, etc. are widely used thermosets and phenolic epoxy, maleimide, acrylic, preimidized polyimide, etc. are the commonly used thermoplastics in ACAs [69]. The thermoplastics have the advantage of the relative ease for rework or repair of interconnection due to the reversible flow characteristics above the glass transition point. However, this may result in the “spring-back” phenomenon after bonding or the increased resistance after thermal shock due to the creep characteristic of thermoplastics [74]. In contrast, the thermosets have better mechanical strength, good chemical and corrosion resistance and elevated temperature performance due to the three-dimensional cross-linked structure formed upon curing. These are normally chosen as the adhesive matrix for conventional ACAs [53, 75]. There are basically three ways to formulate an ACA blending [76]:

- i) Simple mixing of the constituents (conductive particles, adhesive resin and curing agent), degassing and sheeting out on a substrate to the desired thickness;
- ii) Random but controlled sprinkling of particles on the surface of the sheet-out, uncured polymer matrix layer of desired thickness and allowing the particles to sink into the polymer by gravity;
- iii) Mixing of the particles in a polymer liquid (diluted or solvent-based adhesives), sheeting out into a thin layer and obtaining the desired thickness by subsequent evaporation of the solvent or water.

ACAs are normally prepared as a film or sheet form, which are called as ACFs. Meanwhile, a protective carrier film such as silica or plastic paper is usually attached to one side of the film due to the tackiness of the adhesive and therefore the film can be rolled up in

a reel tape for mass production purposes. Fig. 2.2 illustrates the cross-sectional structure of the ACF, where the film thickness is about 2-3 times the diameter of the conductive particles. Nevertheless, the film thickness may vary from one to several times the diameter of the conductive particles, depending on the size and density of the particles inside the film.

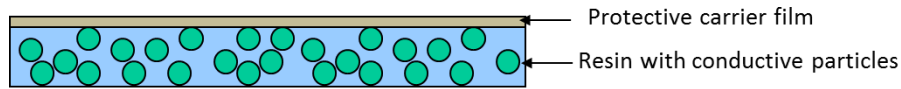


Figure 2.2 The cross-sectional structure of the conventional ACF with the conductive particles dispersed in the resin and a protective carrier film on side of the film.

2.2.2.2 Magnetic Particle Dispersed ACAs

One of the challenging issues in the formation of particle-based ACAs is the uniform dispersion of the particles in the polymer matrix, because this determines the uniformity of conductivity of the ACAs. The common methods for particle dispersion include the physical approaches such as sonication to uniformly distribute particles and chemical approaches such as the use of surfactants [77]. To produce a uniform, two-dimensional particle distribution, AT&T lab invented the magnetic particle (iron, nickel, cobalt and their alloys, or a ferrite material) dispersed ACF, which are prepared under a magnetic field before and during polymer hardening. Fig. 2.4 [78] (a) shows the random particle distribution without applying a magnetic field and (b) the effect of the magnetic field to result in a more uniform distribution of the particles. Compared to the randomly distributed particles, the magnetic distributed particles in such ACAs reduce the tendency for electrical shorts and pad-to-pad variations in contact resistance. However, the limitation of this technology is that a ferromagnetic material has to be used to form the particles.

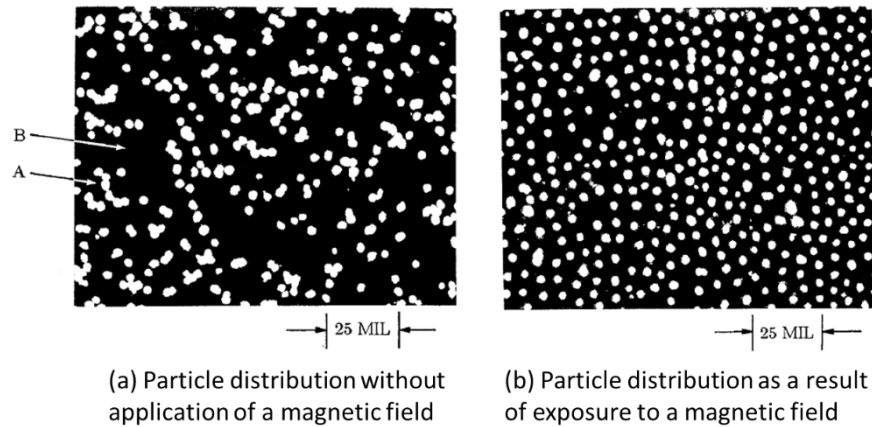


Figure 2.3 The surface view of the particle distribution in an ACF of (a) random particle distribution and (b) more uniform distribution of the ferromagnetic particles when prepared under magnetic field [78].

2.2.2.3 Double-layer ACFs

The concept of one or more layer ACAs was first proposed in the patent by AMP Incorporated in 1987 [79]. This was followed by the development of the double-layer ACFs by Hitachi [54]. The double-layer ACF comprises a two layer system with one layer of resin containing conductive particles as in the normal ACF and the second resin layer without conductive particles, i.e. a non-conductive film (NCF) layer, as shown in Fig. 2.4. This double layer design reduces particle density in the X-Y spacing of the interconnection pads and provides more adhesive volume that can help to trap more particles between the pads [53]. By adjusting the top layer thickness to have a thicker NCF layer and a thinner ACF layer, the number of trapped conductive particles can be enhanced [80]. Comparing with the single layer ACF, the double-layer ACF can result in a better electrical insulation stability, improved thermo-mechanical properties and better reliability [81].

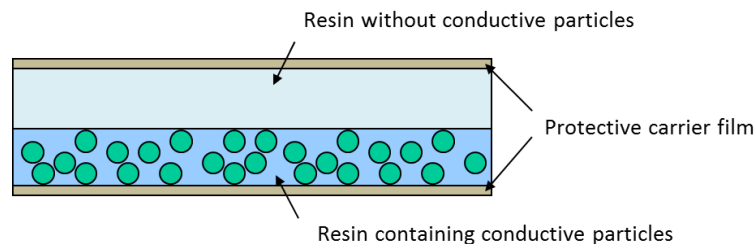


Figure 2.4 Schematics showing the material composition of the double-layer ACF.

2.2.3 Formation of ACF Interconnects

A common technique to form ACF interconnects between chip and substrate is to use flip-chip bonding with heat and pressure. Fig. 2.5 shows the process flow of applying an ACF to connect between the chip pads and the substrate pads. Firstly, the ACF is laminated onto the substrate side with a relatively low temperature and force. The purpose of this process is to tack the adhesive to the substrate in order to remove the protective carrier film. The typical pre-bonding temperature is 80-100 °C, with a low pressure range of 0.5-1 MPa for 1-7 s for thermosetting adhesives [53, 75, 82]. Then, the top chip is aligned with the bottom substrate in a flipped manner and brought down by the tool head. During final bonding, the heat and pressure is simultaneously applied, during which the adhesive flow around the pads and the thickness of the adhesive layer is reduced to let the conductive particles to make contact with both connection surfaces. At the same time, the thermosetting adhesive is thermally cured and hardened and the mobility of the particles is constrained. For the majority of thermosetting polymer based ACFs, the typical bonding temperature is 150-230 °C for 5-20 s with a pressure range of 30-110 MPa [82-84]. Finally, the bonded module is cooled down to room temperature and the bonding force is removed. The mechanical strength of the interconnects can be maintained by the adhesion force due to polymer curing and the compressive force due to thermal shrinkage of the polymer.

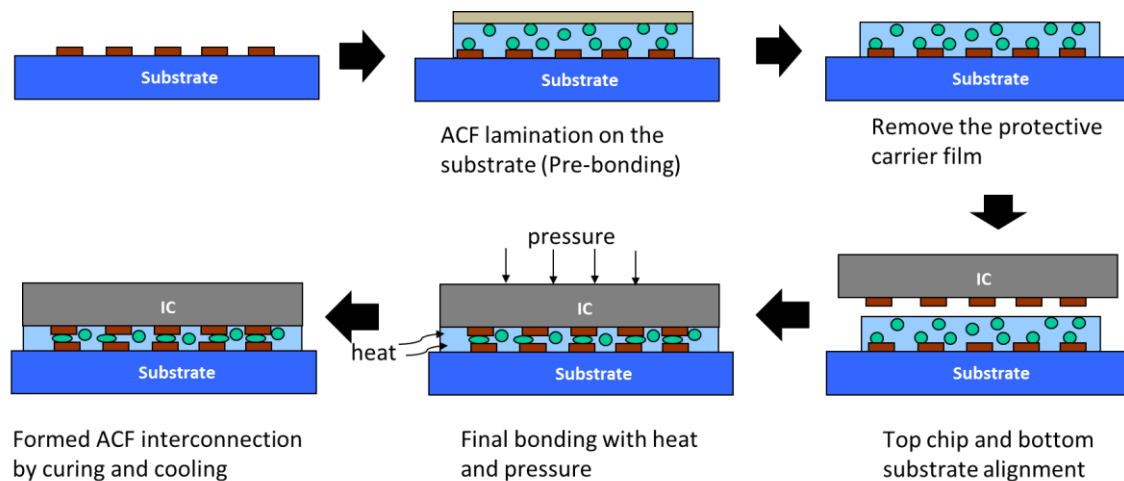


Figure 2.5 The process flow of applying an ACF material for chip to substrate interconnection.

2.2.3.1 Effect of Bonding Temperature and Time (Thermosetting Polymer)

For most particle dispersed ACAs, the adhesive matrix consists of a thermosetting epoxy, which can be cured under a low temperature. There are many publications that describe the effects of bonding temperature on electrical and mechanical performance of thermosetting polymer based ACA joints [53, 54, 75, 83-88]. For example, Uddin et al. [85] defined the curing degree of the thermosetting adhesive in terms of bonding temperature and its relationship to the peel strength and the contact resistance of the ACF applied for the chip-on-flex package. They found that the curing degree of ACF increased with increasing curing temperature due to the initiation and acceleration of the cross-linking reaction by providing higher active energy to the polymer chain. At a higher bonding temperature, the contact resistance was also decreased, which can be due to the short curing time to prevent most of the conductive particles squeezed out of the pads during bonding. Meanwhile, the adhesion strength increases at a higher curing degree due to stronger chemical bonding between the adhesive and adherent. Paik et al. [86] studied the curing characteristics of a thermosetting ACF in terms of curing temperature and isothermal curing time by DSC analysis, as shown in Fig. 2.6. The degree of cure increases with increased temperature and/or time. They found that when the degree of cure is more than 90%, the electrically and mechanically stable ACF interconnects can be established.

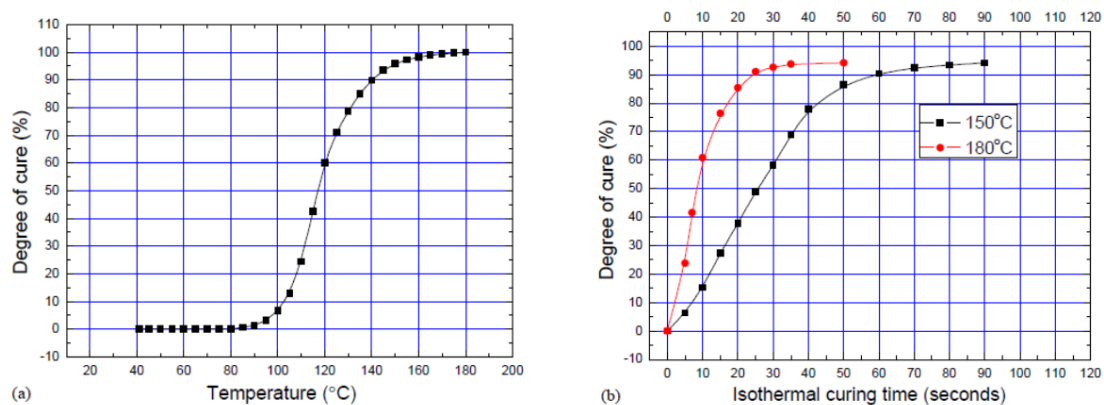


Figure 2.6 Degree of cure in terms of (a) temperature and (b) isothermal curing time [84].

During the ACF bonding, the thermo-mechanical and rheological properties as a function of temperature of the adhesive will also influence the quality of the formed interconnections. Paik et al. [81] designed the viscosity-controlled ACFs with a double-layer structure, where the NCF layer has a low viscosity and flows readily to fill the gaps between the bumps and

the ACF layer has a high viscosity and can trap more conductive particles under the bump. Paik also studied the thermo-mechanical properties of the cured ACF materials under thermo-mechanical analysis (TMA) and dynamic mechanical analysis (DMA) and concluded that the ACFs with a higher glass transition point (T_g), a low coefficient of thermal expansion (CTE) and a higher storage modulus at elevated temperature will result in a better reliability under the thermal and humidity environmental testing for chip-to- substrate applications [87].

2.2.3.2 Effect of Bonding Pressure

The development of electrical conduction in the particle dispersed ACA/ACF has mainly been due to the elastic/plastic deformation of conductive particles on the connecting surfaces under contact pressure and maintained by tensile stress in the adhesive [89]. From the material side, the conductive particles should have a modulus of elasticity (in tension) of almost the same value or higher than that of the adhesive component, so that the particles are able to approach the conductors when the external load is applied [72]. For both rigid and hard particles, the larger the bonding force, the lower the contact resistance [67]. The relation between contact/bonding force and electrical resistance is generally illustrated in Fig. 2.7 [89].

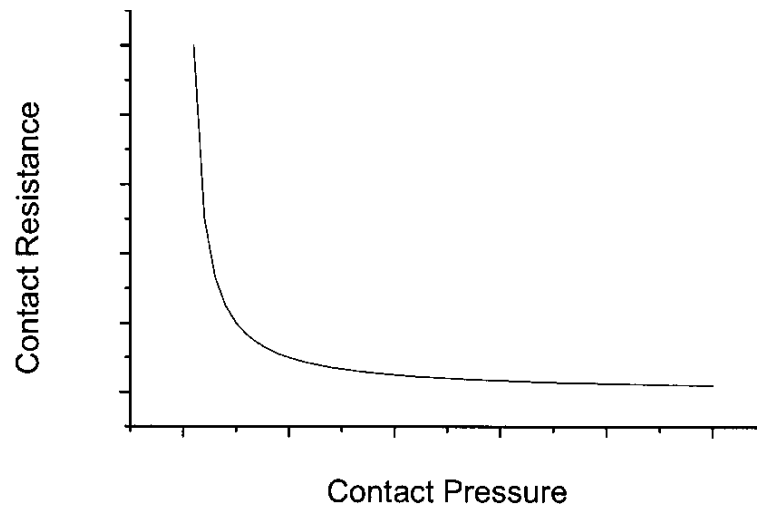


Figure 2.7 Contact pressure versus contact resistance [87].

Kwon et al. [90] related the effect of bonding force to the deformation degree of the conductive particles with quantitative analysis both theoretically and experimentally. They conducted nano-indentation experiments for a single conductive particle and obtained the compressive load versus deformation curves for two kinds of conductive particle with

different polymer core materials. They explained that the nonlinearity of the force-deformation relationship was due to the nonlinear change of the contact area during the particle compression and the viscoelastic properties of the polymeric core material. By carrying out an actual bonding experiment with 120-bumped chip-on-glass test chips, they verified the validity of the predicted values of the force-deformation relationship by postulating that the total force required to compress particles was equal to the compressive force required for a single particle multiplied by the number of the particles under compression. They also calculated the theoretical values of the contact area in terms of the elastic and plastic deformation and found the particles with the soft core material were under elastic-plastic deformation above a certain deformation degree. The plastic deformation showed a higher rate of contact area increment than the elastic deformation, and this helped to obtain a lower contact resistance under the same bonding force. However, if the bonding force was too high, the outer layer of the particles became broken and the contact resistance increased due to discontinuities of the metallic layer. Chan et al. [91] also observed this phenomenon for the polymer core particle based ACF and concluded that the optimized dimension change of the conductive particles should be about 25-30% increase in the X-direction (horizontally) and about 40-50% reduction in the Y-direction (vertically). In terms of adhesion strength, the bonding strength was reported to increase very slightly as the bonding pressure increased. A proper pressure should be applied to assure intimate intermolecular contact between adhesive and adherent so that Van Der Waals interaction, electrostatic adsorption and other bonds at the interfaces can take place [83].

2.2.3.3 Contact Resistance Theory

Electrical conduction through particle based ACAs is established by elastic or plastic deformation of conductive particles under pressure. Yim et al. [92] introduced an analytical model for calculating the contact resistance of the deformed particles between the conductive surfaces considering the elastic deformation of the particles and including the intrinsic resistance of the particle and the constriction resistance as:

$$R_c = \frac{0.69 (\rho_1 + \rho_2) \left(\frac{NE^*}{FD} \right)^{\frac{1}{3}} + \frac{\rho_1}{0.524D}}{N} \quad (2.1)$$

$$\frac{1}{E^*} = \frac{1-\nu_p^2}{E_p} + \frac{1-\nu_s^2}{E_s} \quad (2.2)$$

where R_c is the contact resistance, ρ_1 and ρ_2 are the intrinsic resistivity of metal conductive particles and surface, N is the number of conduction paths, E is elastic modulus, ν is Poisson's ratio, and the subscripts p and s represent the particle and surface, respectively. F is the contact force and D is the diameter of particle. This analytical model shows as predicted that the contact resistance decreases with increasing number of conductive particles, particle size and intrinsic conductivity. The contact resistance for a situation that has five conductive particles between two pads is in the range of 0.01-0.02 Ω .

Chin et al [93] compared the above model with experimental data and found that large discrepancies exist, where they stressed the other contributing factors to the contact resistance such as elastic recovery, residue force [94], the edge effects and interactions between multiple particles [95]. From their study of the effect of elastic recovery, they found when the contact force is removed, the contact resistance can increase sharply from 0.02 to 0.1 Ω [94]. However, by tuning the parameters such as modulus of elasticity, the adhesive strength of the cured resin and the optimal range of bonding force, this trend of increase in the contact resistance can be prevented. From the study of the multiple particle model and by considering edge effects and the interactions between particles, the increments of contact resistance were smaller than the effect of elastic recovery when assuming that the particle was more conductive than the conductive track. Generally, the results showed that a uniform distribution of the particles leads to smaller values of contact resistance [95].

Jackson et al. [96] studied contact resistance by considering tunnelling resistance and particle flattening. They claimed that due to the roughness on the surface and the viscous nature of the epoxy, a thin film is likely to remain between the conductive particle and the surface. Based on quantum theory, a finite probability exists for the electrons to tunnel through this barrier, depending on the size and shape of the barrier. They firstly deduced the formulas for the critical contact area and critical load based on von Mises yield criterion when the deformation is small and applied with Hertizian solution (elastic deformation theory), and when the deformation is of the elasto-plastic contact type. The tunnelling resistance was then deduced in two scenarios:

- i. When the applied voltage is nearly zero, the tunnelling resistance was deduced as a function of contact area, the thickness and the dielectric constant of a thin insulating film and the energy height above the Fermi level to the conductive surfaces.

- ii. When the applied voltage is above zero, the tunnel resistance shows non-ohmic behaviour and decreases with increasing voltage.

By assuming the insulating thickness = 5.96 \AA , the energy height above Fermi level $\phi_0 = 4.75 \text{ eV}$, the dielectric constant $K = 4.2$ and applied current of 0.1 A , the theoretical values of contact resistance are of the same magnitude as the experimental values. The important parameters that influence the tunnelling resistance are the applied voltage and the insulation layer thickness. The tunnelling resistance was found to decrease by several orders of magnitude when the voltage was increased from 0 V to above $\sim 1 \text{ V}$. Whereas, having one order thicker of insulation layer, the tunnelling resistance can increase by eight orders. It should be noted that the trapped insulation thickness is mainly dependent on the rheological property of the adhesive.

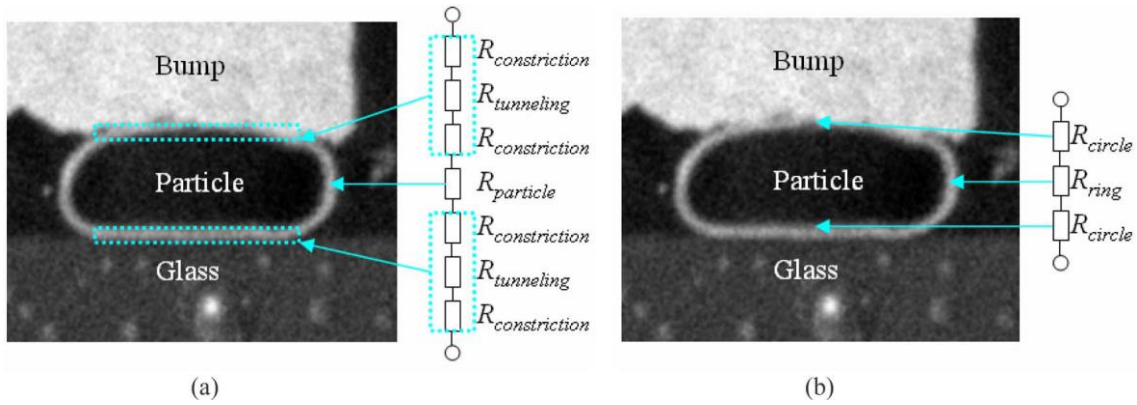


Figure 2.8 Components of (a) total contact resistance and (b) particle resistance in a single conductive particle [95].

In addition to contact resistance, Xie et al. [97] studied the intrinsic resistance of nickel-coated particles with and without cracks. By applying a cohesive element modelling approach to simulate crack initiation and propagation at a certain bonding pressure, they deduced the traction evolution as a function of separation and found that the crack in the particle initiates at the central area and is propagated to the polar contact area. For both cases with and without cracks, the particle resistance comprises two circle resistance, corresponding to the two circular planes at the top and bottom of the particle that are in contact with the conductive surfaces, and one ring resistance when the metal coating is intact, or the crack resistance when the coating is broken. Fig 2.8 [97] illustrates the components of total contact resistance (a) consisting of two constriction resistance ($R_{constriction}$) and one tunnelling resistance

($R_{\text{tunnelling}}$) on both the particle to bump and particle to glass interfaces, and particle resistance (b) consisting of two circle resistance (R_{circle}) and one ring resistance (R_{ring}) for a deformed particle between the electrodes. Based on these analytical models, the particle resistance was calculated to be in the range of 0.3 to 0.8 Ω in terms of particle deformation degrees and the effect of particle cracks can add up to 30% increment of such resistance.

2.2.3.4 Failure Mechanisms

Failures in ACF interconnection have been reported due to factors including oxidation of conductive particles, initial misalignment due to co-planarity issues, thermal stress due to CTE mismatch, post assembly residual compressive stresses, polymer expansion due to moisture absorption and degradation of the polymer at high temperature [98]. Unlike solder based interconnects like C4 bumps, the adhesive does not generate surface tension forces that drive the self-alignment process and allows misplaced chips to be pulled into the correct position. Process-related failures such as misalignment and co-planarity can impair the bonding yield by causing open/short failures. Fan et al. [99] studied the probability of electrical open and shorting as a function of pad misalignment. With the pad size of 2000 μm^2 , the open probability for ACF containing 3.5% volume fraction and four 1.5 μm radius spherical particles would be $> 10^{-4}$ when the pad misalignment is $> 4 \mu\text{m}$. The shorting probability also increases rapidly with any increase in misalignment. On the other hand, Chiu et al. [58] studied the short-circuiting effects due to the degree of cure of the ACF and found that when the degree of cure is below 50%, there are ~25% failures due to short-circuiting at pad space of 15 μm . The movement of the particles in an insufficiently cured polymer is considered to be the main cause of this phenomenon. Such failures were also found with the ACF containing conductive particles with an insulating layer and were explained by the wear-out mechanism of the insulation layer due to friction between particles during movement. Dou et al. [100] studied the effect of co-planarity on ACA joints by deliberately rotating the angle of the bonding tool head. They found that the contact resistance is much higher in the less compressed side than in the highly compressed side due to the bad co-planarity.

Environmental factors also influence the reliability of ACF interconnection in a way different from the soldered connections, where the formation of intermetallic compounds and coarsening of grains are the main failure mechanism for solder joints. For the ACF interconnects, two main failure mechanism are recognized as [66]:

- i) the formation of insulating oxide film on either the contact areas or conductive particle surfaces,
- ii) the loss of mechanical contact between the conductive elements which is either due to a loss of adherence or relaxation of the compressive force.

When the conductive adhesive interconnects are subjected to cyclical thermal stress, interfacial delamination and fracture can occur due to the thermo-mechanical stress caused by CTE mismatch. Furthermore, variation in elastic modulus and interfacial adhesion strength all directly influence the electrical performance of the interconnects [101-103]. Humidity is the other environmental factor which can impair an ACA interconnect. Under a humid environment, the ACA matrix absorbs water, which weakens the mechanical properties of the polymer [104, 105]. The moisture absorption also causes swelling and hygroscopic stresses in the bonding structure, and this can lead to the permanent failure of interconnects [106, 107]. Meanwhile, electrochemical corrosion is reported to be the main cause of interfacial delamination and contact resistance shift, when the contacting metals possess different electrochemical potentials and non-noble metals are corroded to form insulating metal oxides at the interface [108].

2.2.4 Applications and Recent Developments

Particle dispersed ACAs have been used as packaging technologies in flat panel displays for more than thirty years [54, 55, 109]. The main technologies using ACAs include chip-on-flex [53, 84, 85, 110], chip-on-glass [81, 82, 111] and chip-on-board [112-115], flex-on-board/glass [88, 116] and chip-on-chip [87]. The main advantages of particle dispersed ACAs are low process temperature and fine pitch capability. Furthermore, this technology eliminates the need for underfill as compared to solder technology; hence, it greatly decreases the packaging cost and simplifies the process. It also provides an acceptable joint resistance and relative ease of rework/repair [109]. Due to the ability of compliance under bending, low bonding temperature and better flexibility than solder based interconnection, ACFs also show great potential for use in flexible electronics, such as chip-on-flex (COF) or chip-in-flex (CIF) packages. With the application of ACF, the accumulated plastic strains in the package can be effectively lowered and the bending reliability is enhanced [117]. Micro-particle based ACAs are also proposed for advanced packaging applications, such as wafer-level packages and 3D IC integration. ACAs composed of benzocyclobutene (BCB) and conductive particles can be spin or spray coated onto full wafers and bonded at wafer level to realize both electrical and

mechanical connections [57]. Modified ACA solutions with high fluidity can be directly coated on a wafer with a blade coating method and individually bonded to the substrates [118]. These new approaches greatly reduce the process steps and time, as compared to the film based ACF technologies. Furthermore, the BCB type ACA has also been proposed for 3D chip stacking to form interconnects between TSV and MEMS die [119].

With the trend of I/O shrinkage in the IC industry, conventional ACF faces challenges to accommodate the reduced pad and pitch sizes. Two problems are mainly reported for these conditions: the electrical open due to the reduced number of particles that can be trapped between the pads and electrical shorts due to a higher chance of particle agglomeration in the pad gaps. New types of ACAs have been developed to solve these problems. A nanofiber incorporated particle-based ACF was developed in order to suppress conductive particle movement during resin flow and to improve the fine-pitch capability [120-122]. For spherical particles, the particle size cannot be smaller than 2-3 microns to achieve an adequate bondline thickness. Therefore, magnetically aligned anisotropic conductive adhesive with a columnar structure is considered as a possible solution for further scaling of the initial particle size [123]. To improve the electrical properties such as power handling capability and reliability, flux function added solder ACFs have been proposed to form metallurgic connections to the pads [124, 125]. By reducing the particle size to nanometer size, nano-silver (Ag) filled anisotropic conductive adhesive [126] has been developed with low sintering temperature ($< 200\text{ }^{\circ}\text{C}$). By incorporating an organic self-assembly monolayer in such nano-Ag ACA, the electrical resistance can be further reduced with a further advantage of a high current carrying ability.

2.3 Vertical Wire ACFs

The other type of the ACFs is based on conductive fillers that are distributed in an orderly fashion in the adhesive base. Its fabrication requires a more complicated manufacturing process, by firstly forming the ordered structure in the polymer base material and filling the specific area of the structure with the conductive materials. One of the ordered structures in such ACFs is the vertical through-holes created in the polymer matrix. By inserting metal or conductive materials into the holes, an inherently anisotropic conductive structure can be created. With this novel structure, a lower pitch and pad area as well as a low electrical resistance can be achieved with less chance of lateral shorting [127, 128].

2.3.1 Concept and Early Patents

The early example of vertical wire ACF was patented by Takayama et al. [129] in 1992, where the ACF with through-holes filled with metallic material was proposed. The through-holes were made by piercing the film in the thickness direction, while a metallic substance that fills the holes serves as the conduction paths. The diameter of through-holes was generally from 15-100 μm and the film thickness was 5-200 μm . The insulation film material can be thermosetting and thermoplastic resins and the metallic substance can be various metals such as gold, silver, copper, tin, lead, nickel, cobalt, indium and various alloys of these metals. The through-holes can be formed by mechanical process, such as punching, dry etching using a laser or plasma beam and wet chemical etching using chemical or solvents through a mask or photoresist patterning. The holes can be filled by various techniques, such as sputtering, vacuum evaporation and plating. However, because of the large hole diameter, it should have a rivet-like shape so that one end of the hole can form a bump-like projection to prevent the metals from falling out later. Hotta et al. published the characterization and applications of such novel anisotropic conductive film for the connection between bump-less chips and fine-pitch printed circuit boards [130, 131]. The minimum pitch of the conductors in this ACF was 25 μm , and was composed of 18 μm diameter Cu pillars of 70 μm length. The micro-size Cu pillar conductors can stand vertically to electrically conduct between the chip and board with 100 μm interconnection pitch and resulted in a contact resistance of 20 m Ω . The interconnections also showed a stable contact resistance and good insulation properties under high temperature and humidity environments. Due to the large ratio of metal conductor in this ACF, the die shear strength were compromised in these interconnects due to the low ratio of adhesive.

Ishibashi et al. [132] reported the fabrication process for the ACF with arrayed Ni bumps using photoresist patterning. The arrayed Ni bumps were obtained by Ni electroplating in the triangular arranged open holes of the patterned photoresist on a substrate. The holes had a diameter of 12 μm at 20 or 40 μm spacing and typical bump heights were from 9-20 μm . The ACF as prepared by laminating a 30 μm thick epoxy adhesive film onto the metal bumps followed by a peeling off process. The difficulty lies in the transfer process, which requires an appropriate pressure during lamination to stop the adhesive from contacting the substrate surface and preventing the metal structure from deformation.

2.3.2 Z-axis ACF

A research group in Leti (Souriau et al.) developed the so-called Z-axis ACF with pyramidal tips for the single bumpless chip connection and wafer level interconnection [127, 133, 134]. The conductors were composed of 10 μm long Ni inserts with 10 μm diameter and 30 μm pitch by photolithographic method. With the gluing and thermocompression process, the Z-axis ACF is reported to achieve a contact resistance of 6 m Ω with 50 \times 50 μm^2 pad and a stable contact under thermal cycling. The challenges for this technology were reported to be the damage caused by the shape tips of the Ni inserting into the passivation layer on chip and the rapidly increased contact resistance due to the effect of humidity exposure.

2.3.3 Mechanical Models

Diop et al. [128] proposed ACF based on vertical fibers for non-permanent bonding in a wafer-level packaging application. The ACF under evaluation was from Btechcorp with high density cylindrical nickel fibers with the pitch and diameter of 11 and 8 μm , respectively embedded in a polyamide matrix of 230 μm thickness. They studied the elastic-plastic deformation mode of the ACF and found that the plastic deformation is the dominant mode during micro-indentation test. Meanwhile, the hardness and modulus are also decreased with the increased indentation depth due to the manifesting influence of the matrix. Two buckling modes of the fiber composite, extension and shear mode to simulate such vertical structures under compression are illustrated in Fig. 2.9 [128] and the compressive strengths under the respective mode can be expressed as:

$$(\sigma_{fcr})_{extension} = 2 \sqrt{\frac{V_f E_m E_f}{3(1-V_f)}} \quad (2.3)$$

$$(\sigma_{fcr})_{shear} = \frac{G_m}{V_f(1-V_f)} \quad (2.4)$$

where V_f is the volumetric factor of the fiber, E_m and E_f are the Young's modulus of the matrix and fiber, respectively and G_m is the matrix shear modulus. Due to the high volume of the high modulus vertical fibers in such an ACF, the electrical contact can be directly made by compressing the film. The contact mechanism was studied by increasing the compression length and it was found that a plastic deformation occurred in the solder bump while the Ni

fibers in the ACF were shown to penetrate into the bump with an anisotropic sliding. With increasing compression length up to 80 μm , the resistance decreased below 500 m Ω and became stable.

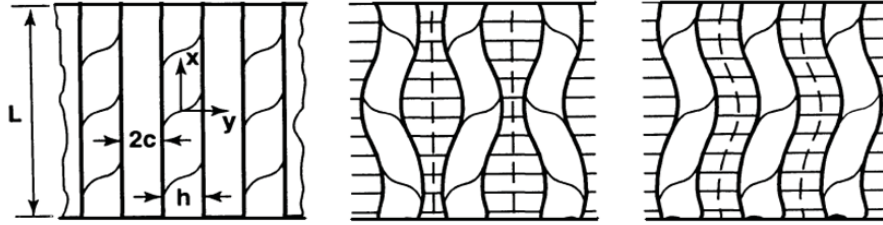


Figure 2.9 Composite buckling model of the vertical fibers in the composite given in [128] (a) Representative volume element, (b) Extension mode and (c) Shear mode.

2.4 Nanowire ACF

Despite the process feasibility and good connection properties that can be achieved for vertical wire ACF, the technical challenges lie in achieving an even smaller hole structure (below 1 μm diameter) with high aspect ratio when the standard photolithography method is used. In addition, due to the high tensile strength of the micro-size wires [128], they may not be structurally compliant. Therefore, nano-hole/pore structures with filling metals are proposed to form nano-wire conductors in the ACF.

2.4.1 Concept and Early Patents

Fine-pitch low tortuosity porous polymer sheets were proposed for the fabrication of the ultra-small size (0.1-50 μm) conductors along the straight-line pores to form anisotropically electrically conductive article in 1991 [135]. Several methods were mentioned in this patent for piercing a suitable number of holes in dielectric including nuclear track etching, laser drilling, punching and re-dissolving. Among them, the nuclear track etching method works by exposing the polymeric sheet to high energy ion bombardment and induces damage tracks. After irradiation, etching in a suitable solution is performed to form tubular pores. This is able to produce the smallest hole diameter down to 0.1 μm in 5-100 μm thick sheets of polymer such as polycarbonate and polyimide. Methods to produce the anisotropically electrically conductive fillers may include several steps: electro- or electroless plating metals in the pores by conditioning the surface of the sheet with a catalyst or coating a thin metal

layer, embedding solder or any fusible low melting metal inside the metal line pores, removing the metal from the surface by simple friction, e.g. wiping or polishing the ends of the tubes and removing the insulating material to expose portions of the conductive material. The fabricated material has been proposed as a temporary or permanent electrical connection in electrical devices or for IC testing purposes.

The other type of the ACF composed of a plurality of minute pores of about 0.01-0.2 μm diameter and a predetermined depth of about 1-100 μm can be formed by anodic oxidation of Al substrate. This was firstly patented by Yoshida in 1993 [136]. The anodic oxidation film, e.g. Al_2O_3 has a plurality of pores formed in a honeycomb pattern and each pore extends in the thickness direction of the film with the diameter of less than 0.2 μm and a pitch between the pores of 0.3-0.4 μm . Ni and Au can be used to fill the pores by the electrolytic deposition method, which have the protruding portions to provide a connection point without applying pressure.

2.4.2 Nanowire Fabrication

A membrane-based synthetic approach to synthesize the desired material within the pores of a nanoporous membrane to obtain monodispersed nanocylinders of the desired material was introduced by Martin's research group in 1994 [137, 138]. Two main types of the nanoporous membranes are track-etch membranes and porous alumina membranes (AAO). For AAO templates, the pores are arranged in a regular hexagonal lattice with pore densities as high as 10^{11} pores/ cm^2 [139]. Although AAO has a highly ordered structure when compared to track-etched membranes, the brittle nature of the AAO templates make them unsuitable as the interconnection material to be sandwiched between two electrodes. Instead, track-etched polymeric membranes [140, 141] containing cylindrical pores of uniform diameter can be used as the base material to form an ACF due to their adhesive properties and great flexibility.

2.4.2.1 Ion-track Etched Membranes

Ion-track etched membranes are commonly polymeric materials having a pore size of 0.01-30 μm and a pore density of 10^4 to 3×10^9 pores/ cm^2 . A thin sheet of polymeric material such as polyethylene terephthalate (PET), polyimide (PI) and polycarbonate (PC) serves as a raw material for the mass production of track-etched membranes. Track-etched membranes made of PET and PC are commercially available.

The fabrication of the track-etched membranes involves two separate processing steps [142]:

- i) irradiation of the template material with energetic heavy ions and creation of latent tracks,
- ii) selective ion-track dissolution and formation of channels by chemical etching.

By controlling the irradiation and etching conditions, membranes with different pore channel geometries (pore sizes, shape, aspect ratios and pore density) can be produced. Typically, ion beams with energy of 2.5-5 MeV per nucleon are employed to penetrate a polymer foil with a thickness of 10-20 μm [141]. The pore density is determined by the applied ion fluence, in a wide range from single ion to 10^{12} ions/ cm^2 [142]. Each ionic projectile induces electronic excitation and ionisation processes in a cylindrical zone along its trajectory. The chemical bonds of the polymer are destroyed in these ion damaged regions and form the ion tracks. The ion tracks have a typical diameter of a few nanometres. To obtain a stochastically distributed and parallel pore shape, magnetic defocusing can be used to generate homogenous ion beams. Depending on the pore density and parallelism of the ion tracks, the non-overlapping or overlapping pore channels can be formed in the membranes. Fig. 2.10 [142] shows schematics that illustrate tracked etched membranes with different porosity regime and the ion irradiation setup.

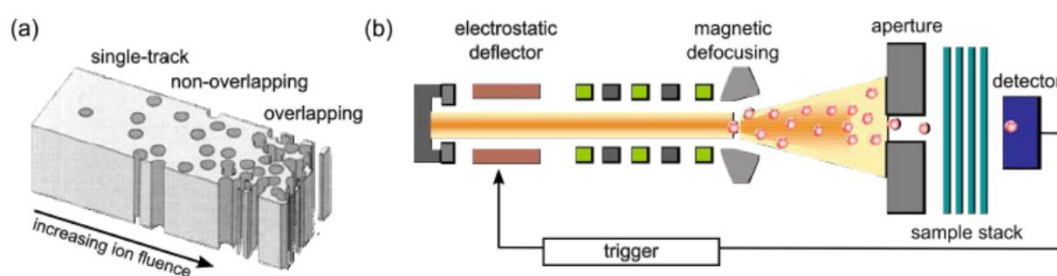


Figure 2.10 Schematics showing tracked etched membranes with different porosity regime and ion irradiation setup (for single ion in this case) [142].

The production of membranes with open channels requires selective dissolution of the latent tracks. The anisotropic dissolution rate along the ion track must be higher than the dissolution rate of the undamaged bulk material. With a suitable etching solution the ion tracks can be selectively dissolved and subsequently enlarged into channels. Tracks in PC are preferentially etched in sodium hydroxide (NaOH) solutions. The etching can be performed

in a thermostated etching bath or in a two-compartment electrolytical cell at constant temperature to produce symmetric cylindrical channels, as shown in Fig. 2.11 (a) and (b), respectively [142]. By applying a voltage between the two electrodes placed at each side of the foil, the electric current can be measured and the etching process is monitored online. Before the pore is etched through, there is no current flow and current increases as the open channels are formed or the pore diameter is enlarged.

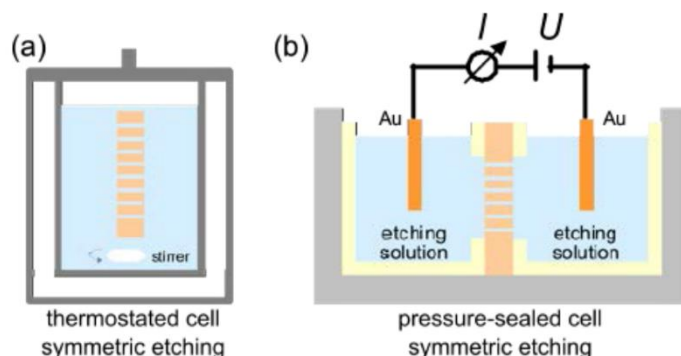


Figure 2.11 Schematics of etching equipment. Symmetric etching conditions leading to cylindrical channels in (a) thermostated cell and (b) electrolytical cell with an applied voltage [142].

2.4.2.2 Electrochemical Deposition

Using the template synthesis method, nanotubes and fibrils of polymers, metals, semiconductors, carbons and other materials can be obtained [138]. Metals are mainly deposited in this work to act as conductors in the ACF. Two convenient methods to deposit metals are electrochemical or chemical (electroless) reduction of the appropriate metal ion. For electroless deposition, a catalyst must be applied to the pore walls and metal tubules are obtained after a brief deposition time [138]. These close up to form solid metal fibrils over longer deposition times. The drawback of this method is that the length of the fibrils run the complete thickness of the pores, but the length is not controlled by the deposition time. On the other hand, electrochemical deposition (ECD) is a widely used method for depositing conducting materials, such as copper, platinum, gold, silver and nickel into the nanopores to form continuous nanowires with large aspect ratios [143-146]. The principle of the electrodeposition is ion transfer reaction that a metal species M^{n+} in solution gain the number n of the electrons e^{-1} and form a metal adatom M_s on a conducting substrate [147]:



The direction of this reaction is determined by the potential applied to the conducting substrate E and the equilibrium potential of the solution E_{eq} . The difference between these potentials is called overpotential, η , where $\eta = E - E_{eq}$. When E is more negative than the E_{eq} , metal ions can be electrodeposited and this is called a reduction process. When E is more positive than E_{eq} , the metal phase is unstable and dissolves and this is called an anodic or oxidation process. During a reduction process, the metal species is firstly deposited on the conducting substrate in a nucleation mode and then an extensive growth of small nuclei takes place to form a continuous layer. The advantages of electrodeposition are [148]:

- high conductivity nanowires can be obtained as dense, continuous and highly crystalline structure can be fabricated using electrodeposition;
- the length of the nanowires can be controlled by monitoring the total amount of passed charge;
- nanowires with multiple segments of different metals in a controlled sequence can also be fabricated by controlling the potential in a solution containing different metal ions.

2.4.3 Nanowire Properties and Characterization

When the characteristic size of the material is reduced to the submicron and nano-meter range, its intrinsic properties including electrical, mechanical and thermal properties can vary from those of bulk materials. For one-dimensional (1D) nanowires, the surface to volume ratio increases considerably with decreasing wire diameter. The size-dependent resistivity due to effects such as surface scattering and grain boundaries increases with the decrease of the cross-sectional areas of nanowires [149-151]. For electrochemically grown single-crystalline copper nanowires, the resistance was measured to be $145 \, \Omega$ for the wire with a diameter of 60 nm and length of 2.4 μm [152]. The specific resistivity calculated from these values is about 10 times higher than that obtained for bulk Cu at 300 K. The onset of Cu oxidation was reported to mainly account for the enhanced value. The reflow properties of nano-scale solder was studied by Gu et al. [153] by forming nanowires containing Au-Ni-Au solder segments that optimize wetting of solder while limiting intermetallic diffusion between the segments. The formation of joints was achieved by reflowing the solder segments together and an ohmic behaviour resistance was obtained in the range of 30-200 Ω as a

function of the effective contact radius. It was also found that solder degradation mechanisms including oxidation, intermetallic diffusion and corrosion can render such solder joints non-conductive at the sub-micrometer length scale.

On the other hand, the mechanical properties of the single nanowire such as elastic modulus and hardness have been studied using electrostatic resonant-contact atomic force microscopy (AFM) method [154, 155]. It is reported that the elastic modulus of nanowires below 100 nm diameter increases remarkably with decreasing diameter due to surface tension effects. The surface effects on buckling of nanowires under uniaxial compression was studied by Wang et al. [156]. By deriving the analytical models for nanowires considering surface effects, they found the critical load became more significant as the diameter decreased to the range of nanometers and as the aspect-ratio of the wires increased. For the arrayed structure of the nanowires, mechanical behaviours such as compression, bending and buckling under indentation have been studied experimentally and with theoretical models, respectively [157, 158]. This is also true for nanowire arrays, where Young's modulus of nanowire arrays increases with decreasing diameter. This is attributed to highly compressive internal stress levels resulting from the surface stress and high surface-to-volume ratios at the nanoscale [157]. Using analytical models of indentation of a nanotube forest [158], it was found that the force-depth behaviour scales linearly with tube areal density, tube moment of inertia, tube modulus and indenter radius and that it scales inversely with the square of tube length. The effects of tube radius (0.15-0.3 μm), tilt angle of tubes and heterogeneous spatial arrangement (square and randomly distributed pattern) are not significant when compared to the effects of other factors. They also concluded that the buckling model predicts the rough friction condition between the indenter and tubes better; while the bending model predicts the behaviour of the no-friction condition more accurately.

2.4.4 Nanowires for Packaging Applications

Packaging-specific applications of nanowires lie mainly in the fields of interconnect formation, sensor development and photonics [159]. The examples of the latter two applications include gold nanoelectrode ensembles (NEEs) for DNA (Deoxyribonucleic acid) biosensing [160], vertically aligned copper nanocones as field emitters with controllable size and shape [161] and cobalt nanowires with a face centred cubic lattice showing anisotropic magnetic properties and a broad optical extinction band for potential magnetic and optical sensor uses [162].

Nanowires in various forms have also been widely used for interconnection purpose. Yousef et al. [163] developed the vertical via interconnects in flexible PCB made from high-aspect-ratio (300:1) Ni nanowires. With 10% via metal fraction, the resulting electrical resistance per via is $0.07\ \Omega$ (via dimension: $26 \times 26\ \mu\text{m}^2$ and thickness of $10\ \mu\text{m}$). Xu et al. [164, 165] reported copper nanowire arrays to be grown on the conductive pads through an AAO template to form metal nanowire bumps. By utilizing flip-chip bonding for two nanowire-bumps, the nanowire to nanowire interweaving “Velcro” type contact can be formed at low temperature with a contact resistance of $0.35\ \Omega$ [165]. Such interconnects were also reported with a bonding strength of more than $5\ \text{N/cm}^2$ at a room-temperature bonding [166]. Fiedler et al. [167] further studied the intercalated nanowires after annealing and found that with increasing annealing temperature or time, a fusion of the nanowires can occur.

Nanowire arrays embedded in a polymer template have been proposed to form an ACF material by several research groups in the last decade. Maekawa et al. [168] studied the potential of PET/Cu hybrid membranes as an ACF by probing the four terminal resistance of the film in the vertical direction and the resultant resistance was found to be in the range of 10^{-7} to $10^{-8}\ \Omega/\text{cm}^2$ for Cu wires of $12\ \mu\text{m}$ length and $200\ \text{nm}$ diameter and wire density of $3 \times 10^7\ \text{cm}^{-2}$. A similar feasibility study has been conducted by Sykes et al. [169] for the PC/Au hybrid membranes as anisotropic conductors. The contact resistance was $\sim 37\ \text{m}\Omega$ measured on their home-made contacting apparatus with a sufficiently high pressure. They also verified experimentally that no conduction between neighbouring wires down to a $25\text{-}\mu\text{m}$ spacing occurred. The research group in ITRI [170], on the other hand, proposed the fabrication of nanowire-ACF based on AAO templates to obtain Ag/Co multilayer nanowire arrays and magnetic alignment of the nanowires after the removal of AAO and during refilling the low viscous PI into the nanowires. The reported Z-axis resistance was less than $0.2\ \Omega$ and X-Y insulation resistance was $4\text{-}6\ \text{G}\Omega$ of the fabricated film. Meanwhile, such nanowire ACF was proposed for fine-pitch flip-chip bonding between the chip and substrate with the application of additional non-conductive paste (NCP) [171]. The effective properties of nanowire ACF was modelled by the rule-of-mixture (ROM) technique and the optimization of the material and process related properties was carried out by a combination of finite element modelling and quadratic regression models to minimize warpage and peeling stress and maximize contact stress for the proposed package [172]. Stam et al. [173] reported Cu nanowire based ACF for the electrical connection between the gold stud bump and Au layer with a resultant electrical resistance of $2.5\text{-}3\ \Omega$. In addition, Razeeb et al. [174-176] has explored the viability of Ag nanowires embedded in polycarbonate template as a thermal interface material, which

is regarded as an additional benefit that could apply to such nanowire composite material for interconnection purpose with good thermal properties. All these works preliminarily establish the concept of nanowire embedded polymer material as an ACF material.

2.5 Conclusions

This chapter discussed the development trends of ACA technologies, from commercial particle dispersed ACAs to vertical wire ACFs and brought forward the concept of nanowire ACF. As a well-developed electrically conductive bonding agent, commercial particle dispersed ACAs have widely been used in the display industry for more than thirty years. There are immense studies towards material, fabrication and interconnection process of these ACAs and the effects of process parameters, contact resistance theory and failure mechanisms were explicated. New developments of particle dispersed ACAs such as nano-Ag or solder particles have led to new applications with finer pad/pitch size. However, constraints such as particle agglomeration and low volume fraction of the particles make such ACAs not suitable for chip-to-chip applications with low electrical resistance requirement. To solve the particle agglomeration issue, vertical wire ACFs have been developed with orderly distributed conductors in the patterned structures. The Z-axis ACF with vertical wire conductors has been successfully demonstrated for fine-pitch chip/wafer level interconnection. However, limitations of this technology are the photolithographic based patterning process and the rigidity of the wire conductors with micro-size diameter. To obtain high aspect-ratio nano-size wire conductors, the concept of nanowire ACF is proposed by fabricating nanowires in ion-track etched membranes. The nanowires show promising results in terms of electrical, mechanical and thermal properties, which can be used as compliant conductors in an ACF. It is the focus of this work to fabricate nanowire ACF and evaluate the structural, thermal, electrical and mechanical properties of such novel material for interconnection purpose, which will be discussed in the following chapters.

Chapter 3 Fabrication and Material

Characterization of Nanowire ACF

3.1 Introduction

In this work, the fabrication of nanowire-ACF (NW-ACF) is based on the electrochemical deposition (ECD) method in nanoporous templates. Track-etched polymeric membranes, made from flexible polycarbonate, have been used to directly fabricate composite films for both electrical [169, 173] and thermal [174] conductive purposes. The challenges associated with the fabrication of NW-ACF for interconnect purposes are to select templates with a high quality pore structure and to raise the filling ratio of metal in the templates during the ECD process. The pore structure and density will determine the electrical properties of the fabricated film. Three different track-etched polycarbonate membranes from three different suppliers were employed to fabricate the NW-ACFs. To obtain a high filling ratio, a novel overgrowth-stripping method was developed to fabricate a copper nanowire based ACF (Cu NW-ACF). The material properties of the NW-ACFs in the different templates were characterized by microstructural and thermal analysis. To electrically characterize the NW-ACF, bonding experiments were carried out with In coated Ti/Cu/Si substrates. The bonding parameters were investigated in terms of interconnection resistance and die shear strength.

3.2 Fabrication of the NW-ACF

3.2.1 Selection of Template

Commercially available track-etched polycarbonate membranes with nominal pore size of 200 nm were selected as the nanoporous template to fabricate the NW-ACF. As the nanowires will mimic the shape and size of the pores, the pore diameter in the film should be carefully considered to obtain the fine-pitch conductors and should not be so small as to compromise the electrical performance. Copper was selected as the low resistivity metal to be deposited in the pores to form the nanowire conductors. The resistivity of copper (Cu) is reported to increase substantially, when the line width (or diameter of the nanowire)

decreases below ~100 nm [150]. Therefore, templates with an average pore diameter of 200 nm were considered suitable to fabricate the Cu nanowires with the same size.

Table 3.1 Specifications of polycarbonate membranes.

Template	Supplier	Pore size (nm)	Thickness (μm)	Nominal Porosity (by suppliers)	Calculated Porosity (by SEM)
A	Millipore	220	25	13.8%	20%
B	Whatman/GE	200	10	< 15%	6.4%
C	Sterlitech	200	10	9.4%	9.8%

Three types of template were selected from different suppliers as: 1. Millipore, 2. Whatman and 3. Sterlitech for evaluation as potential substrates. The specifications of the selected membranes are listed in Table 3.1. In addition to the pore size, the membrane thickness and porosity will also determine the electrical and mechanical properties of the NW-ACF to be fabricated. The larger membrane thickness corresponds to a longer nanowire length and therefore higher electrical resistance of individual wires. Whereas, a larger film thickness can enhance the adhesion properties of the polymer due to a better conformability with surface roughness [177]. A high porosity will result in a high volume fraction of nanowires in the template after fabrication and this will increase both the electrical conductivity and the longitudinal modulus of the composite film. However, if the pore density is too high, it will compromise the X-Y plane insulation of the nanowire conductive films, which is not a desirable outcome.

Compared to the nominal porosities which are given by suppliers, the actual porosity can be obtained by processing SEM images of the respective templates with ImageJ software [178] and obtaining the percentage of the pore area from the total surface area. The surface morphology of the respective templates are shown in Fig. 3.1. The calculated porosities for each template are listed in Table 3.1 and compared with the nominal porosities given by the supplier. The difference between the nominal and calculated porosities are possibly due to the different measurement methods applied. Generally, Template 1 had a higher porosity and thickness, as compared to Template 2 and 3.

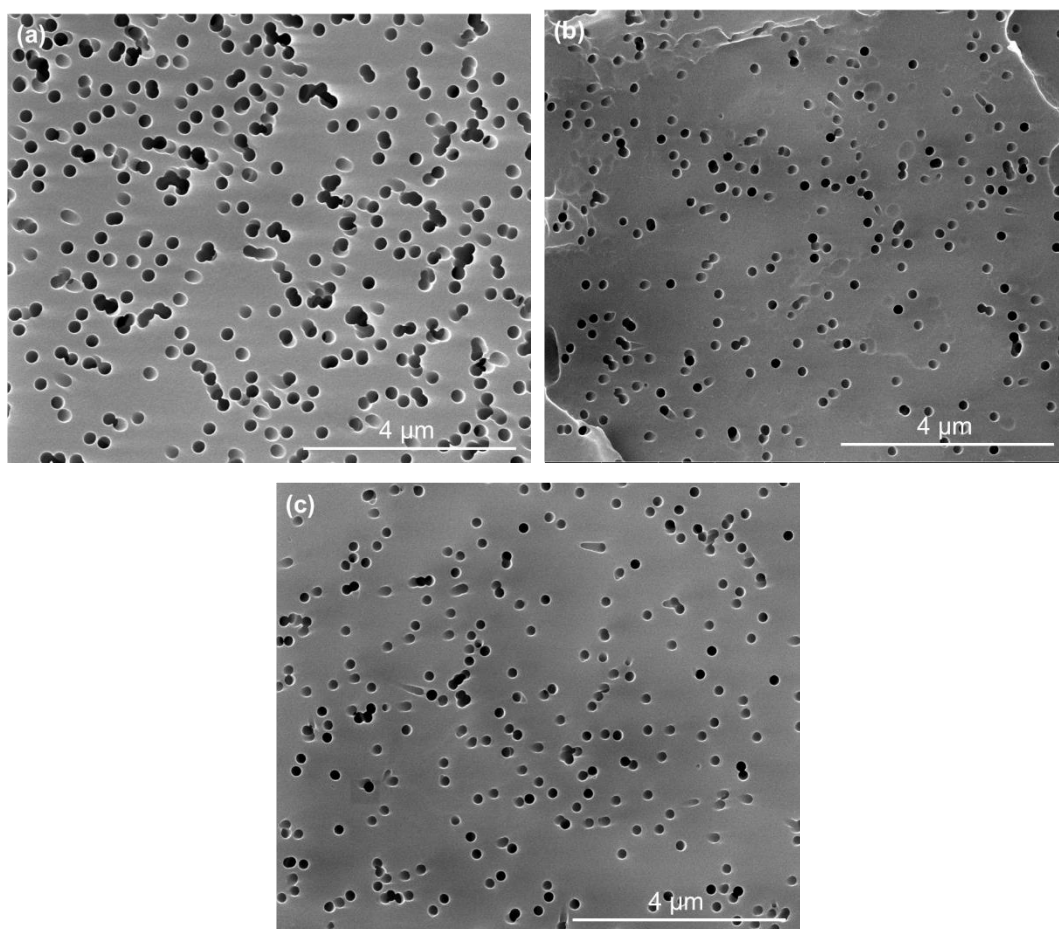


Figure 3.1 Surface morphology of polycarbonate membranes from different suppliers (in Table 3.1), (a) Template 1, (b) Template 2 and (c) Template 3.

3.2.2 Copper Electrochemical Deposition

Electrochemical deposition is the technique used to fabricate the Cu nanowires through the porous template in this work. There are many factors that influence the nanowire growth in the template, such as the influence of current density applied during electrodeposition, the bath temperature, and the type of electrolyte on the resulting crystallinity of the nanowire [179]. The electrolyte cell setup and the pore characteristic of the template also play a role on the homogenous growth of the nanowires in the template [180, 181]. On the other hand, to achieve a high conductivity of the NW-ACF, the pores are expected to be fully filled with the deposited metal, i.e. a high filling ratio needs to be achieved. According to the research work by H. Yosef et al. [163], the filling ratio in the template mainly depends on the process parameters of electrodeposition, the quality of the seed layer and the wetting of the template.

Furthermore, to form a NW-ACF material, efforts should be made to remove all metal residues on both surfaces of the film to ensure that no lateral electrical conduction occurs.

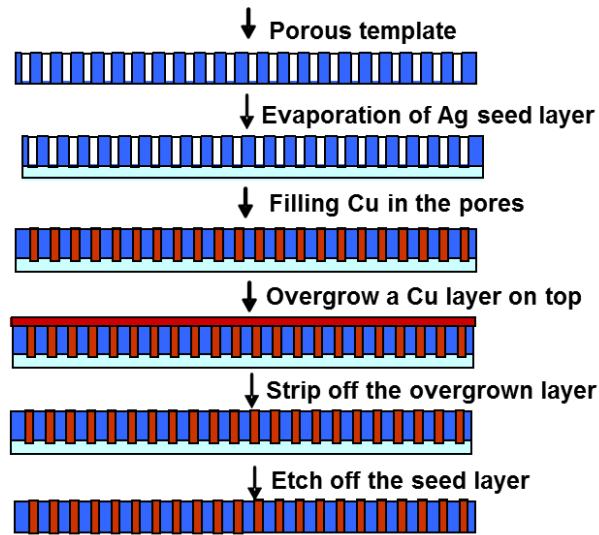


Figure 3.2 Process flow of NW-ACF fabrication.

Fig. 3.2 illustrates the process flow used in this work to fabricate NW-ACF. Firstly, a 400 nm thick Ag layer was evaporated in a Temescal FC-2000 E-beam evaporation system. This serves as the cathode and the seed layer for growing nanowires. With 400-nm thickness of seed layer, the 200-nm diameter pores can be sufficiently blocked. A SEM image of the sputter Ag seed layer on the porous template is shown in Fig. 3.3. From the image, the pore openings (as shown in Fig. 3.1) can hardly be seen, where the tiny holes in the metal layer represent the blocked pores underneath. The blockage of the pores is to prevent the ions in the electrolyte during electrodeposition from diffusing through a shorter way from backside of the template and alleviate the ion diffusion problem during deposition [182]. Then the Ag-coated template was assembled in a home-made sample holder for electrodeposition, as shown in Fig. 3.4. The Teflon sample holder is a solid support, where a cut-to-shape copper foil is used as the back contact to the seed layer on the template with the plastic O-ring and the clips with screws were used to seal the periphery of the template to prevent deposition on the backside. The geometric area exposed for deposition is $\sim 12 \text{ cm}^2$.

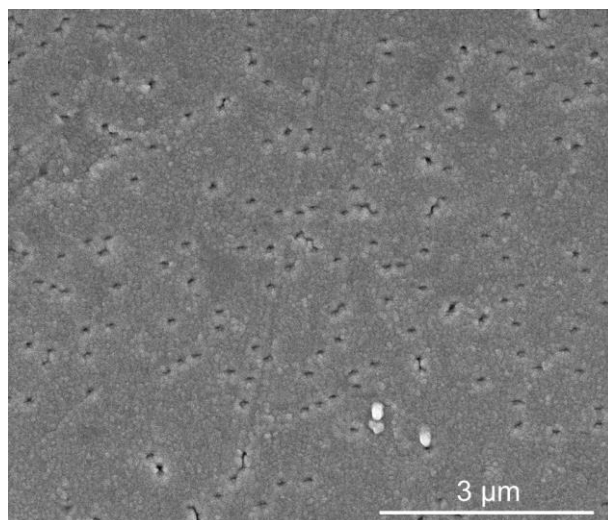


Figure 3.3 SEM image of the backside of PC membranes with 400 nm Ag sputtering.

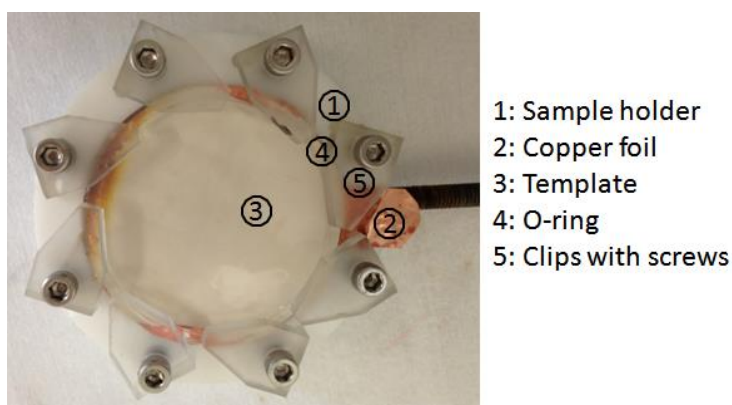


Figure 3.4 Optical image of the sample holder used for electrodeposition.

Electrodeposition was carried out in an electrochemical cell with two-electrode (working and counter electrode) configuration under galvanostatic conditions, as shown in Fig. 3.5. During deposition, the metal coated membrane was connected to the working electrode and immersed in the electrolyte solution. A copper plate (dimension of $50 \times 50 \times 2 \text{ mm}^3$, 99.99%, Goodfellow) was used as the anode and connected to the counter electrode. The electrolyte for Cu deposition consisted of 0.24 M $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$ and 1.8 M H_2SO_4 in an aqueous solution. A high concentration of CuSO_4 was used to supply a sufficiently large number of ions inside the pores during the deposition and sulfuric acid was added to increase the conductivity of the solution [179]. Meanwhile, the additives of polyethylene glycol (PEG) (300 ppm) and Cl^- (50 ppm) as NaCl were added in the electrolyte as the stabilizers, according to the earlier work by Hasan et al. [183]. The wetting of the template was performed by immersing the template in the electrolyte for at least 30 minutes before deposition. For galvanostatic deposition, a

constant current of 40 mA was applied between the cathode and anode using a CHI 660C instrument and the potential-time (V-t) curves were generated to monitor the deposition process. The deposition was carried out at room temperature and magnetic stirring was applied at 100 rpm to improve the ion diffusion into the pores.

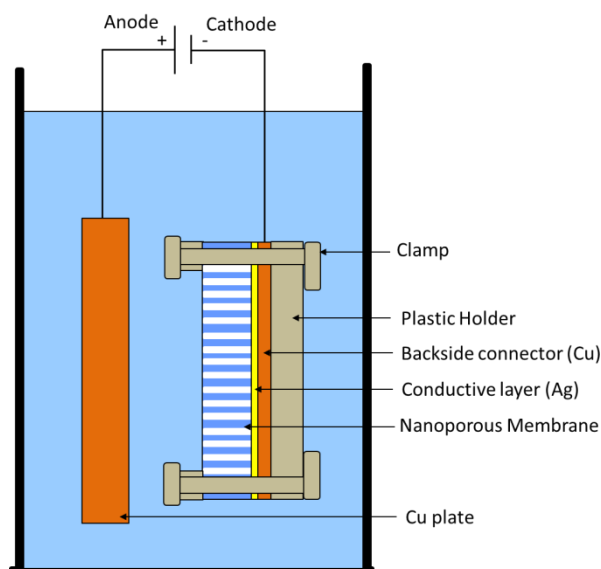


Figure 3.5 Schematic showing the electrodeposition in a two-electrode setup.

Fig. 3.6 shows a representative V-t curve obtained during the Cu electrodeposition process. The V-t characteristics in different colour regimes corresponding to the four stages of nanowire growth, which has also been reported elsewhere by monitoring the I-t curve [142]. The four nanowire growth stages are reflected by the V-t curve as:

- (a) a sharp decrease of the potential at the beginning of the process (~ 400 s) attributed to the creation of the diffusion layer of the deposited metal;
- (b) a nearly constant potential period (~ 1800 s) demonstrating the nanowire growth along the pores;
- (c) a rapid potential increase period (~ 1800 s) when the nanowires reaches the top side of the membrane and the metal caps start to grow on the membrane surface;
- (d) if the process is continued, the caps grow further and eventually form a continuous layer.

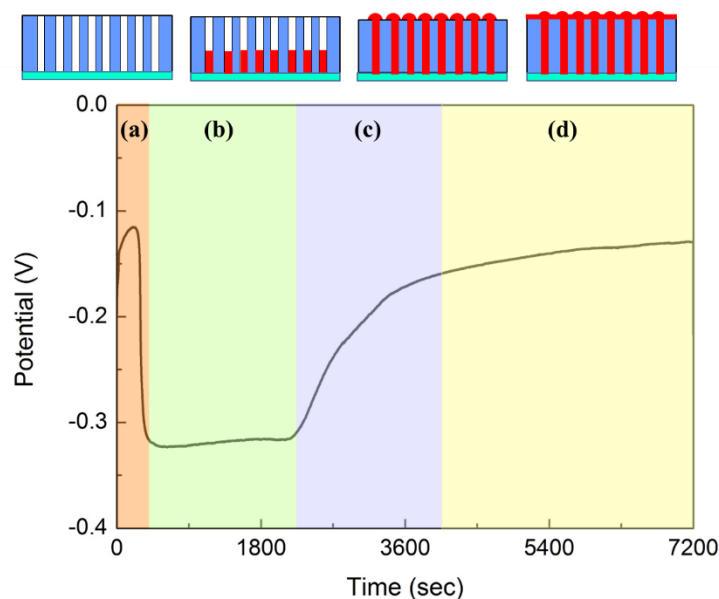


Figure 3.6 Representative V–t curve and schematic of the four different deposition regimes.

During the deposition, it was found that not all pores are filled up with nanowires at the same time. One possible reason for this is that not all pores in the templates were aligned parallel to each other and some exhibit a considerable angular distribution of $\sim 30^\circ$ to the surface normal [148]. To achieve the complete filling of every pore in the template, a so-called overgrowth-stripping method was developed in this work. This method allows nanowires to grow in as many pores as possible by depositing at a small current for a very long time (3–4 hours) and allowing a continuous Cu layer to grow on the template surface. With a several hundred- μm thick overgrown layer of Cu, it can be mechanically stripped off from the template with a tweezer applying a 90° peeling force to the membrane surface. After stripping off the overgrown layer, a residue-free surface without Cu particles can be achieved. Fig. 3.7 (a)–(c) show the stripping process for preparing a NW-ACF film, where (a) is the Cu-filled membrane with an overgrown layer, (b) is the half separated Cu layer from the underneath film and (c) is the finished film with a residue-free surface. Finally, the Ag seed layer was etched in dilute $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$ (1:1) solution for several seconds. The fabricated film was thoroughly rinsed in deionized (DI) water and dried with a nitrogen gun before using.

As further improvement to the fabrication process, a double-stripping method can be applied by depositing overgrown Cu layer on both sides of the template. During chemical etching of Ag seed layer, a length of the nanowires exposing to the chemicals can also be etched off. To regrow the etched length of the nanowires, the first overgrown layer was kept

to serve as the new seed layer to allow nanowires growing to the opposite side and forming the second overgrown layer of Cu. Then both overgrown layers were stripped off to prepare the residue-free surfaces and the full length of nanowires along the pores can be achieved.

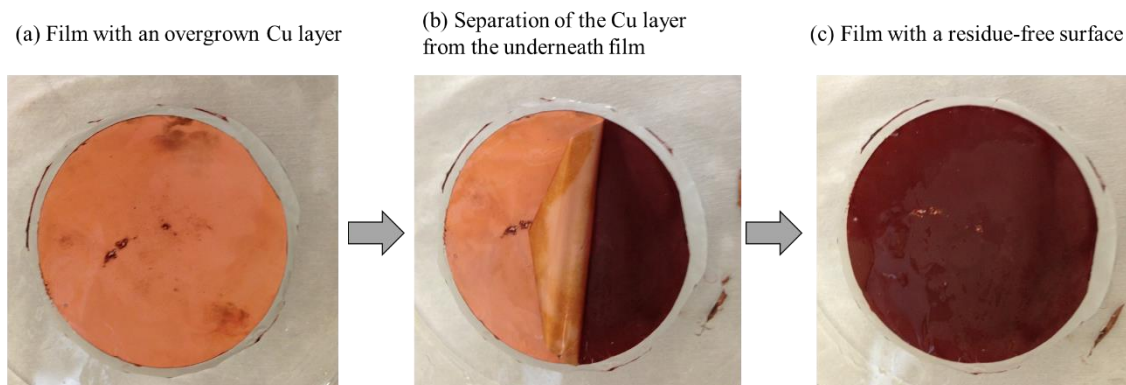


Figure 3.7 Optical images showing the stripping process of the Cu overgrown layer, (a) film with an overgrown Cu layer after electrodeposition, (b) separation of the Cu layer from the underneath film and (c) the resultant film with a residue-free surface.

3.3 Microstructural Analysis of the NW-ACF

3.3.1 Morphology of Nanowires in the Template

Scanning Electron Microscope (SEM) is an exceedingly useful inspection and analysis tool for material microstructure studies especially in the aspect of imaging of surface topography and analyzing elemental composition of structures. An FEI QuantaTM 650 FEG SEM combined with Energy-Dispersive X-ray Spectroscopy (EDS) was used to observe the micro/nano-structure of the fabricated film and conduct the compositional analysis in this work. For observing polymer samples under SEM, a very thin (~ 20 nm) layer of Au was sputtered on the surface of the samples to eliminate the polymer charging issue and the secondary electrons scanning mode was used to obtain these images. Fig. 3.8 shows the cross-sectional view of the NW-ACF based on template A and C as the representative images of the fabricated films. To obtain the images, the films were laterally torn so that the edge of the films can be exposed, rendering the embedded nanowires visible. From the images, the nanowires are seen to span the entire thickness of the membrane and some of them are protruding from the pore opening as seen in image (b). For both films, no lateral short Cu particles are found on the film surface so that the residue-free surfaces are confirmed to be

obtained using the stripping method. Comparing the two films, NW-ACF A has much longer nanowires as compared NW-ACF C, due to the membrane thickness variance. To further observe the fabricated nanowire arrays in the films, PC template can be chemically removed.

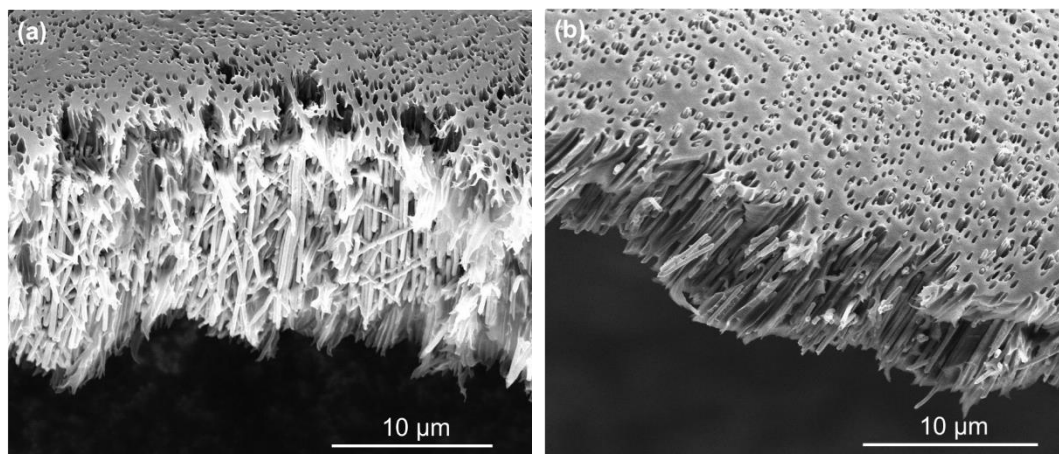


Figure 3.8 SEM images showing cross-sections of the fabricated NW-ACFs, (a) NW-ACF A and (b) NW-ACF C. The films were laterally torn to obtain the images.

The nanowire arrays in the template represent the same structure as the pore channels. As previously stated, one potential problem with the PC membranes is the occurrence of non-parallel pore structure due to the pore formation process [140]. In order to understand the positioning of pores in the template, we observe the morphology of the grown nanowires which replicates the pore structure. To obtain the image of nanowire arrays in the template, the specimen was carefully prepared by dissolving PC template using dichloromethane (CH_2Cl_2) solution. By controlling the etching time, a small amount of residue of the PC was left on the specimen of the exposed nanowires to retain their positions as in the template. Fig. 3.9 (a) to (c) shows the representative structures of nanowire arrays in the respective NW-ACF after removing the template. For nanowires in NW-ACF A, we can see that many wires grew laterally between the vertically standing wires. This possibly results from the pore shape with many branches as previously described by Dobrev et al. [184]. In contrast, nanowires in NW-ACF B and C are more distinct and insulated from each other. However, these nanowires still have a distribution angle and are not totally parallel to each other. This will be a process that will need to be optimized with membrane suppliers for the future development of the NW-ACF.

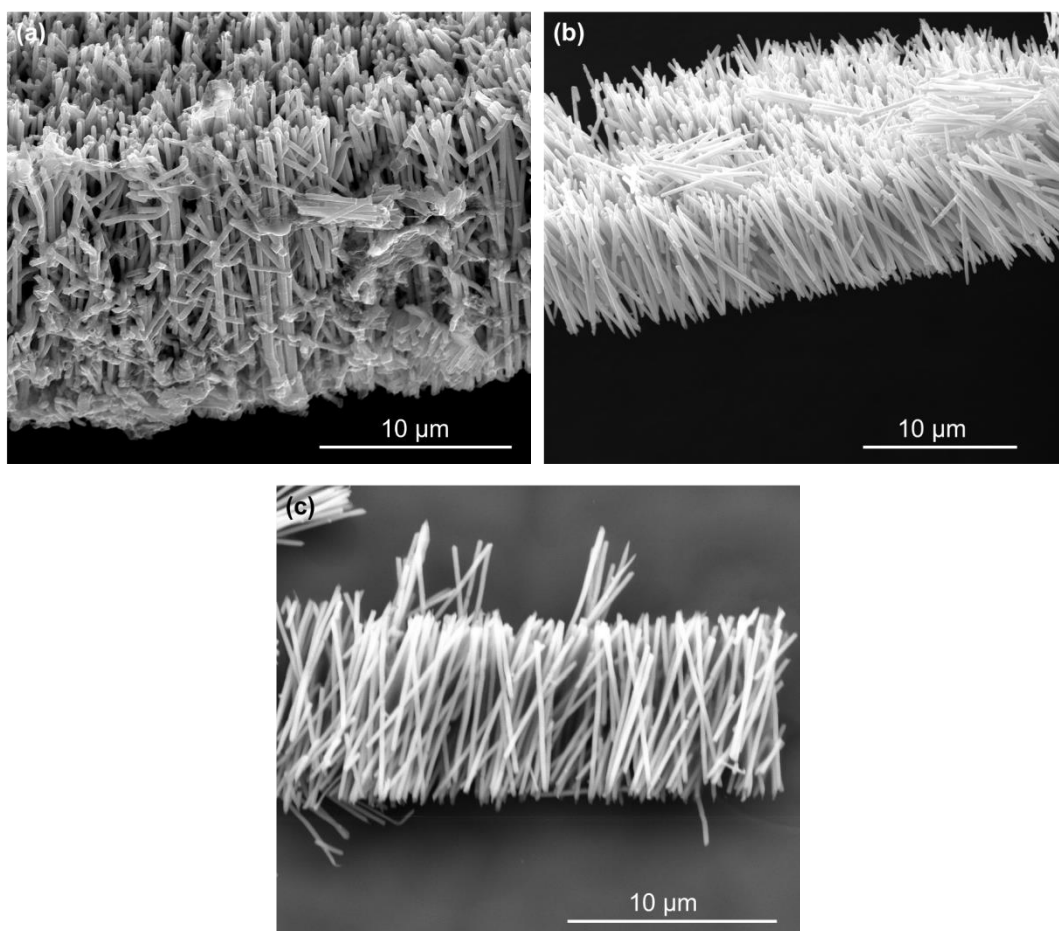


Figure 3.9 SEM images showing the morphologies of nanowire arrays in (a) NW-ACF A, (b) NW-ACF B and (c) NW-ACF C. The samples were obtained by dissolution of polycarbonate membranes in dichloromethane.

3.3.2 Filling Ratio Calculation

There are two methods to calculate the nanowire filling ratio (or volume fraction) in the template. These give the so-called apparent filling ratio and the real filling ratio for nanowires inside the templates. Fig. 3.10 (a) to (c) show the SEM images of pore distribution and the filling of the pores in NW-ACF A, B and C respectively. The white dots in the image indicate the extruding nanowires which are visible from the opened pores. From the images, NW-ACF A has a higher pore density than those of the other two NW-ACFs and the pore shapes are more irregular as the merged pores. By counting the number of the visible nanowires that are a proportion of the total pore number, the percentage of the filled pores was obtained, which are 60%, 40% and 65% for NW-ACF A, B and C, respectively. The apparent filling ratio is defined as the percentage of the filled pores multiplied by the porosity of the template.

The calculated porosity (from Table 3.1) and the filled pore percentages are listed in Table 3.2 and the resulting apparent filling ratios for NW-ACF A, B and C are 12%, 2.6% and 6.4%, respectively. However, the actual values could be higher due to the limit of viewing angle. The apparent filling ratios have an impact on the bonding property of the NW-ACF, since the protruding nanowires out of the pores are more inclined to contact the pads during bonding. To obtain a higher apparent filling ratio, the electrodeposition process can be further optimized or some etching methods can be used to obtain the protruding nanowires [185].

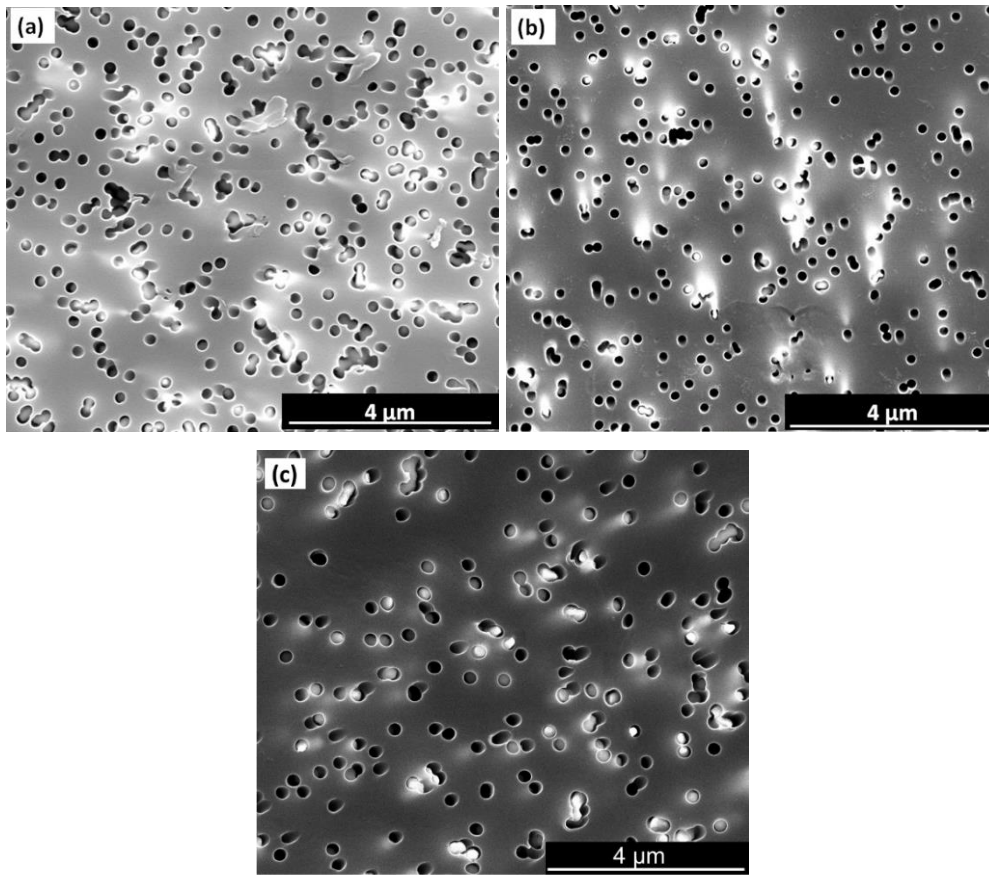


Figure 3.10 SEM images showing the pore density and the apparent filling ratio of (a) NW-ACF A, (b) NW-ACF B and (c) NW-ACF C at the same magnification.

To obtain a real filling ratio, it is necessary to include all deposited metal in the template. To obtain this ratio, the weight of the film before and after deposition was measured. The real filling ratio ϕ as defined by Xu et al. [174] is provided as:

$$\phi = \frac{V_{Cu}}{V_T} = \frac{(W_2 - W_1) / \rho_{Cu}}{hS} \quad (3.1)$$

where V_{Cu} is the volume of Cu nanowire, V_T is the total volume of template including the pore volume, W_1 and W_2 is the film weight before and after electrodeposition, ρ_{Cu} is the density of copper, h is the thickness of the film, S is the surface area of the sample being weighed (the film with $1 \times 1 \text{ cm}^2$ surface area was cut and weighed in this work). The calculated results are given in Table 3.2. Compared to the apparent filling ratios, the real filling ratios are nearly two times higher for all NW-ACFs, which are 25.3%, 6.4 % and 12.5% for NW-ACF A, B and C, respectively. Interestingly, it was found that the real filling ratio of NW-ACF A and C is even higher than the respective porosity of the template. This can be due to some pore structures without openings to the surface, which are created by the ions that have not penetrated the membrane during the ion track process. For NW-ACF B, the calculated porosity is 6.4 % and this value coincides with the real filling ratio as calculated, which indicates that nearly 100% of the pores have been filled. Generally, the filling ratios of NW-ACF A and C are greatly improved as compared to the previously reported data ($\sim 9\%$) for the fabrication of the Ag-NW arrays in the polycarbonate template [174].

Table 3.2 Filling ratios of the NW-ACFs.

NW-ACF	Calculated porosity (By SEM)	Filled pore percentage (By SEM)	Apparent filling ratio ¹	Weight of Cu deposit (mg/cm ²)	Real filling ratio ²
A	20 %	60 %	12 %	6.78	25.3 %
B	6.4 %	40 %	2.6 %	0.57	6.4 %
C	9.8 %	65 %	6.4 %	1.4	12.5 %

¹: Apparent filling ratio is the observed surface pore density multiplied by the observed filled pore percentage.

²: Real filling ratio is calculated from the weight method based on eq. 3.1.

3.4 Thermal Analysis of the NW-ACF

3.4.1 Glass Transition Point

When considering a polymer material to be used for an adhesive bonding purpose [47], the phase change of such a polymer from a solid state to liquid, semi-liquid or viscoelastic state at certain temperatures is one of the important material variables. This may affect the

contact quality, bonding strength, nanowire stability during bonding, and even yield and reliability. Glass transition point (T_g) is the temperature when a polymer changes from a solid, glassy state to a viscous, liquid-like state [186]. The NW-ACF in this work is based on a polycarbonate template, which is a thermoplastic polymer, whose glass transition point will determine the minimum bonding temperature needed to form adhesive bonding between the polymer part of the NW-ACF and the bonding surface.

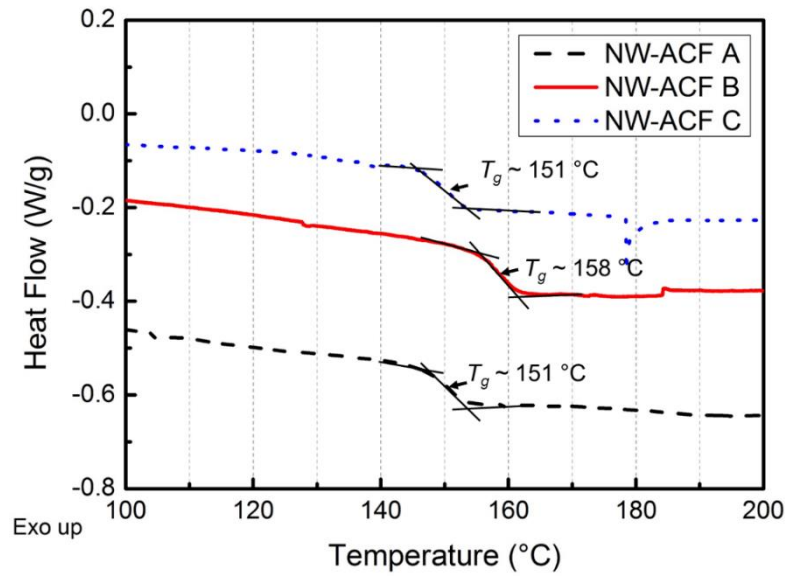


Figure 3.11 Glass transition temperature of NW-ACF A, B and C measured by DSC. (Note the marked point for T_g is to approximate the half- C_p extrapolated point.)

Differential Scanning Calorimetry (DSC, TA Q1000), which can provide quantitative analysis of the glass transition, was used to measure the T_g for all three types of NW-ACFs. The operational principle of DSC is that the temperature of a sample of a material is measured continuously, and a differential technique is used to assess the heat flow into it and to equalize incidental heat gains and losses between the reference and the sample materials [187]. By recording the heat capacity (C_p) change during heating or cooling the material within the transition period, T_g is obtained by approximating the half- C_p extrapolated point in the heat flow curve. The half- C_p point represents the middle point of the glass transition process. In this work, the DSC measurement was conducted at a standard heating rate of 10 °C/min under N_2 purge in the temperature range of 30 - 300 °C. Fig. 3.11 shows the DSC containing glass transition in the temperature range of 100 - 200 °C for the three NW-ACFs. From the curves, glass transition points of NW-ACF A and C are 151 °C, and that of NW-

ACF B is 158 °C. The transition ranges including the onset and end points of the NW-ACFs are 147 -153 °C for NW-ACF A and C and 155 - 161 °C for NW-ACF B. The variation of the T_g values for NW-ACF B can be attributed to the different polycarbonate material or material treatment during manufacturing of the template by the supplier. Generally, the measured T_g values for the NW-ACFs are comparable to the T_g of bisphenol-A polycarbonate (~ 150 °C) as reported by Sohn [188]. The T_g of the NW-ACFs imply that the minimum bonding temperature should be above 160 °C to achieve a proper bonding.

3.4.2 Thermal Stability

The thermal stabilities of the NW-ACF were studied using thermogravimetry analyser (TGA, TA Q500) to monitor the weight change of the polymer under various temperatures. The experiment was conducted using a heating rate of 5 °C/min from ambient temperature to 400 °C in a nitrogen environment. The results of the weight loss of each NW-ACF in terms of the temperature are shown in Fig. 3.12. It was found that NW-ACF B and C have a small weight loss of < 2% up to 400 °C, which can be caused by the evaporation of moisture in the films. NW-ACF A shows an obvious weight loss up to 6 wt% at 300 - 400 °C, which may indicate the onset of the polymer decomposition at 300 °C. Therefore, NW-ACF B and C show a better thermal stability at high temperatures as compared to that of NW-ACF A.

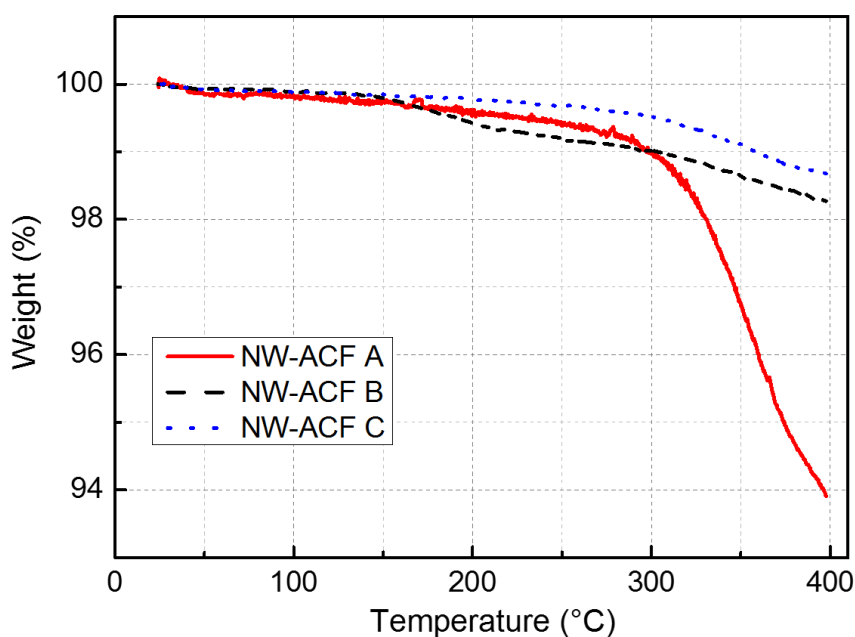


Figure 3.12 TGA analysis of NW-ACF A, B and C.

3.4.3 Dynamic Mechanical Analysis

The study of elastic and viscoelastic materials under conditions of cyclic stress or strain is called dynamic mechanical analysis, DMA [186]. Dynamic mechanical analyser (DMA) is the instrument used to measure stress versus strain as a function of frequency and temperature, which is a direct link to the mechanical behaviour of polymeric materials. From DMA, the temperature dependent storage, loss modulus, and tangent delta ($\tan \delta$) of the material can be obtained. The storage and loss modulus correspond to the elastic and viscous component of the sample and $\tan \delta$ reflects the phase difference between the two. The storage modulus is related to the sample's stiffness and the loss modulus is related to the sample's ability to dissipate mechanical energy through molecular motion.

Dynamic mechanical properties of the NW-ACFs were investigated using a DMA instrument TA Q800, with a film tension clamp. After a sample was mounted on the clamp, the temperature was raised from 30 °C to 180 °C at a heating rate of 3 °C/minute. The sample was studied under an oscillation mode with a frequency of 1 Hz at an amplitude of 15 μm . Fig. 3.13 (a) and (b) shows the DMA curves of the NW-ACF A and C, respectively. Under the temperature of 140 °C, the storage modulus of NW-ACF A and C are 1.8-2.2 GPa and 1.5-1.9 GPa, respectively. The modulus data are comparable to the storage modulus of the particle-based ACFs as reported by Hwang [189] and the high modulus of ACF materials were reported to be effective to obtain the reliable flip chip assembly. The higher storage modulus of NW-ACF A is resulted from a higher volume fraction of Cu in this film. During the glass transition period, the storage modulus decreases and the loss modulus increases. This corresponds to the change of the polymer from elastic to the rubbery and viscous states. The modulus and viscosity of the polymer at high temperature are important for NW-ACF bonding. With a low modulus, the nanowires are able to penetrate through the polymer to make the contact. Furthermore, with a lower viscosity, the polymer can easily flow over the bonding surfaces to fill the gaps. It is interesting to note that for NW-ACF C, the film snapped at ~160 °C during the testing, which causes all values to return to zero. This may indicate a low modulus and viscosity property of the film at that temperature.

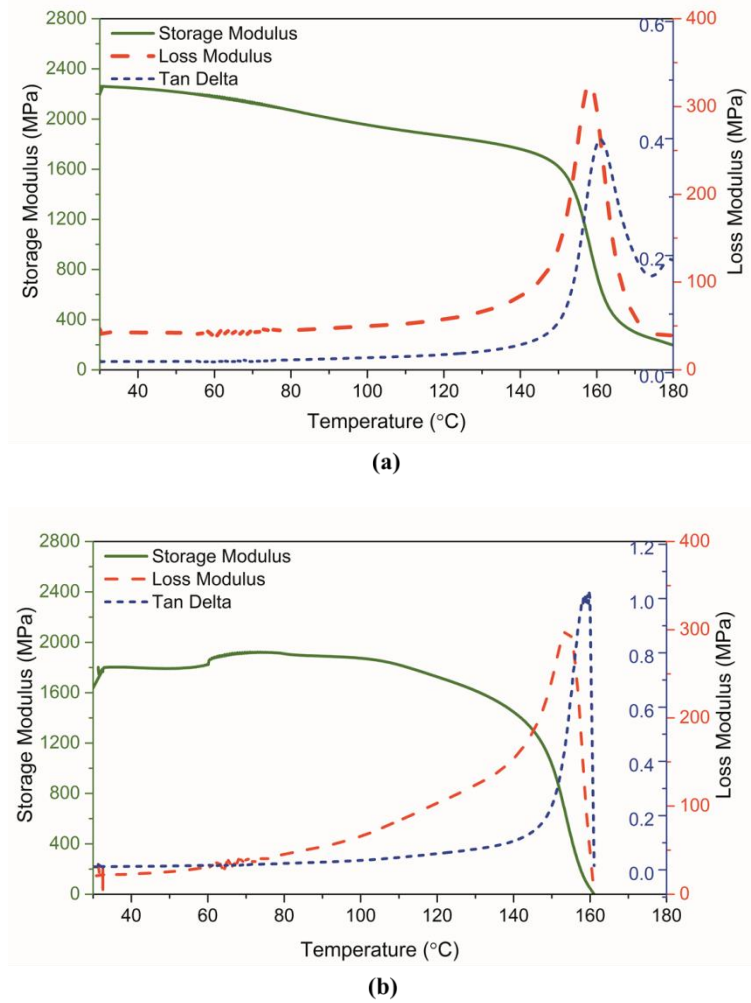


Figure 3.13 DMA analysis of (a) NW-ACF A and (b) NW-ACF C.

3.5 Thermocompression Bonding with NW-ACF

3.5.1 Bonding Instrument

Thermocompression bonding (TCB) was carried out with a FINETECH lambda flip-chip bonding system as shown in Fig. 3.14. The system is used for micro-assembly with a placement accuracy of $\pm 2 \mu\text{m}$. The system is mainly composed of a die pick-up module, a chip heating module, as well as substrate heating, bonding force and process video modules. During bonding, the die pick-up module picks up the flipped top die and aligns with the bottom die or substrate placed on the heating plate. The co-planarity between the top and bottom die/substrate is adjusted by focusing the bonding surfaces with the aid of the process video module.



Figure 3.14 FINEPLACER® lambda flip-chip bonder.

With the TCB process, the NW-ACF can be bonded between the top and bottom chip as shown in Fig. 3.15. After carefully alignment of the top and bottom chip with a sharp focus on both surfaces, the NW-ACF is placed gently on the bottom chip and the top chip is brought down with the tool head. The bonding force is manually adjusted with a lever weight system. Then the temperature process can be started using the computer control according to the pre-programmed temperature profile.

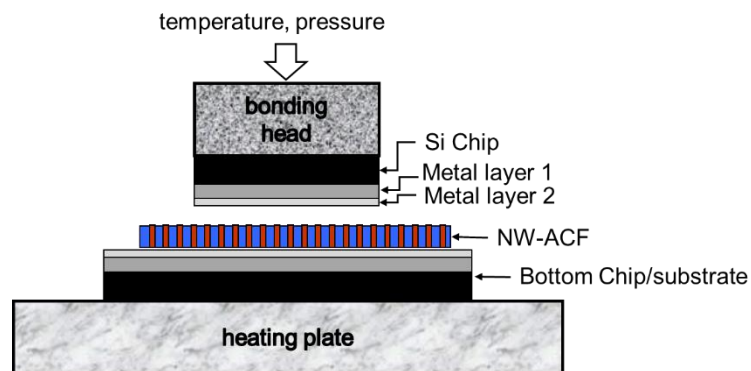


Figure 3.15 Schematic showing thermocompression bonding with the NW-ACF between the top and bottom chip.

3.5.2 Process Parameters

During the bonding between two chips, two types of connections are expected to occur, the physical contact or alloying of the Cu nanowires with the bonding metals and the polymer adhering to the whole bonding surface area. Many factors have been studied that affect the

ACA bonding such as bonding conditions, pad size, bump height and substrate stiffness [55]. Among them, the bonding conditions, including bonding temperature and force are primarily important to achieve a successful bonding. To set up the bonding temperature, it should be noted that the minimum temperature of the NW-ACF during bonding should be above the glass transition temperature of the polymer in order to achieve a proper adhesion. This temperature is ~ 160 °C according to the DSC data in Fig. 3.11. Since the bonding was conducted in an ambient air environment, there was heat loss from the heating tool to the position of the NW-ACF layer. The preliminary bonding experiments showed that a minimum bonding temperature of 180 °C is needed to be applied to form a stable joint, which may indicate a ~ 20 °C temperature loss from the bonding tool/ heating plate to the ACF bonding layer. As the same temperatures were applied on both top and bottom Si dies which have good thermal conductivity, a thermal equilibrium can be established quickly in such a bonding system, where it is assumed that the temperature gradient is not significant to cause high thermal stress during bonding. To investigate the temperature influence on the bonding process, the bonding temperature was varied at 180, 200 and 220 °C in the experiment. During bonding, a typical bonding profile is set as shown in Fig. 3.16 (yellow line), where the peak temperature is set at 220 °C for both top and bottom heating. From the profile, the heating starts at the standby temperature of 40 °C with a ramping rate of 3 °C/s. The peak bonding time is 60 s and the total heating time is ~ 120 s before the cooling started. The actual top and bottom heating curves during one bonding process are also shown in the same graph, where the green and blue lines represent the measured heating/cooling curves at the heating plate and the tool head respectively. During the thermal process, the bonding force is applied from the start of heating till the cooling down to standby temperature. The adjustable bonding force in the bonding system is 1 - 40 N with a resolution of 1 N.

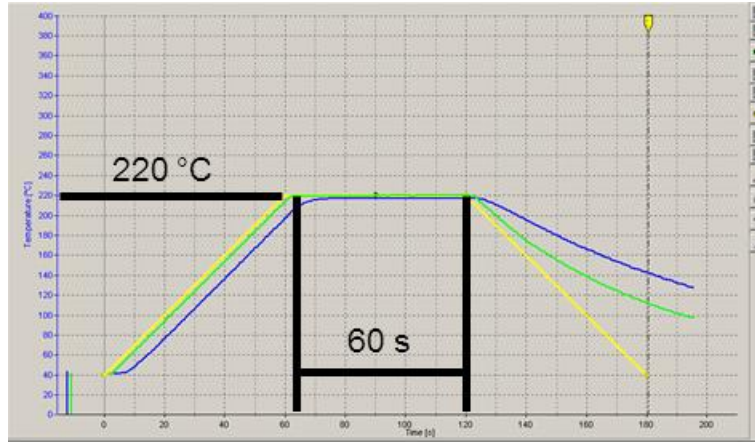
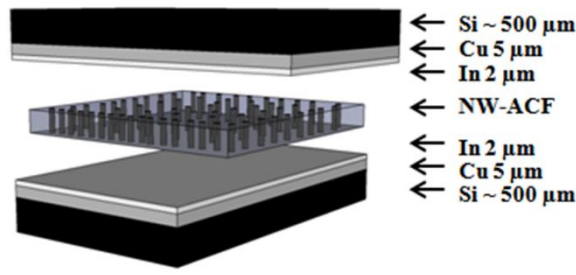


Figure 3.16 A typical temperature profile for NW-ACF bonding.

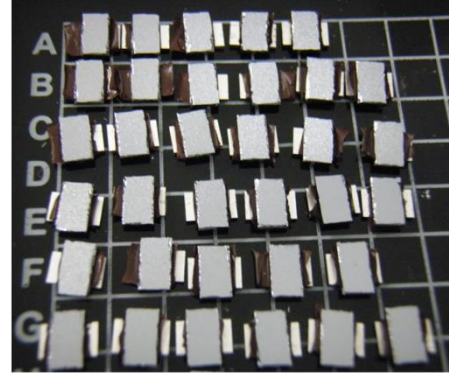
3.6 Electrical Characterization of the NW-ACF Interconnects

3.6.1 Bonding Structure and 4-Point Measurement

To explore the vertical conductivity of the NW-ACF, the initial bonding experiment was carried out by applying the NW-ACF between two metallized Si dies. The test die were prepared by metallizing a 4-inch Ti/Cu seeded wafer with $\sim 5 \mu\text{m}$ thick electroplated copper and $\sim 2 \mu\text{m}$ thick indium, followed by dicing the wafer into individual die of a dimension of $3 \text{ mm} \times 5 \text{ mm}$. Indium was used as the metal finish due to its low melting temperature and ability to form alloys with other metals. This is expected to reduce the contact resistance between the Cu NWs and the bonding surface significantly. With the rectangular shape of the test die, the bonding structure can be arranged as shown in Fig. 3.17 (a), where the top die is flipped and approximately aligned in the center of the bottom die. Then a cut-to-size NW-ACF is sandwiched in between them for bonding. In such manner, the approximate bonding area is $\sim 9 \text{ mm}^2$ and the hanging area of each die can be used for 4-point electrical probing. A group of bonded samples are shown in Fig. 3.17 (b).



(a)



(b)

Figure 3.17 (a) bonding structure of the NW-ACF with two Cu-In metallized die and (b) a group of bonded samples.

The electrical measurement was conducted using an Agilent 34420A Micro-Ohm Meter by connecting four wires of current source and voltage sense to the hanging side of the dies as shown in 3.18. In such way, the 4-point resistance of the NW-ACF as the interconnection between the top and bottom dies can be measured. The current applied during resistance measurement is ± 10 mA. As a preliminary study to understand the bonding and electrical properties of the NW-ACF, an experiment was carried out using NW-ACF A and B, which have a different film thickness (25 and 10 μm , respectively) and a different nanowire density (25.3 % and 6.4 %, respectively).

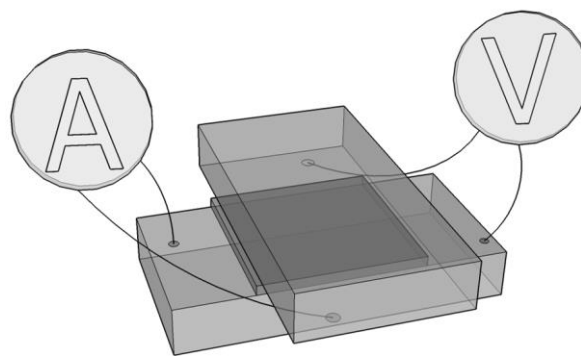
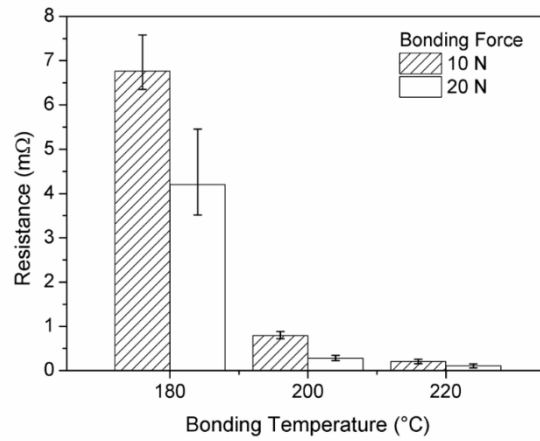


Figure 3.18 Schematics of 4-point probing of a NW-ACF bonded samples.

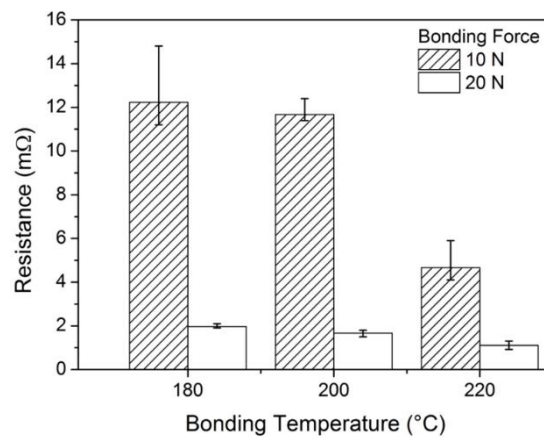
3.6.2 Results and Discussion

The bonding temperature and force play important roles to establish a low contact

resistance during ACF bonding. Three bonding temperatures of 180, 200 and 220 °C and two bonding forces of 10 and 20 N were studied in terms of the interconnection resistance of the NW-ACF A and B, respectively. Fig. 3.19 (a) and (b) shows the trend of the interconnection resistance change of NW-ACF A and B at an increasing bonding temperature and force, respectively. For both types of NW-ACF, the resistance progressively decreased with the increase in bonding temperature or force. The resistance data at each bonding condition is listed in Table 3.3. The minimum resistance achieved by NW-ACF A is $0.1 \pm 0.05 \text{ m}\Omega$, at the highest bonding temperature of 220 °C with a bonding force of 20 N. With the same bonding temperature and force, the minimum resistance achieved by NW-ACF B is about one factor of magnitude higher with a value of $1.1 \pm 0.2 \text{ }\Omega$.



(a)



(b)

Figure 3.19 Interconnection resistance as a function of bonding temperature and force of (a) NW-ACF A and (b) NW-ACF B.

Comparing the two types of NW-ACF, NW-ACF A has generally lower resistance than that of B, which can be attributed to the larger number of nanowires available per bonding area for type A to that of B. The continuous decrease of the resistance by increasing the temperature is probably due to adequate flowing of polymer and indium above the respective glass transition and melting point. NW-ACF A is found to be more sensitive to temperature change from 180 to 200 °C. This is attributed to a larger thickness of the NW-ACF A (3 times thicker compared with NW-ACF B). It is inferred that in case of NW-ACF A, either longer time or higher temperature is required to achieve comparable bonding to NW-ACF B. The influence of the bonding force is also significant on both types of NW-ACFs, especially for the NW-ACF B. Due to the smaller thickness of NW-ACF B, a higher bonding force is required to achieve intimate contact between the NW-ACF and the bonding surface, because a thinner layer compensate to a lesser extent for small surface non-uniformities as compared to the thicker one [47]. The higher bonding force helps to significantly lower the resistance of NW-ACF B interconnects by ~7 times. The resistance data obtained in this work has improved by at least a factor of 10^3 when compared to the previously reported values (1.5 Ω) [173]. The reason for the decrease in the resistance could be due to the employment of the indium metallized bonding substrates and the improved filling percentage of the nanowires in the template. A high filling percentage results in more nanowires capable of making contacts with the indium surfaces and this greatly improves the interconnection resistance of the ACF film.

Table 3.3 Interconnection Resistance of NW-ACF A and B with different bonding force and temperature.

NW-ACF	Bonding Force (N)	Bonding Temperature (°C)	Resistance (m Ω)
A	10	180	6.8 \pm 0.7
		200	0.8 \pm 0.09
		220	0.2 \pm 0.05
	20	180	4.2 \pm 1.1
		200	0.3 \pm 0.06
		220	0.1 \pm 0.05
B	10	180	12.2 \pm 2.2
		200	11.7 \pm 0.6

		220	4.7 ± 1.1
	20	180	2.0 ± 0.1
		200	1.7 ± 0.2
		220	1.1 ± 0.2

3.6.3 Theoretical Model of Interconnection Resistance

The interconnection resistance in this work is defined as the electrical resistance measured between the two die with the 4-point method. This includes the resistance of the metal multilayers, the resistance of the nanowires and the resistance at the bonding interfaces. Fig. 3.20 shows a schematic which represents all of the resistance components in the 4-point measurement system. The interconnection resistance is composed of two Cu-In metal multilayer resistances R_{Cu-In} , the resistance of the nanowires R_{NW} and two contact resistances $R_{Contact}$. R_{Sheet} are the sheet resistances generated by the distance from the probes to R_{Cu-In} , which are excluded from the 4-point measurement.

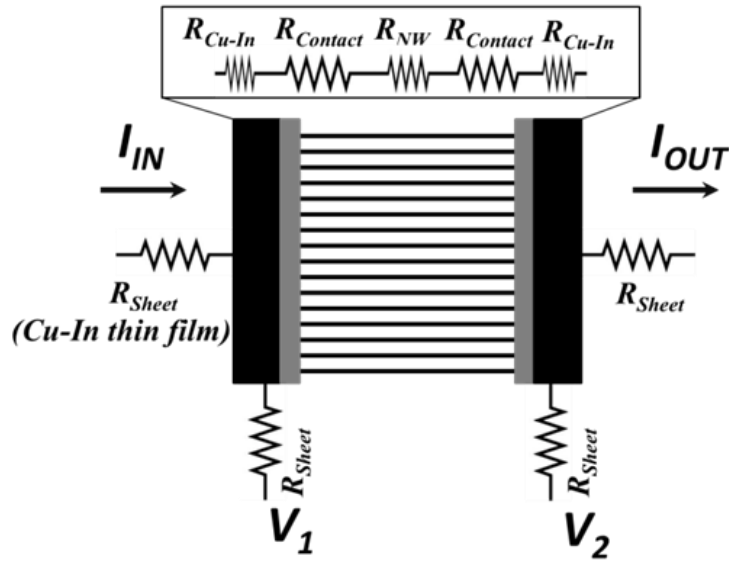


Figure 3.20 Schematic of all resistance components in the 4-point measurement.

The resistance of the metal multilayer R_{Cu-In} is defined as a function of the composite material resistivity ρ_{Cu-In} and the effective length L and cross-section area S by

$$R_{Cu-In} = \frac{\rho_{Cu-In} \times L}{S} \quad (3.2)$$

where L is 7 μm (thickness of Cu-In multilayer) and S is 9 mm^2 (die bonding area). The resistivity value $\rho_{\text{Cu-In}}$ used for the Cu-In multilayer in this work is derived from a comparable study by Parretta et al. [190] at a value of $1.4 \times 10^{-6} \Omega\cdot\text{m}$. Therefore, the calculated resistance of $R_{\text{Cu-In}}$ is $1.1 \times 10^{-6} \Omega$.

The resistance of nanowires R_{NW} per bonding area is calculated as the parallel resistance of the number of nanowires in the given area by:

$$R_{\text{NW}} = \frac{4 \rho_{\text{NW}} L}{\pi D^2 n} \quad (3.3)$$

where ρ_{NW} is the resistivity of Cu nanowire, L is the length, D is the diameter of the nanowires and n is the number of the nanowires per bonding area. For Cu nanowires of 200-nm diameter, the one-dimensional effect is not significant, because the Cu NW diameter is much larger than the Cu mean free path of ~ 39 nm at room temperature [150]. Therefore, ρ_{NW} in the calculation is approximated as the resistivity value of bulk Cu ($1.71 \times 10^{-8} \Omega\cdot\text{m}$). By incorporating the nanowire diameter and length in Eq. (3.3), the calculated resistance of a single nanowire in NW-ACF A and B is 13.5 Ω and 5.4 Ω , respectively. The theoretical number of the NWs available for bonding at the 9 mm^2 bonding area was calculated based on the apparent filling ratio given in Table 3.2, assuming that only protruding nanowires in the film will make contact to the bonding surface. This results in the number of nanowires of 2.9×10^7 and 7.5×10^6 per 9 mm^2 area for the NW-ACF A and B, respectively. According to Eq. (3.3), the calculated values for R_{NW} is given in Table 3.4, being $2.8 \times 10^{-7} \Omega$ and $7.2 \times 10^{-7} \Omega$ for NW-ACF A and B, respectively.

Table 3.4 Theoretical calculation of the resistance of NW-ACF

NW-ACF	NW diameter (nm)	NW length (μm)	Resistance per single NW (Ω)	Number of NWs per 9 mm^2 area	R_{NW} per 9 mm^2 area (Ω)
A	220	30	13.5	2.84×10^7	4.8×10^{-7}
B	200	10	5.4	7.45×10^6	7.2×10^{-7}

By comparing the measured resistance data to the theoretical resistance, it was found that the theoretical values of both $R_{\text{Cu-In}}$ ($\sim 10^{-6} \Omega$) and R_{NW} ($\sim 10^{-7} \Omega$) were several factors lower

than the measured resistance values for both NW-ACFs (10^{-4} - $10^{-3} \Omega$). It is thereby concluded that the resistances associated with the contact behaviour of the nanowires (i.e. the actual number of the connected nanowires) and the contact resistance between individual nanowires and the bonding surface can be the major contributing factors to the interconnection resistance in the NW-ACF bonded sample.

3.7 Contact Mechanism of the NW-ACF

3.7.1 Bonding Interface Analysis

To understand the microstructure of the bonding interface, cross-sectional samples were prepared using micro-sectioning method with grinding and polishing. The grinding was accomplished using waterproof silicon carbide grinding paper with various grit sizes, from coarse to fine; while the polishing was conducted with the soft cotton polishing paper and a polishing lubricant was dispensed to achieve the structural morphology with a desired fineness.

Fig. 3.21 shows the micro-sectioned images of the bonded samples with NW-ACF A (a) and B (b) at the bonding condition of 200 °C, 20 N. The different layers in the bonding system were scanned by the EDS line scan spectra. From the images, the bond lines at the interfaces of both samples were found intact without any gaps or voids. This indicates that a good flow occurred between indium and polymer at the given temperature and bonding force. The nanowires (the white lines in the image) were found to be vertically connected between the two surfaces. However, some connection between NWs and the surface could have been broken during the polishing process. For both types of NW-ACF, some polymer gaps were seen in the interface area. Two possible reasons account for this: 1) NWs in that area were not grown up to the surface and 2) as the polymer can flow under a temperature above T_g , an insulating layer of the polymer can flow in the gap between the NWs and the surface at an applied force. Due to these insulation gaps, the nanowires cannot form a proper electrical contact with the bonding surface in these areas. Therefore, the actual number of the NWs that make a connection can be far less than the number of NWs in the film.

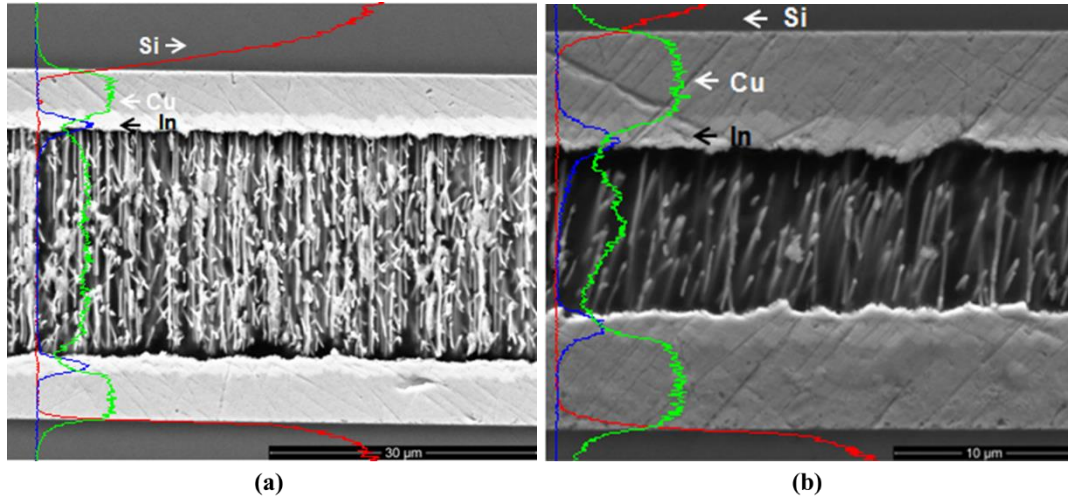


Figure 3.21 SEM image and EDS line scan of the cross-sectional area of the bonded sample with (a) NW-ACF A and (b) NW-ACF B.

3.7.2 Contact Mechanism of Single Nanowire

To visualize a direct contact formed between the Cu NW and the In surface, a micro-sectional sample was carefully prepared by dissolving the polycarbonate surrounding the NWs. A typical image after sample preparation is shown in Fig. 3.22. One of the nano-contacts formed between a single NW with the top surface was found and marked in the image. A lot of these joints could have been broken during the sample preparation process. Due to the resolution limits of SEM and EDS analysis, the nanostructural and compositional information of this kind of contact will need advanced microscopic analysis to solve it. It should also be noted that the grainy surface of the nanowires seen in this image may be due to the present of Cu oxides formed on the nanowires during sample preparation. While for NW-ACF bonding, the Cu oxides can be removed using diluted sulfuric acid treatment and then properly rinsed by DI water and nitrogen-dry before bonding.

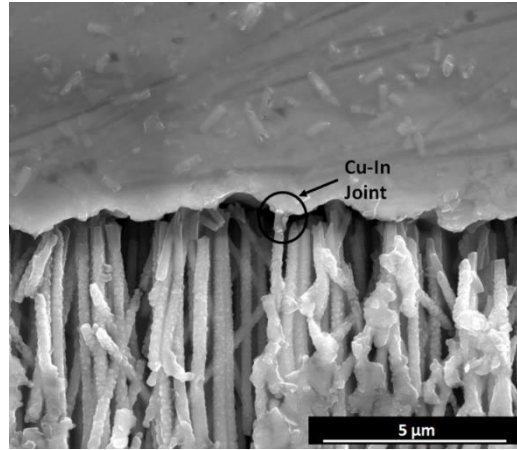


Figure 3.22 SEM image showing a NW joint with In surface after dissolution of the polycarbonate in a micro-sectional sample.

3.7.2.1 Nanostructure and Compositional Analysis of the Nano-contact

To understand the nanostructure of the contact formed between the NW and In surface and to verify the elemental composition of this contact, a cross-sectional lamina of the bonding interface area was prepared using focused ion beam (FIB, FEI Dual Beam FIB Helios Nanolab 600i) and further analyzed by scanning transmission electron microscopy energy-dispersive X-ray spectroscopy (STEM-EDS) element mapping. Fig. 3.23 (a) shows the dark-field STEM image of the FIB prepared sample.

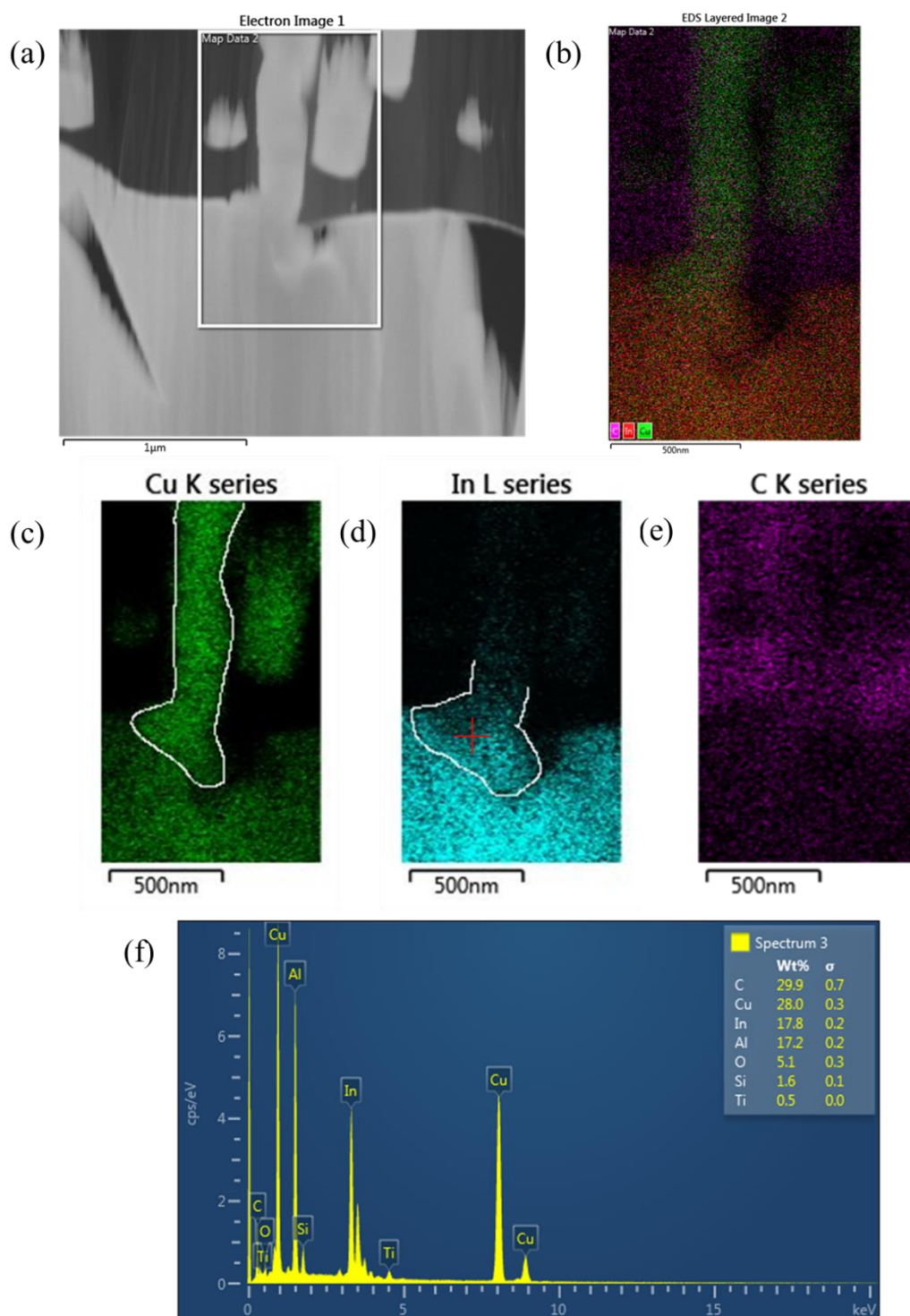


Figure 3.23 STEM-EDS analysis of the contact interface of the Cu-NW to In surface (a) dark-field STEM image of the contact interface, (b)-(e) EDS elemental mapping images of the combined and single element distribution of Cu, In and C and (f) EDS spectrum image showing the element composition in the detected image area (note that Al, Si, Ti signals are seen as the machine noise).

A single NW can be seen to form a close contact with the underneath In surface. By conducting EDS mapping analysis, the element distribution of Cu, In and C corresponding to the marked area of (a) is shown in Fig. 3.23 (b)-(e), where (b) shows the combined element map and (c)-(e) show the single elemental distribution of Cu, In and C. In both combined and single element mapping images, the contours of the Cu NW, In surface and the contact interface between them can be well distinguished. The contour of the Cu NW is displayed in the image (c) and contour of the area with both high density Cu and In is displayed in the image (d). Carbon element distribution representing the polymer distribution surrounding the NW is shown in the image (e). To obtain the element ratio of Cu:In within the contoured area in (d), the EDS spectrum analysis was conducted and the result is shown in the graph (f). From the graph, clear Cu and In peaks were observed. The atom ratio of Cu and In is 28.0:17.8 and is very close to the ratio of the Cu-In alloy of $\text{Cu}_{11}\text{In}_9$ (Cu:In is 11:9). It is reported that In can form the metastable CuIn_2 phase in equilibrium with Cu at near room temperature and completely transfer to the stable $\text{Cu}_{11}\text{In}_9$ compound phase during a thermal treatment [190]. Both the EDS mapping and spectrum analysis confirms the Cu-In diffusion in this contact and the alloy of $\text{Cu}_{11}\text{In}_9$ is likely to be formed.

3.7.2.2 XRD Analysis of the NW-ACF Film

To identify the crystal phase of the Cu NWs in the polymer and to confirm the constitution of the Cu-In alloys, X-Ray Diffraction (XRD) analysis was conducted using XRD instrument (Philips X'pert PW3710-MPD diffractometer) with filtered $\text{Cu-K}\alpha$ ($\lambda = 1.54 \text{ \AA}$) radiation, operating at 45 keV and 40 mA. The test sample for XRD analysis was the NW-ACF film detached from the bonded sample. In such film, Cu NWs are left embedded in the template and the contact parts of the Cu NWs are expected to be broken during detachment and remain as the small segments in the NW tips.

Fig. 3.24 (a) shows the XRD spectrum of the NW-ACF film after bonding and the major diffraction peaks are labelled as the small lines on top of the graph. The diffraction peaks (numbered 1-7) are compared with the standard patterns of Cu and the Cu-In alloys using the respective JCPDS (Joint Council for Powder Diffraction Studies) cards, as shown in Fig. 3.24 (b). By comparing to the standard Cu pattern (04-0836), three diffraction peaks (number 1, 3, 7) at 2θ scattering angles of 43.28° , 50.41° and 74.17° are assigned to the (111), (200) and (220) crystal planes of cubic-phase Cu respectively. The results are in agreement with the work reported by Duan et al. [191] for the electrodeposited Cu nanowires in the template.

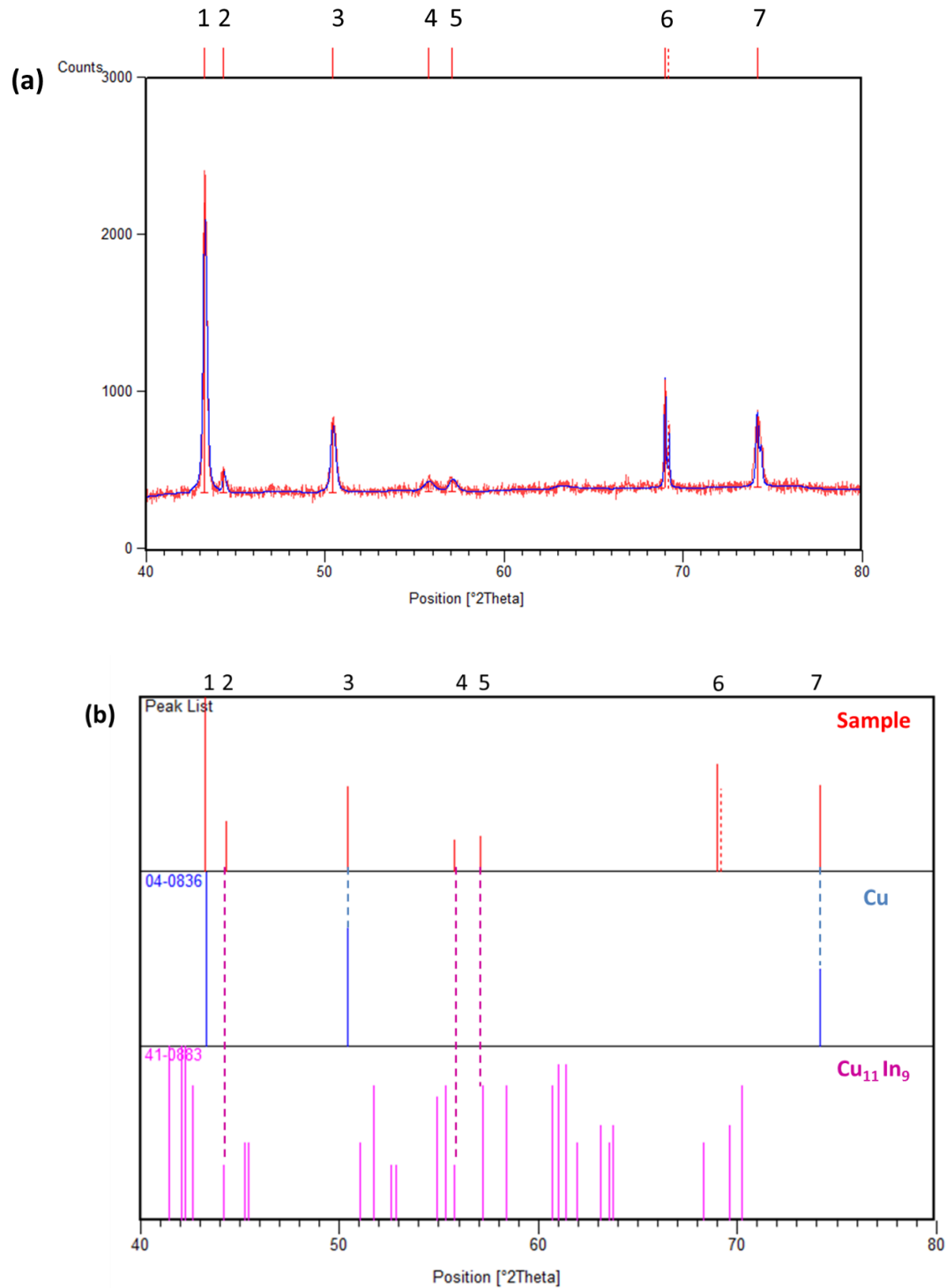


Figure 3.24 XRD spectrum analysis of the detached NW-ACF film after bonding (a) the diffraction pattern of the NWs in the detached film and the Bragg peak positions and (b) the Bragg peak list as compared to the standard pattern of Cu (JCPDS card No., 04-0836) and Cu₁₁In₉ (41-0883). The dotted lines are drawn to guide the eye.

The relatively intense peak of (111) demonstrates that the NWs possess a strong (111) growth direction. The other peaks in the obtained spectrum are further compared to the standard pattern of Cu-In alloys. Among them, the standard $\text{Cu}_{11}\text{In}_9$ pattern (41-0883) shows the best match to three peaks (number 2, 4, 5) at 2θ scattering angles of 44.35, 55.79 and 57.11 °, which are assigned to the (40-1) (11-3) and (423) crystal planes of monoclinic $\text{Cu}_{11}\text{In}_9$ respectively. The other strong peak (number 6) found at 2θ scattering angles of 69.01 ° is corresponding to the (100) Si [192]. During sample preparation, some Si residue can be left on the sample. As a result, the XRD data confirms the formation of $\text{Cu}_{11}\text{In}_9$ during NW-ACF bonding at the contact point of Cu NWs and In.

3.7.3 Contribution of Contact Resistance

The other factor contributing to the interconnection resistance of the NW-ACF is contact resistance of Cu NWs to In. A comparable study was reported by Diop et al. [128] with the ACF based on vertical fibers where the contact resistance of such an ACF under a compression interconnect system was found to be the major contributor in the total resistance. In this work, the NW-ACFs were bonded under both pressure and heat. From TEM and XRD analysis, it has been confirmed that the single NW can be penetrated into In surface to make the contact and the In atoms can diffuse into the Cu NW and form $\text{Cu}_{11}\text{In}_9$ alloy. From Fig. 3.23 (d), the cross-sectional dimension of such an alloy joint is about 750×250 nm. As the length of such a joint (250 nm) is much smaller than the NW length (10 μm), the contribution of the resistance caused by such an alloy joint can be negligible when compared to R_{NW} . However, there could be other contact modes of the NW that result in different contact resistances. Fig. 3.25 shows schematics of three contact modes which could occur during NW bonding. The first penetration mode refers to the tip of the NW penetrating into the bonding surface due to the external force and this can result in the minimum contact resistance, especially when Cu and In also diffuse into each other. The second mode is the elastic contact formed between the NW and the surface. In this case, the constriction resistance [193] should be accounted for the contact resistance. The third mode refers to a thin layer of polymer or an oxidation layer existing between the two contact surfaces. In this case, the quantum mechanical tunnelling of electrical current takes place and this can significantly increase the contact resistance by adding to the tunnelling resistance [96]. Therefore, the higher the number of NWs in penetration contact mode, the lower the contact resistance. One method to improve the penetration of the wires to the bonding surface and to avoid the tunnelling

resistance caused by the trapped polymer is to prepare the NW-ACF with a large number of protruding NWs from the template. With such structure, the NWs are able to contact the bonding surface before the polymer layers start to flow and form the gaps.

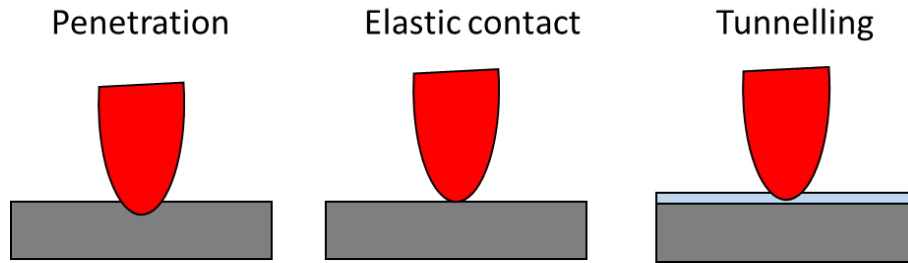


Figure 3.25 Schematics showing the three contact modes of the NW to the bonding surface.

3.8 Die Shear Strength of the NW-ACF Interconnects

3.8.1 Test Setup

Die shear test was carried out with a JOYCE 552 Bond Tester. The bonded sample was fixed in the support and the shear tool with a 20-kg cartridge was placed parallel to the edge of the top chip as shown in Fig. 3.26. The shear tool moved at a speed of 25 $\mu\text{m/s}$ in the horizontal direction until the maximum shear force occurred when the top die was detached from the bottom one. The shear force was recorded and displayed in units of kilogram force (kgf). In the experiments, the die shear test was conducted to investigate the influence of bonding temperature and force on the shear strength of bonded samples with NW-ACF A and B.

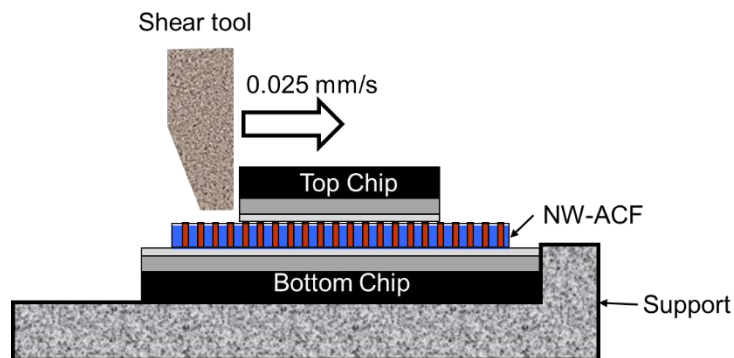


Figure 3.26 Schematic of die shear test for the NW-ACF bonded sample.

3.8.2 Results and Discussion

Fig. 3.27 shows the shear strength values plotted for NW-ACF A and B bonded samples in terms of bonding temperature and force. It was found that both the temperature and the force have a positive influence on the shear strength.

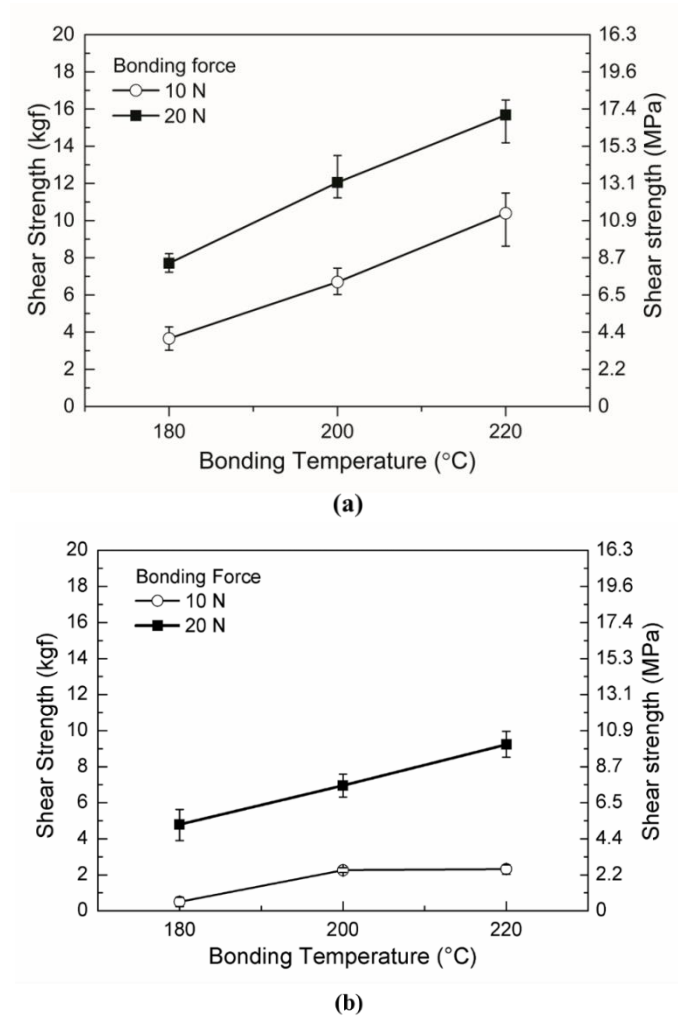


Figure 3.27 Shear strength as a function of temperature and force of (a) NW-ACF A and (b) NW-ACF B.

For NW-ACF A, the shear strength shows a nearly linear increment with the increased temperature for both force variations. With a higher bonding force of 20 N, the maximum shear strength was achieved at 15.7 ± 1.3 MPa. Compared to NW-ACF A, the shear strengths of NW-ACF B are generally lower. The linear increase trend of shear strength with the increasing temperature is valid for NW-ACF B at a bonding force of 20 N. At a bonding force of 10 N, the shear strengths are generally low for NW-ACF B and the influence of the temperature is limited. The maximum average shear strength was achieved by NW-ACF B at

the highest bonding condition (220 °C, 20N) and is 9.2 ± 0.7 MPa. The die shear strength values of the NW-ACFs are comparable to the values of the conventional ACFs, which are ranging from 5-15 kgf per 9 mm² bonding area (equal to 5.4-16.3 MPa) according to the study by Jang et al. [87] .

The shear strength of the ACF bonded samples is mainly dependent on the adhesion strength of the polymer matrix. At a higher temperature, the polymer reaches a low enough viscosity that it can reflow sufficiently and redistribute at the bonding interface. A higher bonding pressure helps to deform the polymer, and this enables it to adapt to the surface topography and thickness non-uniformities [47]. However, to have a bonding temperature and pressure that is too high is not desirable due to the resultant high thermal and mechanical stress in the bonded samples. The ACF thickness can also affect the adhesion strength. A thicker polymer layer can more easily reflow around the surface structures; while a thinner one compensates to a lesser extent for non-uniformities of bonding surfaces [47] or non-planarity induced during bonding process. Another reason is that a thicker film would absorb a higher amount of plastic and elastic energy compared to the thinner ones and therefore it could withstand higher shear force [177]. In a good agreement with the above explanation, NW-ACF A in this work resulted in a higher shear strength than that of B due to the larger thickness of the film.

3.8.3 Fracture Surface Analysis

To understand the fracture mode of the NW-ACF, it is essential to study the fracture surface of the sheared samples. During die shear test, most fractures occurred at the interface of NW-ACF and the top or bottom die. Fig. 3.28 (a) shows a typical shear surface of NW-ACF B detached from the top die, which was bonded under 200 °C, 60s, 20 N. The rough fracture surface indicates that a gross plastic deformation took place during fracture. This demonstrates a good adhesion formed between the polymer and the bonding surface. However, some relatively smooth areas were found in the fractural surface as shown in Fig. 3.28 (b). It is speculated that an inadequate adhesion of the NW-ACF to the bonding surface formed in this area. One reason for that would be the curling of the NW-ACF due to internal stress after electrodeposition and that no lamination process of the film was conducted before bonding (due to the lack of tackiness of the polycarbonate film). Secondly, the levelling of the bonding force would be limited by the bonding system. A similar fractural mode was also found with the NW-ACF A.

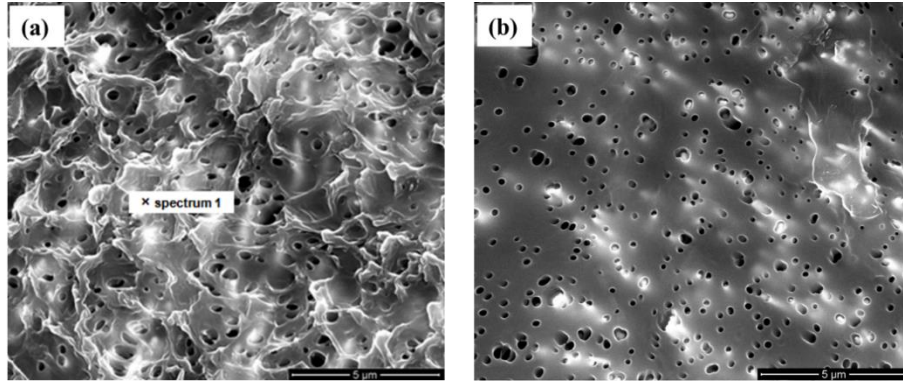


Figure 3.28 SEM images showing the fractural surface of the NW-ACF (a) the good adhesion area with a rough fractured surface and (b) an inadequate adhesion area showing a smooth surface.

3.9 Conclusions

In this chapter, the fabrication process of Cu NW-ACF with the developed overgrowth-stripping method was described. A high filling ratio of Cu up to 100% was achieved for all polycarbonate templates as selected. One potential problem observed with the commercial templates is the non-parallel and overlapping pores in the template. These were observed by observing the microstructure of the nanowire arrays. The fabricated NW-ACF was investigated using thermal analysis for glass transition point, thermal stability and dynamic mechanical analysis. The results show that the polycarbonate based NW-ACF has a glass transition range at 150-160 °C and a good thermal stability (low weight loss) up to 400 °C. The storage modulus of the NW-ACFs are > 1.4 GPa at a temperature < 140 °C, which is comparable to the conventional ACF.

Thermocompression bonding was applied for NW-ACF bonding with Cu-In metallized dies. The influence of bonding conditions (bonding temperature and force) was studied in terms of interconnection resistance and shear strength. It was found that the increase of the temperature and force generally result in a low interconnection resistance and a high shear strength for the NW-ACF interconnects. The minimum interconnection resistance of ~ 0.9 m Ω .mm² and the maximum shear strength of ~ 17 MPa can be achieved by the NW-ACF with a higher nanowire density and a larger film thickness. By conducting the STEM-EDS analysis of the FIB prepared cross-sectional sample of the Cu-NW/In bonding interface, the contact mode of the nanowire to the bulk surface was characterized and by conducting XRD

analysis, the formed $\text{Cu}_{11}\text{In}_9$ alloy is confirmed in the Cu-NW/In joint. These promising results lead to further study in exploring the fine pitch potential of NW-ACF. This will be discussed in the following chapter.

Chapter 4 Nanowire ACF for Fine-Pitch Interconnection

4.1 Introduction

In this chapter, the fine pitch capability of Cu NW-ACF was investigated with the fine-pitch test modules. Test chip modules including daisy-chain, 4-point and insulation test structures were designed with four different pad/pitch variations with the stressing pad/pitch size down to 10/30 μm . A test wafer with bond pads composed of ~ 3 μm thick Cu and ~ 1 μm thick In was fabricated by photolithography and electroplating process. Template related open/short failures were evaluated for the three NW-ACFs using the test module with the largest pad/pitch size of 80/160 μm . The NW-ACF with both Z-axis conduction and X-Y direction insulation was subjected to further testing with ultra-fine pitch test modules. The effects of bonding temperature and bonding force on the electrical performance of the NW-ACF interconnects were studied and the corresponding bonding interfaces were analyzed and compared.

The other part of the study focuses on the NW-ACF interconnects formed with the Au bumpless pads. The electrical performance and the resultant bonding interfaces were studied and compared to the particle-ACF based interconnects. The RF properties of the NW-ACF were evaluated with an RF test module and compared to solder based interconnects. Thermal performance of the NW-ACF interconnects was studied by thermal impedance measurement and compared to the particle-ACF based interconnects.

4.2 Fine-Pitch Interconnects Formed with NW-ACF and Cu-In Pads

It was shown experimentally in the previous chapter that the NW-ACF can form a low resistance interconnection with the Cu-In metallized die. However, the fine-pitch capability of the NW-ACF can only be evaluated with the test die with the fine-pitch bond pads. In this

section, the designed test chip, the Cu-In bond pad fabrication and the bonding experiments of the NW-ACF with the test chips are described and the test results are given and discussed.

4.2.1 Daisy-chain Test Chip Design

The stacked test chip modules with daisy-chain, 4-point and insulation test structures were designed to electrically characterize the Z-axis interconnection resistance and X-Y direction insulation property of the fine-pitch interconnects formed by NW-ACF. Fig. 4.1 shows the layout of the bottom and top chip design by CleWin software [194]. The 100 daisy-chain square bond pads are placed in the centre of both top and bottom chip with the same pad and pitch size. The Kelvin connected probing pads are placed in the bottom chip for probing purposes at different daisy-chain intervals, which are pad numbers 2, 6, 8, 10, 30, 60, 96, 98 and 100. There are four variations of the daisy-chain test modules that have different bond pad size and pitch, with the specifications listed in Table 3.1. All test modules have a bottom chip size of $5\text{ mm} \times 5\text{ mm} \times 0.5\text{ mm}$. For test module 1 and 2, with a larger pad/pitch size of $80/160\text{ }\mu\text{m}$ and $40/80\text{ }\mu\text{m}$, have a top die dimension of $2.5\text{ mm} \times 2.5\text{ mm} \times 0.5\text{ mm}$. While for test module 3 and 4, with a smaller pad/pitch size of $20/40\text{ }\mu\text{m}$ and $10/30\text{ }\mu\text{m}$, have a top chips dimension of $1.1\text{ mm} \times 1.1\text{ mm} \times 0.5\text{ mm}$.

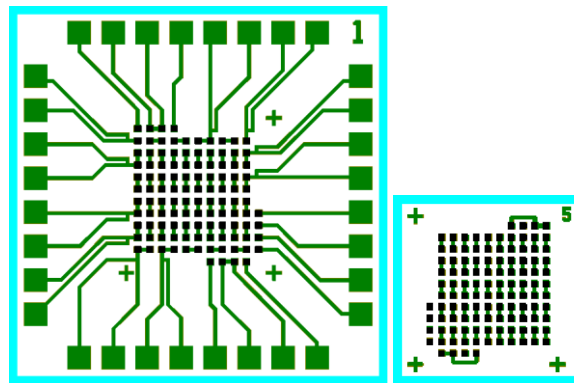


Figure 4.1 Layout of daisy-chain test module containing 100 daisy-chain pads, two 4-point test structures and four insulating pads (die 1 is bottom die and die 5 is corresponding top die).

Table 4.1 Specifications of the pad geometry.

Daisy-chain Test module	Number of Daisy chain contacts	Number of 4-point structures	Number of Insulating pads	Square Bond pad width (μm)	Bond pad pitch (μm)
1	100	2	4	80	160
2	100	2	4	40	80
3	100	2	4	20	40
4	100	2	4	10	30

Meanwhile, two 4-point structure and four unlinked pads are placed in the periphery of the daisy-chain pads to enable 4-point single interconnect measurement and insulation tests to be performed. The principle of the 4-point structure for single interconnect measurement is illustrated in Fig. 4.2 (a), where the voltage/current is applied between V_1/I_1 and V_2/I_2 and the voltage drop is measured between V_3 and V_4 . For the insulation test, the neighbouring NW-ACF interconnects with unlinked bond pads are shown in Fig. 4.2 (b), where the voltage/current is applied between V_1/I_1 and V_2/I_2 and the leakage current I_{leak} is measured between the two points.

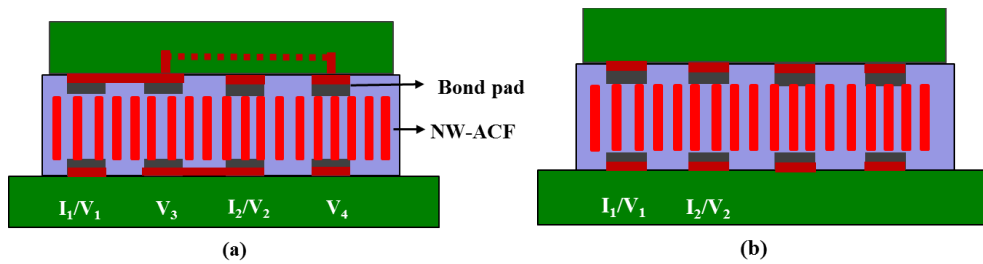


Figure 4.2 Schematics showing (a) 4-point single interconnection resistance structure and (b) insulation test structure.

4.2.2 Test Wafer Fabrication

The test wafer containing daisy-chain and other test modules was fabricated using a 4-mask wafer fabrication process, as shown in Fig. 4.3. The 4-mask process mainly consists of:

- 1) Cu electroplating process with the first photoresist (PR) mask to form the base metal of pads and tracks,

- 2) the In electroplating process with second PR mask to form the bond pad finish of In,
- 3) Cu seed layer etching process with the third PR mask to remove the residue metal and insulate the structures,
- 4) SiO₂ passivation process by sputtering a thin layer of SiO₂ on the whole wafer area and patterning the pad area with the fourth PR mask to create open windows for the dry etching process.

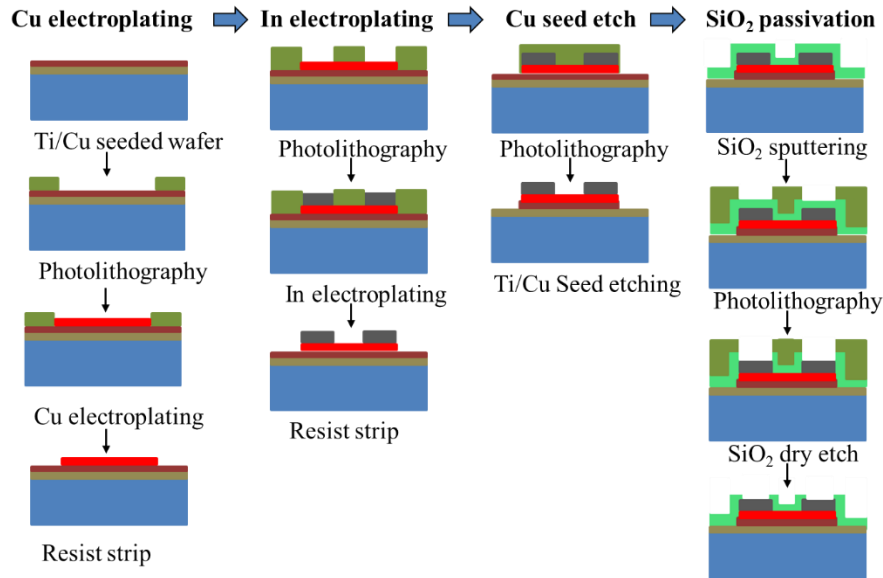


Figure 4.3 Schematic representation of the process flow of the test wafer.

The detailed process is as follows. The oxidized 4-inch Si wafers were sputtered with Ti (20 nm) and Cu (100 nm) layers, as adhesion and seed layer, respectively. The pattern for Cu plating was created by a photolithography process with a relatively thick ($\sim 9 \mu\text{m}$) AZ 9260 photoresist, which was used as through-plating resist. A set value of $3 \mu\text{m}$ thick Cu was electroplated using a commercial Cu bath through the photoresist pattern. The actual thickness of the electroplated Cu was measured by KLA-Tencor profilometer to be $3\text{-}3.5 \mu\text{m}$. Then the 2nd photolithography was carried out with the corresponding PR mask for In plating. In was deposited in a commercial In sulfamate plating bath (from Indium Corporation) by applying a small current density of $\sim 1 \text{ mA/cm}^2$ using a two electrode cell at room temperature and the deposited thickness was measured to be $1\text{-}1.5 \mu\text{m}$. Plasma treatment with 1.5 mL/min O_2 flow was carried out before each electroplating procedure to ensure the cleanness of the surface. In was only deposited on bond pads and serves as the bonding layer to the Cu nanowires in the NW-ACF. The photolithography-based wafer-level electroplating

requires accurate process control in order to get the desired thickness and an acceptable roughness of the metallized surface. It was found that an appropriate surface cleaning and wetting are essential before plating and a low plating current density should be applied to allow the deposition through the relatively thick photoresist. After electroplating, the Ti/Cu seed layer in the non-patterned area should be removed. Again, the 3rd PR mask was applied before chemical etching to protect the electroplated Cu and In area. Then, the Cu and Ti seed layer was subsequently etched by ammonium sulfate ((NH₄)₂SO₄) and buffered hydrofluoric acid (BOE) solution. To avoid over-etching, the immersion time of the wafers in the etchant was controlled carefully. The final step was passivation, which involves a 200 nm thin SiO₂ layer sputtered on the whole wafer. A dry etch process was then used to open the access windows for the bond and probe pads with the 4th PR mask. A representative SEM image of the fabricated test structure on a Si chip is shown in Fig. 4.4 (a). No over-etch or metal residues were observed. Fig. 4.4 (b) shows a tilted SEM image of a magnified bond pad (80 × 80 μm²), where the top In layer was deposited on the underneath Cu layer with 2 μm tolerance designed on each width side for the mask alignment. The topography image also shows a certain degree of the surface roughness of the electroplated In.

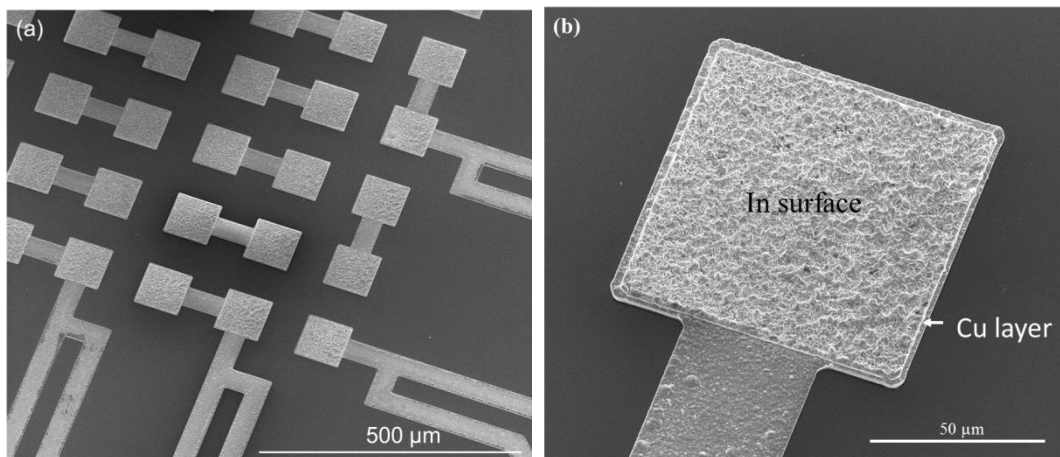


Figure 4.4 SEM top images of the fabricated test chip (a) daisy chain pattern and (b) the morphology of a bond pad surface.

4.2.3 Thermocompression Bonding

The interconnections between the bottom and top chips were achieved by interposing the NW-ACF between two chips using thermocompression bonding. Due to the fine pitch

structure of the test chips, alignment is critical for achieving a successful bond. It is reported that the open and shorting probability increases abruptly after misalignment for ACF joints [99]. The other issue with ACF bonding is non-planarity, which can create an uncontacted bonding area due to an uneven distribution of the bonding force [100, 195]. Fig. 4.5 shows the captured alignment images of the daisy-chain test module 1 (with the largest pad/pitch size of 80/160 μm) and test module 4 (with the smallest pad/pitch size of 10/30 μm) by the process camera in the bonding system. Even with the smallest pitch size designed in this work, good alignment can be achieved with the bonding system. To ensure a good coplanarity of the assembled dies, the bonding system needs to be carefully calibrated before the bonding experiments. Since the die has a considerable surface topography due to the bond pads structure, the coplanarity within the bonding area is very critical and has an influence on the bonding yield. After alignment, a cut-to-size NW-ACF film (with a dimension larger than the top die) was gently placed on the bottom die for final bonding process. The bonding parameters, i.e. bonding temperature and force, were adjusted in the experiment to understand their effects on the formed interconnects. Three bonding temperatures, 180, 200 and 220 $^{\circ}\text{C}$ were evaluated with test module 1 and a bonding force ranging from 1.5 to 10 N was evaluated using all four test modules.

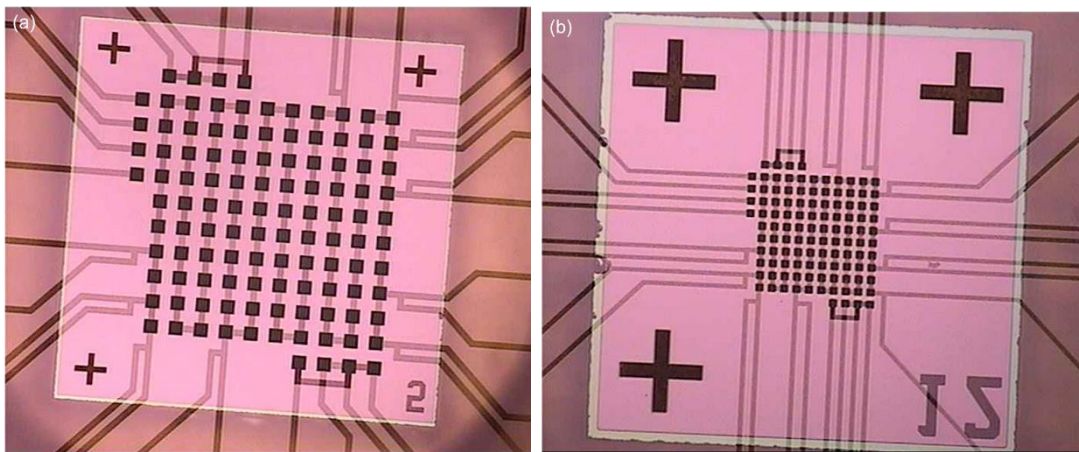


Figure 4.5 The captured image of chip alignment during bonding, (a) the alignment with pad/pitch size of 80/160 μm and (b) the alignment with the pad/pitch size of 10/30 μm .

4.2.4 Template Related Open/Short Failures

The electrical properties (Z-axis conduction and X-Y direction insulation) of the three NW-ACFs (as described in Chapter 3.3) were evaluated by the test module 1 (80/160 μm

pad/pitch size). The open and short failures were measured by 2-point method with a multimeter. An open failure for the daisy-chain interconnects is defined as the measured resistance $> 1 \text{ k}\Omega$ and a short failure probed between two insulated pads was screened by the continuity test. The bonding experiments for all three NW-ACFs were carried out with the optimized bonding temperature and time ($220 \text{ }^{\circ}\text{C}$ and 60 s , based on the test results in Chapter 3.6.2) and a relatively large bonding force of 15 N to ensure a sufficient contact. The measurement results of the bonded samples are shown in Table 4.2, where NW-ACF A shows short failure by probing the insulation pads and NW-ACF B shows open failure by probing the pads connected with the daisy-chain interconnects. In contrast, NW-ACF C showed none of the short and open failures that occurred using NW-ACF A and B. NW-ACF C was therefore considered as an electrically workable ACF material for further electrical characterization.

Table 4.2 Electrical screening of the fine-pitch interconnects formed with three NW-ACFs.

	NW-ACF A	NW-ACF B	NW-ACF C
Daisy-chain Conduction Test	PASS	FAIL	PASS
Insulation Test	FAIL	PASS	PASS

(NW-ACF A, B and C from Table 3.2)

To understand the failure mechanisms of NW-ACF A and B, cross-sectional samples were prepared for bonding interface analysis. Figure 4.6 (a) to (c) compares the bonding interfaces of the three NW-ACFs. For NW-ACF A in Fig. 4.6 (a), due to the high volume fraction ($\sim 25\%$) and the long length of the nanowires in this NW-ACF, the vertical compressive force were mainly loaded on the nanowires due to their high modulus of elasticity. This ensures a good contact between the nanowires and the bonding surfaces. However, the high density nanowires result in laterally interconnected nanowire networks, and this accounts for the short failures in the fine-pitch interconnects. In comparison, the nanowires in NW-ACF B in Fig. 4.6 (b) have a smaller length and a lower density. Nevertheless, polymer gaps were found in the interface areas between the nanowires and the bonding surfaces, and this causes the open interconnects. The polymer gap can be attributed to the rough surface of the corresponding template, where the protruding areas of polymer may flow over the nanowire ends and block the contacts during bonding. Moreover, the nanowire density of NW-ACF B

is the lowest among the three NW-ACFs ($\sim 6.4\%$), and this may also contribute to a number of open failures. Figure 4.6 (c) shows the bonding interface of the NW-ACF C, where the bondline thickness of the film is much smaller than that of NW-ACF B, which is due to a lower modulus of the film at high temperature. This results in the highly deformed nanowires to make sufficient contact with the bonding surfaces. In NW-ACF C, the nanowire density ($\sim 12.5\%$) is neither too high to result in the nanowire networks, nor too low to effect the proper contact formed between the nanowires and the bonding surfaces. Therefore, it is the most suitable being fine-pitch interconnection material among the three tested template samples.

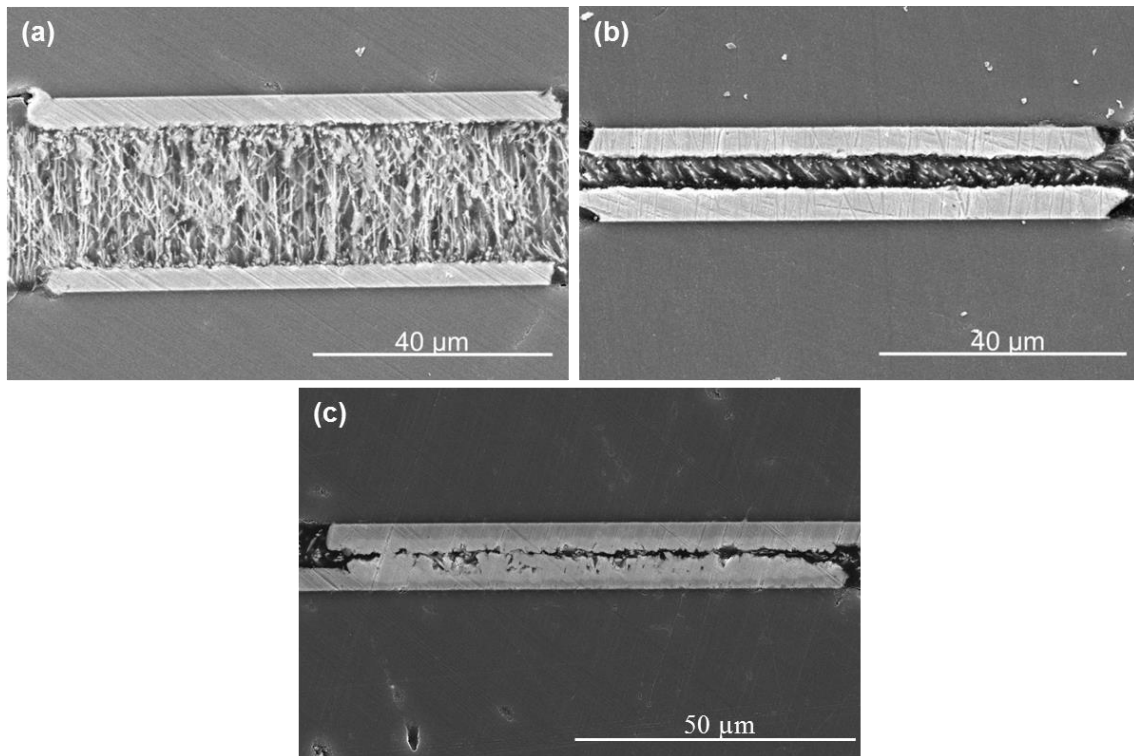


Figure 4.6 Bonding interfaces of three NW-ACF interconnects, (a) NW-ACF A, (b) NW-ACF B and (c) NW-ACF C (bonding condition: 220 °C, 15 N, 60 s).

4.2.5 Electrical Measurement and Daisy-chain Resistance

The interconnection formed by NW-ACF C (bonded at 220 °C, 15 N, 60 s) was subjected to full electrical characterization with the 4-point Kelvin probing using a Cascade manual probe station and Agilent B1500A Semiconductor Device Analyser. The 4-point measurement was set up by connecting four source/monitor units (SMUs) of the instrument as voltage force and sense, separately. SMU 1 and 2 were connected as voltage force and

SMU 3 and 4 were connected to sense the voltage drop. Fig. 4.8 shows the schematic of the 4-point measurement for two connected daisy chains. It should be noted that with this probing structure, a small part of the track and the bond pad resistance (between SMU 3 and 4) can be included in the measurement. For each measurement, the forcing voltage started from -100 mV to 100 mV with steps of 1 mV. The current flow from SMU 1 to SMU 2 and the voltage drop between SMU 3 and 4 were recorded to generate the I-V curve.

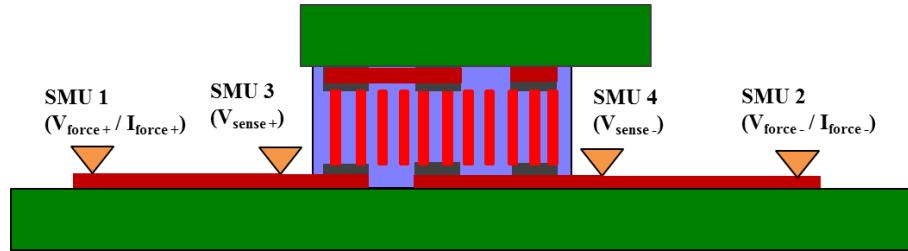


Figure 4.7 Schematic showing the 4-point kelvin probing for daisy-chain resistance (two connected chains probed in this case). SMU 1 and 2 supply a voltage force and SMU 3 and 4 record the voltage drop. The resistances of the tracks and bond pads between SMU 3 and 4 are also included in the measurement.

The measured I-V curves at the interconnect intervals of 2, 6, 8, 10, 30, 60, 96, 98, 100 in a full daisy-chain circuit are shown in Fig. 4.9. The resistances were obtained as the slope of the respective curves and are 0.15, 0.53, 0.65, 0.68, 1.80, 4.10, 7.18, 7.28 and 7.36 Ω respectively. These resistances have been plotted as a function of the number of interconnects as shown in Fig. 4.10. From the graph, the resistances are nearly linearly increased with the number of the interconnections and a linearized line was plotted to fit the points. The deviation of the points to the linearized line was found, which is caused by the resistance variation of individual NW-ACF interconnects. The slope of the linearized line (using equation: $y = a + b * x$) is defined as the average daisy-chain resistance per interconnect and applicable to all the average resistance referred hereafter. The fitting of the data is verified by R^2 (the coefficient of determination) and all fitting should have $R^2 > 0.95$ as a valid fitting. In this case, the obtained resistance is 75 m Ω per interconnect with $R^2 = 0.99$.

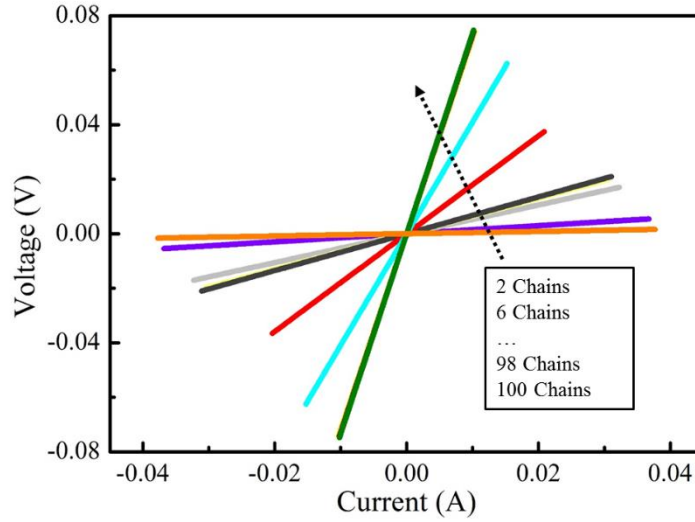


Figure 4.8 I-V curves of a representative bonded sample by probing the daisy-chain intervals.

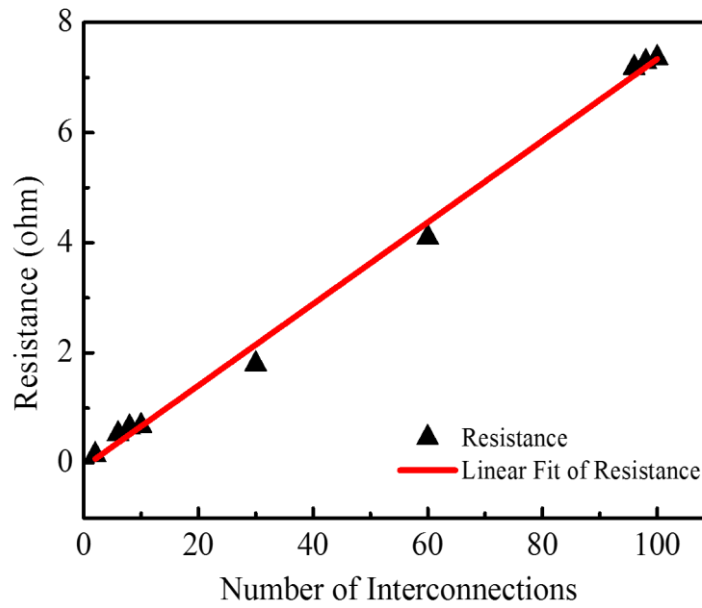


Figure 4.9 Daisy-chain resistance as a function of number of interconnects.

4.2.6 The Effect of Bonding Temperature

Sufficiently high temperature should be applied during the NW-ACF bonding process in order to get a reliable NW-ACF interconnect with good electrical and mechanical properties. At the temperature above glass transition point (T_g) or melting point, the thermoplastic polymer starts to become soft and sufficiently deformable to conform and adhere to the bonding surfaces [47]. Meanwhile, the modulus of the polymer is reduced below that of the

NWs and the physical contact between the NWs and the bonding surfaces can be established. However, an exceedingly high temperature is not desired due to the possible mechanical degradation or decomposition of the polymer and the oxidation of the filler metals that could occur.

4.2.6.1 Bonding Temperature Effect on Bonding Yield and Daisy-Chain Resistance

The bonding experiment was conducted with test module 1 and NW-ACF C by varying the bonding temperatures from 180 to 240 °C at 20 °C intervals. The bonding yield is defined as the percentage of the bonded samples with full conduction in the 100 daisy-chain interconnects. The electrical probing was conducted after die bonding with simple multimeter measurements to verify the conduction. It was found that a good bonding yield can only be achieved at the bonding temperature ≥ 200 °C. At a lower bonding temperature of 180 °C, nearly all bonded daisy-chain modules are partly open. On the other hand, at the highest set bonding temperature of 240 °C, the bonding yield was greatly reduced. The oxidation of the Cu NWs was observed at this temperature with obvious colour change of the film (Cu colour turning dark red) and the degradation of the polymer film (PC becoming very brittle).

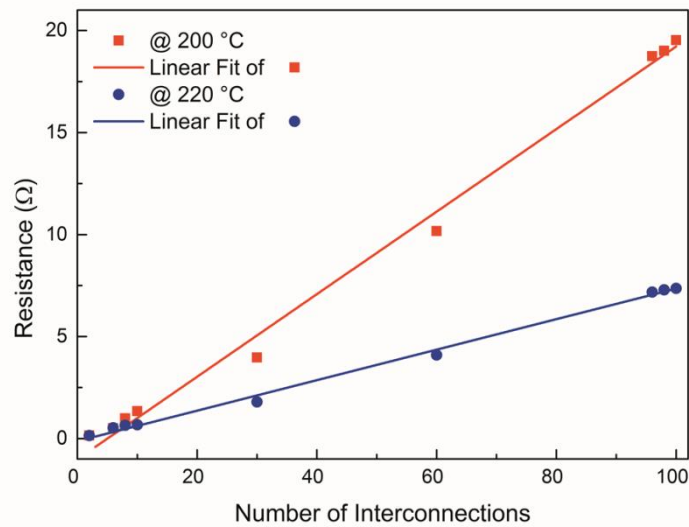


Figure 4.10 Daisy-chain resistances at different bonding temperatures.

Then, the NW-ACF interconnects bonded under two temperature variables of 200 and 220 °C were evaluated with full electrical characterization. Fig. 4.10 compares the daisy-chain resistance of the NW-ACF interconnects bonded under the two temperatures with the same bonding force. The obtained average daisy-chain resistance is 0.2 Ω for the 200 °C

bonded sample, as compared to $0.075\ \Omega$ for $220\ ^\circ\text{C}$ bonded samples. Also, it can be seen from the graph that at $200\ ^\circ\text{C}$, the resistances were found to deviate more to the fitting line. This demonstrates the larger variation of the individual resistance in the daisy chain. Hence, with the optimized bonding yield, the minimum interconnection resistance can be achieved at a bonding temperature of $220\ ^\circ\text{C}$.

4.2.6.2 Bonding Temperature Effect on Bonding Interfaces

In order to understand the effect of bonding temperatures on the formation of NW-ACF interconnects, the bonding interface analysis was conducted. Fig. 4.11 (a) to (c) compare the bonding interface of the NW-ACF interconnects at a pad size of $80\ \mu\text{m}$ at a different bonding temperatures of 180 , 200 and $220\ ^\circ\text{C}$, respectively. As shown in Fig. 4.6 (c), a $15\ \text{N}$ force may be too big to crash the nanowires and therefore a fixed bonding force of $5\ \text{N}$ was applied in this experiment. It was found that the bondline thickness of the interconnects decreases dramatically from $\sim 6.7\ \mu\text{m}$ as bonded at $180\ ^\circ\text{C}$ to $\sim 2.7\ \mu\text{m}$ as bonded at $200\ ^\circ\text{C}$ and keep nearly constant till $220\ ^\circ\text{C}$. This indicates that bondline thickness stabilizes since $200\ ^\circ\text{C}$.

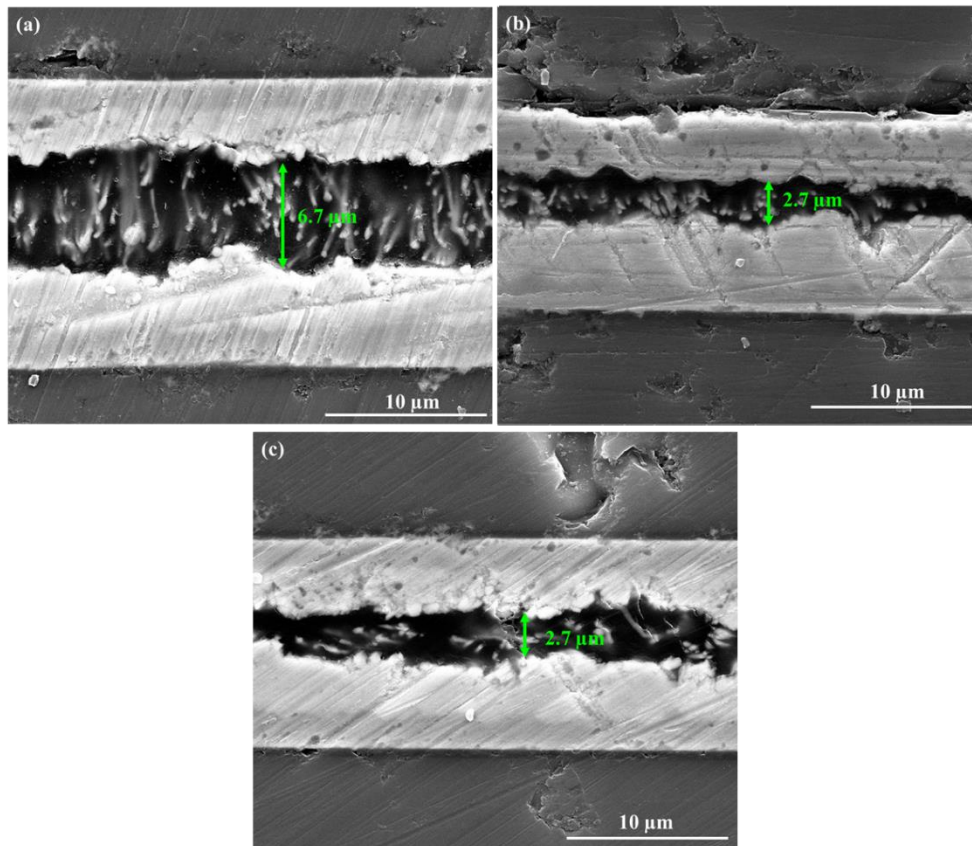


Figure 4.11 SEM images showing the representative bonding interfaces of the NW-ACF interconnects with test module 1 at different bonding temperatures of (a) $180\ ^\circ\text{C}$, (b) $200\ ^\circ\text{C}$ and (c) $220\ ^\circ\text{C}$ and with a bonding force of $5\ \text{N}$.

The phenomenon of the bondline thickness change indicates that 200 °C is a minimum bonding temperature for the NW-ACF when the mechanical property of the composite material may undergo a significant change. The mechanical property of the NW-ACF during bonding can be attributed to two parts, which are the viscoelastic part of the polymer and the elastic part of the nanowires. The former is temperature dependent. By increasing the bonding temperature, the modulus of the polymer is decreased, as described in chapter 3.4.3. In contrast, the elastic modulus of the nanowires relies mainly on its dimensions (diameter and length), as well as the density and the distribution of nanowires in the polymer, and is less temperature dependent. Thus, it can be inferred that at a temperature < 200 °C, the modulus of the polymer is dominating to withstand the external force and determine the bondline thickness. When the bonding temperature is ≥ 200 °C, the modulus of the polymer greatly drops and the external force starts to load on the nanowires. If the external force is higher than both the axial modulus of the nanowires and the modulus of the polymer at the temperature, the deformation of the polymer and the nanowires occurs, which results in a reduced bondline thickness.

4.2.7 Effect of Bond Pad Size

4.2.7.1 Daisy-chain Resistance at Different Pad Sizes

Four daisy-chain modules (in Table 4.1) with the pad size of 80, 40, 20 and 10 μm were used to evaluate the applicable pad size of the NW-ACF interconnects. At the optimized bonding temperature of 220 °C, a minimum bonding force of 1.5 N was applied for NW-ACF bonding for each test module. For all test modules, the electrical conduction of 100 daisy-chain interconnects can be achieved with different resistance values. Fig. 4.12 compares the measured daisy-chain resistances for test module 1-4, where test module 1 and 2 with larger pad sizes and die size have the average resistances of 0.39 and 0.56 Ω per pad, compared to the resistances of test module 3 and 4 of 0.28 and 0.24 Ω per pad. It was found that the smaller pad sizes (20 and 10 μm) results in a smaller resistance, which can be due to the higher equivalent pressure resulted from the same bonding force and smaller bonding area of the die. The convert of bonding force to the equivalent bonding pressure will be described in the following section. It is verified that at all designed bond pad pitches, the successful bonding of 100 daisy-chain interconnects with NW-ACF can be achieved.

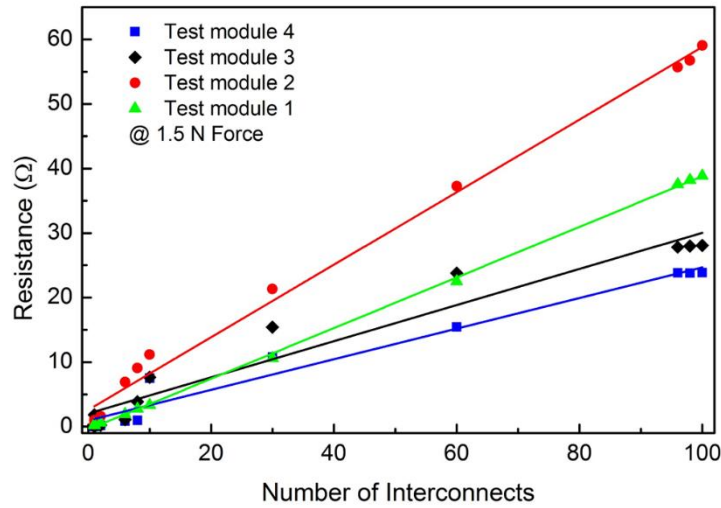


Figure 4.12 Daisy-chain resistance of the NW-ACF interconnects with different pad sizes (bonding condition: 220 °C, 1.5 N and 60 s).

4.2.7.2 Equivalent Bonding Pressure

With the same bonding force, the resultant pressure can be different based on the respective bonding area of the die. For each test module, there are primarily two surface areas to be considered. These two areas subsequently withstand the bonding force based on the bond pad topography, as shown in Fig. 4.13. Surface area 1, composed of Cu and In layer has the largest thickness to compress the film between the bond pads with two pad thickness of $\sim 8 \mu\text{m}$ and surface area 2 is composed of Cu layer, which further compress the film under/above the Cu track areas. Due to the comparable film thickness ($\sim 10 \mu\text{m}$) to the bond pad and track height, the NW-ACF will be mostly compressed between these two areas before it touches the Si die area. Therefore, the equivalent bonding pressure can be calculated based on the surface area 2 of each test module in order to normalize the bonding force. The calculated surface areas and the equivalent bonding pressures (for four bonding forces) for test module 1-4 are shown in Table 4.3. It can be seen from the table that at the same bonding force, the test module 3 and 4 result in much larger bonding pressures as compared to test module 1 and 2.

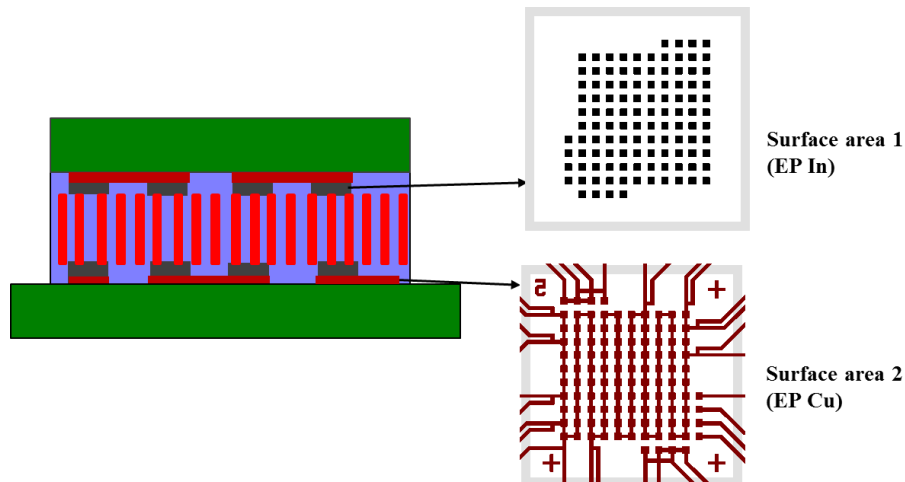


Figure 4.13 Schematics showing the two surface areas of (a) surface area 1 of electroplated indium (thickness $\sim 4 \mu\text{m}$) and (b) surface area 2 of electroplated copper (thickness $\sim 3 \mu\text{m}$).

Table 4.3 The average daisy-chain resistance of the NW-ACF interconnects of test module 1-4 at a different bonding force.

Test module	Bond pad size (μm)	Surface area 1 (mm^2)	Surface area 2 (mm^2)	Equivalent bonding pressure (MPa) (Based on surface area 2)			
				1.5 N	3 N	5 N	10 N
1	80	0.72	0.63	2.4	4.8	8	16
2	40	0.18	1.22	1.2	2.4	4	8
3	20	0.045	0.15	10	20	33	66
4	10	0.011	0.17	9	18	29	58

4.2.7.3 Bond Pad Effect on Bonding Interfaces

Compared to solder based interconnects which require a specific ratio of bump size to bump height [196], the NW-ACF interconnects shows a good tolerance to the bond pad structure with a varying bump size to height ratio. In this work, all bond pads of different sizes were fabricated with the same bump height ($\sim 4 \mu\text{m}$). This results in a “thin” (low pad height-to-width ratio) pad structure of 80 and 40 μm pad size and a “thick” (high pad height-to-width ratio) pad structure of 20 and 10 μm pad size. Fig. 4.14 (a) to (c) compare the bonding interface images of the NW-ACF interconnects formed with different bond pads of

80, 40 and 20 μm at a bonding force of 1.5 N. It was found that the 80 and 40 μm pad sizes resulted in a similar bondline thickness of 2-3 μm , compared to a more squeezed bondline thickness of ~ 1 μm for 20 μm pad size. This is because nearly 5 times higher bonding pressure was applied to 20 μm pads at the same bonding force. With the decreased bondline thickness at the smaller pad size, a better contact can be formed between the NWs and the bonding surfaces and this therefore reduces the contact resistance.

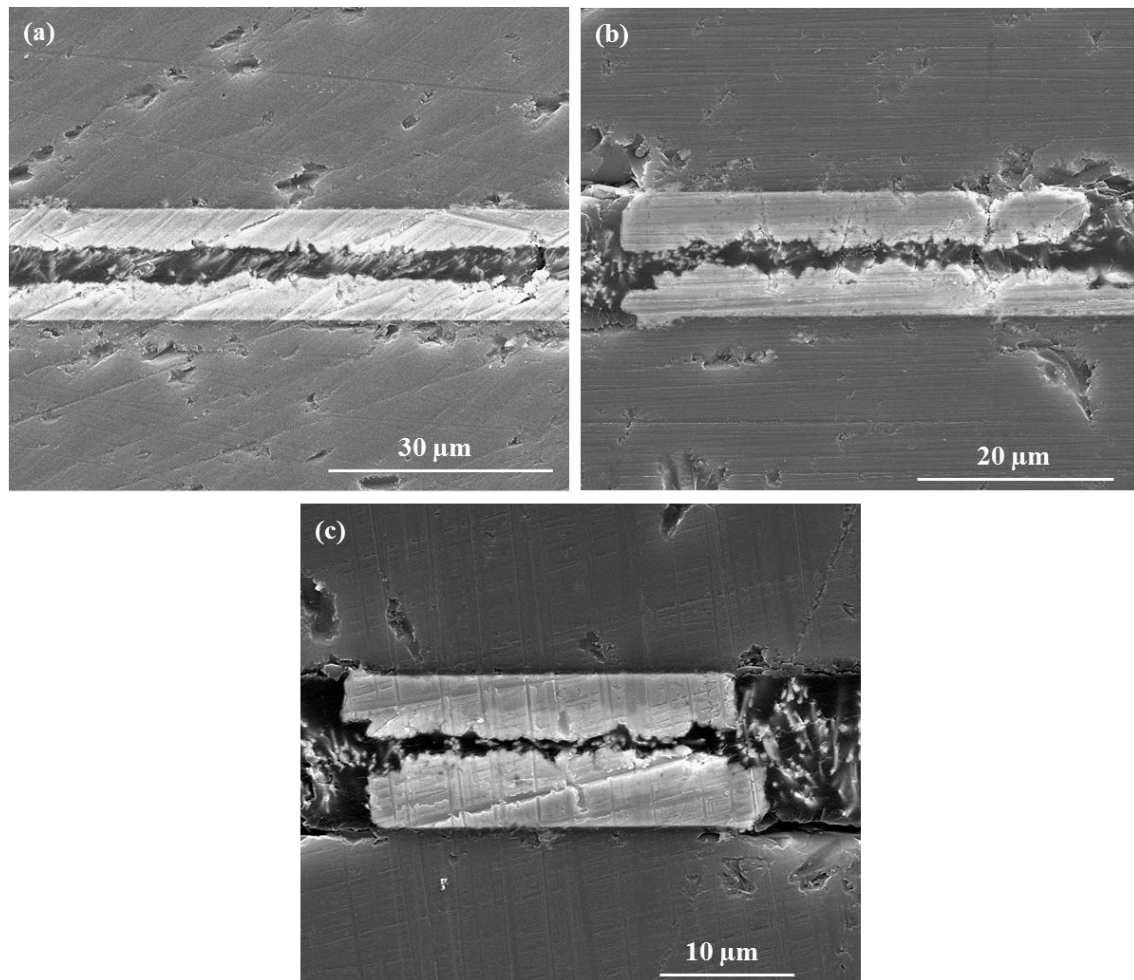


Figure 4.14 SEM images of the bonding interfaces of the NW-ACF interconnects formed at different pad sizes of (a) 80 μm , (b) 40 μm and (c) 20 μm respectively, at a bonding force of 1.5 N.

4.2.8 The Effect of Bonding Force

4.2.8.1 Bonding Force Effect on Daisy-chain Resistance

To understand the bonding force effect on daisy-chain resistance of NW-ACF interconnects, the bonding force was increased from 1.5 N to 15 N for each test module and the obtained average resistance (based on 100 daisy-chain interconnects) was plotted in Figure 4.15 to show the trend. From the graph, the resistances were found to decrease with the increasing forces and became stable for all test modules till the maximum bonding force. For test module 1 and 2, the minimum resistances were obtained at 10 N bonding force and are 30 m Ω per interconnect. The same level of the resistance (30 m Ω) can be achieved by test module 3 and 4 at a bonding force of 5 N. The best resistance data obtain by NW-ACF (30 m Ω at a pad size of 10 μm) is comparable to the contact resistance of the ultra-fine pitch Cu-Sn μbumps , which is ~ 70 m Ω at a pad size of 5 μm [197].

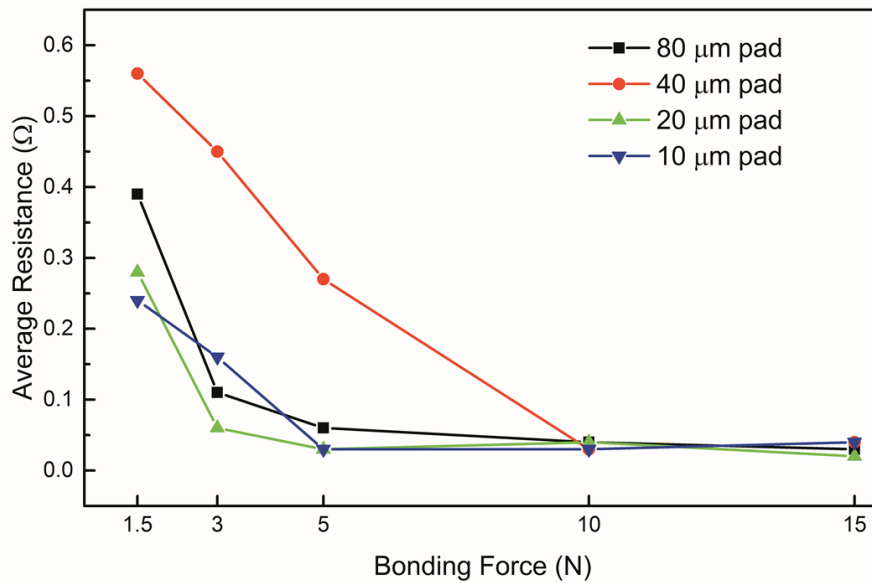


Figure 4.15 Averaged daisy-chain resistances in terms of bonding force for all test modules.

To further compare the resistance of different pad size under equivalent bonding pressure, the resistance data for each test module under corresponding pressure are listed in Table 4.4. The equivalent pressure for test module 1 and 2 to obtain the minimum resistance are 16 and 8 MPa, compared to that of ~ 30 MPa for test module 3 and 4. Due to the higher bonding pressure, the smaller pad sizes reach the same level of minimum resistance as that of

the larger pad size. To compare the resistance between different pad sizes at a similar pressure (8-10 MPa), the resistances for 80, 40, 20 and 10 μm pad are 0.06, 0.03, 0.28 and 0.24 Ω , respectively. It was found that the resistance is not linearly scaled with the bond pad area at the nearly same bonding pressure. The same phenomenon was reported by IBM [198] in comparing the contact resistance of the solder bumps with different bump size. They explained the current crowding and spreading resistance contribute to the resistance inconsistency per pad size. For the NW-ACF interconnect, this can be attributed to the variant number of the contacted NWs per interconnect and the different contact resistance resulted by individual NWs depending on their contact types.

Table 4.4 The average daisy-chain resistance of the NW-ACF interconnects of test module 1 to 4 at a different bonding force/pressure.

Test module	Pad size (μm)	Average daisy-chain resistance (Ω) @ Equivalent Bonding Pressure (MPa)			
		1.5 N	3 N	5 N	10 N
1	80	0.39 @ 2.4	0.11 @ 4.8	0.06 @ 8	0.04 @ 16
2	40	0.56 @ 1.2	0.45 @ 2.4	0.27 @ 4	0.03 @ 8
3	20	0.28 @ 10	0.06 @ 20	0.03 @ 33	0.04 @ 66
4	10	0.24 @ 9	0.16 @ 18	0.04 @ 29	0.03 @ 58

4.2.8.2 Bonding Force Effect on Bondline Thickness

The effect of bonding force on the NW-ACF interconnects can be better understood by analyzing the bonding interfaces of interconnects with the same pad size at a varying bonding force. Fig. 4.16 (a) to (c) shows the change of the bondline thickness by increasing the bonding force from 1.5, 5 to 10 N for 80 μm pad size. By increasing the bonding force from 1.5, 5 to 10 N, the bondline thickness is gradually decreased from 4.2, 2.7 to 0.7 μm . Fig. 4.16 (d) shows a nearly inversely linear decrease of the bondline thickness of the NW-ACF by increasing the bonding force. By observing the morphologies of the nanowires in the different bonding interfaces, it was found that at a small bonding force of 1.5 N (2.4 MPa) in Fig. 4.16 (a), the nanowires are seen to make the contact to both bonding surfaces with an

inclination angle, but still maintain a vertical conducting position. At the larger bonding forces of 5 N (8 MPa) in Fig. 4.16 (b) and 10 N (16 MPa) in Fig. 4.16 (c), the nanowires are seen to be bent in the horizontal direction and the cross-sectional surfaces of the nanowires are visible. This phenomenon has also been reported by Fiedler et al. [199], where the vertical nanowires are seen to change their positions with the visible cross-sectional surfaces of the nanowires, when the bonding pressure is increased from 3 MPa to 15 MPa.

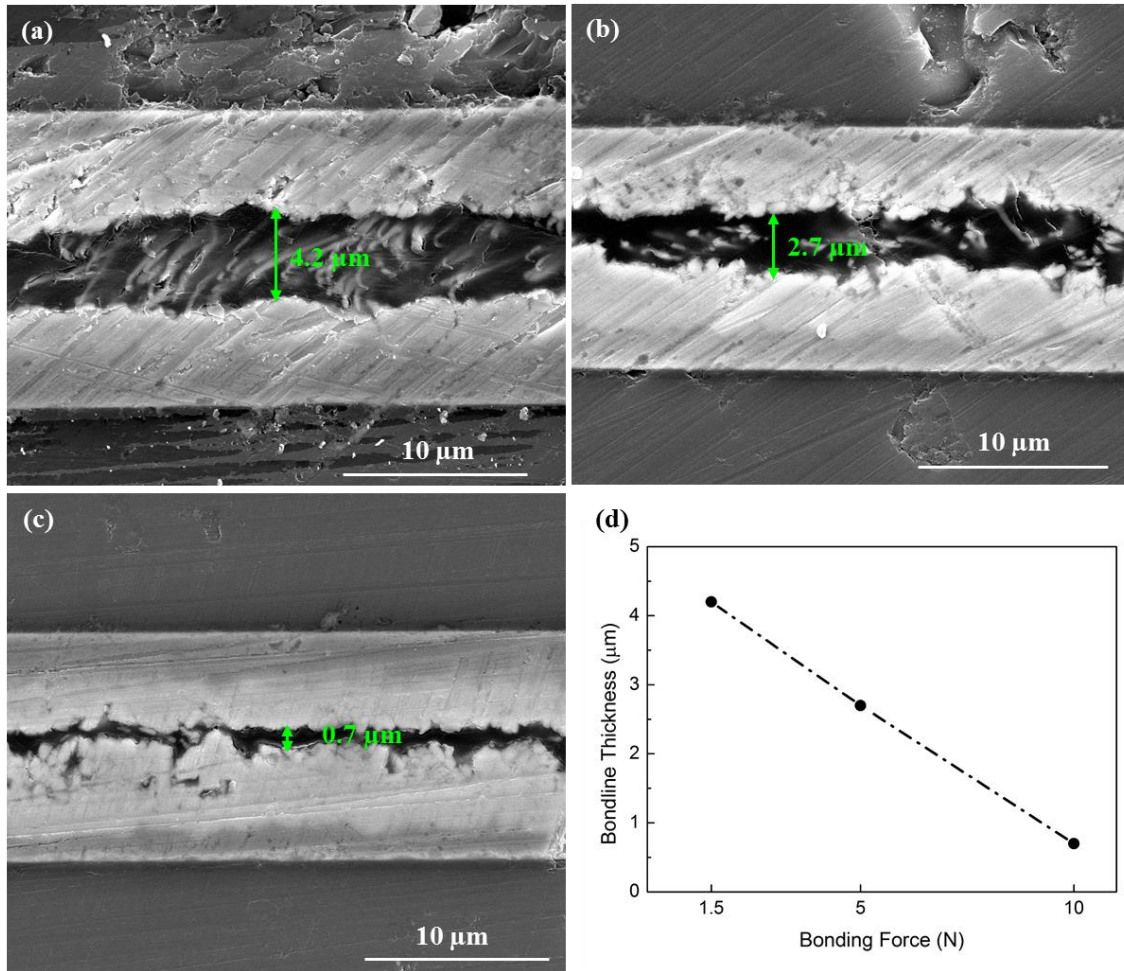


Figure 4.16 SEM images of the bonding interfaces of the NW-ACF interconnects with 80 μm pad size at different bonding forces of (a) 1.5 N, (b) 5 N and (c) 10 N respectively. The plot (d) shows the change of the bondline thickness of the NW-ACF in terms of bonding force.

The morphology of the bent NWs can be observed at the bond pad area after detaching the bonded sample and dissolving the polycarbonate of the NW-ACF. A small bunch of the bent NWs were found to be attached to the In surface as shown in Fig. 4.17. The bending

morphology of the NWs does not recover even when the bonding force was removed. This demonstrates that plastic deformation of the nanowires occurred during bonding. Due to the largely deformed NWs during bonding, the contact area between the NWs and the bonding surface can increase and this results in a decreased contact resistance.

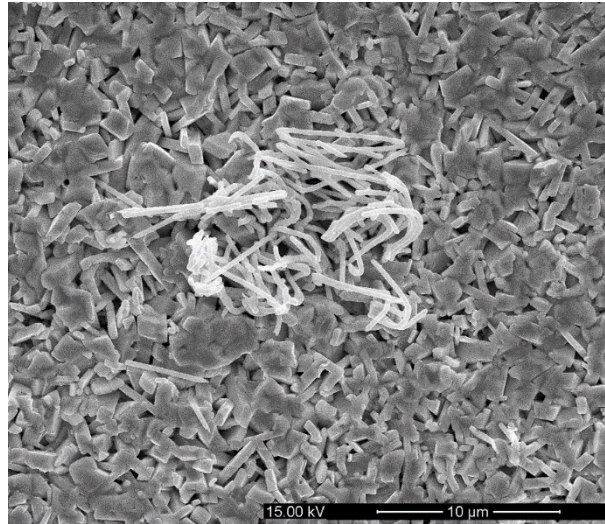


Figure 4.17 The morphology of the bent nanowires found on the detached bond pad surface (polycarbonate was removed by dichloromethane).

4.2.9 Insulation Properties

For the NW-ACF, the polymer matrix acts as the insulation material between the nanowires to prevent lateral conduction. The conductivity of pure polycarbonate is about 10^{-13} S/m [200] and it has been used as the base insulation material to form CNT/polymer composite for electrical applications. On the other hand, the distribution of nanowires which is predetermined by the pore distribution in the polymer is the key factor to influence the insulation properties of the NW-ACF. Due to the random distribution of pore positions as seen from the template surface (Fig. 3.1(c)) and the different angles of inclination of the pore channels, the merged pores seen in the template surface and the existence of the overlapping pores inside the template mainly account for the insulation issues for such NW-ACF material.

The insulation properties of the NW-ACF interconnects for each successfully bonded samples have been evaluated by probing the four insulation pads on the same die and the results are presented in Table. 4.5. The leakage current was measured at increased voltages from 0 to 20 V with a step size of 50 mV. A failure criteria is defined as a measured leakage

current $I_{\text{leak}} > 10^{-9}$ A, which is an analogy to the failure criteria defined to measure the leakage characteristic of the fine-pitch TSVs in the Si substrate [201]. Table 4.5 lists the maximum voltage at which the tolerant leakage current can be maintained. Three pairs of the insulation pads were probed for each test module and the voltage represents the worst case scenario among the tested groups. It was found that for the large pitch sizes (160 and 80 μm), nearly all interconnects can maintain a small leakage current up to 20 V (except for the test module 2 at 5 N). For the smaller pitch size (40 and 30 μm), there are more variations of insulation voltage from sample to sample and one shorted interconnect was found with the test module 4 at 3 N. The drop of insulation voltage and the occurrence of short failure at smaller pad sizes can be attributed to the smaller insulation space at fine pitch and the higher bonding pressure to result in more bending of the wires between the interconnects. A high percentage of bent wires in the pad gap can increase the chance of short circuiting. However, most of the insulated interconnects show a good insulation property with a small leakage current even at a small pitch size.

Table 4.5 Insulation properties of NW-ACF interconnects of test module 1-4 at different bonding forces.

Test module	Pitch size (μm)	Insulation Voltage (V) @ Bonding force (Failure criteria: $I_{\text{leak}} > 10^{-9}$ A)			
		1.5 N	3 N	5 N	10 N
1	160	20	20	20	20
2	80	20	20	6	20
3	40	9	7.5	18	20
4	30	20	Short	14	20

Fig. 4.18 shows the I-V curves representing the typical leakage current behaviours of the measured NW-ACF interconnects at a pitch size of 30 μm . Fig. 4.18 (a) shows the I-V curve indicating the best-case insulation property, where the leakage current is well maintained below 10^{-12} A with an applied voltage up to 20 V. Comparatively, Fig. 4.18 (b) shows the increase of the leakage current with the increasing voltage. This represents the typical insulation behaviour for the interconnects with an insulation voltage < 20 V (in Table 4.5). In

the graph (b), as the applied voltage is > 14 V, the leakage current drops below 10^{-9} A and gradually increased up to 10^{-6} A. The decreased insulation voltage can be attributed to the random distribution of the pores in the membrane template and the existence of the overlapping pores in some small areas. If such areas are captured between two adjacent pads, the tiny conduction channels formed by the linked nanowires can be established in the X-Y direction and cause the increased leakage current and even short failures at an increased applied voltage. However, it should be noted that both the applied voltage and the leakage current limit have been set stricter than the normal requirement of IC application voltage of ~ 3 V and the leakage current limit of $< 10^{-6}$ A.

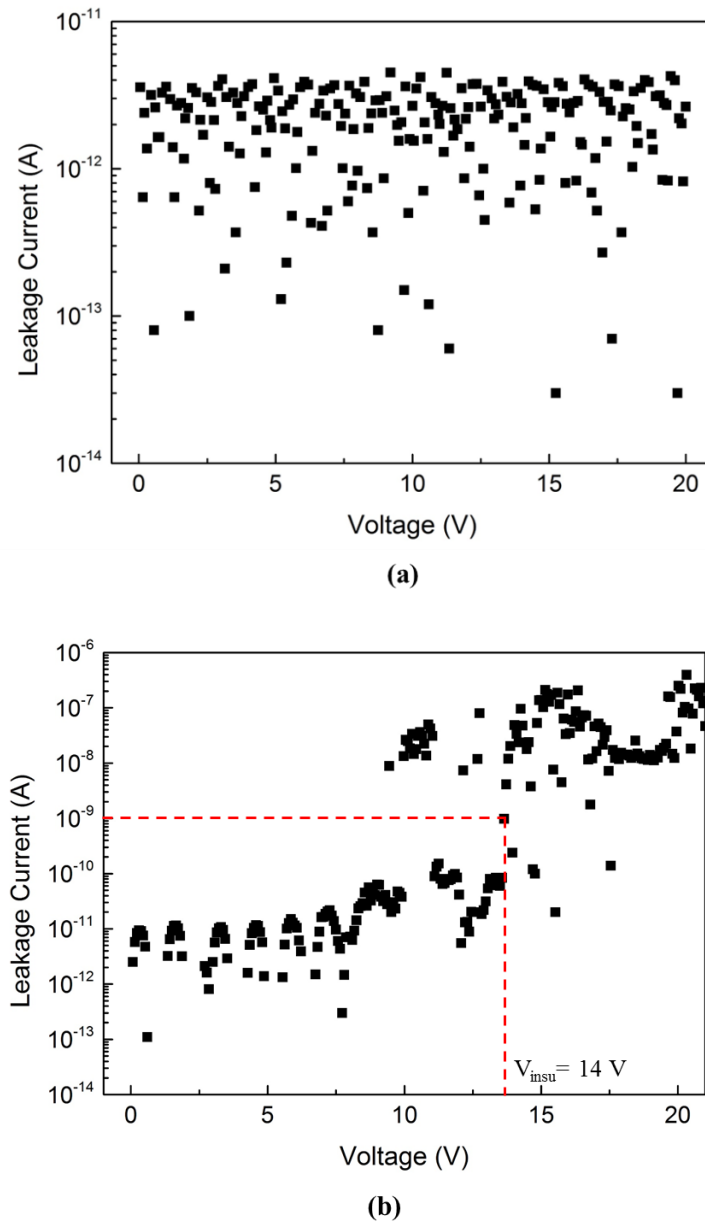


Figure 4.18 The typical I-V curves showing leakage current behaviours as a function of voltage, (a) insulation voltage of 20 V and (b) insulation voltage of 14 V.

4.3 Bumpless Interconnects Formed with NW-ACF and Au Pads

In the previous sections, NW-ACF has been shown to bond effectively between Cu-In bond pads. Indium was applied as a layer of solder on the Cu bond pads to facilitate nanowire bonding. However, the question remains: will the NW-ACF be able to bond with a non-solder metal surface? To answer this question, bond pads of the test chip are prepared with Ti/Au metallization. Meanwhile, the bond pad thickness was reduced to 0.7 μm in order to form a bumpless scenario for NW-ACF bonding. Fig. 4.19 shows the schematics of applying the NW-ACF for bumped and bumpless die bonding, where scenarios 2 and 3 are mainly discussed in this section. Two pad/pitch sizes of 80/160 μm and 40/80 μm were evaluated for NW-ACF bonding and a comparison study has been carried out to compare NW-ACF bonding to that of conventional particle-based ACF.

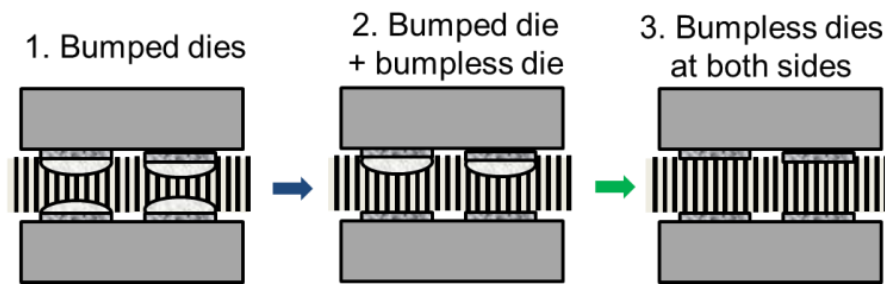


Figure 4.19 Schematics showing the scenarios of applying NW-ACF as the interconnections between: 1) bumped die, 2) bumped and bumpless die and 3) bumpless die.

4.3.1 Test Chips and TCB Bonding

Daisy-chain test modules with $\sim 0.7 \mu\text{m}$ thick Au Pads were fabricated by a Ti ($\sim 20 \text{ nm}$) and Au evaporation process followed by dry etch process using the seed etch mask as mentioned in Chapter 4.2.2. The bottom die of test module 2 with the patterned Au pads is shown in Fig. 4.20 (a). A magnified image to show a single pad area with smooth surface morphology is shown in Fig. 4.20 (b). The bonding process was carried out at a condition of 220 $^{\circ}\text{C}$, 60 s and 2 N. A relatively small bonding force was used because the best bonding yield can be achieved. The reason for applying a small bonding force will be explained in the following chapter 4.3.3. For the purpose of comparison, a commercial particle-based ACF was bonded under the condition of 190 $^{\circ}\text{C}$, 5 s and 20 N, according to the supplier specifications.

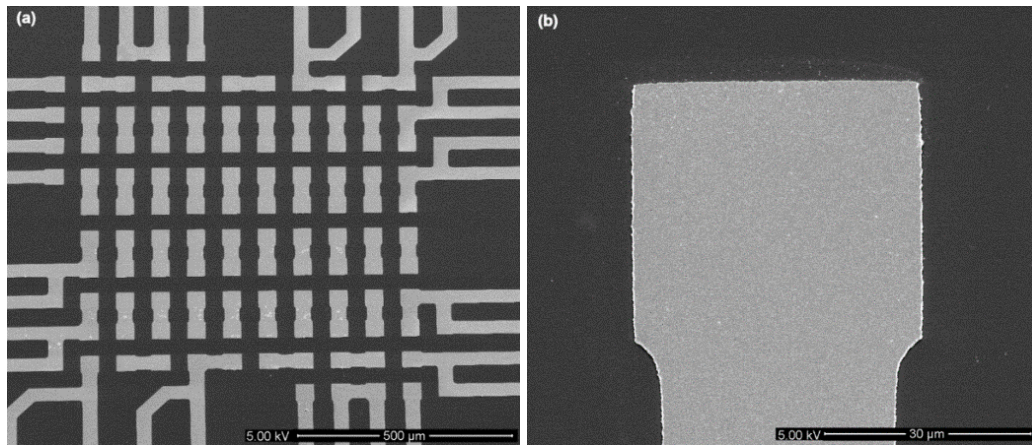


Figure 4.20 Bottom chip of test module 2 with bumpless Au pads of $\sim 0.7 \mu\text{m}$ thickness, (a) the daisy-chain pattern and (b) pad surface morphology.

4.3.2 NW-ACF Interconnects Formed between Bumped and Bumpless Pads

The experiment started with the bonding scenario 2 as shown in Fig. 4.19 with test module 2 (bond pad/pitch size of $40/80 \mu\text{m}$). The NW-ACF was bonded between the bottom chip with Au bumpless pads and the top chip with Cu-In pads. The daisy-chain resistance was measured using the 4-point measurement in the Cascade Probe Station. Fig. 4.21 shows the results of the resistance in terms of number of interconnects. By linearizing the resistance, the average resistance is 0.21Ω ($R^2=0.99$) for this bonding scenario.

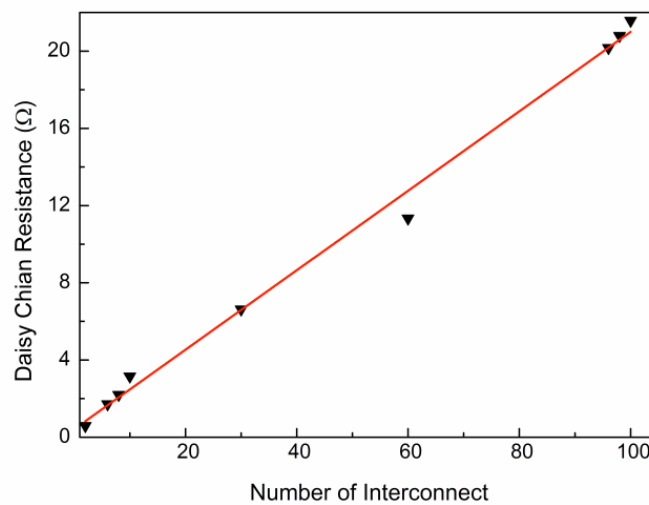


Figure 4.21 Daisy-chain resistance of a NW-ACF interconnect between the bumped and bumpless dies (pad/pitch size $40/80 \mu\text{m}$).

The insulation properties were measured by stressing two neighbouring insulated pads with an applied voltage from 0 to 20 V. Fig. 4.22 shows a typical leakage current in terms of the applied voltage. It was found that the leakage current can be maintained below 10^{-8} A at a voltage ~ 5 V and then nearly linearly increased with the increased voltage up to 10^{-6} A (due to the existence of linked nanowires in XY-direction). Also, it was found that there is a general decrease of the insulation voltage as compared to the previous bonded samples (in Table 4.5). This may be caused by the membrane variations from the different production batch of the supplier. In different purchased batches, the membrane porosity and pore characteristic was found to vary within supplier specification, but sufficiently to cause the material property change when fabricated as NW-ACF material. As the membranes is not design for this particular purpose (to fabricate ACF), the current product variations can easily result in different leakage current behaviour of NW-ACFs. Therefore, a specified membrane film with a tight control of the desired quality, especially with regard to a more consistent porosity and pore structure, becomes a key step to further develop the NW-ACF material.

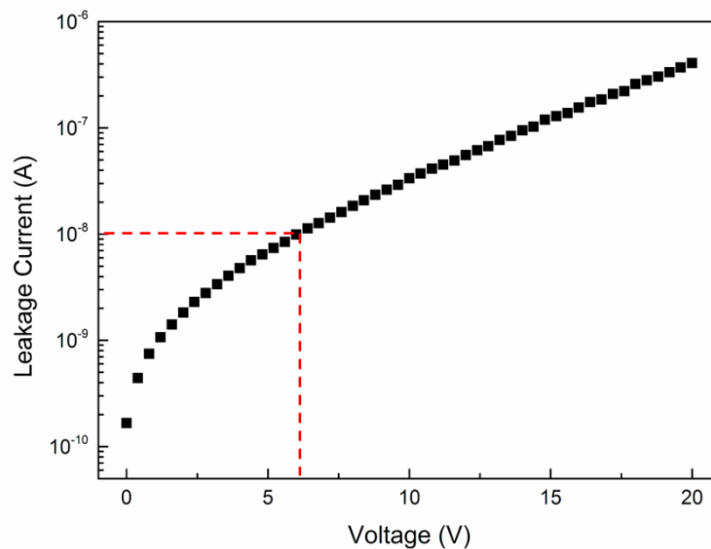


Figure 4.22 Insulation property of the NW-ACF interconnects between the bumped and bumpless dies (pad/pitch size 40/80 μm).

Fig. 4.23 show the SEM images of the bonding interfaces of the NW-ACF interconnects between the bumped and bumpless pads. Fig. 4.23 (a) shows a pair of daisy chain connections at 40/80 μm pad/pitch size. Due to the height of the top bond pads, the NW-ACF under the top bumped pads is mostly compressed with a reduced bondline thickness to

conform to the pad thickness. Fig. 4.23 (b) shows a magnified image of a single interconnect, where the nanowires are seen to bend to nearly half of their length and contact the top and bottom surfaces with an inclination angle.

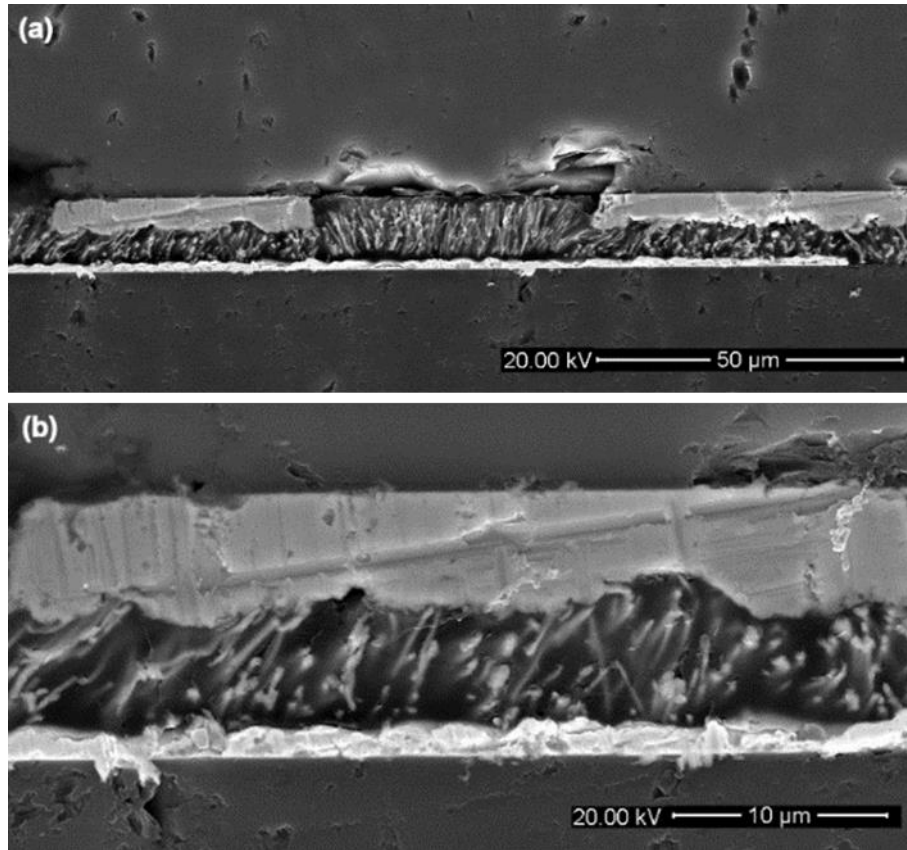


Figure 4.23 Bonding interface of the NW-ACF between the top Cu/In bond pad and the bottom bumpless Au pad, (a) a pair of daisy chain connections and (b) the magnified image of the NW-ACF interconnection.

4.3.3 NW-ACF Interconnects between Two Bumpless Dies

As the first experiment verified the bondability of NW-ACF to one side of the Au pad (scenario 2 in Fig.4.19), the next step was to evaluate the NW-ACF bonding with two Au pads with a very small bond pad height (scenario 3 in Fig. 4.19). The same bonding condition (220 °C, 60 s, 2 N) was applied for the bumpless die bonding. Fig. 4.24 shows the daisy chain resistances per NW-ACF interconnect at the pad sizes of 80 and 40 μm of test module 1 and 2. It was found that for both pad sizes, a comparable resistance of 0.13 and 0.09 Ω was obtained for 80 and 40 μm pads. This may demonstrate that a certain number of NWs can be captured per pad regardless of these two pad sizes.

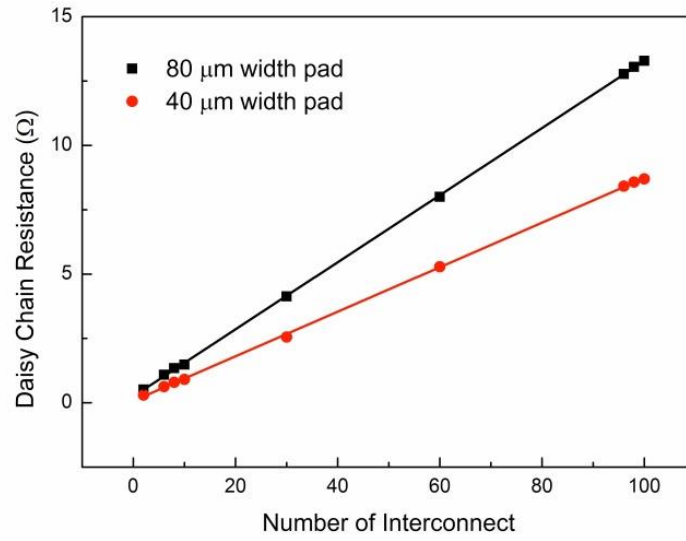
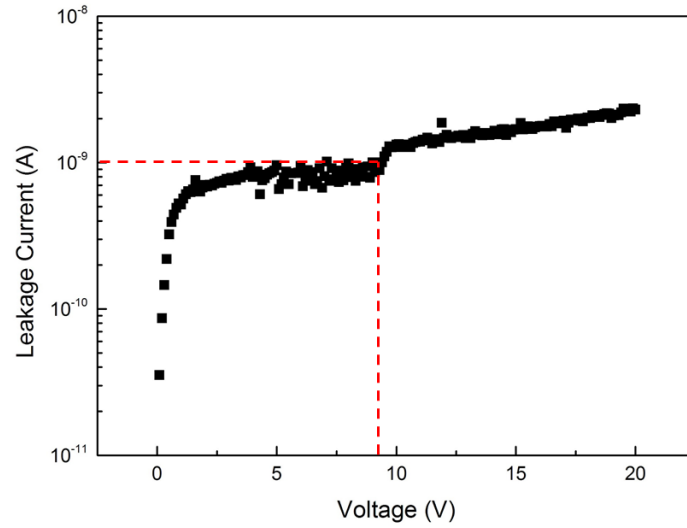
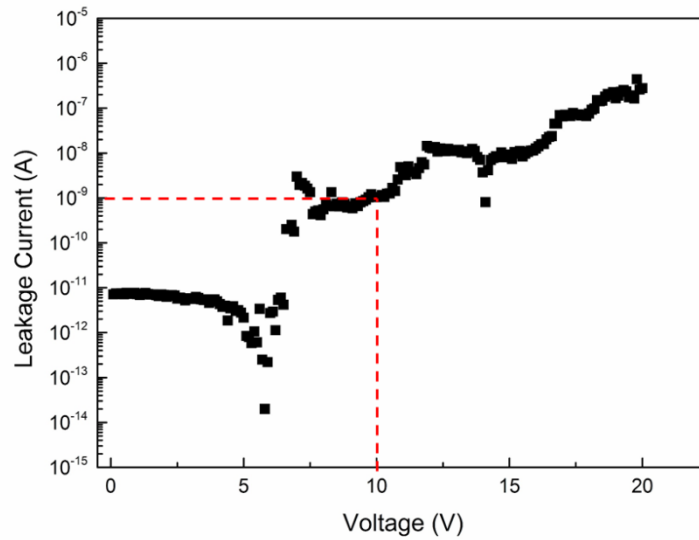


Figure 4.24 Daisy-chain resistance of a NW-ACF interconnect between two Au bumpless die, (a) black line for 80/160 μm pad/pitch size and (b) red line for 40/80 μm pad/pitch size.

Compared to the NW-ACF interconnects formed between Cu-In and Au pads at the same bonding force, the resistance of the NW-ACF interconnects between two Au pads is even smaller. This can be explained by the different metallization of the bond pads. For In-finished pads, it is highly possible that a thin layer of oxidation was formed on the In surface before bonding, and this requires a higher bonding force to break it through. While for the oxidation-free Au-finished pads, a small amount of bonding force is sufficient for the nanowires to intimately contact the metal. Compared to the minimum interconnection resistance of the NW-ACF interconnects with the both sides In-finished pads (0.03-0.04 Ω), the minimum resistance achieved by the NW-ACF bonding to both sides Au bumpless pads is quite comparable $\sim 0.09 \Omega$. The results show that without an In finish, Cu nanowires can still form a low contact resistance joint with non-solder Au surfaces, which constitutes the provisions for the future application of the material for the bumpless architecture in 3D applications.



(a)



(b)

Figure 4.25 Insulation property of (a) NW-ACF interconnects between bumpless dies at a pitch size of 160 μm and (b) at a pitch size of 80 μm .

Fig. 4.25 (a) and (b) show the insulation properties of the NW-ACF bumpless interconnects formed with test module 1 and 2, respectively. For both pitch sizes (160 and 80 μm), the leakage currents are well maintained below 10^{-9} A at an applied voltage up to 10 V. Table 4.7 compares the electrical performance of NW-ACF interconnects formed with different bond pad types. It was found that both the pad size and metallization have an influence on the interconnection resistance. At the same bonding condition, a smaller pad size

and Au bonding surface may result in a lower resistance. On the other hand, the insulation voltage is dependent on the pitch size and the bond pad height of the interconnects. When the pitch size is decreased or the bond pad height is increased, the insulation voltage can be decreased due to the higher chance of the occurrences of the short channels formed by the linked nanowires in the X-Y direction.

Table 4.6 Electrical performance of NW-ACF interconnects at various bond pad structures.

Bond Pad Types	Pad/Pitch size (μm)	Electrical Properties	
		Average Daisy-chain Resistance (Ω)	Insulation Voltage (V, $I_{\text{leak}} < 10^{-9}$ A)
Bumped Cu-In + Bumpless Au	40/80	0.21	3
Bumpless Au + Au	80/160	0.13	10
Bumpless Au + Au	40/80	0.09	5

Note: Bonding condition for all bonded samples is 220 °C, 2 N, 60 s.

The bonding interfaces of the NW-ACF interconnects with the bumpless pads are shown in Fig. 4.26. Fig. 4.26 (a) shows a pair of daisy-chain connections formed by the NW-ACF between the top and bottom thin Au pads at a pad/pitch size of 40/80 μm . Compared with the greatly decreased bondline thickness of the interconnects formed with either one side or two sides of the bumped pads, the bondline thickness in such interconnects is nearly not changed from the original film thickness of the NW-ACF. Fig. 4.26 (b) shows the magnified image of a single interconnect, where the nanowires are seen to contact with both surfaces on their length direction without bending. Due to the very thin pad thickness, the bonding force is nearly uniformly distributed on the whole die surface area ($2.5 \times 2.5 \text{ mm}^2$) instead of loading on the bond pad and metal track area (which is the case for the Cu-In bumped dies). At a bonding force of 2 N, the equivalent bonding pressure is $< 1 \text{ MPa}$. With such a small bonding pressure, the contact mode of the nanowires are direct point contacts of nanowire ends to the Au surfaces instead of bending of nanowires as occurred during bonding with the Cu-In bond pads. It was found that such point contact can result in most effective contact between nanowires and the thin Au pads. Unlike the Cu-In pads with an In finish to better “capture” the nanowires even after their bending, the smooth Au finish may result in more mechanical

sliding of the nanowires under compression so to lose the contact. Therefore, a small force is needed for NW-ACF bonding with the Au pads.

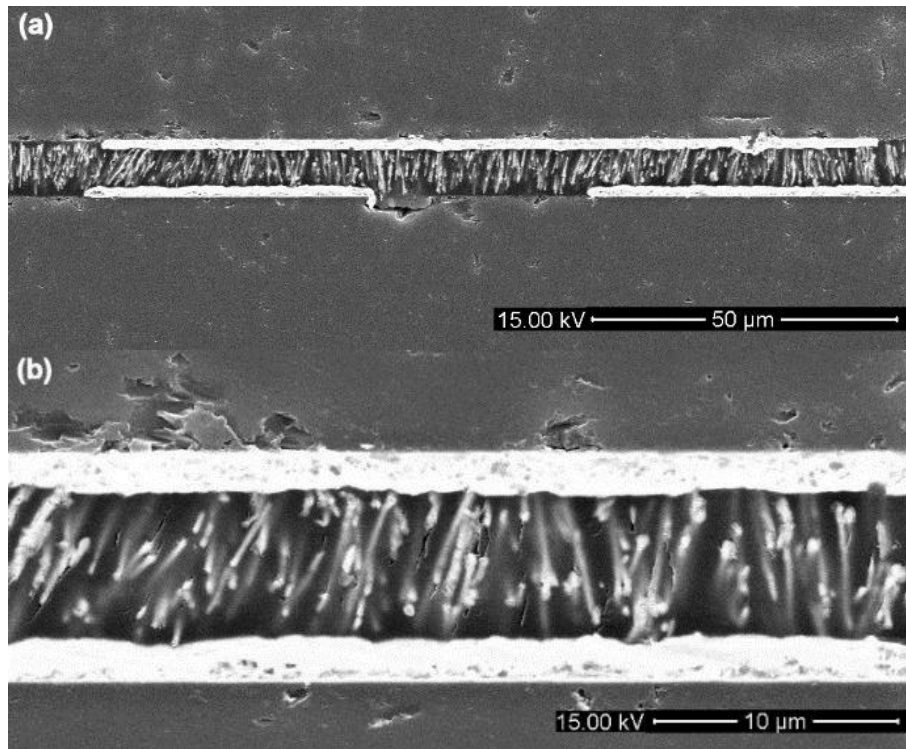


Figure 4.26 SEM images of the bonding interfaces of NW-ACF interconnects between the bumpless pads (pad/pitch size of 40/80 μm), (a) a pair of daisy chain connections and (b) the magnified nanowires interconnects.

4.3.4 Comparison with Particle based ACF

A study was carried out to compare the fine-pitch interconnects formed by the NW-ACF and a commercial particle based ACF using test modules 1 and 2. The commercial ACF is composed of $\sim 3 \mu\text{m}$ diameter Ni-Au coated polymer spheres. A pre-lamination process was needed for the particle-based ACF to attach the ACF to the bottom chip and peel off the protective carrier film. This was conducted at 110 $^{\circ}\text{C}$ for 2 s with a small manually applied lamination force. The main bonding process was carried out at a peak temperature of 190 $^{\circ}\text{C}$ for 5 s, and a bonding pressure of 20 N was applied. Fig. 4.27 compares the bonding interfaces of the NW-ACF interconnect to that of a particle based ACF at a pad size of 80 μm . A much larger number of the NWs were found in the pad area of the NW-ACF interconnects

(a), as compared to a few spherical particles observed for the particle-based ACF interconnects (b).

Depending on the shapes of the conductors, the required filler densities could be different. For the particle-based ACF, the electrical connection was formed by the deformation of the spherical particles and each of the particles can result in a relatively large contact area. While for the high aspect-ratio conductors such as nanowires in the NW-ACF, they contacted the surfaces mainly with the nanowire ends. Therefore, a higher density of nanowires will be needed for the NW-ACF to act as the conductors in the interconnects to achieve a sufficiently low interconnection resistance. However, the high density nanowires can result in an increased leakage current in X-Y direction which is discussed in the next paragraph.

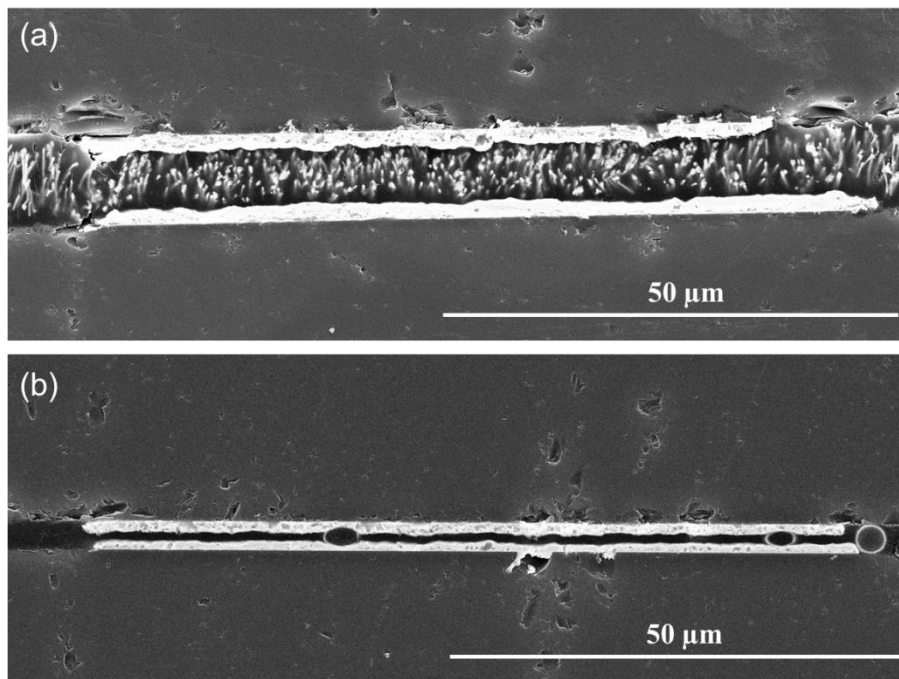


Figure 4.27 SEM images of the bonding interfaces of (a) NW-ACF interconnects and (b) a particle based ACF between Au bumpless pads (pad/pitch size: 80/160 μm).

Fig. 4.28 (a) and (b) compare the daisy-chain resistances of the particle-based ACF interconnects to those of the NW-ACF interconnects formed with Au bumpless pads at a pad size of 80 and 40 μm , respectively. At a pad size of 80 μm , the interconnection resistances of the particle-based ACF (0.16 Ω) is comparable to that of the NW-ACF (0.13 Ω). At a pad size of 40 μm , the interconnection resistance of the particle-based ACF increased to 0.3 Ω , which is nearly $3\times$ larger than that of the NW-ACF (0.09 Ω). Therefore, the superiority of the

electrical conduction by the nanowires appears in the application with a small pad size. Due to the lower volume fraction and the micro-size particles in the particle based ACF, the probability to trap the particles in the pad area can be dramatically decreased at a certain pad size [82]. By contrast, such probability will not so much reduce for the nanowires by decreasing the pad size. This is due to the lower mobility of the nanowires in the X-Y direction, as compared to the spherical particles in the conventional ACF.

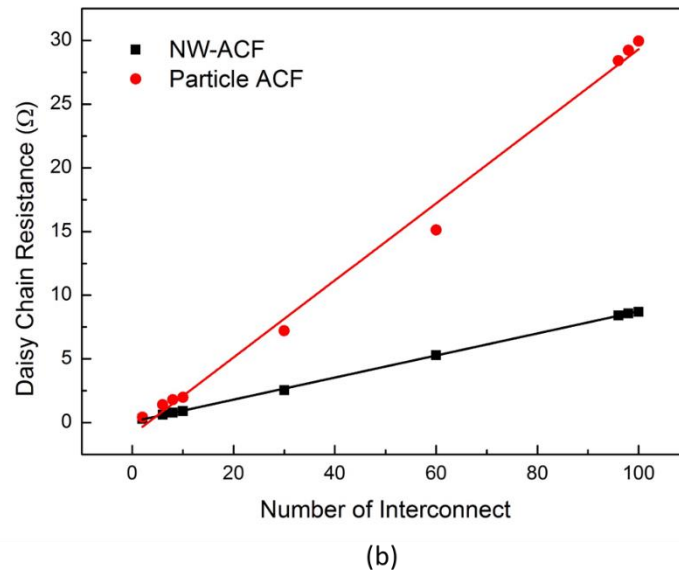
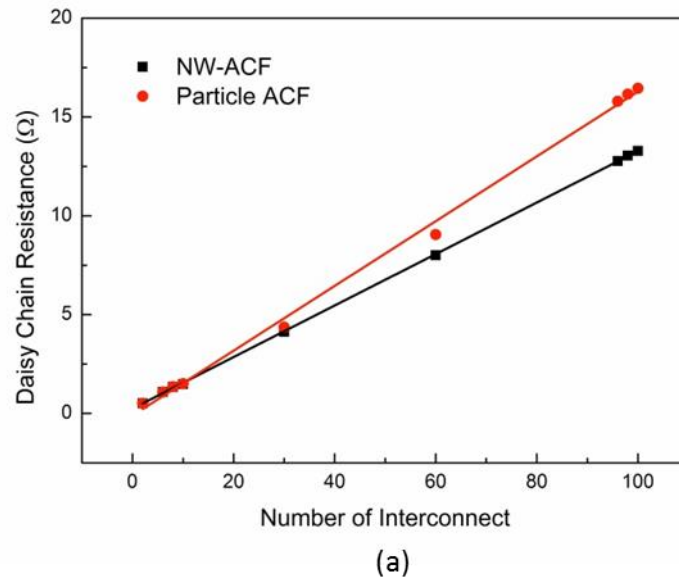


Figure 4.28 Daisy-chain resistance of NW-ACF bonding (black) compared to particle based ACF bonding (red) with the bumpless dies at a pad size of (a) 80 μm and (b) 40 μm .

The insulation property of the particle ACF is shown in Fig. 4.29, where the leakage current is well maintained below 10^{-12} A for an applied voltage up to 20 V. Compared with the leakage current behaviour of the NW-ACF at the same pitch size (Fig. 4.25 (a)), the particle-based ACF shows a better insulation property. This is due to a much lower density (5-10 vol.%) of the conductive particles in the particle ACF [55], as compared to the density of the nanowires (12.5 vol.%) in the NW-ACF.

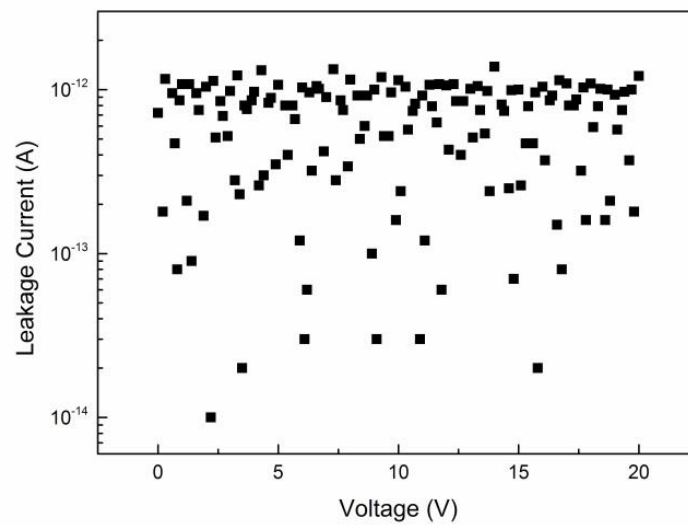


Figure 4.29 Insulation property of particle based ACF interconnects in bumpless dies at a pitch size of 160 μm .

Table 4.7 compares the electrical performance of the NW-ACF interconnects to that of particle based ACF. It shows that the particle based ACF required a 10 times higher bonding force to form the electrical contact with a comparable resistance of the NW-ACF at a large pad size. Due to the different conduction mechanism, the particle based ACF needs a very high pressure to achieve a sufficiently small bondline thickness, when the spherical particles are deformed to make the contact. In contrast, a much smaller bonding force is needed for the nanowire conductors, due to the fact that the length of the nanowires is equal to the film thickness. Moreover, NW-ACF has a better fine-pitch capability as compared to that of the particle based ACF, in that a lower interconnection resistance can be achieved at a smaller pad size by the NW-ACF, as well as the minimum applicable pitch size (30- μm pitch size tested with the Cu-In pads). However, the insulation properties of the NW-ACF need to be

further improved. One feasible solution will be to use membranes with a more evenly distributed and parallel pore structures as the template to fabricate the NW-ACF.

Table 4.7 Comparison of electrical performance of fine-pitch interconnects formed by the particle based ACF and the NW-ACF with the Au bumpless pads.

ACF Type	Pad /Pitch size (μm)	Bonding Condition	Averaged Daisy-chain Resistance (Ω)	Insulation Voltage (V) ($I_{\text{leak}} < 10^{-9}$ A)
Particle-based ACF	80/160	190 $^{\circ}\text{C}$, 5 s, 20 N	0.16	20
Particle-based ACF	40/80	190 $^{\circ}\text{C}$, 5 s, 20 N	0.3	20
NW-ACF	80/160	220 $^{\circ}\text{C}$, 60 s, 2 N	0.13	10
NW-ACF	40/80	220 $^{\circ}\text{C}$, 60 s, 2 N	0.09	10

4.4 High Frequency Performance of the NW-ACF Interconnects

High frequency characterization and modelling of the flip-chip interconnects of solder bump or ACA in the transmission line test structure has been reported by several research groups [202-204]. The electrical properties of the IC interconnects in microwave frequency range are important to influence the integrity of signal propagation in the functional chips. For 3D stacked chips, high frequency performance of the TSVs and bumps have also been investigated to evaluate the suitability of the TSV interconnects for signal transmission in the applied frequency range [205]. As an alternative interconnect method to connect 3D chips, the high frequency performance of the NW-ACF interconnects should be understood. In this work, the high frequency characterization of the NW-ACF interconnects were conducted with S-parameter measurement and the extraction of RLCG parameters up to 20 GHz.

The high frequency measurement can be conducted with a two-port network system to obtain scattering parameters (S-parameters). A typical two-port network system with port 1 and 2 is illustrated in Fig. 4.30, with four input/output parameters of a_1 , b_1 , a_2 and b_2 , where a_1 and a_2 represent the incident waves into port 1 and port 2, b_1 and b_2 represent the reflected waves from port 1 and port 2. The four wave parameters are defined as:

$$a_1 = \frac{V_1^+}{\sqrt{Z_0}} \quad a_2 = \frac{V_2^+}{\sqrt{Z_0}} \quad (4.1)$$

$$b_1 = \frac{V_1^-}{\sqrt{Z_0}} \quad b_2 = \frac{V_2^-}{\sqrt{Z_0}}$$

where V_1^+ and V_2^+ are the amplitudes of the voltage wave incident on port 1 and port 2, V_1^- and V_2^- are the amplitudes of the voltage wave reflected from port 1 and port 2, Z_0 is the characteristic impedance of lossless transmission line in the 50- Ω measurement system. The two-port system can be characterized by S-parameter measurement with transmission and reflection coefficient. The scattering matrix, or [S] matrix, is defined in relation to the incident and reflected waves as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (4.2)$$

Thus, S_{11} is the reflection coefficient seen looking into port 1 when port 2 is terminated in matched loads ($a_2 = 0$), and S_{21} is the transmission coefficient from port 2 to port 1, which can be expressed as:

$$S_{11} = \frac{b_1}{a_1} \quad S_{21} = \frac{b_2}{a_1} \quad (4.3)$$

Similarly, by terminating the port 1 in matched loads ($a_1 = 0$), S_{22} and S_{12} can be obtained.

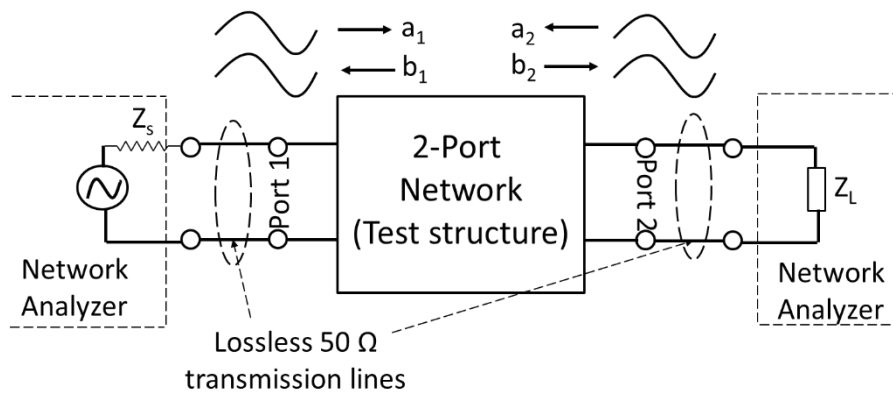


Figure 4.30 Two-port network measurement system of a test structure connected to the network analyser with the representative travelling power waves.

Signal propagation $V(x, t)$ in a single line interconnect is modelled by the Telegrapher's transmission line equation [206] with line parameters R , L , C and G as:

$$\frac{\partial^2 V}{\partial x^2} = RG V + (RC + LG) \frac{\partial V}{\partial t} + LC \frac{\partial^2 V}{\partial t^2} \quad (4.4)$$

where R is the series resistance per unit length of the line, L is the series inductance per unit length, C is the shunt capacitance per unit length (i.e. the capacitance between the line and ground plane), G is the shunt or leakage conductance per unit length (i.e. the conductance from the line to the ground plane). The transmission line which is treated as an idealized distributed component by its length can also be characterized by its characteristic impedance Z and propagation constant γ as:

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (4.5)$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (4.6)$$

$\omega = 2\pi f$, where f is the signal frequency. Based on the earlier work by Eisenstadt and Eo [207], the frequency-variant parameters Z , γ , R , L , C and G for an IC interconnect with a length l can be extracted from S-parameters by following mathematical equations:

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1} \quad (4.7)$$

$$K = \sqrt{\frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2}} \quad (4.8)$$

$$Z^2 = Z_0^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2} \quad (4.9)$$

Then,

$$R = \text{Re} \{ \gamma Z \} \quad (4.10)$$

$$L = \text{Im} \{ \gamma Z \} / \omega \quad (4.11)$$

$$G = \text{Re} \{ \gamma / Z \} \quad (4.12)$$

$$C = \text{Im} \{ \gamma / Z \} / \omega \quad (4.13)$$

Based on the above mathematical relationships, we aim to obtain the S-parameters of the test structure with NW-ACF interconnects from two-port measurement system and further extract the R , L , C and G parameters from the measured data.

4.4.1 Test Structure and Measurement

The RF test die module designed in this work to evaluate the high frequency characteristics of the NW-ACF interconnects are illustrated in Fig. 4.31 (a) and (b). The test structure is a GSG (Ground-Signal-Ground) coplanar configuration, where the central line is the signal line and two side lines are used as the ground lines. The probe pads are designed at the two ends of the lines and fitted to connect with 125- μm pitch Cascade GSG probes. For the bonded sample, the NW-ACF is interconnected between the top and bottom die, as illustrated in Fig. 4.31 (c). The test structure was connected to an Agilent E8361A Vector Network Analyser (VNA). The network analyser is PC-controlled under Wincal software [208] and the S-parameters can be obtained across the frequency range of 10 MHz to 67 GHz. In this work, the S-parameters were measured in the frequency range of 100 MHz to 20 GHz. Before measurement, the network analyser was calibrated using the standard calibration substrate with “open” (probes not connected) and “through” (metal shorts between port 1 and port 2 probes) structures. The open- and through-structures of GSG transmission line were also fabricated on the test die and used for de-embedding purpose of probe pads or tracks, as shown in Fig. 4.31 (d). The open-structure has an open signal line and the through-structure has the through signal and ground lines. The open- and through-structures can also be used as a control tool to measure any lossy substrate effects and as a reference line to compare with the line with the NW-ACF interconnects.

Test structures were fabricated on two types of substrate with two different metallization schemes, which are Si test die with electroplated Cu lines and Cu-In bond pads, and quartz test die with sputtered Au lines and Au bond pads. The test die were fabricated with the same masks and therefore have the same line dimensions (line length is 2.1 mm and line width is 80 μm). The specifications of the Si and quartz test die are listed in Table 4.8. The characteristic impedance of the transmission line on Si die was designed to be 50 Ω . For Si die, the Si substrate has a low resistivity of 1-10 $\Omega\cdot\text{cm}$. On top of the Si, it has a 0.5 μm thick thermal oxide layer of SiO_2 , where the metal layer was deposited or electroplated. A passivation oxide layer of 0.2 μm thick SiO_2 was sputtered on the metal lines. For quartz die,

it has a thin evaporated Ti/Au of $\sim 0.7 \mu\text{m}$ thick. The quartz substrate was used due to its high dielectric constant and high resistivity to eliminate the lossy substrate effect.

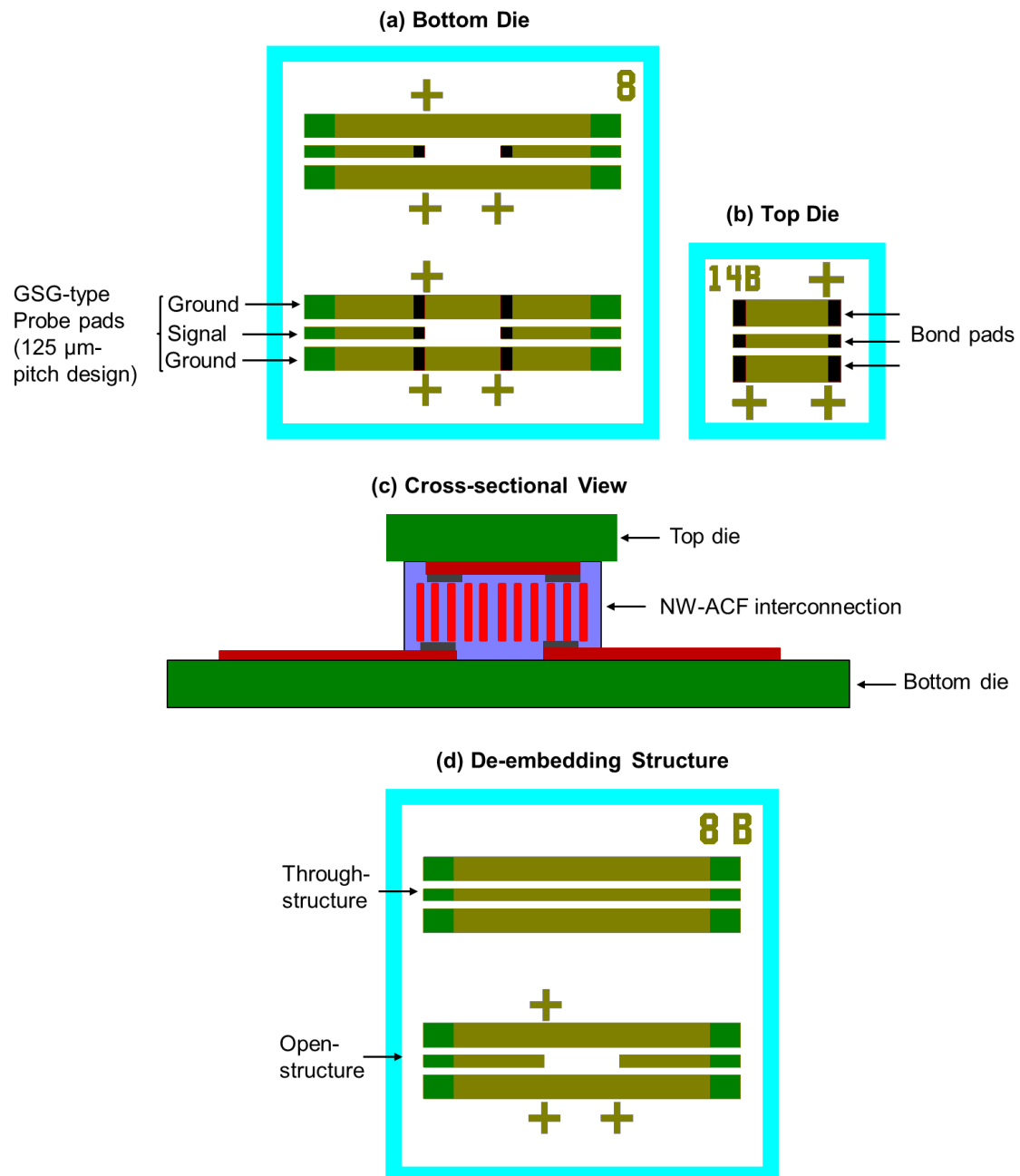


Figure 4.31 RF test die module for high frequency characterization of the NW-ACF interconnects, (a) bottom and (b) top die layout, (c) cross-sectional view of the bonded sample with NW-ACF interconnects and (d) the de-embedding “through” and “open” structure.

Table 4.8 Design parameters of the RF test die with Si and quartz substrate and the metal line dimensions.

Design Parameter	Si test die	Quartz test die
Substrate Type	Si <100> wafer	Quartz wafer
Substrate Thickness	525 μm (+ 0.5 μm SiO ₂)	500 μm
Base Metal/thickness	Sputtered Ti/Cu 0.2 μm + Electroplated Cu, ~3.5 μm	Sputtered Ti/Au, 0.7 μm
Transmission line length	2100 μm	2100 μm
Signal line width	80 μm	80 μm
Ground line width	160 μm	160 μm
Bond pad width (signal line)	80 μm	80 μm
Bond pad width (ground line)	80, 160 μm (length)	80, 160 μm (length)
Signal line-to-ground line space	46 μm	46 μm
Bond pad finish/thickness	Electroplated In, ~1.0 μm	-
Passivation on metal/thickness	SiO ₂ , 0.2 μm	SiO ₂ , 0.2 μm

4.4.2 Lossy Si Substrate Effect

The first part of the experiment was conducted with the Si test die samples. By measuring the through-line structure in the Si substrate, we found the lossy characteristics of the Si substrate [209]. The results showed reduced characteristic impedances Z_0 at low frequencies, with the impedances returning to the designed values (50 Ω) at higher frequencies. The result of the line impedance on the Si substrate is shown in Fig. 4.32 (where the measurement on the long Cascade impedance standard substrate, ISS, line is also shown).

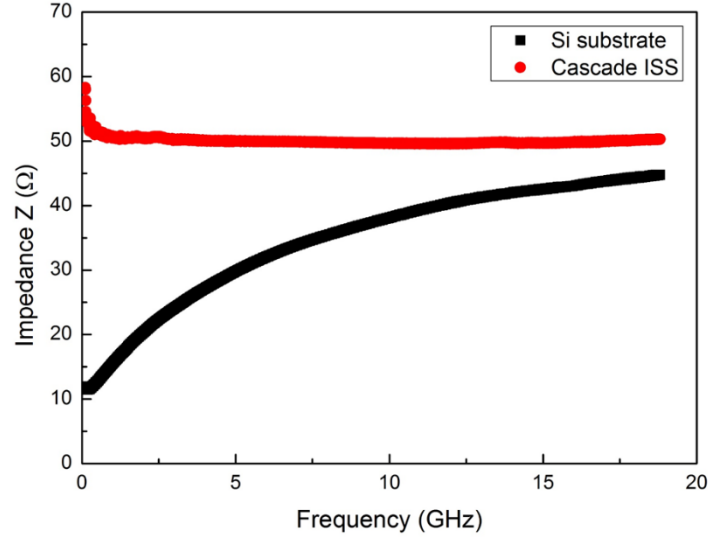


Figure 4.32 Transmission Line Impedance of Si substrate as compared to Cascade ISS line.

The Si wafer has a resistivity specification in the range 1-10 Ω cm and 0.5 μm of SiO_2 deposited on top. Consequently, it would be expected to have the additional transverse elements due to the lossy characteristics of the Si substrate that must be added to the conventional RLCG transmission line model. Fig. 4.33 (a) shows the additional resistance and capacitance elements induced by the low resistivity Si in the GSG test structure as R_{leak} and C_{ox} . The equivalent distributed transmission line model is shown in Fig. 4.33 (b). The transmission line equations are therefore reworked to include R_{leak} and C_{ox} in the usual distributed RLCG model as:

$$G \rightarrow G + \frac{R_{leak}}{R_{leak} + \frac{1}{C_{ox}^2 \omega^2}} \quad (4.14)$$

$$C \rightarrow C + \frac{C_{ox}}{1 + C_{ox}^2 R_{leak}^2 \omega^2} \quad (4.15)$$

Thus, the characteristic impedance of the line Z_0 can be expressed as:

$$Z_0 = \sqrt{\frac{(R + i \omega L)(1 + i C_{ox} R_{leak} \omega)}{G + i \omega (C + C_{ox} + C_{ox} G R_{leak}) - \omega^2 C C_{ox} R_{leak}}} \quad (4.16)$$

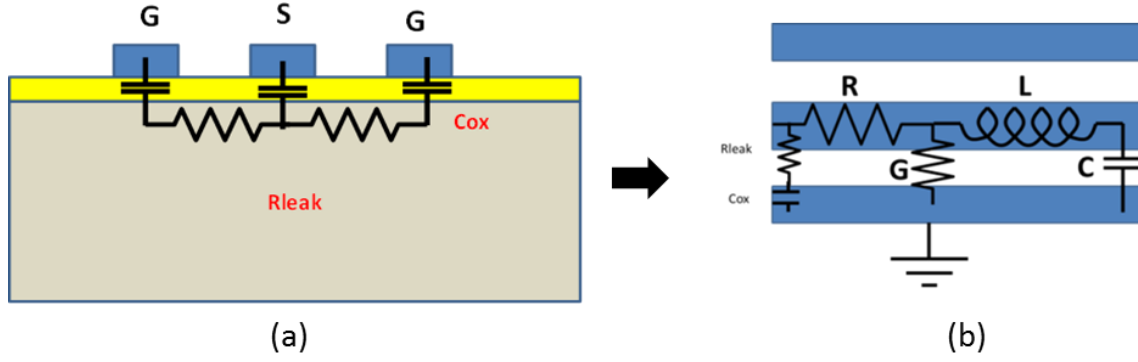


Figure 4.33 Schematics showing (a) the additional transverse elements R_{leak} and C_{ox} in the test GSG test structure on the lossy Si substrate and (b) the equivalent distributed transmission line model.

There are now 6 parameters R, L, C, G, R_{leak} and C_{ox} instead of the four parameters R, L, C, G that directly impact the four measured S parameters of $\text{Re}[S_{11}]$, $\text{Im}[S_{11}]$, $\text{Re}[S_{12}]$ and $\text{Im}[S_{12}]$ (S_{22} and S_{21} are assumed to be the same as S_{11} and S_{12} due to symmetry of the test structure). The measured S-parameters are plotted in the polar chart as shown in Fig. 4.34. The circuit implication of this is that since the transmitted power goes with $(\text{Abs}[S_{21}])^2$, above the hook frequency in S_{21} (in this case about 2 GHz), only approximately 36% of the power is fed along the line. Due to the lossy characteristics of the Si substrate, the RF characteristics of the transmission line on the Si test die cannot be correctly obtained. Hence, only lossy characteristic effect of the Si test die could be confirmed in this part of work.

Further, the RLCG parameters were extracted from the S-parameters using eq. (4.7) to (4.13). The obtained data on the lossy Si substrate (to 20 GHz) gives parameter values $R = 597 \Omega/\text{m}$, $L = 3.9 \times 10^{-7} \text{ H/m}$, $C = 0.16 \text{ nF/m}$, $G = 0.7 \text{ S/m}$. The parameters R_{leak} and C_{ox} can be obtained using eq. (4.14) and (4.15): when $\omega \rightarrow 0$, $C(\omega \rightarrow 0) \rightarrow C + C_{ox}$, C_{ox} can be obtained by $C(\omega \rightarrow 0) - C$, where $C(\omega \rightarrow 0)$ can be regarded as C value at the lowest frequency; when $\omega \rightarrow \infty$, $G \rightarrow G + \frac{1}{R_{leak}}$, R_{leak} can be obtained by $\frac{1}{G(\omega \rightarrow \infty) - G}$, where $G(\omega \rightarrow \infty)$ can be regarded as G value at the highest frequency. Therefore, the obtained values are $C_{ox} = 3.37 \text{ nF/m}$ and $R_{leak} = 0.085 \Omega/\text{m}$. The verification of the extracted parameters was conducted by calculating the S-parameters based on the above values and the calculated S-parameters are plotted in the same polar plot as shown in Fig. 4.34. From the graph, the measured data and the simulated data (using the modified transmission line model) show a good fitting, which validates the electrical models and the extracted values. Z_0 value

can also be verified using the extracted parameters using eq. (4.16). The measured value and the calculated values are compared in Fig 4.35, which shows a good fitting. It is interesting to note that as the frequency increases, S_{11} returns to the origin and Z_0 becomes 50Ω . This can be explained by when $\omega \rightarrow \infty$, $Z_0 = \sqrt{\frac{L}{C}}$ and $C(\omega \rightarrow \infty) \rightarrow C$, the line impedance returns to the designed value of 50Ω and the reflection caused by Si substrate becomes less dominating.

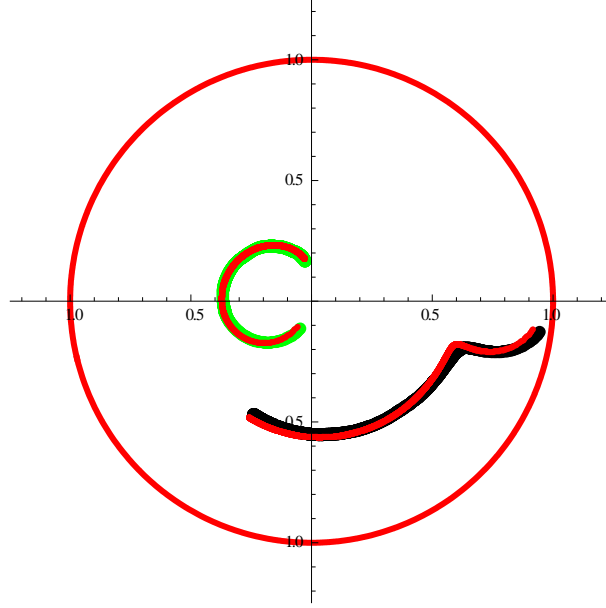


Figure 4.34 Measured S-parameters (Red) and the simulated S11 (Green) and S12 (Black) showing a good fitting.

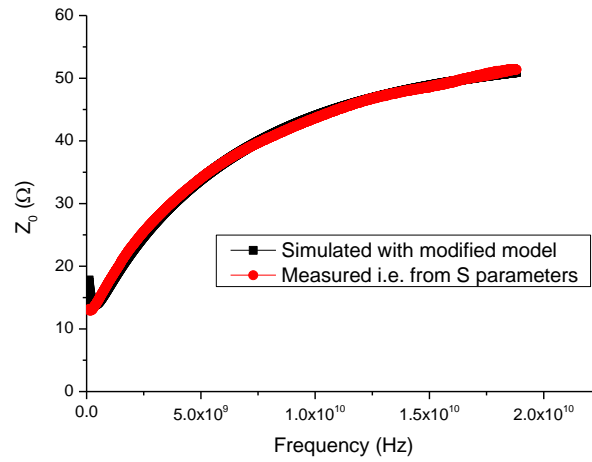


Figure 4.35 Measured (red) and simulated (black) transmission line characteristic impedances showing a good fitting.

4.4.3 RF Property of the NW-ACF Interconnects on Quartz Substrate

The second part of the experiment was conducted with the quartz test die samples. The characteristic impedance Z_0 of the through-line on quartz substrate shows a steady value of $\sim 90 \Omega$ in the measured frequency range of 0.1 to 20 GHz, as shown in Fig. 4.36. However, as compared to the Cascade ISS lines, the Z_0 value of the transmission line on quartz is no longer 50Ω . This is mainly due to the changed dielectric constant of the substrate from Si to quartz. Nevertheless, the mismatched Z_0 value will not affect the accuracy of the measured S-parameters from the network system. With no lossy characteristics of the quartz substrate, the S-parameters of the transmission line with the NW-ACF interconnects can be reasonably obtained and the respective line parameters of R , L , C and G can be extracted from S-parameters using eq. (4.7) to eq. (4.13). Meanwhile, a comparison study was carried out with the solder-bump interconnects on the same test die. Instead of the NW-ACF applied in the whole bonding area between the top and bottom die, $50\text{-}\mu\text{m}$ diameter solder bumps are deposited only on the bond pads and reflowed at temperature of $\sim 270^\circ\text{C}$ to make the connection.

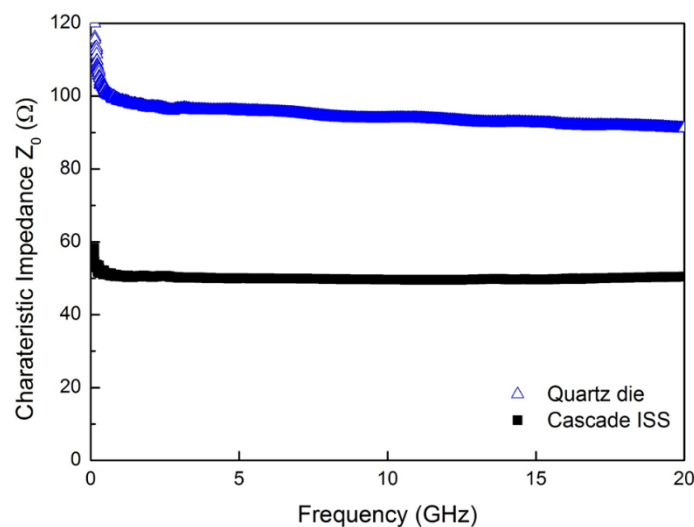


Figure 4.36 Transmission Line Impedance of quartz substrate as compared to Cascade ISS line.

Fig. 4.37 shows the extracted resistance, R of the through line (no flip-chip interconnects) on quartz and the line with the NW-ACF and solder-bump interconnects. From the graph, R of the line with the NW-ACF interconnects shows a generally higher value than the R value of the through-line and the line with the solder-bump interconnects at all frequencies. The

higher value of R for NW-ACF interconnects could be due to a higher contact resistance of the NW-ACF interconnects as compared to that of the reflowed solder joints. At the low frequency (100 MHz), R of the line with the NW-ACF interconnects is $3.3\ \Omega$ for the specific line length. This value corresponds well with the measured DC resistance $\sim 2.5\ \Omega$. For all three lines, R values were found to increase with the frequency till ~ 8 GHz. This can be explained by the skin effect of the transmission line (i.e. the electric field of a transverse electromagnetic wave propagating through a conductor dies off exponentially from the conducting boundaries to the center of the conductor, so at high frequency, the waves effectively travels along the outside edges or skin of the conductor.) However, at higher frequency R values show abnormal behavior by dropping below zero. This phenomenon is interpreted as the R values being too small to be correctly measured by the network system. As the actual resistances of the line and the interconnects can be just several tens or hundreds of $m\Omega$, only a four-probe measurement will be able to precisely measure the R value by excluding the cable and probing resistance as existing in the current measurement system. Therefore, only the R values obtained at a relatively low frequency ($R = 2.2\ K\Omega/m$, at 8 GHz) are used as the valid data and verified by re-calculating the S-parameters.

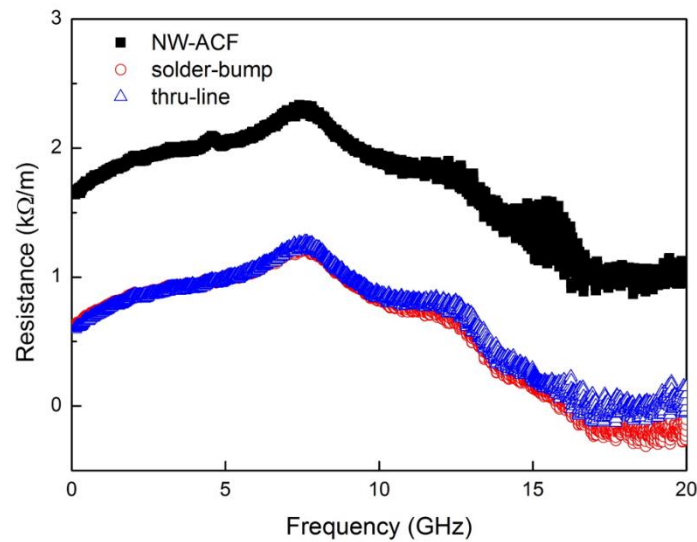


Figure 4.37 Resistance, R per unit length of the through line, the line with the NW-ACF interconnects and the line with the solder-bump interconnects as a function of frequency.

Fig. 4.38 show the extracted inductances, L of the through line, the line with the NW-ACF interconnects and the line with the solder-bump interconnects, respectively in all frequencies. For all line types, L values show no substantial differences. L obtained for the line with NW-ACF interconnects is $0.42 \mu\text{H/m}$ at 20 GHz.

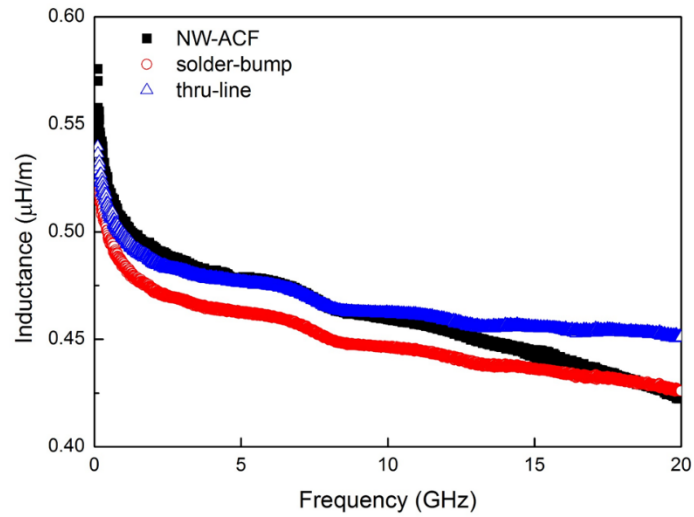


Figure 4.38 Inductance, L per unit length of the through line, the line with the NW-ACF interconnects and the line with the solder-bump interconnects as a function of frequency.

Fig. 4.39 shows the extracted capacitance, C of the through line, the line with NW-ACF interconnects and the line with the solder-bump interconnects at all frequencies. From the graph, it shows a substantial difference for the three line types. Among them, the through line has the smallest C value. At 20 GHz, C for through line is 54.3 pF/m . C values of the line with the solder-bump interconnects are generally higher than C of the through line. At 20 GHz, C for solder-bump line is 71.9 pF/m . The increase of C for the line with the solder-bump interconnects as compared to the through line is due to adding the bump capacitance in the circuit. While for the line with the NW-ACF interconnects, the C values are the highest. At 20 GHz, C for the NW-ACF line is 96.3 pF/m . The highest value of C for the line with the NW-ACF interconnects can be attributed to the fact that the NW-ACF material was applied over the entire die area. The parallel nanowires existing between the signal and ground line can generate a number of small parasitic capacitances and add to the total capacitance. Fig. 4.40 (a) illustrates the NW-ACF applied between the signal and ground line and (b) gives an equivalent circuit model to show the capacitance induced by nanowires C_{NW} in the circuit. Although the NWs can add $\sim 25 \text{ pF/m}$ ($\sim 34\%$ increase of) parasitic capacitance to the

transmission line as compared to solder interconnects, the effect is not significant to influence the overall transmission line properties (no obvious change in S-parameters as compared to other two line types) at high frequencies.

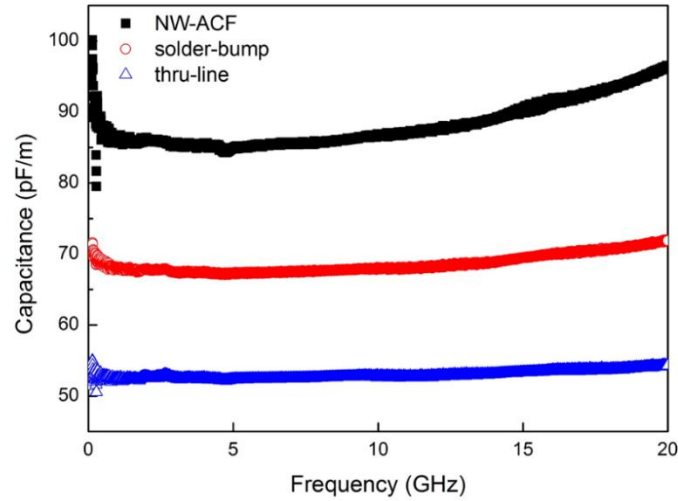


Figure 4.39 Capacitance, C per unit length of the through line, the line with the NW-ACF interconnects and the line with the solder-bump interconnects as a function of frequency.

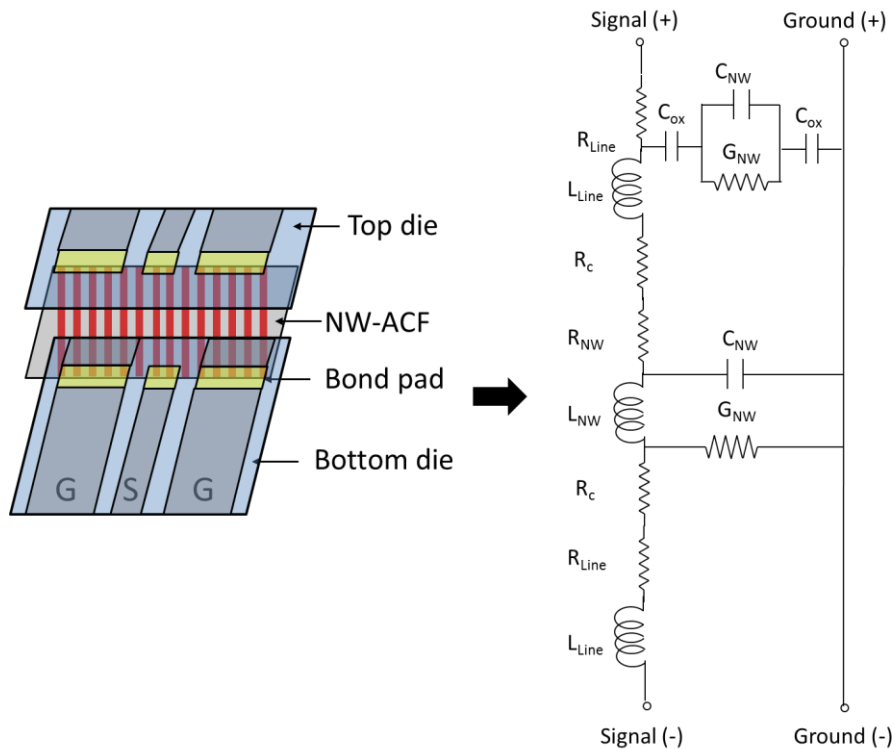


Figure 4.40 Schematics showing the vertical NW-ACF interconnects between the top and bottom die with GSG transmission lines and the equivalent circuit model between the signal line and a ground line. (Note that only half of the line and interconnection and the most front layer of the NW-ACF are shown in the image.)

Fig. 4.41 compares the extracted leakage conductance, G of the through line and the line with the NW-ACF interconnects and the line with the solder-bump interconnects respectively in all frequencies. The leakage conductance for all line types gradually increase with the frequency and have no substantial difference for different line types. For the line with the NW-ACF interconnect, G value is ~ 0.5 mS for the specific long length at a frequency of 20 GHz.

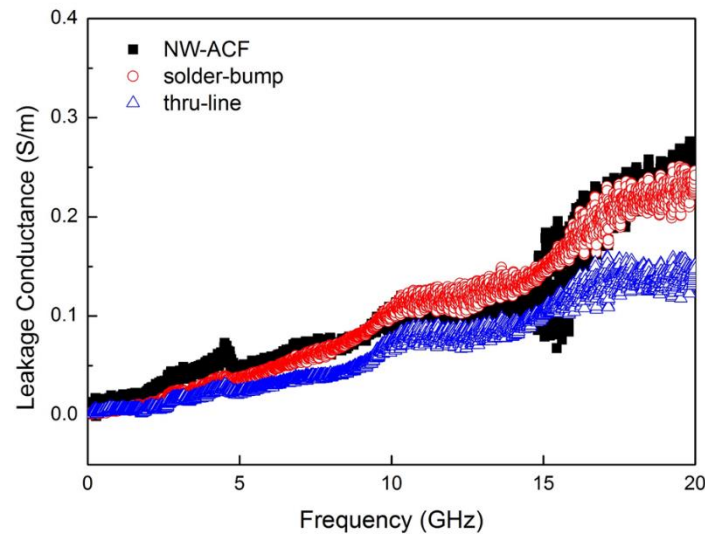


Figure 4.41 Conductance, G per unit length of the through line, the line with the NW-ACF interconnects and the line with the solder-bump interconnects as a function of frequency.

The above extracted parameters for the line with the NW-ACF interconnects were further verified by re-calculating the S_{11} and S_{12} using eq. (4.5) to (4.9) and plotted in the polar plot to show the fitting with the measured S-parameters, as shown in Fig. 4.42. The good fitting between the measured data and the calculated data validates the extracted values of the RLCG. Finally, the magnitudes of the S_{11} and S_{21} which represent the reflection and insertion loss of the line with the NW-ACF interconnects are shown in Fig. 4.43 and compared to the line with solder-bump interconnects. The line with the NW-ACF interconnects shows a low insertion loss (magnitude of S_{21}) < 1 dB up to the frequency of 20 GHz. It is also evident that the transmission line with the NW-ACF interconnects has a comparable high frequency performance to its solder-bump counterpart.

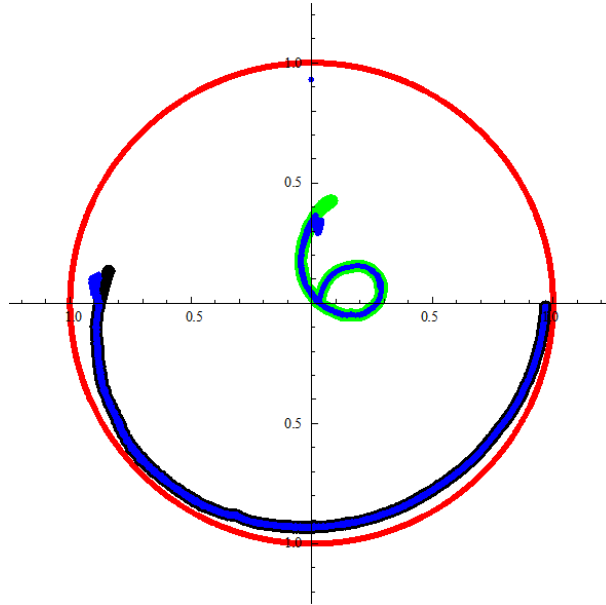


Figure 4.42 Measured S-parameters (blue) of the line with the NW-ACF interconnects displayed in the polar plot and the simulated S11 (Green) and S12 (Black) based on the RLCC values showing a good fitting.

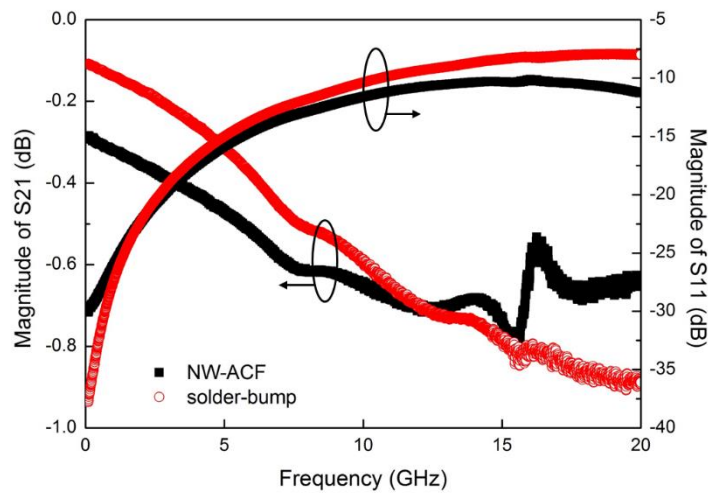


Figure 4.43 Magnitude of S21 and S11 of the line with NW-ACF interconnects and solder bumps as a function of frequency.

4.5 Thermal Performance of the NW-ACF Interconnects

For chip stacking architecture in System-in-Package (SiP), two of the difficult challenges are heat-dissipation design and heat-isolation design between the stacked dies with different maximum operation temperatures, according to the ITRS report in 2012 [210]. The typical

maximum junction temperature (T_{j_max}) for a microprocessor is about 100 °C and that for a memory device is about 85 °C. To dissipate the heat from the power device through the heat spreader (normally placed on the top of the stacked die) and heat sink and to maintain all die in the stack at acceptable junction temperature, thermal interface material (TIM) with low thermal resistance are usually used. For the 3D ICs, the hot spot with a power density up to 500 W/cm² can be generated in the module, which magnifies the cooling challenges by stressing the demand for the improvement in heat sink, heat spreaders and thermal interface material with a high thermal conductivity and low contact thermal impedance. To further enhance the heat transfer, different solutions were explored including the embedded thermal cooling technologies within the stack by constructing the “thermal TSVs” to enable “routing” of the heat to the top of the stack and the inter-layer microfluidic liquid cooling technologies using micro-channels or micro pin fin array [211].

On the other hand, increasing the thermal conductivity of the chip to chip interfaces in the 3D stack by optimizing the thermal performance of the interconnection material would be beneficial in 3D thermal management. For the current prevailing μ bump interconnects, the solutions would be designing additional metal bumps for thermal conduction purposes and using high conductivity underfill material to enhance the thermal conductivity. As a competing technology proposed in this work for fine-pitch chip-to-chip interconnects, the NW-ACF formed interconnects have shown a good electrical performance as compared to the conventional ACF in the last sections. The thermal performance of the NW-ACF interconnects in the bonded Si chips with Cu-In pads was also studied and compared to that of conventional ACF by thermal impedance measurement in the following sections.

4.5.1 Experiment Setup

A modified ASTM D5470-06 standard setup was employed for thermal impedance measurement as reported by Xu et al. [174]. A detailed drawing of the experimental setup is shown in Fig. 4.44, where different components are numbered to describe the setup. The meter bars (7) are made of two round copper C11600 rods 60 mm long and 20 mm-diameter and have a nominal thermal conductivity of 388 Wm⁻¹K⁻¹ at 25 °C. The contact surfaces were ground with a Buehler grinder apparatus and polished with 1 micron diamond paste to get a mirror finish. From atomic force microscope (AFM) measurement, the surface of the copper calorimeter has an RMS (root-mean-square) roughness of 88 nm. Eight 0.5 mm diameter thermistors were embedded within the bars to measure the thermal gradients with an accuracy

of $\pm 0.01\text{ }^{\circ}\text{C}$, between $0\text{--}70\text{ }^{\circ}\text{C}$. Calibration of the thermistors was performed with a Hart Scientific 5611T model reference probe with an absolute calibrated uncertainty of $0.002\text{ }^{\circ}\text{C}$. The thermistor resistances were recorded using two National Instruments DAQ-mx USB cards, each equipped with 4-channels and each in 4-wire resistance configuration using a built-in low excitation current. Cooling of the lower meter bar was provided by a Lauda thermal bath constant-temperature cooler loop whose stability was $\pm 0.02\text{ }^{\circ}\text{C}$. The upper meter bar was heated using an aluminum heater block with two internal 250 W cartridge heaters controlled by a Red-Lion PID controller. The heater block was attached to an AST KAF-S Load Cell with rated load of $2\text{ kN } \pm 0.2\%$ (11). The load cell, in turn, was then attached to Nanotec Ball Screw Linear Actuator, which can apply a maximum force of 1.8 kN onto a surface of $3.14 \times 10^{-4}\text{ m}^2$. Furthermore, the actuator (15) has a minimum step size of $1\text{ }\mu\text{m}$ resolution. The distance between the two mating surfaces of the bars was measured using an MX-Metralight laser micrometer (10) with a $0.4\text{ }\mu\text{m}$ resolution and thereby the bond line thickness (BLT) of the sample could be measured in situ. During testing, the meter bars were wrapped in an insulating material (not shown) to minimize heat losses. Calibration of the test facility was carried out by machining 4 stainless steel (303 grade) disks of different thicknesses with a nominal thermal conductivity of $15.10\text{ Wm}^{-1}\text{K}^{-1}$ at $29.27\text{ }^{\circ}\text{C}$. By measuring the thermal impedance of the steel disk with the different thicknesses, the effective thermal conductivity can be extracted as the slope of the thermal impedance data as a function of the disk thickness, which is $15.01\text{ Wm}^{-1}\text{K}^{-1}$. The discrepancy is within 0.59% of the manufacture's value and therefore validates the measurement accuracy.

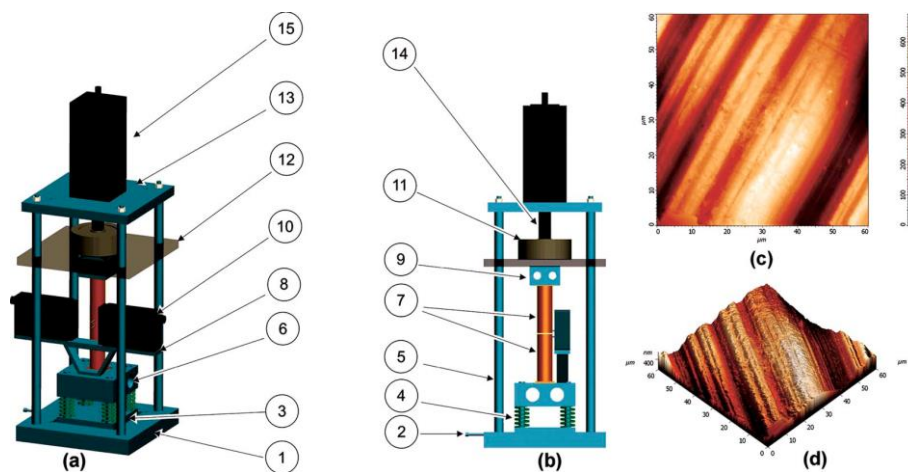


Figure 4.44 CAD design of the experimental apparatus [172]. (a) Front view and (b) side view of the apparatus: (1) aluminum plate, (2) fine threaded linear screw for x-y displacement, (3) insulating Perspex plate, (4) compression springs, (5) aluminum shafts, (6) aluminum

cooler block, (7) copper bars, (8) micrometer stand, (9) Peltier cell and heat, (10) laser micrometer, (11) load Cell, (12) Perspex plate, (13) steel plates, (14) stainless steel ball screw and (15) linear actuator. (c) and (d) show the representative topographic and the 3D topographic images of the surface of copper calorimeter.

4.5.2 Thermal Impedance of the NW-ACF Interconnects

The thermal impedance of the NW-ACF bonded test module 1 (Si chips with Cu-In bond pads) was measured using the test system described above. The test was conducted at room temperature with a pressure applied from 0.1 to 1 MPa in order to minimize the contact impedance between the Si die surfaces and the Cu bar surfaces. Meanwhile, some highly thermal conductive paste (TIM paste) was applied between the Si and Cu surfaces to further reduce contact impedance. The same test module bonded with the particle-ACF was measured to compare to the bonded sample with the NW-ACF. Fig. 4.45 shows the thermal impedances as a function of pressure for the NW-ACF and particle-ACF bonded samples.

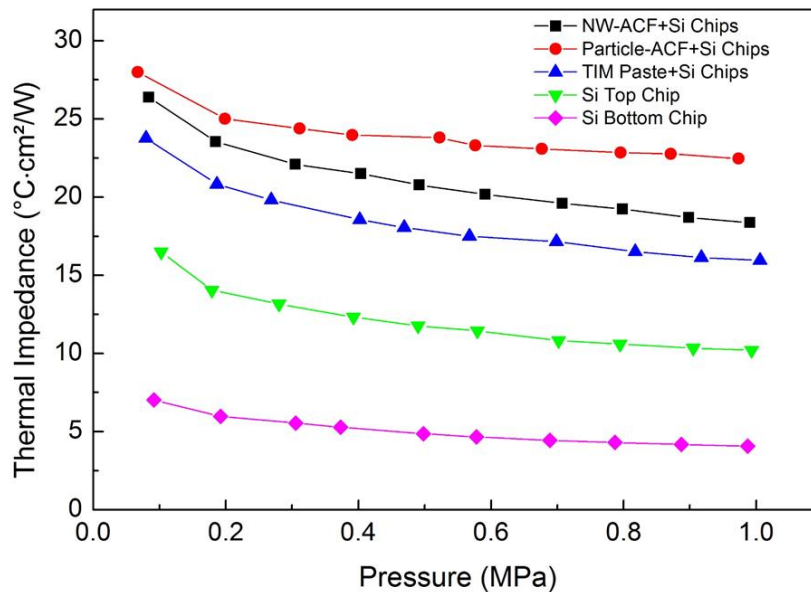


Figure 4.45 Thermal impedance of the NW-ACF bonded test module 1 with Cu-In pads (black), comparing to the same bonded test module with particle-ACF (red) and with the commercial TIM paste (blue). The thermal impedance of the top (green) and bottom chip (magenta) of the test module was measured as the references.

It was found that with an increased pressure, the thermal impedences were gradually reduced for both the NW-ACF and the particle-ACF bonded samples, which can be attributed to the lower contact impedences at all contact interfaces at a higher pressure. By comparing the NW-ACF and particle-ACF bonded samples, the thermal impedences of the former are lower than the latter at all pressure values. The minimum thermal impedences that achieved for the NW-ACF and the particle-ACF bonded samples at 1 MPa are 18.38 and 22.47 °C cm²/W, respectively. With the same bonded chip system, the thermal impedance of the NW-ACF formed interconnects is therefore ~ 18% lower than that of the particle-ACF formed interconnects.

Furthermore, a commercial TIM paste has been applied between the same test chips to compare the thermal impedance of the system to the NW-ACF bonded sample, as shown in the same graph of Fig. 4.32. For the commercial TIM paste based interconnect, the thermal impedance of the system at 1 MPa pressure is 15.97 °C cm²/W, which is ~ 13% lower when compared to that of the NW-ACF interconnects. This is due to the fact that commercial TIMs are loaded in excess of 60% with conductive particles [212]. It should also be noted that the TIMs are not designed for electrical interconnection purpose, because they are either electrically insulating (when non-metallic particles are loaded) or isotropic conductive (when the metallic particles are loaded) and thereby cannot be used as an ACF.

4.5.3 Thermal Impedance Models

As the total thermal impedance due to the TIM insertion (Θ_{TIM}) between the two mating surfaces can be retrieved as [212]:

$$\Theta_{TIM} = \frac{BLT}{k_{TIM}} + \Theta_{c1} + \Theta_{c2} \quad (4.1)$$

where Θ_{c1} and Θ_{c2} represent the contact impedences of the TIM with the two bounding surfaces, k_{TIM} is the thermal conductivity of the TIM and BLT is its bond line thickness. The same formula can be applied for the ACF based interconnects under thermal consideration. Therefore, for the ACF material as a good thermal interconnection, a high intrinsic thermal conductivity of the ACF and low contact impedences to the bonding surfaces are mostly desirable. According to Nan's model [213], the thermal conductivity of the carbon nanotube (CNT)-based composites is proportional to the thermal conductivity of the CNT and the

fractional volume content of the CNT in the polymer. This is assumed to be the same for the thermal conductivity of the metallic nanowire-polymer composite material with a similar structure as that of the CNT-polymer composite. For the contact impedance, the model proposed by Vishal et al. [214] can be used, where the mechanical properties of the composite material, i.e. Young's modulus and Poisson's ratio have significant influence on the contact impedance in addition to thermal conductivity of the material. It is reported by Xu et al. [174] that Ag nanowire based polycarbonate material with a filling ratio of $\sim 9\%$ can result in a much lower contact impedance (due to its lower Young's modulus) and therefore a lower total thermal impedance to that of the CNT-polymer composite material with the same filling ratio. In a similar way, Cu NW-ACF in this work is assumed to have a comparable or better intrinsic thermal impedance, due to its higher filling ratio ($\sim 12.5\%$) than that of Ag ($\sim 9\%$) and a comparable thermal conductivity of Cu (401 W/m K) to that of Ag (429 W/m K). Despite the fact that the Young's modulus of Cu (117 GPa) is higher than that of Ag (63 GPa), it is still nearly 7 times lower than CNT (800 GPa). Therefore, a low contact impedance of Cu NW-ACF to the bonding surfaces can be expected. Compared to the metallic particles used in the particle-ACF, the metallic (Cu, Ag) NW arrays are expected to be more effective thermal conduits due to their inherent continuity, vertically-aligned orientation and their ability to conform to micron-scale unevenness of the mating surfaces [215]. All the above theories can explain satisfactory thermal impedance achieved by the NW-ACF interconnects as shown in Fig. 4.31.

4.6 Conclusions

In conclusion, Cu nanowire based ACF has shown satisfactory electrical and thermal performance as the fine-pitch chip-to-chip interconnects. The template based open/short failure screened out the electrically workable NW-ACF C, due to its suitable porosity, few overlapping pores and smooth surface as compared to NW-ACF A and B. The minimum pad/pitch size achieved for NW-ACF bonding was $10/30 \text{ }\mu\text{m}$. The average daisy-chain resistance for the NW-ACF interconnects with Cu-In pads was $0.03\text{-}0.04 \text{ }\Omega$ per interconnect (for $10\times 10 \text{ }\mu\text{m}^2$ pad). In the bonding experiments with Cu-In pads, it was found that a small bondline thickness of the NW-ACF, formed at a sufficiently high temperature and force, generally resulted in a low interconnection resistance due to the bending of the nanowires.

The NW-ACF has also been successfully bonded with Au bumpless dies, where a comparably low interconnection resistance of $0.09\ \Omega$ (for $40\times 40\ \mu\text{m}^2$ pad) was achieved with a relatively small bonding force and no significant bending of the nanowires. When compared with the commercial particle-based ACF, NW-ACF showed the superiority in terms of electrical (finer pitch capability, lower interconnection resistance and smaller bonding force) and thermal (lower thermal impedance) performance. The leakage current in the NW-ACF interconnects was found to be higher than that of the particle-based ACF. This was attributed to the non-parallel pore structure of the template, which results in the existence of overlapping nanowires in the NW-ACF film. The improvement on the pore characteristics of the polymeric template is therefore key to improve the insulation properties of the NW-ACF material in future development. Moreover, the transmission line with NW-ACF interconnects showed good high frequency performance as compared to the line with solder bumps. The line parameters of RLGC were extracted based on the measurement of S-parameters up to 20 GHz.

Chapter 5 Mechanical and Reliability Properties of the NW-ACF Interconnects

5.1 Introduction

Semiconductor packaging technologies are exposed to various environments, such as temperature, humidity, dust, shock and vibration and the main causes for failure of electronic package are reported to be temperature fatigue (55%), vibration fatigue (20%), humidity (19%) and dust (6%) [216]. Solder joints/bumps are the most prevailing interconnection method that provide the mechanical and electrical connections at the die, substrate and board levels, which are all susceptible to failure during the harsh environment, including cyclic thermal exposure, mechanical shock and humidity. For solder bumps, the fluctuations of temperature result in thermal expansion mismatch between the various package materials and the stress and strain accumulated in the soldered joints, which induce fatigue cracks [217]. On the other hand, the effects of humidity on the solder bumps mainly originate from the underfill or non-conductive adhesive (NCA) materials used in the joint. The adhesion strength of the polymer is deteriorated due to moisture absorption, which cause delamination and therefore oxidation of the joint metals [218-220]. Meanwhile, the mechanical reliability of solder joints relies mostly on the ductile part of solder and the brittle part of IMCs, where the fractures can occur due to mechanical loading [221, 222].

ACA/ACF material as an alternative replacement to solder has found various applications for temperature sensitive devices or processes, such as chip on flexible substrate, glass and chip-on-chip. Failures in ACF interconnection have been reported due to the factors including oxidation of conductive particles, initial misalignment due to coplanarity issues, thermal stress due to CTE mismatch, post assembly residual compressive stresses as well as polymer expansion due to moisture absorption and degradation of the polymer at high temperature [98]. When conductive adhesive interconnects are subjected to cyclical thermal stress, interfacial delamination and fracture can occur due to the thermo-mechanical stress caused by CTE mismatch, variations in elastic modulus and interfacial adhesion strength, all of which directly influence the electrical performance of the interconnects [101-103]. The other environmental factor to impair the ACA interconnects is humidity. Under a humid

environment, the ACA matrix absorbs water, which weakens the mechanical properties of the polymer [104, 105]. Moreover, the moisture absorption causes swelling and hygroscopic stresses in the bonding structure, which leads to the permanent failure of interconnects [106, 107]. For ACF interconnects especially used in portable devices, the major mechanical impacts are from accidental drop [223]. By conducting die shear test, the basic failure modes are reported as cohesive and adhesive failure [107, 223]. The former is the internal fracture of the cured ACA material, and the latter occurs in the interface between the ACA and the bonding surfaces.

In this chapter, the mechanical reliability of the NW-ACF interconnects was evaluated by the die shear test. The shear strengths of the interconnects were correlated with the fracture mode to understand the failure mechanism. Environmental acceleration tests were performed in terms of thermal shock test and high temperature and humidity tests. The electrical performance of the bonded test die under the respective test conditions was studied in terms of contact resistance shift and open/short failures. Failure analysis was conducted by the means of cross-sectional and fractural surface analysis. A comparative study was carried out with a commercial particle-based ACF, which gives an insight into possible awareness for the further improvement of the NW-ACF material.

5.2 Mechanical Properties of the NW-ACF Interconnects

5.2.1 Die Shear Strength of the Daisy-chain Modules

For the mechanical evaluation of the NW-ACF interconnects, a die shear test was conducted due to the simplicity of the method and its convenient implementation. The NW-ACF interconnects formed with the Cu-In pads on a Si die were prepared for die shear test. The test was performed with a ROYCE 550 system with a 20 kg cartridge. The tool was positioned at a distance of 30 μm above the surface of the bottom chip, and moved horizontally at a speed of 25 $\mu\text{m/s}$ while contacting on edge of the top die (schematics shown in Fig. 3.26). The shear force was recorded when the top die was detached from the bottom die.

The test modules 1-3 (as describe in Table 4.1) with different pad size of 80, 40 and 20 μm were evaluated. Test modules 1 and 2 have a bonding area of 6.25 mm^2 and the test module 3 has a bonding area of 1.21 mm^2 . The samples were bonded under a conditions of 220 $^{\circ}\text{C}$, 60 s, 2 N. Due to the limitation of the bonder machine co-planarity, a small bonding force was

applied in this experiment to achieve best bonding yield and consistency. 3-5 bonded samples were prepared for each test module for die shearing. Fig. 5.1 shows the averaged shear strength with error bars for the test module 1-3. The shear strength was calculated by dividing the shear force by the respective bonding area. According to the graph, test modules 1 and 2 have higher averaged die shear strengths of 5.3 and 5.9 MPa, when compared to a lower strength of the test module 3 of 3.7 MPa. The values were found generally to be lower than the shear strength of the unpatterned die bonded samples, which is ~10 MPa (in chapter 3.8.2). This could be explained by the different surface topography and the different surface material of the test die. The height of the bond pad may result in a reduced bonding area, due to the inability of the polymer to flow over the uneven surfaces. Moreover, the test die composes of the surface area of In, Cu and SiO₂ and the NW-ACF is expected to form the best adhesion to In surface due to In melting during bonding.

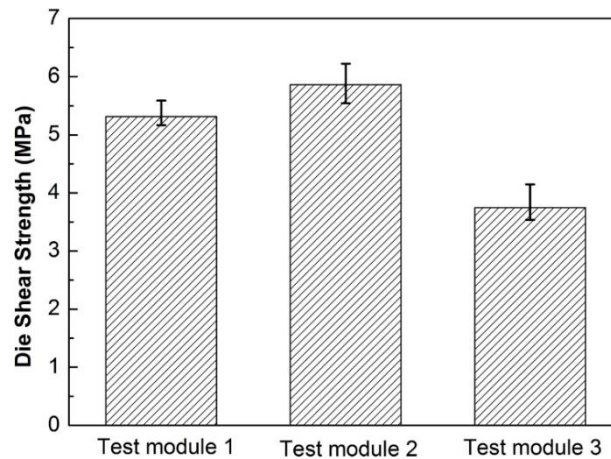


Figure 5.1 Die shear strength of the NW-ACF bonded test module 1-3.

5.2.2 Fractural Surface Analysis

Fig. 5.2 (a) to (c) shows the fractured die surfaces of test module 1, 2 and 3 under optical microscope observation. The images only show the fractured side (mostly the bottom die) with the remaining NW-ACF film. For most fractures, the detachments of the NW-ACF film from the bonding surface (of the top die) occurred and the fracture mode of the NW-ACF was interfacial adhesive failure rather than cohesive failure of the polymer itself. It can be inferred that no strong chemical bonds have been formed between the polycarbonate and the bonding surfaces, as is usually the case in common thermosetting polymer in the conventional ACAs [224]. For test module 3, it was found that many bond pads were peeled off mechanically due

to insufficient pad adhesion to the die surface, which should account for the reduced shear strength of this test module. Fig. 5.2 (a') to (c') show the corresponding SEM images of the fractural film surfaces in a single bond pad area. It was found that in the bond pad area, the fractured film surface is much rougher than that of the surrounding die (SiO_2) adhering area. Meanwhile, due to the bond pad height, the film thickness is greatly reduced in the bond pad area, which forms a concave shape as compared to the surrounding area, i.e. the ACF is “imprinted” under the bond pad area. The imprinted ACF after detachment is illustrated in Fig. 5.2 (d). Both the rough bonding surface and the height of the bond pad help to improve the adhesion of the polymer in these areas. However, the adhesion may still need to be improved in the adhering area to the die passivation surface area.

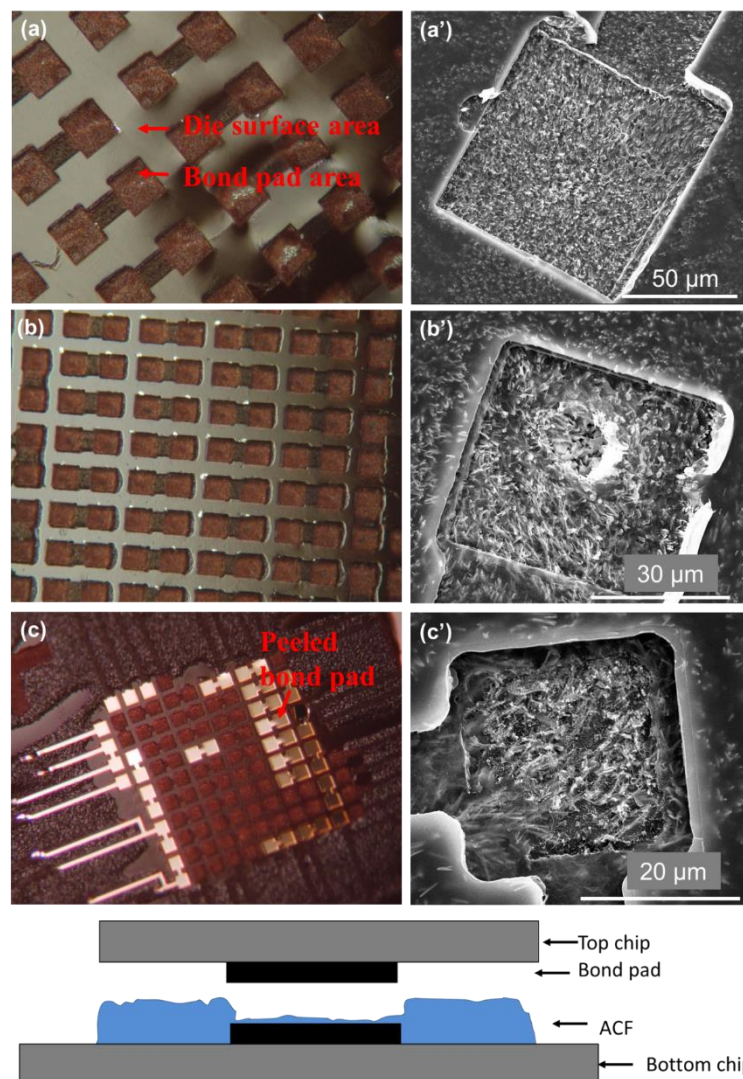


Figure 5.2 Optical image (100 \times magnification) of the fractured surfaces of (a) test module 1, (b) test module 2 and (c) test module 3. The SEM images (a') to (c') show the fracture morphology of the polymer in a single bond pad area of the corresponding dies. Schematic (d) shows the “imprinted” ACF under bond pad area.

5.3 Reliability Properties of the NW-ACF Interconnects and Failure Analysis

5.3.1 Test Methods

To investigate the reliability of the NW-ACF formed interconnects with the daisy-chain test modules, a thermal shock (T/S) test as well as high temperature and a humidity (HT/HH) test were performed according to JEDEC standard. The test conditions are listed in Table 5.1. The T/S test was conducted to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes [225]. The temperature changing rate is required to exceed 30 °C/min in a thermal shock test to differentiate it from the temperature cycling test, which is less severe. The dominating stressing mechanism in a thermal shock test is the tensile overstress and tensile fatigue resulting from the large transient thermal gradient. In this work, the T/S test was conducted in a thermal shock chamber at a temperature between -55 °C and 125 °C for 1100 cycles, according to the standard JESD22-A106B, condition C [225]. The dwell time at the maximum and minimum temperature was 15 min, and the transition time from low to high temperature was 10 s. The daisy-chain resistance was read out at the cycle intervals of 0, 100, 200, 300 and 1100 cycles, when the samples were taken out of the test chamber and measured at room temperature.

Table 5.1 Reliability test conditions.

Test method	Test condition	Stress level	Readout intervals
Thermal shock (T/S) test, (according to JESD22-A106B-C)	-55 ~ 125 °C, 10s transition, 15 min dwell at peak	1100 cycles	0, 100, 200, 300, 1100 cycle
High temperature and high humidity (HT/HH) test (JESD22-A101C)	85 °C, 85% humidity	800 hours	0, 100, 200, 300, 800 hour

HT/HH test were conducted to evaluate the reliability of non-hermetic packaged IC devices in a humid environment [226]. Temperature is known to accelerate the penetration of moisture in the IC package and along the interface between the substrate die and the

interconnection, which is detrimental to the interconnect integrity. In this work, the HT/HH test was performed using a constant temperature and humidity chamber at 85 °C/85% RH for 800 h according to the standard JESD22-A101C condition [226]. The daisy-chain resistance was read out at the cycle intervals of 0, 100, 200, 300 and 800 hour at room temperature. It should be noted that due to the resistance measurements were not conducted during reliability test, the real-time and intermittent failures between the intervals were not observed in this experiment. Further experiment with real-time resistance measurement as reported in [227] may be needed to address the other failure types.

5.3.2 Sample Parameters

It is known for conventional ACAs, the reliability of interconnects depends on the bonding parameters and materials [102]. In this work, two test die modules were mainly evaluated for their bonding reliability with the NW-ACF, which are Si die with Cu-In bond pads (as described in chapter 4.4) and quartz die with the Au bumpless pads (as described in chapter 4.5). For the quartz die, two bond pad size of 80 and 40 μm were evaluated. As a comparative study, the commercial particle-based ACF were employed to bond with all test die variations. The different group of the bonded sample for reliability test are listed in Table 5.2.

Table 5.2 Sample parameters for reliability tests.

Test module	Bond pad size (μm)	ACF Type	Sample size for T/S test	Sample size for HT/HH test
Si substrate, Cu-In pads	80	NW-ACF	4	4
		Particle-ACF	4	4
Quartz substrate, Au pads	80	NW-ACF,	2	2
		Particle-ACF	2	2
Quartz substrate, Au pads	40	NW-ACF	2	2
		Particle-ACF	2	1

For each group, 2-4 samples were prepared and tested. The influence of bonding parameters on the reliability properties were not investigated in this work. Instead, an

optimized bonding condition for 220 °C, 60 s, 2 N was used for all test modules as the best bonding yield was achieved at these parameters. For the particle-ACF, the bonding condition was set at 190 °C, 20 N, 5 s, according to the specification of the supplier information.

5.3.3 Reliability Assessments of the NW-ACF Bonded Cu-In Pads

5.3.3.1 Electrical Performance

Thermal Shock Test

Four of the NW-ACF bonded Cu-In pads samples were subjected to the thermal shock test. At the read-out cycles of 0, 100, 200, 300, 1100, the samples were taken out and the daisy chain resistance was measured. No electrical open failures were found for any samples till the cycle end. Fig. 5.3 shows the resistances in the daisy chains for one of the samples in the five readout intervals. From the graph, there is a rapid resistance increase in the first 100 cycles, as compared to the following 200 cycles. And for the last 800 cycles, the resistance data show more fluctuations to the linearized line as compared to the previous cycles, which indicates the variation of the interconnection resistance in the daisy chains after the thermal shock.

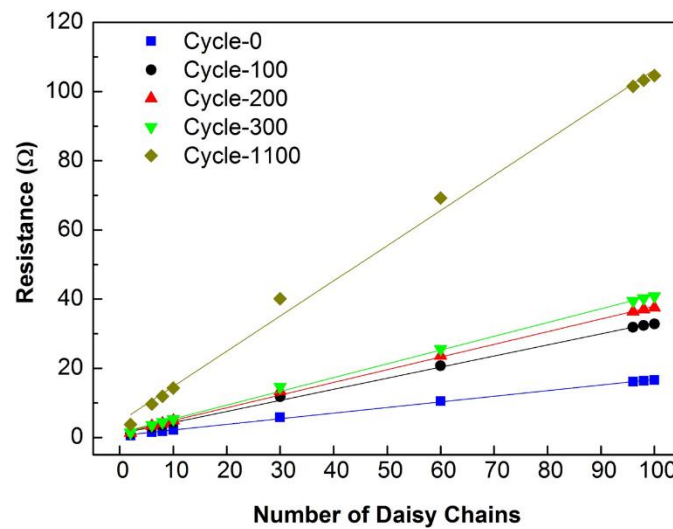


Figure 5.3 Electrical resistance in terms of number of daisy chains for a NW-ACF bonded Cu-In pads sample in the read-out cycles of 0, 100, 200, 300, 1100.

The averaged daisy-chain resistances of the four test samples were plotted in terms of the thermal cycles, as shown in Fig. 5.4. As a comparison, the results of the four particle-ACF

bonded samples are also shown in the graph. For the NW-ACF interconnects, the averaged daisy-chain resistance increases with the increased operational cycles. The resistance values of the four samples increased about 4 times from 0.1-0.2 Ω to 0.4-1.0 Ω after 1100 cycles. It was found that the higher increment rate of the resistance occurred in the first 100 cycles and the last 800 cycles, as indicated by the larger slopes of the segments of the lines. The possible reason for the rapid resistance increment in the first 100 cycles can be attributed to the initial oxidation of In (comparable to the Al pads [228]) on the bond pads, which slowed down in the following cycles. However, further study is needed to ascertain this assumption. The higher increment rate in the last 800 cycles may indicate that the degradation rate of the interconnects can increase with time.

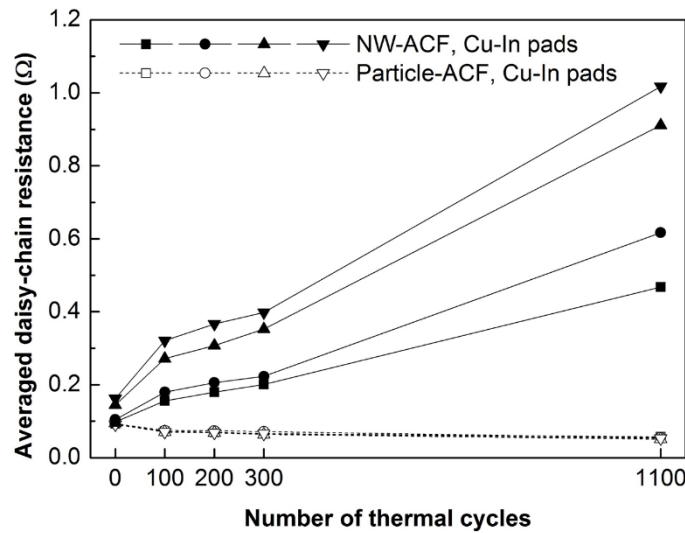


Figure 5.4 Averaged daisy-chain resistance shift of the NW-ACF bonded samples and the particle-ACF bonded samples with Cu-In pads in terms of the thermal shock cycles.

Comparatively, the particle-ACF showed a stable electrical performance till the cycle end. The resistance even slightly decreased with the ongoing cycles. The possible explanation is that at high temperature thermoset electrical conductive adhesives (ECAs) tend to post-cure, which may initially lead to smaller volume and thus lower contact resistance [229]. For the particle-ACF under study, the polymer matrix is based on epoxy, which is a thermosetting material and can be further cured at high temperature during thermal shock test and resulted in a decreased resistance.

High Temperature High Humidity Test

Four NW-ACF bonded samples with Cu-In pads were subjected to high temperature and high humidity testing at the readout interval of 0, 100, 200, 300 and 800 hours. One sample failed after 100 hours due to the electrical opens in the daisy chains. The other two samples show a dramatically increased resistance after 100 hours and electrically failed after 200 hours. Only one sample survived till the cycle end. Fig. 5.5 shows the electrical resistance shift and open occurrence of the NW-ACF bonded samples in terms of the HT/HH hours. From the graph, the initial resistances of the four samples were 0.3-0.7 Ω . Two of the samples displayed a large resistance increment to 2.5 Ω and 9.2 Ω after 100 HT/HH hours. The best performance sample shows $\sim 4\times$ resistance increase (from 0.3 to 1.4 Ω) after 800 hours. It is reported that ACF reliability is strongly affected by moisture compared to the impact of thermal excursion [98]. Compared to the samples under thermal shock test, the HT/HH samples show the early stage failures with a high failure percentage. By contrast, all particle-ACF bonded samples show a low and stable electrical resistance under hydrothermal aging. It is concluded that the electrical performance of the particle-ACF under the HT/HH testing is superior to that of the NW-ACF. The cause of high failure rate of NW-ACF interconnects under HT/HH test was further understood and discussed by bonding interface analysis in the following section.

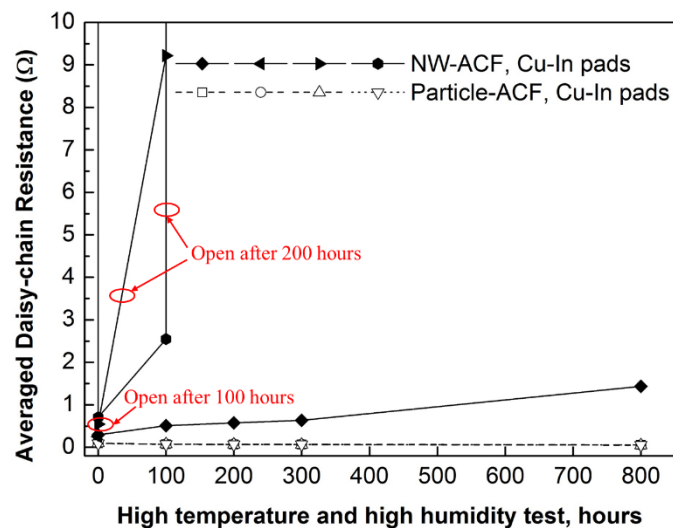


Figure 5.5 Averaged daisy-chain resistance shift/opens of the four NW-ACF bonded samples with Cu-In pads and the four particle-ACF bonded samples in terms of the time duration of high temperature and high humidity test.

5.3.3.2 Bonding Interface and Fractural Surface Analysis

Thermal Shock Test samples

The NW-ACF interconnects with the Cu-In pads were prepared for cross-sectional analysis to find the cause of the resistance increment under thermal shock test. Fig. 5.6 compares the NW-ACF interconnect before (a) and after (b) thermal shock test. To make a valid comparison, a group of micro-sections were prepared under same condition (cured in the same mould with same position of the die and polished once at a time). The magnified image shows the bondline thickness expansion of $\sim 1 \mu\text{m}$ (from $3.4 \mu\text{m}$ to $4.3 \mu\text{m}$) after 1100 thermal shock cycles. Small cracks were seen at the bonding interface of (a') and (b') and this is mostly due to the polishing related mechanical stress. The thermal expansion can be explained as: under cyclic thermal conditions, the polymer matrix of the NW-ACF was repeatedly subjected to the thermal contraction and expansion due to the rapid temperature change at the minimum and maximum temperature range [101]. As the polymer has a higher CTE as compared to the materials around it, such as Cu, In, and SiO_2 , the polymer expands due to tension stress to push the pads apart from each other at high temperature. With the expansion, the nanowires within the polymer bounced back in the thickness direction, which resulted in a reduced number and decreased contact area of the nanowires to the bonding surface and therefore an increased resistance. At low temperature, the polymer contracts and induced compressive stress, which act opposite to the contact stress of the polymer. With the cyclic expansion and contraction, the contact stresses to hold the pads together may decrease as a result of polymer fatigue and creep. On the other hand, the T_g of the polymer can be regarded as stress-free temperature of the interconnect when considering shear stress in the interconnect under cyclic temperature change. For PC, the T_g is $\sim 150^\circ\text{C}$ and the test condition temperature does not exceed the T_g in this experiment. It was reported that the shear stress in the interconnect increases with the decreasing temperature below the T_g and the higher shear stress indicates the higher probability of interconnect failure [102]. Further study on the modelling of the shear stress in NW-ACF interconnects should be carried out in future work.

Fig. 5.6 (c) shows the particle-ACF formed interconnect between Cu-In pads after 1100 cycles. Compared to the NW-ACF interconnects, the bondline thickness of the particle-ACF interconnect is kept small $\sim 1 \mu\text{m}$ even after the thermal shock test. It can be assumed that despite the particle-ACF expands and contracts under high and low temperature, the thermosetting epoxy has sufficient adhesion strength to resist the thermal stress and maintain

the proper contact. Meanwhile, as the particles in the ACF were highly compressed during bonding, it has better compliance to expansion induced by high temperature than the nanowires in NW-ACF.

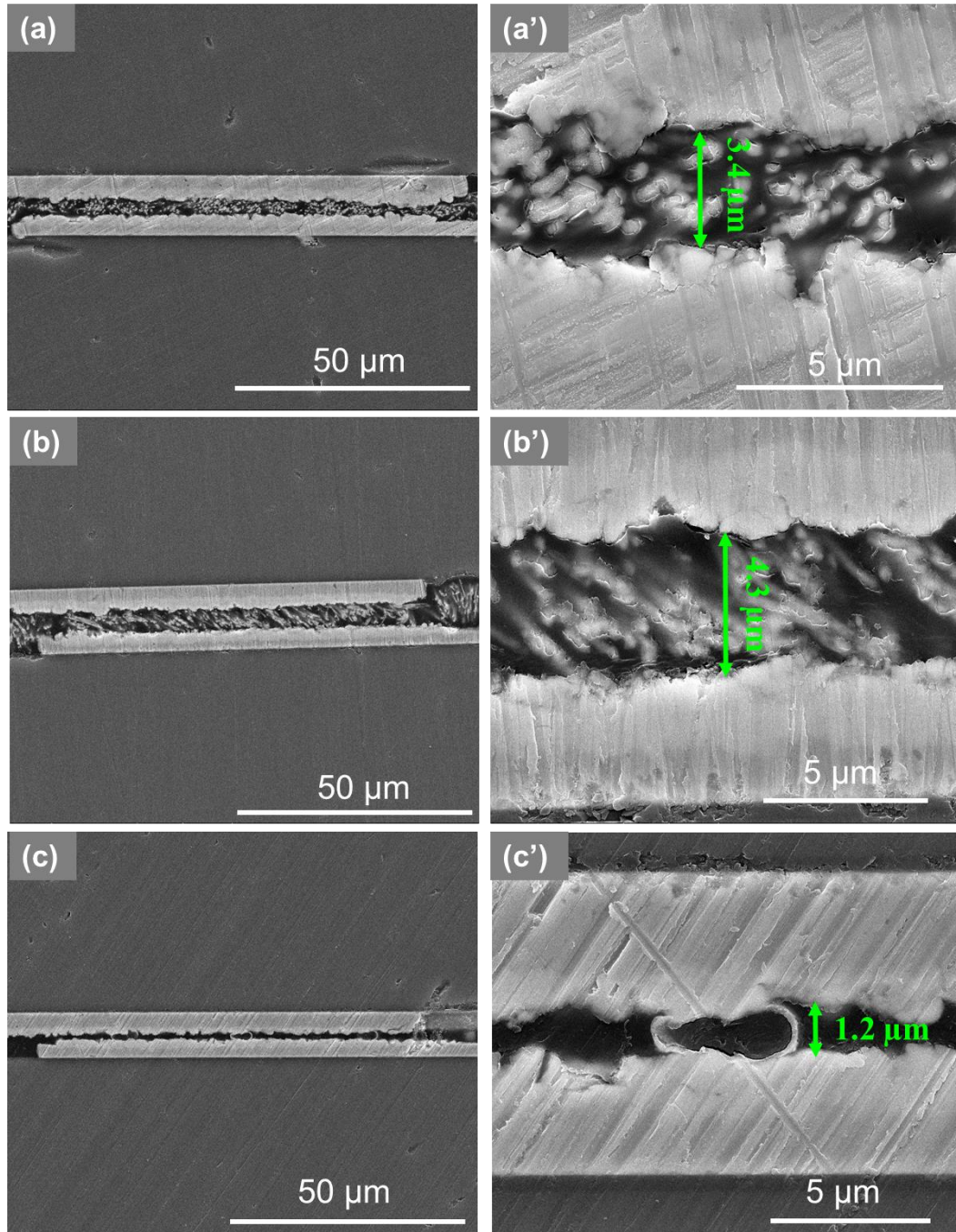


Figure 5.6 SEM images of the bonding interfaces of (a) the as bonded NW-ACF interconnect, (b) the NW-ACF interconnect after 1100 T/S cycles and (c) the particle-ACF interconnect after 1100 T/S cycles. The magnified images (a') to (c') show the morphology of the nanowires or conductive particle in the interconnects with measurement of bond lines thickness.

A die shear test was performed with the NW-ACF bonded samples and the particle-ACF bonded samples after 1100 thermal shock cycles. Typical die shear strength of the NW-ACF bonded sample was 6.6 MPa, which is slightly higher than the value of the as-bonded samples of 5.3 MPa. The effect of thermal shock may improve or at least not degrade the shear strength of the NW-ACF interconnects. The same test was conducted with the particle-ACF bonded sample after thermal shock test and the shear strength is 28.4 MPa. Compared to the NW-ACF, much higher shear strength can be achieved by the particle-ACF, which may correlate with the better reliability of the particle-ACF.

The fractural surfaces of the NW-ACF before and after the test are compared in Fig. 5.7 (a) and (b). Blisters were found with the NW-ACF film in the inter-pad/die surface area after the test, which is marked in Fig. 5.7 (b). This can be attributed to the penetration of the air or moisture through the polymer into the bonding area through the air gaps in the bonding area. Due to the small film thickness of current ACF, the whole bonding area especially Si area was not sufficiently sealed. The formation of blisters will degrade both the electrical and mechanical performance of the interconnects by inducing the delamination failure of the film to the bonding surface. To avoid such defect, both the polymer material and the film thickness should be improved in the further development. Nevertheless, the fracture morphology of the film under SEM (a') and (b') before and after reliability test shows no substantial difference. Comparatively, the fractured surface of the particle-ACF is shown in Fig. 5.7 (c) and (c'). During shear test, only one edge of the die was sheared and the bond pads were peeled off, as shown in Fig. 5.7 (c). In the ACF adhering area to the die surface, the fracture occurred mainly due to the fracture within the polymer. The fracture mode was proved to be cohesive instead of adhesive failure as found with the NW-ACF, as the fragments of the fractured polymer were also observed to be attached on both sides of the bonding surface. For particle-ACF, the interfacial adhesion strength is higher than the cohesive strength of the polymer epoxy, which demonstrates a superior mechanical property of the epoxy based ACF as compared to the thermoplastic based NW-ACF.

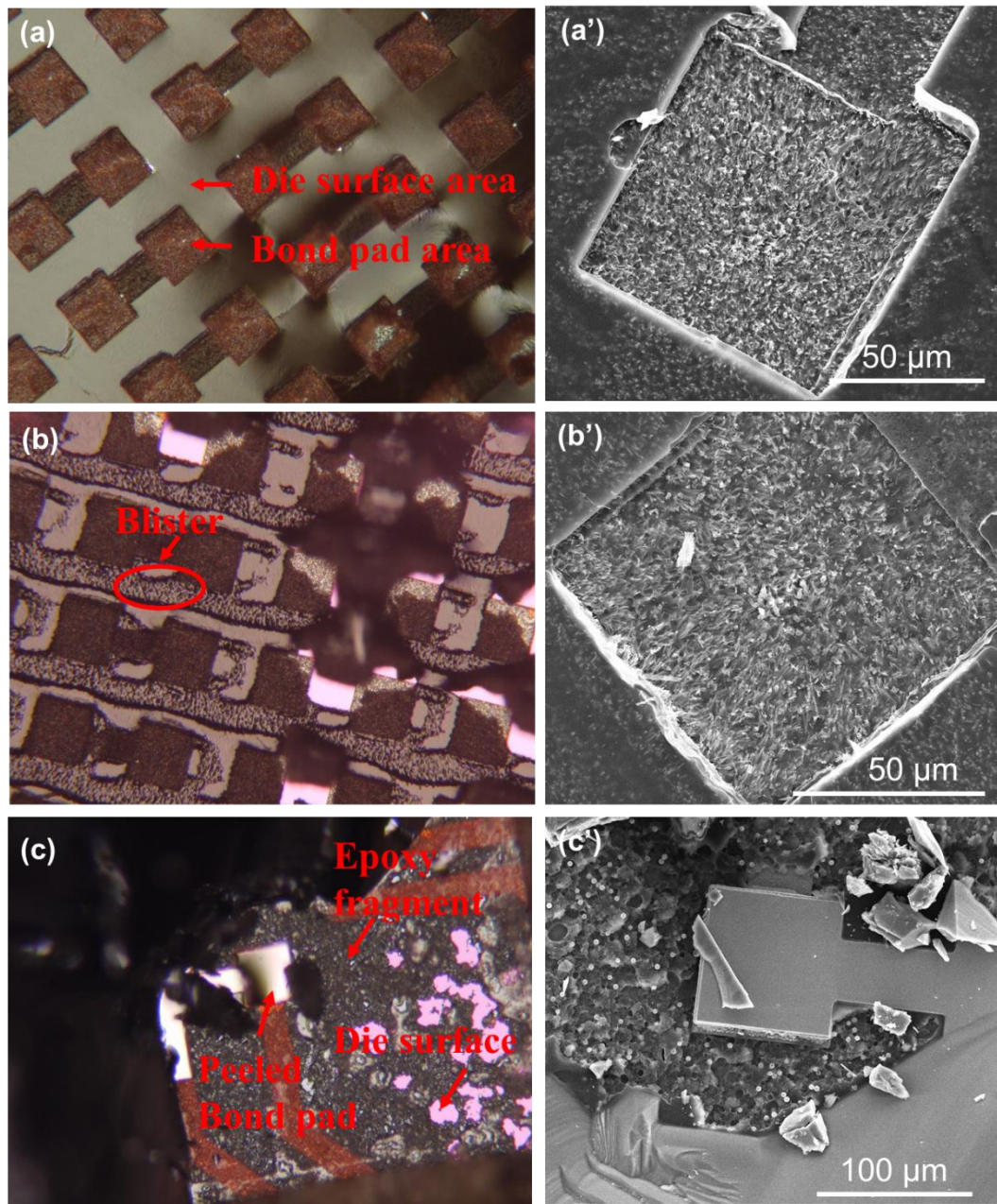


Figure 5.7 Optical images ($100\times$ magnification) of the fractured die surfaces of (a) the as-bonded NW-ACF sample with Cu-In pads, (b) the NW-ACF bonded Cu-In pads sample after 1100 thermal shock cycles and (c) the particle-ACF bonded Cu-In pads sample after 1100 thermal shock cycles. The SEM images (a') to (c') show the fracture morphology of the polymer in a single bond pad area of the corresponding dies.

High Temperature and High Humidity Test Samples

Cross-sectional samples were prepared for the electrically failed samples after high temperature and humidity test. Fig. 5.8 (a) and (b) show the bonding interfaces of the samples after 200 and 800 HT/HH hours, respectively. These showed similar characteristics to the

thermal shock samples, expansion of bondline thickness $\sim 1\ \mu\text{m}$ occurred after 800 HT/HH hours. The expansion of the interconnects can be attributed to the moisture diffusion through PC where the PC volume increased after water uptake. The ratio of the polymer volume increase (%) to the maximum water uptake volume (%) at a temperature is defined as coefficient of moisture expansion (CME). For a polymer, CME increases with the increased temperature [105]. At $85\ ^\circ\text{C}$, PC swells due to high moisture uptake and induces high hygroscopic stress due to the mismatch of CME (CME of PC is much higher than that of Si die and metal pads). Such stresses are mainly accumulated in the bonding interface area where cracks are prone to initiate and cause the interconnects to fail [230]. For the electrically failed sample after 200 testing hours, cracks of the polymer in the interfacial area near the pad surface was found. For the sample after 800 testing hours, cavities were found in the thickness direction of the polymer. Both the cracks and cavities indicates the degradation of PC in the interconnects. Two degradation mechanisms of PC under hydrothermal aging have been reported [231]: the absorption of the water in the free volume and the structural damage such as micro-cavities and cracks due to inter-chain bond breakage as well as water reaction with functional groups of PC such as hydroxyl (OH) groups. The former leads to the expansion of the polymer and the latter cause brittleness and rigidity of the PC. Due to the moisture induced swelling, the interface was under a high tensile load to pull the pads apart. Meanwhile, the mechanical strength of the polymer to hold the pads together was weakened due to the degradation of PC. Both factors lead to the open failures in the NW-ACF interconnects. Comparatively, the bonding interfaces of the particle-ACF interconnect are shown in Fig. 5.8 (c) and (c'), where a small bondline thickness was maintained even after HT/HH test and no cracks or cavities as those in the NW-ACF interconnects were observed.

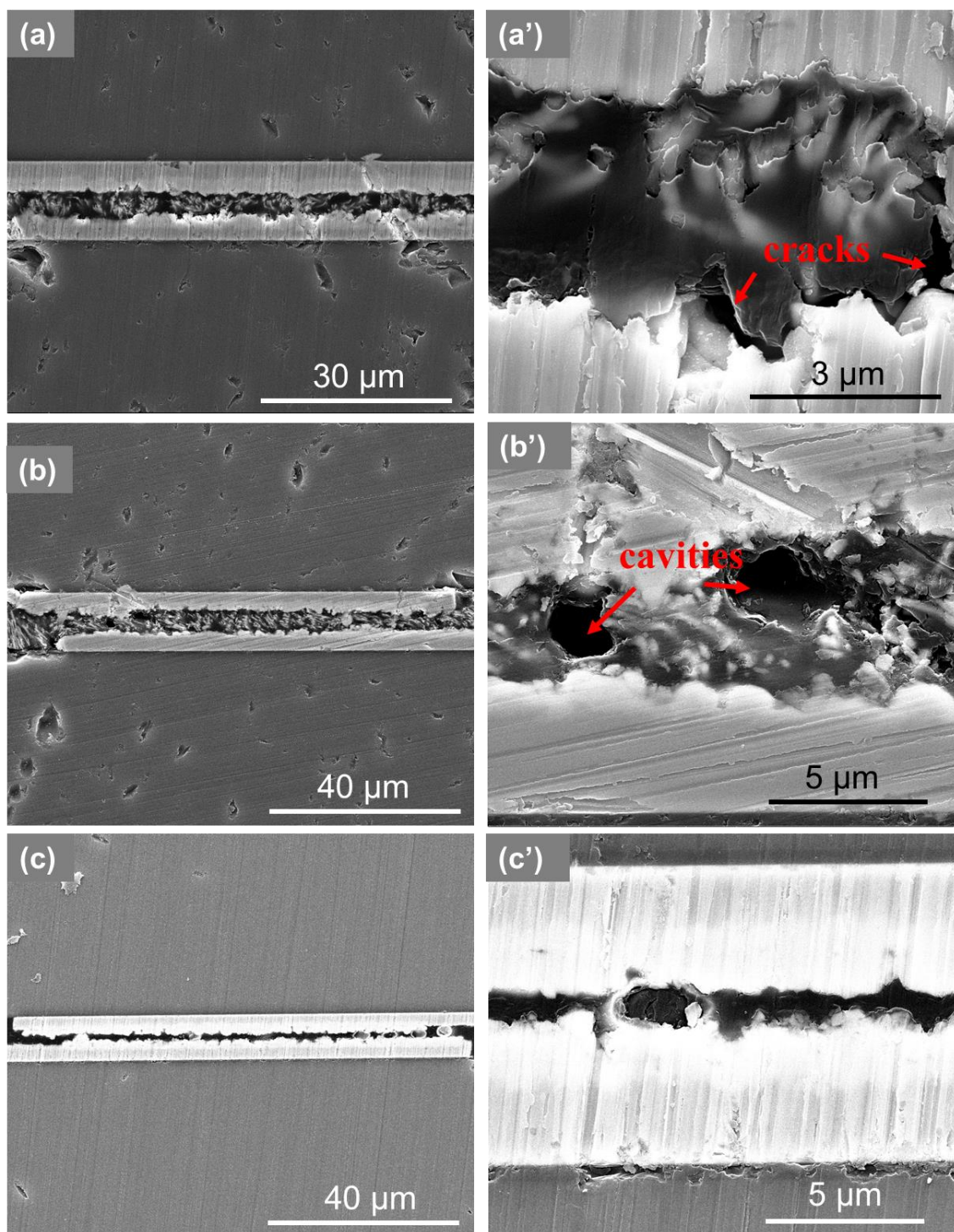


Figure 5.8 SEM images of the bonding interfaces of (a) the electrically failed NW-ACF interconnect after 200 HT/HH hours, (b) the electrically failed NW-ACF interconnect after 800 HT/HH hours and (c) the particle-ACF interconnect after 800 HT/HH hours. The magnified images (a') to (c') show the morphology change of the polymer in the respective ACF after testing, where cracks and cavities were found with the NW-ACF interconnects.

Die shear test was performed with the electrically failed NW-ACF bonded sample after 100 HT/HH hours and the die shear strength is 3.7 MPa. Compared to the as-bonded sample, the value is 30% decreased. The fractured die image of hydrothermal aging sample is shown in Fig. 5.9 (a). Blisters were again found with the NW-ACF film in the inter-pad area. Meanwhile, a noticeable colour change and oxidation of the film especially in the inter-pads area were found as shown in image (b). Two types of Cu oxides were observed in SEM images (c) and (d) and confirmed by EDS analysis as Cu- or Cu/In- formed oxides or hydroxides compounds. The oxides were grown on top of the NWs and form the grainy or cubic-like structure attached on the film surface with a typical diameter of several hundreds of nm. Such oxides were not observed in the fractured surface of as-bonded or thermal shock test samples. Cu is known to have lower normal potential of 0.34 V, when compared to that of water of 0.40 V and galvanic corrosion can happen if the potential of a metal which acts as anode is lower than the potential of the cathode reaction, $2\text{H}_2\text{O} + 4\text{e}^- + \text{O}_2 = 4\text{OH}^-$ [108]. It was reported in the same study that the galvanic corrosion at the interface between Ni flake and Ag metal wire is the main cause of the contact resistance shift [108]. In this study, this galvanic corrosion can probably occur between Cu NWs and the absorbed water in the interfacial area. With the oxidation or corrosion of Cu NWs in the interconnects, the contact resistance increased abruptly.

Comparatively, the particle-ACF bonded sample after 800 hours of HT/HH test had a shear strength of 25.4 MPa. Compared to its thermal shock counterpart, the shear strength was also decreased. The fractural surfaces of the particle-ACF after HT/HH test are shown in Fig. 5.9 (e) and (f). It was found that a higher ratio of adhesion failures occurred in the bonding area, as compared to the T/S samples. The decreased shear strength and higher ratio of adhesive failures indicate a certain degree of the mechanical degradation of the particle-ACF under hydrothermal environment as well.

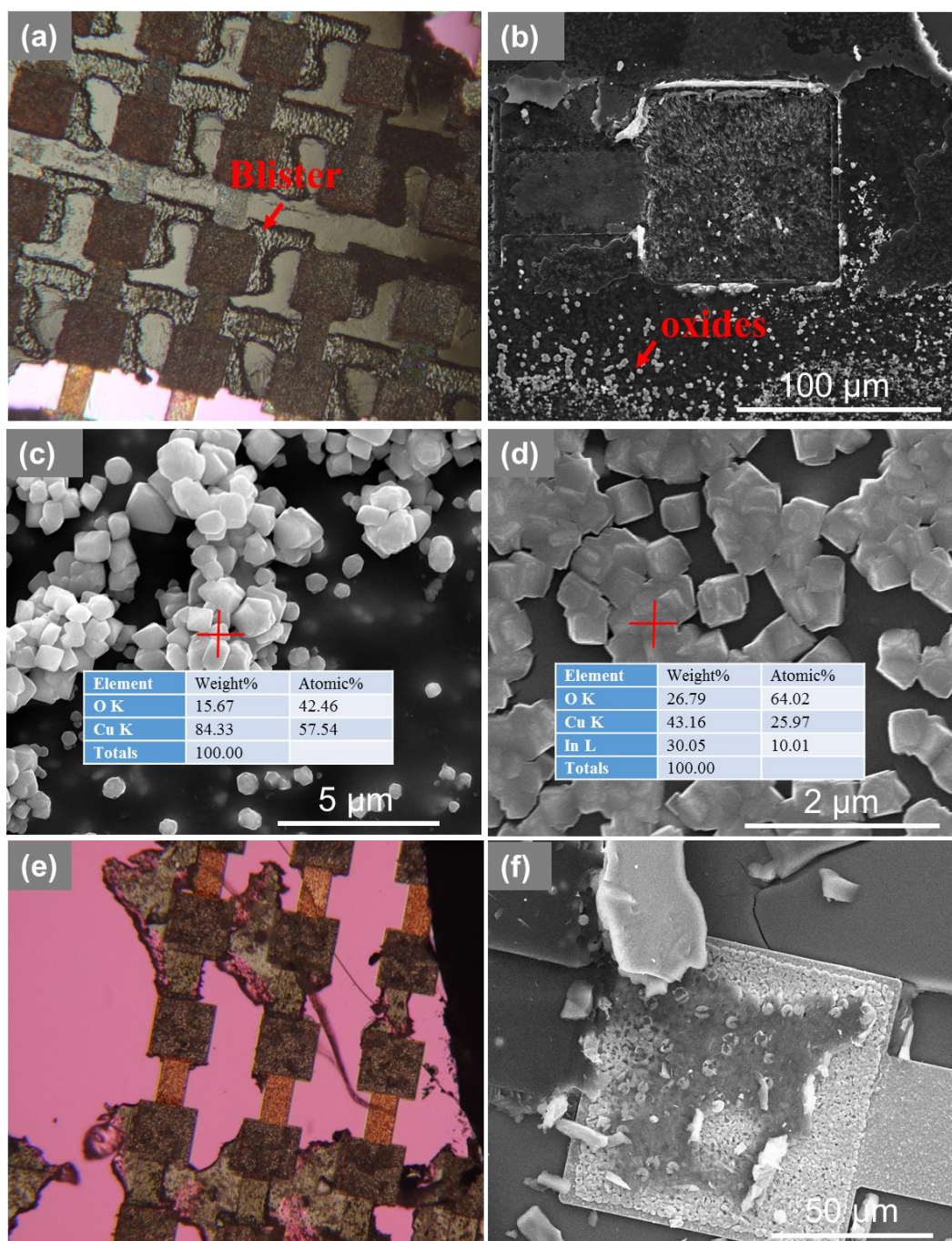


Figure 5.9 Optical image (100 \times magnification) of the fractural surfaces of (a) the NW-ACF bonded sample after 100 hours of hydrothermal aging and the corresponding SEM images showing (b) the magnified bond pad areas, (c) the Cu oxides or hydroxides found in the fractured surface and verified by EDS and (d) the Cu-In formed oxides or hydroxides found in the fractured surface and verified by EDS. A comparative analysis for the particle-ACF bonded sample after 800 hours of hydrothermal aging, (e) optical image (100 \times magnification) of the fractured die surface and (f) SEM image of a fractured bond pad area.

5.3.4 Reliability Assessments of the NW-ACF Bonded Au Bumpless Pads

5.3.4.1 Electrical Performance

Thermal Shock Test

To investigate the reliability behaviour of NW-ACF interconnects with Au pads as described in Chapter 4.3, the T/S tests were conducted with each of the two NW-ACF bonded Au pads samples with 80 and 40 μm pad sizes. The study aims to understand the effects of non-solder bonded surface and low pad height of Au pads as compared to Cu-In pads on the interconnect reliability. Fig. 5.10 shows the T/S test results for NW-ACF interconnect with Au pads, where all samples showed early stage failures regardless of the pad sizes. Two samples had daisy-chain opens after 100 cycles and the other two failed in the same way after 200 cycles. The samples failed in the first 100 cycles were prepared for failure analysis. One sample failed after 200 cycles with $> 50\%$ daisy opens was no longer subjected for further testing, while the other sample with $< 50\%$ failures was continued for testing till the cycle end, when $> 50\%$ daisy chain opens occurred. Comparatively, the particle-ACF bonded samples with Au pads show no failure and good electrical stability in such test.

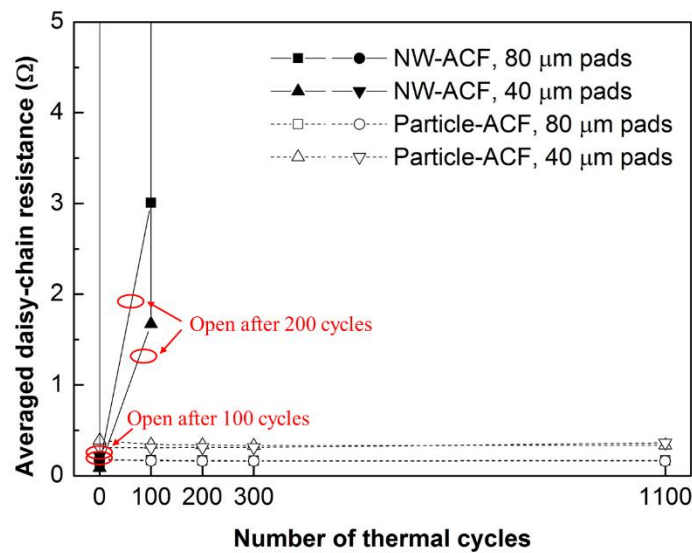


Figure 5.10 Early stage electrical failure of the NW-ACF bonded Au daisy-chain pads under thermal shock cycles, while the particle-ACF shows no failure and stable resistance till the cycle end.

High Temperature and High Humidity Test

Two NW-ACF bonded Au pads samples with 80 μm and 40 μm pad size were also subjected to HT/HH testing. The early stage failures were found with all samples regardless of the pad sizes, as shown in Fig. 5.11. Two samples show daisy-chain opens after 100 cycles and the other two failed after 200 cycles. The samples that failed in the first 100 cycles were prepared for failure analysis. The other two samples were subjected for further testing till > 50% chain failures were found, which occurred after 300 hours and 800 hours, respectively. Comparatively, the particle-ACF bonded samples showed no failure and good electrical stability till the end of the test. The causes of the high failure rate of NW-ACF bonded Au samples in reliability test were understood by failure analysis in the following sections.

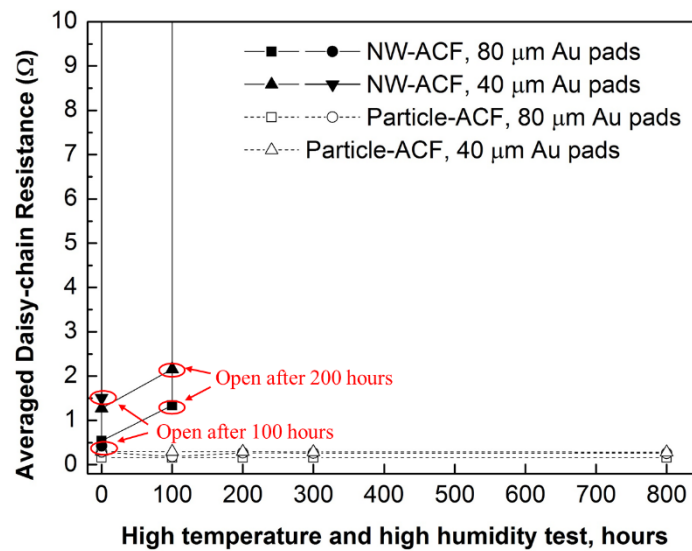


Figure 5.11 Early stage electrical failure of the NW-ACF bonded Au daisy-chain pads under high temperature and high humidity test, while the particle-ACF shows no failure and stable resistance till the duration end.

5.3.4.2 Bonding Interface and Fractural Surface Analysis

Thermal Shock Test Samples

The failure mechanism of the NW-ACF bonded Au pads after thermal shock test was examined by preparing cross-sectional samples. Fig. 5.12 compares the bonding interfaces of the NW-ACF interconnects in (a) as-bonded, (b) after 200 T/S cycles and (c) after 1100 T/S cycles. There was no obvious delamination or crack growth in the interfacial area with the

sample after T/S test. However, the continued expansion (from 6.2 μm to 7.1 μm) of the bondline thickness with the number of the cycles was found. Compared to the NW-ACF interconnect bonded with the thick Cu-In pads, the interconnect with thin Au pads has a larger bondline thickness and lightly bent nanowires, as illustrated in Fig. 5.13. For such interconnects, the NWs have less tolerance to bondline expansion before they completely lose contact with the bond pads. With the same level of bondline expansion ($\sim 1 \mu\text{m}$), the interconnects can be more severely impaired due to open failures. Moreover, due to lack of In solder layer to make penetration contact mode with NWs, the contact force between the Au surface and the NWs is weaker and the NWs can lose contact easily. To improve the reliability performance with non-solder bonding surface, one possible solution is to design the thick bond pads with which a small bondline thickness and the highly bent NWs can be created.

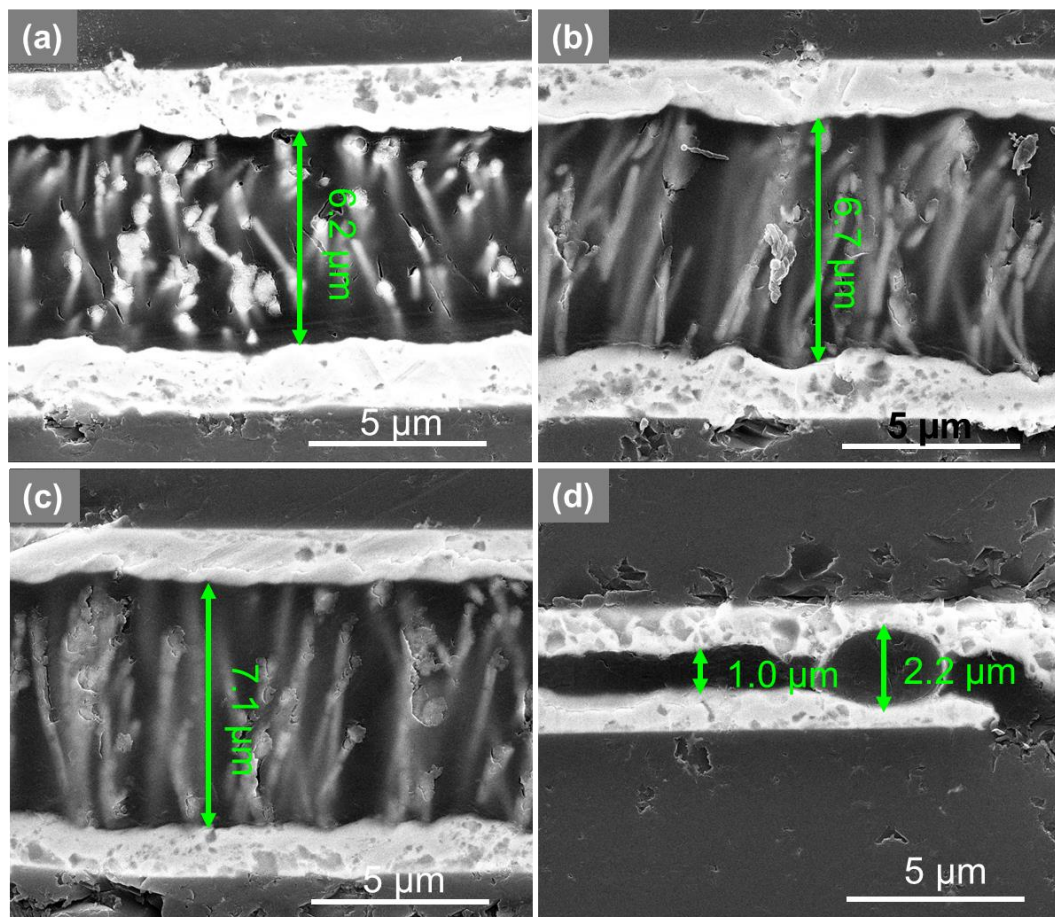


Figure 5.12 Bondline interface analysis of (a) the as-bonded NW-ACF interconnect, (b) the electrically failed NW-ACF interconnect after 200 T/S cycles, (c) the electrically failed NW-ACF interconnect after 1100 T/S cycles and (d) the particle-ACF interconnect after 1100 T/S cycles.

On the other hand, the interconnect of the particle-ACF with Au pads after 1100 T/S cycles is shown in Fig. 5.12 (d). It was found that even with a thin Au pad, the small bondline thickness of $\sim 1.0 \mu\text{m}$ was formed and maintained before and after T/S test. The formation of small bondline thickness during bonding can be attributed to the very low viscosity of the epoxy polymer during curing to be deformed under sufficiently high bonding pressure. With the small bondline thickness, the conductive particles were highly deformed with the compression thickness of $2.2 \mu\text{m}$. The highly deformed particles are more compliant to the thermal induced expansion as compared to less deformed nanowires and therefore maintained a stable electrical resistance in the testing cycles.

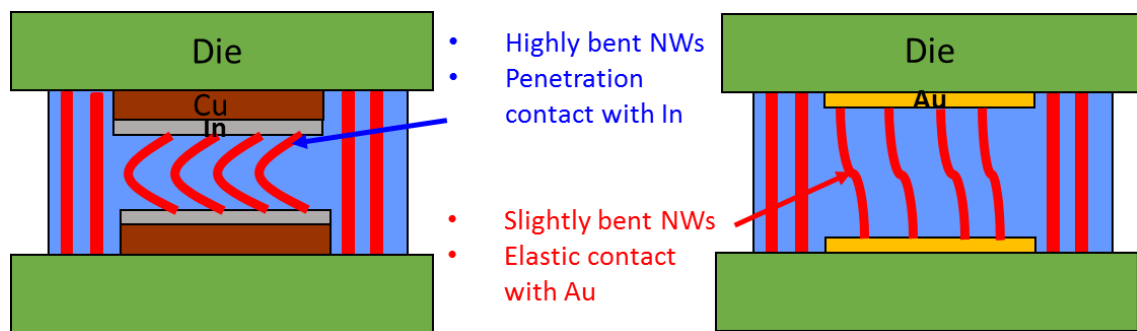


Figure 5.13 Schematics showing the different bonding mechanisms of the NW-ACF bonding with Cu-In pads and Au pads.

Die shear test was conducted with the NW-ACF bonded test module 2 with $40 \mu\text{m}$ Au pads failed after 100 T/S cycles for fractural surface analysis. The die shear strength was $\sim 7.1 \text{ MPa}$ and was comparable to the value of the as-bonded samples of $\sim 6.7 \text{ MPa}$, which indicates no degradation of the shear strength after thermal shock test. Compared to the Cu-In pads bonded samples ($\sim 5.9 \text{ MPa}$), the Au pads bonded sample had a higher shear strength, which can be attributed to the low topography of the test die. Fig. 5.14 (a) shows the fractural surface of the as-bonded NW-ACF sample with Au pads. The fracture mode was the adhesive failure in the interface area between the NW-ACF and the die surface. In the corresponding SEM image of Fig. 5.14 (a'), the fractural surface of the NW-ACF in the pad area shows a much smoother surface, as compared to that of the Cu-In pads in Fig. 5.2 (b'). The smooth fracture surface may indicate the lower adhesion strength formed between the NW-ACF and the Au pad surface, which cause the nanowires to lose contact easily. Fig. 5.14 (b) shows the fractural surface of the sample after 100 T/S cycles. Blisters were again found in the fractured NW-ACF surface in the inter-pad area, due to the penetration of the moisture into the

polymer. A crack of the film was also observed in the fractured surface, which is possibly due to the die shearing process. The blister area was also observed in the SEM image of Fig. 5.14 (b') as the uneven surface of the film.

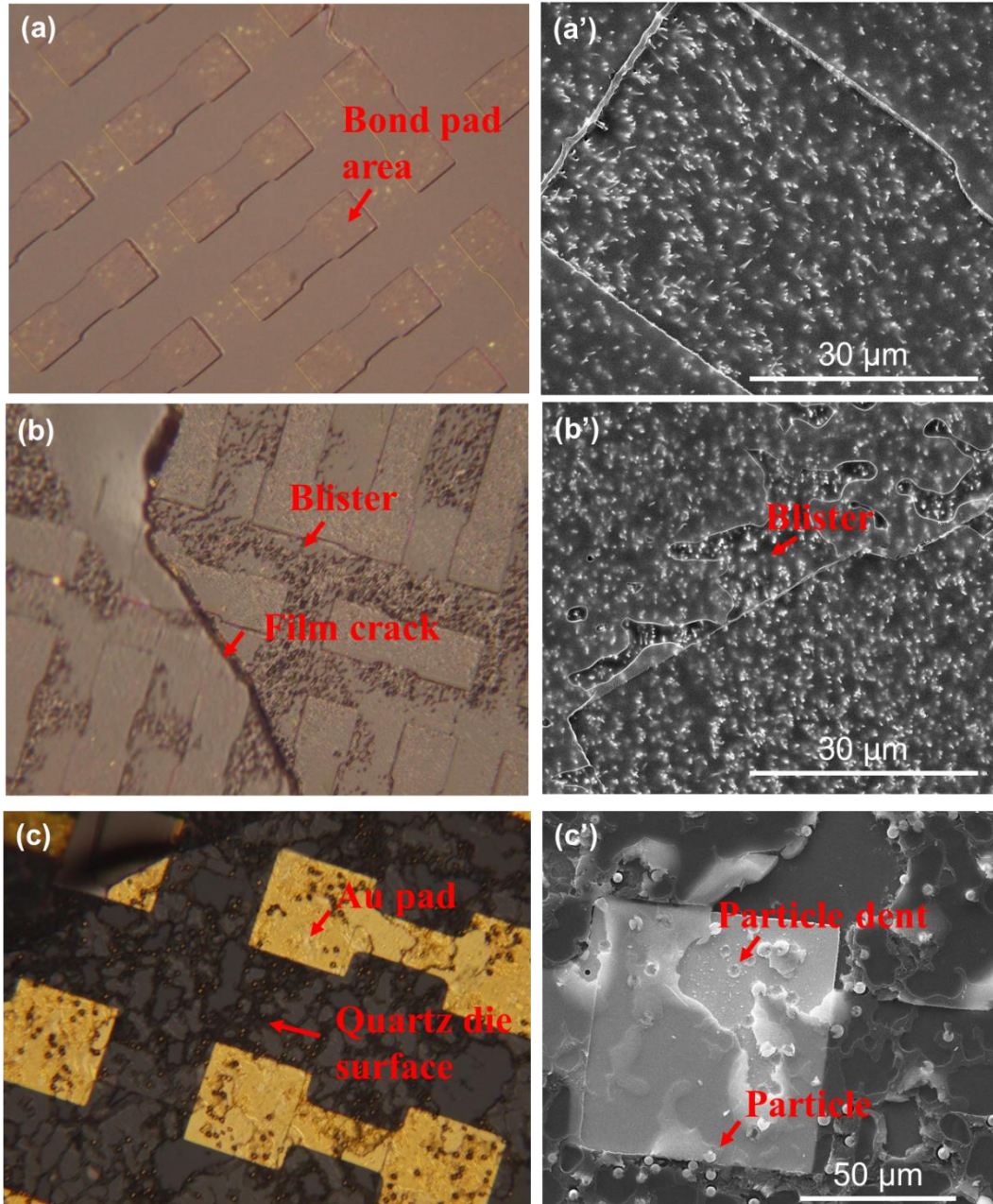


Figure 5.14 Optical images (100 \times magnification) of the fractural surfaces of (a) the as-bonded NW-ACF sample with Au pads, (b) the electrically failed NW-ACF bonded Au pads sample after 100 thermal shock cycles and (c) the particle-ACF bonded Au pads sample after 1100 thermal shock cycles. The SEM images (a') to (c') show the fracture morphology of the polymer in a single bond pad area of the corresponding die.

A comparative study of the die shear test was conducted for the particle-ACF (test module 1) after 1100 T/S cycles. The die shear strength was above the maximum shear force of 20 kgf (> 32 MPa), which was even higher than the particle-ACF bonded samples with Cu-In pads. To obtain a fracture surface of such sample, the die was sheared for several times until a small piece was detached as shown in Fig. 5.14 (c). It was found that the fracture occurred mostly due to the breakage of the polymer with the polymer fragments found on both fractural surfaces of the die. In the respective SEM image of Fig. 5.14 (c'), the morphology of the fractured polymer and the conductive particles in the polymer can be observed. The dents formed by the particles compressed into the Au pad were observed, which indicate the good physical contacts formed between the particles and the Au pads.

High Temperature and Humidity Test Samples

Cross-sectional samples were prepared for the electrically failed NW-ACF interconnects after 100 and 800 HT/HH hours, as shown in Fig. 5.15 (a) and (b).

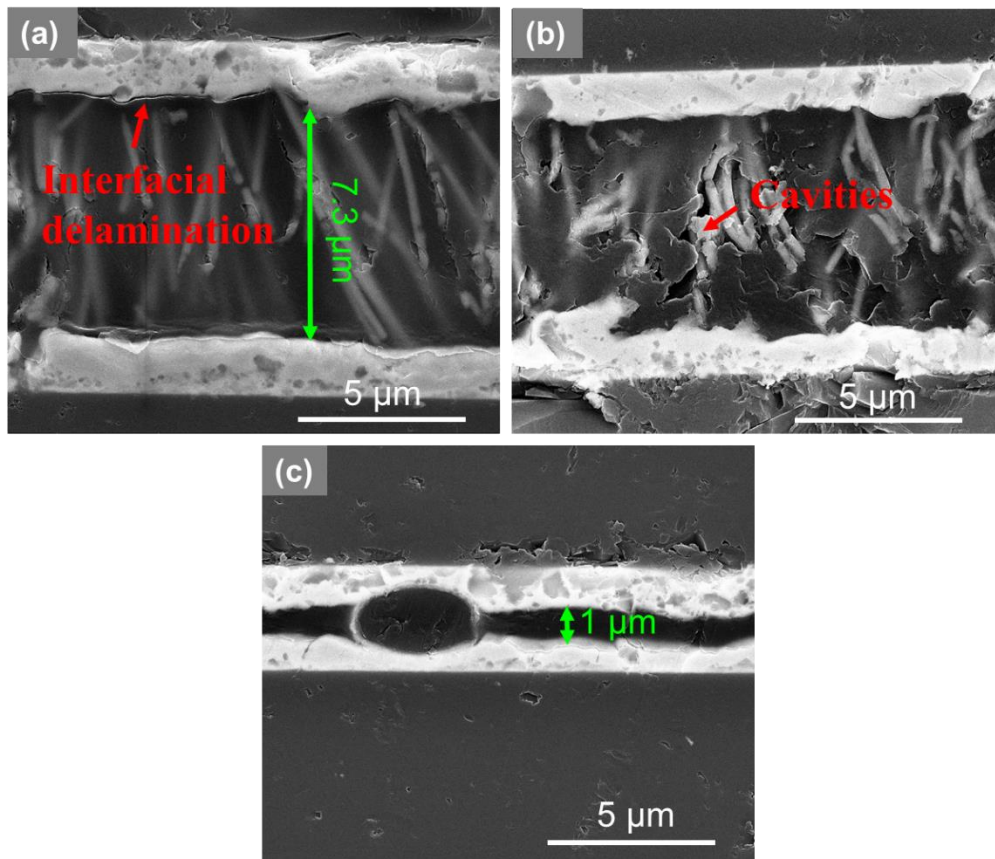


Figure 5.15 SEM images of the bonding interfaces of (a) the electrically failed NW-ACF interconnect with Au pads after 100 HT/HH hours, (b) the electrically failed NW-ACF interconnect with Au pads after 800 HT/HH hours and (c) the particle-ACF interconnect with Au pads after 800 HT/HH hours.

Compared to the as-bonded interconnects in Fig. 5.12 (a), it was found that the bondline thickness expanded already 1 μm for the sample after 100 HH/HT hours. Moreover, the delamination was found in the interfacial area between the polymer and the pad surface. Both factors cause the nanowires to lose contact with Au pads at a very early stage. One sample that electrically failed after 200 HT/HH hours was subjected for further duration till 800 hours, until a higher percentage of daisy-chain opens occurred. The cross-sectional image is shown in Fig. 5.15 (b). Compared to the previous sample, the expansion of the bondline thickness in this sample was less severe. However, the cavities were found in the polycarbonate matrix, which demonstrates the degradation of the polymer after long exposure time in the humid environment. Comparatively, the particle-ACF interconnects with Au pads after 800 HT/HH hours is shown in Fig. 5.15 (c). The small bondline thickness of $\sim 1 \mu\text{m}$ was maintained after testing and no interfacial delamination and cavities in the polymer were observed in the interconnect.

Die shear test was performed with the NW-ACF bonded sample after 300 HT/HH hours. The die shear strength was 3.1 MPa, which was $\sim 50\%$ decrease as compared to that of the as-bonded sample (~ 6.7 MPa). The optical image of the fractured surface is shown in Fig. 5.16 (a). The blister was not found with this sample in the inter-pad area. However, the cavities of the polymer due to degradation were found in the fractured bond pad area, as shown in the SEM image of Fig. 5.16 (b). Meanwhile, Cu oxides or hydroxides were also found to grow on top of the individual nanowires on the film surface, as shown in Fig. 5.16 (c). Due to the moisture penetration in the film, the corrosion of the metal occurred in the interfacial area. Such corrosion was even severe in the edge area of the dies, as shown in Fig. 5.16 (d). The heavy oxidation of the nanowires and the extensive degradation of polymer were seen. It can be inferred that the water penetration firstly occurred in this area which is closer to the outer environment.

Comparatively, the particle-ACF bonded sample after 800 hours of HT/HH test was sheared under the same condition and the shear strength is 31.1 MPa, which is a bit lower than that of the thermal shock sample (> 34 MPa). The fractured die surface under optical image and a pad area under SEM image are shown in Fig. 5.16 (e) and (f), respectively. It was found that an increased ratio of adhesive failures occurred in the fractured area, as compared to the sample after thermal shock test in Fig. 5.14 (c). The mechanical behaviours of such ACF after hydrothermal aging demonstrate a certain level of mechanical degradation of the polymer as well.

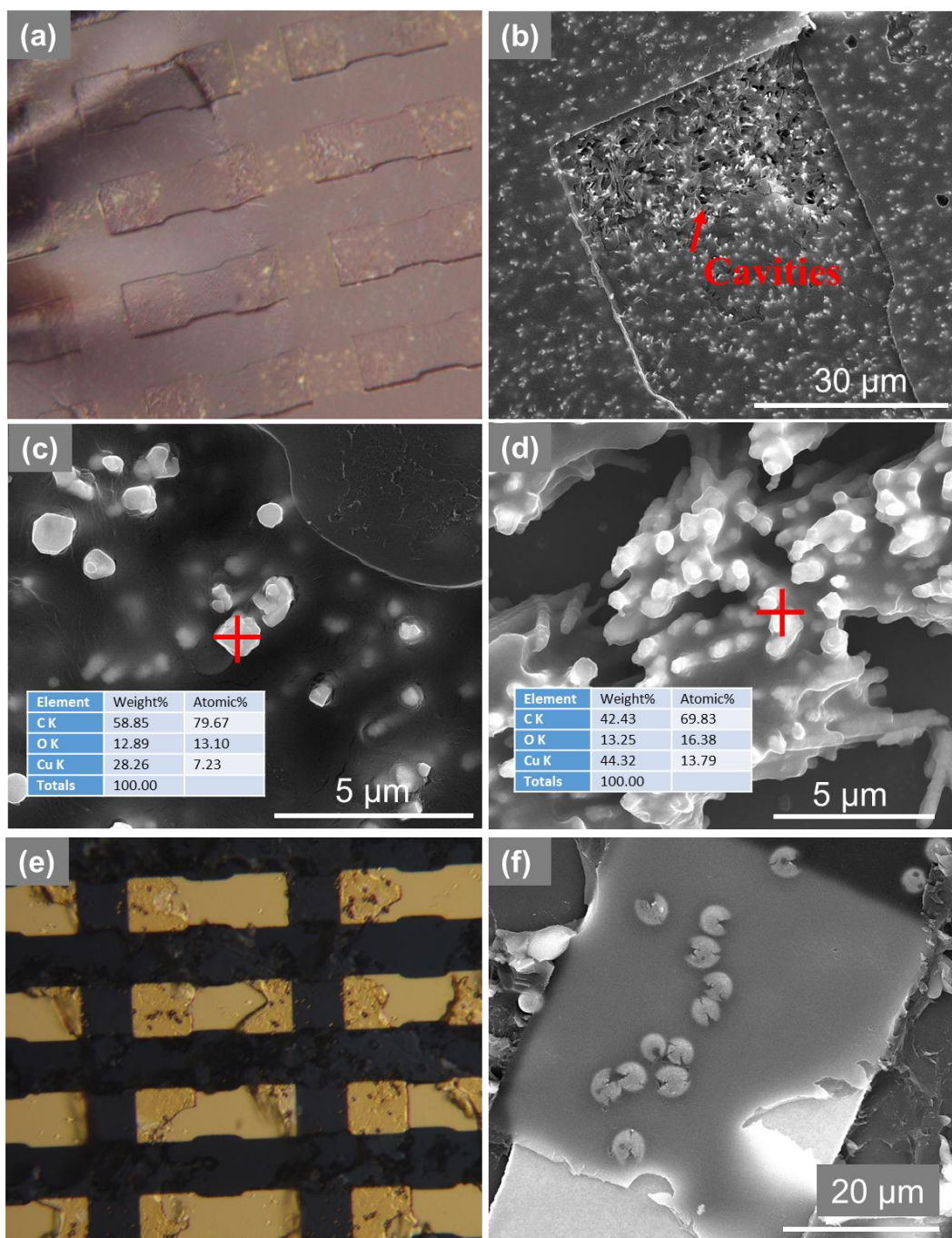


Figure 5.16 Optical image (100× magnification) of the fractured surfaces of (a) the NW-ACF bonded Au pads sample after 300 HT/HH hours and the corresponding SEM images showing (b) the magnified bond pad areas, (c) the Cu oxides or hydroxides found in the fractured surface and verified by EDS and (d) the heavy oxidation of the nanowires and polymer recession in the edge of the die. A comparative analysis for the particle-ACF bonded sample after 800 hours of hydrothermal aging, (e) optical image (100× magnification) of the fractured die surface and (f) SEM image of a fractured bond pad area.

5.4 Conclusions

The mechanical strength of the NW-ACF bonded daisy-chain test modules with Cu-In pads was evaluated by die shear test. The shear strength of the as-bonded sample is 5-6 MPa and the fracture mode is adhesive failure in the interfacial area.

For the NW-ACF bonded Cu-In pads, the interconnects show $4\times$ increase of the contact resistance after 1100 thermal shock cycles. The expansion of the bondline thickness is the main cause of the resistance increment. No degradation of the adhesion strength was found due to thermal shock. For high temperature and humidity (HT/HH) test, only one out of four samples survived after 800 testing hours without daisy-chain open failures. The moisture absorption and mechanical degradation of polycarbonate mainly accounts for the failures in addition to swelling expansion. The adhesion strength was found to be $\sim 30\%$ decreased already after 100 aging hours and Cu oxidation was found in the fractured film surface.

For the NW-ACF bonded Au pads, all samples show early stage failures in both thermal shock and high temperature and humidity test. The effect of thermal expansion is more prominent due to the large initial bondline thickness of the interconnects. There is a $\sim 50\%$ decrease of the shear strength after HT/HH aging, with heavy oxidation and corrosion of the film found in the fractured surface. Severe swelling expansion and delamination of the NW-ACF are the main causes of the failures in the HT/HH test.

As a comparison, the commercial particle-based ACF bonded samples show good reliability properties in both test conditions. This is attributed to the thermosetting polymer matrix in the particle-ACF, which has a higher adhesion strength and lower moisture absorption as compared to polycarbonate matrix in the NW-ACF. The polymer system also exhibits a low viscosity to flow over the uneven bonding surface and results in a small bondline thickness. Therefore, as the further development of the NW-ACF material, the chemical and mechanical properties of the polymer have to be enhanced in terms of a better processing property (lower viscosity), higher adhesion strength and lower moisture absorption. This can be most effectively achieved by using some types of thermosetting polymer as a template material for the fabrication of the NW-ACF, which is at this moment commercially not available and thereby was beyond the remit of the present investigation. The other feasible solution is to use the adhesion promoters [47] on the bonding surface to effectively enhance the adhesion strength and the adhesion promoters are a few mono-layers thin which should be easily penetrated through by the nanowires.

Chapter 6 Conclusions and Future Work

6.1 Thesis Summary and Main Results

One of the bottlenecks of 3D heterogeneous integration is the low-temperature, high-density interconnects to be formed between stacked dies. Solder based interconnects can no longer meet the cost and performance requirements with the ever-decreasing pitch size. With the trend of I/O shrinkage in the IC industry, conventional ACFs face challenges to accommodate the reduced pad and pitch sizes. It is the aim of this study to develop a new adhesive-based interconnect material (NW-ACF) for potential low-temperature, fine-pitch 3D applications. In this thesis, the design, fabrication and characterization of the NW-ACF for die-to-die interconnects have been systematically investigated. The viability of NW-ACF bonding to both solder based (Cu-In) and non-solder based (Au) bond pads has been verified with a fine-pitch test die. Compared to conventional particle-based ACF, the NW-ACF possesses a different fabrication process, material property and inherent structural advantage (vertical high aspect ratio nanowires). It exhibits a superior electrical (finer pitch capability) and thermal (lower thermal impedance) performance. As a low process temperature and cost-effective solution, it also shows a matching high frequency performance to the solder bumps. Moreover, contact mechanism of the nanowires in the polymer to form electrical connections with a metal surface was studied using SEM, STEM, EDX and XRD analysis. The effects of bonding parameters (bonding temperature and force) on the electrical performance of the NW-ACF interconnects have also been investigated. The polymer related mechanical and reliability issues have been discussed and solutions have been suggested.

Important findings from this study are listed below:

- i. Commercially available polycarbonate nanoporous membranes with an average pore diameter of ~200 nm and different pore characteristics were used as the templates to fabricate the NW-ACF. To achieve a 100% filling ratio of the pores, the overgrowth-stripping method was developed and the achieved volume fractions of Cu nanowire in different templates are in the range of 6-25% (depending on the porosity of the template). SEM cross-sectional analysis of the film showed that the nanowires spanned the entire thickness of the template and variation of nanowire array structures based on different templates were observed.

- ii. Thermal and thermomechanical properties of the fabricated NW-ACF were studied using DSC, TGA and DMA analysis. It was found that the glass transition temperature (T_g) of the NW-ACF is 150-160 °C and the NW-ACFs exhibited a good thermal stability till 400 °C. The storage modulus of the NW-ACF below T_g is ~ 1.4 GPa and sharply decreased at a temperature of T_g , which can facilitate nanowire bonding.
- iii. The bonding experiments with the NW-ACF were carried out with the unpatterned Cu-In metallized die and the effects of bonding parameters on the interconnection resistance and shear strength were investigated. At a bonding condition of 220 °C, 60 s and 2 MPa, the minimum interconnection resistances achieved by the NW-ACFs is ~ 0.9 m Ω .mm² and the maximum shear strengths is ~ 17 MPa.
- iv. The theoretical model of the interconnection resistance was developed to find out the contributions of the interconnection resistance. It was found that the resistances associated with the contact behaviour of the nanowires and the contact resistance of individual nanowires can be the major contributing factors to the interconnection resistance. By bonding interface analysis, it was found that the actual number of the NWs that make a connection can be far less than the number of NWs in the film due to the polymer gap formed between the NWs and the bonding surfaces. The contact mechanism of single nanowires to make effective contact to the bonding surface was understood by the STEM-EDS mapping and XRD analysis. It was found that the Cu-In diffusion occurred in the nanowire contact and the alloy of Cu₁₁In₉ was formed. The contact resistance of three different types of contact modes was discussed and concluded that the penetration contact mode can result in the lowest contact resistance.
- v. A stacked test chip module with daisy-chain, 4-point and insulation test structures was designed to explore the fine-pitch capability of the NW-ACF interconnects. The four pad/pitch variations were designed with the minimum pad/pitch size of 10/30 μ m. A test wafer containing different types of test chips and Cu-In bond pads was fabricated with 4-mask lithography process. Three NW-ACFs based on different templates were evaluated with the fine-pitch test chips to screen out the template related open/short failure. The NW-ACF A was confirmed electrically short due to high nanowire density (~ 25%) and the NW-ACF B was found electrically open due to the small nanowire density (~ 6%) and the unevenness of the template surface. The NW-ACF C with a Cu volume ratio of ~ 13% and a smooth template surface was verified as an electrically workable film for the fine-pitch interconnection.

- vi. The fine-pitch electrical performance of the NW-ACF interconnects were evaluated in terms of daisy-chain resistance and insulation properties (leakage current). The effect of bonding temperature was studied in terms of bonding yield and interconnection resistance and the optimized bonding temperature is 220 °C. By bonding interface analysis, a reduced bondline thickness was found at a bonding temperature ≥ 200 °C. It is concluded that at this temperature, the external force can be higher than both the axial modulus of the nanowires and the modulus of the polymer and the deformation of the polymer and the nanowires can occur. On the other hand, the effects of bond pad size and bonding force were studied in terms of interconnection resistance and insulation properties. By calculating equivalent bonding pressure, it was found that the interconnection resistance for each test module at a similar bonding pressure level will not linearly scale with the bond pad area. The best electrical results achieved by the NW-ACF interconnects are 0.03-0.04 Ω per interconnect for all pad sizes at an optimized bonding temperature and force. At a certain bonding force/pressure (8 MPa), the nanowires were found to be greatly bent in the horizontal direction and resulted in a low contact resistance. Meanwhile, the NW-ACF interconnects at all pad sizes show a good insulation property with a very small leakage ($< 10^{-9}$ A) current at an applied voltage till 20 V. The leakage current was caused by the non-parallel pore structures of the template, which should be improved in the future development of the template material.
- vii. The viability of bonding the NW-ACF to the Au bumpless dies was verified, with a resultant interconnection resistance ~ 90 m Ω per interconnect (40 μ m pad size). It was found that the contact mode of the nanowires with the bumpless pads was point contacts of nanowire ends to the Au surfaces instead of bending of nanowires as occurred during bonding with the Cu-In bond pads. A comparative study was carried out with a commercially particle-based ACF. The results show that NW-ACF has a better electrical performance in terms of finer pitch capability, lower interconnection resistance and smaller bonding force.
- viii. High frequency performance of the NW-ACF interconnects was evaluated based on the measurement of S-parameters of GSG test structure on Si and quartz substrates. The lossy characteristics of the Si substrate were confirmed by calculating and verifying the additional transverse elements R_{leak} and C_{ox} . With quartz substrate, the S-parameters of the transmission line with the NW-ACF interconnects were obtained and the RLCG parameters were extracted. The results show good RF properties of the

line with the NW-ACF interconnects, as compared to the results of through line and the line with the solder bumps.

- ix. Thermal performance of the NW-ACF interconnects was evaluated by thermal impedance measurement. Compared to that of the particle-based ACF, the NW-ACF shows ~ 18% lower thermal impedance. The better thermal impedance can be attributed to a high intrinsic thermal conductivity and low contact impedances of the Cu nanowires.
- x. The mechanical strength of the NW-ACF bonded daisy-chain test modules with Cu-In pads was evaluated by die shear test. The shear strength of the as-bonded sample is 5-6 MPa and the fracture mode was confirmed as adhesive failures in the interfacial area.
- xi. The reliability tests of thermal shock test (-55 to 125 °C, 1100 cycles) and high temperature and humidity test (85 °C, 85% RH, 800 h) were carried out with the NW-ACF bonded daisy-chain test modules. The NW-ACF interconnects show an inferior reliability as compared to the particle-based ACF in terms of the electrical resistance shift and open failure rate. The main failure mechanisms for the NW-ACF interconnects are the thermal expansion of the polymer (PC) under thermal shock test and the moisture absorption of PC under high temperature and humidity test. Thereby, replacing the polymer matrix of the NW-ACF with the alternative polymer templates which have a higher adhesive strength and a lower moisture absorption property will be the key for the future material development.

6.2 Recommendations for Future Work

6.2.1 Optimization of Template Material

To further advance the NW-ACF material, new developments in polymeric materials, pore formation process and large-scale electrodeposition process have to be optimized for mass production. With regard to the development of a polymeric material as the template, it is expected to have better chemical and mechanical properties to enhance the NW-ACF bonding, including low viscosity (to facilitate bonding process), higher adhesion strength and lower moisture absorption. This can be most effectively achieved by using some types of thermosetting polymer as a template material for the fabrication of the NW-ACF, which is at this moment commercially not available. Polyimide membranes would be another option. These have been developed by several universities and institutes [142, 163]. The polyimide

membranes are reported to have a better thermal and chemical stability and high mechanical strength as compared to polycarbonate membranes and therefore could be an ideal material for interconnection purposes. With regard to the pore shape, the specific membranes with different characteristics from the commercially available membranes should be obtained without overlapping pores. The arrangement or orientation of the pore channels with respect to the polymer surface can be controlled during ion irradiation process, so that the membranes with highly parallel channels will be available. With the ideal template, the leakage current issue of the current NW-ACF can be solved. As the current template used for NW-ACF fabrication has a diameter of ~ 4 cm, a template with a larger diameter such as 10 cm (compatible with wafer level processing) can be used for further production. With the fabricated large diameter film, the wafer-level NW-ACF process can be developed to further reduce the process cost and time. Overall, a new template material such as polyimide membranes with highly parallel pores and a large diameter should be obtain by institutional collaboration work for the further development of the NW-ACF material.

6.2.2 NW-ACF with Multilayer Metallic Nanowires

Multi-segmented nanowires with solder materials has been reported to be fabricated with the template-assisted electrodeposition method [153]. Different layers of the nanowires, including gold (Au), nickel (Ni) and tin (Sn) can be prepared by sequential plating through changing the electrolytic solution. Sn can therefore be used as a solder material in the nanowires. The nanowires with two solder ends in the configuration of “solder-barrier layer-base layer-barrier layer-solder” have been demonstrated. Nanowires can be reflow soldered with each other to form the nanowire networks. The multilayer nanowire concept can be adopted for the NW-ACF fabrication by preparing the multilayer nanowires in the polymer template. The difficulties lie in that the uniform deposition across the template is critical in order to obtain the same length of each segment of the nanowires. A new method for preparation of the template surface without residue will be needed as the overgrowth-stripping may not be applied for the Sn or any solder materials. Despite the difficulties in preparing such films, the benefits of using the solder-ended multilayer nanowires will be the lower contact resistance even with the non-soldered bonding surfaces and a better mechanical and reliability performance if the metallurgical joints can be formed by majority of the nanowires. It is therefore an interesting work to be carried for the future development of the NW-ACF material.

6.2.3 Electromigration Study of the NW-ACF Interconnects

The electromigration (EM) properties of the solder joint has been reported as a major reliability concern due to the effect of current crowding and the formation and propagation of a void can occur which results in a final open joint [232]. On the other hand, Cu based interconnects are reported to have better EM resistance than the solder material [233]. The EM property of the Cu nanowires based interconnects becomes an interesting subject for studying in the future work as part of the reliability properties. Corresponding EM test structure was designed as part of the current test wafer and can be used for the evaluation of the EM properties of the NW-ACF interconnects. However, based on the reliability results as far, the adhesion property of the polymer in the NW-ACF needs to be greatly improved in the first step and the suggested solutions have been given. With a better adhesive polymer system in the NW-ACF, the EM properties of the Cu NW-ACF interconnects under high temperature and current density can be evaluated.

6.2.4 Feasibility Study with 3D TSV Chips

Under the further development of the NW-ACF material, this novel interconnection material can be expected to be applied for 3D interconnection between the TSV die/wafer. The high density interconnects accommodating the ultra-small TSV pad/pitch size can be formed once at a time for D2D, D2W and W2W bonding. Compared to the Solid-liquid-interdiffusion (SLID)-TSV bonding [8], the potential advantage of the NW-ACF bonding is the lower process temperature (220 °C, compared to ~ 300 °C for SLID bonding), lower process complexity and cost (bondability to various EBOL metals, no requirement for UBM and underfill), reduced pad/pitch stressing (≥ 3 nanowires per $1\text{ }\mu\text{m}^2$ bond pad area, ideally) and excellent thermal conductivity (all interconnection areas are filled with nanowires). By adopting new polymer systems with better adhesion, the NW-ACF/TSV bonding can be formed as 3D interconnects with the exceedingly good electrical, mechanical and thermal performances as compared to the solder based interconnects.

Bibliography

- [1] E. R. R. Tummala and E. J. Rymaszewski, "Microelectronics Packaging Handbook," ed: Cambridge Univ Press, 1997.
- [2] "Assembly and Packaging White Paper on System Level Integration [online]. Available: <http://www.itrs.net/papers.html>," ed.
- [3] R. Chanchani, "3D Integration Technologies – An Overview," in *Materials for Advanced Packaging*, D. Lu and C. P. Wong, Eds., ed: Springer US, 2009, pp. 1-50.
- [4] M. Töpper, "Wafer Level Chip Scale Packaging," in *Materials for Advanced Packaging*, D. Lu and C. P. Wong, Eds., ed: Springer US, 2009, pp. 547-600.
- [5] M. Brunnbauer, E. Furgut, G. Beer, and T. Meyer, "Embedded wafer level ball grid array (eWLB)," in *Electronics Packaging Technology Conference, 2006. EPTC '06. 8th*, 2006, pp. 1-5.
- [6] R. R. Tummala, "Packaging: past, present and future," in *Electronic Packaging Technology, 2005 6th International Conference on*, 2005, pp. 3-7.
- [7] P. Ramm, M. Wolf, A. Klumpp, R. Wieland, B. Wunderle, B. Michel, *et al.*, "Through silicon via technology—processes and reliability for wafer-level 3D system integration," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, 2008, pp. 841-846.
- [8] P. Ramm, A. Klumpp, J. Weber, N. Lietaer, M. Taklo, W. D. Raedt, *et al.*, "3D Integration technology: Status and application development," in *ESSCIRC, 2010 Proceedings of the*, 2010, pp. 9-16.
- [9] L. Jian-Qiang, "3-D Hyperintegration and Packaging Technologies for Micro-Nano Systems," *Proceedings of the IEEE*, vol. 97, pp. 18-30, 2009.
- [10] J. C. Souriau, N. Sillon, J. Brun, H. Boutry, T. Hilt, D. Henry, *et al.*, "System-on-Wafer: 2-D and 3-D Technologies for Heterogeneous Systems," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, pp. 813-824, 2011.
- [11] R. Agarwal, D. Hiner, S. Kannan, L. KiWook, K. DoHyeong, P. JongSik, *et al.*, "TSV integration on 20nm logic Si: 3D assembly and reliability results," in *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th*, 2014, pp. 590-595.
- [12] "International Technology Roadmap for Semiconductors: ASSEMBLY AND PACKAGING," ed, 2011.

- [13] Y. Developpement, "3DIC & TSV interconnects: 2012 Business update," in *Semicon Taiwan 2012*, 2012.
- [14] X. Zhang, J. K. Lin, S. Wickramanayaka, S. Zhang, R. Weerasekera, R. Dutta, *et al.*, "Heterogeneous 2.5D integration on through silicon interposer," *Applied Physics Reviews*, vol. 2, p. 021308, 2015.
- [15] "International Technology Roadmap for Semiconductors: Interconnect," ed, 2011.
- [16] P. Ramm and R. Buchner, "Method of making a three-dimensional integrated circuit," US Patent 5877034, 1999.
- [17] S. C. Johnson, "Via first, middle, last, or after?," *3D Packaging*, vol. 13, pp. 2-5, 2009.
- [18] B. Wu, A. Kumar, and S. Pamarthy, "High aspect ratio silicon etch: A review," *Journal of Applied Physics*, vol. 108, p. 051101, 2010.
- [19] D. Archard, K. Giles, A. Price, S. Burgess, and K. Buchanan, "Low temperature PECVD of dielectric films for TSV applications," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 764-768.
- [20] L. Yunlong, Y. Civale, Y. Oba, A. Cockburn, P. Jin Hee, E. Beyne, *et al.*, "Impact of barrier integrity on liner reliability in 3D through silicon vias," in *Reliability Physics Symposium (IRPS), 2013 IEEE International*, 2013, pp. 5C.5.1-5C.5.5.
- [21] R. Beica, P. Siblingrud, C. Sharbono, and M. Bernt, "Advanced Metallization for 3D Integration," in *Electronics Packaging Technology Conference, 2008. EPTC 2008. 10th*, 2008, pp. 212-218.
- [22] J. C. Chen, P. J. Tzeng, S. C. Chen, C. Y. Wu, C. C. Chen, Y. C. Hsin, *et al.*, "Impact of slurry in Cu CMP (chemical mechanical polishing) on Cu topography of Through Silicon Vias (TSVs), re-distribution layers, and Cu exposure," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1389-1394.
- [23] T. Uhrmann, T. Matthias, M. Wimplinger, J. Burggraf, D. Burgstaller, H. Wiesbauer, *et al.*, "Recent progress in thin wafer processing," in *3D Systems Integration Conference (3DIC), 2013 IEEE International*, 2013, pp. 1-8.
- [24] S. Olson, K. Hummler, and B. Sapp, "Challenges in thin wafer handling and processing," in *Advanced Semiconductor Manufacturing Conference (ASMC), 2013 24th Annual SEMI*, 2013, pp. 62-65.
- [25] A. Jourdain, T. Buisson, A. Phommahaxay, A. Redolfi, S. Thangaraju, Y. Travaly, *et al.*, "Integration of TSVs, wafer thinning and backside passivation on full 300mm CMOS wafers for 3D applications," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1122-1125.

- [26] J. Colonna, P. Coudrain, G. Garnier, P. Chausse, R. Segaud, C. Aumont, *et al.*, "Electrical and morphological assessment of via middle and backside process technology for 3D integration," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 796-802.
- [27] P. Gueguen, C. Ventosa, L. D. Cioccio, H. Moriceau, F. Grossi, M. Rivoire, *et al.*, "Physics of direct bonding: Applications to 3D heterogeneous or monolithic integration," *Microelectronic Engineering*, vol. 87, pp. 477-484, 3// 2010.
- [28] P. Enquist, G. Fountain, C. Petteway, A. Hollingsworth, and H. Grady, "Low Cost of Ownership scalable copper Direct Bond Interconnect 3D IC technology for three dimensional integrated circuit applications," in *3D System Integration, 2009. 3DIC 2009. IEEE International Conference on*, 2009, pp. 1-6.
- [29] H. Huebner, S. Penka, B. Barchmann, M. Eigner, W. Gruber, M. Nobis, *et al.*, "Microcontacts with sub-30 μm pitch for 3D chip-on-chip integration," *Microelectronic Engineering*, vol. 83, pp. 2155-2162, 2006.
- [30] M. J. Wolf, P. Ramm, A. Klumpp, and H. Reichl, "Technologies for 3D wafer level heterogeneous integration," in *Design, Test, Integration and Packaging of MEMS/MOEMS, 2008. MEMS/MOEMS 2008. Symposium on*, 2008, pp. 123-126.
- [31] R. Agarwal, Z. Wenqi, P. Limaye, R. Labie, B. Dimcic, A. Phommahaxay, *et al.*, "Cu/Sn microbumps interconnect for 3D TSV chip stacking," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 858-863.
- [32] B. Banijamali, S. Ramalingam, K. Nagarajan, and R. Chaware, "Advanced reliability study of TSV interposers and interconnects for the 28nm technology FPGA," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 285-290.
- [33] K. DeHaven and J. Dietz, "Controlled collapse chip connection (C4)-an enabling technology," in *Electronic Components and Technology Conference, 1994. Proceedings., 44th*, 1994, pp. 1-6.
- [34] H. Charles, "Advanced Wire Bonding Technology: Materials, Methods, and Testing," in *Materials for Advanced Packaging*, D. Lu and C. P. Wong, Eds., ed: Springer US, 2009, pp. 113-179.
- [35] S. Kang, P. Gruber, and D.-Y. Shih, "An overview of Pb-free, flip-chip wafer-bumping technologies," *JOM*, vol. 60, pp. 66-70, 2008/06/01 2008.
- [36] L. Johan, A. Tolvgard, J. Malmmodin, and L. Zonghe, "A reliable and environmentally friendly packaging technology-flip-chip joining using anisotropically conductive

- adhesive," *Components and Packaging Technologies, IEEE Transactions on*, vol. 22, pp. 186-190, 1999.
- [37] W. Tie, F. Tung, L. Foo, and V. Dutta, "Studies on a novel flip-chip interconnect structure. Pillar bump," in *Electronic Components and Technology Conference, 2001. Proceedings., 51st*, 2001, pp. 945-949.
- [38] M. Gerber, C. Beddingfield, S. O'Connor, Y. Min, L. MinJae, K. DaeByoung, *et al.*, "Next generation fine pitch Cu Pillar technology - Enabling next generation silicon nodes," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 612-618.
- [39] Y. Aibin, J. H. Lau, H. Soon Wee, A. Kumar, H. Wai Yin, Y. Da-Quan, *et al.*, "Study of 15um pitch solder microbumps for 3D IC integration," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 6-10.
- [40] Z. Chau-Jie, C. Chun-Chih, J. Jing-Ye, L. Su-Tsai, and C. Tao-Chih, "Assembly and reliability characterization of 3D chip stacking with 30 μ m pitch lead-free solder micro bump interconnection," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1043-1049.
- [41] Z. Chau-Jie, J. Jing-Ye, L. Yu-Min, H. Yu-Wei, K. Kuo-Shu, Y. Tsung-Fu, *et al.*, "Development of fluxless chip-on-wafer bonding process for 3DIC chip stacking with 30 μ m pitch lead-free solder micro bumps and reliability characterization," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 14-21.
- [42] C. Hsien-Chie, T. Yu-Min, L. Su-Tsai, and C. Wen-Hwa, "Interconnect Reliability Characterization of a High-Density 3-D Chip-on-Chip Interconnect Technology," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 3, pp. 2037-2047, 2013.
- [43] M. H. Roh, J. P. Jung, and W. Kim, "Electroplating Characteristics of Sn-Bi Microbumps for Low-Temperature Soldering," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, pp. 566-573, 2013.
- [44] K. Murayama, M. Aizawa, K. Hara, M. Sunohara, K. Miyairi, K. Mori, *et al.*, "Warpage control of silicon interposer for 2.5D package application," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 879-884.
- [45] P. Gueguen, L. di Cioccio, M. Rivoire, D. Scevola, M. Zussy, A. M. Charvet, *et al.*, "Copper direct bonding for 3D integration," in *Interconnect Technology Conference, 2008. IITC 2008. International*, 2008, pp. 61-63.

- [46] A. Shigetou, T. Itoh, K. Sawada, and T. Suga, "Bumpless interconnect of 6 μm pitch Cu electrodes at room temperature," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, 2008, pp. 1405-1409.
- [47] F. Niklaus, "(Invited) Adhesive Wafer Bonding, Applications and Trends," *ECS Transactions*, vol. 33, pp. 273-286, 2010.
- [48] C. Ren-Shin, K. Kuo-Shu, C. Jing-Yao, H. Yin-Po, Y. Tsung-Fu, H. Yu-Wei, *et al.*, "Achievement of low temperature chip stacking by a wafer-applied underfill material," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1858-1863.
- [49] Y. Ito, M. Murugesan, T. Fukushima, L. Kang-Wook, K. Choki, T. Tanaka, *et al.*, "Direct multichip-to-wafer 3D integration technology using flip-chip self-assembly of NCF-covered known good dies," in *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th*, 2014, pp. 1148-1153.
- [50] V. Smet, M. Kobayashi, W. Tao, P. M. Raj, and R. Tummala, "A new era in manufacturable, low-temperature and ultra-fine pitch Cu interconnections and assembly without solders," in *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th*, 2014, pp. 484-489.
- [51] L. Yingxia, L. Menglu, K. Dong Wook, G. Sam, D. Y. Parkinson, J. Blair, *et al.*, "Filler trap and solder extrusion in 3D IC thermo-compression bonded microbumps," in *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th*, 2014, pp. 609-612.
- [52] Y. Kishimoto and K. Hanamura, "Anisotropic conductive paste available for flip chip," in *Adhesive Joining and Coating Technology in Electronics Manufacturing, 1998. Proceedings of 3rd international Conference on*, 1998, pp. 137-143.
- [53] L. Li and F. Trelant, "Anisotropic conductive adhesive films for flip chip on flex packages," in *Adhesive Joining and Coating Technology in Electronics Manufacturing, 2000. Proceedings. 4th International Conference on*, 2000, pp. 129-135.
- [54] I. Watanabe, T. Fujinawa, M. Arifuku, M. Fujii, and G. Yasushi, "Recent advances of interconnection technologies using anisotropic conductive films in flat panel display applications," in *Advanced Packaging Materials: Processes, Properties and Interfaces, 2004. Proceedings. 9th International Symposium on*, 2004, pp. 11-16.
- [55] L. Johan, W. Yu, J. Morris, and H. Kristiansen, "Development of ontology for the anisotropic conductive adhesive interconnect technology in electronics applications," in

Advanced Packaging Materials: Processes, Properties and Interfaces, 2005. Proceedings. International Symposium on, 2005, pp. 193-208.

- [56] M. J. Yim and K. W. Paik, "Recent advances on anisotropic conductive adhesives (ACAs) for flat panel displays and semiconductor packaging applications," *International Journal of Adhesion and Adhesives*, vol. 26, pp. 304-313, Aug. 2006.
- [57] M. Taklo, T. Bakke, H. Tofteberg, L. Tvedt, and H. Kristiansen, "Anisotropic Conductive Adhesive for Wafer-to-Wafer Bonding," in *Proceedings of 7th Intl Conference and Exhibition on Device Packaging*, 2011.
- [58] Y. W. Chiu, Y. C. Chan, and S. M. Lui, "Study of short-circuiting between adjacent joints under electric field effects in fine pitch anisotropic conductive adhesive interconnects," *Microelectronics Reliability*, vol. 42, pp. 1945-1951, 12// 2002.
- [59] J. H. Zhang and Y. C. Chan, "Research on the contact resistance, reliability, and degradation mechanisms of anisotropically conductive film interconnection for flip-chip-on-flex applications," *Journal of Electronic Materials*, vol. 32, pp. 228-234, 2003/04/01 2003.
- [60] J. Tao, M. Hasan, J. Xu, A. Mathewson, and K. M. Razeeb, "Investigation of Process Parameters and Characterization of Nanowire Anisotropic Conductive Film for Interconnection Applications," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 4, pp. 538-547, 2014.
- [61] J. Tao, A. Mathewson, and K. M. Razeeb, "Study of fine pitch micro-interconnections formed by low temperature bonded copper nanowires based anisotropic conductive film," in *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th*, 2014, pp. 1064-1070.
- [62] J. Tao, A. Mathewson, and K. M. Razeeb, "Bumpless interconnects formed with nanowire ACF for 3D applications," in *3D Systems Integration Conference (3DIC), 2014 International*, 2014, pp. 1-6.
- [63] J. Tao, A. Mathewson, and K. M. Razeeb, "Test structure for electrical characterization of copper nanowire anisotropic conductive film (NW-ACF) for 3D stacking applications," in *Microelectronic Test Structures (ICMTS), 2014 International Conference on*, 2014, pp. 165-169.
- [64] J. Tao, A. Mathewson, and K. M. Razeeb, "Nanowire-Based Anisotropic Conductive Film: A Low Temperature, Ultra-fine Pitch Interconnect Solution," *Nanotechnology Magazine, IEEE*, vol. 9, pp. 4-11, 2015.

- [65] J. Tao, A. Mathewson, and K. M. Razeeb, "Nanowire based Anisotropic Conductive Film (NW-ACF) for Low Temperature 3D Stacking Applications," in *Micro/Nano-Electronics Packaging and Assembly, Design and Manufacturing (MiNaPAD) Forum, IMAPS France*, 2014.
- [66] L. Daniel and W. C.P., *Materials for Advanced Packaging: Electrically Conductive Adhesives (ECAs)*: Springer, 2009.
- [67] J. Liu, "ACA bonding technology for low cost electronics packaging applications-current status and remaining challenges," *Soldering & surface mount technology*, vol. 13, pp. 39-57, 2001.
- [68] Y. Li and C. Wong, "Recent advances of conductive adhesives as a lead-free alternative in electronic packaging: materials, processing, reliability and applications," *Materials Science and Engineering: R: Reports*, vol. 51, pp. 1-35, 2006.
- [69] Y. C. Lin and J. Zhong, "A review of the influencing factors on anisotropic conductive adhesives joining technology in electrical applications," *Journal of Materials Science*, vol. 43, pp. 3072-3093, 2008/05/01 2008.
- [70] M. Fujita and S. Suzuki, "Electrically conductive adhesive connecting arrays of conductors," US Patent 4113981, 1978.
- [71] T. Kawaguchi and H. Suzuki, "Anisotropically electroconductive film adhesive," US Patent 4568592, 1986.
- [72] I. Tsukagoshi, Y. Yamaguchi, A. Nakajima, Y. Mikami, K. Muto, and Y. Ikezoe, "Anisotropic-electroconductive adhesive composition, method for connecting circuits using the same, and connected circuit structure thus obtained," US Patent 4740657, 1988.
- [73] K. Sugiyama and Y. Atsumi, "Conductive bonding agent and a conductive connecting method," US Patent 5180888, 1993.
- [74] L. Daniel and W. C.P., *Materials for Advanced Packaging*: Springer, 2009.
- [75] M. A. Uddin, M. Y. Ali, and H. Chan, "Achieving optimum adhesion of conductive adhesive bonded flip-chip on flex packages," *Rev. Adv. Mater. Sci*, vol. 21, pp. 165-172, 2009.
- [76] S. Jin, T. H. Tiefel, C. Li-Ilan, and D. W. Dahringer, "Anisotropically conductive polymer films with a uniform dispersion of particles," *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on*, vol. 16, pp. 972-977, 1993.
- [77] Y. Li, K.-s. J. Moon, and C. Wong, "Nano-conductive adhesives for nano-electronics interconnection," in *Nano-Bio-Electronic, Photonic and MEMS Packaging*, ed: Springer, 2010, pp. 19-45.

- [78] S. Jin, J. J. Mottine, S. G. Seger, R. C. Sherwood, and T. H. Tiefel, "Anisotropically conductive composite medium," US Patent 4737112, 1988.
- [79] R. A. Dery and W. C. Jones, "Adhesive electrical interconnecting means," US Patent 4588456, 1987.
- [80] M. J. Yim, J. Hwang, and K. W. Paik, "Anisotropic conductive films (ACFs) for ultra-fine pitch Chip-On-Glass (COG) applications," *International Journal of Adhesion and Adhesives*, vol. 27, pp. 77-84, 1// 2007.
- [81] C.-K. Chung, J.-H. Kim, J.-W. Lee, K.-W. Seo, and K.-W. Paik, "Enhancement of electrical stability of anisotropic conductive film (ACF) interconnections with viscosity-controlled and high Tg ACFs in fine-pitch chip-on-glass applications," *Microelectronics Reliability*, vol. 52, pp. 217-224, 1// 2012.
- [82] Y. Myung Jin, H. Jinsang, and P. Kyung Wook, "Anisotropic conductive films (ACFs) for ultra-fine pitch chip-on-glass (COG) applications," in *Advanced Packaging Materials: Processes, Properties and Interfaces, 2005. Proceedings. International Symposium on, 2005*, pp. 181-186.
- [83] Y. P. Wu, M. O. Alam, Y. C. Chan, and B. Y. Wu, "Impact properties of flip chip interconnection using anisotropically conductive film on the glass and flexible substrate," in *Electronic Components and Technology Conference, 2003. Proceedings. 53rd, 2003*, pp. 544-548.
- [84] L. Su-Tsai, L. Yu-Min, C. Chun-Chih, C. Tai-Hong, and C. Wen-Hwa, "Development of a Novel Compliant-Bump Structure for ACA-Bonded Chip-on-Flex (COF) Interconnects With Ultra-Fine Pitch," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, pp. 33-42, 2011.
- [85] M. A. Uddin, M. O. Alam, Y. C. Chan, and H. P. Chan, "Adhesion strength and contact resistance of flip chip on flex packages—effect of curing degree of anisotropic conductive film," *Microelectronics Reliability*, vol. 44, pp. 505-514, 2004.
- [86] W.-S. Kwon and K.-W. Paik, "Fundamental understanding of ACF conduction establishment with emphasis on the thermal and mechanical analysis," *International Journal of Adhesion and Adhesives*, vol. 24, pp. 135-142, 2004.
- [87] K.-W. Jang, C.-K. Chung, W.-S. Lee, and K.-W. Paik, "Material properties of anisotropic conductive films (ACFs) and their flip chip assembly reliability in NAND flash memory applications," *Microelectronics Reliability*, vol. 48, pp. 1052-1061, 7// 2008.

- [88] J. Kiilunen, L. Frisk, and M. Hoikkanen, "The Effect of Bonding Temperature and Curing Time on Peel Strength of Anisotropically Conductive Film Flex-On-Board Samples," *Device and Materials Reliability, IEEE Transactions on*, vol. 12, pp. 455-461, 2012.
- [89] K. N. Chiang, C. W. Chang, and C. T. Lin, "Process Modeling and Thermal/Mechanical Behavior of ACA/ACF Type Flip-Chip Packages," *Journal of Electronic Packaging*, vol. 123, pp. 331-337, 2001.
- [90] K. Woon-Seong and P. Kyung-Wook, "Experimental Analysis of Mechanical and Electrical Characteristics of Metal-Coated Conductive Spheres for Anisotropic Conductive Adhesives (ACAs) Interconnection," *Components and Packaging Technologies, IEEE Transactions on*, vol. 29, pp. 528-534, 2006.
- [91] Y. C. Chan and D. Y. Luk, "Effects of bonding parameters on the reliability performance of anisotropic conductive adhesive interconnects for flip-chip-on-flex packages assembly II. Different bonding pressure," *Microelectronics Reliability*, vol. 42, pp. 1195-1204, 2002.
- [92] Y. Myung-Jin and P. Kyung-Wook, "Design and understanding of anisotropic conductive films (ACFs) for LCD packaging," in *Polymeric Electronics Packaging, 1997. Proceedings., The First IEEE International Symposium on*, 1997, pp. 233-242.
- [93] M. Chin, K. A. Iyer, and S. J. Hu, "Prediction of electrical contact resistance for anisotropic conductive adhesive assemblies," *Components and Packaging Technologies, IEEE Transactions on*, vol. 27, pp. 317-326, 2004.
- [94] M. Chin, J. R. Barber, and S. J. Hu, "Effect of elastic recovery on the electrical contact resistance in anisotropic conductive adhesive assemblies," *Components and Packaging Technologies, IEEE Transactions on*, vol. 29, pp. 137-144, 2006.
- [95] M. Chin and S. J. Hu, "A Multiple Particle Model for the Prediction of Electrical Contact Resistance in Anisotropic Conductive Adhesive Assemblies," *Components and Packaging Technologies, IEEE Transactions on*, vol. 30, pp. 745-753, 2007.
- [96] R. L. Jackson and L. Kogut, "Electrical Contact Resistance Theory for Anisotropic Conductive Films Considering Electron Tunneling and Particle Flattening," *Components and Packaging Technologies, IEEE Transactions on*, vol. 30, pp. 59-66, 2007.
- [97] X. Bin, X. Q. Shi, and D. Han, "Investigation of Mechanical and Electrical Characteristics for Cracked Conductive Particle in Anisotropic Conductive Adhesive (ACA) Assembly," *Components and Packaging Technologies, IEEE Transactions on*, vol. 31, pp. 361-369, 2008.

- [98] L. L. Mercado, J. White, V. Sarihan, and T. Y. T. Lee, "Failure mechanism study of anisotropic conductive film (ACF) packages," *Components and Packaging Technologies, IEEE Transactions on*, vol. 26, pp. 509-516, 2003.
- [99] S. H. Fan and Y. C. Chan, "Effect of misalignment on electrical characteristics of ACF joints for flip chip on flex applications," *Microelectronics Reliability*, vol. 42, pp. 1081-1090, 2002.
- [100] G. Dou, D. C. Whalley, and L. Changqing, "The effect of co-planarity variation on anisotropic conductive adhesive assemblies," in *Electronic Components and Technology Conference, 2006. Proceedings. 56th*, 2006, p. 7 pp.
- [101] B.-S. Yim, J. I. Lee, B. H. Lee, Y.-E. Shin, and J.-M. Kim, "An investigation of the reliability of solderable ICA with low-melting-point alloy (LMPA) filler," *Microelectronics Reliability*, vol. 54, pp. 2944-2950, 2014.
- [102] K. Saarinen and L. Frisk, "Reliability Testing and Modeling of Anisotropic Conductive Adhesive Joints Under Temperature Cycling Test," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 3, pp. 1512-1523, 2013.
- [103] L. Frisk, J. Järvinen, and R. Ristolainen, "Chip on flex attachment with thermoplastic ACF for RFID applications," *Microelectronics Reliability*, vol. 42, pp. 1559-1562, 2002.
- [104] L.-L. Gao, X. Chen, and H. Gao, "Mechanical Properties of Anisotropic Conductive Adhesive Film Under Hygrothermal Aging and Thermal Cycling," *Journal of Electronic Materials*, vol. 41, pp. 2001-2009, 2012.
- [105] M. Y. M. Chiang and M. Fernandez-Garcia, "Relation of swelling and Tg depression to the apparent free volume of a particle-filled, epoxy-based adhesive," *Journal of Applied Polymer Science*, vol. 87, pp. 1436-1444, 2003.
- [106] L. Frisk and K. Saarinen-Pulli, "Reliability of adhesive joined thinned chips on flexible substrates under humid conditions," *Microelectronics Reliability*, vol. 54, pp. 2058-2063, 2014.
- [107] J. Kiilunen and L. Frisk, "Hygrothermal Aging of an ACA Attached PET Flex-on-Board Assembly," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 4, pp. 181-189, 2014.
- [108] L. Daoqiang, Q. K. Tong, and C. P. Wong, "Mechanisms underlying the unstable contact resistance of conductive adhesives," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 22, pp. 228-232, 1999.

- [109] H. Kristiansen and J. Liu, "Overview of conductive adhesive interconnection technologies for LCDs," *Components, Packaging, and Manufacturing Technology, Part A, IEEE Transactions on*, vol. 21, pp. 208-214, 1998.
- [110] C. W. Tan, Y. W. Chiu, and Y. C. Chan, "Corrosion study of anisotropic conductive joints on polyimide flexible circuits," *Materials Science and Engineering: B*, vol. 98, pp. 255-264, 2003.
- [111] J. Lei, D. Han, S. Xinjun, and X. Bin, "Evaluation of a double-layer anisotropic conductive film (ACF) for fine pitch chip-on-glass (COG) interconnection," in *Electronic Packaging Technology, 2005 6th International Conference on*, 2005, pp. 344-347.
- [112] L. Zonghe and L. Johan, "Anisotropically conductive adhesive flip-chip bonding on rigid and flexible printed circuit substrates," *Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on*, vol. 19, pp. 644-660, 1996.
- [113] R. Miessner, R. Aschenbrenner, and H. Reichl, "Reliability study of flip chip on FR4 interconnections with ACA," in *Electronic Components and Technology Conference, 1999. 1999 Proceedings. 49th*, 1999, pp. 595-601.
- [114] A. Seppälä, S. Pienimaa, E. Ristolainen, and M. Director, "Flip chip joining on FR-4 substrate using ACFs," *The International Journal of Microcircuits and Electronic Packaging*, vol. 24, pp. 148-159, 2001.
- [115] J. Liu and Z. Lai, "Reliability of Anisotropically Conductive Adhesive Joints on a Flip-Chip/FR-4 Substrate," *Journal of Electronic Packaging*, vol. 124, pp. 240-245, 2002.
- [116] Y. Myung-Jin and P. Kyung-Wook, "The contact resistance and reliability of anisotropically conductive film (ACF)," *Advanced Packaging, IEEE Transactions on*, vol. 22, pp. 166-173, 1999.
- [117] J. H. Kim, T. I. Lee, J. W. Shin, T. S. Kim, and K. W. Paik, "Ultra-thin chip-in-flex (CIF) technology using anisotropic conductive films (ACFs) for wearable electronics applications," in *Electronic Components and Technology Conference (ECTC) , 2015 IEEE 65th*, 2015, pp. 714-718.
- [118] K. Il, J. Kyung-Woon, S. Ho-Young, K. Jae-Han, and P. Kyung-Wook, "Wafer-Level Packages Using Anisotropic Conductive Adhesives (ACAs) Solution for Flip-Chip Interconnections," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, pp. 792-797, 2011.

- [119] M. M. Taklo, A. Klumpp, P. Ramm, L. Kwakman, and G. Franz, "Bonding and TSV in 3D IC integration: physical analysis with plasma FIB," *Microsc. Anal.*, vol. 25, pp. 9-12, 2011.
- [120] S. Kyoung-Lim, C. Chang-Kyu, and P. Kyung-Wook, "Nanofiber anisotropic conductive adhesives (ACAs) for ultra fine pitch chip-on-film (COF) packaging," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 656-660.
- [121] S. Kyoung-Lim, H. Joon Hee, L. Jeong Yong, and P. Kyung-Wook, "Advancing Electronic Packaging Using Microsolder Balls: Making 25-nm Pitch Interconnection Possible," *Nanotechnology Magazine, IEEE*, vol. 7, pp. 24-30, 2013.
- [122] L. Sang Hoon, K. Tae Wan, and P. Kyung-Wook, "A study on nanofiber anisotropic conductive films (ACFs) for fine pitch chip-on-glass (COG) interconnections," in *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th*, 2014, pp. 1060-1063.
- [123] M. Sungwook and W. J. Chappell, "Analysis of Failure Rate by Column Distribution in Magnetically Aligned Anisotropic Conductive Adhesive," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, pp. 784-791, 2011.
- [124] K. Seung-Ho, C. Yongwon, K. Yoosun, and P. Kyung-Wook, "Flux function added solder anisotropic conductive films (ACFs) for high power and fine pitch assemblies," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 1713-1716.
- [125] K. Yoo-Sun, K. Seung-Ho, S. Jiwon, and P. Kyung-Wook, "Reliability improvement methods of solder anisotropic conductive film (ACF) joints using morphology control of solder ACF joints," in *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th*, 2014, pp. 841-845.
- [126] G. Yi Li and C. P. Wong, "Nano-Ag Filled Anisotropic Conductive Adhesives (ACA) with Self-Assembled Monolayer and Sintering Behavior for High," in *Electronic Components and Technology Conference, 2005. Proceedings. 55th*, 2005, pp. 1147-1154.
- [127] A. Gasse, C. Rossat, J. C. Souriau, C. Gillot, F. Glasser, and J. C. Clemens, "Assessment of advanced anisotropic conductive films for flip-chip interconnection based on Z axis conductors," in *Nuclear Science Symposium Conference Record, 2003 IEEE*, 2003, pp. 237-241 Vol.1.
- [128] M. D. Diop, M. Radji, A. A. Hamoui, Y. Blaquiere, and R. Izquierdo, "Evaluation of Anisotropic Conductive Films Based on Vertical Fibers for Post-CMOS Wafer-Level

- Packaging," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 3, pp. 581-591, 2013.
- [129] Y. Takayama, A. Mochizuki, A. Hino, K. Ouchi, and M. Sugimoto, "Anisotropic conductive film with through-holes filled with metallic material," ed: Google Patents, 1992.
 - [130] Y. Hotta, M. Maeda, F. Asai, and F. Eriguchi, "Development of 0.025 mm pitch anisotropic conductive film," in *Electronic Components & Technology Conference, 1998. 48th IEEE*, 1998, pp. 1042-1046.
 - [131] M. Yamaguchi, F. Asai, F. Eriguchi, and Y. Hotta, "Development of novel anisotropic conductive film (ACF)," in *Electronic Components and Technology Conference, 1999. 1999 Proceedings. 49th*, 1999, pp. 360-364.
 - [132] K. Ishibashi and J. Kimura, "A new anisotropic conductive film with arrayed conductive particles," *Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on*, vol. 19, pp. 752-757, 1996.
 - [133] J. C. Souriau, C. Rossat, A. Gasse, P. Renard, and G. Poupon, "Electrical conductive film for Flip-Chip Interconnection based on Z-axis conductors," in *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*, 2002, pp. 1151-1153.
 - [134] J. C. Souriau, J. Brun, R. Franiatte, and A. Gasse, "Development on wafer level anisotropic conductive film for flip-chip interconnection," in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, pp. 155-158 Vol.1.
 - [135] L. G. Svendsen and N. R. Bates, "Anisotropically electrically conductive article," US Patent 5262718, 1991.
 - [136] Y. Yoshida, "Anisotropic conductive film," US Patent 5262226, 1993.
 - [137] C. R. Martin, "Nanomaterials: A Membrane-Based Synthetic Approach," *Science*, vol. 266, pp. 1961-1966, 1994.
 - [138] C. R. Martin, "Membrane-Based Synthesis of Nanomaterials," *Chemistry of Materials*, vol. 8, pp. 1739-1746, 1996.
 - [139] H. Masuda and K. Fukuda, "Ordered Metal Nanohole Arrays Made by a Two-Step Replication of Honeycomb Structures of Anodic Alumina," *Science*, vol. 268, pp. 1466-1468, June 9, 1995 1995.
 - [140] P. Apel, "Track etching technique in membrane technology," *Radiation Measurements*, vol. 34, pp. 559-566, 2001.

- [141] P. Y. Apel and S. Dmitriev, "Micro- and nanoporous materials produced using accelerated heavy ion beams," *Advances in Natural Sciences. Nanoscience and Nanotechnology*, vol. 2, pp. 013002-1, 2011.
- [142] M. E. Toimil-Molares, "Characterization and properties of micro- and nanowires of controlled size, composition, and geometry fabricated by electrodeposition and ion-track technology," *Beilstein Journal of Nanotechnology*, vol. 3, pp. 860-883, 2012.
- [143] I. Schuchert, M. T. Molares, D. Dobrev, J. Vetter, R. Neumann, and M. Martin, "Electrochemical Copper Deposition in Etched Ion Track Membranes Experimental Results and a Qualitative Kinetic Model," *Journal of The Electrochemical Society*, vol. 150, pp. C189-C194, 2003.
- [144] D. Dobrev, J. Vetter, N. Angert, and R. Neumann, "Periodic reverse current electrodeposition of gold in an ultrasonic field using ion-track membranes as templates: growth of gold single-crystals," *Electrochimica Acta*, vol. 45, pp. 3117-3125, 2000.
- [145] M. Motoyama, Y. Fukunaka, T. Sakka, Y. H. Ogata, and S. Kikuchi, "Electrochemical processing of Cu and Ni nanowire arrays," *Journal of electroanalytical chemistry*, vol. 584, pp. 84-91, 2005.
- [146] C. Schönenberger, B. M. I. van der Zande, L. G. J. Fokkink, M. Henny, C. Schmid, M. Krüger, *et al.*, "Template Synthesis of Nanowires in Porous Polycarbonate Membranes: Electrochemistry and Morphology," *The Journal of Physical Chemistry B*, vol. 101, pp. 5497-5505, 1997.
- [147] M. Hasan, "Electrochemical Nucleation and Growth of Copper from Sulfuric Acid and Methanesulfonic Acid Solutions," Master thesis, Katholieke University Leuven, Belgium, 2005.
- [148] H. He and N. J. Tao, "Electrochemical fabrication of metal nanowires," *Encyclopedia of nanoscience and nanotechnology*, vol. 10, pp. 1-18, 2003.
- [149] W. Steinhögl, G. Schindler, G. Steinlesberger, and M. Engelhardt, "Size-dependent resistivity of metallic wires in the mesoscopic range," *Physical Review B*, vol. 66, p. 075414, 2002.
- [150] D. Josell, S. H. Brongersma, and Z. Tókei, "Size-Dependent Resistivity in Nanoscale Interconnects," *Annual Review of Materials Research*, vol. 39, pp. 231-254, 2009.
- [151] Q. Huang, C. M. Lilley, and M. Bode, "Surface scattering effect on the electrical resistivity of single crystalline silver nanowires self-assembled on vicinal Si (001)," *Applied Physics Letters*, vol. 95, p. 103112, 2009.

- [152] M. E. Toimil Molaes, E. M. Hühberger, C. Schaefflein, R. H. Blick, R. Neumann, and C. Trautmann, "Electrical characterization of electrochemically grown single copper nanowires," *Applied Physics Letters*, vol. 82, pp. 2139-2141, 2003.
- [153] Z. Gu, H. Ye, D. Smirnova, D. Small, and D. H. Gracias, "Reflow and Electrical Characteristics of Nanoscale Solder," *Small*, vol. 2, pp. 225-229, 2006.
- [154] S. Cuenot, C. Frégnier, S. Demoustier-Champagne, and B. Nysten, "Surface tension effect on the mechanical properties of nanomaterials measured by atomic force microscopy," *Physical Review B*, vol. 69, p. 165410, 2004.
- [155] G. Y. Jing, H. L. Duan, X. M. Sun, Z. S. Zhang, J. Xu, Y. D. Li, *et al.*, "Surface effects on elastic properties of silver nanowires: Contact atomic-force microscopy," *Physical Review B*, vol. 73, p. 235409, 2006.
- [156] G.-F. Wang and X.-Q. Feng, "Surface effects on buckling of nanowires under uniaxial compression," *Applied Physics Letters*, vol. 94, p. 141913, 2009.
- [157] L.-W. Ji, S.-J. Young, T.-H. Fang, and C.-H. Liu, "Buckling characterization of vertical ZnO nanowires using nanoindentation," *Applied Physics Letters*, vol. 90, p. 033109, 2007.
- [158] L. Wang, C. Ortiz, and M. C. Boyce, "Mechanics of Indentation into Micro- and Nanoscale Forests of Tubes, Rods, or Pillars," *Journal of Engineering Materials and Technology*, vol. 133, pp. 011014-011014, 2010.
- [159] S. Fielder, M. Zwanzig, R. Schmidt, and W. Scheel, "Nanowires in Electronics Packaging," in *Nanopackaging*, J. E. Morris, Ed., ed: Springer US, 2008, pp. 441-463.
- [160] R. Gasparac, B. J. Taft, M. A. Lapierre-Devlin, A. D. Lazareck, J. M. Xu, and S. O. Kelley, "Ultrasensitive electrocatalytic DNA detection at two-and three-dimensional nanoelectrodes," *Journal of the American Chemical Society*, vol. 126, pp. 12270-12271, 2004.
- [161] P. Serbun, F. Jordan, A. Navitski, G. Müller, I. Alber, M. Toimil-Molaes, *et al.*, "Copper nanocones grown in polymer ion-track membranes as field emitters," *The European Physical Journal Applied Physics*, vol. 58, p. 10402, 2012.
- [162] J. Duan, J. Liu, T. W. Cornelius, H. Yao, D. Mo, Y. Chen, *et al.*, "Magnetic and optical properties of cobalt nanowires fabricated in polycarbonate ion-track templates," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 267, pp. 2567-2570, 2009.

- [163] H. Yousef, K. Hjort, and M. Lindeberg, "Reliable small via interconnects made of multiple sub-micron wires in flexible PCB," *Journal of Micromechanics and Microengineering*, vol. 17, p. 700, 2007.
- [164] J. Xu, K. M. Razeeb, S. K. Sitaraman, and A. Mathewson, "The fabrication of ultra long metal nanowire bumps and their application as interconnects," in *Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on*, 2012, pp. 1-6.
- [165] J. Xu, L. Chen, A. Mathewson, and K. M. Razeeb, "Ultra-long metal nanowire arrays on solid substrate with strong bonding," *Nanoscale Research Letters*, vol. 6, pp. 525-525, 2011.
- [166] Y. Ju, M. Amano, and M. Chen, "Mechanical and electrical cold bonding based on metallic nanowire surface fasteners," *Nanotechnology*, vol. 23, p. 365202, 2012.
- [167] S. Fiedler, M. Zwanig, R. Schmidt, and W. Scheel, "Metallic submicron wires and nanolawn for microelectronic packaging: Concept and first evaluation," *NSTI Nanotech, Boston MA*, 2008.
- [168] Y. Maekawa, H. Koshikawa, and M. Yoshida, "Anisotropically conducting films consisting of sub-micron copper wires in the ion track membranes of poly(ethylene terephthalate)," *Polymer*, vol. 45, pp. 2291-2295, 2004.
- [169] E. C. H. Sykes, A. Andreu, D. A. Deadwyler, K. Daneshvar, and M. El-Kouedi, "Synthesis and characterization of nanowire-based anisotropic conductors," *Journal of nanoscience and nanotechnology*, vol. 6, pp. 1128-1134, 2006.
- [170] L. Ren-Jen, H. Yung-Yu, C. Yu-Chih, C. Syh-Yuh, and U. Ruoh-Huey, "Fabrication of Nanowire Anisotropic Conductive Film for Ultra-Fine Pitch Flip Chip Interconnection," in *Electronic Components and Technology Conference, 2005. Proceedings. 55th*, 2005, pp. 66-70.
- [171] C. Hsien-Chie, C. Wen-Hwa, L. Chieh-Sheng, H. Yung-Yu, and U. Ruoh-Huey, "On the Thermal-Mechanical Behaviors of a Novel Nanowire-Based Anisotropic Conductive Film Technology," *Advanced Packaging, IEEE Transactions on*, vol. 32, pp. 546-563, 2009.
- [172] H.-C. Cheng, K.-Y. Hsieh, and K.-M. Chen, "Thermal–mechanical optimization of a novel nanocomposite-film typed flip chip technology," *Microelectronics Reliability*, vol. 51, pp. 826-836, 2011.
- [173] F. Stam, K. M. Razeeb, S. Salwa, and A. Mathewson, "Micro-nano interconnect between gold bond pads and copper nano-wires embedded in a polymer template," in

- Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 1470-1474.
- [174] J. Xu, A. Munari, E. Dalton, A. Mathewson, and K. M. Razeeb, "Silver nanowire array-polymer composite as thermal interface material," *Journal of Applied Physics*, vol. 106, p. 124310, 2009.
- [175] K. M. Razeeb, M. Hasan, D. Gautam, and E. Dalton, "Metallic Nanowire-Polymer Composite as Thermal Interface Material," in *Meeting Abstracts*, 2014, pp. 1862-1862.
- [176] K. M. Razeeb, J. Xu, E. Dalton, S. Roy, and A. Mathewson, "A process for the manufacture of large area, homogeneous, ultra-long, one dimensional nanostructures on a solid substrate and the application of same," UK Patent 1013456.7, 2010.
- [177] Y. Kwon, J. Seok, J.-Q. Lu, T. S. Cale, and R. J. Gutmann, "Critical adhesion energy of benzocyclobutene-bonded wafers," *Journal of The Electrochemical Society*, vol. 153, pp. G347-G352, 2006.
- [178] <http://imagej.nih.gov/ij/>, ed.
- [179] M. T. Molares, V. Buschmann, D. Dobrev, R. Neumann, R. Scholz, I. U. Schuchert, *et al.*, "Single-crystalline copper nanowires produced by electrochemical deposition in polymeric ion track membranes," *Adv. Mater.*, vol. 13, pp. 62-65, 2001.
- [180] Y. Konishi, M. Motoyama, H. Matsushima, Y. Fukunaka, R. Ishii, and Y. Ito, "Electrodeposition of Cu nanowire arrays with a template," *Journal of Electroanalytical Chemistry*, vol. 559, pp. 149-153, 2003.
- [181] M. E. Toimil Molares, J. Brötz, V. Buschmann, D. Dobrev, R. Neumann, R. Scholz, *et al.*, "Etched heavy ion tracks in polycarbonate as template for copper nanowires," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 185, pp. 192-197, 2001.
- [182] J. Fu, S. Cherevko, and C.-H. Chung, "Electroplating of metal nanotubes and nanowires in a high aspect-ratio nanotemplate," *Electrochemistry Communications*, vol. 10, pp. 514-518, 2008.
- [183] M. Hasan, T. Chowdhury, and J. Rohan, "Core/Shell (Cu/Cu₂O) Nanotubes as High Performance Anode Materials for Li-ion Rechargeable Batteries," *ECS Transactions*, vol. 19, pp. 3-15, 2009.
- [184] D. Dobrev, J. Vetter, and N. Angert, "Electrochemical preparation of metal microstructures on large areas of etched ion track membranes," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 149, pp. 207-212, 1999.

- [185] S. Yu, N. Li, J. Wharton, and C. R. Martin, "Nano Wheat Fields Prepared by Plasma-Etching Gold Nanowire-Containing Membranes," *Nano Letters*, vol. 3, pp. 815-818, 2003.
- [186] B. Wunderlich, "Basics of Thermal Analysis," *Thermal Analysis of Polymeric Materials*, pp. 71-188, 2005.
- [187] B. Wunderlich, "Thermal Analysis Tools," in *Thermal Analysis of Polymeric Materials*, ed: Springer Berlin Heidelberg, 2005, pp. 279-454.
- [188] S. Sohn, "Crystallization Behavior of Bisphenol-A Polycarbonate: Effects of Crystallization Time, Temperature, and Molar Mass," Virginia Polytechnic Institute and State University, 2000.
- [189] J. S. Hwang, "Filler size and content effects on the composite properties of anisotropic conductive films (ACFs) and reliability of flip chip assembly using ACFs," *Microelectronics Reliability*, vol. 48, pp. 645-651, 2008.
- [190] A. Parretta and A. Rubino, "Kinetics of intermetallics transformation in sputtered Cu-In alloys studied by electrical resistance measurements," *Solid state communications*, vol. 96, pp. 767-770, 1995.
- [191] D. Jinglai, L. Jie, M. Dan, Y. Huijun, M. Khan, C. Yonghui, *et al.*, "Controlled crystallinity and crystallographic orientation of Cu nanowires fabricated in ion-track templates," *Nanotechnology*, vol. 21, p. 365605, 2010.
- [192] J. Nezamdost, A. Zolanvari, H. Sadeghi, and J. Nezamdost, "Nanocrystalline Fe Thin Films on Si (100) Substrate," *Middle-East Journal of Scientific Research*, vol. 18, pp. 845-848, 2013.
- [193] J. H. Constable, "Analysis of the constriction resistance in an ACF bond," *Components and Packaging Technologies, IEEE Transactions on*, vol. 29, pp. 494-501, 2006.
- [194] <http://www.phoenixbv.com/product.php?prodid=50010105>, ed.
- [195] G. Dou, D. C. Whalley, C. Liu, and Y. C. Chan, "An experimental methodology for the study of co-planarity variation effects in anisotropic conductive adhesive assemblies," *Soldering & Surface Mount Technology*, vol. 22, pp. 47-55, 2010.
- [196] M. Hutter, F. Hohnke, H. Oppermann, M. Klein, and G. Engelmann, "Assembly and reliability of flip chip solder joints using miniaturized Au/Sn bumps," in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, pp. 49-57 Vol.1.
- [197] J. D. Reed, M. Lueck, C. Gregory, A. Huffman, J. M. Lannon, and D. Temple, "High density interconnect at 10 μm pitch with mechanically keyed Cu/Sn-Cu and Cu-Cu

- bonding for 3-D integration," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 846-852.
- [198] S. L. Wright, R. Polastre, H. Gan, L. P. Buchwalter, R. Horton, P. S. Andry, *et al.*, "Characterization of micro-bump C4 interconnects for Si-carrier SOP applications," in *Electronic Components and Technology Conference, 2006. Proceedings. 56th*, 2006, p. 8 pp.
- [199] S. Fiedler, M. Zwanzig, R. Schmidt, E. Auerswald, M. Klein, W. Scheel, *et al.*, "Evaluation of Metallic Nano-Lawn Structures for Application in Microelectronic Packaging," in *Electronics Systemintegration Technology Conference, 2006. 1st*, 2006, pp. 886-891.
- [200] R. Ramasubramaniam, J. Chen, and H. Liu, "Homogeneous carbon nanotube/polymer composites for electrical applications," *Applied Physics Letters*, vol. 83, pp. 2928-2930, 2003.
- [201] M. Stucchi, D. Perry, G. Katti, W. Dehaene, and D. Velenis, "Test Structures for Characterization of Through-Silicon Vias," *Semiconductor Manufacturing, IEEE Transactions on*, vol. 25, pp. 355-364, 2012.
- [202] R. Sihlbom, M. Dernevik, L. Zonghe, P. Starski, and L. Johan, "Conductive adhesives for high-frequency applications," in *Polymeric Electronics Packaging, 1997. Proceedings., The First IEEE International Symposium on*, 1997, pp. 123-130.
- [203] M. Dernevik, R. Sihlbom, K. Axelsson, L. Zonghe, L. Johan, and P. Starski, "Electrically conductive adhesives at microwave frequencies," in *Electronic Components & Technology Conference, 1998. 48th IEEE*, 1998, pp. 1026-1030.
- [204] M. J. Yim and K. W. Paik, "High Frequency Properties of Anisotropic Conductive Films (ACFs) for Flip Chip Package Application," *Electronic Materials Letters*, vol. 2, pp. 7-14, 2006.
- [205] C. Bermond, L. Cadix, A. Farcy, T. Lacrevez, P. Leduc, and B. Flechet, "High frequency characterization and modeling of high density TSV in 3D integrated circuits," in *Signal Propagation on Interconnects, 2009. SPI '09. IEEE Workshop on*, 2009, pp. 1-4.
- [206] K. C. Gupta, *Microwaves*: Wiley Eastern Limited, 1989.
- [207] W. R. Eisenstadt and Y. Eo, "S-parameter-based IC interconnect transmission line characterization," *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on*, vol. 15, pp. 483-490, 1992.
- [208] <https://www.cmicro.com/products/probes/wincal-xe>, ed.

- [209] L. Floyd, J. Pike, J. Tao, and N. Jackson, "Observations on substrate characterisation through Coplanar Transmission Line Impedance measurements," in *Microelectronic Test Structures (ICMTS), 2015 International Conference on*, 2015, pp. 224-229.
- [210] "International Technology Roadmap for Semiconductors: ASSEMBLY AND PACKAGING," ed, 2012.
- [211] M. S. Bakir, C. King, D. Sekar, H. Thacker, B. Dang, H. Gang, *et al.*, "3D heterogeneous integrated systems: Liquid cooling, power delivery, and implementation," in *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, 2008, pp. 663-670.
- [212] R. Prasher, "Thermal Interface Materials: Historical Perspective, Status, and Future Directions," *Proceedings of the IEEE*, vol. 94, pp. 1571-1586, 2006.
- [213] C. W. Nan, Z. Shi, and Y. Lin, "A simple model for thermal conductivity of carbon nanotube-based composites," *Chemical Physics Letters*, vol. 375, pp. 666-669, 2003.
- [214] S. Vishal, T. Siegmund, and S. V. Garimella, "Optimization of thermal interface materials for electronics cooling applications," *Components and Packaging Technologies, IEEE Transactions on*, vol. 27, pp. 244-252, 2004.
- [215] K. M. Razeeb and E. Dalton, *Nanowire-Polymer Nanocomposites as Thermal Interface Material*: INTECH Open Access Publisher, 2011.
- [216] L. Zhang, S.-b. Xue, L.-l. Gao, Z. Sheng, S.-l. Yu, Y. Chen, *et al.*, "Reliability study of Sn–Ag–Cu–Ce soldered joints in quad flat packages," *Microelectronics Reliability*, vol. 50, pp. 2071-2077, 2010.
- [217] R. Coyle, R. Parker, B. Arfaei, F. Mutuku, K. Sweatman, K. Howell, *et al.*, "The effect of nickel microalloying on thermal fatigue reliability and microstructure of SAC105 and SAC205 solders," in *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th*, 2014, pp. 425-440.
- [218] L. Shijian and C. P. Wong, "Influence of temperature and humidity on adhesion of underfills for flip chip packaging," in *Electronic Components and Technology Conference, 2001. Proceedings., 51st*, 2001, pp. 155-162.
- [219] K. Saarinen and L. Frisk, "Changes in Adhesion of Non-Conductive Adhesive Attachments During Humidity Test," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, pp. 1082-1088, 2011.
- [220] K. Sun-Chul, H. Myung-Hwan, L. Ji-Hyun, and K. Young-Ho, "Development of highly reliable flip-chip bonding technology using non-conductive adhesives (NCAs) for 20 μm pitch application," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 785-789.

- [221] R. Rongen, R. Roucou, P. J. vd Wel, F. Voogt, F. Swartjes, and K. Weide-Zaage, "Reliability of Wafer Level Chip Scale Packages," *Microelectronics Reliability*, vol. 54, pp. 1988-1994, 2014.
- [222] K. Jae-Myeong, K. Byung-Hyun, J. Myeong-Hyeok, Y. Sehoon, and P. Young-Bae, "Effects of surface finish conditions on interfacial reaction characteristics and mechanical reliability of novel Sn-1.2Ag-0.7Cu-0.4In solder bump," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 1272-1277.
- [223] J. Meng, P. Stark, A. Dasgupta, M. Sillanpaa, E. Hussa, J. P. Seppanen, *et al.*, "Effect of strain rate on adhesion strength of Anisotropic Conductive Film (ACF) joints," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 1252-1258.
- [224] Y. Li and C. P. Wong, "Recent advances of conductive adhesives as a lead-free alternative in electronic packaging: Materials, processing, reliability and applications," *Materials Science and Engineering: R: Reports*, vol. 51, pp. 1-35, 2006.
- [225] JESD22-A106B, "Thermal Shock," ed, 2004, p. 4.
- [226] JESD22-A101C, "Steady State Temperature Humidity Bias Life Test," p. 6, 2009.
- [227] L. Frisk, K. Saarinen, and A. Cumini, "Reliability of ACF Interconnections on FR-4 Substrates," *IEEE Transactions on Components and Packaging Technologies*, vol. 33, pp. 138-147, 2010.
- [228] J. H. Zhang, Y. C. Chan, M. O. Alam, and S. Fu, "Contact resistance and adhesion performance of ACF interconnections to aluminum metallization," *Microelectronics Reliability*, vol. 43, pp. 1303-1310, 2003.
- [229] S. Lahokallio, J. Kiilunen, and L. Frisk, "High temperature reliability of electrically conductive adhesive attached temperature sensors on flexible polyimide substrates," *Microelectronics Reliability*, vol. 54, pp. 2017-2022, 2014.
- [230] W. Zhou, W. Low Siu, L. Neo Yong, K. Eng Meow, and M. Huang, "Studies on moisture-induced failures in ACF interconnection," in *Electronics Packaging Technology Conference, 2002. 4th*, 2002, pp. 133-138.
- [231] G. Weibin, H. Shimin, Y. Minjiao, J. long, and D. Yi, "The effects of hydrothermal aging on properties and structure of bisphenol A polycarbonate," *Polymer Degradation and Stability*, vol. 94, pp. 13-17, 2009.
- [232] K. N. Tu, "Recent advances on electromigration in very-large-scale-integration of interconnects," *Journal of Applied Physics*, vol. 94, pp. 5451-5473, 2003.

- [233] S. A. Khan, N. Kumbhat, A. Goyal, K. Okoshi, P. Raj, G. Meyer-Berg, *et al.*, "High current-carrying and highly-reliable 30 um diameter Cu-Cu area-array interconnections without solder," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 577-582.