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Organic Functionalisation, Doping and Characterisation of Semiconductor Surfaces for Future CMOS Device Applications

John Joseph O'Connell, B.Sc. (Hons), M.Sc.

Department of Chemistry

University College Cork, Ireland



Presented for the degree of Doctor of Philosophy to the National University of Ireland

Supervisors: Prof. Justin D. Holmes

Dr Gerard P. McGlacken

Head of Department: Prof. Justin D. Holmes

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DECLARATION

I, John Joseph O'Connell, certify that the work I am submitting is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents. I have read and understood the regulations of University College Cork concerning plagiarism.

_____

John Joseph O'Connell

ABSTRACT

Semiconductor materials have long been the driving force for the advancement of technology since their inception in the mid-20th century. Traditionally, micro-electronic devices based upon these materials have scaled down in size and doubled in transistor density in accordance with the well-known Moore's law, enabling consumer products with outstanding computational power at lower costs and with smaller footprints. According to the International Technology Roadmap for Semiconductors (ITRS), the scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) is proceeding at a rapid pace and will reach sub-10 nm dimensions in the coming years. This scaling presents many challenges, not only in terms of metrology but also in terms of the material preparation especially with respect to doping, leading to the moniker "More-than-Moore". Current transistor technologies are based on the use of semiconductor junctions formed by the introduction of dopant atoms into the material using various methodologies and at device sizes below 10 nm, high concentration gradients become a necessity. Doping, the controlled and purposeful addition of impurities to a semiconductor, is one of the most important steps in the material preparation with uniform and confined doping to form ultra-shallow junctions at source and drain extension regions being one of the key enablers for the continued scaling of devices. Monolayer doping has shown promise to satisfy the need to conformally dope at such small feature sizes.

This thesis aims to investigate the potential of monolayer doping to complement or replace conventional doping technologies currently in use in CMOS fabrication facilities across the world.

Chapter 1 summarises and critically assesses developments in the last number of years regarding the application of gas and solution phase doping techniques to dope silicon-, germanium- and III-V-based materials and nanostructures to obtain shallow diffusion depths coupled with high carrier concentrations and abrupt junctions. Advanced doping technologies are key for the continued scaling of semiconductor devices and the maintenance of device performance beyond the 14 nm technology node. Due to limitations of conventional ion-beam implantation with thin body and 3D device geometries, techniques which allow precise control over dopant diffusion and concentration in addition to excellent conformality on 3D device surfaces are required. Spin-on doping has shown promise as an old technique for new materials, through its application as a hybrid technique with other dopant methods, but may not be suitable for conformal doping of nanostructures. Additionally, residues remain after the spin-on-doping process which are quite difficult to remove. In-situ doping of nanostructures is especially common for bottom-up grown nanostructures but concentration gradients in the device are common in addition to issues with nanostructure morphology. Monolayer doping (MLD) has been shown to satisfy the requirements for extended defect-free, conformal and controllable doping on many materials ranging from the traditional silicon and germanium devices to emerging replacement materials such as III-V compounds but challenges still remain, especially with regard to metrology and surface chemistry at such small feature sizes.

Chapter 2 details the experimental methods used to functionalise the semiconductor surfaces with the dopant-containing molecules. In the case of custom-synthesised precursors, the reaction schemes and synthetic procedures are outlined. Characterisation methods and procedures are also described.

Chapter 3 discusses the functionalisation of planar Si substrates and also nanowire devices with organo-arsenic monolayers. Characterisation of doped structures after the MLD process confirmed that they remained defect and damage free, with no indication of increased roughness or a change in morphology. X-ray photoelectron spectroscopy (XPS) characterisation confirmed the presence of an organo-arsenic monolayer on the Si surface and was used to monitor the Si oxide level post-functionalisation. Electrical characterisation of the doped substrates and nanowire test structures allowed determination of resistivity, sheet resistance and active doping levels. Extremely high As-doped Si substrates and nanowire devices could be obtained and controlled using specific capping and annealing steps. Significantly, the As-doped nanowires exhibited resistances several orders of magnitude lower than the pre-doped materials. High-resolution, cross-sectional TEM imaging showed that the doped nanostructures remained without extended defects, which are easily visible using electron microscopy.

Chapter 4 extended the work undertaken in chapter 3 and investigates the application of click-chemistry i.e. azide-alkyne cycloaddition reaction, to introduce dopant-containing azides onto reactive terminal acetylene groups. Covalently bonded and well-ordered alkyne-terminated monolayers were prepared from a range of commercially available dialkyne precursors using a well-known thermal hydrosilylation mechanism to form an acetylene-terminated monolayer. The terminal acetylene moieties were further functionalised through the application of copper-catalysed azide-alkyne cycloaddition (CuAAC) reactions between dopant-containing azides and the terminal acetylene groups. The introduction of dopant molecules *via* this method does not require harsh conditions typically employed in traditional monolayer doping approaches, enabling greater surface coverage with improved

resistance towards re-oxidation. X-ray photoelectron spectroscopy studies showed successful dialkyne incorporation with minimal Si surface oxidation and also showed successful azide-alkyne cycloaddition through monitoring of the C *1s* and N *1s* core-level spectra. Electrochemical capacitance-voltage (ECV) measurements showed effective diffusion of the activated dopant atoms into the Si substrates.

Chapter 5 outlines the functionalisation of Si+S containing monolayers as well as Sn-containing monolayers of InGaAs substrates. Epitaxial InGaAs layers were grown on semi-insulating InP and functionalised with both S and Si using mercaptopropyltriethoxysilane (MPTES) and Sn using allyltributylstannane (ATBS). The functionalised surfaces were characterised using x-ray photoelectron spectroscopy (XPS). Dopant diffusion was monitored using electrochemical capacitance-voltage measurements and secondary ion mass-spectrometry (SIMS) characterisation. Raman scattering was also utilized to non-destructively determine the presence of dopant atoms, prior to destructive analysis, by comparison to a blank undoped sample. Additionally, due to the As-dominant surface chemistry, the resistance of the functionalised surfaces to oxidation in ambient conditions was elucidated by monitoring of the As *3d* core-level peak for the presence of oxide components.

Finally, Chapter 6 presents important conclusions and future outlook.

LIST OF ABBREVIATIONS

2D	**Two dimensional**
3D	**Three dimensional**
AA	**Arsenic azide**
ABAPE	**Allyl boronic acid pinacol ester**
ADP	**Allyldiphenyl phosphine**
AFM	**Atomic Force Microscopy**
APT	**Atom probe tomography**
ATBS	**Allyl tribuytlstannane**
BOX	**Buried oxide**
CMOS	**Complementary Metal Oxide Semiconductor**
CuAAC	**Copper-catalysed azide-alkyne cycloaddition**
CVD	**Chemical Vapour Deposition**
DI	**Deionised Water**
DPP	**Diphenylphosphine**
DPPA	**Diphenylphosphoryl azide**
DPPO	**Diphenylphosphine oxide**
FET	**Field-Effect Transistor**
FFT	**Fast Fourier Transform**
FIB	**Focused Ion Beam**
FIBDD	**Focused Ion Beam Direct Deposition**
FinFET	**Fin Field-Effect Transistor**
GeOI	**Germanium on insulator**
HF	**Hydrofluoric Acid**
HRTEM	**High Resolution Transmission Electron Microscopy**
IPA	**Isopropyl alcohol**
ITRS	**International Technology Roadmap for Semiconductors**
KPFM	**Kelvin Probe Force Microscopy**
MBE	**Molecular Beam Epitaxy**
MLCD	**Monolayer Contact Doping**

MLD	**Monolayer Doping**
MOCVD	**Metal Organic Chemical Vapour Deposition**
MOSFET	**Metal Oxide Semiconductor Field-Effect Transistor**
MOVPE	**Meta Organic Vapour Phase Epitaxy**
MPTES	**Mercaptopropyltriethoxysilane**
NIL	**Nanoimprint lithography**
NIST	**National Institute of Standards and Technology**
NMOS	**n-channel MOSFET**
NW	**Nanowire**
ODPA	**Octadecylphosphonic acid**
PDEVP	**poly(diethylvinylphosphonate)**
PMOS	**p-channel MOSFET**
PV	**Photovoltaic**
PVBAPE	**poly(vinylboronic acid pinacol ester)**
RCA	**Radio Corporation of America**
RTA	**Rapid Thermal Anneal**
SEM	**Scanning Electron Microscopy**
SIMS	**Secondary Ion Mass Spectrometry**
SOD	**Spin on dopant**
SOI	**Silicon on insulator**
SRP	**Spreading resistance**
STM	**Scanning Tunnelling Microscopy**
TAA	**Triallylarsine**
TEM	**Transmission Electron Microscopy**
TEMEP	**Tetraethylmethylene diphosphonate**
TGA	**Thermogravimetric Analysis**
TOF-SIMS	**Time-of-flight SIMS**
TPPO	**Triphenylphosphine oxide**
UHV	**Ultra-high vacuum**
UV	**Ultraviolet**
XPS	**X-ray photoelectron spectroscopy**

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To, Eoin, Cian, Joe, Colm Eile, Hugh and Dave; I'd count you lot amongst my closest friends and I wish you only the very best in your lives both personally and professionally.

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Dedicated to my family

Chapter 1

Chemical Approaches for Doping of Nanodevice Architectures

This chapter has been published in IOP Nanotechnology as an invited review. Consequently, sections of the chapter such as the abstract and introduction may contain repeating concepts and paragraphs

O'Connell, J.; Biswas, S.; Duffy, R. and Holmes, J. D. Chemical approaches for doping nanodevice architectures *Nanotechnology* **2016**, *27* (34), 342002.

1 CHEMICAL APPROACHES FOR DOPING NANODEVICE ARCHITECTURES

1.1 ABSTRACT

Advanced doping technologies are key for the continued scaling of semiconductor devices and the maintenance of device performance beyond the 14 nm technology node. Due to limitations of conventional ion-beam implantation with thin body and 3D device geometries, techniques which allow precise control over dopant diffusion and concentration, in addition to excellent conformality on 3D device surfaces, are required. Spin-on doping has shown promise as a conventional technique for doping new materials, particularly through application with other dopant methods, but may not be suitable for conformal doping of nanostructures. Additionally, residues remain after most spin-on-doping process which are often difficult to remove. In-situ doping of nanostructures is especially common for bottom-up grown nanostructures but problems associated with concentration gradients and morphology changes are commonly experienced. Monolayer doping (MLD) has been shown to satisfy the requirements for extended defect-free, conformal and controllable doping on many materials ranging from traditional silicon and germanium devices to emerging replacement materials such as III-V compounds but challenges still remain, especially with regard to metrology and surface chemistry at such small feature sizes. This chapter summarises and critically assesses developments over the last number of years regarding the application of gas and solution phase techniques to dope silicon-, germanium- and III-V-based materials and nanostructures to obtain shallow diffusion depths coupled with high carrier concentrations and abrupt junctions.

1.2 INTRODUCTION AND MOTIVATION

Semiconductor devices sizes have been decreasing perennially since their inception.[1–4] Metal-oxide-semiconductor field-effect transistors (MOSFETs) currently available in computers and smartphones are now fabricated with feature sizes approaching tens of nanometres at most, not only due to the rapid development of state-of-the-art fabrication tools and processes but also because of an increased understanding of device operation at these extreme scales. With smaller devices comes increased manufacturing efficiency with more devices per wafer and lower cost per die, provided fabrication technology and knowledge can keep up commensurately. Increased scaling in conjunction with other developments have greatly increased the available power and number of applications for transistor technology. The conventional operation model of a transistor, *i.e.* based on drift-diffusion current flow, may come to be replaced at sub-10 nm dimensions by more physical models such as quantum tunnelling.

Advanced lithography fabrication techniques currently used within the semiconductor industry are beginning to reach limits in terms of their effectiveness at small feature sizes. Additionally, difficulties are being encountered with deposition of dielectric layers in new device architectures. Dielectric layers are now approaching dimensions of several atoms thick in relation to the surrounding device structure as shown in **Figure 1.1**. To mitigate this, current devices are now transitioning from flat, planar structures to three dimensional geometries, *e.g.* fin field effect transistors (FinFETs) which contain a much wider dielectric layer than traditional MOSFET devices, allowing for increased performance at ever-decreasing feature sizes. Ideally, semiconductors at the nanoscale require ultra-shallow junctions with sharp dopant

profiles. The ideal ultra-shallow junction needs (i) low dopant diffusivity to allow device scaling to continue and (ii) high dopant solubility.[5]

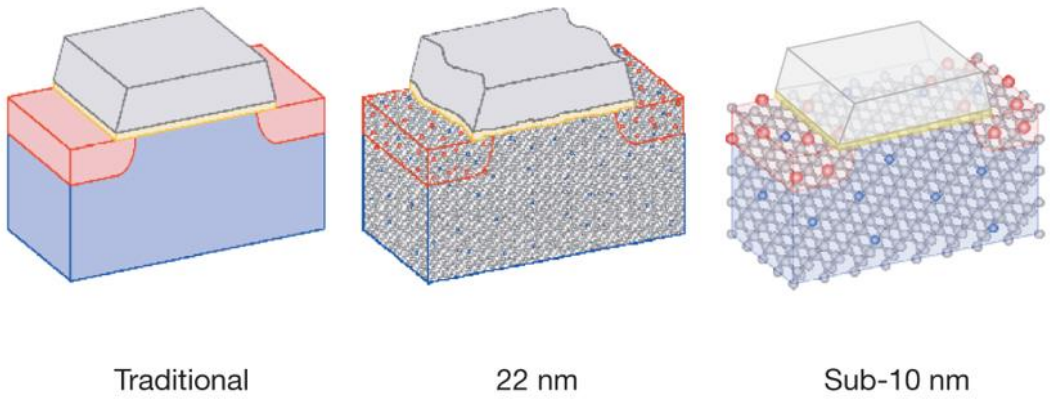


Figure 1.1. Schematic showing the shrinkage of the dielectric layer shown in yellow, as technology nodes reduce. At sub-10 nm the thickness approaches 0.5 nm, on the order of several atoms in thickness[6] Adapted from ref: 6

Ion implantation is considered the most common technique to introduce dopant atoms into a semiconductor material. The technique suffers from a number of drawbacks at the nanoscale such as stochastic dopant distribution and an inability to control the depth within a nanometre. More importantly, especially at the nanoscale, the high-energy ion beam either damages the device being doped or the atoms pass straight through the crystal lattice while still causing the same damage. Most pertinently, however, the biggest problem with ion implantation is its inability to conformally dope non-planar device geometries like the FinFET shown in **Figure 1.2**. The chemical techniques discussed herein may prove to be successful for the non-destructive and conformal doping of future device architectures, that is currently unattainable when using ion implantation.

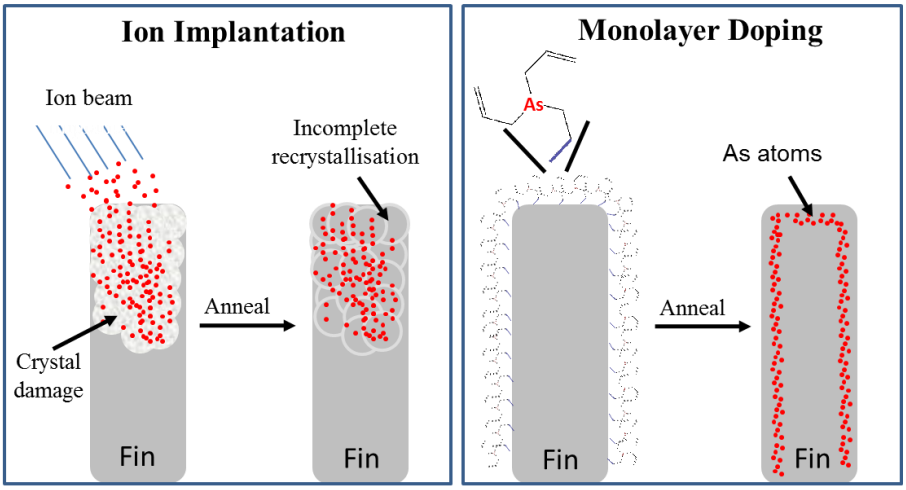


Figure 1.2. Schematic representation of the incompatibility of ion-beam implantation with extreme 3D nanostructures such as FinFETs. (a) Implant is unidirectional and at high energy causing crystal lattice damage and non-homogenous dopant distribution. The subsequent anneal does not completely recrystallise the crystal structure leading to the formation of extended defects which are visible by electron microscopy. (b) Arsenic-containing monolayers covalently bonded to surface of fin structure and subsequent conformal diffusion of the arsenic atoms into the fin body.

1.3 MONOLAYER DOPING

Monolayer doping (MLD) is one potential technique for the replacement of ion-implantation. MLD comprises two steps: (1) functionalisation of a semiconductor surface with a *p*- or *n*- dopant-containing molecule and (2) subsequent diffusion of the surface-bound, chemisorbed dopant atoms into the semiconductor material *via* a rapid-thermal-anneal step. The functionalisation step is most commonly a thermally-initiated hydrosilylation reaction between a hydrogen-passivated semiconductor surface and a labile C=C site on the dopant-containing molecule. Due to the rich and

established chemistry that can be carried out on semiconductor surfaces, many aspects of the MLD process such as the initial surface preparations, molecular footprints, choice of capping layer and the rapid-thermal-anneal recipe can all be optimised and tailored to the particular process, material and required dopant concentration and depth.[7–17] **Figure 1.3** displays an example of a typical MLD process using commercially available triallylphosphine. The MLD process is generally straightforward and may be carried out at its simplest in a Schlenk flask and can easily be scaled up to wafer scale process. The MLD process is also versatile in that it can be applied to bulk semiconductor surfaces and nanostructures, often without the need to change the passivation and functionalisation procedures.

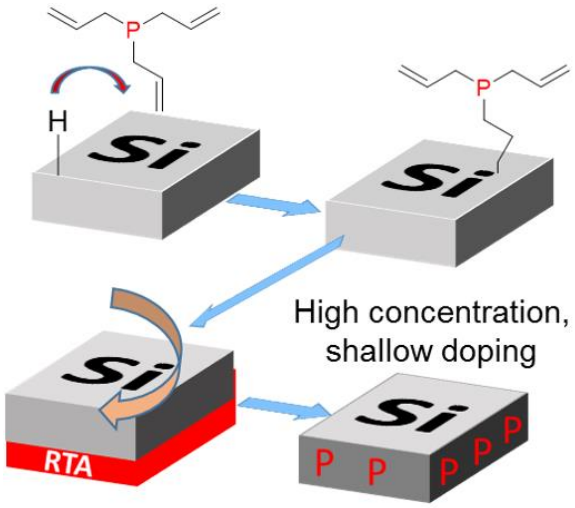


Figure 1.3. Schematic depicting a typical phosphorus MLD process A hydrosilylation reaction occurs between a reactive H-passivated Si surface and the labile C=C site on the dopant containing molecule, in this case triallylphosphine, resulting in a covalently bonded molecular layer. The samples are then capped with 50 nm of SiO_2 and subjected to a rapid-thermal-anneal (RTA) step resulting in high concentration, shallow doping of silicon.

1.3.1 Monolayer doping on Si

The ubiquity of Si as the primary platform for device fabrication in CMOS applications, as well as its established surface chemistry, played a large role in its choice as the initial material on which to attempt the first MLD process. Ho *et al.* were the first to report the MLD process on Si where allylboronic acid pinacol ester (ABAPE) in a 25 % v/v solution in mesitylene was used to passivate a H-terminated Si surface with a boron-containing monolayer.[18] A standard rapid-thermal-anneal recipe of temperatures between 950 – 1000 ^{o}C for 5 seconds was used. For ultra-shallow junctions, shorter times at a given temperature are required to supress transient-enhanced diffusion and therefore reduce the final dopant diffusion depth. Bulk blanket substrates of Si exhibited B concentrations approaching 5×10^{20} cm^{-3}, with this concentration decreasing sharply to 10^{17} cm^{-3} at depths of 18 nm for a sample annealed at 950 ^{o}C and 43 nm for a sample annealed at 1000 ^{o}C.

Ho and co-workers also applied the MLD process to chemically intrinsic, bottom-up grown Si nanowires (NWs) in the same study using a Ti/Al source and drain contacts to form a two-terminal device. Pre-MLD nanowires exhibited resistances on the order of 100 GΩ, partly due to the large Schottky barrier at the metal-nanowire interface. Post-MLD nanowires, while showing a significantly lower resistance of 2 MΩ, still displayed quite a high resistance overall due to the Schottky barriers at the metal-wire interface. The MLD process was also applied to silicon-on-insulator (SOI) substrates containing fabricated field-effect transistors (FETs) in the same study.[18] The impact of MLD on the as-fabricated FET electrical characteristics was stark, with undoped tungsten contacts delivering ~ 0.1 μA at 0.5 V. This observation of lower resistance and improved switching properties was attributed to the thinning of the Schottky

barrier at the metal-SOI interfaces. This seminal work laid the foundations for future research into MLD but still left many avenues to be explored especially with regard to fine tuning of molecular footprints, the role of carbon-incorporation from the organic molecular precursors, rapid-thermal-anneal parameters, more detailed surface analysis and more complex device characterisation in addition to ensuring the defect-free nature of the nanostructures post-MLD.

Indeed, in further work by Ho and co-workers, to investigate the role of anneal temperature and duration, a similar MLD process was applied on a larger, 4 inch wafer-scale but this time using spike-annealing, *i.e.* a high temperature anneal with a dwell time of less than 1s at the target temperature, with a fast ramp-up and ramp-down time, instead of a conventional rapid-thermal-anneal process.[19] For the phosphorus MLD process, surface doping concentrations of $\sim 2.5 \times 10^{20}$, 3.5×10^{20}, 4×10^{20}, 5.5×10^{20} atoms/cm^3 were observed for 900, 950, 1000, 1050 °C spike anneal temperatures respectively.

The concentrations achieved are close to the reported solid solubility limits of P in Si at the temperatures used, with the limit being exceeded at 1050 °C showing a beneficial aspect of MLD. Applying a boron-MLD procedure on a 4 inch wafer scale in the same study achieved 2 nm junction depths for spike anneals at 950-1050 °C. This is expected due to the lower diffusivity of B in Si. The combination of MLD and spike annealing is advantageous in that it permits the formation of such shallow junctions without needing to use sub-millisecond, non-equilibrium annealing methods such as flash and laser annealing.[20,21] Unfortunately, a large error is introduced when measuring the dopant diffusion depth at such shallow depths, as the resolution limit of SIMS becomes a limiting factor, again highlighting a need for metrology to catch up

with the increasingly stringent characterisation requirements of ultra-shallow junctions. Potential effects of carbon incorporation during dopant diffusion were investigated using a non-contact photovoltage measurement as carbon will always be present at the surface during a SIMS analysis even with a pre-emptive cleaning step.[22] Due to the use of organic, carbon-based precursors in MLD, it is important to investigate the potential effect of carbon in MLD-processed materials. Average leakage currents were found to be much less than the then state-of-the art ultra-shallow junction (USJ) leakage currents.[23]

With the ability to finely control the dopant diffusion depth and the effect of carbon found to be negligible on the material electrical properties, a logical next step was to scale up the MLD process in order for it to be applied to a full size 300 mm wafer scale as found in the vast majority of the semiconductor manufacturing plants worldwide. Workers at CNSE Albany and SEMATECH first used phosphorus-MLD, using an unnamed P-based molecule, to conformally dope a 300 mm size wafer. In addition they also investigated the application of the P-MLD process to a small feature size (20 nm) FinFET.[24] Ang and co-workers subjected a H-terminated 300 mm Si wafer to a P-MLD process and following SiO_2 passivation utilised a spike anneal between 1000-1100 °C to cause in-diffusion of the dopant. Dopant concentrations for phosphorus achieved using the P-MLD process approached 1×10^{22} atoms/cm^3 at sub 5-nm depths. In the same study, an analogous process to that applied to the 300 mm wafers was applied to a FinFET with a fin width of ~20 nm and gate length of ~40 nm. The data obtained demonstrated that MLD permits the formation of uniform silicide contacts whilst maintaining a defect-free fin doping profile, which is advantageous when compared to an ion-implanted fin where a high density of defects is often

observed due to implant damage. The damage caused by ion-implantation causes undesirable silicidation along the dislocation path and leads to poor quality silicide formation. Silicide uniformity is a crucial attribute to consider when delivering low parasitic fin resistance. Ang and co-workers [24] demonstrated the application of the MLD process to dope pseudomorphic SiGe and Si eptaxial films with excellent single crystalline quality which showed significant enhancement over ion-implanted analogues. This ability to control the quality of the silicide formation in addition to the lack of damage to the FinFET structures makes MLD a very attractive alternative to traditional doping techniques.

The previously mentioned papers gradually built the foundations of MLD techniques through the use of well-established surface chemistries. Sample processing, *i.e.* hydrosilylation, capping layer deposition and rapid thermal annealing generally occurred on a single substrate using a single dopant precursor molecule. However, reproducible device fabrication requires a combination of the initial MLD approach with an ability to laterally control the positioning of the molecular monolayer.

Signalling the beginning of a break away from traditional MLD, Voorthuijzen and co-workers combined the MLD process with nano-imprint lithography (NIL).[25] This work is depicted schematically in **Figure 1.4** and involves the utilisation of a method developed previously to directly pattern P-containing organic monolayers onto oxide-free silicon; using a combination of bottom-up monolayer formation and top-down nanoimprint lithography resulting in sub 100 nm highly-doped patterned regions.[26]

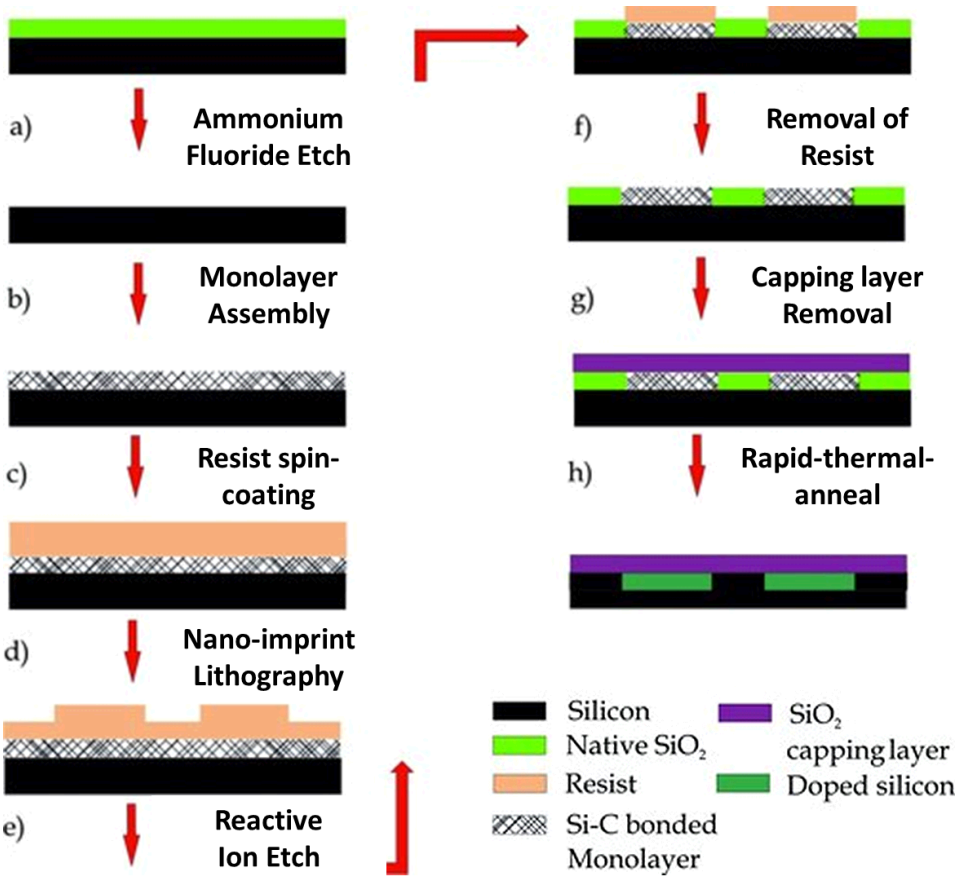


Figure 1.4. Process flow showing the MLD process combined with nano-imprint lithography. (a) Native oxide is removed by ammonium fluoride followed by (b) monolayer formation using dopant-containing monolayer. (c) Spin coating of imprint resist. (d) Etch of residual layer by reactive ion etch. (f) Resist removal by sonication in acetone. (g) Deposition of SiO_2 capping layer by e-beam evaporation. (h) Rapid thermal anneal treatment to cause dopant diffusion.[25] Modified from ref: 25 Copyright 2011, John Wiley and Sons.

TOF-SIMS was used to ascertain dopant concentrations and also to image and depth-profile the highly-doped regions. The dopant surface dose on a doped section approached 2.3×10^{19} atoms/cm^3 which corresponded to an areal dose of approximately 5.6×10^{13} atoms/cm^2. Clear differences were observed in the resistances of the doped regions when the current was measured perpendicular to the regions and when measured parallel. Sheet resistance measurements were obtained using a four-point-probe. The sheet resistance for an unpatterned sample (R_s) was found to be $7.6 \times 10^2\ \Omega$ whereas a value of $1.5 \times 10^3\ \Omega$ was obtained for a patterned sample. Doping efficiencies were extracted to be 26 % for a doped line and 50 % on a full unpatterned sample.

This variation of the MLD process proves that, in principle at least, the positioning of the dopants can be laterally controlled which is important on smaller scale devices such as diodes, nanowires and FinFETs.

Hazut *et al.* introduced another variation of the MLD process termed monolayer contact doping (MLCD).[27] **Figure 1.5** shows a schematic representing the MLCD process.

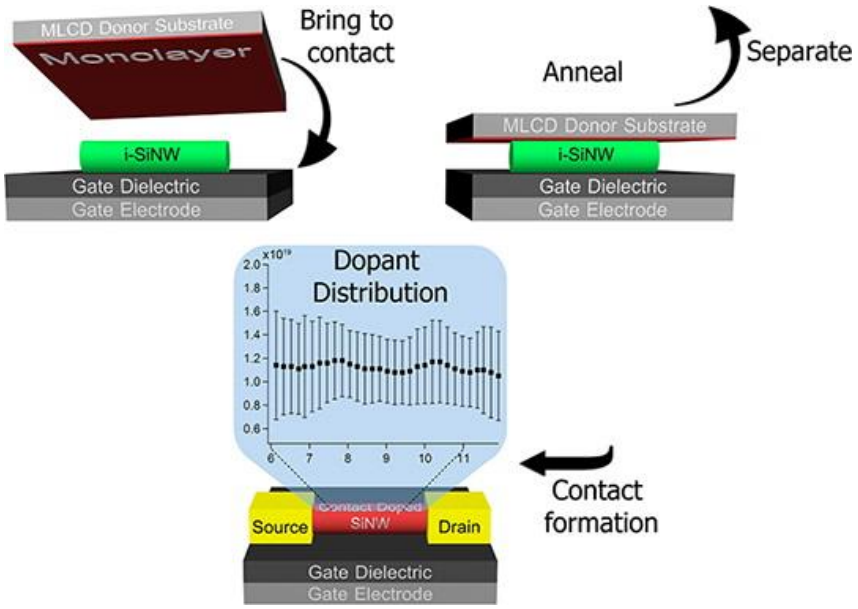


Figure 1.5. Schematic representation of the MLCD process. A dopant containing monolayer on a donor substrate is brought into contact with the substrate that is intended for doping and the two samples are annealed together. Undoped Si NWs may be sandwiched between the donor and acceptor substrates for controllable doping.[27] Adapted with permission from ref: 27 Copyright 2012, American Chemical Society.

The work reported by Hazut *et al.*[27] involved the characteristic formation of the dopant-containing monolayer, not directly on the material, but on a "donor" substrate which was then brought into contact with an "acceptor" substrate that was intended for doping and both substrates were annealed together. The MLCD process utilised, in comparison to the traditional MLD process, did not require the deposition and

removal of a SiO_2 capping layer, but instead using more complex phosphine-oxide based molecules (diphenylphosphine oxide (DPPO), triphenylphosphine oxide (TPPO) and tetraethylmethylene diphosphonate (TEMEP) in conjunction with optimised RTA recipes. This lends advantages to the MLCD process such as fewer process steps, removal of any potential sources of damage which may be caused to the monolayer by the capping layer deposition process and makes the roughness-increasing oxide removal step unnecessary. By using SiO_2 – phosphine oxide chemistry at the native oxide surface of the donor substrate[28], no molecular linker is required which may inadvertently affect diffusion of the dopant atoms during the rapid-thermal-anneal process. The concentration as a function of anneal time was studied initially on blanket Si samples using a constant temperature of 1005 °C for the rapid thermal anneal for each precursor molecule. Four-point-probe measurements were utilised to obtain sheet resistance (R_s) values post-RTA. As expected, R_s values decreased sharply with anneal time on blanket, contact doped samples. Samples with their native oxides and samples with the native oxides removed were tested in tandem. Doping efficiencies for diphenylphosphine oxide were estimated to be 55 and 7 % for H-terminated samples and samples with native oxide respectively.

In order to better understand the difference in sheet resistivities between native-oxide passivated samples and the samples functionalised with DPPO and TEMEP , Hazut *et al.* functionalised SiO_2 nanoparticles (NPs) with DPPO and TEMEP in the same study[27] and thermally annealed the NPs at various temperatures. X-ray photoelectron spectroscopy (XPS) and thermo-gravimetric analysis (TGA) analysis were performed on each sample to characterise the monolayer surface chemistry and the monolayer decomposition mechanism. Samples functionalised with DPPO and TEMEP

exhibited similar results both for XPS and TGA analysis with sharp decreases observed in C *1s* and P *2p* signals at elevated anneal temperatures. In contrast the TPPO functionalised NPs showed complete depletion of C and P at anneal temperatures over 400 °C. TGA analysis confirmed similar behaviour with monolayer retention of ~70 % for DPPO, ~40 % for TEMEP and ~0 % for TPPO functionalised NPs. This difference was attributed to the different chemical environments of the P=O group(s). The MLCD process has also been applied to CVD-grown intrinsic Si NWs which were contacted by two terminals with back-gate electrodes. These nanowires were then drop-cast on a p-doped Si/SiO_2 (100 nm)/Si_3N_4 (200 nm) substrate and contact-doped using the MLCD process using the TEMEP molecule. Immediately prior to the MLCD process application, the pre-doped nanowires exhibited resistances approaching 20 GΩ at 2 V. The MLCD-doped NW devices exhibited a decrease in resistance around 6 orders of magnitude with a 20 kΩ resistance observed at 2 V. To ascertain the longitudinal dopant distribution of the fabricated devices, Kelvin probe force microscopy (KPFM) was used on the Si NW devices with a 10 μm channel length between the source and drain electrodes. Intrinsic Si NWs (80 nm) were doped using the MLCD process with the TEMEP molecule at 900 °C. The KPFM results demonstrated high dopant uniformity along the length of the nanowires compared to traditional *in-situ* methods of nanowire doping.

The MLCD method was expanded upon again by Hazut, to transform undoped silicon nanowires into p-type/n-type parallel p-n junction configured nanowires using a one-step MLCD process, represented schematically in **Figure 1.6**.[29] Firstly, two separate Si substrates were functionalised; one functionalised with a P-containing molecule and another substrate functionalised with a B-containing molecule. The B-functionalised

substrate also contained intrinsic Si NWs previously grown *via* CVD. Thus, the Si NWs were sandwiched between an n-type and p-type substrate and were annealed together in a rapid-thermal anneal furnace under vacuum which resulted in the controlled decomposition of the dopant-containing monolayers of each substrate and dopant diffusion into the NWs.

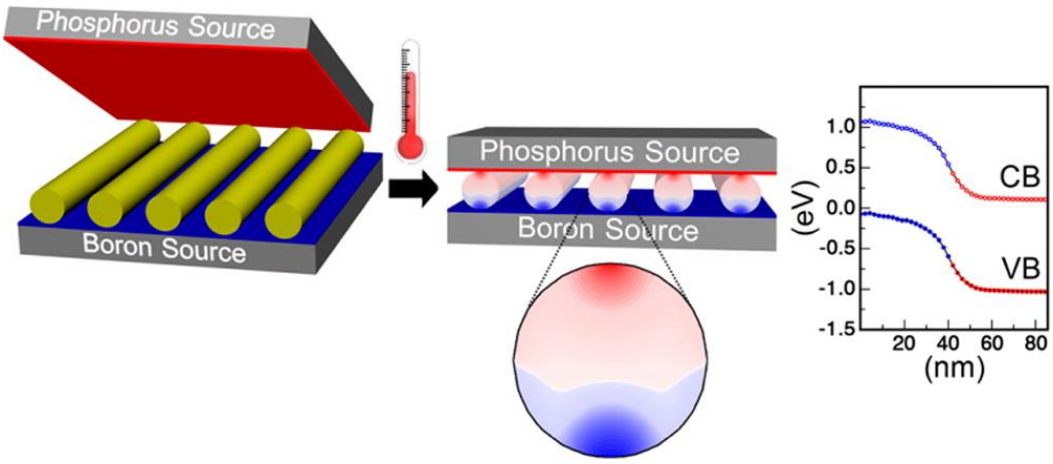


Figure 1.6. Schematic representation of p-n junction formation using the one-step MLCD process. Firstly, undoped Si NWs are transferred to a substrate that has been functionalised with a B-containing monolayer. A second substrate functionalised with a P-containing monolayer is then brought into contact with the NWs and annealed together to yield p- and n-doped Si NWs.[29] Adapted with permission from ref: 29 Copyright 2014, American Chemical Society.

This MLCD approach shown in **Figure 1.6** yielded nanostructures which were both p- and n-doped. The junctions were then studied using a combination of scanning tunnelling microscopy (STM) and scanning tunnelling spectroscopy to determine the spatial electronic properties of the junctions. The junction configuration was also characterised using off-axis electron holography to provide additional information about the junction formation. STM analysis of the Si substrates doped with B and P

showed p- and n-type electronic characteristics respectively. The spatial distribution of the dopants in the nanowires also conformed to expectations, with the highest dopant concentrations at the top and bottom of the nanowires at the point of contact with the donor substrates. At these points on the nanowires, peak P concentrations were approximately 2.6×10^{19} atoms/cm^3 with highest B concentrations approaching 2.0×10^{20} atoms/cm$^{3.}$

More recently Longo and co-workers published a paper investigating the grafting of alkylphosphonic acids on Si by infrared spectroscopy and by using density functional theory calculations for MLD of Si.[30] Again, a comparison to traditional MLD approaches was made where a dopant molecule is attached to the Si-H surface by hydrosilylation. Longo *et al.* studied an alternative approach based on work involving the grafting of OH-containing compounds by Michalak.[31–33] The initial process was based on a methodology to covalently bond an alcohol to a Si-H surface and was extended to phosphonic acids. This study differed by attempting to reduce the amount of potentially deleterious carbon in the process which may be a problem with current carbon-based precursors. Here, the molecules attach to the Si via a Si-O-X linker where X can be P, As, B and other dopant atoms. Simple forms of the acids can be used, *e.g.* monohydride phosphonate in the work of Longo, to reduce carbon contamination. In addition, P-containing moieties with long alkyl chains such as octadecylphosphonic acid (ODPA) contain a "weak link" at the X-C bond, where X is the dopant molecule (P-C in the case of ODPA) with removal of the carbon ligand typically at temperatures approaching 500 °C. This negates the need for the oxide cap that is typical of MLD processes. While the study focused purely on the pre-anneal steps of surface preparation and functionalisation with no electrical studies done on

annealed blanket samples or nanostructured samples, the highly-optimised surface chemistry investigated could prove useful in future MLD studies.

There is still much to understand regarding the diffusion of dopants from an organic self-assembled monolayer especially regarding chemical information so close to the surface where the SIMS resolution limit and organic contaminants present in UHV chambers becomes an issue. Shimizu and co-workers studied the behaviour of phosphorus and contaminants from the MLD method used in conjunction with a conventional spike anneal.[34] Time-of-flight secondary ion mass spectrometry (TOF-SIMS) does not provide useful information within the first 5 nm of a sample again highlighting the need for metrology improvements. By using laser-assisted atom probe tomography (APT), a 3D distribution of the diffused dopant atoms was created to determine the dopant distributions in device structures. By combining the APT technique with a low-energy Si beam deposition step, termed focused ion beam direct deposition (FIBDD), a promising technique to obtain accurate near-surface quantitative dopant information was realised. To investigate ultra-shallow doping using this technique, a Si sample was functionalised with diethyl diphosphonate (DPP) and annealed at 800, 875, 950 and 1025 °C for 5 s in order to achieve different concentrations and differing depths. For anneals at 800 and 875 °C, no significant diffusion of P from the monolayer into the Si surface was observed which is in contrast to the higher annealing temperatures where diffusion of P is observed. SIMS showed that at temperatures of 950 and 1025 °C, all samples exhibited an intense P signal just 2 nm beneath the surface. This was attributed to the pre-equilibrium erosion regime during which the sputtering and ionisation probabilities change constantly. Due to this variation, the P concentration as measured by TOF-SIMS is difficult to interpret

quantitatively. The same sample was analysed using the APT technique. **Figure 1.7** compares SIMS measurements against APT measurements. The results of the two techniques are quite similar with the peak concentration of P obtained by the APT technique observed at slightly lower than the solubility limit of P in intrinsic Si. The APT technique also allowed contaminants (C and O) to be studied. C and O were limited to the first few monolayers with no difference in diffusivity between 800 and 1025 °C. This could be attributed to the Si-C bond formation during the hydrosilylation reaction.

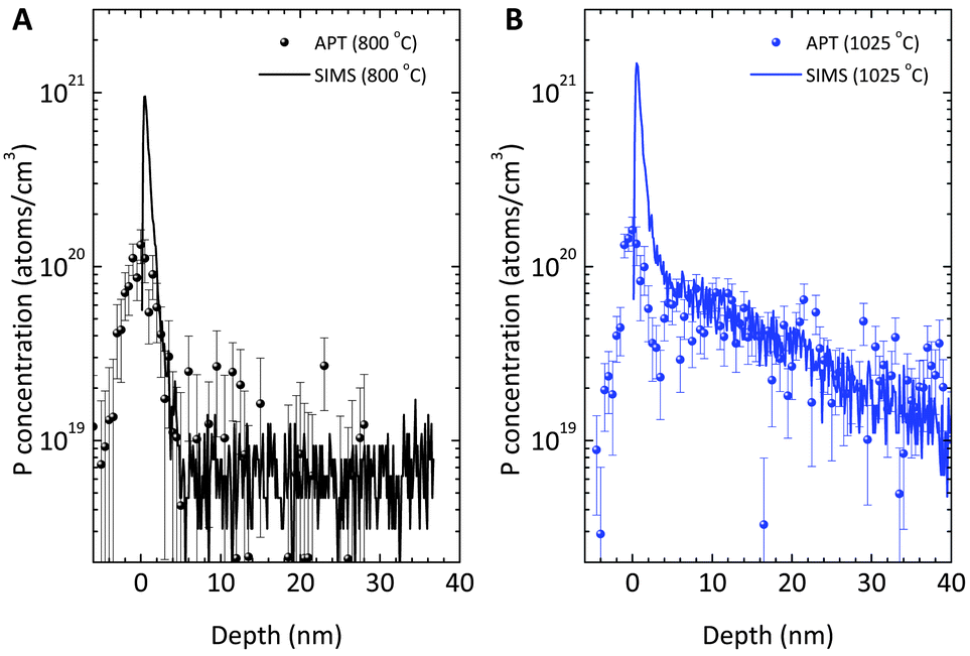


Figure 1.7. (a) Phosphorus concentration depth profiles obtained by the APT technique and (b) TOF-SIMS analysis from the two samples annealed at 800 and 1025 °C. Good agreement between the two techniques is observed over the range of validity for the TOF-SIMS measurements with the APT technique providing a more accurate measurement in the transient region of TOF-SIMS (< 3 nm).[34] Reproduced from ref: 34 with permission from The Royal Society of Chemistry.

While the vast majority of MLD literature to date has focussed primarily on applications for the semiconductor and microelectronics industry, there have been a number of interesting studies performed on photovoltaic (PV) materials for solar sell and energy purposes. Notably, Puglisi and co-workers recently published a study where MLD-doped Si NWs integrated into complete solar cells exhibited higher short circuit currents and fill factors than planar reference cells.[35] CVD-grown *i*-Si NWs were immersed in a gold-cleaning solution to remove traces of the NW growth catalyst. Following a quick HF dip to remove surface oxides and provide the required H-termination, the NWs were immersed in a solution of diethyl 1-propylphosphonate (DEPP) and mesitylene (25%, v/v) at 160 °C for 2.5 h. The nanowires had a mean length of 500 nm and a diameter range between 2.5 and 70 nm. A 1 nm thick oxide layer coating was observed on the nanowires by transmission electron microscopy (TEM). Spreading resistance profiling measurements showed a peak carrier concentration of 1.0×10^{19} atoms/cm^3 in the growth substrate with a junction depth of approximately 120 nm. The improved photovoltaic properties were attributed to two aspects. The MLD-doped NWs allowed a large increase in the photogeneration efficiency due to the reflectivity factor being 2-3 times larger than the equivalent planar diode. Additionally, the absorption factor approaches the ideal value of 1 due to the light trapping effect. In contrast, absorption factor values of 0.1-0.5 were achieved for planar diodes. Puglisi *et al.* noted that the improvement in the light trapping alone could not account for the difference between the NW sample and the planar diode and postulated that the sheet resistance between the top silver contact and the emitter was significantly reduced due to the better conformal doping achievable on the nanostructured surface using the MLD technique. An in-depth study of the

MLD process with regard to solar cell applications is outside the scope of this chapter, and the reader is directed to excellent reviews by Caccamo [36] and Elbersen. [37]

Ye and co-workers further fine-tuned the MLD process through use of mixed-monolayers.[38] Although Ho[18] initially reported two mixing ratios, a more in depth study was required to investigate the effect of mixed monolayers on the MLD process. By mixing dopant-containing alkenes with structurally analogous alkenes that do not contain a dopant, varying ratios of the dopant-containing molecule were grafted onto Si-H surfaces. **Figure 1.8** shows a schematic detailing the sample preparation process for the mixed monolayer doping strategy. XPS and contact angle analysis were used to characterise the functionalised surfaces. A roughly linear relationship existed between the fraction of the dopant molecule on the surface and the amount of dopant-molecule present in the initial liquid mix.

Following surface analysis, the samples were capped with 50 nm of SiO_2 and subjected to a high temperature anneal at 1000 °C for 5 min. SIMS was used to investigate the incorporation of the dopant molecules into the Si substrates. Surface concentrations of approximately 1.6×10^{19} atoms/cm^3 were observed for B-MLD when using the undiluted molecule, with a junction depth of 125 nm. Surface concentrations of 4.2×10^{18} atoms/cm^3 were achieved for B-MLD with the most diluted dopant-alkene mix with a junction depth of 50 nm. A similar trend was observed for the P-MLD process with surface concentration values of 2.4×10^{19} atoms/cm^3 achieved with a junction depth of 125 nm for the pure undiluted molecule, with the most diluted dopant-alkene mix giving a concentration of 2.2×10^{18} atoms/cm^3 with a junction depth of about 50 nm. The study showed that using mixed monolayers is an important feature for

controlling the MLD technique and will potentially enhance the usability of the approach in the formation and fabrication of functional nanoscale devices.

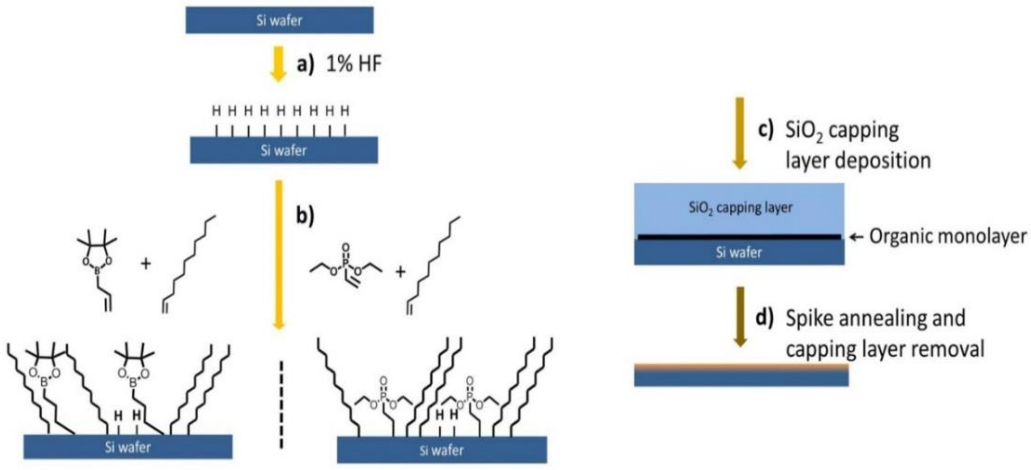


Figure 1.8. Process flow diagram for mixed monolayer doping. (a) Etching of the native oxide with HF removes the oxide and H-terminates the Si surface, (b) hydrosilylation attached dopant and dilution molecules onto the H-terminated Si surface, (c) capping of monolayer with SiO_2 and (d) rapid-thermal-anneal and capping layer removal results in shallowly doped surface [38] Adapted with permission from ref: 38 Copyright 2015, American Chemical Society.

Until very recently only B- and P-containing molecules had been used in MLD studies. Limiting the anneal time to less than 5 s using advanced annealing techniques aids in the formation of sub-10 nm junctions in Si for dopants with fast diffusion rates, such as B and P. Despite the negligible electrical activity of N in Si[39,40], an alternative method was utilised by Guan and co-workers where N, a dopant with a low thermal diffusion coefficient, was introduced onto the Si surface using a standard hydrosilylation reaction.[41] All samples were then capped and then annealed at 1050

°C for 2 min. Nitrogen doping by the use of self-assembled monolayers can potentially form ultra-shallow junctions in Si. For a sample functionalised with an N-containing molecule only, N concentrations were observed as dropping from 4×10^{19} atoms/cm^3 near the surface to approximately 1×10^{17} atoms/cm^3 at 100 nm deep. A similar trend was observed for a sample functionalised with a molecule containing both P and N with N remaining in the top 100 nm and P diffusing to 200 nm below the interface. The activation rates and diffusion coefficient of the N were found to be consistent with literature values. While an interesting application of surface functionalisation, the MLD of Si with N is unlikely to satisfy the need for the high dopant concentration and abrupt junction formation required for future device technologies due to the almost electrically-inactive nature of N in Si.

Mathey and co-workers recently functionalised Si NPs and native Si oxide with tailored boron molecular precursors in order to predictively and efficiently dope Si.[42] The method applied minimises carbon contamination while avoiding the use of hydrofluoric acid due to no requirement for a capping layer. B-containing molecules were custom synthesised to react with silanol groups on the substrate surface at one end and a large, bulky backbone to act as a capping layer on the other end. This approach has been used for oxide functionalisation and catalysis purposes but has not been applied to semiconductor materials for dopant incorporation. Similarly to the work of Hazut[27] , silica NPs were used in this research as a model to aid characterisation of the surfaces. The bulk and NP surfaces were functionalised with the B-containing molecule in dichloromethane and in toluene. The samples were subjected to a rapid thermal treatment in low pressure nitrogen and heated to 985 °C from 300 °C at a rate of 10 °C s^{-1}. **Figure 1.9** shows SIMS data extracted for those

samples showing peak concentrations exceeding 1×10^{21} atoms/cm^3 for samples functionalised in toluene and concentrations of approximately 1×10^{20} atoms/cm^3 for samples similarly functionalised in dichloromethane.

The use of boron molecular precursors that combine both the dopant molecule and a bulky backbone to act as a capping layer, in addition to containing a moiety with anchoring ability on the surface of non-deglazed Si wafers is beneficial to incorporate controlled doses of boron without potential deleterious carbon contamination. This interesting approach to surface functionalisation allows for a molecular level understanding of the surface species using silica NPs as model surfaces. This approach could well prove to be beneficial for advanced CMOS manufacturing processes where few-step process are desired.

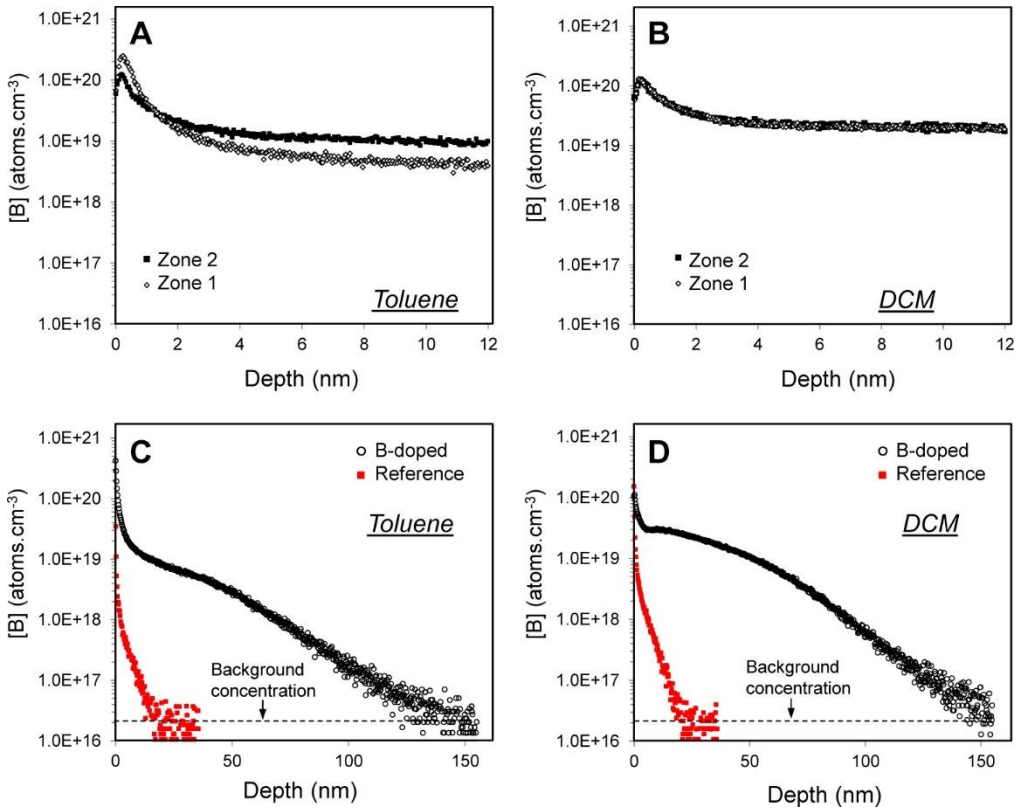


Figure 1.9. Magnetic SIMS depth profiles of boron treated wafers functionalised in toluene (a) and (c) and those grafted in dichloromethane (b) and (d). The profiles shown in (a) and (b) show data obtained over the first 12 nm of the depth for two different areas at a low ion impact energy of 250 eV. Shown in (c) and (d) are profiles containing concentration vs depth data for the control wafer and B-doped wafers.[42] Adapted with permission from ref: 42 Copyright 2015, American Chemical Society.

Semiconductor devices rely on the ability to form two types of electrically-conducting layers: n-type and p-type. An electrically active dopant atom contributes a free carrier to the conduction band or valence band by creating an energy level that is very close to either band. An ideal dopant atom should therefore have a shallow donor/acceptor level and a high solubility. Arsenic and phosphorus are considered to be the most suitable n-dopants based on their high solubilities in Si[43] and also due to their

ionisation energies.[44] For continued fabrication of devices with complex and non-planar 3D geometries which require abrupt, conformal and shallow doping profiles, it is desirable that the diffusion rate of the dopant is small. Arsenic has a much smaller diffusion coefficient when compared to P, making it the ideal dopant for heavy and shallow n-type doping of silicon.[45] O'Connell *et al.* recently published the first application of As-MLD on planar Si and a number of Si nanowire devices.[46] **Figure 1.10** shows the general scheme applied in their study.

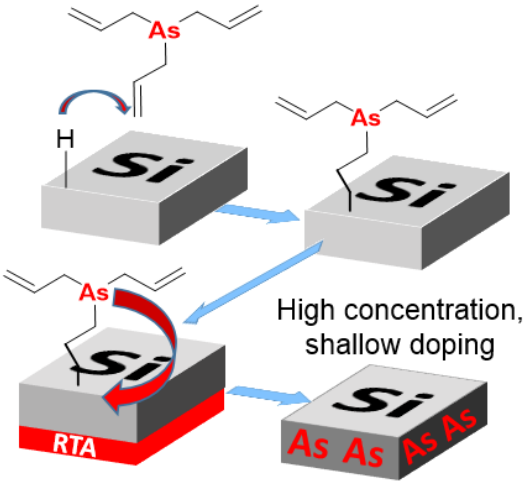


Figure 1.10. Schematic representing the As-MLD process on Si. A hydrosilylation reaction occurs between a reactive H-passivated Si surface and the labile C═C site on the custom-synthesised dopant containing molecule, monolayer formation. The samples are then capped and subjected to a rapid-thermal-anneal (RTA) step resulting in high concentration, shallow doping of silicon.[46]. Adapted with permission from ref: 46 Copyright 2015, American Chemical Society

The functionalised samples were then capped and annealed at various temperatures for a constant time of 5 s. The planar substrates were analysed using XPS and SIMS with the NW samples analysed using four-point-probe measurements, SEM and TEM.

Figure 1.11 shows SIMS-derived chemical concentrations for three planar substrate samples analysed at 950, 1000 and 1050 ^{o}C respectively showing an increase in concentration in line with increasing anneal temperatures. Peak concentrations approached 2×10^{20} atoms/cm^3 for a sample annealed at 1050 ^{o}C.

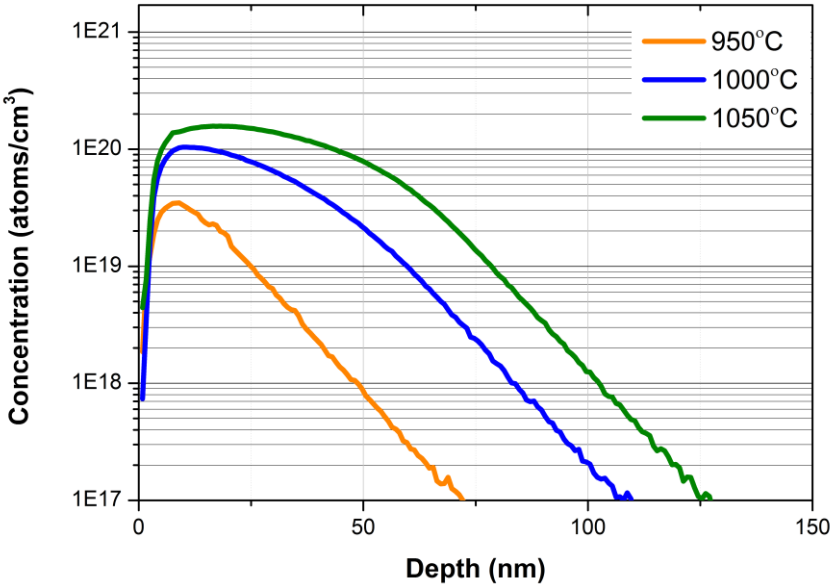


Figure 1.11. Secondary ion mass spectrometry profiles of three samples processed at varying temperatures for 5 s. The carrier depths were observed to be extremely shallow with peak concentrations achieved at less than 25 nm. The dopant concentration increased with an increase in rapid-thermal-anneal temperature. Junction depths ranged from 75 nm at 950 ^{o}C to 125 nm at 1050 ^{o}C.[46] Adapted with permission from ref: 46 Copyright 2015, American Chemical Society.

Diffusivity data obtained from the SIMS and electrochemical capacitance-voltage (ECV) analysis showed that extrinsic diffusivity regimes were observed. Electrical performance was evaluated on a number of nanowire devices ranging from 1000 to 20 nm in width. As most current device dimensions are currently < 40 nm, a model where

current was assumed to flow uniformly through the entire cross-section of the nanostructure, like that of a metal track, was used to evaluate the device performance. This model is applicable to nanostructures with sub-40 nm dimensions such as FinFETs and remains applicable as the device feature size continues to scale down due to the probability of having a uniformly doped cross-section being higher. **Figure 1.12(a)** shows nanowire resistivity data with **Figure 1.12(b)** showing a HRTEM image highlighting the lack of visible extended defects in the NW. As can be seen from the resistivity data shown in Figure 1.12(a), there is a significant difference in the resistivity between the pre-MLD wires and the post-MLD wires. Much lower resistivities were observed for the nanowires with dimensions lower than 40 nm, with a resistivity reduction of 5 orders of magnitude measured nanowires with a width > 100 nm and a reduction of 7 orders of magnitude observed for the nanowires with a width < 100 nm. This data highlights the efficacy of the MLD technique on small, 3D devices. The HRTEM image shown in Figure 1.12(b) shows no indications of any visible extended defects after the doping process, whilst the Fast Fourier Transformation (FFT) inset shows the highly crystalline nature of the nanostructure has been maintained. In the past, {111} twin boundary defects and stacking faults have been the most commonly encountered problems during ion implantation doping of NW structures where crystal damage is very easily visible.

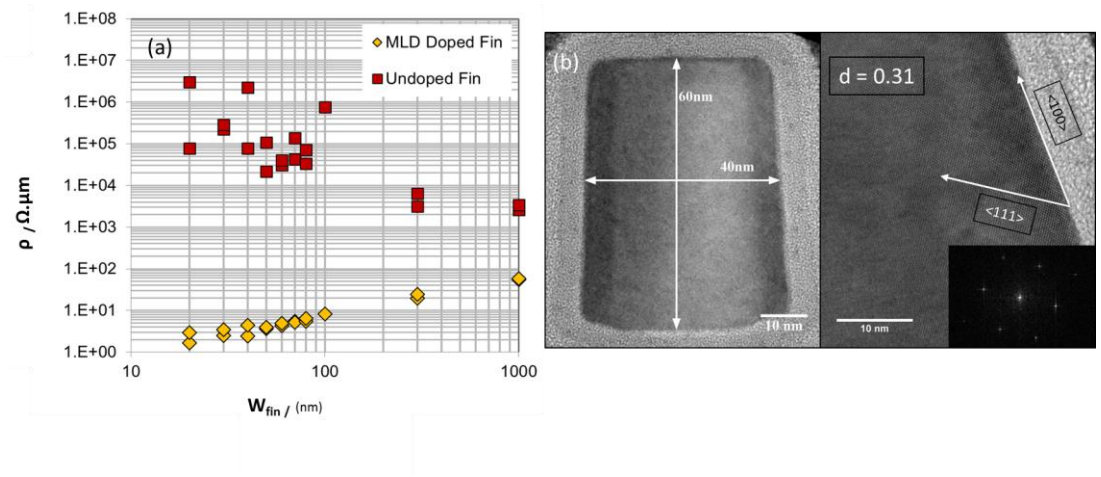


Figure 1.12. (a) Resistivity of NWs as a function of width for pre-MLD and post-MLD wires. The best results were observed for nanowires < 40 nm in width, showing that the MLD strategy employed works extremely well for small feature sizes. (b) TEM image of a section of the 40 nm Si nanowire test device, (b) magnified HRTEM micrograph of the nanowire with the ⟨111⟩ and ⟨100⟩ directions indicated. (b, inset) FFT showing the highly crystalline nature of the nanowire. There are no indications on either micrograph of any defects or damage to the crystal lattice.[46] Adapted with permission from ref: 46 Copyright 2015, American Chemical Society.

These developments in MLD on Si so far have focused on molecules which contain only one dopant atom. Using molecules containing more than one dopant atom should yield a higher concentration when compared to a structurally analogous molecule containing only one dopant atom.

More recently, Ye *et al.* published a study on B-MLD of Si, where they used several carborane molecules containing 8-10 times more B than the frequently used allylboronic acid pinacol ester.[47] Once again utilising the hydrosilylation reaction to functionalise the Si surface, samples were annealed at temperatures between 950 and

1050 °C and characterised using XPS, SIMS and four-point-probe using the van der Pauw method. The XP spectra shown in **Figure 1.13(a)** displays the B *1s* signal intensity for the different bonding configurations for each molecule tested. The SIMS profiles shown in **Figure 1.13(b)** show peak concentrations near the surface approaching 1×10^{20} atoms/cm^3, with junction depths of 40 and 60 nm reported for the differing annealing temperatures. XPS measurements indicated approximately 10 times more boron present on the carborane-modified Si surface when compared to the monolayer composed solely of the ABAPE functionalised samples. SIMS and sheet resistance measurements also confirmed the increase in the dopant dose under the same annealing conditions.

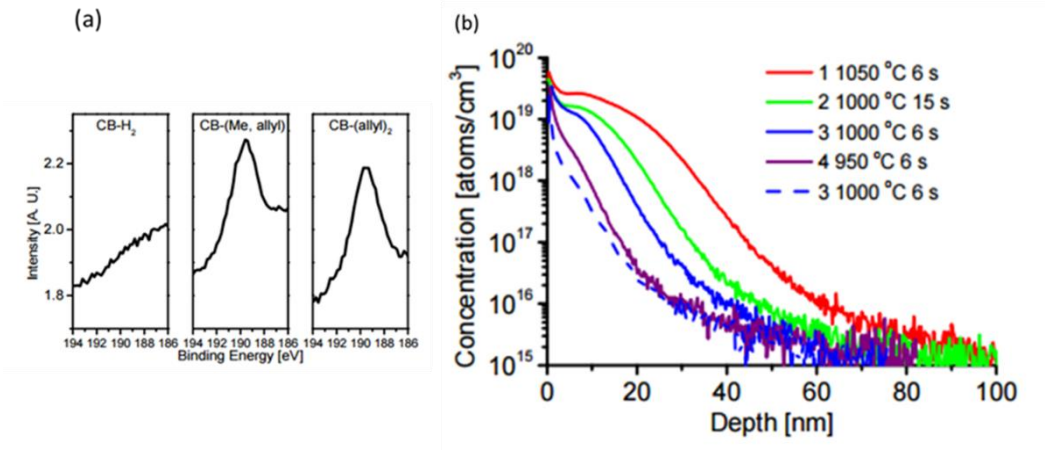


Figure 1.13. (a) XPS B *1s* spectra showing the presence of large intensity signal on substrates treated with three boron-containing carborane derivatives. (b) SIMS profiles for samples doped by MLD using (CB-Me, allyl) (solid line) and ABAPE (dashed line) for varying times and temperatures. Peak concentrations near the surface approached 1×10^{20} atoms/cm^3 with junction depths of 40 nm reported for lower anneal temperatures and approaching 60 nm for higher annealing temperatures. Error in concentrations did not exceed 10 %. [47] Adapted with permission from ref: 47 Copyright 2015, American Chemical Society.

Most recently, O'Connell *et al.* reported the application of a two-step MLD process using azide-alkyne cycloaddition reactions.[48] The hydrosilylation reaction has featured throughout the vast majority of MLD processes as the main method for attaching dopant containing molecules to the Si surface. Molecules suitable for this approach typically contain both the dopant atom and the labile C=C site in the same molecule. Often, these molecules are air-sensitive and difficult to purify, in addition to being unstable at the required hydrosilylation temperatures. O'Connell and co-workers employed a two-step process where a dialkyne was initially grafted onto a Si surface. The resulting tightly packed monolayer of linear alkynes offered excellent protection of the Si surface while providing a reactive "handle" to which dopant-containing azides could be attached *via* Huisgen 1,3-dipolar cycloaddition reactions. This approach greatly suppresses the effect of ambient conditions on the Si surface. Additionally the dopant-containing azides were resilient towards attack from atmospheric water and oxygen, allowing for a very robust functionalisation procedure. Si substrates were functionalised with 1,7 octadiyne and then further functionalised with the dopant-containing azides according to the scheme shown in **Figure 1.14**

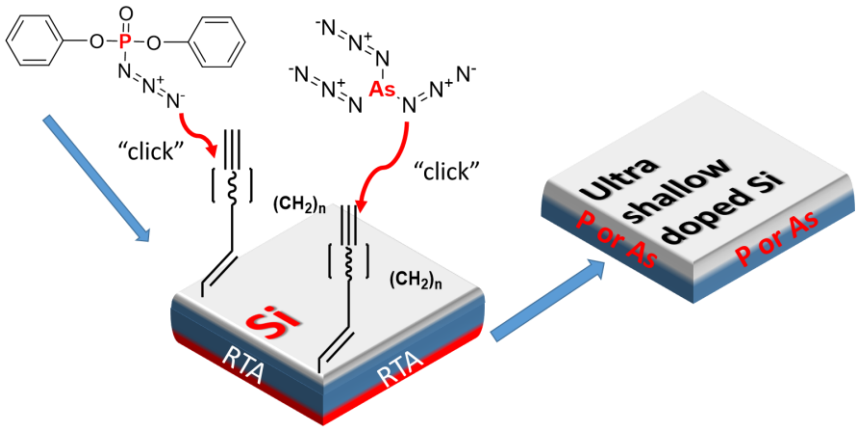


Figure 1.14. Si was functionalised with dialkynes of varying length between 7 and 10 carbons. The terminal alkyne groups were then reacted with P- and As-containing azides *via* an alkyne-azide cycloaddition reaction to form dopant-containing monolayers on the Si surface. These substrates were then capped and annealed to form ultra-shallow doped Si. [48] Adapted with permission from ref: 48 Copyright 2016, American Chemical Society.

Samples were annealed at 1050 ºC for 5 s to diffuse the attached dopants into the Si. To compare the oxidation resistance and dopant profiles to a traditional P-MLD process, a sample of Si was functionalised with allyl diphenyl phosphine using a one-step hydrosilylation process. Both samples exhibited similar dopant profiles with peak concentrations approaching 1×10^{19} atoms/cm^3 with junction depths of approximately 25 nm. The stability of the P-functionalised samples were monitored via XPS. The two-step click chemistry approach offered superior resistance to oxidation, especially in the first 24 h whereas the sample functionalised using a one-step hydrosilylation showed the presence of oxide after 24 h. This stability might prove advantageous for potential integration into future device fabrication process to prevent oxidation of the Si surface between processing steps.

1.3.2 Monolayer doping on Ge

While Si has been the material of choice in the semiconductor and microelectronics industry for many decades, germanium (Ge) has been put forward as a viable alternative for future CMOS processes. Ge, as a Group 14 element, shares several properties with Si such as a diamond cubic crystal structure. Additionally, Ge also exhibits superior properties to those of Si, such as a higher charge carrier mobility. The question remains whether or not scaled Ge FETs can outperform the equivalent Si FET device. Experimentally, the answer may be unclear for now but Eneman *et al.* performed interesting analysis comparing Ge with Si FinFETs in the presence of strain.[49] They concluded that relaxed Ge p-FinFETs cannot outperform strained Si, but needed a mobility boost to do so, possibly through embedded stressors. For Ge n-FinFETs, relaxed channels already outperform strained Si primarily due to favourable fin sidewall mobility. Adding stressors will increase that benefit to more than double the Si performance, in terms of mobility. In addition to the performance differences between such devices, Ge displays more complex oxidation chemistry at its surface. Ge forms oxides in the 2+ (GeO) and the water soluble 4+ (GeO_2) oxidation state. This oxide instability makes surface treatment and passivation strategies and hence, monolayer doping on Ge, much more challenging than analogous chemistry on Si. For example, hydrogermylation, the Ge analogue of the ubiquitous hydrosilylation performed on Si, requires much higher temperatures which will reduce the number of molecules available for surface functionalisation. Additionally oxide removal steps using HF tend to roughen Ge surfaces more than the same process on Si. Ge also has a lower melting point than Si which limits thermal budgets for dopant activation and diffusion processes.[15] Nanoscale doping has been carried out on Ge by other means such ion beam irradiation[50] but monolayer doping has not been as prevalent on Ge as

it has on Si, purely due to the challenging surface chemistry and CMOS processing limitations. Nevertheless, Long *et al.* recently published a study on As-MLD of Ge.[51] The molecule previously utilised by O'Connell and co-workers[46] was used but was dissolved in IPA as opposed to mesitylene. As the hydrogermylation temperature of 200 ^{o}C greatly exceeds the decomposition temperature of the TAA molecule, UV-initiated hydrogermylation was used. The sample was illuminated with a 254 nm UV pen lamp for 3 h. The sample was then rinsed to remove physisorbed species, capped and annealed. Due to the lower melting point of Ge, the thermal budget for the rapid thermal anneal treatments needs to be accordingly adjusted. The anneal temperature was held at 650 ^{o}C with the anneal time varied between 1, 10 and 100 s. **Figure 1.15** shows the active carrier concentration vs depth as extracted from ECV measurements. The peak active carrier concentration approached 6×10^{18} atoms/cm^3 with a maximum junction depth of just under 100 nm. The peak concentration did not change with the differing thermal budgets, showing that the As-MLD process on Ge is likely limited by the solubility of As in Ge at 650 ^{o}C, again highlighting the need to explore more advanced annealing techniques. Inset shows roughness measurements as obtained by atomic force microscopy (AFM).

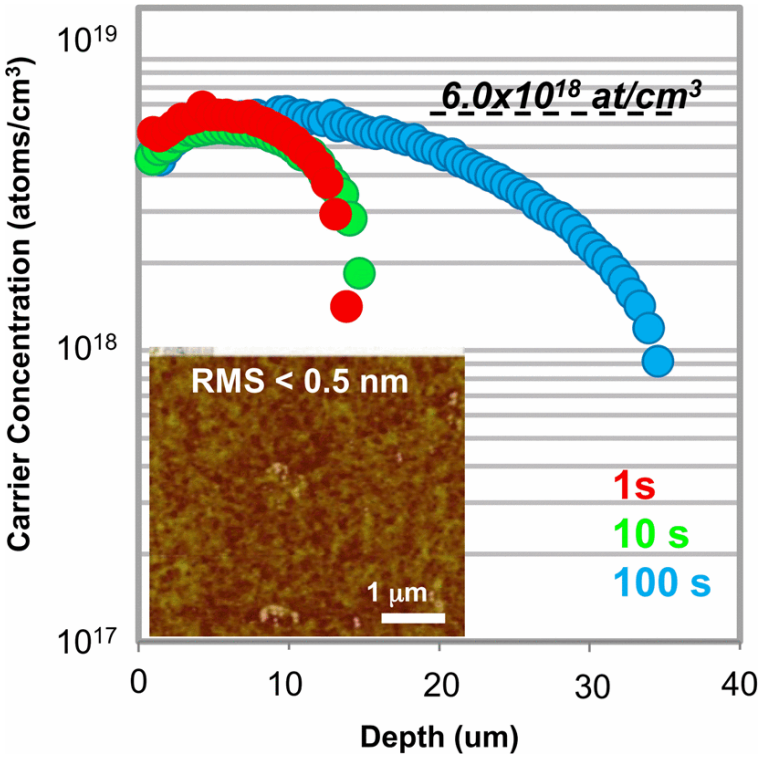


Figure 1.15. Active carrier concentration vs depth extracted by electrochemical capacitance-voltage profiling of As-doped Ge. The peak active carrier concentration approaches 6×10^{18} atoms/cm^3 with inset showing an AFM image of the Ge substrate after the MLD process.[51] Adapted with permission from ref: 51 Copyright 2014, IEEE.

Duffy and co-workers built on the work carried out by Long *et al.*[51] by using an MOVPE-based process to deposit monolayers of P and As on Ge substrates and nanowire devices.[52] **Figure 1.16(a)** shows chemical concentration *vs.* depth profiles as extracted from SIMS analysis on samples with deposited AsH_3. A higher thermal treatment temperature was more effective at incorporating As at the cost of a much deeper junction depth. **Figure 1.16(b)** shows ρ *vs.* W_{fin} profiles where ρ refers to resistivity and W_{fin} refers to the nanowire width, for Ge nanowires doped using AsH_3 and PH_3 at 650 ^oC in the case of AsH_3 and 650 and 700 ^oC in the case of PH_3. The

higher anneal temperature is shown to be more effective for P incorporation. Both As and P dopant species produced similar electrical characteristics in the larger devices while P-doped fins exhibited better electrical characteristics for the smaller-scaled devices. Duffy and co-workers attributed this to As trapping at the Ge surface in the case of smaller devices.

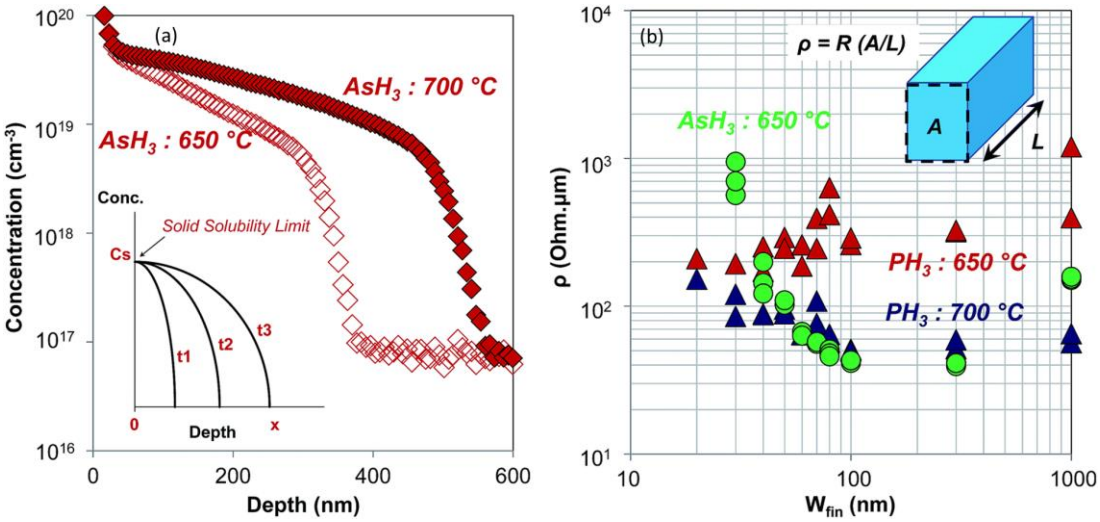


Figure 1.16. **(a)** Chemical concentration *vs.* depth profiles as extracted from SIMS analysis on samples with deposited AsH_3. A higher thermal treatment temperature was more effective at incorporating As at the cost of a much deeper junction depth. (b) showing ρ *vs.* W_{fin} for Ge nanowires doped using AsH_3 and PH_3 at 650 °C in the case of AsH_3 and 650 and 700 °C in the case of PH_3. A higher temperature is shown to be more effective for P incorporation with both P and As species producing similar results in the larger devices while P-doped fins exhibited better electrical characteristics for the smaller-scaled devices.[52] Reproduced from ref: 52 with permission from The Royal Society of Chemistry.

While MLD is in its infancy with respect to its applications on Ge, other methods of achieving ultra-shallow and abrupt junctions such as δ-doping are promising.[53–58]

1.3.3 Monolayer doping on InGaAs

With the exponential rise in handheld computing, there is a need for the design of new device architectures that provide for reduced power consumption in addition to retaining the compatibility with accelerated scaling of device dimensions. III-V semiconductors such as InGaAs have great promise as active channel materials of proposed device geometries that are conducive to aggressive scaling, such as field-effect transistors. However significant improvements in the source and drain resistances are required if InGaAs is to scale beyond the 22 nm technology node. MLD is well suited for this purpose due it to its highly conformal nature, ability to provide ultra-shallow junctions and lack of damage to the III-V zinc blende lattice structure as shown by Yum *et al.* in the first report of solution-based MLD on InGaAs.[59] Again, similarly to Ge, the surface chemistry of InGaAs is challenging and must be overcome in order to find suitable monolayer doping strategies. In the work by Yum *et al*., ammonium sulphide $(NH_4)_2S$ was used to clean the InGaAs substrates which also resulted in S-termination of the surface. While this study focused more on the effect of differing capping layers on the surface, mean concentrations of S ranged from 5×10^{20} atoms/cm^3 to 1×10^{21} atomscm^3 with average junction depths of 11 nm, depending on the particular capping layer used, were reported. The study showed that S-MLD is sensitive to the capping layer growth temperature and precursor reaction energy at the channel surface, and concluded that a SiN_x/BeO bilayer structure as a capping layer may be a more useful solution to improve the activation efficiency of S-MLD to realise small feature sized III-V devices. Further studies on this S-MLD process were carried out by Kort and co-workers, where Raman spectroscopy was used to probe the electron-phonon coupling in InGaAs epilayers doped using a sulfur-MLD method.[60] The process showed an interesting application of Raman scattering

spectroscopy and may prove promising as a method to probe dopant incorporation within shallow junctions formed using the MLD technique. D'Costa and co-workers utilised infrared spectroscopic ellipsometry to study S-MLD doped InGaAs ultra-shallow junctions.[61] The samples were prepared using the previously mentioned $(NH_4)_2S$ cleaning method. The optical response of the epitaxial layer was described with a Drude-like free carrier response from which the carrier relaxation time and electrical resistivity could be extracted. Extracted doping levels approached 1.7×10^{19} atoms/cm^3 at depths of approximately 3-4 nm.

Kong *et al.* recently reported the first application of Si MLD on InGaAs, applying a disilane and silane treatment and using laser annealing (LA) to form conformal, ultra-shallow and highly n-doped regions.[62] Despite not being a traditional solution-based MLD approach, the fact that an *in-situ* clean may be performed in the vacuum system without exposing the substrate to atmosphere thus potentially ensuring a high-quality oxide free surface for MLD, is advantageous. The introduction of the silanes selectively form conformal monolayers of Si which are then annealed in the LA apparatus. LA can potentially overcome the solid solubility of the Si dopant, in addition to reducing the thermal budget and minimising the dopant diffusion to realise abrupt, ultra-shallow junctions. **Figure 1.17(a)** displays SIMS profiles for samples treated with silane (SiH_4) at 500 ^oC for 120 s and then subsequently laser-annealed at 100, 120 and 140 mJ/cm^2. Diodes were also fabricated from the SiH_4-treated samples with dimensions of $L_{diode} \times L_{diode}$ with L_{diode} ranging from 50 to 150 μm. Ni lift-off was used to form the top contacts with Au used to form an ohmic contact on the back side of the InP substrate. **Figure 1.17(b)** plots the I-V characteristics of the 50 μm diodes showing a large difference of between five and seven orders of magnitude between

forward and reverse currents. **Figure 1.17(c)** displays the diode ideality factor, n , plotted against L_{diode}, showing that the samples annealed at 100 mJ/cm^2 exhibited very low values of n, which may be attributed to the absence of implant damage. Diodes annealed at a fluence of 100 mJ/cm^2 had a low ideality factor that is independent of L_{diode} while those annealed at 120 and 140 mJ/cm^2 had a higher ideality factor due to defects induced by melting at the liquid-solid interface during the LA process. HRTEM was also utilised to show that that the crystallinity of the diodes was not affected by the MLD process.

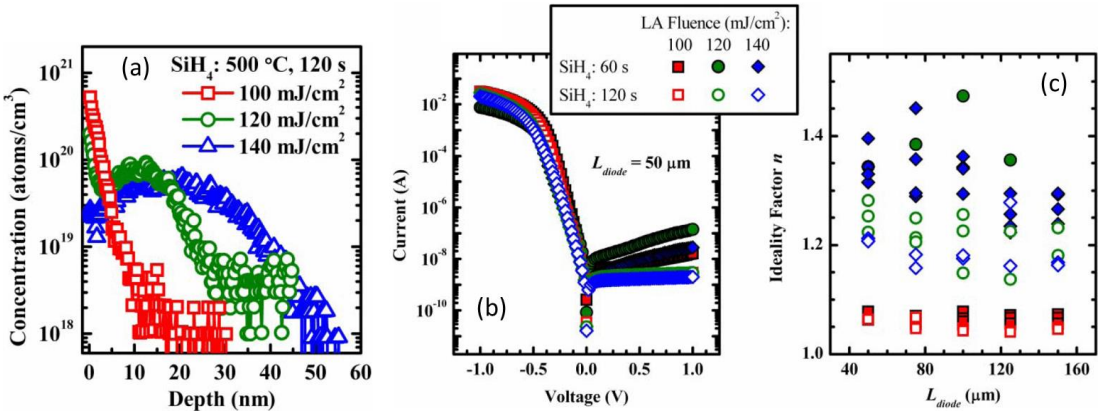


Figure 1.17 (a) SIMS profiles for samples treated with SiH_4 at 500 ^oC for 120 s and laser annealed at 100, 120 and 140 mJ/cm^2. The profiles for fluences of 120 and 140 mJ/cm^2 exhibit a box like profile while the profile for a fluence of 100 mJ/cm^2 has a very high Si concentration of approximately 5. × 10^{20} atoms cm^{-3} at the InGaAs surface. (b) Diode I-V characteristics showing high forward to reverse current ratio of between 5 and 7 orders of magnitude and (c) showing the ideality factor of the diodes plotted against diode size. Diodes annealed at a fluence of 100 mJ/cm^2 had a low ideality factor that is independent of L_{diode} while those annealed at 120 and 140 mJ/cm^2 had a higher ideality factor due to defects induced by melting at the liquid-solid interface during the LA process.[62] Adapted with permission from ref: 62 Copyright 2014, IEEE.

Most recently, Kort and co-workers reported a method of determining the free electron density in sequentially doped InGaAs using Raman spectroscopy.[63] Again, an ammonium sulfide treatment was used to passivate the InGaAs surface with S, and the substrate was then thermally treated and annealed. They showed that the technique, when used to determine the dopant activation and free carrier density is agnostic to the nature of the individual dopants or the manner in which they are incorporated. The relative intensities of the GaAs-like feature and the high frequency coupled mode in the optical phonon region provided a good indication of the surface depletion layer.

1.3.4 Hybrid spin-on doping on Si

Spin on-doping (SOD) is a doping process involving the spin-coating of a dopant-containing solution onto semiconductor substrates, which is followed by a rapid-thermal annealing step during which the dopants diffuse into the substrate. Often, a pre-diffusion annealing step is required to "glassify" the spin-on dopant layer. The dopant-containing solution usually contains either a mixture of SiO_2 and dopant-containing molecule or silicon-containing polymers with dopant atoms already incorporated into the polymer. Spin-on doping is a simple, low-cost, and essentially non-destructive technique, but can suffer from dose control problems in addition to uniformity over large areas and on 3D structures. Additionally, spin-on dopants often leave residual components behind. While pure SiO_2 and silicates are easily removed *via* a wet chemical etch, the presence of residual organics from the solvent during the annealing process results in chemically modified layers that can be quite difficult to remove.

Despite Si being the current material of choice for the semiconductor industry, there have been relatively few reports of spin-on doping on Si in recent years. Hoarfrost and co-workers recently employed spin-on doping on Si substrates using a dopant-containing polymer to demonstrate a hybrid technique that lies between MLD and traditional spin-on doping.[64] Unlike traditional spin-on doping where the dopant-containing layers survive the annealing step, dopant-containing polymer films are easily burned off at the film-air interface. **Figure 1.18(a)** is a schematic showing the approach used in the study by Hoarfrost *et al.* utilising the dopant-containing molecules poly(vinylboronic acid pinacol ester) [PVBAPE] and poly(diethylvinylphosphonate) [PDEVP]. **Figure 1.18(b)** shows sheet resistances of B and P-doped Si using polymeric spin-on dopant films of varying thicknesses. All substrates for the sheet resistance studies were annealed at 1000 °C for 30 s. Peak concentrations for P-doped samples approached 1×10^{21} atoms/cm^3 with average junction depths between 40 – 60 nm. For B-doped samples, peak concentrations reached just over 1×10^{20} atoms/cm^3 with a junction depth of approximately 30 nm for a sample annealed for 10 s and approaching 70 nm for a sample annealed for 60 s.

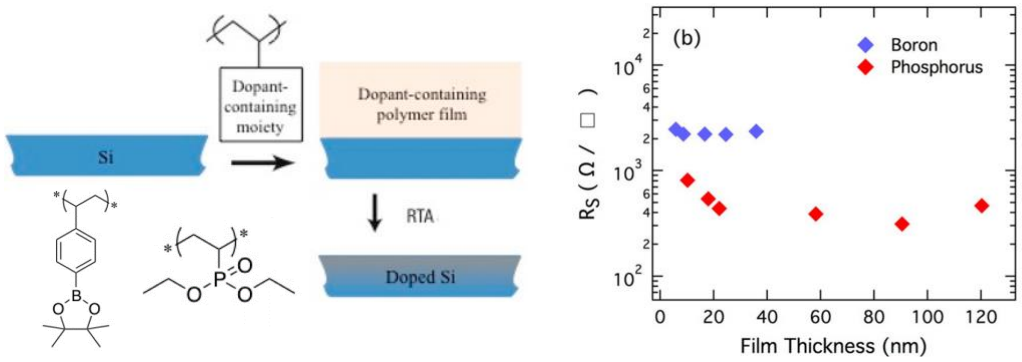


Figure 1.18. (a) Schematic representation of the polymeric spin-on doping process. An organic dopant-containing polymer film is spun onto an oxide-free Si surface from solution and the dopant atoms are diffused into the Si surface using a rapid-thermal-annealing step. The dopant molecules (PVBAPE) and (PDEVP) are shown. (b) Sheet resistance measurements for B- and P-doped Si substrates using polymer films of varying thicknesses.[64] Adapted with permission from ref: 64 Copyright 2013, American Chemical Society.

Sadhu and co-workers used a two-step spin-on process to dope electrolessly etched Si NW arrays.[65] Etching of highly doped Si NWs leads to porous structures with high defect densities. This causes difficulties in forming electrical side-contacts to these NWs. Additionally, integrating such chemically-etched nanowires into high performance devices is non-trivial. While MLD would be suitable for the doping of such structures, the porosity of these structures complicates the surface chemistry. Although dopant depth and concentration can be controlled by anneal temperature and time, Sadhu chose to control the concentration by deposition of various thicknesses of oxide < 25 nm, to act as diffusion barrier layers. Borofilm and Phosphorofilm (Filmtronics©) were used as the spin-on dopants. SIMS was used to verify the concentration and depth profiles with peak B concentrations approaching 2×10^{19}

atoms/cm^3 and lowest concentrations approaching 4×10^{18} atoms/cm^3. P-doped NW arrays exhibited peak dopant concentrations approaching 1×10^{20} atoms/cm^3 without the barrier layer and 6×10^{19} atoms/cm^3 using a barrier layer. **Figure 1.19(a)** shows SIMS profiles for the B-doped NW arrays. Additionally, **Figure 1.19(b)** shows four-point-probe measurements used to obtain *I-V* characteristics and resistances from the doped arrays. Figure 1.19 (c) shows how the *ex-situ* SOD process applied reduces the electrical resistivity of the Si NWs by over three orders of magnitude to between 15-30 mΩ cm and relates the electrical resistance of six nanowire devices with their cross section. The SIMS data obtained for the NW array shows dopant concentrations ranging from 8×10^{18} - 1×10^{19} atoms/cm^3 across the cross section.

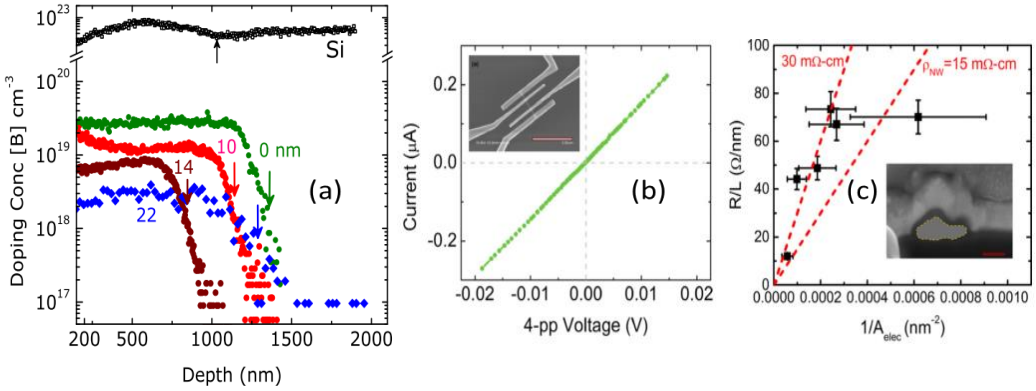


Figure 1.19. (a) SIMS concentration and depth profile data of B-doped Si NW arrays doped using the SOD process with arrows representing length of NW array measured from SEM before analysis. (b) Four-point-probe measurements of single NWs from the doped array. (c) Four point probe resistance values for varied NWs with different diameters taken from an array that was doped to approximately 1×10^{19}atoms/cm^3. Inset shows the focused ion beam (FIB) cross-section of the NW with scale bar indicating 100 nm.[65] Adapted with permission from ref: 65 2008, IOP Publishing.

While hybrid spin-on doping techniques are interesting, monolayer doping may prove to be more beneficial for the doping of devices with complex geometries, conformally.

1.3.5 Hybrid spin-on doping on Ge

Despite the scarce use of Ge in the semiconductor industry, reports of spin-on doping in the last number of years have been more frequent than on Si. Jamil *et al*. recently applied the spin-on doping process in the fabrication of high-mobility P-doped Ge nMOSFETs.[66] **Figure 1.20** shows I_d-V_d characteristics of Ge (100) nMOSFETs. Using similar dopants to Sadhu[65], they showed that the SOD-doped nMOSFETs showed improved junction characteristics and an approximately 1.3 × enhancement in drive current over the ion-implanted control devices. Scanning resistance probe (SRP) measurements showed peak electrical activation approaching 7×10^{19} atoms/cm^3, which is up to 3 times higher than that of the ion-implanted control sample. This higher activation may be attributed to a lower defect density. Raman studies showed an intensity close to pristine Ge, which is in stark contrast to the implanted Ge where the much lower intensity showed significant residual crystal damage. The *I-V* characteristics of the diodes showed a lower defect density when doped using the SOD technique; with approximately two orders of magnitude lower reverse junction leakage when compared to analogous structures doped by ion-implantation. nMOSFETS exhibited good I_{on}-I_{off} ratios of between 10^4 and 10^5. The MOSFETS exhibited high mobility with a μ_{eff} approaching 679 cm^2 V^{-1}.s^{-1}.

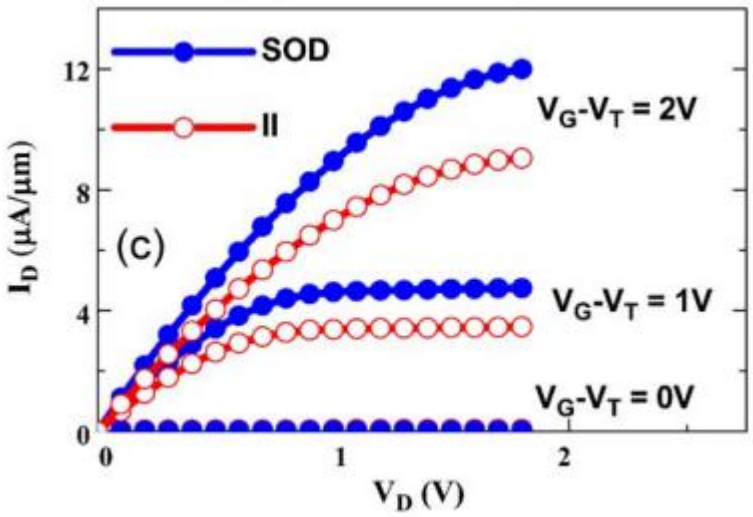


Figure 1.20. I_d-V_d characteristics of the Ge (100) nMOSFETS at V_G-V_T intervals of 1 V showing a 1.3 enhancement in drive current over ion-implanted control samples.[66] Reproduced with permission from ref: 66 Copyright 2011, IEEE.

Sharp and co-workers used a spin-on sol-gel dopant film containing Ga to dope Ge exceeding 10^{20} atoms/cm^3.[67] Sheet resistance and SIMS profiling were used to determine the dopant profiles. Peak dopant concentrations approached 2×10^{20} atoms/cm^3. Unfortunately, junction depths varied with temperature from 80 nm to well over 2 μm, showing a lack of control over the diffusion depth. While this approach may prove useful due to its simplicity and cost-effectiveness, it is unlikely to satisfy the requirements to form ultra-shallow junctions, further highlighting the significance of the MLD technique where dopant depth and diffusion are easily controlled.

More recently, Sorianello *et al.* published a study of SOD phosphorus diffusion in Ge thin films on Si for near-infrared (NIR) detectors.[68] Using a Filmtronics© phosphorus

SOD, a layer of the dopant was spun onto a substrate and then annealed at 580 °C. SIMS analysis showed peak concentrations approaching 1×10^{20} atoms/cm^3. The profile was not box-like, which is expected due to potential inhomogeneity of thermally grown Ge films. The group also applied the SOD process to Ge on Si heterojunction detectors with high responsiveness of 0.1 A/W with a signal-to-noise ratio of 25 dB at 1.55 μm. The junction depth approached 1 μm, again highlighting an application where MLD could provide for a much reduced dopant diffusion depth. The authors also reported cracking in the SOD thin film post-annealing, an issue which would not be encountered in a typical MLD process.

Kim and co-workers reported the application of an Sb-containing SOD to GeOI inversion-type nMOSFETS, with a body thickness of 16 nm, fabricated by a Ge condensation technique.[69] They first applied the process to bulk GeOI before transferring to MOSFETS. After annealing at 650 °C, peak chemical concentrations approached 1×10^{23} atoms/cm^3 with a junction depth of approximately 12 nm. In order to estimate the free electron concentration after Sb diffusion, accumulation-type GeOI nMOSFETS were fabricated and the threshold voltage was monitored before and after doping. The electron concentration after Sb diffusion was observed to be approximately 3×10^{18} atoms cm^3. Ultrathin nMOSFETS with 16 nm widths were fabricated and doped using the Sb SOD process. A high threshold voltage was observed due to the device operating in back-gate mode with the 100 nm buried oxide gate insulator as well as the high hole concentration on the Ge p-body.

Bao and co-workers recently applied laser annealing combined with a P-based SOD to dope n-type Ge (100) to form p-n junctions.[70] Photodetectors were fabricated to

test the combined SOD and laser anneal process. A low junction bulk leakage current density of 5.4 mA/cm^2 and surface leakage current density of 2.0 μA/cm were achieved. The photodetector had a responsiveness of 0.46 A/W at 1.55 μm wavelength at 0 V bias. The 130-μm diameter detector had an approximately -3 dB bandwidth of 190 MHz, highlighting that laser doping is a useful method for forming Ge p-n junctions for microelectronic and photonic device applications. Peak chemical concentrations approached 1×10^{19} atoms/cm^3 for the laser annealed blanket samples but with a junction depth of approximately 850 nm. Although the junction depth reported by Bao and co-workers is a shallower depth than that reported by Sharp *et al.*,[67] future work may require the adaptation of an MLD process to this work to allow for shallower diffusion depths while maintaining the high P-concentration.

Most recently, Al-Attili and co-workers applied SOD using P-containing dopants from two different suppliers with differing physical properties to dope GeOI wafers for monolithic light sources on Si.[71] Using commercially available GeOI wafers, P-containing SODs from Emulsitone© and Filmtronics© at varying ratios of SOD-to-IPA, were spin-coated at a constant speed for a constant time. All samples were annealed at 580 °C. Active carrier concentrations approached 2×10^{19} atoms/cm^3. The study showed that SOD of Ge is not straightforward, and there are numerous practical process issues still to be resolved. In this work, most of the problems arose from the poor adhesion between Ge and the buried oxide (BOX) layer. In particular, uniform coating was very important to avoid the formation of cracks during annealing. Additionally the authors used a ramp of the bake temperature in the case of B and P SOD to minimise cracking of the SOD film which could lead to non-uniformity of the film. This could affect dopant dose uniformity during the rapid thermal anneal

treatment to yield irregular dopant profiles. The minimisation of damage at the surface is one of the advantages of the MLD process and may be more suited to such applications.

1.4 CONCLUSIONS AND OUTLOOK

While the use of gas-phase and solution-phase surface chemistry for ultra-shallow doping of semiconductors is in its infancy, a vast body of research has accumulated over the last 5-10 years. *In-situ* doping of nanostructures, especially of bottom-up grown nanostructures, will remain challenging in terms of scale-up and reproducibility which, for now, makes it unsuitable for integration into CMOS manufacturing processes. Spin-on doping remains a cheap and effective method for doping semiconductor materials but much work remains to be done with respect to their use in nanoscale device structures. The majority of recent studies report that many practical issues remain, such as cracking of the SOD glass post RTA treatment. With device dimensions and geometries becoming smaller and three-dimensional, this aspect of the SOD process is undesirable for doping of such nanostructures. In contrast, the monolayer doping (MLD) technique is a strong candidate to replace ion-implantation, spin-on-doping and *in-situ* doping for thin-body devices and extreme-3D structures due to its conformality, controllable dopant profiles and lack of damage to the semiconductor substrates and devices. The process has also shown great promise on many materials which are relevant to the micro- and nano-electronics industries such as Si and Ge, in addition to upcoming replacement material such as InGaAs. However, work must continue into applications of the MLD process on new device architectures such as junction-less transistors and gate-all-around transistors[72,73] Aside from microelectronics, the MLD process has also been successfully applied with great success to solar cell materials and optoelectronic materials. Concurrently, there is a need for innovative improvements to metrological techniques to be made in order for the ultra-shallow junctions to be characterised to ensure conformality and abruptness. Additionally, the challenge of scaling up the

MLD process from a Schlenk flask to a semiconductor processing line will need to be met if MLD is to be integrated into future CMOS fabrication facilities. There is much scope, in terms of surface chemistry, to finely tune the process to each material. To date, there have been no MLD studies using Al ,Ga, Sn and Sb dopants. Synthesis of suitable precursor molecules for these MLD processes will be challenging with respect to air-sensitivity and toxicity. Despite the challenges, the grafting of organic molecules onto semiconductor surfaces offers an exciting approach over the conventional doping methods. Applications of MLD to next-generation device architectures such as gate-all-around FETs and tunnel FETs may prove interesting and will require the bringing together of expertise from device physicists, chemists and engineers to realise the next building blocks for our electronic devices.

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Chapter 2

Experimental

2 EXPERIMENTAL

2.1 DOPANT PRECURSOR SYNTHESIS

2.1.1 Synthesis of triallylarsine

Arsenic trichloride, anhydrous diethyl ether, stabilised deuterated chloroform and mesitylene were purchased from Acros Organics. Mesitylene was dried, distilled from calcium hydride and stored over molecular sieves before use. All other chemicals were used as received without further purification. Allylmagnesium bromide was purchased from Sigma-Aldrich and used as-received. All chemical manipulations were carried out under strictly anaerobic conditions in an atmosphere of ultra-high purity argon from Air Products Inc. using a combination of Schlenk apparatus and an inert-atmosphere glovebox. Triallylarsine (TAA) was synthesised according to literature procedures. [1-3] A reaction scheme for this synthesis showing the structure of the molecule is shown in **Figure 2.1**. Briefly, allylmagnesium bromide (138.5 ml, 138.5 mmol) was set to stir in a three-neck round bottom flask. To one arm was attached a coil condenser with an argon inlet. A pressure-equalising addition funnel containing arsenic trichloride (5.0 g, 2.3 ml, 28 mmol) in anhydrous diethyl ether (25 ml) was attached to the middle arm and the remaining arm was stoppered. The arsenic trichloride solution was added to the Grignard reagent at 0 °C over a period of 30 min under vigorous stirring. On completion of the arsenic trichloride addition, the reaction was left to warm to room temperature for a further 30 min and was then heated to reflux for 2 h. The reaction was once more cooled to 0 °C after 2 h and a deoxygenated, saturated solution of NH_4Cl at 0 °C was added very slowly to neutralise the remaining Grignard reagent. The mixture was filtered into a large separating

funnel and the organic phase was extracted with a 25 ml portion of diethyl ether. The aqueous phase was washed separately with 3 × 25 ml portions of diethyl ether and the washings were combined with the organic phase. The organic phase was dried with granular magnesium sulfate and filtered into a round-bottom flask. Excess diethyl ether was removed by rotary evaporation and the oily residue was distilled twice using a Kugelrohr short path distillation apparatus.

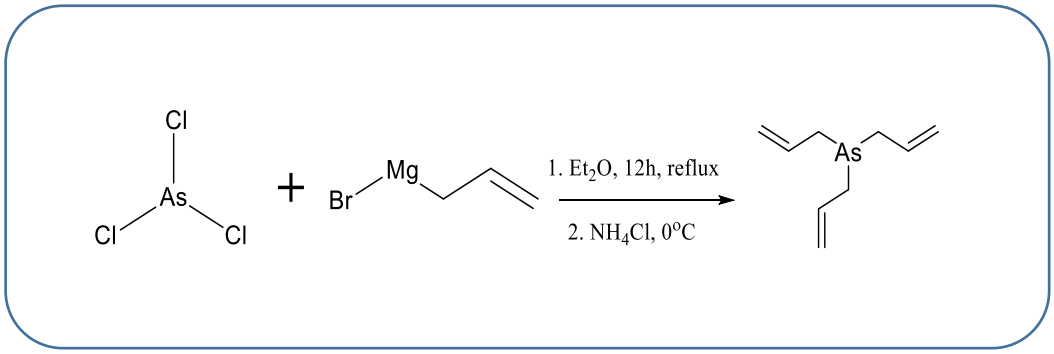


Figure 2.1. Synthetic reaction scheme for the triallylarsine molecule. Arsenic trichloride was reacted with an excess of allylmagnesium bromide in refluxing diethyl ether for 12 h. After the 12 h had elapsed the reaction was quenched with saturated ammonium chloride solution at 0 °C and stirred for a further 2 h after which the oily residue was twice distilled and stored under argon.

2.1.2 Synthesis of arsenic azide

Ascorbic acid, copper sulphate, sodium borohydride, arsenic trichloride, 1,6-heptadiyne, 1,7-octadiyne and 1,9-octadiyne were purchased from Acros Organics. 1,8-octadiyne, carbon tetrachloride, sodium azide and diphenylphosphoryl azide (DPPA) were purchased from Sigma Aldrich. All alkynes were pre-dried using sodium borohydride and distilled under reduced pressure before use. Mesitylene and dimethylformamide (DMF) were dried and distilled from calcium hydride and stored over molecular sieves before use. All other chemicals were used as received without further purification. All chemical manipulations were carried out under strict inert conditions in an atmosphere of ultra-high purity argon from Air Products Inc. using a combination of Schlenk apparatus and an Innovative Technologies inert-atmosphere glovebox. Arsenic azide (AA) $(AsN_3)_3$ was prepared using literature procedures from Klapökte *et al*.[4] CAUTION: While $(AsN_3)_3$ is explosive and can explode on contact with a metal syringe or spatula it may be handled safely in solution. Briefly, sodium azide (NaN_3) (10 g, 150 mmol) was dissolved in a minimum amount of water to make up a saturated solution and was activated by the addition of hydrazine hydrate (1 mol. %) and left to stir for 12 h. Acetone was added to precipitate the activated NaN_3. The precipitate was filtered and washed copiously with acetone and ethanol. 1.06 g (10 mmol) of the activated NaN_3 was added to a two-necked round bottom flask and suspended in 10 ml of carbon tetrachloride (CCl_4). To this solution was added 0.3 mL of arsenic trichloride ($AsCl_3$) and the solution was stirred vigorously for 12 h to ensure complete mixing of the reagents. The suspension was then filtered to remove unreacted NaN_3 and the NaCl side product and the yellow, oily, filtrate in CCl_4 was stored under Ar before being used directly for the CuAAC reactions. A reaction scheme is shown in Figure 2.2.

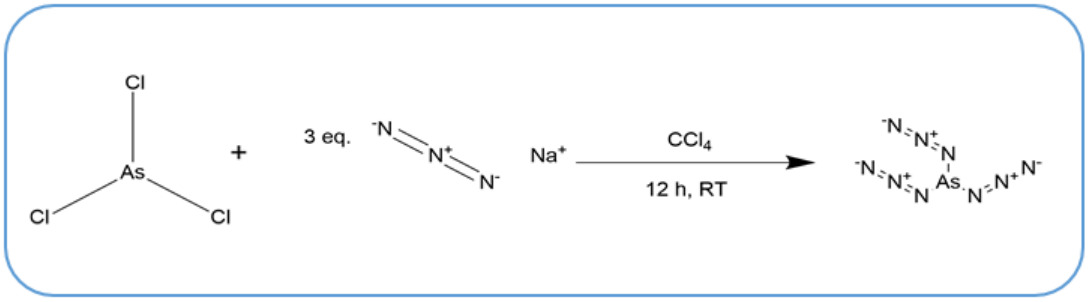


Figure 2.2. Synthesis of arsenic azide. Sodium azide was activated by dissolution in a minimum amount of water to make a saturated solution. 1 mol % of hydrazine hydrate was added and left to stir for 12 h. After 12 h had elapsed, acetone was added to precipitate the sodium azide which was filtered, washed with ethanol and dried. Arsenic trichloride was reacted with 3 equivalents of the activated sodium azide in carbon tetrachloride for 12 h at room temperature and used directly for the azide-alkyne cycloaddition.

2.2 CHARACTERISATION TECHNIQUES

2.2.1 X-ray photoelectron spectroscopy (XPS)

X-ray photoelectron spectroscopy is a technique used to quantitatively measure the elemental compositions and chemical states at surfaces. An XPS spectrometer measures the kinetic energy of electrons emitted from an atomic core level illuminated by x-ray photons of energy $h\nu$. The kinetic energy (E_k) measured is converted to a more chemically-meaningful binding energy (B_E) according to the relationship, $B_E = h\nu - E_k - \Phi$, where Φ refers to the spectrometer work function. Only electrons which are emitted without losing kinetic energy contribute towards the characteristic photoelectric lines. Electrons from deeper within the sample, which lose kinetic energy through inelastic scattering, contribute toward the background spectrum.

An X-ray photoelectron spectrometer typically consists of a hemispherical electron energy analyser and a dual-anode X-ray source, *e.g.* Mg K_α (1253.6 eV) and Al K_α (1486.6 eV) within an ultra-high-vacuum chamber; typical base pressure of 10×10^{-10} mbar. The photons emitted by the Mg and Al anodes offer the best energy resolution while still able to excite at least one core level for each known element.

The XPS data reported in this thesis were acquired on an Oxford Applied Research Escabase XPS system equipped with a CLASS VM 100 mm mean radius hemispherical electron energy analyser with a triple-channel detector arrangement, in an analysis chamber with a base pressure of 5.0×10^{-9} mbar. Survey scans were acquired between 0-1400 eV with a step size of 0.7 eV, a dwell time of 0.5 s and a pass energy of 100 eV. Core level scans were acquired at the applicable binding energy range with a step size of 0.1 eV, a dwell time of 0.5 s and a pass energy of 20

eV averaged over 50 scans. A non-monochromated Al-K_α X-ray source at 200 W power was used for all scans. Where applicable, the N 1s spectra for each sample were acquired immediately after the survey spectrum to negate any effect of the X-ray induced bremsstrahlung on surface azo- groups. All spectra were acquired at a take-off angle of 90° with respect to the analyser axis and were charge corrected with respect to the C 1s photoelectric line by rigidly shifting the binding energy scale to 285 eV. Data were processed using CasaXPS software where a Shirley background correction was employed and peaks were fitted to Voigt profiles. To ensure accurate quantification, atomic sensitivity factors were taken from the instrument spectrum acquisition software and manually inputted into the data processing software.

2.2.2 Fourier Transform Infrared Spectroscopy (FTIR) and Attenuated Total Reflectance (ATR) FTIR

Chemical moieties absorb specific frequencies that are characteristic of their chemical structure and bonding. When subject to infrared radiation (4000 – 500 cm^{-1}) molecules exhibit behaviours such as stretching, bending and vibrations depending on the functional groups present. FTIR analysis involves guiding the IR light through an interferometer and from there through the sample. This allows all of the IR frequencies to be scanned simultaneously allowing faster and higher quality acquisition. FTIR provides an interferogram as its output which is then converted to a spectrum by Fourier transformation.

Attenuated total reflectance infrared spectroscopy (ATR-FTIR) involves passing an incident ray of infrared light through a hemispherical crystal of a high refractive index material (in this case, Ge) which reflects off the internal surfaces in contact with the

sample. The internal reflectance creates an evanescent wave which extends beyond the ATR crystal into the sample which is in tight contact with the crystal. Functional groups on the surface may absorb IR, causing attenuation of the evanescent wave. This attenuation is detected by a liquid nitrogen cooled mercury-cadmium-telluride detector. FTIR and ATR-FTIR measurements were carried out on a Thermo Scientific Nicolet 6700 spectrometer using a Harrick Scientific ATR-FTIR VariGATR accessory.

2.2.3 Electrochemical Capacitance Voltage Profiling

Capacitance-voltage (CV) measurements are one of the most widely used techniques to measure dopant distributions in samples, as the depth distribution of the free charge carriers is related to the dopant profile. Unfortunately, measurement depth is limited due to electrical breakdown of the junction when the critical field intensity is reached. To rectify this problem, Ambridge and co-workers suggested another method where the semiconductor surface is contacted with an electrolyte to form a quasi-Schottky diode. The main advantage of this technique is that the maximum depth is not limited by the maximum breakdown voltage. The ECV process comprises two main steps: 1) measurement of CV characteristics and 2) etching of the material. The etching takes place either using a high-intensity lamp, in the case of *p*-doped samples, or voltage etching where *n*-type samples are being analysed. Repeated etch and measurement cycles enables a depth vs active dopant (carrier) concentration profile to be obtained. ECV analysis was carried out on a WEP Control CVP21 wafer profiler using 0.1 M ammonium hydrogen bifluoride as the etchant for Si and 0.4 M disodium 4,5-dihydroxy-1,3-benzenedisulfonate (Tiron) as the etchant for InGaAs. Scanning parameters were automatically controlled by the instrument by selecting the

appropriate sample type, layer map and etchant combination. Error in concentration. did not exceed 10 % for ECV analysis on Si. For InGaAs analysis, error in concentration did not exceed 10%

2.2.4 Secondary Ion Mass Spectrometry

Secondary Ion Mass Spectrometry (SIMS) is a technique used to analyse compositions of thin films and surfaces by using a focused primary ion beam to sputter the surface of a sample and analyse the ejected secondary ions. SIMS is a qualitative technique nominally but, if combined with standards, can be considered a quantitative technique. A SIMS instrument generally consists of a primary ion gun, UHV chamber holding the sample and ion extraction lens, a mass analyser and a means of detecting the ejected ions. SIMS is used in the semiconductor industry to characterise thin films and, more pertinently, the total dopant concentration in samples. When compared to ECV, SIMS yields the total concentration of the dopants, *i.e.* combined active and inactive carrier concentrations. SIMS analysis was carried out in conjunction with assistance from the Centre Microcharacterisation de Raimond Castaing at the University of Toulouse, France. SIMS measurements were carried out on a CAMECA IMS 4F6 spectrometer equipped with a $O_2^{+,}$ O^- and Ar^+ source. A low energy mode of 2 kV accelerating voltage and beam current of 20 nA was used to analyse the composition of the sample close to the surface of the sample where the diffusion process in MLD is most effective. SIMS analysis was benchmarked using known calibration standards and samples.

2.2.5 Nanowire electrical measurements

Electrical data was obtained from 4-point test structures using a Cascade Probe Station and an Agilent B1500 semiconductor parameter analyser, with the assistance of Dr. Maryam Shayesteh, Tyndall National Institute, Cork. All data were acquired at room temperature using gold-plated probes with tungsten tips.

2.2.6 Electron microscopy

Electron microscopy is the most widely used method for visually characterising nanomaterials. The wavelength of an electron is up to 10,000 times shorter than that of visible light, allowing higher resolving power. Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) are two of the most widely used techniques for imaging nanomaterials. In SEM imaging, the electron beam is rastered across a sample surface, where an image is produced by secondary electrons and backscattered electrons. Secondary electrons are generated when the incident electron beam induces excitation of an electron in the sample, resulting in the loss of energy. These secondary electrons mostly lost at the surface which yield morphology and topography information about the sample. TEM studies the interaction of an electron beam which is transmitted through a sample. Samples must be very thin to be suitable for TEM analysis. TEM is useful in device analysis to monitor for the presence of extended defects. SEM images were acquired on an FEI Quanta 650 FEG scanning electron microscope. Cross-sections for TEM analysis were prepared on a FEI Helios Nanolab. TEM images were acquired using a JEOL 2100.

2.2.7 Thermogravimetric Analysis

Thermogravimetric analysis (TGA) is used to measure changes in weight as a function of temperature. TGA is useful to determine decomposition temperatures for molecules to identify suitable candidates for MLD reactions. Analysis was performed on a Mettler Toledo TGA/DSC 1 STAR system. Experiments were carried out from 25 to 300 ^{o}C at a heating rate of 5 ^{o}C/min in nitrogen.

2.2.8 Atomic Force Microscopy

Atomic force microscopy (AFM) is a technique used to monitor sample topography. Topographic images are generated when a sharp tip at the end of the AFM cantilever is brought near to the surface of a sample surface. A force is observed due to the interaction of a cantilever and a sample surface which leads to a deflection of the cantilever in accordance with Hooke's Law.[5] AFM images were acquitted on a Park Systems XE-100 microscope.

2.2.9 Nuclear Magnetic Resonance

Nuclear magnetic resonance (NMR) spectroscopy was used to verify the formation and purity of synthesised dopant molecules. NMR spectroscopy was performed on a Bruker AVANCE 300 NMR spectrometer.

2.2.10 Raman Scattering Spectroscopy

Raman scattering spectroscopy is a tool used for the measurement of vibrational modes of phonons within a material. In Raman spectroscopy monochromatic light interacts with the material and information on the vibrational modes of the sample is recorded through analysis of this scattered light. This technique is a powerful method

for site-specific measurements, particularly when coupled with a microscope allowing for greater precision of the site to be analysed.[6]

Raman scattering spectroscopy data were collected with a Renishaw InVia Raman spectrometer equipped with a 2400 lines/mm grating using a 514 nm 30 mW Argon Ion laser, spectra were collected using a RenCam CCD camera. The beam was focused onto the samples using either a 20 ×/50 × objective lens. The laser power density was adjusted to ensure that the thin film surfaces did not undergo sample heating during the full spectral acquisition time.

2.3 Organo-Arsenic Molecular Layers on Silicon For High-Density Doping

2.3.1 General Procedure for Si Substrate Functionalisation with TAA

All glassware was cleaned with a piranha wash, dried in an oven overnight at 130 °C and allowed to cool under a stream of dry Ar on the Schlenk line. TAA was dissolved in mesitylene (5 ml) to make up a 2.5 % v/v solution. The solution was degassed and dried using several freeze-pump-thaw cycles and left to purge under a positive pressure of argon while the substrate was being prepared. A 1.5 cm^2 sample of Si was degreased, cleaned by standard RCA washes and immersed in a 20 % solution of hydrofluoric acid to remove surface oxide and metal contaminants and to induce H-passivation of the surface. The substrate was dried under a stream of dry nitrogen and placed immediately into a two neck round bottom flask under argon to prevent re-oxidation of the surface. The TAA solution was then cannulated under a positive pressure of Ar into the flask containing the H-passivated Si substrate. The flask was then heated up to 180 °C under argon and left for 2 h at reflux, maintained by means of a thermocouple temperature feedback controller. The colour of the solution was

monitored over the course of 2 h. After the reaction had completed the substrate was removed from the vessel and immediately immersed in a vial of anhydrous toluene and sonicated to remove any physisorbed species. The sample was rinsed in a vial of fresh anhydrous toluene and sonicated in successive vials of anhydrous toluene, dichloromethane and ethanol with careful drying in a N_2 stream between each vial. The sample was kept under an inert atmosphere before removal for further processing and characterisation.

2.3.2 Fabrication of Nanowire Test Devices

Silicon-on-insulator (SOI) substrates were patterned using a Raith e-Line Plus electron beam lithography (EBL) system. The substrates were patterned using hydrogen silesquioxane (HSQ) (Dow Corning Corp) as the resist. The top Si layer thickness was approximately 50 nm. The substrates were degreased by sonication successively in acetone and isopropylalcohol (IPA) solvents and blown dry in a stream of N_2. Following a bake at 120 °C for 5 min a 1:2 concentration solution of HSQ in methylisobutyl ketone (MIBK) was spun on the substrates at 2000 rpm for 33 s, giving a HSQ film approximately 50 nm thick on any substrate. The substrates were again baked at 120 °C for 3 min prior to EBL exposure. EBL exposure was a two-step process where the first lithography step was carried out to pattern only the high resolution fin structures. In the second step the contact pads for the four probes were exposed. To attain a highly focused beam for the first step, a 10 kV beam voltage and 100 μm write-field was chosen. To avoid a large exposure time, the low resolution contact pads were written with a 1 kV beam voltage and 400 μm write-field. After the EBL exposures, the substrates were developed in a solution of 0.25 M NaOH and 0.7 M NaCl for 15 s followed by a 60 s rinse in DI water and a 15 s immersion in IPA.

For the second lithography step, HSQ was spun onto the substrate with the aforementioned parameters and then exposed. To transfer the HSQ pattern onto the top Si layer of the SOI substrates, they were subjected to a reactive ion etch (RIE) using Cl_2 chemistry in an Oxford Instruments Plasmalab 100 system.

2.4 Monolayer Doping of Si With Improved Oxidation Resistance

2.4.1 General Procedure for Si Substrate Functionalisation with diynes

All glassware was cleaned with Alconox detergent followed by copious rinsing with water and then cleaned with a piranha wash (CAUTION: this is a strong oxidising agent and reacts violently with organic substances), dried in an oven overnight at 130 °C and allowed to cool under a stream of dry Ar on a Schlenk line. 1,7-octadiyne was dissolved in previously dried mesitylene (5 ml) to make up a 25 % v/v solution. The solution was degassed and dried using several freeze-pump-thaw cycles and left to purge under a positive pressure of argon while the substrate was being prepared. A 1.5 cm^2 sample of Si was degreased, cleaned by standard RCA washes[7] of a 5:1:1 solution of H_2O, NH_4OH and H_2O_2 followed by a 5:1:1 solution of H_2O, HCl and H_2O_2. Following a rinse in H_2O the substrate was immersed in a 2.5 % v/v solution of hydrofluoric acid for 1.5 min to remove surface oxides and to induce H-passivation of the surface. These etching parameters are known to give a mainly di-hydride terminated surface.[8] The substrate was dried under a stream of dry nitrogen and placed immediately into a two neck round bottom flask under argon to prevent re-oxidation of the surface. The dialkyne solution was cannulated under a positive pressure of Ar into the flask containing the H-passivated Si substrate. The flask was then heated to 170 °C under Ar and left for 2 h at reflux. After the reaction had completed the substrate was removed from the vessel and immediately immersed in a vial of

anhydrous toluene and sonicated to remove any physisorbed species. The sample was rinsed in a vial of fresh anhydrous toluene and sonicated in successive vials of anhydrous toluene, dichloromethane, ethyl acetate, ethanol and hexane with careful drying in a N_2 stream between each vial. The sample was kept under an inert atmosphere before removal for the subsequent "click" reaction. This process was repeated for the remaining dialkynes.

2.4.2 General procedure for CuAAC "click" reaction

A sample previously functionalised with the applicable dialkyne was placed into a cleaned two-neck round bottom flask. To this flask was added: i) the applicable azide (10 mM in DMF), ii) copper(II) sulphate (0.8 mol% relative to the azide) and (iii) ascorbic acid (80 mol% relative to the azide). The flask was heated to a temperature of 60 °C and left for 12 h under Ar. The samples were rinsed with an excess of water and ethanol and rinsed with 0.5 M hydrochloric acid solution to remove any potential traces of physisorbed Cu salts. Samples were rinsed once more with ethanol and water immediately prior to analysis.

2.4.3 General procedure for functionalisation of Si surface with allyl diphenylphosphine (ADP)

All glassware was cleaned with a piranha wash, dried in an oven overnight at 120 °C and allowed to cool under a positive stream of dry Ar on a Schlenk line. ADP was dissolved in mesitylene (5 ml) to make up a 25 % v/v solution. The solution was degassed and dried using several freeze-pump-thaw cycles and left to purge under a positive pressure of argon *via* cannula while the substrate was being prepared. A 1.5 cm^2 sample of Si was degreased and then cleaned by standard RCA washes and

immersed in a 20 % v/v solution of hydrofluoric acid to remove surface oxide and metal contaminants and to induce H-passivation of the surface. The substrate was dried under a stream of dry nitrogen and placed immediately into a two neck round bottom Schlenk flask under a positive pressure of argon to prevent re-oxidation of the surface. The ADP solution was then cannulated under a positive pressure of Ar into the flask containing the H-passivated Si substrate. The flask was then heated up immediately to 180 °C under argon and left for 2 h at reflux, maintained by means of a thermocouple temperature feedback controller. The colour of the solution was monitored over the course of 2 h. After the reaction was complete the substrate was removed from the vessel and immediately immersed in a vial of anhydrous toluene and sonicated to remove any physisorbed species. The sample was rinsed in a vial of fresh anhydrous toluene and sonicated in successive vials of anhydrous toluene, dichloromethane and ethanol with careful drying in a N_2 stream between each vial. The sample was kept under an inert atmosphere before removal for further processing and characterisation. A schematic of this procedure is shown in **Figure 2.2**.

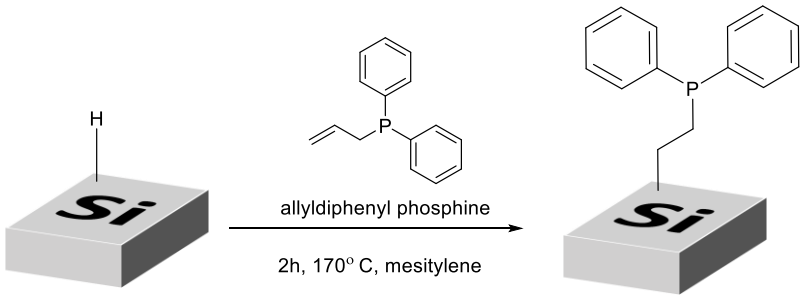


Figure 2.2. Schematic representing the reaction of allyldiphenyl phosphine (ADP) with a H-terminated Si (100) surface. The Si surface was first degreased and cleaned using RCA washes and then etched with HF to give a H-terminated surface. The substrate was then immersed in a solution of ADP in mesitylene for 2 h at 170 °C. After a post-reaction clean in anhydrous solvents the substrate was functionalised with ADP.

2.5 LIQUID-PHASE MONOLAYER DOPING OF INGAAS WITH AN SI-CONTAINING ALKYLTHIOL AND SN-CONTAINING ORGANIC MOLECULAR LAYERS

2.5.1 InGaAs substrate fabrication

Epitaxial $In_{0.57}Ga_{0.43}As$ semiconductor layers with an approximate thickness of 200 nm were grown on 2 inch semi-insulating InP substrates using an Aixtron metal-organic vapour phase epitaxy (MOVPE) system. Trimethylindium, trimethylgallium and arsine were used as the In, Ga and As sources respectively. An AlInAs barrier of approximately 100 nm was grown on the InP substrate prior to epitaxy of the InGaAs to prevent upward diffusion of dopant atoms from the InP substrates during the rapid-thermal-anneal step, thus negating the effect of the substrate on any measurements. This stack structure minimises defects at this composition due to nominal lattice matching between each of the layers. A schematic showing the stack structure is shown in **Figure 2.3**.

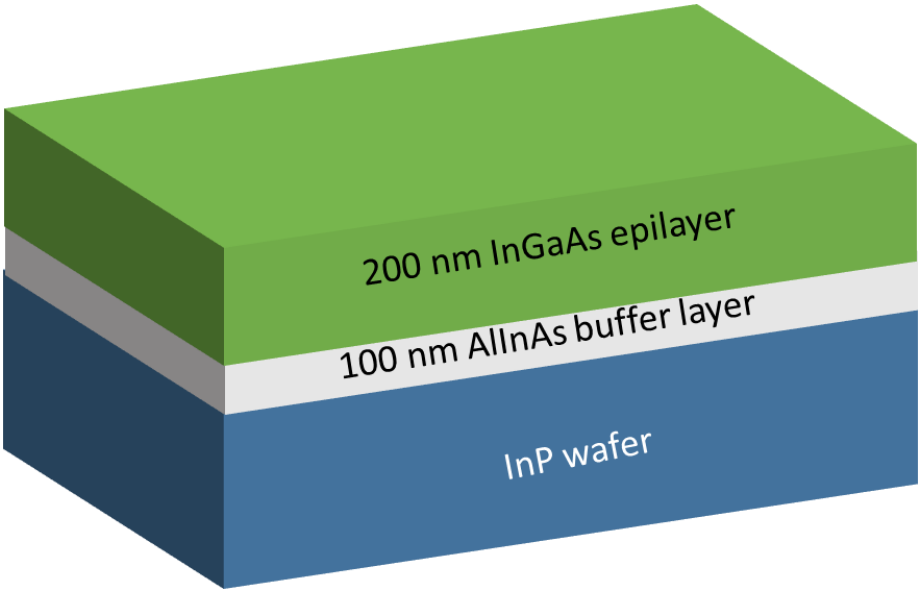


Figure 2.3. Figure showing the stack structure of the substrates used in this work. Epitaxial InGaAs semiconductor layers with an approximate thickness of 200 nm were grown on 2 inch semi-insulating InP substrates using an Aixtron metal-organic vapour phase epitaxy (MOVPE) system at low pressure using N2 as carrier gas Trimethylindium, trimethylgallium and arsine were used as the In, Ga and As sources respectively. An AlInAs barrier of approximately 100 nm was grown on the InP substrate prevent upward diffusion of dopant from the InP substrates thus negating the effect of the substrate on any measurements.

2.5.2 General procedure for the functionalisation of the InGaAs surface with 3-mercaptotriethoxysilane

All glassware was cleaned scrupulously with Alconox detergent followed by copious rinsing with water and then cleaned with a piranha wash (CAUTION: this is a strong oxidising agent and reacts violently with organic substances), dried in an oven overnight at 130 °C and allowed to cool under a stream of dry Ar on the Schlenk line. InGaAs substrates were cleaved into 1 x 1 cm pieces. Samples were prepared for functionalisation using procedures adapted from McGuiness[9] *et al*. Briefly, the InGaAs token was degreased by sonication in acetone, MeOH and IPA for 15 min in each solvent and dried in a N_2 stream. The substrate was then dipped into a concentrated ammonium hydroxide solution for 2 min to remove the native oxides, rinsed in anhydrous IPA and dried in an N_2 stream. The substrate was then immediately placed into a two-necked round bottom flask under a positive pressure of Ar with one arm connected to the Schlenk line and the other neck stoppered. In a separate Schlenk flask, a 25 % v/v solution of 3-mercaptotriethoxysilane in anhydrous IPA was dried and degassed using three freeze-pump-thaw cycles. The solution was cannulated under a positive pressure of Ar into the flask containing the oxide-free InGaAs substrate and was left for 17-24 h at 80 ^{o}C. The substrate was then rinsed using hot IPA to remove physisorbed species and was immediately placed into an inert atmosphere prior to characterisation.

2.5.3 General procedure for the functionalisation of the InGaAs surface with allyltributylstannane.

Glassware was cleaned as described previously. Samples were prepared for functionalisation using procedures adapted from Lie and co-workers.[83] InGaAs substrates were cleaved into 1 × 1 cm pieces. The InGaAs token was degreased by sonication in methanol and acetone for 5 min each followed by drying in a stream of ultra-pure N_2. Native oxide removal was performed in hydrofluoric acid and water. The liquid phase HF etching of the InGaAs token took place in an aqueous solution of HF (49 %, Honeywell) and ultra-pure water (UPW, Milli-Q, 18MΩ cm^{-1}) at a volumetric ratio of 1:50 for 5 min at room temperature. The sample was rinsed with UPW and dried in an ultra-pure N_2 stream. These etching parameters have been reported to give an As-rich surface containing As-As or As-H bonds.[83] Allyltributylstannane, was dissolved in previously distilled and dried mesitylene to make up a 25 % v/v solution in a Schlenk flask. This flask was subjected to three freeze-pump-thaw cycles to remove any dissolved gases. This solution was cannulated directly under a positive pressure of Ar into a flask containing the InGaAs token. The reaction vessel was heated to 160 ^{o}C to maintain reflux and left for 2 h. The sample was rinsed consecutively in anhydrous toluene, hexane, ethanol and a final rinse in toluene to remove any physisorbed species. All samples were kept under an inert atmosphere prior to characterisation and processing.

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Chapter 3

Organo-Arsenic Molecular Layers on Si for High-Density Doping

This chapter has been published as a peer-reviewed article in ACS Applied Materials & Interfaces. Consequently, certain sections of the chapter may contain repeating concepts and paragraphs.

O'Connell, J.; Verni, G. A.; Gangnaik, A.; Shayesteh, M.; Long, B.; Georgiev, Y. M.; Petkov, N.; McGlacken, G. P.; Morris, M. A.; Duffy, R. and Holmes, J. D. Organo-Arsenic Molecular Layers on Silicon for High-Density Doping. *ACS Appl. Mater. Interfaces* **2015**, *7* (28), 15514–15521.

3 ORGANO-ARSENIC MONOLAYERS ON SILICON FOR ULTRA-HIGH-DENSITY DOPING

3.1 ABSTRACT

Ultra-shallow doping with high concentrations are key for the continued scaling of semiconductor device structures. Current techniques such as ion-implantation, spin-on doping and *in-situ* doping are proving to be problematic for doping devices with small feature sizes and complex device geometries. Monolayer doping has shown promise for P-doping and B-doping of a range of semiconductor substrates and nano-fabricated devices.

This chapter details the controlled monolayer doping (MLD) of bulk and nanostructured crystalline silicon with As at concentrations approaching 2×10^{20} atoms cm^{-3}. Characterisation of doped structures after the MLD process confirmed that they remained defect and damage free, with no indication of increased roughness or a change in morphology. XPS characterisation confirmed the presence of an organo-arsenic monolayer on the Si surface and was used to monitor the Si oxide level post-functionalisation. Electrical characterisation of the doped substrates and nanowire test structures allowed determination of resistivity, sheet resistance and active doping levels. Extremely high As-doped Si substrates and nanowire devices could be obtained and controlled using specific capping and annealing steps. Significantly, the As-doped nanowires exhibited resistances several orders of magnitude lower than the pre-doped materials. High-resolution, cross-sectional TEM imaging showed that the doped nanostructures remained without extended defects, which are easily visible using electron microscopy.

3.2 INTRODUCTION

Controlled doping of electronic devices at the nanoscale is challenging, especially as devices transition from planar to non-planar architectures, requiring innovative methods to reliably and reproducibly dope with extremely fine control and conformality.[1,2] Conventional dopant technologies, such as ion implantation, are problematic for advanced non-planar devices, *e.g.* fin field effect transistors (FinFET) due to the intrinsically high-energy nature of the bombardment process at the surface.[3] There are a number of disadvantages associated with ion implantation, including the difficulty in obtaining an abrupt implantation layer on a nanometre scale, poor control over the spatial distribution of implanted ions and often severe damage to the crystal lattice of the semiconductor. Additionally, the source gases used in ion implantation are also invariably harmful from a health and environmental perspective.[4]

An alternative approach to ion implantation is spin-on doping, which consists of depositing a dopant-containing solution onto a semiconductor surface, followed by a diffusion anneal step. Compared to ion implantation, spin-on doping is a non-destructive and simple technique, but there are still issues associated with this approach ranging from a lack of uniformity and dose control over large areas of the substrate.[5] Additionally, residues left over from the solvent containing the dopant precursor are not easily removed from the surface.[6] Plasma doping is an emerging and promising technique due to the suppression of crystalline defect formation and the realisation of nanoscale devices with reproducible electrical characteristics.[7] The doping profiles with plasma approaches are generally more conformal than those achieved using ion implantation, however some crystal damage can still occur and problems can still be encountered when attempting to dope with multiple species at

different energies in a single process.[8] Research is also continuing on the integration of dopants during nanomaterial fabrication and synthesis. This *in-situ* method of doping nanomaterials is promising but the challenges of scale-up and large scale integration in addition to the problematic concentration gradients still remain.[9]

Recently, a facile approach for controllable doping of semiconductor nanostructures was introduced, termed monolayer doping (MLD).[10] MLD comprises two steps: i) functionalisation of the semiconductor surface with a p- or n-dopant containing molecule and ii) thermal diffusion of those dopant atoms into a semiconductor by a rapid thermal anneal (RTA) step. MLD has been applied to a large variety of nanostructured materials fabricated by either the "bottom-up" or "top-down" approaches. The self-assembled monolayers are formed using self-limiting reactions, commonly a hydrosilylation reaction between a hydrogen-terminated surface and a labile C=C site on the dopant containing molecule. The surface chemistry of Si is well known and established, leading to a variety of methods with which to passivate and functionalise the surface.[11–17] MLD is extremely flexible as the surface preparations, molecular footprints, capping layer and also the thermal treatment parameters can all be finely tuned to optimise surface coverage of the molecule and diffusion of the dopant into the semiconductor surface, in addition to its ease of application to both "bottom-up" and "top-down" materials.

MLD has been demonstrated successfully using boron and phosphorus-containing molecules on bulk crystalline silicon substrates enabling the formation of sub-5 nm ultra-shallow junctions in conjunction with conventional spike annealing.[18] The technique has also successfully been applied to the doping of InAs materials and InP photovoltaics using sulfur containing monolayers.[19] MLD has also been successfully

used in conjunction with nanoimprint lithography to control the lateral positioning of the molecular monolayers using selective patterning steps.[20] A variation of the MLD process, termed monolayer contact doping (MLCD), has been demonstrated for the controlled doping of Si wafers where a donor substrate functionalised with the dopant-containing monolayer is placed in contact with an acceptor substrate and annealed together. The MLCD process has been shown on bulk Si substrates and a number of Si nanowire devices.[21] More recently, Hoarfrost and co-workers demonstrated a type of MLD involving spin-on organic polymer dopants in an attempt to bridge the MLD technique and conventional inorganic spin-on dopants. Compared to traditional spin-on dopants, these polymer based spin-on dopants may be easier to remove post-anneal. [22] Most recently, Puglisi *et al* reported an application of the MLD process to arrays of Si nanowire based solar cells, achieving electrical data that proved promising for the next generation of solar cell devices.[23] These examples show the great flexibility that the MLD process has for different materials. **Figure 3.1** schematically represents the MLD approach employed.

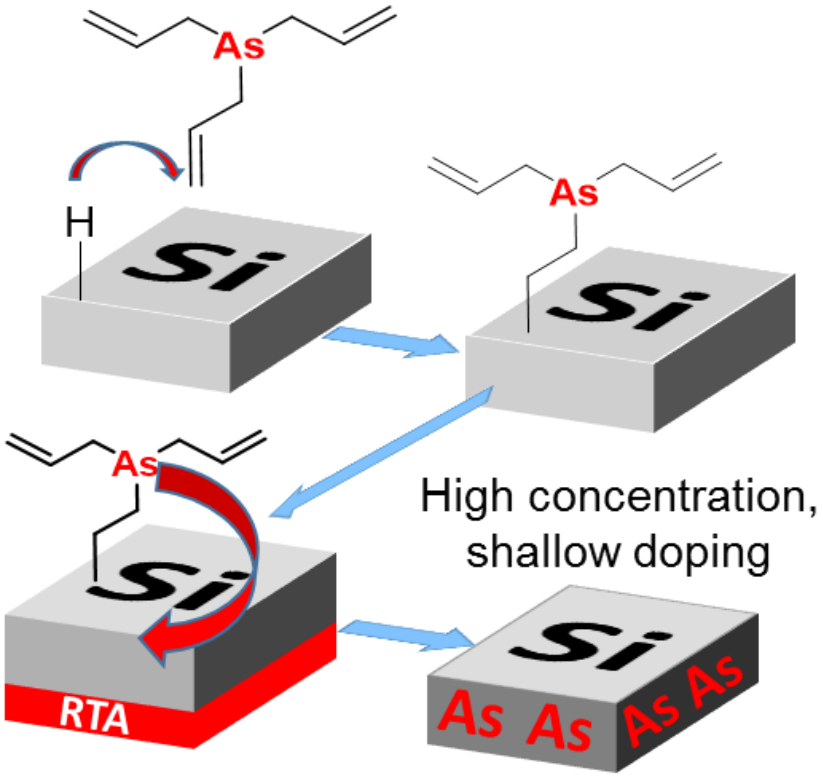


Figure 3.1. Schematic depicting the MLD process developed and applied in this study. A hydrosilylation reaction occurs between a reactive H-passivated Si surface and the labile C=C site on the dopant containing molecule, resulting in a covalently bonded molecular layer. The samples are then capped with 50 nm of SiO_2 and subjected to a rapid-thermal-anneal (RTA) step resulting in high concentration, shallow doping of silicon.

3.3 Results and Discussion

3.3.1 Modification of the H-terminated Si surface with TAA

Initial experiments were performed on bulk crystalline silicon substrates to ensure the process could be applied successfully for the material, to develop an experimental procedure for MLD and also to perform carrier profiling and SIMS profiling that is not possible at nanoscale feature sizes. The synthesis of the triallylarsine molecule is detailed in the Experimental section. **Figure 3.2(a)** shows a high-resolution XPS Si *2p* scan of a freshly cleaned and etched Si substrate with the inset depicting the surface after preparation. The absence of any detectable oxide features in the XP spectra indicated the presence of a close to pristine, oxide-free substrate surface necessary for MLD. **Figure 3.2(b)** shows an XPS survey scan of a Si substrate freshly functionalised with TAA molecules; the As *2p* and *3d* photoelectric lines are shown.

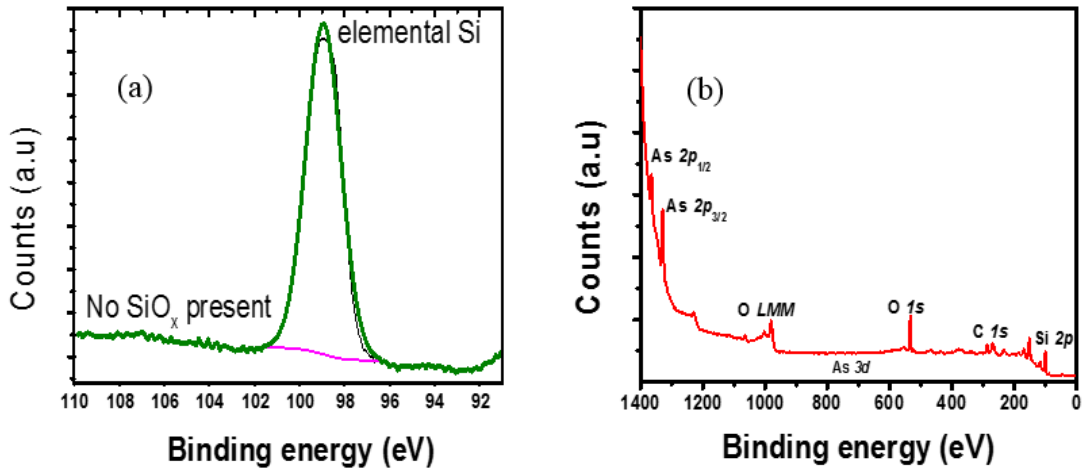


Figure 3.2 (a) High resolution Si 2p core level scan pre-functionalisation, showing the pristine oxide-less surface required for MLD with a schematic representation inset, (b) wide, survey scan of a TAA functionalised Si surface with peaks of interest labelled. Inset shows schematic representations of the functionalised surface.

The binding energy of the Si *2p* core level scan of the functionalised sample, shown in **Figure 3.3(a),** exhibits primarily the non-oxidised elemental peak at 99.8 eV, indicating a passivated surface which consists mainly of Si-C bonds. There is a very small presence of oxide at the higher binding energy of 103 eV[24] suggesting limited uptake during air exposure during transport to the UHV equipment. Note that the sample was transported under a positive pressure of Ar and introduced to the nitrogen-purged environment of the XPS instrument with less than 5 s of contact with air. The As *3d* spectrum acquired from the same substrate is shown in **Figure 3.3(b)**. The elemental As peak is shown at 42.0 eV [25] with a second peak chemically shifted to a higher binding energy of 44.8 eV. This binding energy and the chemical shift of 2.8 eV with respect to the elemental As component is consistent with the presence of an oxidised arsenic species on the surface of the substrate post-functionalisation and may be attributed to oxidation of the TAA molecule in air post-reaction.[26] Again, sample exposure to air was minimized as much as possible. The atomic percentages of the elemental As and oxidised As components were determined to be 28 % and 72 % respectively.

To determine if the Si oxide peak shown in **Figure 3.3(a)** was associated with post-functionalisation oxidation or the functionalisation process itself, a blank, non-functionalised Si sample was exposed to ambient conditions for 24 h and analysed by XPS. The amount of oxide observed was very similar to that obtained for the functionalised sample after a 2 h functionalisation procedure. This was observed despite several freeze-pump-thaw cycles being performed on the dopant molecule solution to remove traces of oxygen and water. The presence of this trace amount of oxide did not appear to have an appreciable effect on the dopant diffusion process.

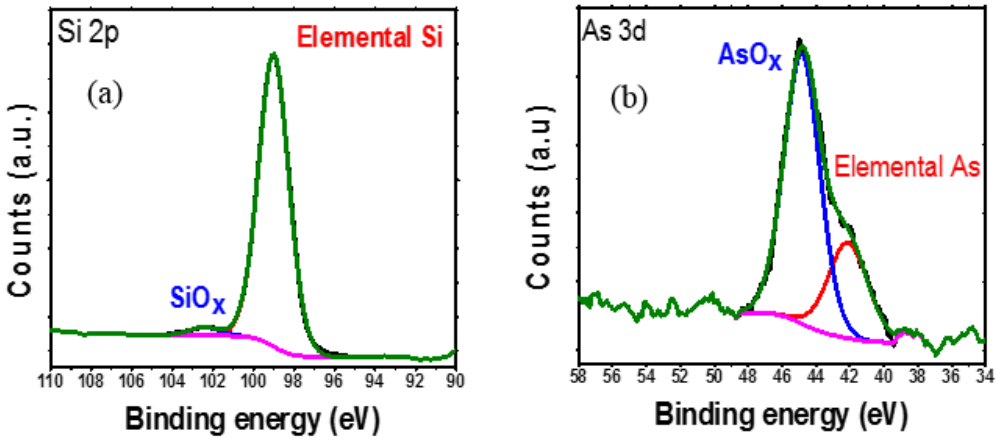


Figure 3.3. (a) Si *2p* core level spectrum of a freshly functionalised substrate composed primarily of elemental Si and a small shoulder peak indicating a low amount of SiO_x, (b) As *3d* core level spectrum of a TAA functionalised Si surface. The elemental components of the peak are labelled in red with the oxidised components of each sample labelled in blue.

3.3.2 Stability of Functionalised Samples toward Ambient Conditions

The stability of the underlying Si surface toward reoxidation is important. Regrowth of the oxide prior to rapid-thermal-anneal treatment and subsequent processing steps is undesirable. Functionalised Si is known to be more resistant to re-oxidation than non-functionalised Si.[27] To determine the resistance to reoxidation of the underlying silicon substrate post-functionalisation, a functionalised sample was left in ambient conditions for periods of time ranging from 24 h to one month and the XPS Si *2p* core level was used to determine the stability of the functionalised sample relative to a piece of unfunctionalised Si. The components corresponding to silicon oxides were monitored and recorded. The acquired stability spectra for the functionalised samples are shown in **Figure 3.4 (a)-(d**) with elemental Si and oxidised Si atomic percentage concentrations labelled. The comparative spectra on the unfunctionalised Si substrates are shown in **Figure 3.5 (a)-(d)**. With the exception of the first 24 h, the acquired data

showed no discernible difference between the rates of oxidation between a TAA functionalised substrate and a non-functionalised substrate. The rate at which the atomic concentrations of Si oxides increased was very similar between both samples. This oxidation may be attributed to the small molecular footprint of the TAA molecule, or possibly pinhole oxidation at unreacted hydrogen passivated sites, which is consistent with the fact that H-passivated silicon surfaces are only stable in air for a matter of minutes.[16]

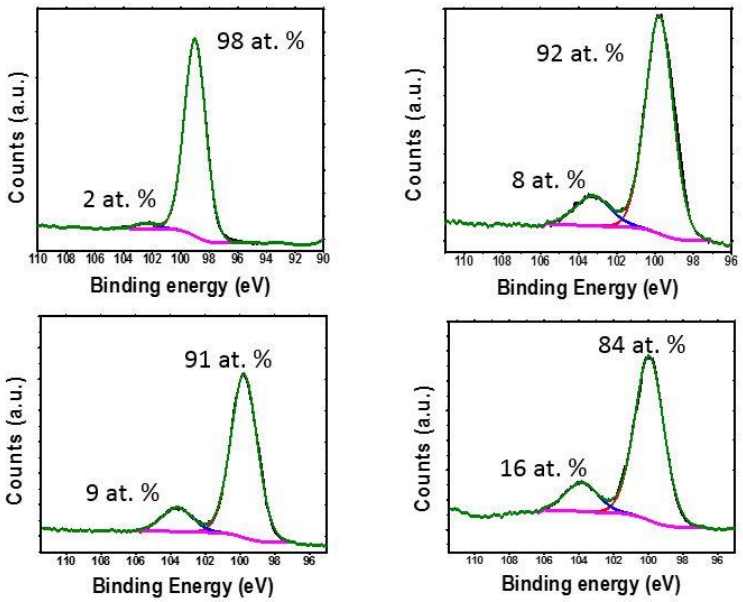


Figure 3.4 High resolution Si 2p core level spectra of a TAA functionalised silicon substrate left out in ambient conditions for comparison purposes. (a) Freshly functionalised substrate characterised immediately. (b) Spectrum acquired after 24 h. (c) Spectrum acquired after 1 week and (d) spectrum acquired after 1 month under ambient conditions.

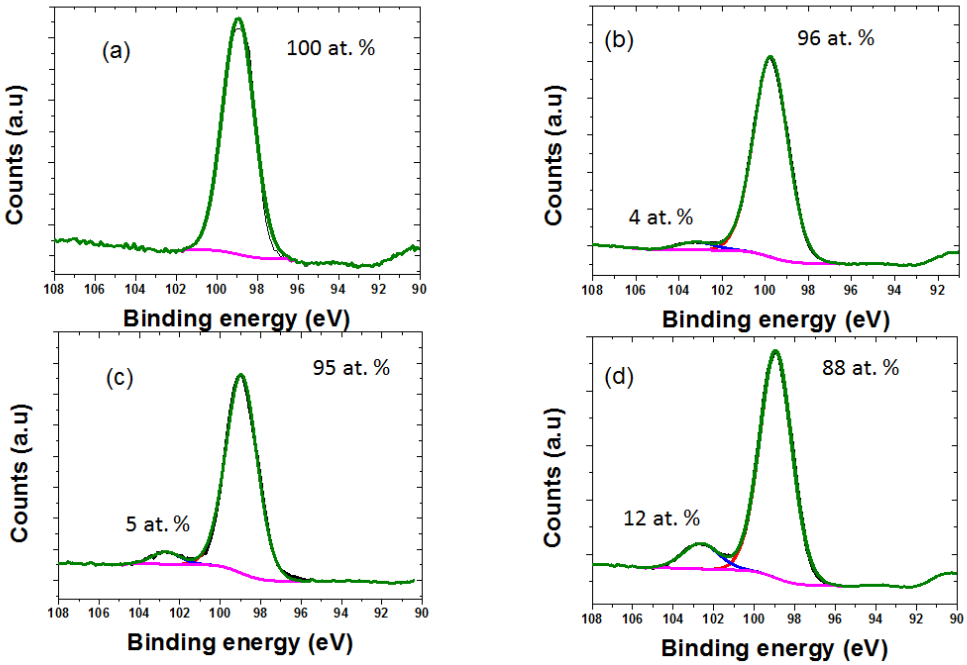


Figure 3.5. High resolution Si 2p core level spectra of a non-functionalised silicon substrate left out in ambient conditions for comparison purposes. (a) Freshly cleaned and etched substrate characterised immediately. (b) Spectrum acquired after 24 h. (c) Spectrum acquired after 1 week and (d) spectrum acquired after 1 month under ambient conditions.

3.3.3 Estimation of Overlayer Thickness

A good indicator of the coverage and thickness of the organo-arsenic layer on Si substrates was estimated by XPS analysis of the TAA functionalised sample as shown in Figure 3.3 (b) using a method originally defined by Cumpson, from equation 1. [28] The overlayer referred to here is the monolayer composed of the TAA molecule.

$$\ln\left(\frac{I_0 S_0}{I_s S_s}\right) - \left(\frac{\lambda_0}{\lambda_s}\right)\frac{1}{\lambda_0 \cos\theta} - \ln 2 = \ln \sinh\left(\frac{t}{2\lambda_0 \cos\theta}\right) \quad (1)$$

where I_0 and I_s represent the respective measured peak intensities of the overlayer and substrate peaks, S_0 and S_s refer to the relative sensitivity factors for the overlayer and the substrate respectively with λ_0 and λ_s referring to the attenuation lengths of electrons in the overlayer and substrate. θ is the emission angle with respect to the surface normal. To minimise the effect of potential errors arising from surface roughness and inelastic scattering a photon emission angle of 35^o was used in conjunction with a 90^o take-off angle with respect to the sample normal. The peak intensity of the organoarsenic overlayer peak, I_o, and the peak intensity of the substrate peak, I_s, were determined using CasaXPS software after a transmission correction. The relative sensitivity factors for the substrate peak S_s and the overlayer peak S_o were obtained from the database in the XPS instrument acquisition software and manually input into the data processing software to remove instrumental factors which may affect quantification. The attenuation length of photoelectrons in the overlayer, λ_o, was estimated using the NIST Electron Effective Attenuation Length database to be 2.6 nm. The overlayer thickness was therefore estimated to be approximately 0.5 nm

which, based on the predicted molecular footprint of the TAA molecule of approximately 0.6 nm, would imply the presence of a monolayer on the Si surface. The surface was thoroughly cleaned by prolonged sonication in anhydrous solvents prior to characterisation to remove all physisorbed species prior to analysis to minimize contributions from contaminants to the overlayer thickness.

3.3.4 Carrier Profiling

The functionalised substrates were capped with a 50 nm layer of sputtered SiO_2 and heated by rapid thermal annealing under nitrogen at varying temperatures for 5 s, to investigate the effect of temperature on the dopant depth and concentration gradient. While the specific composition of the capping layer and the method used for deposition can affect the monolayer integrity and diffusion process but the effect of the capping layer was not studied in this work. Use of electron beam evaporation or plasma-enhanced chemical vapour deposition could be investigated to determine the effect on the MLD process. The oxide cap was removed post anneal using a buffered oxide etch prior to further characterisation. To ascertain the dopant depth, total dopant concentration and active carrier concentration a set of samples were analysed by SIMS. **Figure 3.6** shows SIMS derived chemical concentration *vs.* depth data of three samples thermally treated for 5 s at 950, 1000 and 1050 ^{o}C respectively. The data shows, as expected, that the higher processing temperature results in an overall higher incorporation of As in Si, with the maximum chemical concentrations approaching 2 $\times$ 10^{20} atoms/cm^3 at 1050 °C. **Table 1** summarises the chemical concentration data and also shows chemical dose and diffusivity (*D*) data extracted from the SIMS profiles by integration, in Figure 3.6.

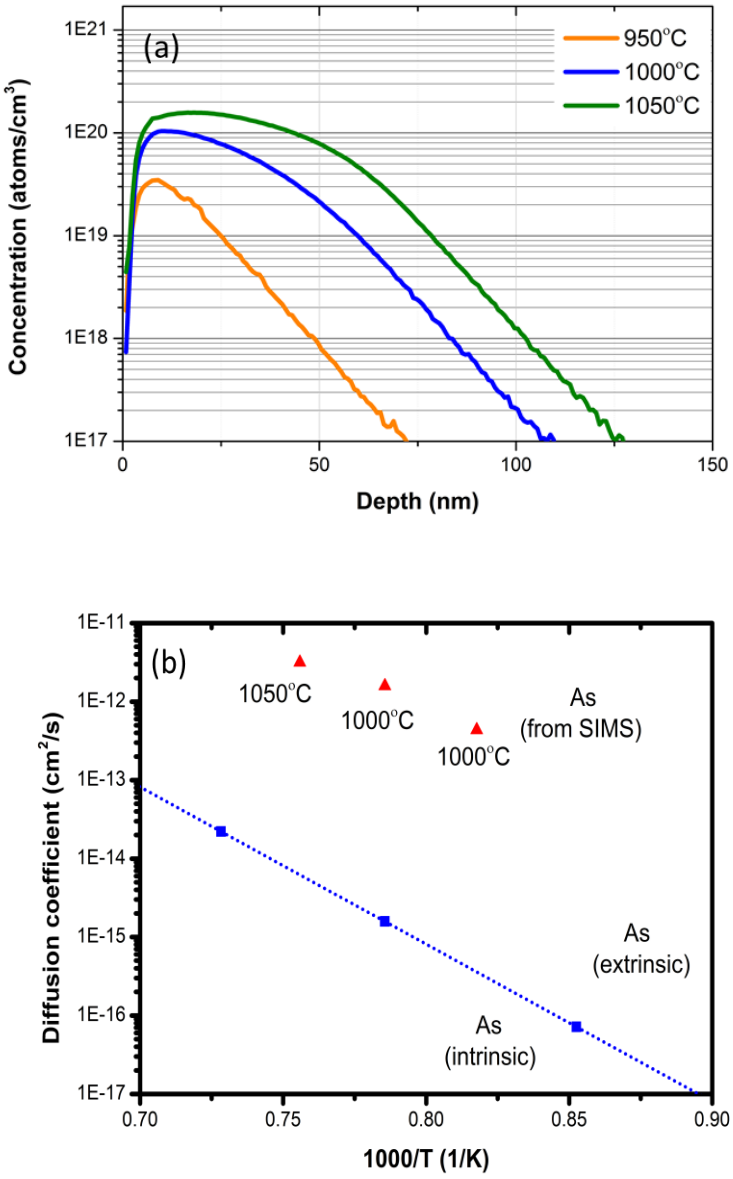


Figure 3.6. (a) Secondary ion mass spectrometry profiles of 3 samples processed at varying temperatures for 5 s. The carrier depths were observed to be extremely shallow with peak concentrations achieved at less than 25 nm (b) Diffusivity data extracted from SIMS analysis. As can be seen in the measured data in red, the samples exhibit diffusivity in the extrinsic regime.

Temperature (°C)	**Dose (atoms/cm^3)**	**Max concentration (atoms/cm^3)**	***D*** **(cm^2/s)**	n_i **(atoms/cm^3)**	C/n_i
950	5.69×10^{13}	3.41×10^{19}	4.36×10^{-13}	7.00E+18	4.9
1000	3.31×10^{14}	1.04×10^{20}	1.58×10^{-12}	1.00E+19	10.4
1050	7.06×10^{14}	1.57×10^{20}	3.16×10^{-12}	1.50E+19	10.5

Table 1. Extracted data for blanket samples showing the total chemical dose and diffusivity data extracted from the SIMS profiles in Figure 3.6, where *D* refers to the diffusivity, n_i refers to the intrinsic carrier concentration and C/n_i is the surface impurity concentration over the intrinsic carrier concentration.

Figure 3.6(b) depicts the extracted diffusivity data *vs*. 1000/*T* (*T* in Kelvin) plotted in red and compared with the intrinsic diffusivities from the literature plotted in blue. The data shows that extrinsic diffusivity rates are observed in this study. The doped substrates also exhibited high carrier concentrations. The concentrations increased evenly with the rising rapid-thermal anneal temperature, *i.e.* controlled diffusion. Semiconductor devices rely on the ability to form two different types of electrically-conducting layers: p-type and n-type. An electrically active dopant atom contributes a free carrier to the valence band or conduction band by creating an energy level that is very close to either band. Therefore an ideal dopant should have a shallow donor/acceptor level and a high solubility. The vast majority of MLD work to date has been concerned mainly with phosphorus- and boron-containing moieties and, thus

far, no reports exist of MLD using As-containing liquid molecules. Concentrations approaching 6×10^{20} atoms/cm^3 have been reported in the literature for phosphorus-MLD in conjunction with spike annealing at 1050°C using a P source with a molecular footprint of approximately 0.12 nm,[29] while concentrations as high as 10^{22} atoms/cm^3 have been noted for P-MLD using a high temperature soak anneal with spike annealing.[30] The TAA molecule has a similar molecular footprint and peak concentrations for the As-MLD process used here are of the same order of magnitude as previous P-MLD work with junction depths an average of 50 nm from SIMS data in Figure 3.6 (a). Arsenic and phosphorus are considered to be the best choices for n-type doping of semiconductors based on their ionisation energies[31] and also based on their high solubilities in Si.[32] For extremely small feature size devices with complex and non-planar geometries that need abrupt shallow doping profiles it is desirable that the diffusion rate of the dopant is small. Compared to phosphorus, As has a much smaller diffusion coefficient, making it the dopant of choice for heavy and shallow n-type doping of silicon.[33] As the junction depth in the MLD process is limited by temperature and duration of anneal, the diffusion of As in Si using the MLD method could be further fine-tuned in terms of shallower junction depths by using emerging spike annealing techniques such as flashlamp annealing and laser annealing.[34-36]

3.3.5 Application of the MLD Strategy to Nanowire Devices

As the MLD process can be applied to various types of semiconductor surfaces, including nanostructured quasi-1D and 2D materials, an analogous arsenic doping process was attempted to controllably dope 'top-down' Si nanowires fabricated on silicon-on-insulator substrates. Intense research continues into semiconductor nanowires due to their potential in the scaling of semiconductor devices.[37] As Si has long been the material of choice in the semiconductor industry its properties are well

known and its processing technologies are well established, making Si nanowires ideal for fundamental research, while maintaining compatibility with current electronic processing techniques for eventual integration into future technology nodes. As nanowires in general have large surface-to-volume ratios, defects trapped at Si/SiO_x interfaces have acute effects on the performance of a device by trapping and scattering mobile charge carriers.[38] The applications of certain surface passivation techniques, such as hydrogen-termination[39], can greatly reduce the density of these defects and increase the FET response of a Si nanowire channel.[40] An advantage of the MLD process developed in this study is that there is no damage to the nanowires, which might otherwise be caused by techniques such as ion implantation. Charge depletion caused by the presence of surface states can potentially limit the effective channel diameter of a nanowire. Additionally, dielectric mismatch between a nanowire and its surrounding can also cause changes in the electrical characteristics by increasing the ionisation energies for dopants which are near the nanowire surface.[41] This problem can be overcome by using good surface treatments which minimize surface damage and enable high-dopant densities and, most importantly for FET doping, high conformality which is attainable using the MLD based strategy employed here.

To properly assess the effects of the MLD process on fine features, top-down patterned Si nanowires (fins) ranging in width from 20 – 1000 nm were fabricated. The fabrication process is described in detail in the Experimental chapter of this thesis. A SEM micrograph of the test structure itself is shown in **Figure 3.7**.

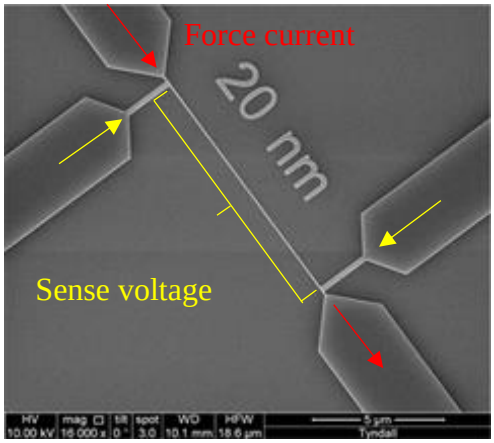


Figure 3.7 A SEM micrograph of the 20 nm nanowire test structure. The four-point probe structure is shown, where a current is forced by the outer electrodes and the resulting voltage drop across the nanowire is sensed by the inner electrodes. Resistance can then be extracted from this current-voltage relationship.

In essence, the structure is a 4-point probe test structure where a user-defined current is forced across the nanowire by the outer electrodes and then the inner electrodes sense the resulting voltage drop across the nanowire. The design of the contact pads ensures that the voltage drop at the nanowire is measured accurately. The nanowire resistance can be extracted from this current-voltage relationship. The raw I-V data shown in **Figure 3.8(a)** are of post-MLD nanowires. The resistivity data shown in **Figure 3.8 (b)** is from the pre- and post-MLD nanowires. In **Figure 3.8(a)** the current as a function of voltage is linear for all nanowires and passes through the origin. As expected, the current level can also be seen dropping as the nanowire width is scaled down. This change in the current is indicative of ohmic current conduction and good dopant activation, where even 20 nm devices were observed to conduct current very well, indicating that the MLD process was non-destructive toward the smallest

nanowires. Assuming that current flows uniformly through the entire cross section of a nanowire, similarly to a metal track, the resistivity (ρ) of a nanowire can be calculated from equation 2:

$$\rho = R\frac{A}{L} \tag{2}$$

where L refers to the length of a nanowire, A is the cross-sectional area and R is resistance. The application of this model is appropriate for sub-40 nm nanowires and FinFETs as at these dimensions the probability of having a uniformly doped cross-section is higher. At the smallest sizes it can be assumed that the entire volume of the device is uniformly doped and current flows throughout the entire cross-section *i.e.* like that of a metal track. As current devices are sub-40 nm and future technologies will continue to scale, this model offers a better platform to evaluate device behaviour in current and future device technologies. Figure 3.8 (b) shows both pre- and post-MLD resistivity data for nanowires. Significantly lower resistivities were obtained for post-MLD nanowires, especially those with widths less than 40 nm. There is a similar striking difference of several orders of magnitude between the resistivities of the nanowires pre- and post-MLD. The largest decrease in resistivity was observed within nanowires with dimensions under 40 nm, with a decrease of between 5 orders of magnitude for larger nanowires and 7 orders of magnitude for the smallest sized nanowires, when compared to the undoped nanowires; showing the efficacy of the MLD process on such small feature size devices.

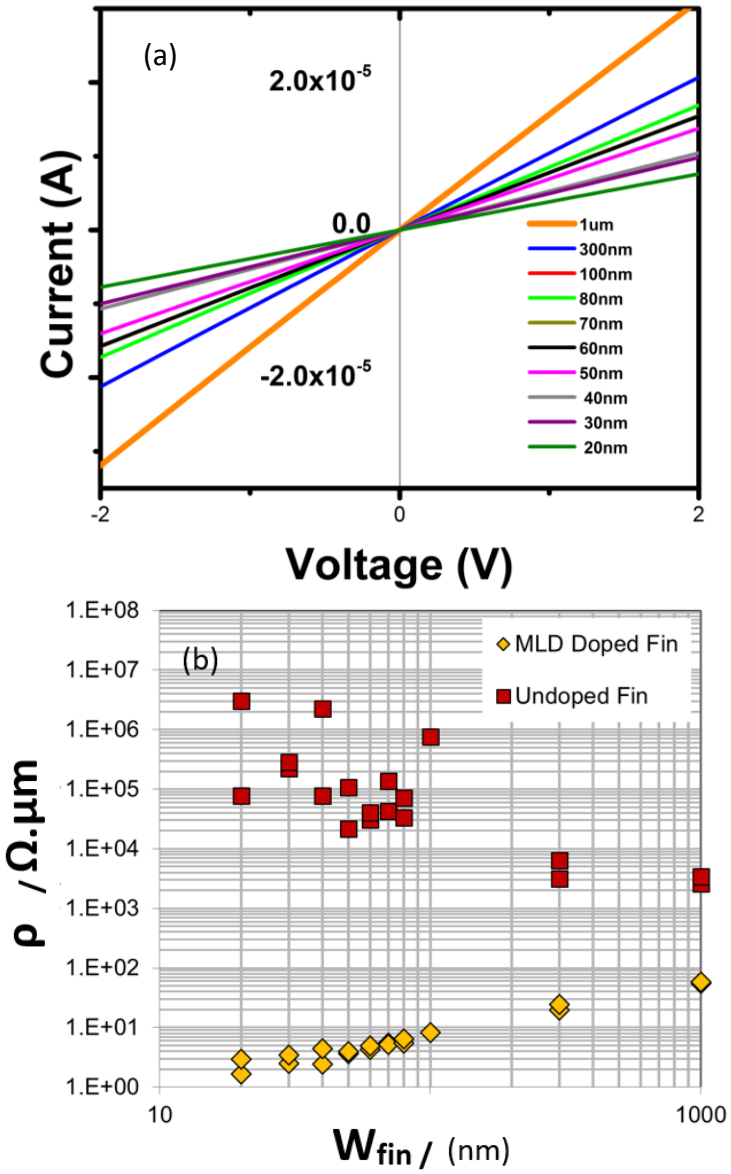


Figure 3.8 (a) Raw I-V data for post-MLD nanowires. The data is symmetrical about the origin with the current obeying Ohms law and scales with reducing nanowire width. (b) Resistivity of nanowires as a function of width for pre-MLD and post – MLD wires. The best results were observed for nanowires < 40 nm in width, showing that the MLD strategy employed works extremely well for small feature sizes.

To confirm that the MLD process did not affect nanowire morphology, cross-sectional TEM analysis of the doped nanowires was undertaken. Historically, {111} twin boundary defect formation and stacking faults are the most common problems faced when doping at small feature sizes, most often caused by ion-implantation processes. Extended defects are considered here as these defects are quite visible by TEM analysis. **Figure 3.9(a)** shows a TEM image of a section of a 40 nm Si nanowire test device. **Figure 3.9(b)** displays a magnified high-resolution TEM image of the same nanowire with the <111> and <100> directions indicated. The Fast Fourier Transform (FFT) shown in the inset of Figure 3.9 (b) shows the highly crystalline nature of the nanowire, which is consistent with the non-destructive nature of the MLD process. There are no indications on either micrograph of any extended defects or damage to the crystal lattice, showing that the developed arsenic-MLD process as applied to bulk Si wafers also transfers very well to nanostructured devices. This is in stark contrast to ion implanted nanostructures where crystal damage is very easily visible and poly-crystalline changes can be problematic with a decreasing $W_{\text{fin.}}$

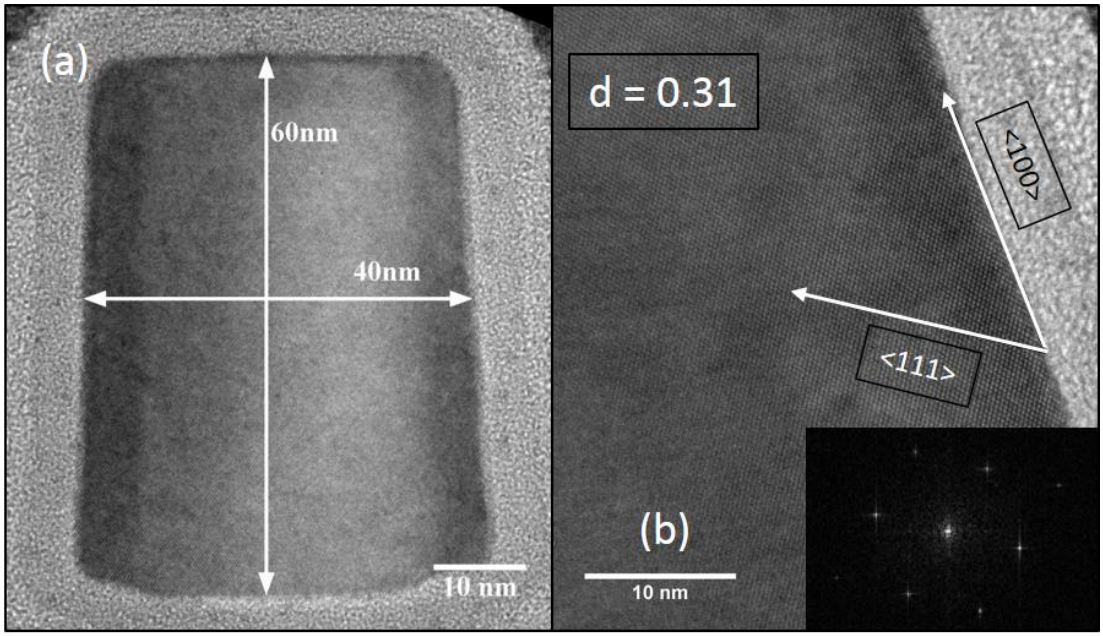


Figure 3.9 (a) TEM micrograph of a section of the 40 nm Si nanowire test device, (b) magnified HRTEM micrograph of the nanowire with the <111> and <100> directions indicated. The FFT shown in the inset of (b) shows the highly crystalline nature of the nanowire. There are no indications on either micrograph of any defects or damage to the crystal lattice.

3.4 CONCLUSIONS

The doping of non-planar nanostructures is difficult due to the non-conformality of conventional doping methods in addition to the problems encountered during diffusion, during their activation, in trying to prevent their escape during the thermal processing treatments and all the while still trying to preserve the crystalline nature of the material. The controlled doping of bulk and nanostructured silicon was achieved successfully *via* the use of organo-arsenic molecular monolayers. Extremely high dopant concentrations approaching 2 x 10^{20} atoms cm^{-3} were observed for bulk Si while excellent electrical characteristics were observed for the MLD-doped Si nanostructures with the with the highest decrease in resistivity of seven orders of magnitude observed for nanowires less than 40 nm in width. The MLD process was observed to have no effect on the crystallinity of the nanowires and no visible damage or defects were observed. Research must continue on the design and characterisation of suitable molecular precursors that are stable during the hydrosilylation procedure and remain stable and resistant to decomposition in ambient conditions afterwards. An interesting investigation would be the use of molecules containing more than one dopant atom; binary arsines and binary phosphines for example. MLD via "click-chemistry" would also be an excellent alternative to current strategies and would provide insight into the dependence of concentration on the distance of the dopant atom from the semiconductor surface.

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Chapter 4

Monolayer Doping of Si With Improved Oxidation Resistance

This chapter has been published as a peer-reviewed article in ACS Applied Materials & Interfaces. Consequently, certain sections of the chapter may contain repeating concepts and paragraphs.

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4 MONOLAYER DOPING OF SI WITH IMPROVED OXIDATION RESISTANCE

4.1 ABSTRACT

This chapter outlines the functionalisation of planar silicon with arsenic- and phosphorus- based azides *via* an alkyne-azide cycloaddition route. Covalently bonded and well-ordered alkyne-terminated monolayers were prepared from a range of commercially available dialkyne precursors using a well-known thermal hydrosilylation mechanism to form an acetylene-terminated monolayer. The terminal acetylene moieties were further functionalised through the application of copper-catalysed azide-alkyne cycloaddition (CuAAC) reactions between dopant-containing azides and the terminal acetylene groups. The introduction of dopant molecules *via* this method does not require harsh conditions typically employed in traditional monolayer doping approaches, enabling greater surface coverage with improved resistance towards re-oxidation. X-ray photoelectron spectroscopy studies showed successful dialkyne incorporation with minimal Si surface oxidation and also showed successful azide-alkyne cycloaddition through monitoring of the C *1s* and N *1s* core-level spectra. Electrochemical capacitance-voltage measurements showed effective diffusion of the activated dopant atoms into the Si substrates.

4.2 INTRODUCTION

A growing challenge for the semiconductor and microelectronics industry is the ability to effectively dope nanoscale materials positioned in non-planar and small feature size device geometries.[1] New methodologies for shallow doping of semiconductors are required if complementary metal oxide semiconductor (CMOS) devices are to continue scaling in accordance with Moore's Law.[2,3] Ion beam implantation, the highly energetic process of bombarding a semiconductor surface with ions has been the conventional method of doping for a number of years but its efficacy is much reduced at the nanoscale.[4] Numerous problems, such as the inability to control the abruptness of the profile over a nanometre range, the crystallographic damage caused to the surface and the incompatibility of the technique with quasi-one dimensional structures such as nanowires, must be overcome if device geometries are to continue to scale effectively. Many potential alternatives to ion beam implantation have been proposed ranging from plasma immersion ion implantation,[5,6] polymeric spin-on dopants[8] and monolayer doping (MLD).[7,9–14] The traditional monolayer doping process combines the rich surface chemistry of semiconductors with the self-assembly of dopant containing molecules on the semiconductor surface, most commonly *via* a one-step hydrosilylation process. MLD has already been shown to be a suitable technique for shallow doping of Si devices with complex and non-planar geometries, allowing fine control over dopant profiles. The functionalisation of Si surfaces can also improve the resistance of the surfaces towards oxidation, a requirement for sensor applications[15-23]

This article describes the use of copper-catalysed alkyne-azide cycloaddition (CuAAC) reactions between a primary passivation layer on a Si surface composed of di-alkynes with reactive terminal alkyne moieties, and a dopant-containing azide. A schematic showing the general functionalisation method is shown in **Figure 4.1**.

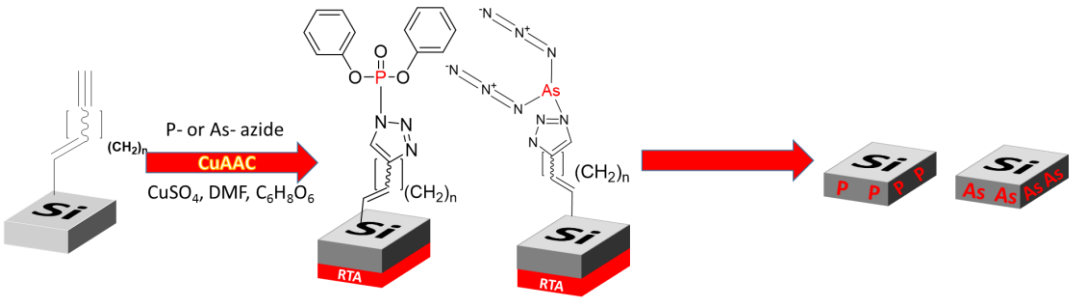


Figure 4.1. Schematic showing the functionalisation and doping strategy employed here. A silicon sample previously functionalised with a dialkyne *via* thermal hydrosilylation is immersed in a solution of a dopant-containing azide, copper sulfate, DMF and ascorbic acid where an alkyne-azide cycloaddition occurs to form a dopant containing monolayer on the Si surface. These samples are then capped with SiO_2, and subjected to a rapid thermal anneal of 1050 ^oC for 5 s and the cap is subsequently removed to give shallow doped Si.

Firstly, di-alkynes of increasing lengths (between 7 and 10 carbons) were attached to the Si-H surface using a thermal hydrosilylation method.[24,25] The dopant-containing azide was then "clicked" onto the alkyne moiety using a Huisgen 1,3-dipolar cycloaddition reaction under very mild conditions, allowing the formation of tightly packed, high-quality monolayers on Si surfaces. Using a commercially-available di-alkyne is advantageous as it is not necessary to synthesise the required di-alkyne. Additionally, the symmetrical structure of the dialkyne molecule permits the

acetylene-terminated monolayer to be formed in one quick step. The Huisgen 1,3-dipolar cycloaddition reaction is one of many reactions independently specified as a "click" reaction by Sharpless *et al.* and also by Meldal.[26,27] Click reactions are nominally of wide scope, selective, proceed in good yield and are exceptionally hardy to most reaction factors considered harsh, such as the presence of oxygen, aqueous solvents and high temperatures. [28] The hydrosilylation reaction remains the most widely used method to produce well-ordered alkyl molecular layers on Si but some disadvantages still remain.[29] For example, the high temperatures required for hydrosilylation limits the type of dopant molecules that can be used in MLD to those which are stable at the reaction temperature. Additionally the presence of any trace amounts of water or oxygen, combined with a high-temperature reaction can cause re-growth of surface oxides, which can disrupt the dopant-containing monolayer. Whilst click chemistry functionalisation has been used in materials science for a range of applications such as redox behaviour studies and protein adsorption[30-33], to the best of our knowledge the technique has not been used for MLD of semiconductors. The coupling of azides to terminal alkynes is one of the most useful modular approaches to building-up monolayers. The click-chemistry approach described in this chapter greatly suppresses the effect that ambient, aerobic conditions could potentially have on the underlying Si surface due to the protection that the primary di-alkyne passivation layer offers. Additionally, the dopant-containing azides used in this study are resistant to attack by atmospheric oxygen and moisture. The conventional MLD approach typically involves the use or design of a molecular precursor that contains not only the dopant atom but also the unsaturated C=C bonds required for the hydrosilylation reaction to take place between the C=C labile site and H- terminated surface. While this route is experimentally convenient for the substrate

functionalisation step, these types of precursors are typically air-sensitive with complex synthesis procedures and difficult to purify. Additionally, the molecular footprints of the molecule, as well as steric effects from substituents, may affect packing at the substrate surface potentially causing pinhole oxidation points. The method described in this chapter separates the C=C labile site from the dopant molecule and instead, introduces the dopant molecule *via* the subsequent alkyne-azide cycloaddition reaction. This two-step process allows the use of established hydrosilylation chemistry with commercially available and decomposition-resistant molecules to form well-ordered monolayers, which offer much improved oxidation protection for the underlying substrate. The terminal acetylene groups act as reactive "handles" on which the dopant-containing molecules can be "clicked" using relatively mild reaction conditions and green solvents.

4.3 Results and Discussion

4.3.1 Assembly of 1,7 Octadiyne Monolayers on the H-terminated Si (100) Surface and Subsequent Functionalisation with Diphenyl Phosphoryl Azide

Functionalisation procedures are outlined in detail in the Experimental chapter of this thesis. **Figure 4.2(a)** shows the Si *2p* core level spectrum of a Si (100) surface after a standard RCA clean and fresh HF etch. The spectrum shows no evidence of Si oxides typically observed at binding energies between 101 eV and 104 eV and exhibits a primary peak centred at ~100 eV[34] implying the presence of a clean, pristine surface required for the functionalisation steps. **Figure 4.2(b)** shows the Si 2p spectrum after functionalisation with 1,7-octadiyne *via* thermally-induced hydrosilylation. The survey spectrum shown in **Figure 4.2(c)** indicates the presence of Si, O and C which is consistent with the presence of an organic monolayer on the Si substrate.[35-37] The absence of oxide associated peaks in the Si *2p* core level spectrum suggest that a well-ordered organic monolayer has formed which offers good resistance toward re-oxidation of the underlying substrate. A small O *1s* peak at 532 eV can be attributed to contributions from adventitiously adsorbed oxygen during sample transport to the UHV environment of the XPS spectrometer.

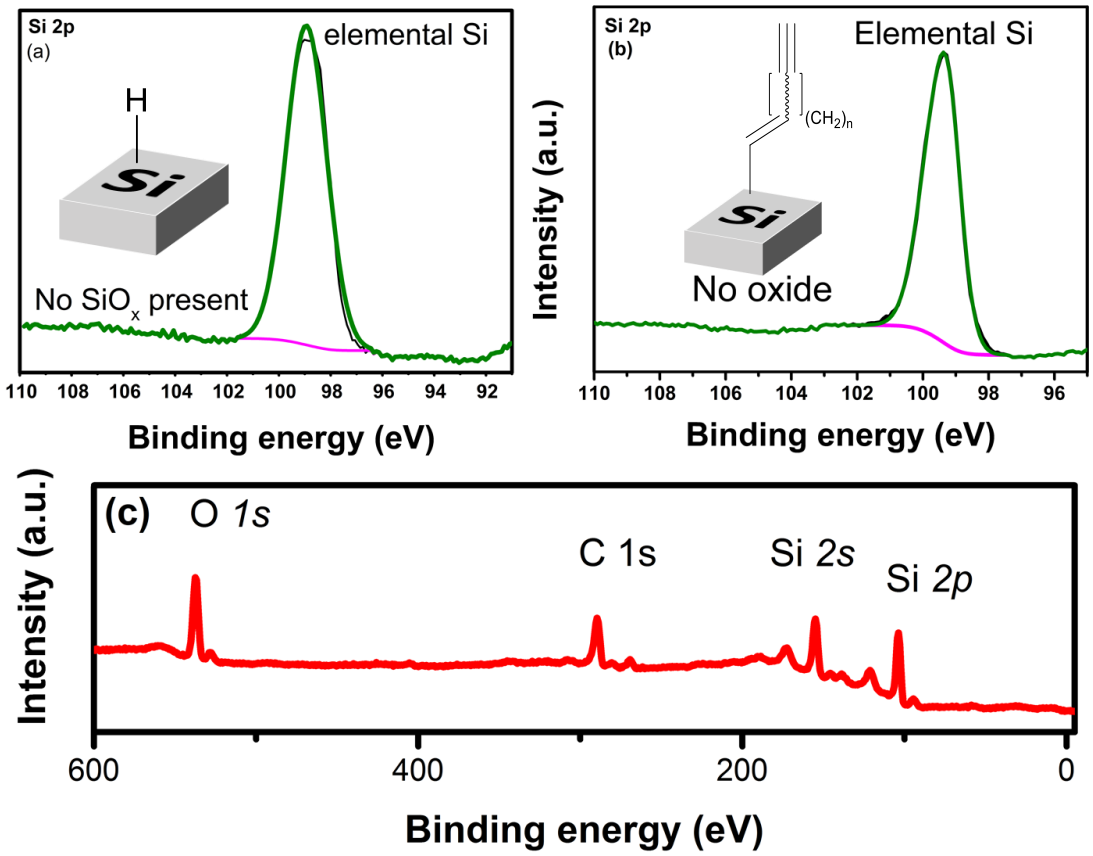


Figure 4.2 (a) displays a Si surface after a standard RCA clean and HF etch. (b) showing the same silicon surface functionalised with 1,7 octadiyne. The surface has no presence of oxide when compared to the HF-etched sample shown in (a). The survey spectrum shown in (c) shows the presence of Si, C and O which is indicative of the presence of an organic monolayer. The intensity of the O peak may be attributed to adventitiously adsorbed O during transport to the UHV environment of the XPS spectrometer.

The C *1s* core-level scan of 1,7-octadiyne functionalised Si showed a broad feature centred at ~285 eV that is consistent with chemical contributions from Si and C bonded carbon atoms. This well-ordered 1,7-octadiyne functionalised Si surface was subsequently functionalised with the DPPA molecule *via* the copper-catalysed azide-alkyne cycloaddition. **Figure 4.3(a)** shows a survey scan of a DPPA functionalised Si sample showing the appearance of a N *1s* signal at approximately 400 eV when compared to Figure 4.1 (c). P *2p* and N *1s* signals were observed in the functionalised substrate which were absent from Figure 4.1 (c). **Figure 4.3(b)** shows a C *1s* core level spectrum for a substrate after attachment of the P-containing azide. Deconvolution of the C *1s* core level spectrum, shows a peak at 285 eV attributed the aliphatic primary passivation layer. A peak centred near 287 eV indicates the presence of a C-N moiety and tentative evidence for the formation of the [1,2,3]-triazole ring which is characteristic of the alkyne-azide cycloaddition. The presence of a small peak at 288 eV, typically assigned to C=O species, may be attributed to adsorbed organic solvent from the post-reaction washes.

Successful attached of the dopant molecule through the formation of a [1,2,3]-triazole ring is confirmed by the N *1s* core-level scan shown in **Figure 4.3(c)** .[38,39] A large, broad peak primarily centred at 401 eV on the N *1s* spectrum is indicative of the presence of distinct nitrogen environments which strongly support the bonding of the azido group to the terminal alkyne. The small satellite peak centred near 405 eV, may be associated with adsorbed DPPA species.[40]

Due to the overlap of the Si *2p* plasmon with the P *2p* photoelectric line, it is not trivial to determine the presence of P on the surface using XPS alone but the presence of the DPPA molecule on the surface can be determined indirectly using the C *1s* and N *1s* core level spectra. XP spectra showed no evidence of Cu *2p* peaks, typically observed

at binding energies of 932 eV and 952 eV respectively, showing complete removal of the copper catalyst post-reaction and prior to the rapid-thermal-anneal treatments.[41]

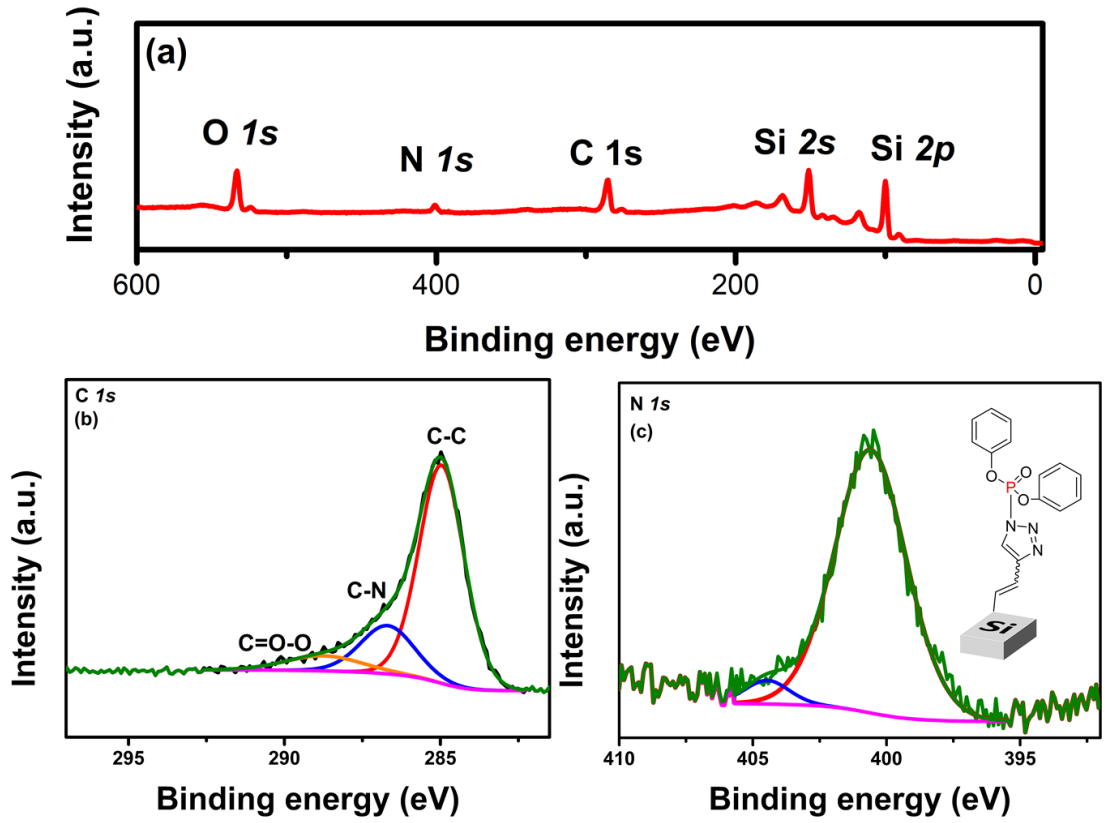


Figure 4.3. (a) shows a survey spectrum containing a N *1s* signal which is absent from the survey scan shown in Figure 4.1 (c), showing tentative evidence for attachment of the DPPA molecule (b) C 1s spectrum after functionalisation of the terminal alkyne. Chemical moieties are indicated. (c) the N *1s* spectrum showing the presence of the triazole moiety.

4.3.2 Assembly of 1,7 Octadiyne Monolayers on the H-terminated Si (100) Surface and Subsequent Functionalisation with Arsenic Azide

A strategy analogous to that used in the functionalisation of Si (100) with the DPPA molecule was performed using the synthesized arsenic azide (AA). **Figure 4.4** shows an XPS survey spectrum indicating the presence of Si, C, O and As which is indicative of an AA functionalised surface.

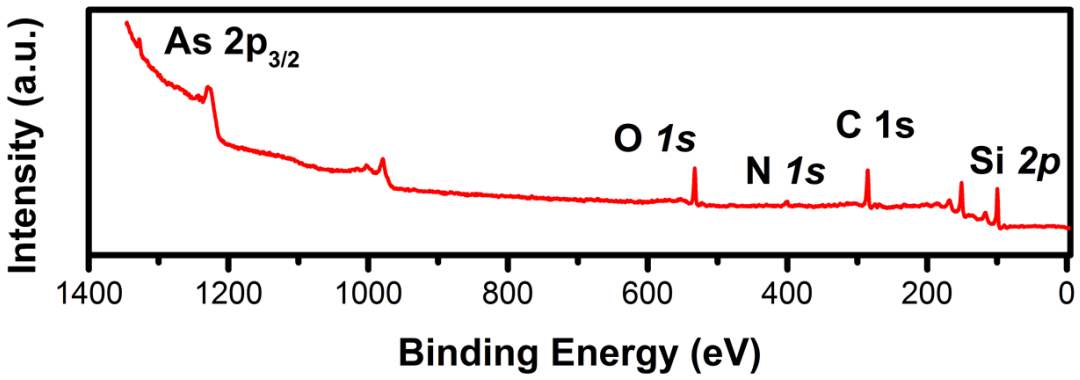


Figure 4.4 – Survey spectrum of an AA functionalised Si surface, showing the presence of N *1s* and As *2p* signals indicative of an AA-functionalised surface.

Figure 4.5(a) shows a Si *2p* core level scan of a Si substrate functionalised with 1,7-octadiyne, followed by attachment of the AA molecule *via* an alkyne-azide cycloaddition. A small level of oxide (< 1 at.%) was observed which may be associated with traces of water from the sodium azide activation procedure.[42] The low amount of oxide detected did not significantly impact on the incorporation of surface dopant.[43] **Figure 4.5(b)** displays a C *1s* core level spectrum of the AA functionalised surface. Similar to the DPPA functionalised substrate, the spectrum consists of a broad peak centred at 285 eV which indicates the presence of C-C bonds. A smaller feature centred at ~287 eV shows the presence of a C-N structure consistent with the establishment of a [1,2,3]-triazole aromatic ring.[44] The binding energy is in good

agreement with previous C-N binding energy values reported by Böcking *et al*. Figure 4.4 (c) shows the N *1s* core level spectrum deconvoluted into two peaks. A broad peak centred at ~401 eV can be assigned to the different chemical environments of the N atoms in the triazole ring, which was fitted using similar parameters to the DPPA functionalised surface shown in Figure 4.2 (b) to confirm successful coupling of the azide to the terminal alkyne. The second feature at ~ 405 eV is chemically shifted by ~ 4 eV with respect to the primary peak, which is indicative of inorganic N species. This may be attributed to the electron-deficient nitrogen of the azide group.[45] Figure 4.4 (d) shows the As *2p* core level scan after functionalisation with the AA molecule. The peak at approximately 1328 eV is shifted to a higher binding energy with respect to the elemental arsenic binding energy of ~1323 eV.[46] Since photoelectric lines related to Cl were not detected, the presence of $AsCl_3$ on the surface was excluded.

Assuming the alkyne-azide cycloaddition occurs at one out of the three azide groups on the AA molecule, this shift in the binding energy may be attributed to the highly electron-deficient nature of the two remaining azide groups bonded to the arsenic of the AA molecule.

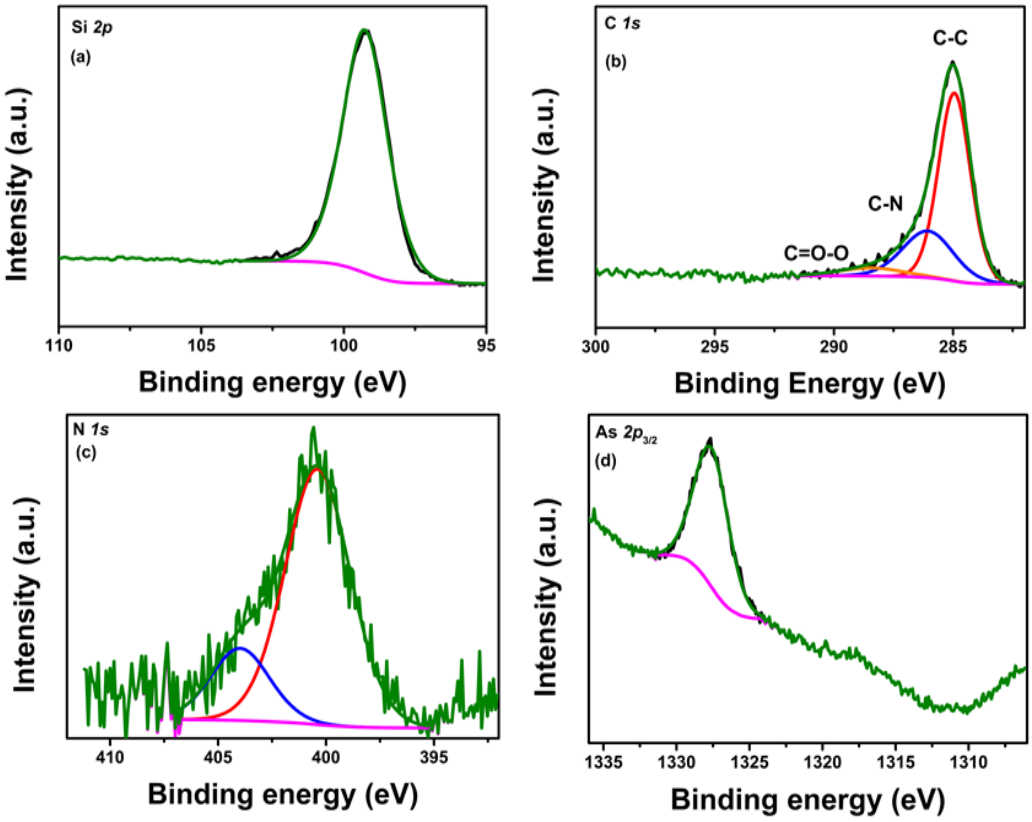


Figure 4.5. Figure 4.5 (a) displays the Si *2p* core level scan for a AA-functionalised Si substrate. (b) shows the deconvoluted C *1s* core level spectrum of a Si sample functionalised with 1,7-octadiyne and subsequently derivatised with the arsenic azide molecule with components corresponding to C-C and C-N moieties labelled (c) showing the N *1s* core level spectrum from the same sample showing a primary peak centred at ~401 eV indicative of the triazole ring formation and satellite peak at ~405 eV signifying the presence of azide groups, (d) an As $2p_{3/2}$ core level scan showing the presence of As on the surface post-reaction.

4.3.3 Stability of the functionalised samples toward ambient conditions

The stability that is inferred on Si surfaces by grafted monolayers is interesting for many applications. With respect to device integration, regrowth of Si oxides prior to rapid-thermal-anneal treatment and other important steps in CMOS processing is not desirable, especially in the moments immediately after a processing step. Surface functionalisation greatly increases the oxidation resistance of Si.[47] To ascertain the stability of the "click" functionalised samples towards ambient conditions, substrates were left exposed to ambient conditions (air, 20 °C) for periods of time ranging from 24 h to one month. Prior to analysis the samples were rinsed with chloroform to remove adventitiously adsorbed material from the surface. The Si *2p* core level scan was used to monitor for an increase in oxide formation. The acquired stability spectra for the DPPA functionalised samples are shown in **Figure 4.6(a-d)**. Comparative spectra for the blank, non-functionalised Si substrates are shown in **Figure 4.7(a-d)** The DPPA-functionalised substrates exhibited excellent resistance towards re-oxidation when compared to the non-functionalised Si substrates, especially 24 h immediately after functionalisation. This stability can be attributed to the tight packing of the initially grafted alkyne layer. **Figure 4.8(a-d)** compares the Si *2p* XPS spectra for AA functionalised samples, acquired immediately after preparation and after exposure to ambient conditions ranging from 24 h, 1 week and 1 month. These samples also displayed strong resistance towards re-oxidation in comparison to the non-functionalised Si substrate. In addition to the influence of the tightly packed alkyl chain on these substrates, the increased oxidation resistance could be attributed not only to the smaller molecular footprint of the AA molecule allowing improved packing post-functionalisation, but also to the use of the alkyne primary passivation layer. These short chain linear molecules have excellent stability and packing characteristics.

In addition, especially in the case of DPPA, the π-π interactions between the two aromatic rings on adjacent DPPA molecules on the surface greatly improve molecular packing to ensure the underlying Si substrate is protected.[3]

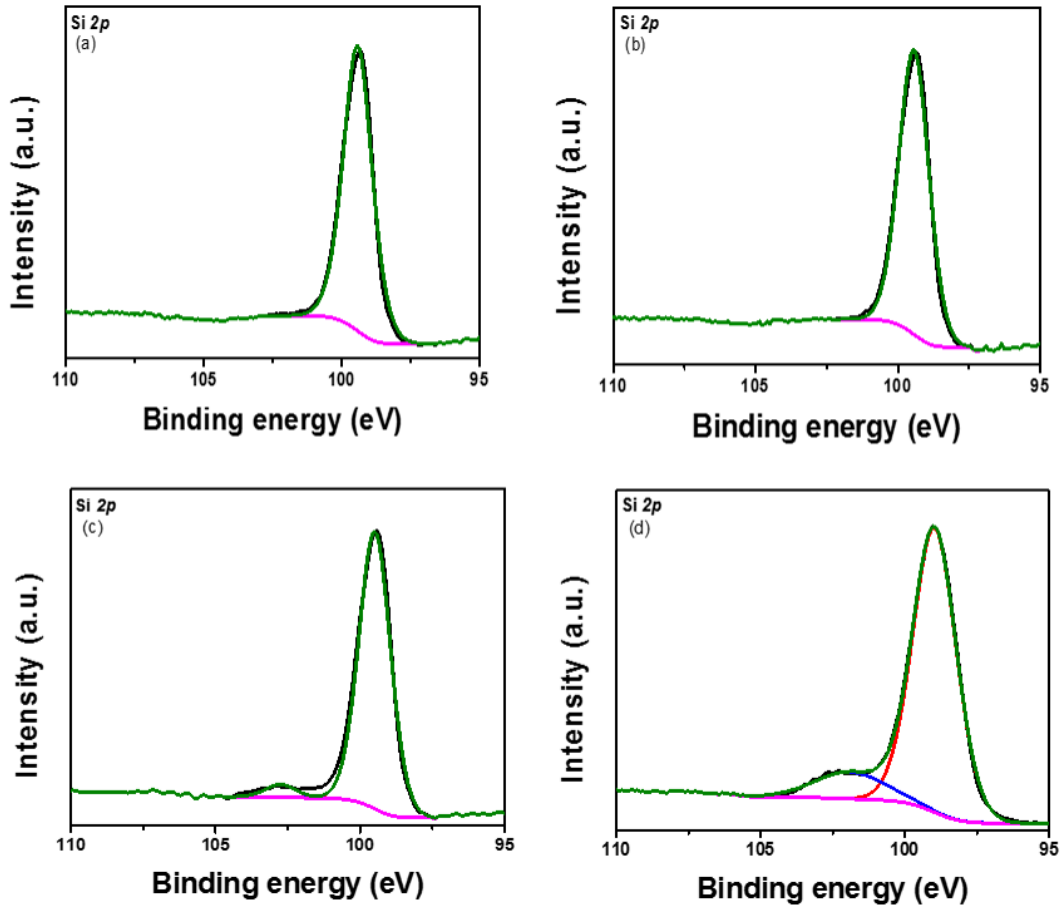


Figure 4.6. High resolution Si 2p core level spectra of a DPPA-functionalised silicon substrate left out in ambient conditions for comparison purposes. (a) Freshly cleaned and etched substrate characterised immediately. (b) Spectrum acquired after 24 h. (c) Spectrum acquired after 1 week and (d) spectrum acquired after 1 month under ambient conditions.

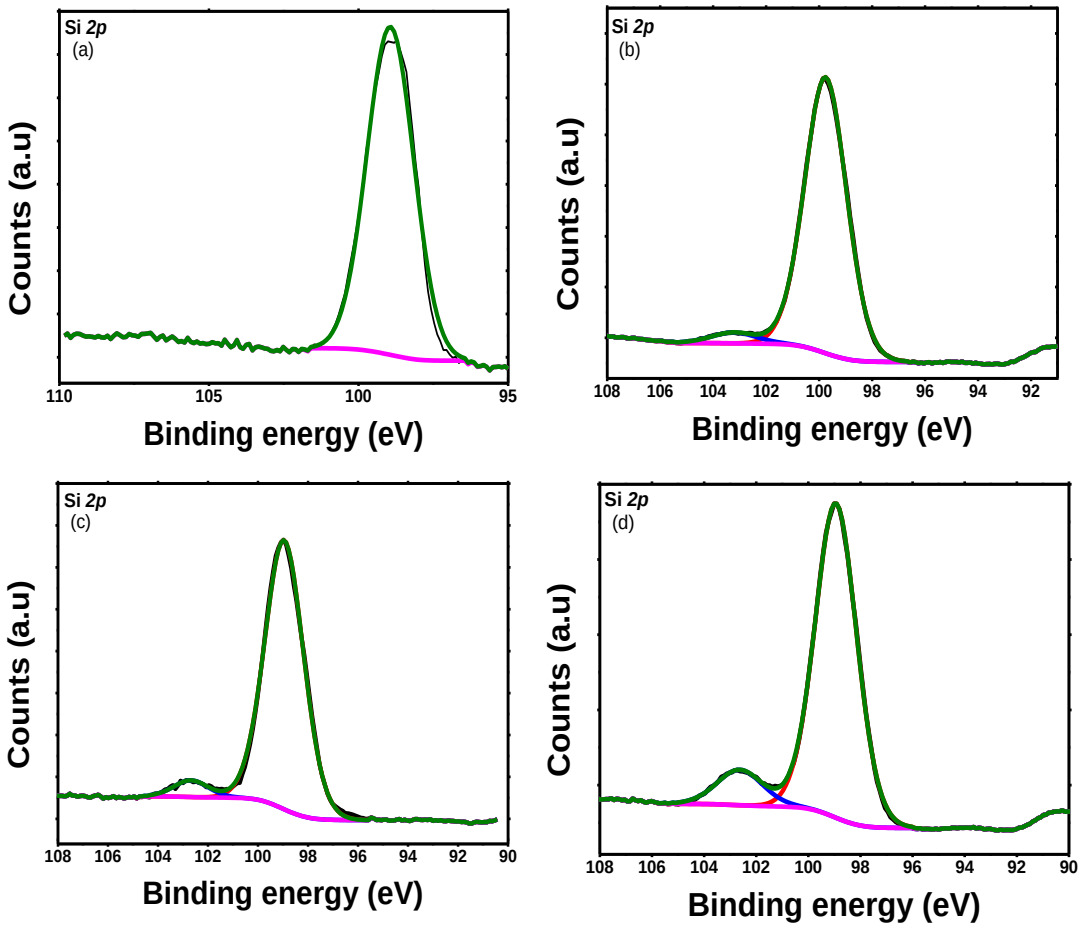


Figure 4.7. High resolution Si 2p core level spectra of a non-functionalised silicon substrate left out in ambient conditions for comparison purposes. (a) Freshly cleaned and etched substrate characterised immediately. (b) Spectrum acquired after 24 h. (c) Spectrum acquired after 1 week and (d) spectrum acquired after 1 month under ambient conditions.

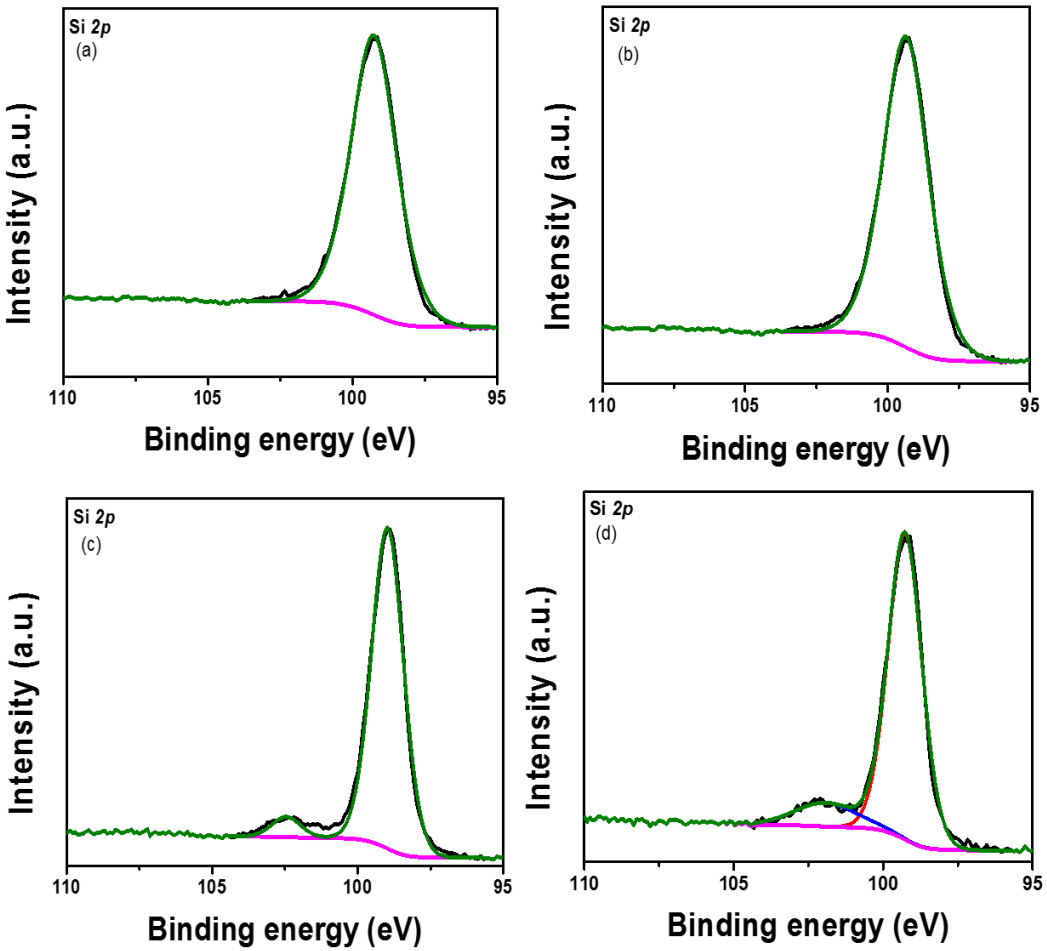


Figure 4.8. High resolution Si 2p core level spectra of a AA functionalised silicon substrate left out in ambient conditions for comparison purposes. (a) Freshly functionalised substrate characterised immediately. (b) Spectrum acquired after 24 h. (c) Spectrum acquired after 1 week and (d) spectrum acquired after 1 month under ambient conditions.

4.3.4 Carrier profiling

Samples were capped with a 50 nm layer of SiO_2 *via* sputtering and transferred to a rapid-thermal-anneal tool where the substrates were subjected to a 5 s anneal at 1050 ^{o}C, based on parameters from previous work, under a nitrogen atmosphere. The cap was removed using a buffered-oxide-etch at 20 ^{o}C and samples were cleaned by sonication in chloroform and toluene prior to electrochemical capacitance-voltage (ECV) analysis. The specific composition of the capping layer and the method used for depositing the capping layer can change the monolayer integrity and may influence the diffusion process, but the effect of the capping layer was not studied in this work.

To compare the "click" functionalisation strategy used in this work to a traditional phosphorus MLD approach, which typically uses a hydrosilylation reaction between the Si-H surface and an organic carbon-based dopant-containing molecule, a Si sample was functionalised with a non-azide precursor, allyldiphenyl phosphine (ADP) *via* a thermally-induced hydrosilylation reaction according to the procedure represented in **Figure 4.9**. The experimental parameters are outlined in the Experimental chapter. This molecule was chosen as it is structurally similar to the diphenylphosphoryl azide molecule employed in the CuAAC click reaction but does not contain an azide functional group; instead undergoing a hydrosilylation reaction between the H-terminated Si surface and C=C labile site on the ADP molecule The RTA parameters were kept identical for the two samples.

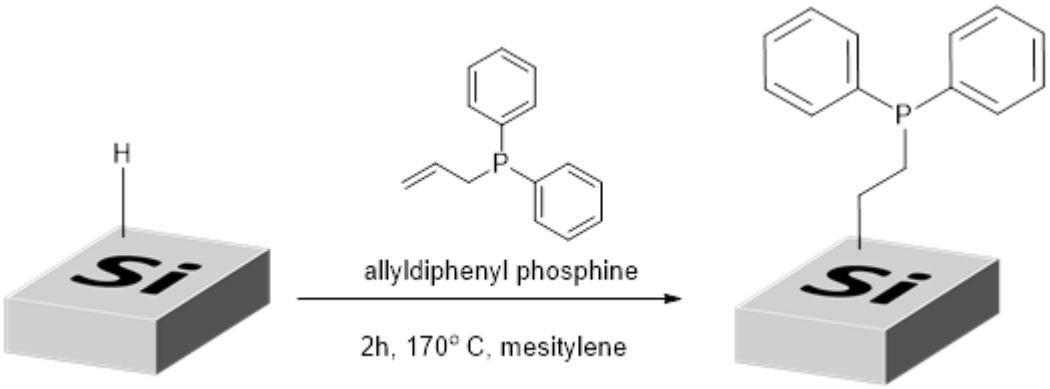


Figure 4.9. Schematic representing the reaction of allyldiphenyl phosphine (ADP) with H-terminated Si (100) surface. The Si surface is first degreased and cleaned using RCA washes and then etched with HF to give a H-terminated surface. The substrate is then immersed in a solution of ADP in mesitylene for 2h at 170°C. After a post-reaction clean in anhydrous solvents the substrate is functionalised with ADP.

Figure 4.10(a) displays an ECV profile of a DPPA functionalised Si substrate which has been thermally treated using RTA. As can be seen from the profile, the peak active carrier concentration was approximately 1×10^{19} atoms/cm^3 with the highest concentration at depths less than 25 nm. **Figure 4.10(b)** shows the ECV profile for a Si substrate which has been functionalised with ADP and subjected to the same RTA recipe as the DPPA-functionalised sample. The ECV profiles for surface prepared by the click chemistry method and the MLD method are quite similar with both exhibiting a peak active carrier concentration of 1×10^{19} atoms/cm^3. This similarity between carrier concentrations may be attributed to the packing characteristics of the DPPA and ADP molecules.

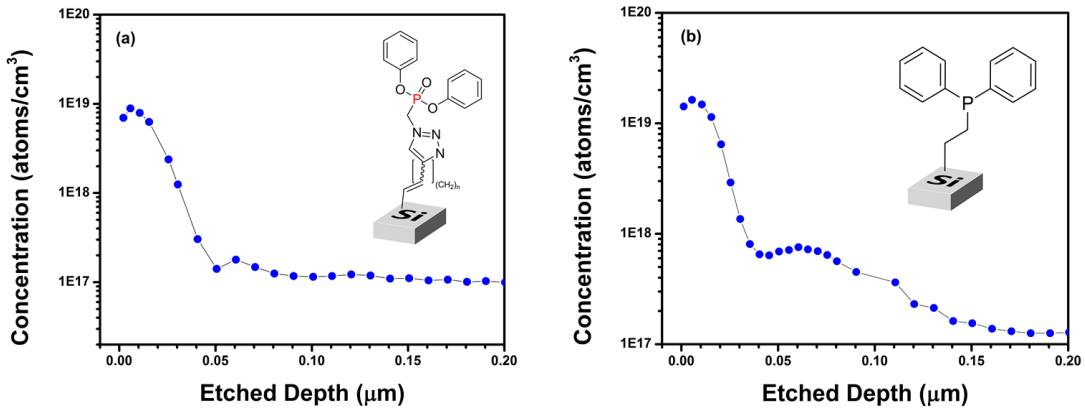


Figure 4.10 - ECV profiles for (a) a sample functionalised with DPPA and subsequently thermally annealed at 1050°C for 5 s and (b) ADP and then subsequently subjected to rapid-thermal-anneal treatment at 1050°C for 5 s. Both samples exhibited similar dopant profiles with peak concentrations at approximately 1E19 atoms/cm^3 measured with highest concentrations occurring at shallow depths less than 25 nm.

Additionally, as shown in **Figure 4.11**, the ADP-functionalised surface oxidized more quickly in ambient conditions, especially within the first 24 h, when compared to the Si samples which had initially been functionalised with the dialkynes. As they are structurally similar, packing densities and conformations would be expected to be quite close, leading to monolayers with near identical steric features. Samples were prepared using dialkynes varying in length between six carbons and ten carbons with each chain being functionalised subsequently with the DPPA molecule using identical conditions each time. No difference in carrier concentration was observed for samples with the shortest carbon chain lengths and the longest carbon chain lengths. This shows that using a primary passivation layer in conjunction with the dopant-containing molecule allows for much improved oxidation resistance without affecting the diffusion of the dopant atoms.

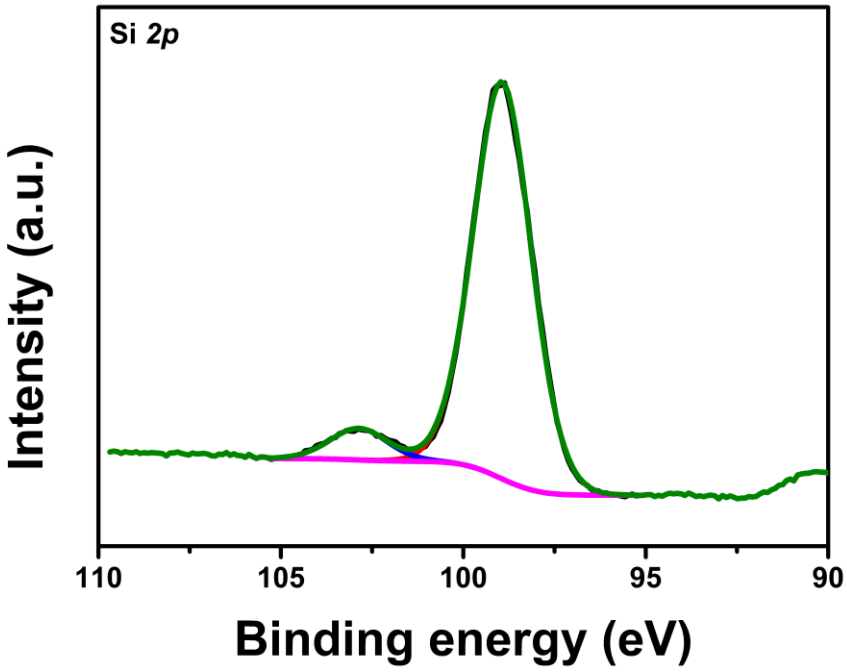


Figure 4.11 – A Si sample functionalised with ADP after 24 h in ambient conditions. When compared to the DPPA-functionalised samples shown in Figure 4.5, the sample does not exhibit the same stability towards reoxidation as those functionalised via the click-chemistry route.

Similar rapid thermal anneal treatments were applied to the Si substrates which were functionalised using the arsenic azide molecule. Characterisation of these surfaces *via* ECV analysis was challenging as the resultant light doping was not amenable to efficient etching for the depth profiling. **Figure 4.12** shows the ECV profile of an AA-functionalised Si substrate thermally treated using RTA for 5 s at 1050 ^{o}C. Peak carrier concentrations approached 2×10^{18} atoms/cm^3 at depths of less than 25 nm.

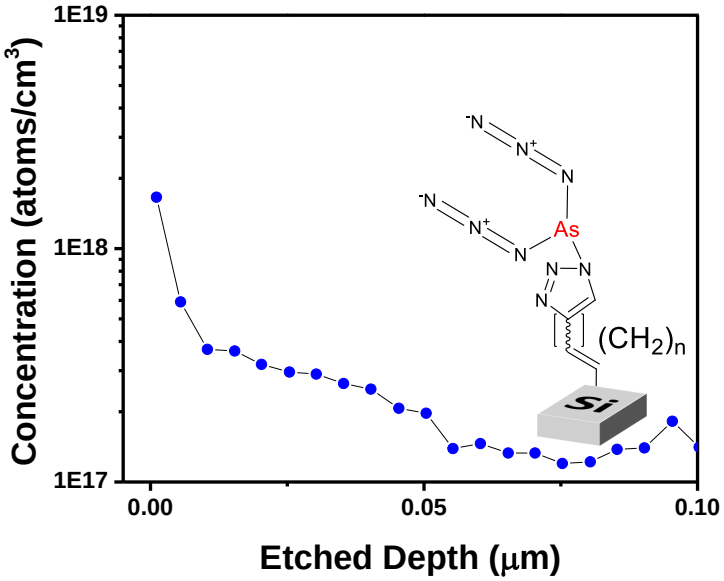


Figure 4.12. ECV profile for a sample functionalised with 1,7-octadiyne and subsequently functionalised with the AA molecule. The substrate was capped and subjected to rapid-thermal-anneal treatment at 1050 ºC for 5 s. The sample exhibited a peak concentration approaching 2×10^{18} atoms/cm^3 with peak concentrations occurring at shallow depths less than 20 nm. Inset represents the AA-functionalised surface

MLD on Si using a traditional carbon-based As-containing precursor in conjunction with a thermally-initiated hydrosilylation reaction has been reported and achieved excellent in-diffusion coupled with high chemical concentrations approaching 2×10^{20} atoms/cm^3.[43] The lower carrier concentration for arsenic observed in this work is unlikely due to diffusion suppression. Nitrogen has been reported to supress diffusion of As in Ge[48] and also suppression of B in Si[49] but has not been reported to suppress the diffusion of As in Si. The lower observed carrier concentration is more likely to be attributed to poor yields of the alkyne-azide fusion reaction. The effect of steric constraints is well known from solution-based chemistry especially for larger

molecular systems.[50] In this study, the effect is more pronounced due to one end of the alkyne being anchored to the surface of the Si[51], which requires the arsenic azide molecule to approach the terminal alkyne at a certain orientation. To obtain higher carrier concentrations requires the close packing of the azides on the surfaces. Despite the small molecular footprint of the arsenic azide molecule, the highly charged and linear structures of azide groups attached to the arsenic may introduce steric effects at the interface that do not allow for close packing. This effect is somewhat negated on the DPPA molecule due to the presence of only one azide group, with the packing densities dominated by the large heteroaryl moieties present. The "click" reaction yield between the arsenic azide and acetylene-terminated Si surface was estimated by comparing the C-N/C-C elemental ratios as obtained from XPS measurements. In order to simplify the curve-fitting needed to make the estimate, the C-O and C-N components were represented by one peak at approximately 286.5 eV, with the ratio reflecting the amount of arsenic azide attached to the acetylene-terminated surface, using a method described by Li *et al*.[52] An elevated temperature of 70 ^{o}C was used in an attempt to increase the yield. Using this method, a 59 % conversion yield was estimated for the reaction between arsenic azide and the acetylene-terminated Si surface. This may be attributed to the sterically-hindered nature of the rigid and charged azide groups on the arsenic azide molecule. Light As doping may be of use for applications in devices where low defect densities are required to minimise dark currents such as high operating temperature detectors and low-capacitance photodiodes for electron detection.[53,54] Similarly to the DPPA-doped substrates, there was no discernible difference in carrier concentrations for samples with the shortest carbon chain lengths and the longest carbon chain lengths.

4.4 CONCLUSIONS

Controlled doping at the nanoscale has become progressively more difficult in recent years as device feature sizes have reduced. There is a need for innovative and reliable methods for the doping of Si while preventing significant re-oxidation of the underlying substrate. Si was successfully functionalised with di-alkynes with chain lengths between 6 and 10 carbon atoms and then subsequently functionalised *via* a copper-catalysed azide-alkyne cycloaddition reaction to give a dopant-containing monolayer on the surface. XPS spectra contained signals referring to the [1,2,3]-triazole ring formation indicating successful incorporation of the dopant-containing azides to the terminal acetylene groups. ECV measurements confirmed successful diffusion of the dopants into the Si substrate with the P-doping process being most effective. The substrates also exhibited excellent resistance toward re-oxidation especially in the immediate 24 h post-functionalisation. The experimental procedure is robust, particularly the dopant molecule introduction *via* the Huisgen 1,3-dipolar cycloaddition. The procedure is insensitive to reaction conditions that would halt traditional MLD reactions such as the presence of trace water and oxygen. The presence of either could potentially oxidise the Si surface and affect the attachment of the dopant-containing monolayer and allows for the introduction of dopant-containing moieties using milder reaction conditions than previously reported. This work also utilised the beneficial application of tightly-packed terminal acetylene monolayers which provide the aforementioned increased resistance to oxidation.

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Chapter 5

Liquid-phase Monolayer doping of InGaAs with Si-containing and Sn-containing molecular layers

This chapter has been prepared as a manuscript for submission to a peer-reviewed journal. Consequently, certain sections of the chapter may contain repeating concepts and paragraphs.

5 Liquid Phase Monolayer Doping Of InGaAs With Si-Containing And Sn-Containing Molecular Layers

5.1 Abstract

The functionalisation and subsequent monolayer doping of InGaAs substrates using a tin-containing molecule and a molecule containing both and silicon and sulfur was investigated. Epitaxial InGaAs layers were grown on semi-insulating InP waters and functionalised with both sulfur and silicon using mercaptopropyltriethoxysilane (MPTES) and with tin using allyltributylstannane (ATBS). The functionalised surfaces were characterised using X-ray photoelectron spectroscopy (XPS). The surfaces were capped and subjected to rapid-thermal annealing causing in-diffusion of dopant atoms. Dopant diffusion was monitored using electrochemical capacitance-voltage measurements and secondary ion mass-spectrometry characterisation. Raman scattering was also utilised to non-destructively determine the presence of dopant atoms, prior to destructive analysis, by comparison to a blank undoped sample. Additionally, due to the As-dominant surface chemistry, the resistance of the functionalised surfaces to oxidation in ambient conditions over periods of 24 hours and 1 week was elucidated using XPS by monitoring the As *3d* core-level for the presence of oxide components.

5.2 INTRODUCTION

InGaAs is a potential future channel material for complementary metal-oxide semiconductor (CMOS) applications due to its direct band gap and high electron mobility.[1-6] With device feature sizes perennially decreasing and a move from SiO_2-based gate dielectric strategies ongoing, new methods for passivating and doping of InGaAs based materials will become more important if the material is to become integrated in future technology nodes. Metal-oxide-semiconductor field-effect transistors (MOSFETs) based on InGaAs will allow continued scaling through a reduction in operation voltage and device footprints without compromising performance. Source and drain (S/D) doped III-V MOSFET devices are still attracting considerable attention. Advanced III-V based CMOS processes and technologies require ultra-thin body channel materials to maintain minimal junction and gate leakage and to reduce short channel effects. S/D regions with increased thickness will also be required to further reduce access resistances. Si and Sn are typical dopants of choice for n-type doping of InGaAs. Doping of InGaAs conventionally takes place either *in-situ* by introduction of a dopant-containing gas during epilayer growth, by ion-implantation post-growth, or in the case of a device such as a MOSFET, selective epitaxy on each side of the gate of *in-situ* doped source/drain materials using the channel material as a seed layer. Typically the highest temperature step for an InGaAs MOSFET fabrication process approaches 550 °C. From a device fabrication perspective it is desirable to reduce the thermal budget as much as possible, while maintaining high carrier concentrations. For this reason, Sn is the preferred n-type dopant at such temperatures, as active carrier concentrations above 5×10^{19} atoms cm^{-3} can potentially be achieved for relatively low epitaxy thermal parameters.[7] However, Si doping may still be more desirable due to its compatibility with front-end CMOS

process. More pertinently, the limited diffusivity of Si in InGaAs would prove beneficial if high-concentration, ultra-shallow junctions are to be realised, especially in the case of nanostructures.

Conformal doping of nanostructures becomes challenging especially for 3D structures as dimensions are scaled down. Established methods for doping, such as ion-implantation, suffer from several drawbacks at the nanoscale such as stochastic dopant distributions, inability to control the abruptness to within a nanometre and, most importantly at the nanoscale, beam-induced damage in the case of devices. Monolayer doping (MLD), a technique to controllably dope semiconductor surfaces and nanostructures at shallow depths, has been applied successfully to Si and Ge using a range of functionalisation and dopant recipes.

A typical MLD process combines the rich surface chemistry of semiconductors[8-11] with the self-assembly of dopant containing molecules on a semiconductor surface. This surface is then capped, to prevent desorption of the chemisorbed monolayer, and annealed using a rapid-thermal-anneal process to yield shallow, high-concentration dopant profiles. MLD has already been shown to be a suitable technique for the shallow doping of Si and Ge devices with complex and non-planar geometries, allowing fine control over dopant profiles.[12-26]

The functionalisation of semiconductor surfaces can also enhance the resistance of surfaces towards oxidation. Due to the challenging surface chemistry of InGaAs and other III-V materials, the application of MLD has been quite limited. There have been reports of direct bonding to oxide-free III-V surfaces using organic thiols[27-31] and due

to the simplicity of the procedure and availability of suitable commercial molecules, this was one of the approaches used in this study. Solution-phase S doping of InGaAs has been relatively widely reported due to the simplicity of the procedure.[32-36] Ammonium sulfide is often used to remove the native oxides on InGaAs but the process conveniently results in a S-terminated surface, allowing diffusion of S as a monolayer into the InGaAs surface *via* a rapid thermal anneal step. While not a traditional MLD process, due to the gas-phase dopant precursor and high-vacuum requirements of the deposition process, Kong and co-workers recently reported the Si MLD of InGaAs nanostructures by means of a MOCVD-deposited silane layer with a thickness of a few monolayers. [37,38] Enabling precision control over dopant profiles in III-V materials remains a challenge to be overcome if the high carrier mobilities are to be exploited in highly-scaled device architectures.

In this Chapter, I report for the first time, the functionalisation of epitaxially grown InGaAs layers, using a typical liquid-phase MLD procedure; a Si-containing thiol and an Sn-containing organometallic molecule. Surface chemistry at the InGaAs surface was characterised using XPS. The presence of dopants in the processed samples was non-destructively ascertained by means of Raman scattering. Dopant diffusion and activation was monitored using ECV characterisation in tandem with SIMS to measure the total chemical concentration of the dopants. A schematic illustrating the chemical functionalisation process is shown in **Figure 5.1**.

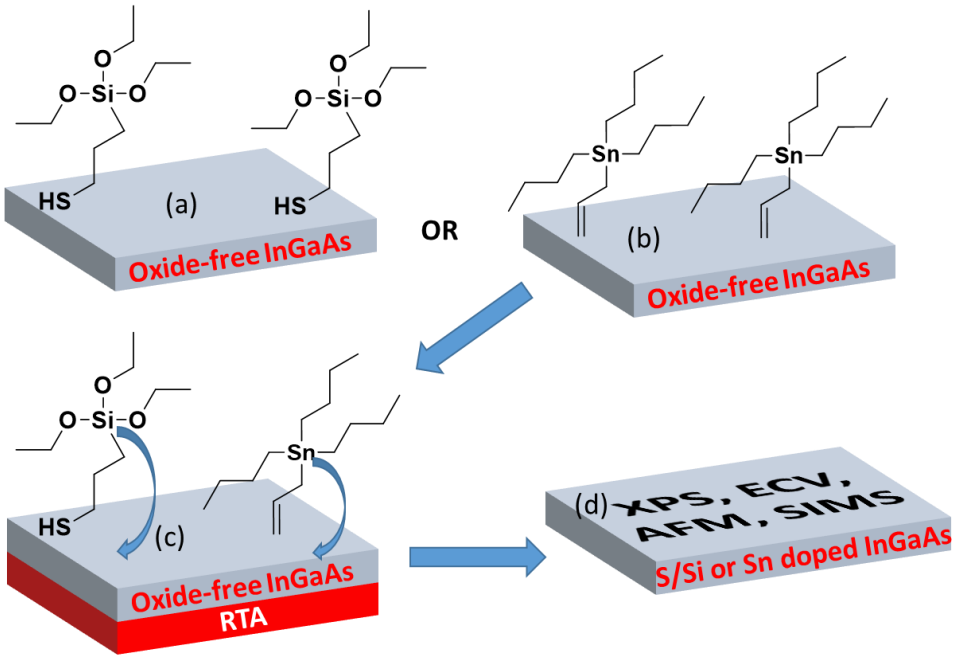


Figure 5.1. General schematic for the InGaAs MLD process applied in this work. (a) An oxide-free InGaAs surface was functionalised with 3-mercaptotriethoxysilane (MPTES) or (b) allyltributylstannane (ATBS). (c) The functionalised substrates were capped with SiO_2 and annealed in a rapid-thermal-anneal furnace to cause in-diffusion of the dopant atoms to yield (d) doped InGaAs substrates.

5.3 Results and Discussion

5.3.1 Modification of the oxide-free InGaAs surface with 3-mercaptopropyltriethoxysilane (MPTES)

The functionalisation procedure is outlined in detail in Chapter 2 of this thesis. Si is one of the most popular dopants for InGaAs, especially when introduced *via* ion implantation and *in-situ* growth. Significantly, Si has a sticking coefficient approaching unity and very low diffusivity making the doping of InGaAs using Si attractive for devices that require high doping concentrations and sharp, shallow doping profiles. Si exhibits amphoteric behaviour in InGaAs leading to complications in determining active carrier concentrations as Si can act as both an *n*-type and *p*-type dopant. Hence, the concentration of conducting electrons is typically less than the number of silicon dopant atoms and it is challenging to achieve a free carrier concentrations in 10^{19} range. XPS characterisation was conducted on all samples to determine if MPTES chemisorbed on the surface of InGaAs and also to investigate whether or not the sample oxidised during the functionalisation process. Each sample was sonicated in anhydrous ethanol prior to insertion into the UHV atmosphere of the XPS spectrometer. **Figure 5.2** shows a XPS As *3d* core-level spectrum for (a) an as-received, cleaved InGaAs wafer, (b) an oxide-free InGaAs wafer and (c) an-oxide free InGaAs surface that has been functionalised with the MPTES molecule. Figure 5.2(a) shows a primarily a peak at 40 eV which is indicative of unoxidised elemental As from InGaAs.[39] A shoulder peak chemically shifted to approximately 44 eV is present which is representative of oxidised arsenic species.[40]. Shown in Figure 5.2(b) is an XPS spectrum of the same sample analysed immediately after a NH_4OH etch to remove the native oxides. The spectrum is dominated solely by the elemental arsenic peak, showing effective native oxide removal at the surface. Figure 5.2(c) shows the

XPS spectrum of same sample after immersion in a 25 % v/v solution of MPTES in IPA for 24 h. The spectrum exhibits only a peak at 40 eV showing the presence of non-oxidised As as part of an-oxide free InGaAs surface. This highlights that despite the long substrate immersion times, no oxide has regrown on the surface post-functionalisation.

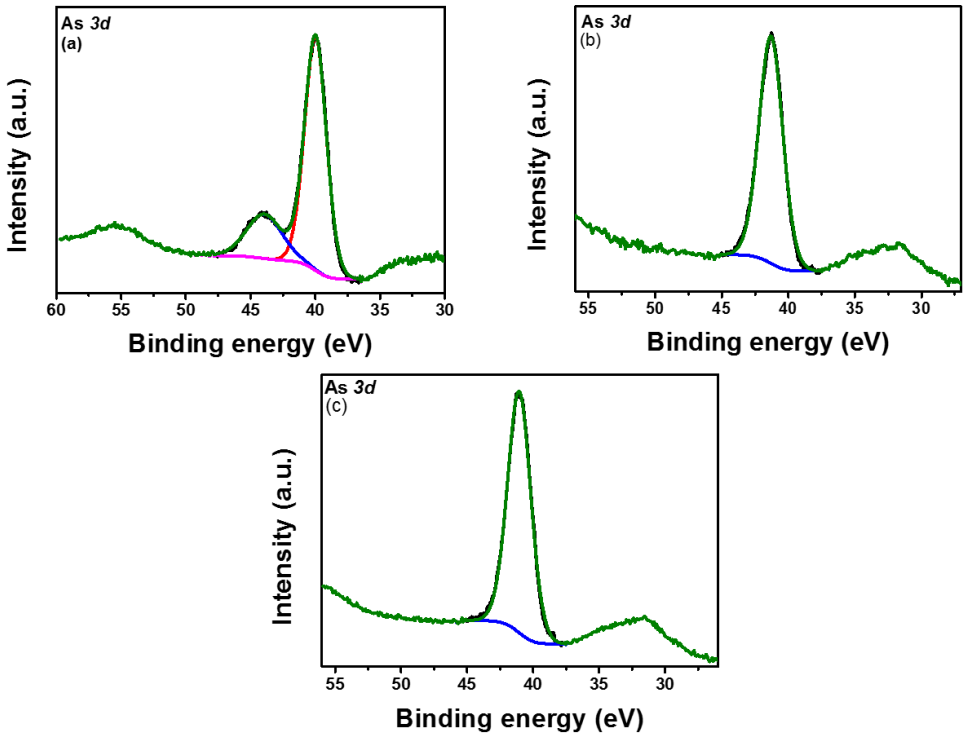


Figure 5.2. XPS spectra of the As 3d core level depicting the surface chemistry for (a) an as-received InGaAs substrate, (b) a InGaAs substrate freshly etched with ammonium hydroxide and (c) a InGaAs substrate functionalised with MPTES. The large oxide component present at 44 eV in (a) disappears after the ammonium hydroxide etch and remains absent in the functionalised substrate, highlighting that the functionalisation process did not increase the amount of As oxides on the surface.

Figure 5.3 shows survey spectra for the as-received wafers, oxide-free wafers and samples that have been functionalised with the MPTES molecule.

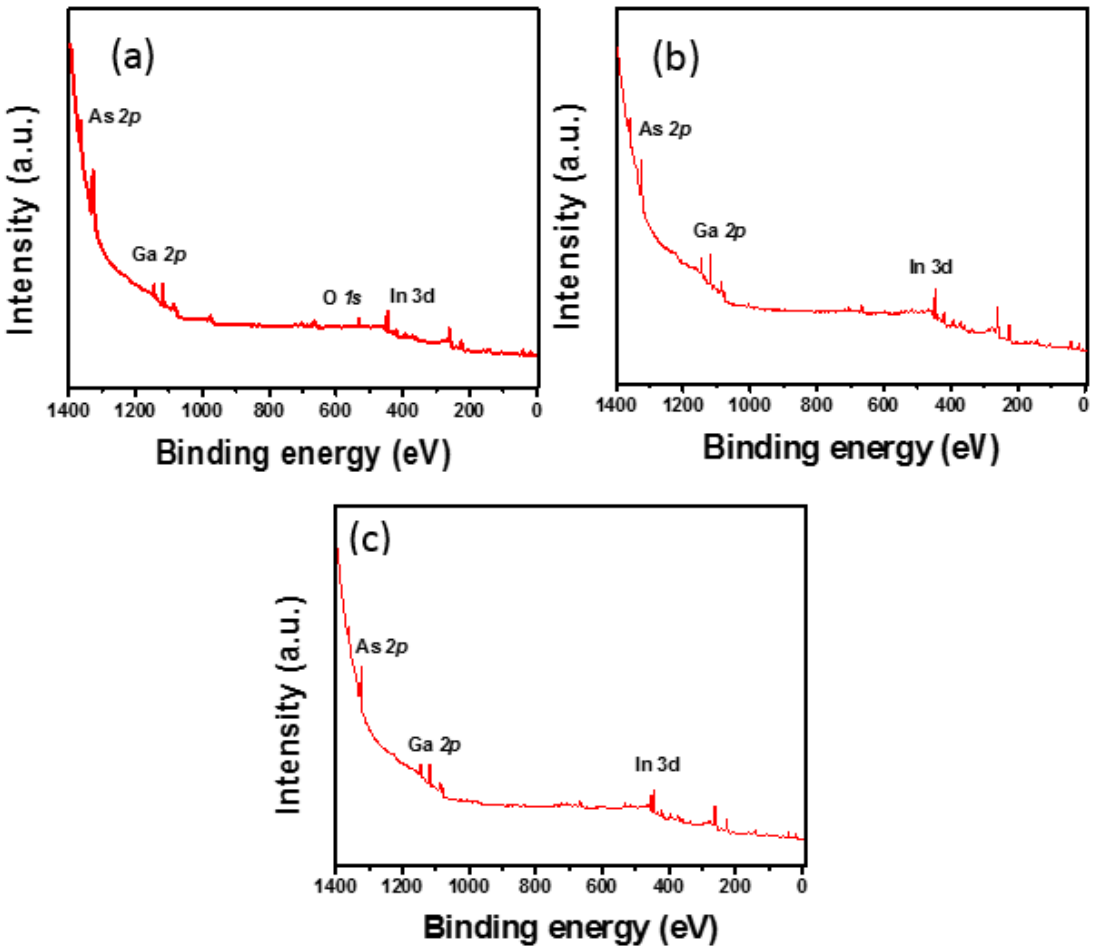


Figure 5.3. XPS survey spectra for (a) an as-received InGaAs substrate, (b) an ammonium hydroxide etched InGaAs substrate and (c) a substrate that has been functionalised with MPTES. The O 1s peak is absent in (b) and (c) showing that the substrate remained oxide-free post-cleaning and post-functionalisation.

Figure 5.4(a) shows the combined XPS As *3p*, S *2p* and Ga *3s* core level scans of the MPTES functionalised substrate. The component at approximately 161 eV can tentatively be attributed to the presence of S in a thiolate form which would be consistent with direct S-substrate bonding of the MPTES molecule.[41] Instrumental

resolution was limited in the experiments due to the use of a non-monochromated X-ray source which precludes further resolution of this thiolate peak to determine if the bonding mode is Ga-S or As-S. Nevertheless, the presence of S on the surface after copious post-reaction washing would imply that the MPTES molecule had successfully bonded to the oxide-free InGaAs surface. **Figure 5.4(b)** shows the C *1s* core-level scan of the MPTES-functionalised surface. The main component shown in red at 285 eV represents a combination of adventitiously bound carbon as well as C-C moieties from the MPTES molecule. The smaller blue component located at approximately 287 eV is indicative of C-O/C-S moieties which are also consistent with the structure of the MPTES molecule. Due to overlap of the S *2p* and Ga *3s* regions shown in Figure 5.4(b) it is not trivial to compare the peak intensities to the C *1s* peak to elucidate rudimentary film-thickness measurements. Nonetheless, with copious post-reaction washing of the substrates, all physisorbed material is likely to be removed leaving only the chemisorbed monolayer. **Figure 5.4(c)** shows the combined scan for the Ga *3p* and Si *2p* regions. Again, due to the complex XPS spectra with regard to peak overlaps and surface plasmons, it is non-trivial to determine the presence of Si. A shoulder located approximately at 101 eV could tentatively be fitted. Attempts were made to fit the peak with and without this shoulder. The peak fit remained better with the shoulder peak present, showing the

presence of Si could cautiously be confirmed. Combined with the data showing the presence of S, the chemisorption of the MPTES molecule was successful.

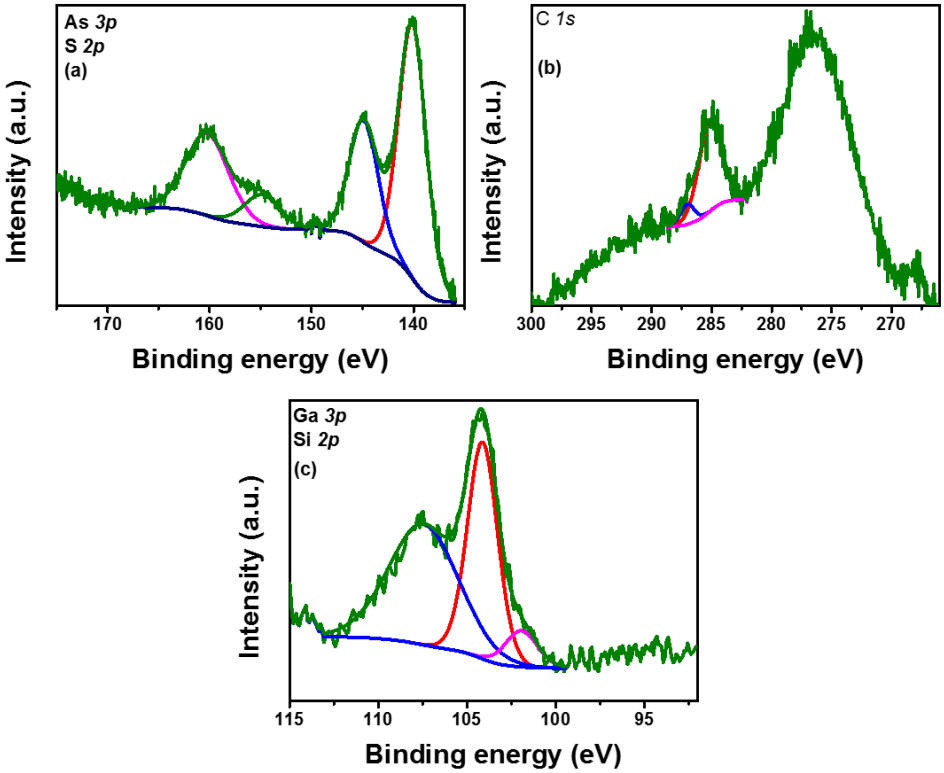


Figure 5.4. (a) Combined As *3p*, S *2p* and Ga *3s* core-level XPS spectra showing the presence of S on the surface with (b) showing the C *1s* peak with C-O/S chemical moieties indicated by the blue peak and (c) combined Ga *3p* and Si *2p* core-level scans. A small shoulder peak in (c) indicated in pink, shows tentative evidence for the presence of Si on the surface from the MPTES molecule.

5.3.2 Dopant characterisation of InGaAs surfaces functionalised with 3-mercaptopropyltriethoxysilane (MPTES) and subsequently capped and treated with a rapid-thermal-anneal.

Samples functionalised with MPTES were removed from an inert atmosphere and capped with 50 nm of sputtered SiO_2 and heated in a rapid-thermal anneal furnace to 750 °C for 15 s and 30 s under nitrogen. While the choice of method for the capping layer deposition and the specific composition of the capping layer may affect the monolayer integrity, this effect was not studied in this work. Plasma-enhanced chemical vapour deposition (PECVD), electron-beam evaporation or spin-coating could be used to determine the effect, if any, on the MLD process. Following the anneal step, a buffered-oxide etch was used to remove the oxide prior to dopant characterisation. Raman scattering was used in the first instance to "fingerprint" the samples non-destructively for the presence of dopants prior to destructive ECV analysis. Raman scattering has shown use as a non-contact method to elucidate carrier density, crystallinity and band-bending in binary and ternary III-V semiconductors.[34,35.42-44] Data obtained during Raman scattering analysis is shown in **Figure 5.5** where scans of a region of interest for MPTES-functionalised samples, which have been subjected to a rapid-thermal-anneal process at different temperatures, are shown. As can be seen when compared to a bulk, nominally undoped sample, the dopant has an effect on the Raman signature of the InGaAs, suggesting an alteration in the structure. Due to the bulk nature of the material, no damage was observed on the surface of the sample, showing the change in the Raman signature is probably due to dopant incorporation, as opposed to thermal stress caused by the laser power. A lower laser power of 50 % (6 mW) was used as a precaution.

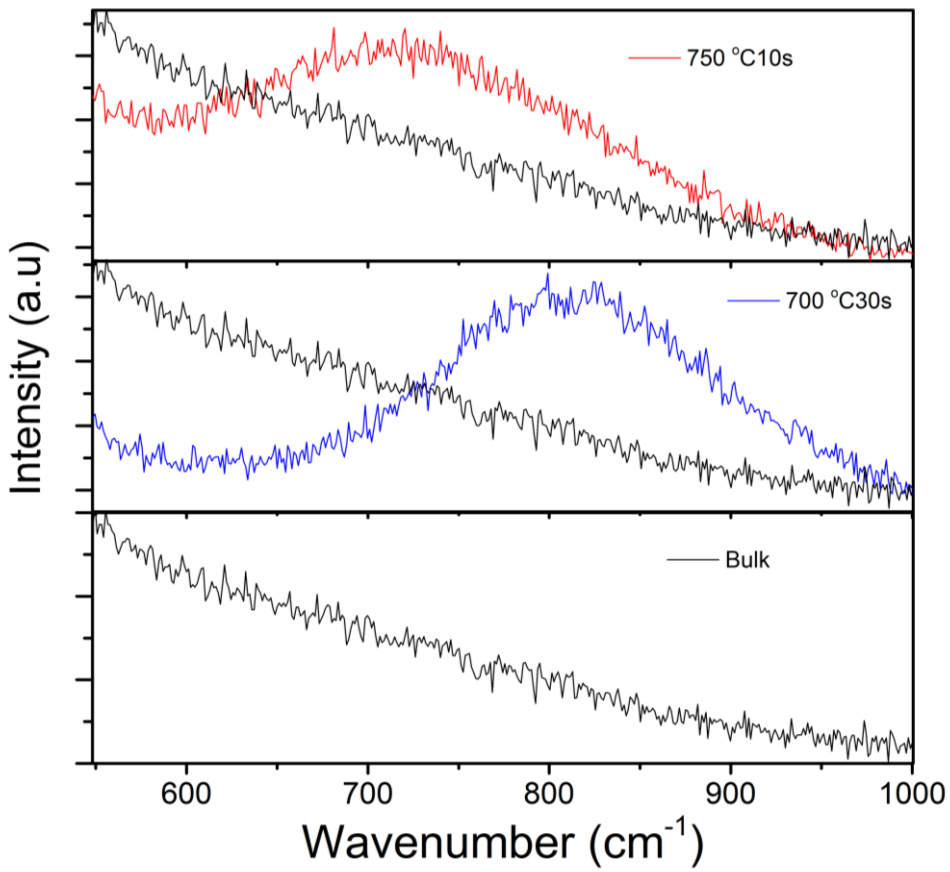


Figure 5.5. Representative Raman scattering spectra of a region of interest for MPTES-functionalised samples which have been subjected to a rapid-thermal-anneal process at different temperatures, using a bulk, undoped sample shown in black for comparison. As can be seen the dopant has an effect on the Raman signature of the InGaAs, suggesting an alteration in the structure. Due to the bulk nature of the material, a lower laser power was used to eliminate changes in the structure due to thermal stress. No damage was observed on the surface of the sample, showing the change in the Raman signature is due to dopant incorporation, as opposed to thermal stress caused by the laser power.

Figure 5.6 displays an ECV carrier profile showing temperature vs concentration data for MPTES-functionalised samples which were subjected to a capping step and rapid-thermal anneal process. Sample annealed at 750 °C for 15 s exhibited a peak carrier concentration of approximately 8×10^{18} atoms/cm^3, with a maximum junction depth of approximately 110 nm. Other MPTES samples functionalised in a similar manner but annealed for a longer time of 30 s exhibited an active carrier concentration approaching 2×10^{19} atoms/cm^3, with an approximate increase of 40 nm in the junction depth to 150 nm. Due to the presence of Si and S in the MPTES molecule, ECV cannot differentiate between the contributions of each atom towards the dopant profile, instead giving a total active carrier concentration. Despite this difficulty in determining which dopant atom is contributing most active carriers we have shown that dopant diffusion from the MPTES monolayer does occur. The junction depths are quite deep when compared to previous MLD processes on InGaAs highlighting the need for more advanced annealing techniques such as flashlamp and laser annealing.[45-48]

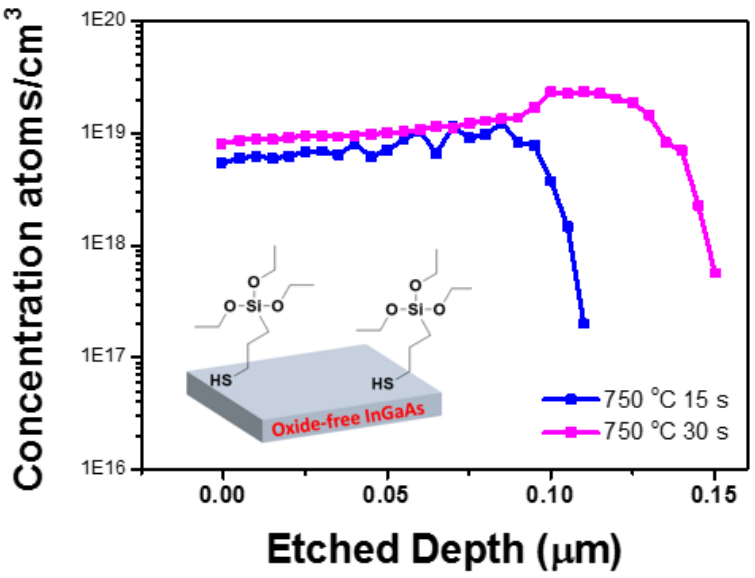


Figure 5.6. ECV carrier profile showing temperature vs concentration data for MPTES-functionalised samples which were subjected to a capping step and rapid-thermal anneal process. The sample annealed at 750 °C for 15 s exhibited a peak carrier concentration of approximately 8×10^{18} atoms/cm^3 with a maximum junction depth of approximately 110 nm. Another MPTES sample functionalised similarly and annealed for a longer time of 30 s exhibited an active carrier concentration approaching 2×10^{19} atoms/cm^3, with an approximate increase of 40 nm in the junction depth to 150 nm. Inset graphic depicts the surface passivation of an InGaAs substrate by MPTES.

5.3.3 Modification of the oxide-free InGaAs surface with allyltributylstannane

Sn is a widely used Group IV dopant for the preparation of *n*-type InGaAs layers, especially in molecular beam epitaxy (MBE). Unlike Si and Ge, Sn does not exhibit amphoteric behaviour in InGaAs and will act as an *n*-type dopant only. Thus, Sn is the dopant of choice to achieve heavily *n*-doped III-V materials. Unfortunately, suitable Sn precursors for MLD are scarce due to the complex InGaAs surface chemistry. Following the cleaning and etching procedure developed by Lie *et al*.[49] gives an As-dominant surface which, following a DI water rinse, leaves a H-terminated surface which may be reacted with the labile C=C site on allyltributylstannane. The presence of inorganic fluorides, typically observed by XPS in the F *1s* region at approximately 690 eV post-clean would indicate an incomplete cleaning process, but XPS analysis did not show evidence for the formation of such moieties. XPS survey spectra for the as-received and cleaned substrates used for the ATBS functionalisation are shown in **Figure 5.7**. **Figure 5.8** shows a Sn *3d* core-level spectrum of an InGaAs surface that has been functionalised with the ATBS molecule. The spectrum is dominated by the Sn *3d* elemental doublet. The doublet separation is approximately 8.3 eV which would indicate slight oxidation of the monolayer which would be consistent with the low stability of the organostannane in air. Samples were prepared to monitor the stability of the underlying substrate towards re-oxidation.

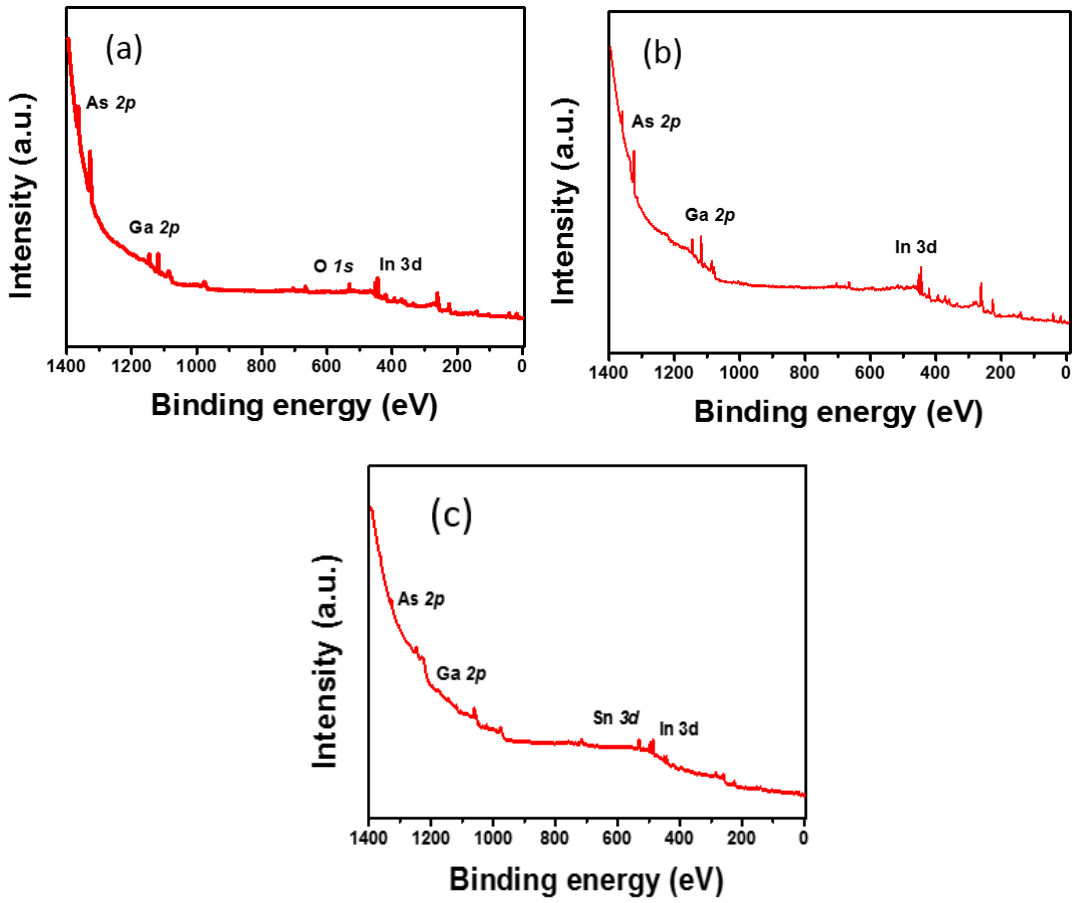


Figure 5.7. XPS survey spectra for (a) an as-received InGaAs substrate, (b) an ammonium hydroxide InGaAs etched substrate and (c) an InGaAs substrate that has been functionalised with ATBS. Attenuation of the substrate peaks was observed in (c) and was attributed to the bulky nature of the ATBS molecule. This was despite prolonged sonication in hexane and toluene to ensure total removal of physisorbed material.

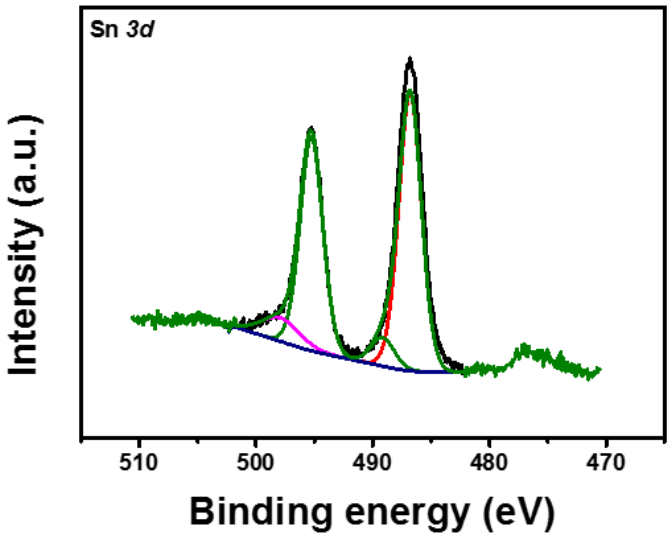


Figure 5.8. A XPS Sn *3d* core-level scan for a sample functionalised with ATBS. The spectrum is dominated by a doublet with a peak-to-peak separation of 8.3 eV. This would suggest the presence of an oxidised Sn species which may be attributed to the low stability of the organo-stannane monolayer on the surface.

5.3.4 Dopant characterisation of InGaAs surfaces functionalised with allyltributylstannane (ATBS) and subsequently capped and treated with a rapid-thermal-anneal.

The ABTS-functionalised samples were removed from an inert atmosphere and capped with 50 nm of sputtered SiO_2 and heated in a rapid-thermal anneal furnace for 10 s at temperatures between 550-650 °C under nitrogen. The ATBS-functionalised and doped InGaAs samples were tested for the presence of Sn by using Raman scattering before ECV and SIMS analysis.

Data obtained during Raman scattering is shown in **Figure 5.9**. Raman spectra show a dampening in the intensity of the GaAs-like longitudinal optical mode when compared to a bulk, nominally undoped sample. The insets more clearly show the reduction of the GaAs-like and InAs-like longitudinal optical peak. This reduction is due to the creation of charge carrier density as a result of the doping which causes a decrease of the surface depletion layer. Due to the bulk nature of the material, no damage was observed on the surface of the sample, suggesting that the change in the Raman signature was due to dopant incorporation, as opposed to thermal stress caused by the laser power. As a precaution, a lower laser power of 50 % (6 mW) was used.

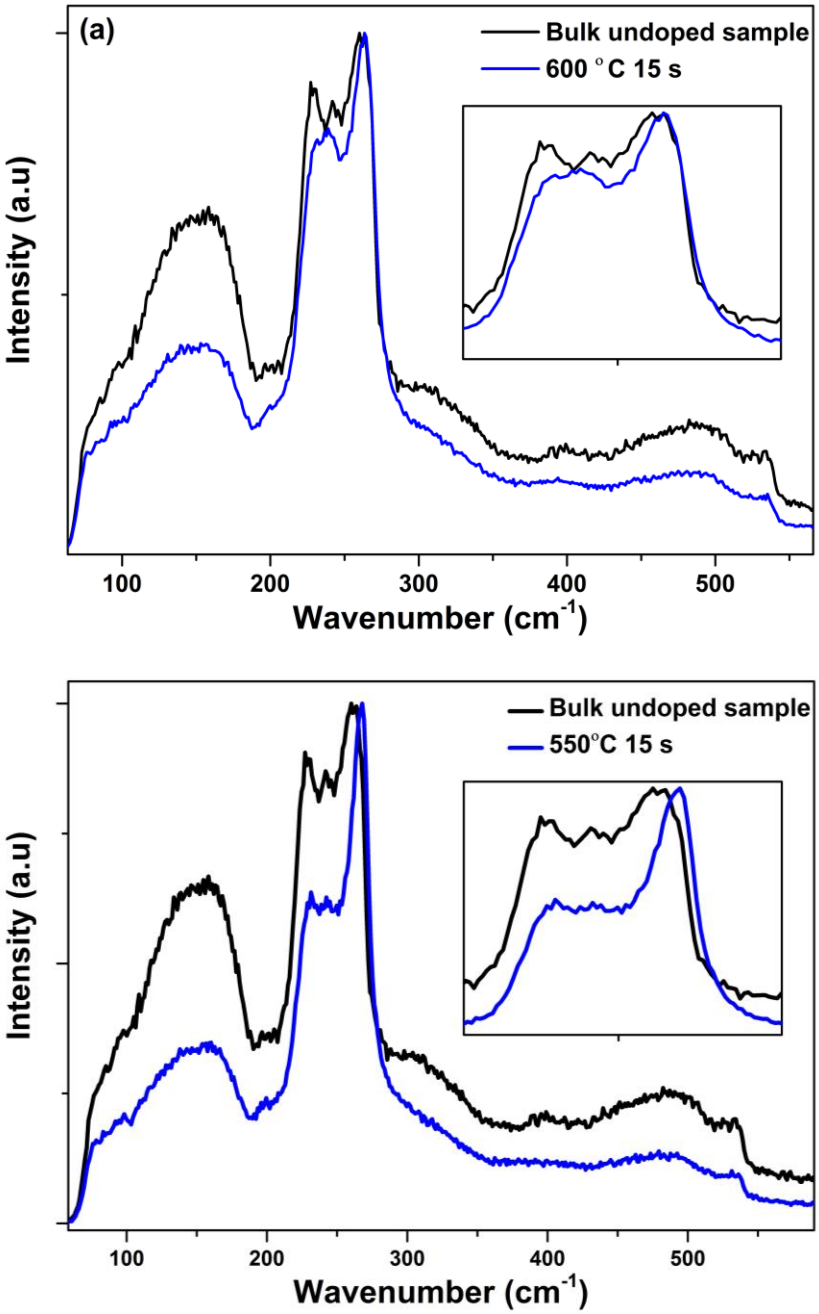


Figure 5.9. Raman spectra of ATBS-functionalised samples which have been subjected to a rapid-thermal-anneal process at different temperatures, using a bulk, nominally undoped sample for comparison. The insets show the reduction of the GaAs-like and InAs-like longitudinal optical peaks. As can be seen the dopant has an effect on the Raman signature of the InGaAs, suggesting an alteration in the structure. Potential alterations to the samples through thermal stress was prevented by using a lower laser power of 50 % (6 mW).

Figure 5.10 displays a carrier profile obtained from ECV measurements showing temperature vs concentration data for ATBS-functionalised samples which were subjected to a capping step and rapid-thermal anneal process. Samples annealed at 550 °C for 15 s exhibited a peak carrier concentration of approximately 1×10^{18} atoms/cm^3. Another ATBS-functionalised sample similarly treated and annealed at 650 °C exhibited an active carrier concentration approaching 9×10^{18} atoms/cm^3. The junction depths, similarly to the MPTES-doped samples were quite deep, approaching 200 nm, highlighting the need for more advanced annealing techniques.

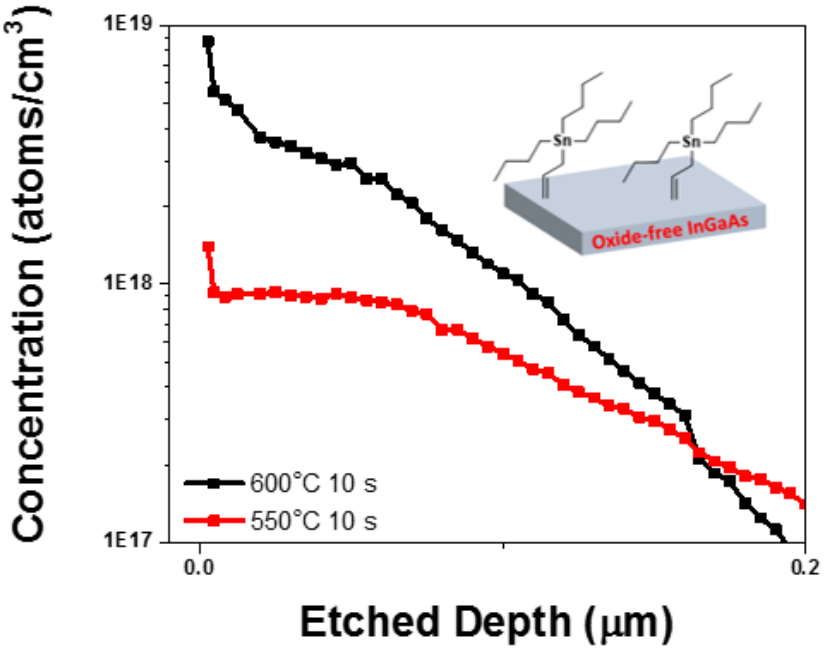


Figure 5.10. ECV carrier profile for InGaAs substrates functionalised with the ATBS molecule and subsequently functionalised at different temperatures for 10 s. The samples exhibited similar carrier profiles as well as similar maximum junction depths. The depths are quite deep, showing a need for the application of more advanced annealing techniques.

5.3.5 Stability of MPTES- and ATBS-functionalised InGaAs samples towards re-oxidation

The stability that is conferred on semiconductor surfaces by grafted monolayers is interesting for many applications. With respect to device integration, regrowth of surface oxides prior to rapid-thermal-anneal treatment and other important steps in CMOS processing is undesirable, especially in the moments immediately after a processing step. Surface functionalisation greatly increases the oxidation resistance of semiconductor surfaces.[50,51] To ascertain the stability of the MPTES and ATBS functionalised samples, substrates were left exposed to ambient conditions (air, 20 °C) for periods of time of 24 h and one week. Immediately prior to analysis the samples were rinsed with anhydrous chloroform to remove adventitiously adsorbed material from the surface. The As *3d* core level scan was used to monitor for an increase in oxide formation. Both of the functionalised samples showed no presence of oxide after 24 h. The non-functionalised sample showed the slight presence of oxide after being left out in ambient conditions for 24 h. The complete acquired stability spectra for the MPTES-functionalised samples are shown in **Figure 5.11.**

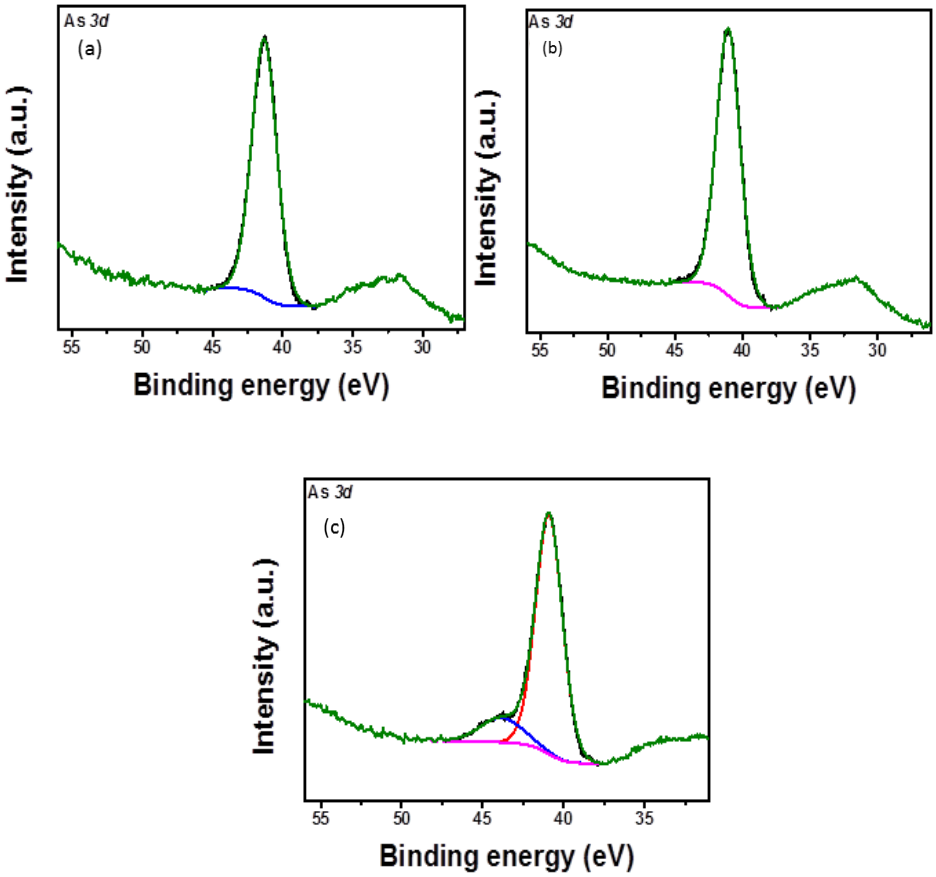


Figure 5.11. XPS As *3d* core-level data for MPTES-functionalised InGaAs substrates left out in ambient conditions for stability studies. A freshly etched sample is shown in (a) with a sample left in ambient conditions for 24 h shown in (b) and a sample left in ambient conditions for 1 week shown in (c). The spectrum displayed in (b) shows no presence of oxide after 24 h, showing effective passivation of the oxide-free InGaAs surface.

As *3d* core-level XPS data from non-functionalised InGaAs substrates are shown in **Figure 5.12**. The MPTES-functionalised substrates exhibited excellent resistance towards re-oxidation when compared to non-functionalised InGaAs substrates, especially 24 h immediately after functionalisation. This stability can be attributed to the tight packing of MPTES molecules. McGuiness and co-workers also postulated, due to thiol-functionalised III-V compounds showing no observable oxide, that the thiols pack very densely to protect the underlying surface.[52] Additionally, McGuiness suggests that removal of remaining substrate oxides after monolayer formation occurs by a "cleaning" action by the alkanethiol molecules, perhaps involving exchange of S for O at the surface and sacrificial reduction of the inorganic oxides by thiols.

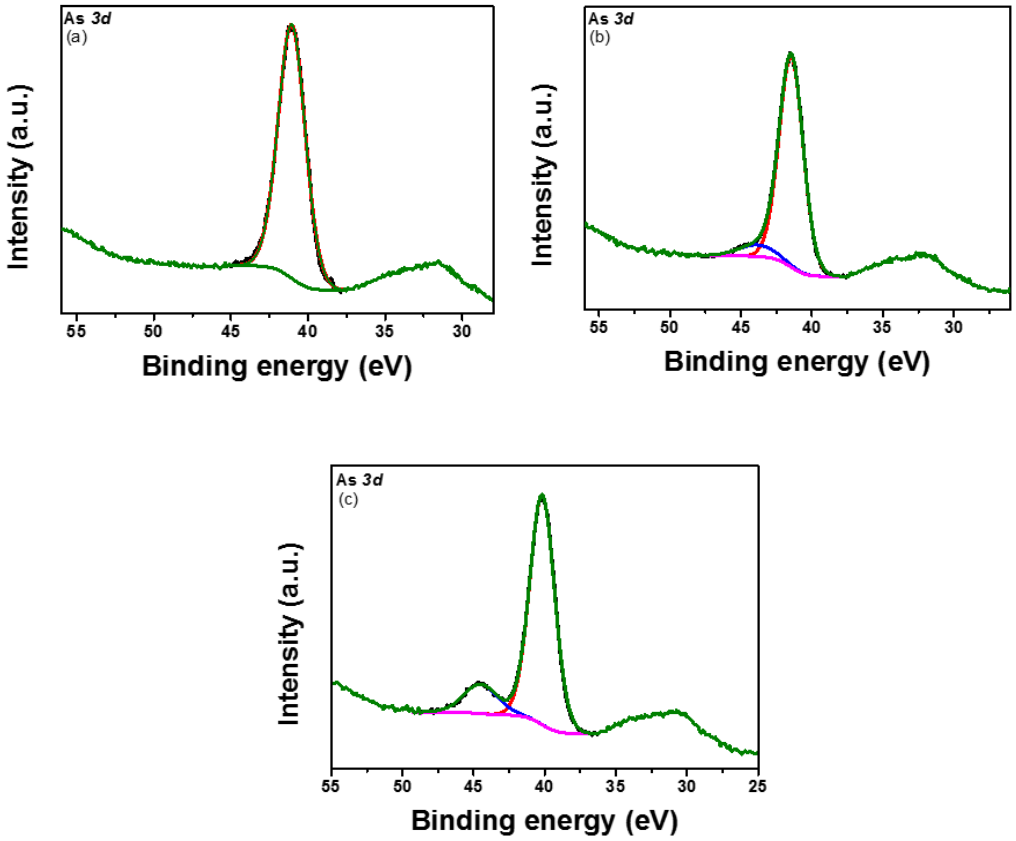


Figure 5.12. As *3d* core level XPS data for non-functionalised InGaAs substrates left out in ambient conditions for stability studies. A freshly etched sample is shown in (a) with a sample left in ambient conditions for 24 h shown in (b) and a sample left in ambient conditions for 1 week shown in (c).

Figure 5.13 compares the As *3d* XPS spectra for ATBS-functionalised samples, acquired immediately after preparation and after exposure to ambient conditions for 24 h and 1 week. These samples exhibited resistance toward oxidation that was not as resilient as the MPTES-functionalised samples can be attributed to the bulky nature of the ATBS molecule; where the bulky butyl groups may not allow for as close packing as the MPTES molecule causing pinhole oxidation at certain sites on the passivated surface. Efforts were made during the MLD process to ensure strict exclusion of oxygen and moisture. The ATBS sample was exposed to atmospheric

conditions for as short a time as possible during transport to the UHV environment of the XPS spectrometer.

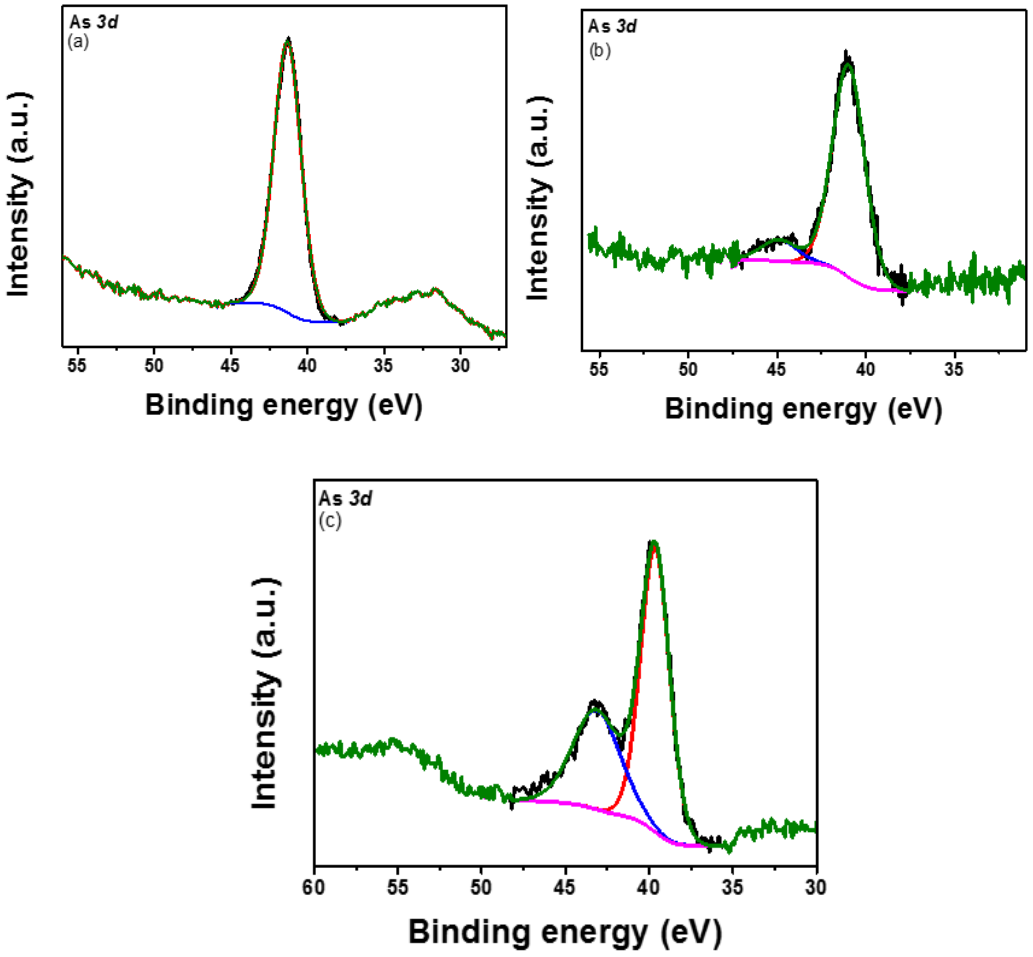


Figure 5.13. As *3d* XPS core level data for ATBS-functionalised InGaAs substrates left out in ambient conditions for stability studies. A freshly functionalised sample is shown in (a) with a sample left in ambient conditions for 24 h shown in (b) and a sample left in ambient conditions for 1 week shown in (c). The samples did not display the same resistance to oxidation as the MPTES-functionalised samples. This was attributed to the bulky structure of the ATBS molecule in addition to possible pinhole oxidation.

5.4 CONCLUSIONS

The monolayer doping process has been shown as a versatile technique for the conformal doping of a range of bulk and nanostructured materials such as Si and Ge. However, reports of MLD on III-V materials are scarce due to the challenging surface chemistry of InGaAs. As III-V materials come to the fore as prime candidates for future CMOS devices, there will be a need to conformally dope such materials whilst ensuring the substrates remain free from oxide ingress. InGaAs can successfully be functionalised with MPTES, a Si containing alkylthiol as well as ATBS, an organo-stannane, as shown by XPS analysis. The MPTES-functionalised substrates in particular, exhibited excellent resistance towards re-oxidation, especially within the first 24 h after functionalisation which is advantageous for future integration into CMOS fabrication processes. Raman scattering showed dopant incorporation into the crystal lattice in the case of both MPTES- and ATBS-functionalised substrates when compared to a bulk undoped samples. While junction depths may need to be optimised, by use of more advanced annealing techniques such as laser annealing or flashlamp annealing, ECV measurements also showed successful dopant diffusion into the substrates with maximum concentrations and depths varying with temperature.

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Chapter 6

Conclusions and Future Work

6.1.1 Conclusions

Advanced digital logic applications require semiconductor materials that provide for improved performance, energy efficiency and reliability. Integration of future channel materials into current CMOS manufacturing processes will be challenging and high control will be needed over defect minimisation as well as interface and surface chemistry. Concurrently, there is a need to be able to conformally and controllably dope these materials, especially as device geometries progress from planar structures to more complex non-planar and three-dimensional geometries such as architectures built around nanowires or fins.[1–3]

Functionalisation of semiconductor surfaces with dopant-containing monolayers will become more useful at scaled device dimensions, due to the large increase in the surface to volume ratio. To further increase channel mobility, new materials are being considered in efforts to continue boosting device performance. A number of non-silicon channel materials are being considered for advanced CMOS devices such as SiGe, Ge and GeSn for PMOS as well as III-V materials such as InGaAs, and GaAs for NMOS.[4–6] Additionally, carbon materials, *e.g.* carbon nanotubes, nanowires and graphene are also being considered.[7] These materials introduce differing challenges in terms of their surface chemistries. Strategies to successfully functionalise and dope such materials will need to be developed to ensure continued scaling and device performance.

Thus far, there have been no MLD studies using Al, Ga, Sn and Sb dopants. Synthesis of suitable precursor molecules for MLD processes based on such dopants will be challenging in terms of toxicity and air-sensitivity. Despite the challenges, the

bonding of organic monolayers onto semiconductor surfaces offers an exciting approach over conventional doping methods. Applications of MLD to next-generation device architectures such as gate-all-around FETs and tunnel FETs may prove interesting and will require the bringing together of expertise from device physicists, chemists and engineers to realise the next building blocks for our electronic devices.

Chapter 1 reviewed recent developments over the last number of years regarding the application of gas and solution phase techniques to dope silicon-, germanium- and III-V-based materials and nanostructures to obtain shallow diffusion depths coupled with high carrier concentrations and abrupt junctions *via* molecular monolayers. While the use of gas-phase and solution-phase monolayer surface chemistry for ultra-shallow doping of semiconductors is in its infancy, a vast body of research has accumulated over the last 5-10 years. The monolayer doping (MLD) technique has been shown to be a strong candidate to replace conventional doping methods such ion-implantation, spin-on-doping and *in-situ* doping for the doping of thin-body devices and extreme-3D structures due to its conformality, controllable dopant profiles and lack of damage to the semiconductor substrates and devices. The MLD process has also shown great promise for many materials which are relevant to the micro- and nano-electronics industries such as Si and Ge in addition to upcoming replacement material such as InGaAs.

Chapter 2 outlined the experimental methods used to functionalise the semiconductor surfaces used in this work with dopant-containing molecules and their subsequent capping and thermal treatment. The synthesis of custom-designed molecules was also detailed schematically. FTIR, NMR, CHN microanalysis and TGA were used to determine purity and decomposition points of the molecules prior to their use in the MLD process. Characterisation methods for planar substrates included XPS, AFM,

SIMS and ECV. For nanostructured devices, SEM and TEM was used to monitor nanowire morphology and also to ensure no damage was done to the test-structures by the MLD process. Fabrication of the nanostructured devices by EBL and their testing procedure was also outlined.

Chapter 3 described the first application of organo-arsenic monolayers on Si for high-density doping. A custom-synthesised organo-arsenic molecule was used to successfully functionalise planar Si substrates and Si nanowire devices ranging from 1000 to 20 nm. Extremely high dopant concentrations approaching 2×10^{20} atoms cm^{-3} were observed for bulk Si while excellent electrical characteristics were observed for MLD-doped Si nanostructures, with the highest decrease in resistivity of seven orders of magnitude observed for nanowires less than 40 nm in width. SEM and TEM analysis showed that the MLD process had no damaging effect on nanowire device structure and crystallinity, showing that the MLD process is suitable for the doping of extremely small devices without causing damage. Sample stability towards re-oxidation, as elucidated by XPS, showed that the functionalised samples were not as resistant towards oxidation as a non-functionalised sample.

Chapter 4 advanced the work started in Chapter 3 by using alkyne-azide cycloaddition reactions to introduce the dopant-containing molecules on Si surfaces. Si was successfully functionalised with di-alkynes with chain lengths between 6 and 10 carbon atoms and then subsequently functionalised *via* a copper-catalysed azide-alkyne cycloaddition reaction to give a dopant-containing monolayer on the surface. A commercially-sourced P-based azide was used as the P source while a custom As-based azide was synthesised based on literature procedures to serve as a useful comparison to the As-MLD process described in Chapter 3. XPS spectra contained signals referring to the [1,2,3]-triazole ring formation indicating successful grafting of

the dopant-containing azides to the terminal acetylene groups. ECV measurements confirmed successful diffusion of the dopants into the Si substrate with the P-doping process being most effective. In comparison to the work outlined in Chapter 3, the functionalisation approach outlined in Chapter 4 showed a marked improvement in the stability of the samples towards re-oxidation especially within the first 24 h. Additionally the click-chemistry approach was compared to a traditional MLD reaction to compare concentrations and oxidation resistance. The carrier profiles obtained from samples functionalised using the alkyne-azide reaction, in the case of the P-based azide, were essentially identical to that of a traditional MLD reaction using a structurally analogous precursor. However, the surface functionalised with a traditional MLD precursor exhibited a large presence of oxide after 24 h when compared to the click chemistry functionalised sample. The sample functionalised by the arsenic azide exhibited a lower carrier concentration when compared to the data reported in Chapter 3. This difference was attributed to a lower molecular packing density due to the rigid and charged azide groups in the molecule.

Chapter 5 investigated the application of a liquid-phase MLD process to InGaAs surfaces. Epitaxial InGaAs layers were grown on semi-insulating InP and functionalised with both S and Si using mercaptopropyltriethoxysilane (MPTES) and Sn using allyltributylstannane (ATBS). InGaAs was successfully functionalised with MPTES, a Si containing alkylthiol as well as ATBS, an organo-stannane, as shown by XPS analysis. The MPTES-functionalised substrates in particular, exhibited excellent resistance towards re-oxidation, especially within the first 24 h after functionalisation which is advantageous for future integration into CMOS fabrication processes. Raman scattering showed dopant incorporation into the crystal lattice in the case of both MPTES- and ATBS-functionalised substrates when compared to a bulk undoped

sample showing that Raman scattering will prove a useful tool to determine the presence of dopants in III-V materials non-destructively. The junction depths both for Si- and Sn-doped samples ranged from 110 nm for the shallowest Si + S doped samples to approximately 200 nm for the Sn-doped samples, nm, highlighting a need for use of more advanced annealing techniques such as laser annealing or flashlamp annealing. ECV measurements also showed successful dopant diffusion into the substrates with maximum concentrations and depths varying with temperature.

6.1.2 Future Work

The surface functionalisation approaches used in this thesis are extremely adaptable for applications where different dopant atoms are required. Additionally, the functionalisation routes are also suitable for application on a wide range of semiconductor surfaces and devices. Chapter 3 outlined the functionalisation of Si substrates and nanowire devices with triallylarsine monolayers. To extend this work into a future study, the synthesis of molecules containing more than one As atom, which could then be used in a MLD reaction, would be interesting. The maximum dose of a particular dopant is inherently limited by packing of the dopant-containing molecules at the surface. Introducing multiple dopant atoms within a molecule will allow an increase of the dose without impacting the monolayer packing density to a large degree. While MLD using multiple B atoms has been reported[8], there have been no reports of MLD using multiple As atoms or Al, Ga, Sb or P. While the synthesis of suitable precursors for approaches based on multiple Ga, Sb or P atoms will prove challenging this avenue of research could prove useful for increasing the maximum dose of dopant for an MLD process.

The click-chemistry approach used to functionalise and dope Si in Chapter 4 could be further advanced through synthesis of dopant-containing azides with different steric

features. Although azide stability during synthesis can be unpredictable, the superior oxidation resistance offered by the click-chemistry functionalisation process may be an acceptable trade-off. The study undertaken in Chapter 4 noted that the molecular packing at the surface, in the case of As, was limited due to the rigid nature of the arsenic azide molecule, which directly affected the maximum obtainable carrier concentration. Many routes exist for the synthesis of azides with differing steric characteristics based on P, As and Sb.[9–16]

In the case of nanodevices, the click-chemistry approach would be extremely useful to study the dependence of carrier concentration on carbon-chain length. By functionalising a nanowire surface with acetylene chains of varying lengths and then subsequently functionalising the chains with dopant-containing azides *via* CuAAC reactions, dopant atoms can be situated at certain distances from the nanowire. By annealing the nanowires at the same temperature for a given dopant, information about the dependence of carrier concentration on chain length would be yielded. Concurrently a stability study of nanowires functionalised in this manner could be conducted. This information may prove useful for eventual integration of MLD-processed nanowires in future CMOS processes.

Functionalisation as a technique for protecting and doping future channel materials such as InGaAs, GeSn and other materials will remain central for advancing CMOS technologies. The functionalisation strategy applied to the InGaAs substrates in Chapter 5 could be applied to III-V nanowire devices. This is an advantage of the MLD technique where methodologies applied to bulk substrates can also generally be applied to nanostructures. InGaAs-based materials possess higher electron mobilities than Si and their integration into future device structures will be beneficial for a wide range of technologies such as microelectronics and photo-voltaic applications. [17–20]

The application of MLD to InGaAs is in its infancy when compared to efforts on Si, showing that there are still many unexplored avenues. Application of MLD using strategies analogous to those reported in Chapter 5 may be relatively trivial but metrology of such devices may prove to be challenging.

Two-dimensional (2D) materials such as graphene are being studied for a number of applications such as advanced composite materials, photovoltaics, energy storage and microelectronics. Functionalisation of graphene-based materials is essential in order to engineer its band gap for its eventual integration into microelectronic devices. [21–23] 2D materials based on Ge such as germanane and germanene require functionalisation to introduce a band-gap and also to increase its thermal stability, which is required for such materials to be manipulated easily.[24–26] Stanene, a Sn-based 2D material, has recently been theorised as a contender to replace corresponding Si nano-electronics. The incorporation of F atoms into the Sn lattice has been predicted to extend the operating temperature to 100 °C to make it practically useful for future CMOS technologies.[21,27,28] The surface chemistry of these materials is varied and challenging but the MLD process may prove invaluable for band-gap engineering of this emerging class of materials. Each MLD process on future channel materials will also require optimisation of the junction depths by using advanced annealing techniques such as flashlamp annealing and laser annealing.[29–33]

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Appendix – Dissemination

7 APPENDIX

7.1 PUBLICATION LIST

7.1.1 Publications arising directly from this thesis

1. **O'Connell, J**.; Verni, G. A.; Gangnaik, A.; Shayesteh, M.; Long, B.; Georgiev, Y. M.; Petkov, N.; McGlacken, G. P.; Morris, M. A.; Duffy, R.; et al. Organo-Arsenic Molecular Layers on Silicon for High-Density Doping. *ACS Appl. Mater. Interfaces* **2015**, *7* (28), 15514–15521.
2. **O'Connell, J**.; Collins, G.; McGlacken, G. P.; Duffy, R.; Holmes, J. D. Monolayer Doping of Si with Improved Oxidation Resistance. *ACS Appl. Mater. Interfaces* **2016**, *8* (6), 4101–4108.
3. **O'Connell, J**.; Biswas, S.; Duffy, R. and Holmes, J. D. Chemical approaches for doping nanodevice architectures *Nanotechnology* **2016**, *27* (34), 342002
4. **O'Connell, J**.; Glynn, C.; Duffy, R.; O'Dwyer C. and Holmes, J.D. Liquid Phase Monolayer Doping Of InGaAs With Si-Containing And Sn-Containing Molecular Layers. (In preparation)

7.1.2 Co-authored Publications

5. Geaney, H.; **O'Connell, J**.; Holmes, J. D.; O'Dwyer, C. On the Use of Gas Diffusion Layers as Current Collectors in Li-O2 Battery Cathodes. *J. Electrochem. Soc.* **2014**, *161* (14), A1964–A1968.
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7.1.3 Conference Presentations

1. **O'Connell, J**; Gangnaik, A; Shayesteh M; Long, B; Georgiev, Y. M.; Duffy, R; McGlacken, G. P. and Holmes, J. D. "Organic Monolayers on Silicon for high-density doping" **EMRS 2015 Spring Meeting**, 11-15 May 2015, Lille, France (Oral Presentation).
2. **O'Connell, J**.; Long, B.; Duffy, R.; McGlacken, Gerard P.; Holmes, Justin D. "Organic monolayers on semiconductor surfaces: Passivation and Doping" **MRS Spring Meeting 2014** 21-25 April 2014, San Francisco, California, USA (Oral Presentation).
3. **O'Connell, J**.; Long, B.; Duffy, R.; McGlacken, Gerard P.; Holmes, Justin D. "Organic Functionalisation of Semiconductor Surfaces" **SMNOHDS 2013**, Ile d'Oléron, Bordeaux, France (Oral Presentation).