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Calculation of the capacitance-voltage characteristic of GaAs, $In_{0.53}Ga_{0.47}As$, and InAs metal-oxide-semiconductor structures

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Calculation of the capacitance-voltage characteristic of GaAs, $In_{0.53}Ga_{0.47}As$, and InAs metal-oxide-semiconductor structures[a)]

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The capacitance-voltage characteristic of GaAs, $In_{0.53}Ga_{0.47}As$, and InAs metal-oxide-semiconductor capacitors (MOSCAPs) is calculated in three cases. First, quantization is not considered, then quantization of the Γ-valley is included, and finally quantization of the Γ-, X-, and L-valleys is included. The choice of valley energy-minima is shown to determine the onset of occupation of the satellite valleys and corresponding increase in total capacitance. An equivalent-oxide-thickness correction is defined and used as a figure-of-merit to compare III-V to Si MOSCAPs and as a metric for the density-of-states bottleneck. © *2011 American Institute of Physics*. [doi:10.1063/1.3652699]

High mobility III-V semiconductors are considered for scaling beyond the 22 nm node because they promise a significant electron mobility enhancement over silicon.[1] The high electron mobility of III-V semiconductors is a result of the small effective mass in the Γ-valley conduction band. The small conduction-band effective-mass leads to a small conduction-band density-of-states (DOS) and the so-called DOS bottleneck,[2] where a large gate voltage is necessary to swing the Fermi level deep into the conduction band in order to strongly invert the III-V surface. As a consequence, the ideal capacitance-voltage (CV) characteristic of III-V metal-oxide-semiconductor (MOS) structures can deviate considerably from the well established CV characteristic of silicon MOS structures.[3–7] Knowledge of the ideal III-V MOS CV characteristic is essential, as it is required when assessing the impact of interface defects on the experimental CV responses of real III-V MOS systems.[8,9] In this letter, we extend on the work reported in Ref. 10 to calculate the theoretical CV characteristic for the case of p-type GaAs, $In_{0.53}Ga_{0.47}As$, and InAs metal-oxide-semiconductor capacitors (MOSCAPs). This work investigates the impact of III-V satellite valley occupation on the ideal CV, and the DOS bottleneck is quantified using the metric of an equivalent thickness of SiO_2 (t_{corr}) as a function of the inversion charge density.

The CV characteristics are modeled for a planar device geometry with a metallic gate, gate dielectric, and III-V semiconducting channel. We choose Al_2O_3 for the gate dielectric and consider GaAs, $In_{0.53}Ga_{0.47}As$ (referred to as InGaAs from here on), and InAs for the semiconducting channel. We set the constant p-type doping to $N_A = 2 \times 10^{17}\,cm^{-3}$, the physical oxide thickness to 2 nm, the metal work function to 5.05 eV, and the (001) surface orientation. The effective mass in the Γ-valley along the quantization direction, m_Γ, is listed in Table I for the III-V semiconductors considered in this work. We choose a 2 nm-thick gate-dielectric to reveal the strong asymmetry between the accumulation and inversion capacitance. We show later that the strong asymmetry allows the occupation of the L and X valleys to be clearly observed in the ideal CV characteristic. A perfect dielectric/semiconductor interface is assumed, with the interface traps, bulk traps, and bulk charge all set to zero, to more clearly observe the DOS bottleneck. Reference 10 describes the calculation in more detail.

To quantify the DOS bottleneck, the reduction in total capacitance below the oxide capacitance (due to the finite value of the semiconductor capacitance, C_s) is equated to an equivalent-oxide-thickness (t_{corr}) of SiO_2 in series with the gate dielectric. If the interface trap density is negligible, the t_{corr} correction is simply

$$t_{corr} = \frac{\epsilon_{SiO_2}\epsilon_0}{C_s}, \tag{1}$$

where t_{corr} is an implicit function of the charge density, and ϵ_{SiO_2} is the static dielectric constant of SiO_2. This value, while not physically meaningful, is used here as a metric to compare the impact of the low DOS in the Γ-valley and effect of satellite valley occupation for III-V semiconductors.

Figure 1 shows the electron concentration as a function of position for a silicon, GaAs, InGaAs, and InAs inversion layer at an electron sheet-charge, $n_s = 4 \times 10^{12}\,cm^{-2}$. Comparing the higher-mobility (lower mass and lower DOS) semiconductors of GaAs, InGaAs, and InAs to the higher-

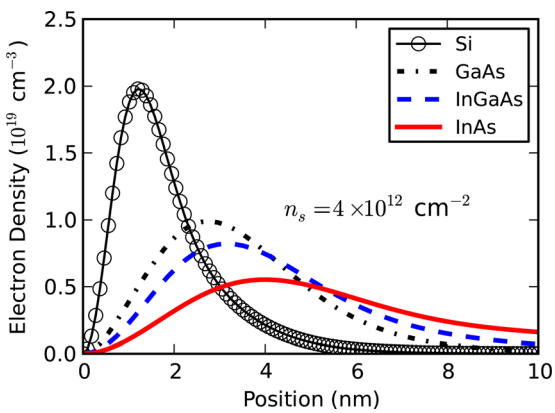


FIG. 1. (Color online) Electron density vs. position for Si, GaAs, InGaAs, and InAs MOSCAPs under strong inversion.

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TABLE I. Semiconductor parameters. E_Γ, E_L, and E_X are energies measured from the top of the valence band to the bottom of the Γ, L, and X valleys, respectively. N_C and N_V are the effective DOS for the conduction band and valence band, respectively. m_Γ is the effective mass and α_Γ is the nonparabolicity parameter in the Γ-valley. For all semiconductors, the nonparabolicity parameters of all satellite valleys are set to 0.5/eV (see Ref. 10).

Semiconductor	E_Γ (eV)	E_L[a] (eV)	E_X[a] (eV)	E_L[b] (eV)	E_X[b] (eV)	N_C (cm^{-3})	N_V (cm^{-3})	N_C/N_V–	m_Γ (m_o)	α_Γ[c] (/eV)
Si	3.40	2.0	1.12	—	—	3.2×10^{19}	1.8×10^{19}	1.78	—	0.5
GaAs	1.42	1.71	1.90	1.74	1.87	4.7×10^{17}	9.0×10^{18}	0.052	0.067	0.61
$In_{0.53}Ga_{0.47}As$	0.73	1.21	1.33	1.49	1.98	2.1×10^{17}	7.7×10^{18}	0.027	0.048	1.0
InAs	0.35	1.08	1.37	1.43	1.96	8.7×10^{16}	6.6×10^{18}	0.013	0.023	1.4

[a]Reference 12.
[b]Reference 13.
[c]References 10 and 17.

mass silicon, the peak electron concentration is pushed further away from the dielectric interface.[11] The peak of the electron concentration moves from about 1 nm for silicon to around 4 nm for InAs, with GaAs and InGaAs lying in-between these values.

Figure 2 shows the CV characteristic for 2 nm Al_2O_3 on p-type (a) GaAs, (b) InGaAs, and (c) InAs. Starting from GaAs, then InGaAs, and finally InAs, we see that the classical (no quantization, but including Fermi-Dirac statistics) CV-curve becomes more asymmetric as the DOS in the conduction band, N_C, reduces with respect to the DOS in the valence band, N_V. Table I lists N_C, N_V, and the ratio N_C/N_V for the semiconductors considered in this work. Including quantization of the Γ-valley increases the threshold voltage in all cases due to the shifting of the charge centroid away from the dielectric/III-V interface.

When including quantization of the Γ, L, and X valleys, the CV characteristic exhibits an increase in capacitance as the satellite valleys become occupied under strong inversion.[10] The shoulder in the capacitance occurs at different gate voltages for the three semiconductors because the energy separation between the valleys and 2D DOS is material dependent (as well as the differences in band gap and quantization masses, see Table I). In addition, we must rely on theoretical values of the energy minima of the satellite valleys because they are not known experimentally. In Table I,

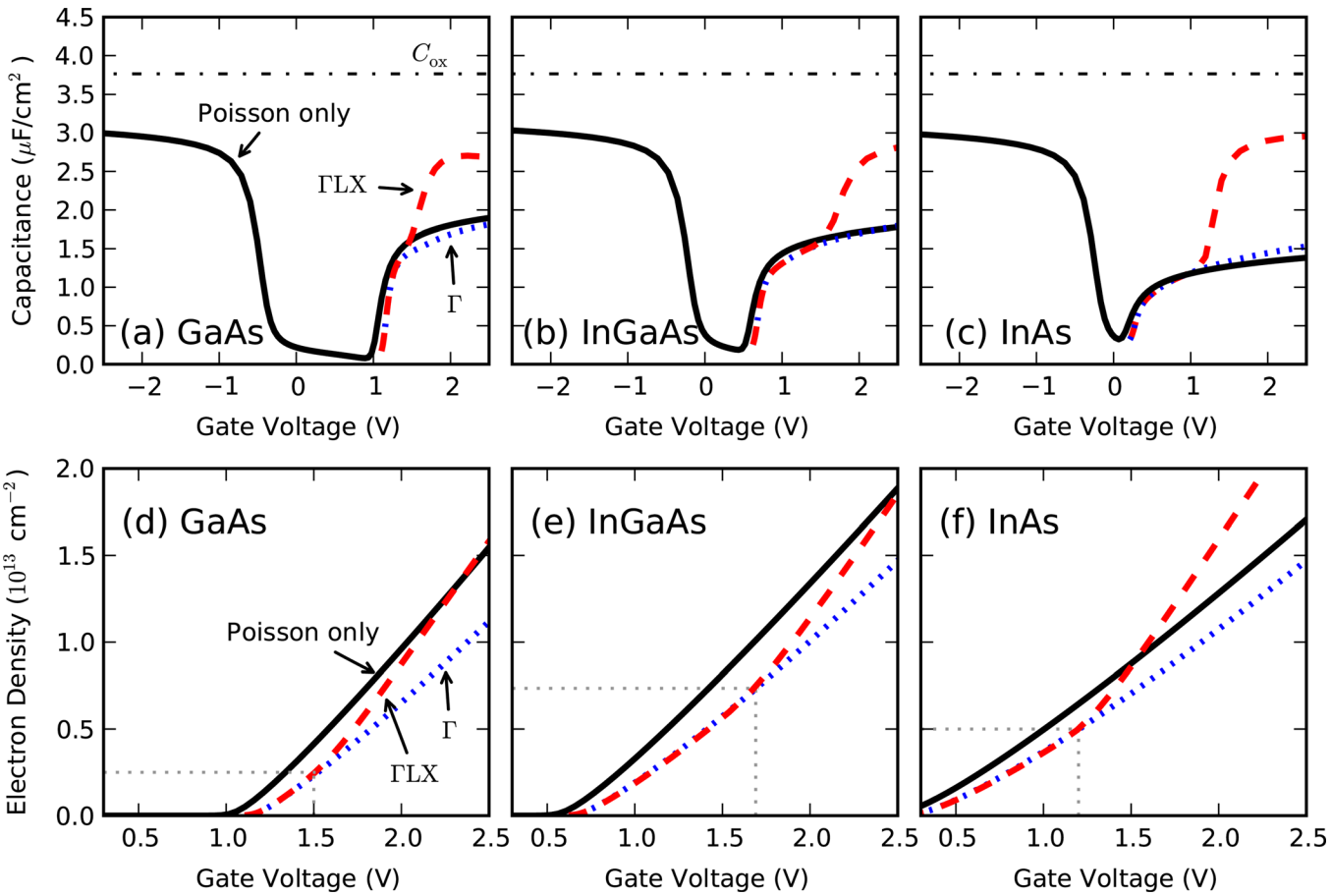


FIG. 2. (Color online) Ideal CV characteristic of (a) GaAs, (b) InGaAs, and (C) InAs MOSCAPs with 2 nm Al_2O_3 gate-dielectric. Corresponding electron-sheet-density vs. gate voltage for (d) GaAs, (e) InGaAs, and (f) InAs. The solid lines are solutions to the Poisson equation only, the dotted lines include quantization of the Γ valley, and the dashed lines include quantization of the Γ, L, and X valleys (using $E_{L,X}^{max}$ from Table I). In (d)-(f), the location where the dashed line clearly deviates from the the dotted line is highlighted by a box (grey dotted lines) with the upper right corner at the onset of satellite valley occupation.

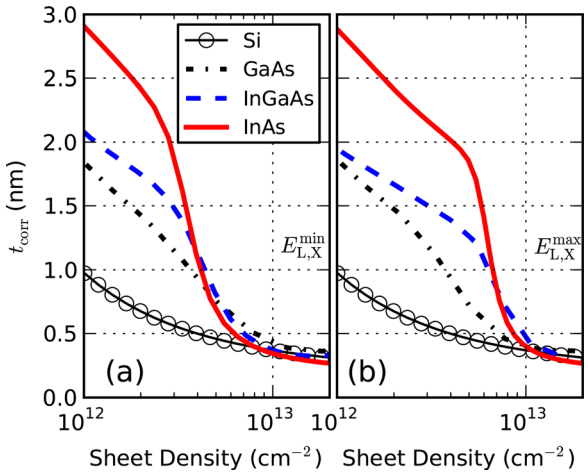


FIG. 3. (Color online) Equivalent-oxide-thickness correction vs. n_s. (a) The energy gaps in Table I from Ref. 12 are used (here denoted $E_{L,X}^{min}$). (b) The energy gaps in Table I from Ref. 13 are used (here denoted $E_{L,X}^{max}$).

we list two sets of values for the satellite valley minima that represent the maximum and minimum values from the literature, denoted $E_{L,X}^{min}$ (Ref. 12) and $E_{L,X}^{max}$ (Ref. 13), respectively. In Fig. 2, we use $E_{L,X}^{max}$, and discuss below the effect of this choice in the context of t_{corr}. Figures 2(d)–2(f) show n_s vs. gate voltage, corresponding to the CV curves in Figures 2(a)–2(c). Figures 2(d)–2(f) show the approximate n_s and gate voltage at which the satellite valley occupation becomes significant. This location, where n_s clearly deviates from the Γ-valley only case, is highlighted by a box with the upper-right corner at the onset of satellite valley occupation. As discussed in Ref. 10, nonparabolic corrections strongly effect the energy subband minima and compress the energy differences between subbands in the satellite valleys and the Γ-valley. This effect overcomes the large satellite valley offsets in InAs, and occupation of the satellite valleys commences at lower n_s for InAs compared to InGaAs (see Figs. 2(e) and 2(f)).

Figure 3 shows t_{corr} for the two sets of satellite-valley energies listed in Table I. In both Figs. 3(a) and 3(b), at mid $n_s = 10^{12}\,cm^{-2}$, InAs has the largest t_{corr}, followed by InGaAs, GaAs, and finally Si. This is a direct consequence of the low DOS in the Γ valley, which becomes significant as the DOS decreases from GaAs to InGaAs to InAs (see Table I). The effect of quantization, as shown in Fig. 1, also contributes to t_{corr}. For all the III-V semiconductors in Fig. 3(a), t_{corr} drops to the t_{corr} value of Si (<0.5 nm) in the range $n_s = 5$–$6 \times 10^{12}\,cm^{-2}$. However, for InAs and InGaAs in Fig. 3(b), t_{corr} drops to the Si t_{corr} value (<0.5 nm) in the range $n_s = 8$–$9 \times 10^{12}\,cm^{-2}$. In both cases, the drop in t_{corr} reflects the occupation of the satellite valleys.[10] The shift in the drop of t_{corr} to lower n_s is due to the choice of satellite-valley energy gaps. In Fig. 3(b), the gaps are higher compared to Fig. 3(a) and the occupation shifts to higher inversion densities. Similar values of t_{corr} versus n_s for Si and GaAs has been reported by Rafhay and co-workers (Ref. 14).

It is noted, that in real III-V MOS systems formed on GaAs, InGaAs, or InAs, the sharp increase in capacitance as a result of the satellite valley occupation may not be observed, as the CV characteristic is influenced by interface defects. In particular, experimental evidence indicates that in the case of high-k/InGaAs MOSCAPs, interface states exist not only in the energy gap but also with energies aligned with the InGaAs Γ-valley,[15,16] which can prevent the Fermi level from reaching the satellite valley energies. If interface defects can be reduced to negligible levels, the CV characteristics presented in Figs. 2(a)–2(c) should be observable as the electric field in the oxide is about 2 MV/cm for all Al_2O_3/III-V MOSCAPs at $n_s = 10^{13}\,cm^{-2}$.

In conclusion, we have shown the CV asymmetry of III-V MOSCAPs is a result of the lower conduction-band DOS relative to the valence-band DOS. The CV asymmetry is largest for InAs which has the lowest conduction band DOS compared to InGaAs and GaAs. The CV symmetry is partially recovered when including quantization of the satellite valleys, with the sharp increase in capacitance corresponding to the re-population of charge into the satellite valleys. The sharp increase in capacitance is semiconductor dependent, with the choice of satellite-valley energy gaps a key input parameter. Finally, the capacitance of Si, GaAs, InGaAs and InAs inversion layers was related to an equivalent thickness of SiO_2 (t_{corr}). The values of t_{corr} were used to quantify the degradation due to the low conduction-band DOS of the inversion capacitance in p-type III-V MOS systems with respect to Si.

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