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Publication date	2019-03-28
Original Citation	Fontana, A., Pazos, S., Aguirre, F., Vega, N., Müller, N., De la Fourniere, E., Silveira, F., Debray, M. E. and Palumbo, F. (2019) 'Pulse quenching and charge-sharing effects on heavy-ion microbeam induced ASET in a full-custom CMOS OpAmp', IEEE Transactions on Nuclear Science, 66(7), pp.1473-1482. https://doi.org/10.1109/TNS.2019.2908174
Type of publication	Article (peer-reviewed);journal-article
Link to publisher's version	10.1109/tns.2019.2908174
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Pulse quenching and charge sharing effects on heavy-ion microbeam induced ASET in a full-custom CMOS OpAmp

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***Abstract*—In this work, charge sharing effects on Analog Single Event Transients are experimentally observed in a fully-custom designed, 180nm CMOS Operational Amplifier by means of a heavy-ion microbeam. Sensitive nodes of the differential stage showed bipolar output transients that cannot be explained by single node collection for the closed loop characteristics of the circuit under test. Layout of these transistors are consistent with charge sharing effects due to deposited charge diffusion. Implementation of linear modeling and simulations of multiple node collection between paired transistors of the input stage showed great coincidence with the obtained experimental waveforms, shaped as bipolar, quenched pulses. These effects are also observed due to dummy transistors placed in the layout. A simple parametrization at the simulation level is proposed to reproduce the observed experimental waveforms. Results indicate that charge-sharing effects should be taken into account during simulation-based sensitivity evaluation of analog circuits, as pulse quenching can alter the obtained results, and linear modeling is a simple approach to emulate simultaneous charge collection in multiple nodes by applying superposition principles, with aims of hardening a design.**

***Index Terms*—Analog Single Event Transients (ASET), Microbeam, heavy ion, radiation, charge sharing, pulse quenching.**

I. Introduction

SINGLE event effects (SEE) on integrated circuits (ICs) are electrical disturbances produced by the interaction of high energy particles, such as those found in a space environment, with the underlying semiconductor substrate [1], [2]. Energy deposition of such particles along their path results in ionization, injecting a charge excess that can be collected by electric fields in the circuit, i.e. reversed biased junctions [3]. The impact of this charge collection on IC functionality varies widely with technologies, circuit topologies, working conditions and time domain response of the system under test. Particularly, from a time domain perspective, SEE in analog ICs are referred to as analog single event transients (ASET).

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Analog Complementary Metal-Oxide-Semiconductor (CMOS) circuits are key building blocks of complex mixed-signal systems. A distinctive characteristic of analog circuits, respect to CMOS digital ones, is the large variety of topologies, bias conditions, design considerations and also physical implementations for the same schematic design. Therefore, ASET sensitivity is hard to define for a given circuit. Efforts have been made so far to model, mitigate and experimentally assess SEE on digital circuits [4]–[9], but the experimental analysis of ASET has been mainly performed on commercial devices [10], [11], through laser experiments [11]–[13] or directly in simulation environments [14]–[18].

Particularly in sub-micron technologies, charge sharing effects have been observed in digital [4], [19] and analog [12], [13], [15], [20] circuits. This can cause multiple errors by a single ion strike or even pulse quenching in ion-induced transients, resulting in a reduced overall sensitivity of the system against SEE [12], [13], [15], [20], [21]. Nevertheless, these effects are difficult to model or predict: main approaches to modeling involve complex, high computational cost simulations including technology computer assisted design tools (TCAD) integrated in complex multi-physical environments [22]–[25]. Hence, the aforementioned complexity of mixed-signal systems increases the challenge of hardening an analog circuit block intended for space applications during design stages following this approach.

Experimental evaluation of SEE in ICs under heavy-ion irradiation can be performed in a handful of facilities around the world [8], [21], [26]. Such experiments provide information regarding the sensitivity of a given circuit against SEE, in working conditions that well reproduce those expected for a system that performs in a space environment, including the possible effects of physical implementations on the ASET response. However, microbeam irradiation of complex analog circuits have not been widely reported in the literature, particularly for full-custom ICs, where the possibility to map the ASET to each device of the circuit can prove of great value for calibrating simulation tools or assessing the sensitivity of each device on actual working conditions.

In this work, a full-custom 180nm bulk-CMOS operational amplifier (OpAmp) has been irradiated by means of a heavy-ion microbeam to capture the output ASET response under different incident ion species. The resulting waveforms are mapped to X-Y coordinates over the circuit layout and tran-

sients are linked to the sensitive transistors in the design. The characteristics of the observed voltage waveforms cannot be explained by single device collection. Therefore, charge sharing phenomena are taken into account to reproduce the response against events triggered in closely laid-out, matched transistors of the differential stage. Linear modeling of the circuit under test (CUT) is employed to model the response of the circuit considering charge injection into multiple nodes by superposition principles, allowing a simple but efficient representation of complex charge sharing effects to evaluate sensitivity of the circuit and possible hardening strategies. A simple empirical approach is proposed to introduce the impact of charge sharing effects in circuit sensitivity assessment. During the design stage, parametric sweeps of widely accepted current injection models can reflect, at first order, the charge sharing between nodes. Simulation results are compared to obtained experimental data, showing good agreement with reduced simulation efforts. The proposed modeling and the verification through heavy ion microbeam experimental results can prove very valuable to designers during system-level and circuit-level awareness of SEE on complex analog/mixed-signal (AMS) building blocks, such as phase-locked loops (PLL), voltage control oscillators (VCO), low dropout regulators (LDO), analog to digital and digital to analog converters (ADC and DAC), etc. A concise ASET simulation method can be used to predict experimental results as well as those results can be used to improve the simulation environment, pursuing a simple yet effective modeling for hardened IC design purposes.

II. Materials and Methods

The experiments were performed in the heavy ion microbeam facility at the Buenos Aires TANDAR Laboratory, which comprises a National Electrostatic Corporation 20UD tandem accelerator with a SNICS ion source coupled to an Oxford Microbeams, Ltd. OM55 high strength magnetic quadrupole triplet lens system, capable of focusing high energy heavy ions up to $\sim 160\ MeV\ amu/q^2$, and a standard end-station having a manual XYZ stage for sample manipulation. This facility consists of a fast beam switch to control the timing and the ion beam current, and a Si PIN photodiode (Hamamatsu S1223-01) to directly measure the number of ions hitting the device. The particle detector intercepts the beam periodically, fast enough to avoid significant dead times between the measurement and the irradiation periods. Therefore, extremely low heavy ion beam currents down to hundred ions/s can be accurately controlled, allowing to perform SEE studies in electronic devices. For further detail regarding the facility, the reader is referred to previous work by the group [26], [27].

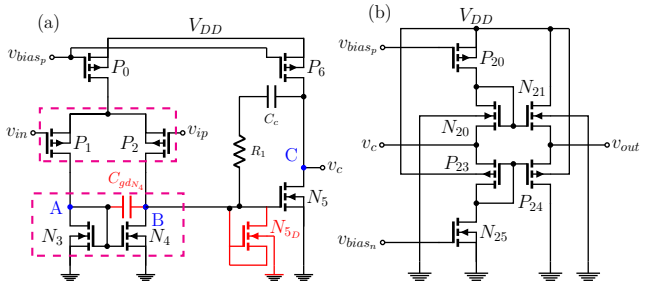


Fig. 1: Circuit schematic of the evaluated OpAmp: (a) shows the compensated two stage Miller OTA and (b) the output buffer. Dashed rectangles indicate matched transistor pairs and red components represent parasitic devices: $C_{gd_{N4}}$ is the gate-drain capacitance of N_4 linking sensistive nodes A and B, while N_{5_D} is the electrical equivalent of the dummy transistors of N_5.

A beam spot with a diameter of $5\mu m$ and an intensity of $\sim$100 ions per second was used for the experiments. $^{32}S^{5+}$ ions at 75MeV, $^{16}O^{5+}$ at 50MeV and $^{12}C^{4+}$ at 25MeV were used for the experiments, to provide different charge deposition densities and profiles along the substrate. The schematic of the CUT is shown in fig. 1, where the bias stage is comprised of a bandgap voltage reference with simple current mirrors [28] (not shown). The whole circuit was designed using thin oxide 1.8V transistors and vertical bipolar devices for the voltage reference. The total area of interest was 142x136μm^2, hence a scan region of 170x170μm^2 was selected. The delidded IC was mounted on a printed circuit board in a closed-loop non-inverting configuration with gain 10, and placed inside a chamber in high vacuum. The output of the OpAmp (v_{out} in fig. 1) was connected outside the chamber through BNC connectors and coaxial cables of lengths no larger than 1m to reduce parasitic effects and acquired by a 200MHz 4-channel DSO (GW Instek GDS-2204E) with the trigger level at 3mV, slightly above the background noise of the entire setup. X-Y location of the events was obtained by measuring the voltages of the beam deflectors every time an output pulse was detected. The frequency response of the circuit was measured before and after the experiment, showing negligible changes after the irradiation thus ruling out total ionizing dose degradation during the experiment.

III. Experimental Results

Fig. 2 shows the X-Y mapping over the circuit layout of the acquired output transients for the S ions. The color scale represents the peak value (positive or negative) of the acquired pulse for each position, as a heat-map representation. It can be clearly observed that the largest amplitudes are found to be close to the regions of the differential stage transistors. This stage is composed by two pairs of matched transistors, P_1-P_2 for the input, laid out on an ABBA interdigitation pattern, and N_3-N_4 for the current mirror load, designed on an arrayed 2x2 common centroid structure [29], [30]. In all cases, minimum distances and diffusion size rules were adopted for the transistors. It is interesting to note that both polarities for the peak voltages are observed in the layout of each transistor pair. Particularly for P_1-P_2, positive and negative pulses are distributed alternatively along the transistors' drains, in concordance to the ABBA pattern. Other sensitive transistors include the biasing devices P_{44} and N_{41} in the current reference stage (which for the sake of clarity is not shown in fig. 1) and their current copies P_{20} and N_{25} in the output stage, the common source stage following the differential input stage N_5 and the diode-connected transistors of the output stage N_{20} and P_{23}. Lighter O and C ions rendered similar mapping but with much lower pulse amplitudes.

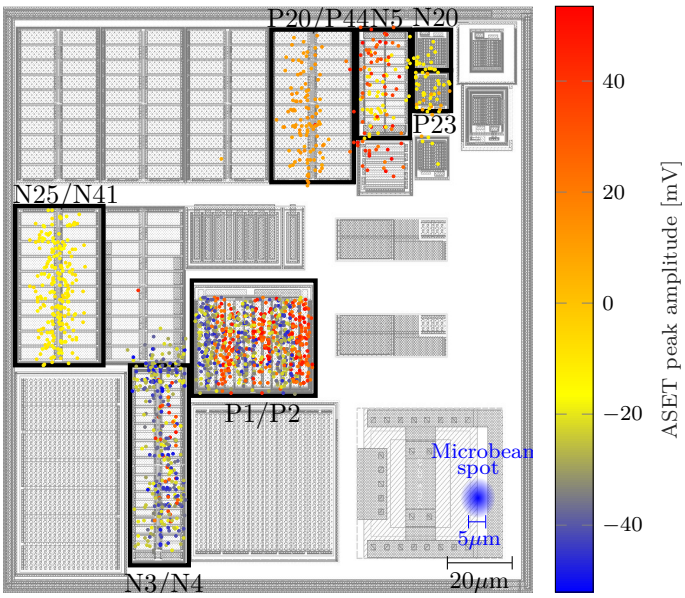


Fig. 2: X-Y mapping of the S ions for all single event coordinates of the beam deflection and overlap with the actual layout of the designed amplifier. The most sensitive devices are labeled.(For color version of this figure, the reader is referred to the online version of this article).

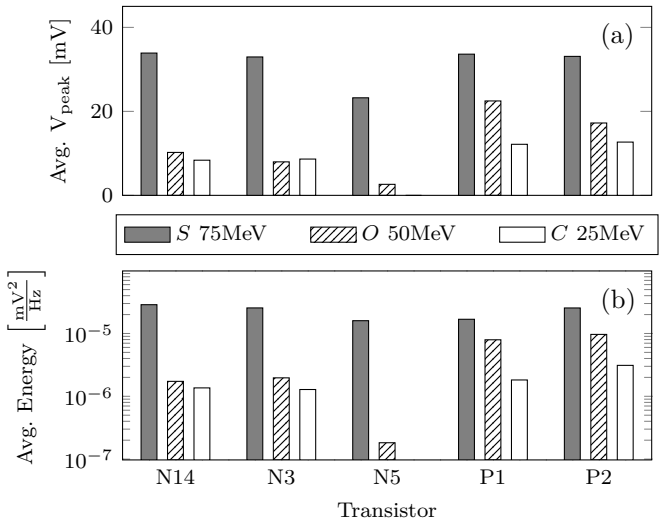


Fig. 3: Bar diagrams for average peak voltage (a) and output pulse energy (b) of the three experiments for the most representative transistors of the circuit.

In order to picture the sensitivity of the circuit under each of the ions used in the experiments, acquired output waveforms were characterized through specific data of interest in the time and frequency domains. Fig. 3.a shows a bar diagram for the average peak voltages, i.e. the mean peak value calculated from all the acquired pulses mapped to each transistor. on the other hand Fig. 3.b displays the average energy of the output pulses per transistor, obtained as the mean value of the integral of the Fourier transform for the acquired transients for each transistor and ion species, normalized against a 1Ω impedance, as calculated in [31]. From the point of view of the voltage threshold criteria [32], the voltage peak evaluation of the circuit (Fig. 3.a) may be useful in analog/mixed signal circuits for the identification of the transistors that can cause the capture of an error, e.g. single event upsets (SEU) or errors in analog to digital converters (ADC) [16]. On the other hand, on time continuous systems, the frequency domain study highlight the signals that may propagate downstream through the system and when the noise tolerance boundaries are exceeded [18], [31]. Moreover, pulse energy analysis can provide a figure of merit to quantify the radiation sensitivity of the circuit as well as assessing the contribution of each transistor for hardening proposes . Additionally, the figure of merit can be used to perform a comparison between different designs with the same functionality [33], [34] working on a system with fixed bandwith specifications. Hence, the criteria to establish circuit sensitivity is strongly dependent on the system within which the circuit will perform, and should therefore be chosen accordingly.

For both metrics, larger values are observed for S ions, while results for C and O are clearly lower: average voltage peak values range from 35mV down to 8mV while energies show in excess one order of magnitude of difference between ions. To better understand the observed differences in the results obtained for each ion in fig. 3, and to validate the experimental conditions, a deeper analysis of the energy transfered to the silicon substrate by the ions used in the experiments has to be considered. In this regard, a common criteria to quantify the ion-matter interaction is related to the linear energy transfer (LET) of the incident ions, as the amount of deposited charge on a target is proportional to the LET [1]. For a unit length of a given target material, the average energy lost by the ion as it displaces through the target can be quantified in units of MeV·cm^2/mg. In this framework, for a target of bare silicon, calculations of LET using SRIM [35] for the ions used in the experiments yield 3.4, 4.5 and 14.8 MeV·cm^2/mg for C, O and S ions, respectively. However, when working with heavy ions (such as S), even with delidded ICs, the non-negligible energy loss across the IC back-end-of-line (BEOL) passivation layers should be taken into account to fully understand the observed transient response, as it has been widely studied by means of simulation in the literature, using TCAD, GEANT4 or specifically designed simulation tools [22].

It should be pointed out that the presence of metal layers on the BEOL can induce a slightly larger energy loss than simple SiO_2 passivation, typical in 180nm technologies [36]. However, the circuit under test was laid out under a maximum of 3 metal layers, required to perform circuit interconnects, and therefore SRIM simulations were performed considering the worst case scenario in terms of ion energy loss, i.e. 3 metal lines in between the IC passivation layers. For aluminum interconnets, typically used in 180nm nodes for upper metal layers, their impact can be neglected on the overall energy transfer of the ion to the substrate, as the density of Al (2.7g/cm^3) is relatively low and comparable to that of SiO2 (2.65g/cm^3) inter-layer passivation. In the case of copper metal lines, mostly used for first level metal interconnets, the

density of Cu is considerably higher ($8.96 g/cm^3$) and may therefore affect the mean deposited charge, mainly by heavier ions that loose a considerable amount of energy along the BEOL.

To perform more accurate simulations of the expected charge deposition on the substrate by the impinging ions, the passivation thickness of the IC was measured, down to the third level of metal interconnects, by means of a cross-section imaging of the upper layers of the die performed using a high energy focused-ion beam (FIB). Fig. 4a shows a passivation thickness of around 15.5 μm down to the third metal layer, and Fig. 4b shows the relative thickness of the polyimide passivation (typical final passivation layer for ICs) measured from the profile image of the unpassivated bonding pads, which is around 4μm of the total passivation thickness. Taking these considerations into account, the mean charge deposited in the substrate by the ions was calculated, using SRIM simulations, to be 380 fC for C, 1.31 pC for O and 420 fC for S. These quantities are plotted in the inset figure of Fig. 5, which shows the simulation results for the average deposited charge on the substrate (Q_{dep}, left y-axis) as a function of each ion maximum LET into a bare silicon target. This clearly shows that, when dealing with a non-negligible energy loss in the BEOL stack, using higher LET won't necessarily represent larger amounts of charge deposited on the sensitive area of the CUT (i.e. the substrate), as it is observed for our experimental conditions. Although S ions have the highest LET, the O ions suppose larger amounts of deposited charge. This is consistent with experimental results obtained for Ni ions at 75 MeV (results not shown), that although having a LET of around 31 MeV·cm^2/mg showed very low count and very small events during the experiments. This was expected as the heavier Ni ions loose all their energy in the BEOL, and there is a very low probability of transmission down to the substrate (approximately 0.044 from SRIM calculations).

Additionally, stopping range (SR, shown in the right y-axis) was extracted from the deposition profile shown in Fig. 5. Numbers next to each curve represent the average ratio in percent of the ion energy that is effectively deposited on the substrate after traversing the BEOL. Largest acquired ASET pulses were observed for S ions, even though O ions deposit the largest amount of charge in the substrate as shown in Fig. 5. This is well in agreement with the literature, as the sensitive volume of a device is observed down to 2∼5μm from the surface, showing saturation of the collected charge beyond that point for similar CMOS technology nodes [37]. Although roughly 13% of the energy is lost in the substrate (around 9.7MeV), the shortest stopping range and higher LET for the heavier S ions result in most of the deposited charge located close to the shallow sensitive area of the devices (SR around 5um into the substrate), i.e. close to the surface of the substrate, maximizing the charge collection by sensitive nodes of the circuit. In contrast, though O ions deposit around 3 times the charge (59% of it's total energy, 29.5MeV), most of this charge is deposited along it's track down to ca. 21μm into the substrate, yielding considerably smaller ASET. This provides valuable information to prepare experiments and to validate the interpretation of our experimental results, as the full framework of our experiment is consistent with results previously reported in the literature. In the next section, acquired waveforms are analyzed and experimental conditions here described are essential to the understanding and modeling of the ASET response.

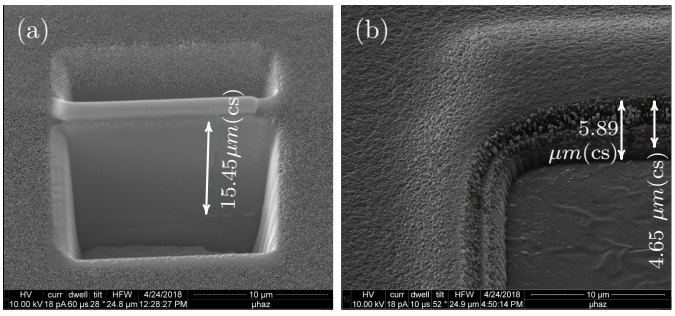


Fig. 4: FIB cross section imaging of the passivation layers of the die. A total width of 11.5μm of SiO_2 is considered down the third metal layer (a) for SRIM simulations, plus ca. 4μm of final die passivation assumed to be Kapton (polyimide) as shown in the bonding pad imaging (b).

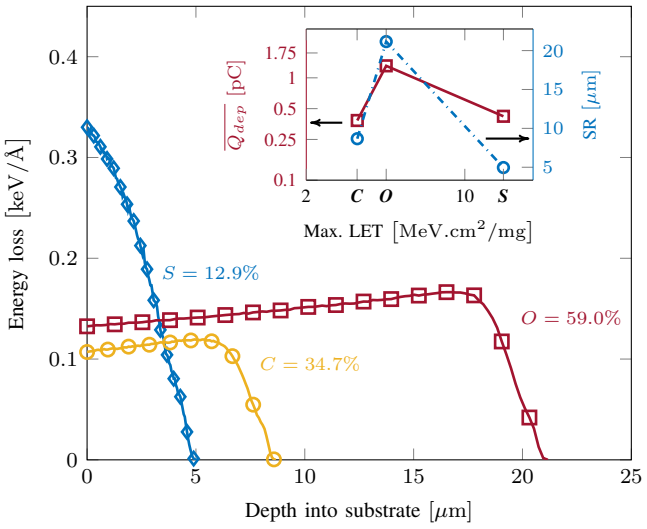


Fig. 5: Energy deposition profiles of the three ions on the silicon substrate. Numbers next to each curve represent the ratio of the ion energy lost in the substrate. Inset figure shows the average total deposited charge (solid line) and stopping range (dash-dotted line) as a function of the ions' LET into bare silicon (Ni not shown).

IV. Charge Sharing Effects and ASET Modeling

A. Experimental observation of charge sharing

It's worth mentioning that the microbeam uncertainty (recall that the diameter of the spot is roughly 5μm) is larger than the physical size of the single transistors in the matched pairs of the differential stage (channel length 2μm). Nevertheless, considering both the polarity of the waveform's peak and the expected response of the circuit to an impact on a given node (by simple circuit inspection and incremental current analysis),

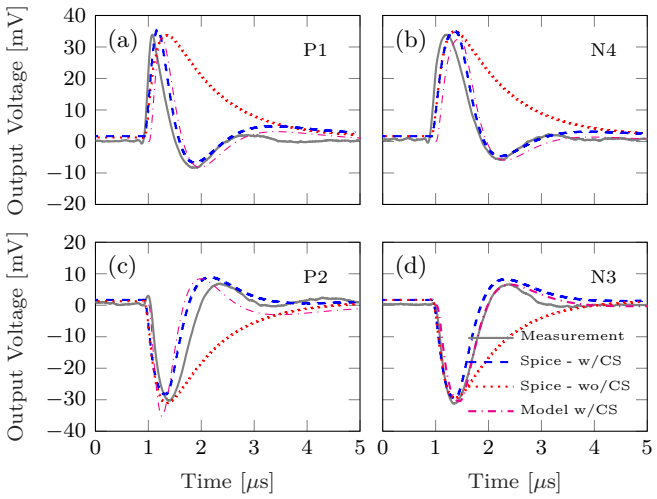


Fig. 6: ASET at the output of the OpAmp configured at gain 10 for each transistor in the differential stage. SPICE simulations with (w/CS) and without charge sharing effects (wo/CS) and linear model (w/CS) results are superimposed.

each ASET pulse was initially linked to a single transistor. Fig. 6 shows representative output transients induced by ions striking these transistors. For all cases, output transients show a bipolar behavior which could be, at first glance, misinterpreted as an underdamped response of the CUT to an impulse-like input.

However, for the closed loop configuration of this study, the CUT shows no ringing at its output on the step response in simulations nor on electrical characterizations including the impact of cables and setup in the irradiation chamber (results not shown). This is consistent with the projected phase margin for the amplifier, designed to present an overdamped closed-loop response. Furthermore, ion rate is low enough to discard multiple ions reaching the CUT during the time it takes for an ASET to decay below observable values ($\sim$1 ion per 10ms vs. a maximum ASET duration of 3μs). Additionally, ASET injection through current pulse sources in SPICE on each sensitive transistor of the device do not reproduce this output behavior, consistently with the design specifications of the circuit [34]. Current injection was performed using the widely accepted double exponential current pulse model [7], [20], [38], [39], whose expression is included for clarity in equation 1.

$$I(t) = \frac{Q_{coll}}{\tau_f - \tau_r}(e^{-\frac{t}{\tau_f}} - e^{-\frac{t}{\tau_r}}) \quad (1)$$

A brief comment is required at this point regarding the strongly non-linear energy deposition of heavier ions, as *S*, and its possible impact on the experimental results and on the modeling of the collection current used in this work. Although the precise modeling of such currents is not the main scope of this work, the complete energy deposition profile of the ions, previously shown in fig. 5 after considering BEOL losses, is considered to calculate the maximum charge that is to be collected by a struck node. Ignoring the effects of the BEOL and using the impinging ion LET into bare silicon to calculate charge deposition can lead to overestimations of the deposited charge that may not be representative of the actual conditions of the experiment. For this reason, the analysis of the experimental framework provided in the previous section becomes very important in the modeling stage.

Parameters of the double exponential current pulses were adjusted to a total collected charge lower than that expected from S ions (as collection efficiency is usually below 100% when some amount of charge is deposited beyond the sensitive depth of the device) and to obtain the output pulse amplitudes observed in the experimental results, with characteristic times well within the widely spread values reported in the literature [20], [38]. It is worth mentioning that, for certain circuits (e.g. logic gates, memories) the use of the double exponential current pulse in circuit simulations has shown to drive internal nodes of the CUT beyond the bias rails, i.e. +VDD or -VSS. In the case of the OpAmp, the most sensitive nodes in terms of output response are located in the differential stage, which is driven at 5μA per branch. Simple SPICE simulations representing an ion impact on N_3 of the differential stage and considering a rectangular current pulse of 50ns width showed that currents in the order of 40μA are required to drive the drain of N_3 to swing beyond the rails. This would represent a rough charge collection of 2pC, which is at more than four times the magnitude of the deposited charge by the S ions in our experiments if a sensitive volume depth of $2\mu m$ is considered. Therefore, it is safe to assume that, for our experimental conditions, the double exponential model represents well the disturbances of the impinging particles in the simulation realm.

These simulations are shown as dotted waveforms in fig. 6 (SPICE - wo/CS, where CS stands for charge sharing). Clearly, the output response shows a slow decay back to the initial conditions for all transistors, inconsistent with the experimental results. It should be highlighted at this point that test fixtures can have a strong impact on the acquired output transients: packaging, connectors and long cables introduce non-negligible parasitics that can strongly load the output of the CUT. At high frequencies, greater than 100 MHz, the cables must be modeled as a transmission line of characteristic impedance Z_0. A long transmission line, added to impedance mismatching, can result on considerable reflections of fast pulse edges along the line [40]. At relatively low frequencies, below 100 MHz, the test fixtures can be modeled by lumped elements, mainly series inductance and shunt capacitance that are both proportional to cable length. Under this conditions, a typical coaxial cable can introduce several tens of pF per meter length that load the output of the CUT. Taking this into account, simulations considering a worst case parasitic shunt capacitance of 120pF and a series inductance of 250nH, representing a 1m long cable as those used for this study, can be performed directly in SPICE. This is a good approximation since the bandwidth of the OpAmp is limited to 2MHz by design. Simulation results shown in Fig. 6 include these parasitic effects. Introducing double exponential current pulses in such simulations does not reproduce the acquired waveforms. Therefore, second order effects must be considered.

Given the fact that transistors of the differential stage were laid out to maximize device matching, it is logical to consider

charge sharing effects as observed in digital [4], [6], [19], [41], [42] and analog circuits [20], [43], [44] built in sub-micron technologies. In fact, charge sharing has been proposed as a mechanism to desensitize sections of analog circuits and evaluated through laser experiments [10], [12], [13], [45]. Fig. 7 shows a basic representation of the most important charge sharing phenomena on a simplified cross section view of the PMOS transistors in a bulk CMOS technology front-end-of-line. The figure represents a part of the ABBA (2112) pattern of P_1-P_2, where the ion impacts directly on the drain of transistor 1 for the sake of simplicity (note that parasitic bipolar junction transistor effect in PMOS transistors is not considered in this analysis). In Fig. 7.a, after a fraction of the ion induced charge is rapidly collected through the funneling mechanism [46], [47], the excess of ionized carriers distribute throughout the semiconductor substrate by means of ambipolar diffusion [6], [48]. In Fig. 7.b, the bipolar based equalization mechanism is represented [4], [20], [21], [49]. This effect is of importance to the collection current as it induces charge sharing between the terminals of a single MOSFET, where a parasitic bipolar transistor injects excess holes from the source to the drain of the MOSFET due to the excess electrons in the N-well that induce a bias to the base of the bipolar parasitic device. [4], [20], [21], [49]

In this work we focus on the charge sharing between devices by diffusion to explain the experimentally observed output transients. Depending on the amount of ionized charge and the energy deposition profile of the ion on the die, a non-negligible amount of charge can be collected by other sensitive areas located close enough to the initial ion path, i.e. the drains of transistor 2 in fig. 7.a. In such case, the expected output of the system will be the result of a superposition

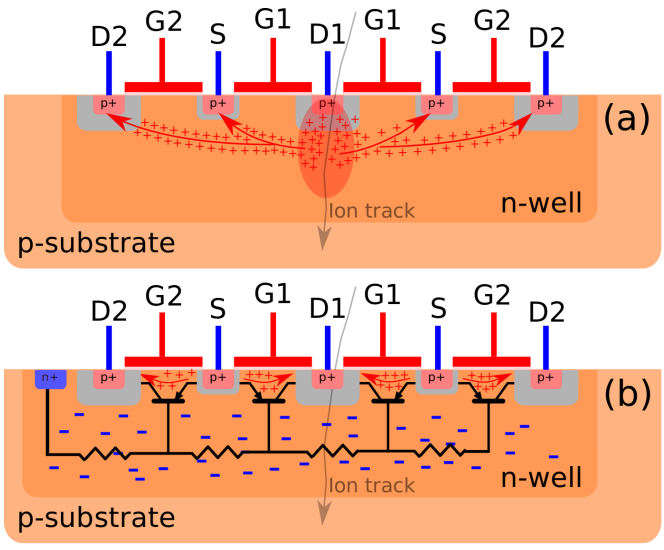


Fig. 7: Schematic representation of (a) charge sharing effects due to injected carrier diffusion and (b) due to parasitic bipolar based equalization mechanism. The gray areas indicate depletion regions. Note that in (b) charge sharing is performed between terminals of the same transistor, and not between transistors as in (a). (For color version of this figure, the reader is referred to the online version of this article).

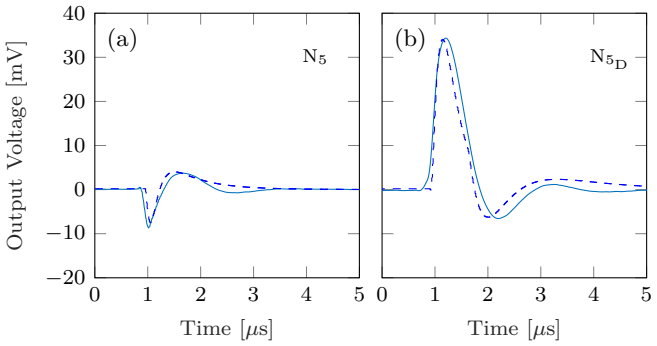


Fig. 8: Typical ASET waveforms acquired for impacts in the area of N_5. (a) represents pulses that start with a negative peak (linked to N_5 itself) and (b) those that show positive peak and bipolar characteristics (linked to the dummy transistor on the upper and lower edges of the layout, N_{5_D}). Dashed curves show simulation results in SPICE introducing charge sharing between nodes B and C of the schematic.

of effects on different circuit nodes triggered by a single ion. In this framework, considering that the distance between transistor drains is less than 5μm for P_1-P_2 and that typical diffusion lengths for carriers in lightly doped silicon is roughly 100μm [50], charge sharing should be taken into account to understand the experimental results. Electrically, this means a current injection at nodes A and B (see marked up nodes in fig. 1), which have complementary responses in terms of the resulting output voltage. The same interpretation can be considered to explain the pulses triggered by impacts on N_3-N_4 (same nodes A and B in the differential stage), where the drains of both transistors are closely located in 2x2 arrays with a common centroid layout, with distances between transistor drains as low as 0.5μm. It is important to highlight at this point that although the charge sharing effect has been strongly considered to mitigate ASET sensitivity [10], [12], [15], [45] and that although the observed waveforms in our circuit are quenched pulses from the simulated electrical response (shorter duration), the bipolar underdamped characteristic can pose a severe failure condition.

A separated analysis should be performed to understand the ASET response to impacts on N_5 observed in fig. 2. Although being N_5 solely laid out (far from other sensitive devices), experimental waveforms plotted in fig. 8 showed both positive and negative peaks on the output when struck by an ion, as clearly shown by the color scale in fig. 2. Contrarily, SPICE simulations and linear model analysis yield small, negative peaks in the output pulses when current is injected at node C, i.e. the drain of N_5. However, in fig. 2, large, positive ASET can be traced towards the upper and lower bounds of N_5, where dummy transistors were included in the layout and are connected as shown in fig. 1, named N_{5_D}.

The X-Y mapping and the output experimental waveforms are consistent with collection effects in the dummy transistors (placed at the top and the bottom of the transistor's layout) which are shorted but connected to the gate of N_5. Charge collection in such devices induce a voltage transient at the input of the common source stage (as for ion strikes at N_4, node B) that results in large swings on it's output. Therefore, events

triggered by impacts on N_5 are the result of the superposition between the transient resulting from the collection of charge directly at node C (small negative pulses) and the response of the stage to an input voltage fluctuation due to charge collection in the dummy transistors (large positive peaks). This effect is represented in Fig. 8, where typical positive and negative pulses for ASET due to N_5 are shown.

The higher amplitude of the pulses related to the dummy transistors suggests a much higher sensitivity to charge collection in these devices than at the drain of N_5, hence deposited charge diffusion plays a crucial role on the ASET response of the circuit.

In the next section, the analysis of this phenomenon is carried out by means of a linear model of the CUT that reveals the inconsistency between single node collection and the experimental output waveforms. Superposition principles can be applied to reproduce the effects of a disturbance signal, i.e. the collection current, on different nodes of the CUT occurring at the same time from a theoretical modeling.

B. Circuit linear modeling and charge sharing

In order to reproduce the output voltage waveforms due to impacts on different transistors of the OpAmp, a linear model of the closed-loop system was obtained to superimpose the response to charge collection in multiple nodes after an ion impact. The small amplitude of the observed pulses allows to implement small signal linear equivalent models to describe the problem. The main advantage of such models relies on its widely accepted use in analog IC design and that it allows to apply superposition principles to evaluate the expected circuit response to multiple signal inputs with small calculation efforts. Hence, the OpAmp can be represented by the voltage transfer function (derived from small signal analysis) of the differential stage G_1 cascaded with the common source G_2 and output stage G_3, as shown in the block diagram of the non-inverting configuration in Fig. 9. The block H comprises the feedback transfer function $\frac{v_b}{v_o} = \frac{R_2}{R_1+R_2}$, implemented with the external components R_1 and R_2.

Due to their random nature, the transients originated by SEE can be understood as disturbances in the system. Therefore, the voltage fluctuation in the internal nodes of the circuit due

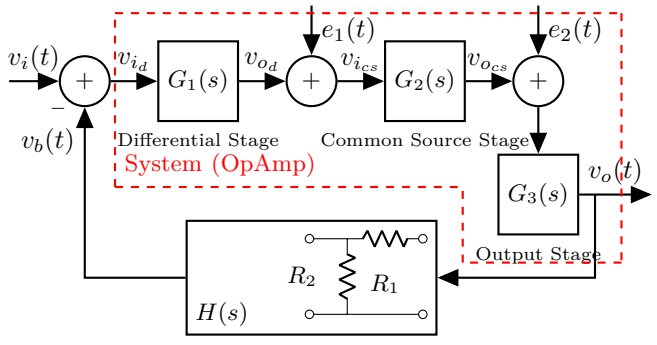


Fig. 9: Block diagram of the OpAmp feedback model with disturbance inputs e_1 and e_2 representing ASET induced signals at the output of the differential and common source stages.

to the collision of a heavy ion can be added as disturbance sources in the different nodes of the block diagram, e_1 and e_2. The voltage-time characteristics of these sources depend exclusively on the transistor where the impact occurred and on the collection current transient. In this representation, the voltage waveform of the source e_1 is defined by the events triggered on the devices of the differential stage, while e_2 is determined by the impacts on the common source stage. The output stage was considered capable of driving the load presented by the testbench without influencing the voltage transfer function of the OpAmp ($G_3 = 1$) but was taken into account in the transfer function of G_2 because the input impedance of this stage loads that block.

In this scenario, three different cases (A, B and C, representing the struck nodes in fig. 1) can be observed when obtaining expressions for e_1 and e_2 from the small signal equivalent of the CUT. In case A, to obtain e_1 the small signal analysis is performed with a current input in the drains of transistors P_1/N_3 and extracting the transimpedance function Z_m. The direction of the source current depends on the transistor under study, generating positive (P_1) or negative (N_3) output pulses. Regarding case B, the events generated by impacts on P_2/N_4 can be analyzed without considering the complementary branch, because the gate-drain capacitance $C_{gd_{N4}}$ linking the two branches of the differential stage (see fig. 1) is too small and local feedback effects can be neglected. Thus, in this case e_1 is produced due to the pulse current through the output load of the differential stage and the input load of the common source, i.e. the output voltage is the result of the ASET current flowing through the equivalent load impedance at the output of the differential stage. Finally, case C is similar to case B, but this time the influence of the compensation capacitance C_c has to be considered.

The previous analysis results on an overdamped response for cases A and B (e_1), which is inconsistent with the experimental output waveforms if no charge sharing phenomena is considered. To take these into account, it is possible to use the linear model to superimpose the resulting output waveforms of more than one current pulse injecting ASET current into different nodes of the circuit. The results of such procedure, injecting two double exponential current pulses with a small delay between them, are also shown in fig. 6 ("Model - w/CS") for each transistor of the differential stage, observing good agreement with SPICE transient simulations ("SPICE - w/CS") and experimental results. Under this conditions, the voltage transient waveforms of the output node reveal a bipolar characteristic that could not be explained by single node collection, and the pulse quenching effect is observed in the ASET response when compared with the single node collection case ("SPICE - wo/CS"). These results indicate that, although charge-sharing effects are the result of complex transport mechanisms and strongly depend on the physical implementation of the circuit, the possible incidence of such effects on the sensitivity of an analog circuit can be estimated through relatively simple, linear models by superposition of multiple collection effects, allowing a thorough exploration during design stages of the IC.

It should be highlighted that, as the model is obtained trough

linearization of strongly nonlinear CMOS devices, the validity of such representation is limited to specific working conditions for such devices. First, the linear model is obtained for a specific common mode of operation, in our case 0V input common mode voltage, that fixes the quiescent biasing point of the devices in the circuit. If the common mode input voltage is driven towards the limits of the circuit, some devices will change their quiescent point or may also be driven away from saturation, hence breaking down the small signal equivalent model. A similar analysis can be performed in terms of the effects of a transient disturbance of an internal node of the circuit, i.e. an ASET. Secondly, the same analysis performed in the previous section can be used to estimate at which LET values some devices can be driven into the triode region so to render the linear modeling invalid.

In the case of our circuit, the output stage works on a follower configuration and is highly linear up to the output dynamic range specification ($\sim$ +/- 350mV). The most sensitive stages to non-linearities are those that compose the compensated miller OTA, that are designed in terms of the small signal equivalent circuit of the MOSFET. Simple circuit simulations in SPICE allow to monitor the voltage of all nodes during a SEE. From SPICE simulations, it is possible to obtain the approximate maximum LET of a particle under certain collection current assumptions, for each transistor of the circuit. LET can be calculated as $LET = \frac{Q_{coll}3.6}{q\rho_{Si}d}$ where q is the electron charge, ρ_{Si} is the density of silicon, 3.6 eV is the required energy per ionized electron-hole pair in silicon and d the approximate depth of the sensitive volume of the device from the surface of the substrate. For the case of our experiments, it is shown in the manuscript that the linear model behaves very well and no strong non-linearities seem to impact the output waveforms. But, considering d=2 μm, for LET exceeding 96 MeV.cm^2/mg of a particle striking N_5, transistors N_5 and N_4 are driven out of saturation due to the injected charge. Hence, the linear modeling of the devices is a good approximation for a large part of the expected particle spectra in typical spacecraft missions [1], [51], where the flux is mainly composed by particles up to $\sim$100 MeV.cm^2/mg with a cumulative probability 99%.

From the design perspective, simulation of SEE sensitivity has been largely boarded in the literature through the years at SPICE level [14], [15], [17], [38], [52]. Even though these effects have been proposed to reduce the resulting ASET through pulse quenching [12], [13], [15], [44], works tackling design-time sensitivity assessments often consider simplified collection models [14], [38], [52] and little regard for second order effects. As shown by our results so far, the resulting transient at the output is severely modified by charge sharing effects resulting from the implementation of widely accepted layout techniques. Hence, a quick parametrization for ASET sensitivity analysis that takes into account such effects on a first order approximation is desirable to obtain a prediction closer to what would be expected from the physical implementation, without incurring into computationally costly simulations and allowing to perform radiation hardening strategies on an early design stage.

In this framework, a simple parametric approach to charge

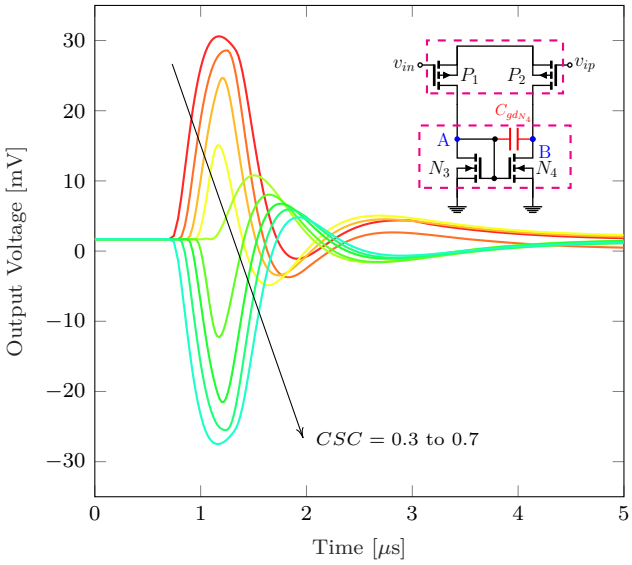


Fig. 10: Representation of the expected ASET response to S ions introducing a charge sharing coefficient, CSC between 0.3 and 0.7, between the input transistors P_1/P_2 of the differential stage. Inset figure shows the schematic circuit of the parametrization of the charge sharing effect, using two double-exponential current sources with characteristic parameters collected charge Q_{coll} and delay time t_d dependent on the CSC value.

sharing is exemplified that can be implemented both in the small signal design stage (applying linear superposition at the output) or, at later stages, at the SPICE level. Let us consider the transistors of the differential input stage of the amplifier, where charge will be shared between transistors of the matched pairs. Using two double exponential current sources, our approach proposes the use of a charge sharing coefficient (CSC), that ranges from 0 to 1, that linearly affects the total collected charge by each node of the circuit and introduces a proportional delay between the charge collection currents. In this framework, for a fixed collected charge Q_{coll}, each transistor of a matched pair would collect $Q_1 = Q_{coll}.CSC$ and $Q_2 = Q_{coll}(1 - CSC)$. Note that for the extreme values of CSC, only one of the transistors would be collecting charge. The second parameter to be considered is a slight delay between the collection currents, that can be parametrized as $t_{delay} = t_{d_0}(0.5 - CSC)$, where t_{d_0} is a constant representing a maximum delay between collection currents and each current is delayed in $\pm t_{delay}$, respectively. Rise and fall times are selected from within values reported in the literature for both current pulses, but considering the rise time of the secondary pulse (the one linked to the lowest charge collection) longer than that of the main collection pulse, given that the dominant collection mechanism is diffusion. Fig. 10 shows simulation results for the differential pair using this parametric approach, showing a good resemblance with the experimental results showed in fig. 6. Although this approach involves a strong simplification of a complex physical phenomenon, additional parameters can be included in a stochastic approach introducing variations of collected charge and rise and fall times. This type of parametrization allows to take design-time decisions

to harden the device against radiation effects with reduced computational costs.

V. Conclusion

In this work, a full characterization process is presented involving experimental heavy ion microbeam irradiation under high vacuum of a full-custom 180nm CMOS OpAmp, the mapping of ASET to the devices in the circuit, thorough analysis of the experimental framework to validate the results, identification of charge-sharing and dummy effects across the sensitive devices of the circuit, the use of simple linear modeling of the system and the straightforward introduction of charge sharing effects into early design stages of complex mixed signal systems.

Pulse quenching effects due to charge sharing are observed on heavy ion microbeam induced ASETs in a full-custom 180nm CMOS OpAmp. The use of a heavy ion microbeam allows to evaluate the behavior of the circuit under the working conditions expected for a device performing in space applications and the precise experimental conditions are essential to obtain accurate modeling. Captured ASET were mapped on the circuit layout and assigned to individual transistors. Experimental results showed output waveforms that cannot be explained by single node collection in the circuit, but linear modeling of the circuit under test allows to reproduce the observed transients by simple linear superposition effects that model the response to a delayed, asymmetric collection of complementary nodes in the differential stage. Such effects are consistent with the layout characteristics of the design, such as matched transistor pairs and layout dummy transistors. A basic parametric approach for design-time modeling of the charge sharing was proposed through a charge sharing coefficient that modifies the ratio of the total charge collected by each device of a matched pair of transistors and the relative delay between the injected currents at each node. Results showed good agreement between experimental data, SPICE simulations and linear superposition of charge injection in certain nodes of the circuit.

Finally, experimental results are valuable towards the calibration of simplified, yet efficient, simulation procedures to allow designers to introduce hardening at the system, circuit and physical levels in early design stages of complex AMS building blocks, such as LDO, PLL, ADC, VCO, etc. Future work involves the addition of simplified particle models to be introduced in the behavioral level to improve the completeness of the system level description of the problematic.

Acknowledgment

The authors would like to thank to the TANDAR Laboratory staff and Dr. Mariano Llamedo Soria for the inspiring discussions. This work has been funded by MINCyT under Contract PICT2013/1210 and PICT2016/0569, CONICET under Project PIP-11220130100077CO and UTN.BA under Projects PID-UTN 4395TC3, 4764TC, 4936 and 5219TC.

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