CORA Cork Open Research Archive
Cartlann Taighde Oscailte Chorcaí

Title	Inducing imperfections in germanium nanowires
Authors	Biswas, Subhajit;Barth, Sven;Holmes, Justin D.
Publication date	2017-03-02
Original Citation	Biswas, S., Barth, S. and Holmes, J. D. (2017) 'Inducing imperfections in germanium nanowires', Nano Research, 10(5), pp. 1510-1523. doi:10.1007/s12274-017-1430-9
Type of publication	Article (peer-reviewed)
Link to publisher's version	http://link.springer.com/article/10.1007/s12274-017-1430-9 - 10.1007/s12274-017-1430-9
Rights	© Tsinghua University Press and Springer-Verlag Berlin Heidelberg 2017. This is a pre-print of an article published in Nano Research. The final authenticated version is available online at: https://doi.org/10.1007/s12274-017-1430-9
Download date	2026-11-17 12:24:26
Item downloaded from	https://hdl.handle.net/10468/5288



UCC
University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

Inducing Imperfections in Germanium Nanowires

Subhajit Biswas and Justin D. Holmes

Materials Chemistry & Analysis Group, Department of Chemistry and the Tyndall National Institute, University College Cork, Cork, Ireland. AMBER@CRANN, Trinity College Dublin, Dublin 2, Ireland.

[*] Corresponding Author:

Prof. Justin D. Holmes

Tel: +353(0)21 4903608

Fax: +353(0)21 4274097

E-mail: j.holmes@ucc.ie

Dr. Subhajit Biswas

Tel: +353 (0) 21 4902911

Email: s.biswas@ucc.ie

ABSTRACT: Nanowires with inhomogeneous heterostructures such as polytypes and periodic twin boundaries are interesting due to their potential use as components for optical, electrical and thermophysical applications. Additionally, the incorporation of metal impurities in semiconductor nanowires could substantially alter their electronic and optical properties. In this highlight article, we review our recent progress and understanding in the deliberate induction of imperfections, in terms of both twin boundaries and additional impurity, in germanium nanowire for new/enhanced functionalities. The role of catalysts and catalyst-nanowire interfaces for the growth of engineered nanowires via a three phase paradigm is explored. Three phase bottom-up growth is a feasible way to incorporate and engineer imperfections such as crystal defects and impurities in semiconductor nanowires via catalyst and/or interfacial manipulation. An "epitaxial defect transfer" process and catalyst-nanowire interfacial engineering is employed to induce twin defects parallel and perpendicular to the nanowire growth axis. By inducing and manipulating twin boundaries in the metal catalysts, twin formation and density is controlled in Ge nanowires. The formation of Ge polytypes is also observed in nanowires for the growth of highly dense lateral twin boundaries. Additionally, metal impurity, in the form of Sn, is injected and engineered via third-party metal catalysts resulting above-equilibrium incorporation of Sn adatoms in Ge nanowires. Sn impurities are precipitated into Ge bi-layers during Ge nanowire growth, where the impurity Sn atoms become trapped with the deposition of successive layers, thus giving an extraordinary Sn content (> 6 at.%) in the Ge nanowires. A larger amount of Sn impingement (> 9 at.%) is further encouraged by the utilising eutectic solubility of Sn in Ge along with the impurity trapping.

KEYWORDS: Germanium, Nanowire, VLS growth, Twinning, Impurity incorporation

1. Introduction

Semiconductor nanowires have attracted great interest due to their potential application in optically active devices, as building blocks for nanocircuitry and in energy conversion devices, for which electron and phonon transport play a significant role in determining their properties.[1-4] In particular, group IV nanowires, such as Si and Ge, are playing a big role in the development of new functional microelectronic modules, such as gate-all-around field-effect transistor devices, on-chip lasers and photodetectors. Recently there has been a renewed interest in Ge [5-8] for applications such as nano-electromechanical systems (NEMS) [9, 10], lithium-ion batteries [11-13], field effect transistors (FETs) [14] and photovoltaics [15]. Like Si, Ge is a group 14 semiconductor material and exhibits certain properties that are superior to those of Si, including a higher charge carrier mobility [16] and a larger Bohr exciton radius, leading to more pronounced quantum confinement effects at higher dimensions.[17] Notably, the many parallels between Si and Ge should allow the seamless integration of Ge into current Si based devices.

In case of semiconductor nanowires, engineering the morphology, structure and composition, *e.g.* crystal defects, heterostructure, impurity incorporation *etc*. adds new functionalities for the applications of these nanowires in future technologies, such as spin-based electronic devices, tunnelling-based transistors and quantum computing devices. Also, to fully utilise the potential of nanowires, it is important to understand and control their structural properties, such as defect density and polytypism (one-dimensional variant of polymorphism), as they can influence electron and phonon transport and the electronic band structure in the nanomaterials. Nanowires with inhomogeneous heterostructures and periodic twin boundaries are particularly interesting to study due to their potential use as components for optical, electrical and thermophysical applications.[18-20] In recent years, a remarkable degree of control of

twinning and polytype generation has been demonstrated in III-V nanowires with the formation of twinning superlattices.[21, 22] However, the intentional induction and control of twin boundaries and polytypes in group IV semiconductor nanowires (Si and Ge) are an ongoing challenge, although for group IV semiconductors the influence of twin boundaries on the electronic band structure of Si and Ge is well documented.[23] Explorations of altered phonon transport through twin defects and hence a change in thermal conductivity and thermoelectric properties, has also made defect-engineering of nanostructures appealing.[19], [24], [25], [26]

Additionally, the incorporation of a non-equilibrium amount of impurities in semiconductor nanowires is attracting enormous research interest recently as the impurity induction could substantially alter the basic properties of semiconductors which are critical for emerging nanometre scale technologies. Colossal incorporation of foreign atoms in the host semiconductor lattice allows new or added functionalities (strain engineering, controlled defect formation, band structure modulation *etc*.) in the existing semiconductor system. For example, with non-equilibrium incorporation (6-10 at.%) of Sn in Ge, the small energy separation of 140 meV between the indirect (L) and direct (Γ) conduction band valleys of Ge can be overcome to make it direct bandgap semiconductor. Theoretical modelling[10] as well as photoluminescence experimental studies[11] have predicted no less than 6.5 at.% Sn, far above the equilibrium concentration of ~ 1%, in Ge is required for the transition to a direct bandgap material.[6, 12, 13]

The widely popular vapour-liquid-solid (VLS) growth model [27] refers to a three phase system where material supplied from a vapour phase absorbs into a liquid catalyst alloy and precipitates upon supersaturation to form a solid crystal. This mechanism has also been referred to when unidirectional growth results from any three phase system such as solid

catalysts, mainly resulting in single crystalline nanowires. Three phase bottom-up growth is a feasible way to incorporate and engineer imperfections such as crystal defects and impurities in semiconductor nanowires via catalyst and/or interfacial manipulation. Recently we were successful in implementing controlled crystal imperfections, mainly in the form of twinning defects in both axial and radial direction, in Ge nanowire via catalyst engineering in a three phase nanowire growth.[28, 29] An "epitaxial defect transfer" process and catalyst-nanowire interfacial engineering was employed to induce twin defects parallel and perpendicular to the nanowire growth axis. For impurity injection and engineering, a third-party metal catalyst was used to guide the non-equilibrium incorporation of Sn adatoms into the precipitated Ge bi-layers, during Ge nanowire growth, where the impurity Sn atoms become trapped with the deposition of successive layers, thus giving an extraordinary Sn content in the alloy nanowires. In this highlight article we review our progress and understanding in the deliberate induction of imperfections, in terms of twin boundaries and additional impurity, in Ge nanowires for new/enhanced functionalities. The role of catalysts and catalyst-nanowire interfaces for the growth of engineered imperfect nanowires via three phase paradigm is explored. The future research pathway for the defect/impurity engineered group IV nanowires and their possible device implementations is discussed.

2. Results & Discussion

2.1 **Induction of twinning defects in nanowires.** A twin boundary is isolated to a single atomic plane that separates two neighbouring crystal domains with very specific relative crystallographic orientations, without any dangling interface bonds. The control of twin periodicity in group IV nanowires offers the possibility of band structure engineering and interesting thermoelectric properties through modulated side faceting. Twinning and surface faceting can induce inhomogeneous stress fields which locally affect the conduction and

valence band potential, thus altering electronic band structure.[23] The occurrence of twin boundaries is not usual in VLS-grown Si and Ge nanowires as revealed by Davidson *et al*.[30] In general, for Au-seeded VLS growth of Si and Ge nanowires < 5 % of nanowires with {111} twin boundaries are generally observed along the nanowire growth axis in <112> directed nanowires.[30] Using classical nucleation theory, Johansson *et al.* proposed [31] that the energy barrier (ΔG_T) for the nucleation of a semi-circular twin nucleus, of radius *r* and height *h*, at the triple phase boundary (TPB), depends on the sum of the nucleus energy of a {111} plane, the twinning energy and the energy of the surface step associated with the nucleus, as shown below:

$$\Delta G_T = -\frac{\pi}{2} r^2 \left(\frac{\Delta \mu}{S} - \gamma_t \right) + \left(\pi \sigma_{ls} + 2\sigma_{sv} \right) rh$$

where $\Delta\mu$ is the change in the chemical potential/supersaturation, *S* is the inverse of the nucleation site density on a {111} plane, γ_t is the twin energy and all of the σ_s terms are different interfacial energies. As the twin energy (γ_t) is small compared to $\Delta\mu/S$, the energy barrier does not change significantly for twinned or ordinary nucleation. The interfacial tensions at the TPB and the deformation of the catalyst particle during crystal growth is liable for twin boundary formation in nanowire during catalytic bottom-up growth.[30] As such, the cross-sectional shape of a nanowire continuously evolves from hexagonal to triangular during growth, which dramatically increases the surface tension on the liquid. This effect causes the catalyst droplet to deform asymmetrically and the wetting angle to change, which governs the process of twin nucleation.[30] The fluctuation in the contact angle between the seed and the nanowire must be large enough to accommodate surface "re-faceting" without hindering nanowire growth (Fig 1).

Longitudinal twin boundary along the nanowire growth axis. Research initiatives on the intentional induction and understanding of twin formation in Si and Ge nanowires are motivated by interesting science and devices offered by twinned one-dimensional nanostructures. Twin formation in nanowires has been explained through nanowire growth kinetics, the inherent thermodynamics of a three phase system, surface energies of nanowires and interfaces and metal catalyst phases. [32] [33] Axial twinning in nanowires is generally observed in <112>-directed nanowires, where {111} planar faults along the growth axis produce defects in the *ABC* stacking sequence, along the <111> direction. Structural defects in the form of longitudinal twin boundaries have been described in a few articles dealing with Si nanowires.[34], [35], [33], [32], [36], [37]

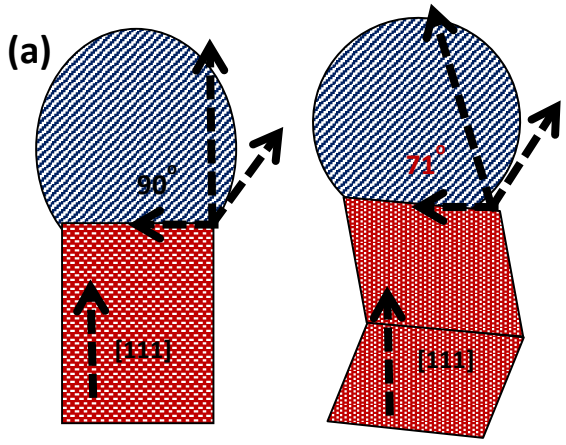


Figure 1: *Illustration of catalyst-nanowire interface and contact angle fluctuation for twin plane generation.*

Solid phase seeding in a three phase growth paradigm is a feasible way to introduce longitudinal twin defects in the {111} plane for <112>-oriented nanowires. Theoretically a solid seed should enable the transfer of crystal information to a growing material similar to the defect-supported growth of nanowires "seeded" by screw dislocation translations from epitaxial substrates to the growing material [38]. There are therefore distinct features of the

solid phase seeding mechanism that potentially offer opportunities for the controlled processing of nanomaterials with new physical properties. In this regard, we have introduced and demonstrated an epitaxial defect transfer process [39] from a solid catalyst seed into a nanowire. This technique was touted as a viable technique to introduce large numbers (> 50 %) of axial twin boundaries in <112> directed Ge nanowires. Requirements for this defect transfer process included: (i) matching lattice constant and crystal structure of the catalyst and the growing nanowire, (ii) moderate solubility of the growth material in the solid seed, (iii) moderate twin formation energy of the nanoparticle seed and (iv) prevention of any VLS-like growth at the reaction temperature. Germanide forming seeds during nanowire growth are not suitable for defect transfer processes as they usually go through the structural rearrangement of atoms in the seed prior to nanowire growth, which will change the particle properties. Additionally, binary seeds are less predictable in terms of extended defect generation due to generally limited literature data on most of these compounds. Silver as the solid growth promoter was perfect to induce twinning in large numbers (~ 40 %) of Ge nanowires, due to the high eutectic point of the Ag-Ge system and the retention of the cubic crystal structure during growth, with little change in the volume of the seed.[39] Ag is also especially receptive to forming stacking faults [40], leading to a large amount of twinning formation in the seed nanocrystals. To increase the defect density in the seed material Ag nanocrystals of small sizes (d ~ 6 nm) were annealed at nanowire growth temperature ~ 400 °C, creating large numbers of stacking faults in the Ag seeds through *in-situ* fusion. The major growth direction of these nanowires was along the <112> axis (~40 %), which is known to show lamellar {111} twinning along the axis and represents the identical planes present in Ag crystals. The regular appearance of twin planes in the Ag seed particles and in the corresponding Ge nanowires grown from them are shown in Figure 2a; similar diffraction contrasts visible in the Ag particles and the body of the Ge nanowires confirmed the epitaxial defect transfer process. The

interfaces of the segments in the Ge crystal were identified as (111) stacking faults (inset of Figure 2a). Considering the strain between both Ag and Ge cubic crystals, due to a lattice mismatch of ~3.5 % (4 Ag and 3 Ge {111} planes), the Ag-Ge binary system can relax for thin nanowires by tilting the Ag nanoparticle off-axis along with the {111} planes in the nanocrystal (Figure 2b). This tilting possibly occurred during cooling of the system and depletion of Ge in the Ag seed matrix. The resulting quasi-widening of the interface lattice spacing helps to minimise strain between both crystals. Most of these twinned terminating metal particles have rough interfaces resulting in steps (inset of Figure 2b). The creation of a defect site in the semiconductor nanowire was observed at these kinked interface sites.

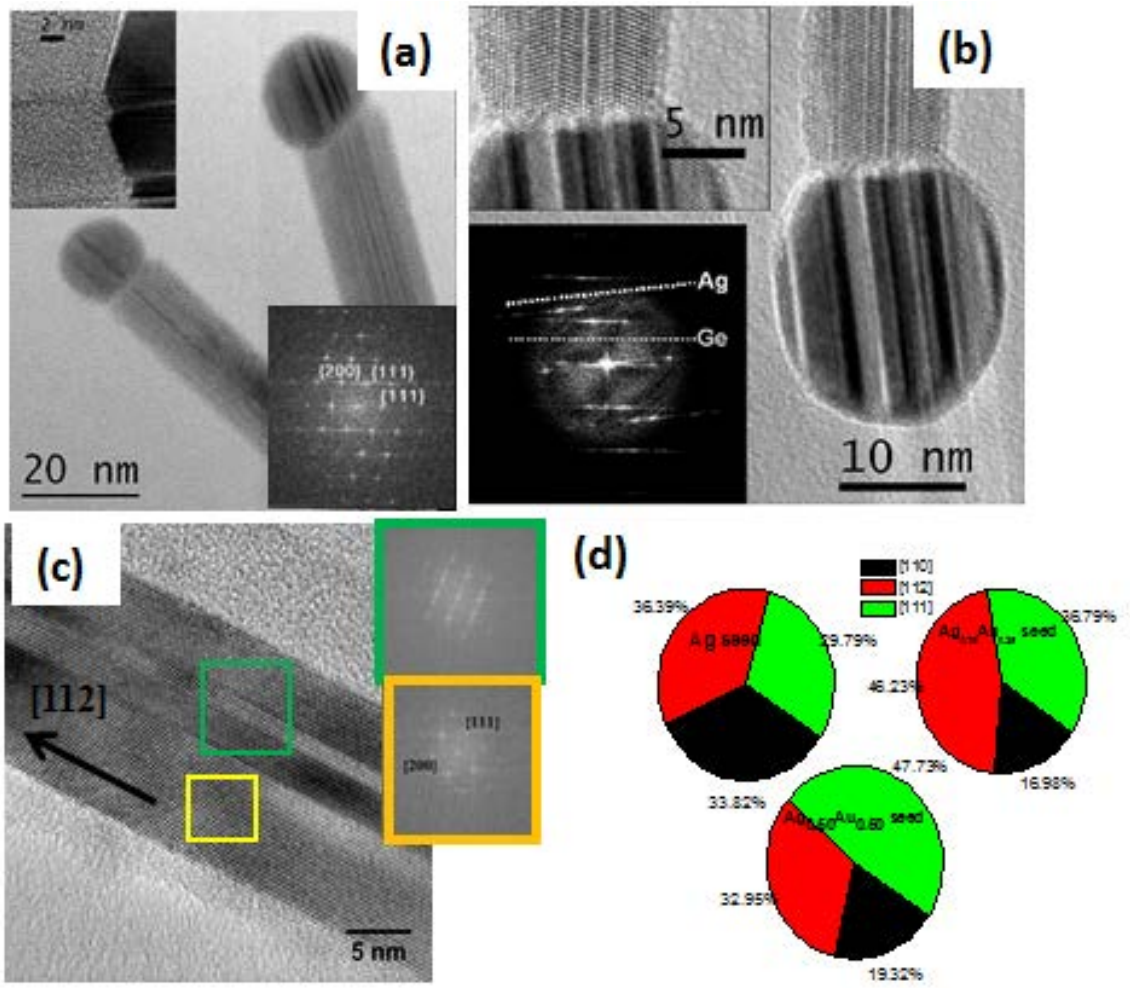


Figure 2: *(a) TEM image showing defect Transfer in Ag seed to Ge nanowires. The inset shows the interface between the seed particle with steps, which influences the Ge lattice of the growing nanowire. The other inset demonstrates the FFT pattern of single crystalline segment of the nanowire. HRTEM images in (b) illustrate the formation of {111} twin planes and the defect transfer from the Ag seeds to the Ge nanowires, the different segments are clearly visible with similar thickness (adopted from ref. 28). Part (c) illustrates the formation of {111} twin planes with <112> growth axis for nanowires growth with AuAg alloy seed. (d) TEM investigations show highest number of <112> oriented twinned nanowires formation for* $Ag_{0.25}Au_{0.75}$ *alloy seed.*

The high number of <112>-oriented Ge nanowires observed with the defect transfer process suggests a preferential nucleation of these unusual wires when compared to other growth seeds, which could be an effect of the twinning. Normally the nucleation centres for twinning at nanoparticle-nanowire interfaces are positions of highly localised strain in the lattice [36], which could be due to stacking faults at the interface between metal seeds and growing nanowires. Usually twinning defects formed during nucleation in metal seed-semiconductor nanowire interfaces provide a preferential addition site at the triple phase boundary for diffusing species and maintaining subsequent growth in the <112> direction.[39] Also defect sites in the seed particles can act as a favoured diffusion pathway for semiconductor atoms to be attached at the triple phase boundary.[41] After the nucleation of twins at a metal seed-semiconductor interface, during the layer-by-layer growth of a nanowire, ledge nucleation remains immobilised at the twinning boundary, thus preventing access of Si or Ge adatoms to low energy {111} facets, promoting the propagation of twin planes along the nanowire [112] axes.[36]

The “epitaxial defect transfer” process to induce large amount of twins in <112> directed nanowires was further verified with binary alloy catalysts.[28] In binary alloy catalysts, the density of planar defects in the catalyst seed particles can potentially be varied by alloying seeds with different intermetallic compositions, Au and Ag in our case. Differing amounts of Ag and Au in the alloy nanoparticles changes the stacking fault energy and interparticle diffusion chemistry of the nanoparticles, which in turn is utilised to vary crystallographic information in the collector seed particles and subsequently the nanowires grown from them, through epitaxial knowledge transfer. An “epitaxial defect transfer” process; similar to the Ag seed mediated twin formation was also responsible for the defect induction in semiconductor Ge nanowires from the binary metal catalysts (Figure 2c). Three different binary alloy catalysts

were explored to control twin formation in Ge nanowires. The probability of forming planar defects in the seed particles as a function of Ag and Au composition, *i.e.* Ag, $Ag_{0.50}Au_{0.50}$, $Ag_{0.75}Au_{0.25}$ allowed the distribution of defects in the growing Ge nanowires to be manipulated. Three competing factors participated together in determining the overall defect distribution in the seed particles and the subsequent transfer of these defects into the Ge nanowires: (i) twin energies of the constituent metals in the alloy: Ag with a lower twin energy than Au will encourage greater twin formation in Ag and Ag rich alloy nanoparticle seeds, (ii) the presence of multiple twinned nanoparticle seeds, using the corresponding cohesive energies for each system, a higher probability of forming multiple twinned particle (MTP) in the as-synthesised alloy nanoparticles than in phase pure Ag nanoparticles is predicted [42] and (iii) the nature of attachment of these nanoparticles during coalescence upon heating; softer interparticle interaction during the coalescence process will encourage a greater twinning in the annealed growth seeds.[43] The most favourable defect formation kinetics was observed for $Au_{0.25}Ag_{0.75}$ nanoparticle seeds through the epitaxial defect transfer mechanism (Figure 2d). Differences in stacking fault energy, formation enthalpy and coalescence chemistry for alloy seeds with varying intermetallic compositions result in distinctive twin formation in nanoparticle seeds, enabling overall control over twin formation in Ge nanowires. With the knowledge gained from using different binary alloy seeds for twin formation in Ge nanowires, a metal seed with a low twinning energy and controlled grain boundary diffusion can be predicted to cause unprecedented numbers of periodic twinning events in group IV nanowires.

Transverse twin boundary perpendicular to nanowire growth axis. If the formation of periodic twins along the axis of a <112> directed group IV nanowire is challenging, the formation of periodic twins and polytypism in <111>-directed group IV nanowires, where the twin plane bisects the nanowires perpendicular to the growth direction, is even more

demanding. The twin formation energy in a cubic system (zinc blende or diamond) is typically half the stacking fault energy and normally less than the thermal energy, k_BT (k_B is the Boltzman constant), provided in the system during growth at the usual process temperature (~ 400 ºC). Although twinning energies for zinc blende and diamond crystals are not very different, {111} twins form very easily in <111>-oriented zinc blende nanowires (InP, GaAs *etc*.)[44, 45], but not in the diamond lattices (Ge, Si), especially when using Au as a catalyst. Random transverse twin events in Si nanowires have been demonstrated with different non-Au catalysts such as Cu[46], Al[47], Ga[48], AuAg[49], *etc*. The first demonstration of controlled rational generation of transverse twin boundaries in Au-catalysed Si nanowires was reported by Shin *et al.*[50] Characteristic saw-tooth faceting in nanowire morphology, due to twin boundary formation, was observed in Si nanowires. In their case, twin boundary formation was influenced by changes to the solid-vapour interface chemistry near the triple-phase contact line, which occurred upon modulation of the growth conditions. Fabrication of multiple transverse twin boundaries were also achieved in <111> oriented Si nanowires.[51] First a twin boundary was driven by inward moving {111} facets that formed following an abrupt increase in disilane pressure and a decrease of the substrate temperature. Another twin boundary resulted from a different set of thin {111} facets that traversed the {110} sidewalls. The formation mechanisms of both twin boundaries deform the triple-phase line and favour twin nucleation.

Recently, in our group, we have used innovative nanoparticle growth promoters to engineer catalyst-nanowire interface to influence the formation of transverse twin boundaries perpendicular to nanowire growth axis. Controlled transverse twin formation in Ge nanowire was initiated through the use of new growth promoter such as patterned hemispherical magnetite nanodots.[29] These particular magnetite nanodot catalysts were suitable, due to the

particular curvature of the catalyst-substrate and catalyst-nanowire interface and the adherence of the patterned nanodots with a substrate, to promote the growth of large numbers of <111> oriented Ge nanowires with lateral growth of twin planes perpendicular to the nanowire growth axis (Figure 3a). A 60° rotation of crystal orientation on both sides of the twin planes with the growth axis represents a mirror reflection of a 3C stacking order of the {111} planes without any bond-breakage at the interface (Figure 3b). Periodic modulations of altering (-1-11) and (-1-1-1) 3C cubic lateral facets, making an angle of ~ 141º were observed when viewed along the <110> zone axis (Figure 4b). Orientation of critical nuclei at the interface determines the formation of twin or normal plane crystals because of the difference in the energy barrier for twin and normal plane nucleation is very small. The presence of both Fe^{2+} and Fe^{3+} ions in the Fe_3O_4 nanodots induced competitive kinetics in the germination process during nanowire growth, thus generating enormous strain at the catalyst-substrate and catalyst-nanowire interface. Competitive germination processes within the nanodots resulted in a stretching and narrowing of the hemispherical seed-substrate and seed-nanowire interface, thus triggering the formation of nanofaceted side-walls[52] and lateral twin boundaries at the seed-nanowire interface. Additionally, a pseudoepitaxial relationship between the complex alloy catalyst and the Ge nanowires influenced the layer-by-layer arrangement in the triple phase interface to promote lateral stacking faults.

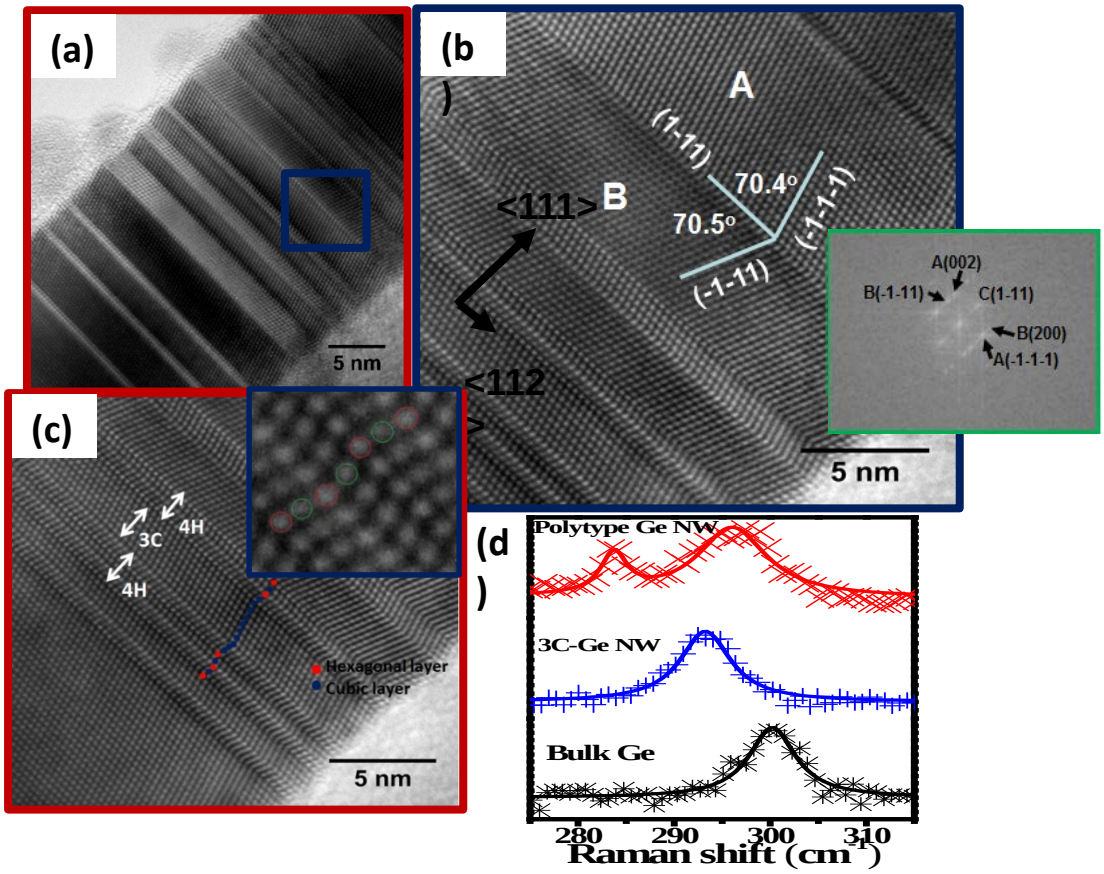


Figure 3: *Parts (a) bright-filed TEM images with lateral twin boundaries perpendicular to the <111> nanowire growth axis. HRTEM image in part (b) shows the formation of {111} twin planes where two 3C mirror segments (A and B) are separated by twin boundaries (also shown in the FFT pattern in the inset). The angle between the nanofacets were measured to be ~ 141°. The HRTEM image shown in (c) and the inset portray the formation of a 4H-polytype in a 3C diamond cubic nanowire. Different polytype regions are marked by colour dots. (d) Raman spectra of 3C-Ge, polytype and bulk Ge nanowires with laser power density of 1 mW/ μm^2. (Adopted from ref. 38)*

The formation of densely ordered transverse twin boundaries can influence the local crystal structure of nanomaterials.[53], [54] Periodic twinned planes can generate polytype superstructures where stacking faults in the *ABC* stacking sequence along the <111> direction can produce local hexagonal ordering in a cubic crystal, for example, *ABA*, leading to polytypes

with distinctly unique properties. The polytype combination of lonsdaleite (2H)/diamond (3C) leads to a type-I heterostructure, where both electrons and holes are localised in the region of the hexagonal polytype. These novel structures can act as crystal phase quantum dots in a chemically homogeneous nanowire.[55] In our case, Ge nanowires (diameters > 20 nm) grown from Fe_3O_4 nanodots displayed changes from tetrahedrally co-ordinated 3C crystals to 4H polytypes (Figure 3c).[29] Local diversion of *abcabc* stacking of close-packed atomic arrangement in a (111) plane in a diamond-type cubic structure (Ge-I) in Ge nanowires locally changed to an $a^{"}b^{"}c^{"}b^{"}a^{"}b^{"}c^{"}b^{"}$ arrangement of the 4H-Ge polytype with a 50 % hexagonal layer. The presence of polytype structures in the Ge nanowires introduces strain which shifts the Ge-Ge vibrational mode towards a higher wavenumber, as observed by Raman spectroscopy.[56] An additional Raman peak situated at 284 cm^{-1} was detected for the polytype nanowires (Figure 3d), assigned to the deviation from the 3C stacking sequence and the presence of 4H Ge in the nanowires, where the stacking fault modifies the Raman polarisability tensors. The vibrational modes of 4H Ge can be obtained by folding the Brillouin zone of a diamond lattice.[57] This particular crystal phase heterostructure has great potential for photonics and thermoelectric applications.

2.2 Non-equilibrium impurity induction in nanowire. Based on thermodynamic limitations, a non-equilibrium growth scenario influenced by the kinetics of the system is required to incorporate a large amount, far from equilibrium, of metal impurities into a one-dimensional lattice. The triple-phase boundary at the catalyst-nanowire interface in a bottom-up growth process is known to be a feasible pathway for impurity incorporation in a one-dimensional lattice and can act as a localised non-equilibrium centre for excessive impurity dissolution.[58, 59] A kinetic-dependent framework was predicted to be responsible for the extraordinary incorporation of impurity adatoms from the catalyst tip. Particularly, non-equilibrium

induction of impurities in the host (Ge in this case) is justified through diffusionless solute trapping at a finite growth velocity of the crystals. 'Solute trapping' is a process of solute redistribution at the interface resulting in an increase of chemical potential and deviation of partition coefficient. In the case of nanowire growth, local chemical equilibrium at the alloy solidification front at the liquid (seed)-solid (nanowire) interface is relaxed due to a large interface velocity resulting in kinetic interface undercooling. At a high solidification rate at the catalyst-nanowire interface impurity adatoms can be trapped on the high energy sites of the crystal lattice, leading to the formation of metastable solids, for example $Ge_{1-x}Sn_x$ with non-equilibrium Sn content at the nanowire growth front.

Taking advantage of solute trapping at fast growth kinetics in three phase bottom-up growth protocol, we have recently reported fabrication of highly crystalline, uniform diameter, direct bandgap $Ge_{1-x}Sn_x$ nanowires with considerable ($x > 0.09$) Sn incorporation; around 10 times the equilibrium solubility.[60] Different third-party metal catalysts (Au or AuAg alloy) were used to alter nanowire growth kinetics to guide the non-equilibrium incorporation of Sn adatoms into the precipitated Ge bi-layers, where the impurity Sn atoms become trapped with the deposition of successive layers, thus giving an extraordinary Sn content in the alloy nanowires. Nanowire growth at 440 ºC with a AuAg alloy growth promoter resulted in a Sn assimilation of 6.3 at.% in Ge through solute trapping (Figure 4a). These values of Sn concentration is much higher (almost 6 times) than the extrapolated bulk equilibrium solid solubility of Sn in Ge.[31] During the bottom-up growth, the incorporation of Sn in the Ge nanowires through nanowire sidewalls due to homoepitaxy and vapour-solid growth is also negligible, as the nanowires were not tapered and demonstrated a uniform Sn distribution (Figure 4b). The role of kinetic factors in the non-equilibrium incorporation of Sn in Ge is also profound from the fact that the amount of Sn incorporated in the nanowires increased upon

using AuAg catalysts which promotes faster Ge nanowire growth kinetics than Au seeds.[61, 62]

The non-equilibrium induction of Sn as an impurity in the Ge host was justified through diffusionless solute trapping at a finite growth velocity of the crystals. During VLS-like growth of Ge nanowires, local chemical equilibrium at the alloy solidification front at the liquid (seed)-solid (nanowire) interface is relaxed due to a large interface velocity resulting in kinetic interface undercooling. At a high solidification rate at the catalyst-nanowire interface Sn impurity adatoms are trapped on the high energy sites of the crystal lattice, leading to the formation of $Ge_{1-x}Sn_x$ metastable solids at the nanowire growth front. For the particular case of $Ge_{1-x}Sn_x$ nanowires we have proposed a few factors which aided the kinetic incorporation of Sn. The fact that Sn diffusion in Ge at our growth conditions was negligible helped trapping of Sn at the interface. Also the epitaxial mismatch between Sn and Ge results in elastic strains at and near the catalyst-nanowire interface and this elastic strain accommodates a high Sn incorporation into the newly forming layer relative to the pristine Ge crystal. Finally, at equilibrium the catalyst-nanowire interface is expected to have truncated side facets.[63] These truncating facets are absent in $Ge_{1-x}Sn_x$ nanowires and the interface is fully faceted which is indirect confirmation of the elastic strains due to non-equilibrium Sn incorporation. As a result, the Sn incorporation is uniform through the nanowire, as opposed to being localised at the core or within a surface shell (Figure 4b).

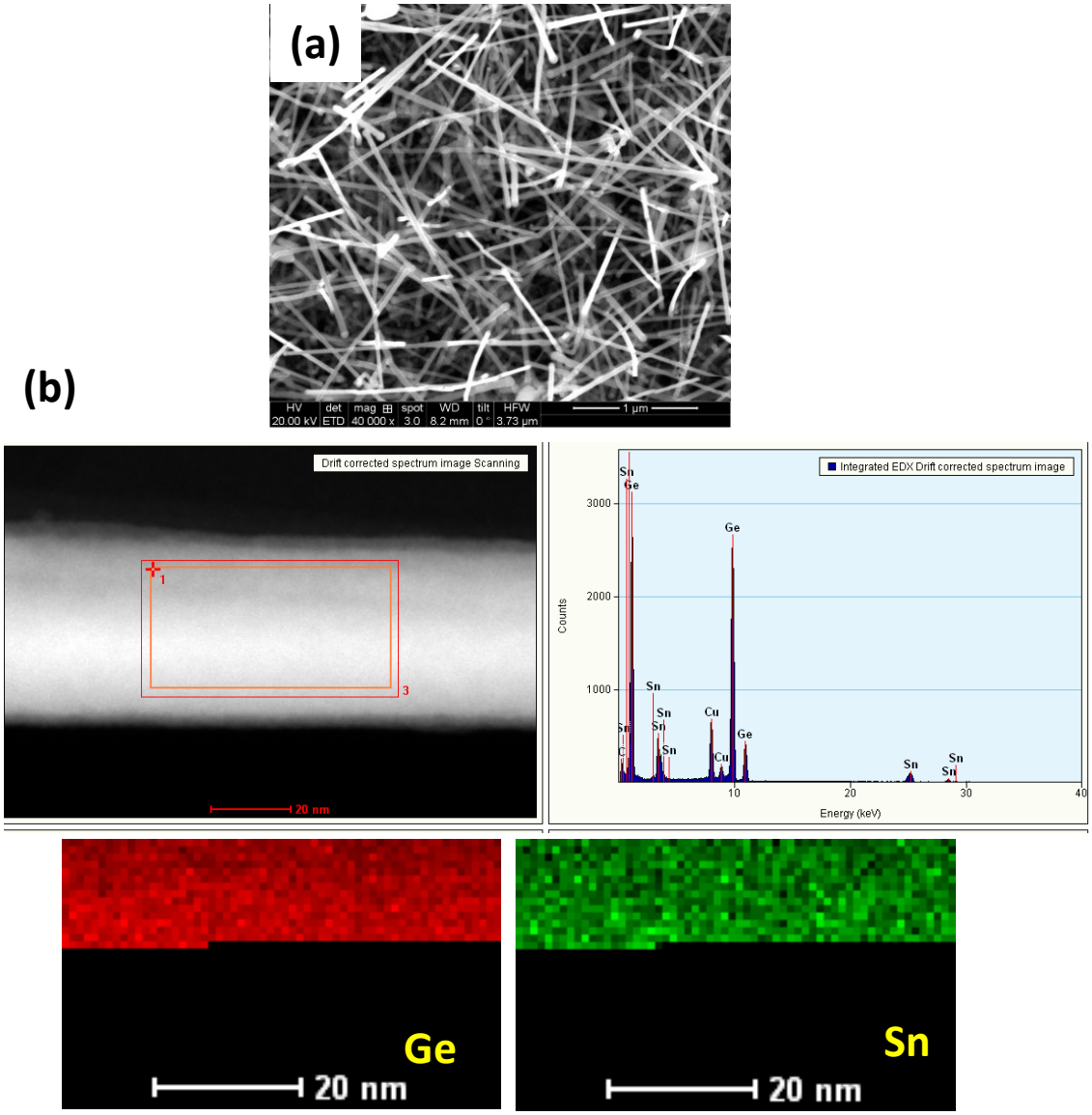


Figure 4: *(a) Scanning electron microscopy (SEM) image of* $Ge_{1-x}Sn_x$ *nanowire. (b) EDX spectra shows Sn inclusion in Ge nanowire and EDX mapps depict uniform Sn distribution. (adopted from ref. 60).*

Assuming that growth of the nanowire is layer by layer, the step flow kinetics can result in solute trapping of Sn from the Sn-rich droplet. In the nanoscale system, where the crystal growth proceeds with the formation of steps at the interface, impurity atoms remain frozen at the step edges upon the formation of a new row of atoms. Hence, impurity incorporation during

nanowire growth depends on the step velocity rather than on the interface velocity. With a high step velocity, the time required for local impurity exchange at the catalyst-nanowire interface decreases thus the rate of solute trapping increases in the nanowire. The growth velocity of $Ge_{1-x}Sn_x$ nanowires is much lower (~ 0.5-1 nm sec^{-1}) than the growth velocity required for kinetic driven solute trapping. However, for our particular system a much higher Sn concentration in the catalyst seed (greater than 90 at.%) than the impurity concentration in a typical bulk solidification process, and a continuous Sn flux throughout nanowire growth could account for the high Sn incorporation.

We have further encouraged Sn dissolution in Ge nanowires from 6.3 to 9.2 at.% via a step cooling process with a 2 hr annealing at 230 ºC, during the cooling down of nanowires (Figure 5a). The choice of the step cool down process and temperature was driven by the existence of a small Sn precipitation window at the lowest eutectic, near the Sn rich side of the binary bulk Au-Sn phase diagram[64], at around 215-230 ºC. Although there is a large lattice mismatch between the components (Ge and Sn) of the alloy, the epitaxial mismatch in the nanowires with a large influx of Sn is compensated by elastic deformation near the hetero-interface and relieved at the nanowire surfaces, thus maintaining highly crystalline nanowires (Figure 5b). The liquid eutectic catalyst at the tip of the nanowires can also naturally accommodate elastic strain.

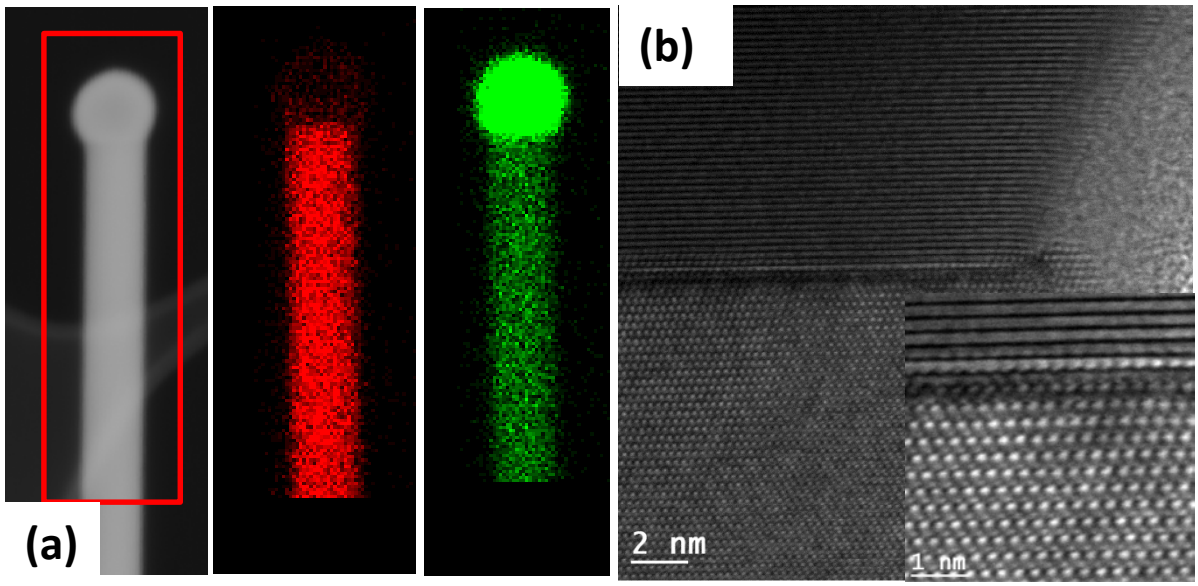


Figure 5: *(a) EDX mapping for* $Ge_{1-x}Sn_x$ *nanowire with 9.2 at.% Sn shows uniform Sn distribution throughout the length of the nanowires and a Sn rich seed. (b)* Lattice-resolved STEM HAADF image recorded near seed-nanowire interface (magnified image in the inset) shows single crystalline nature of the nanowire and abrupt catalyst-nanowire interface. *(adopted from ref. 60).*

We have proposed a deposition and dissolution based process for the increase incorporation of Sn in the alloy nanowires, where Sn precipitation from the supersaturated catalyst drop is encouraged at 230 ºC.[60] Precipitated Sn from the supersaturated catalyst gets further dissolved into the Ge nanowire host lattice at 230 ºC due to the eutectic solubility. Metastability and continuous dissolution of Sn in the Ge host at the eutectic temperature encourages large Sn dissolution. A very large amount of Sn could be dissolved in the Ge lattice in the metastable state as projected in the Ge-Sn phase diagram. Coincidence of a Sn precipitation window for the Au-Sn (or AuAg-Sn) binary system and the eutectic temperature (at 230 ºC) of the Ge-Sn binary system encourages the homogeneous dissolution of precipitated Sn from the catalyst

drop in the Ge nanowires at the eutectic temperature (Figure 5a). We predicted that a precipitation-dissolution based process is liable for this large Sn influx rather than a diffusion mediated incorporation process during step annealing. A diffusion based process during step annealing would have resulted in non-uniform Sn distribution, with a large Sn concentration near the seed-nanowire interface, with a continuous drop in the Sn concentration along the nanowire length. Analysis of $Ge_{1-x}Sn_x$ sample grown following the step cool-down process does not demonstrate this trend but shows a similar distribution of Sn along the length of nanowires.

Three phase catalytic bottom-up growth was demonstrated as a feasible pathway, via catalyst-crystal interface, to incorporate large amount of impurities and dopants in semiconductor nanowires. An innovative nanowire growth process involving alloy metal catalysts, kinetic driven solute trapping and eutectic dissolution of impurities in nanowire together influenced colossal injection of Sn in Ge. Demonstration of colossal incorporation of foreign atoms in the host semiconductor lattice allows new or added functionalities (strain engineering, controlled defect formation, band structure modulation *etc.*) in the existing semiconductor architecture.

Outlook

Engineered nanostructures with intentional addition of crystal defects or impurities inject new or added functionalities such as strain engineering, band structure manipulation, manipulation of phonon transport *etc*. With regards to engineered crystal defects, the control of twin periodicity in group IV nanowires offers the possibility of band structure engineering and interesting thermoelectric properties through modulated side faceting. Twinning and surface faceting can induce inhomogeneous stress fields which locally affect the conduction and valence band potential, thus altering electronic band structure.[23] Periodic twinned planes in

semiconductor nanowires can also generate polytype superstructures, where stacking faults in the *abc* stacking sequence, along the <111> direction, can produce local hexagonal ordering in a cubic crystal, for example *ABA* packing, leading to polymorphs with distinctly unique optical and electrical properties.[18, 55, 65] Importantly, the generation of controlled twinned and polytype defects within individual nanowires allows the realisation of heterostructures from a single component semiconductor, with perfect lattice matching and preserved interface bonds. These polytype nanowire structures potentially augment electron scattering at the interfaces between the different crystal phases, permitting the formation of superlattice states, as the Bloch wave functions in the two adjacent layers are quite different due to different band structure and crystal orientation.

Existing knowledge about how nucleation and growth kinetics can effect twin boundary and polytype formation, through control over the triple phase contact lines and droplet morphology in VLS/VSS-like growth models, could be applied to engineer nanowire superstructures. An ultimate aim would be to utilise growth engineering at the interfaces to form twinning superlattices or polytypic superstructures in elemental group IV nanowire systems with a range of new physical properties. The controlled synthesis of twinned superstructures or polytype heterostructures allows realisation of fabricating inhomgeneous heterostructures from single semiconductor materials, with perfect lattice matching and bond preservation at interfaces. A polytype superlattice would consist of a specific periodic polytype sequence containing both fcc and hcp portions of the same semiconductor. Superlattices formed from twinned nanowires would allow the formation of periodic scattering centres, by varying the crystal orientation, without the formation of stress at the interfaces. Although the interface between two crystal orientations is perfectly lattice matched for a twinned superlattice, the wave functions are highly symmetry mismatched. This makes the twinning superlattice a periodic heterostructure,

although it consists of same composition and lattice type. Because electronic band structures can differ markedly between hexagonal and cubic crystals in semiconductors, twin interfaces have a direct impact on band-gap and band profiles due to their unique structure as hexagonal monolayers. The band offset between different crystal structures could therefore be used to create new types of quantum structure, *e.g.* crystal phase quantum dots. However, uncontrolled variation of the crystal structure in nanowires could be detrimental to electron transport. Surface faceting associated with saw-tooth facets of nanowire superstructures can significantly decrease the thermal conductivity in nanowires, suggesting that twinned superlattices may also play a crucial role in thermal transport characteristics due to surface effects. A direct correlation between twin density and optical properties can also be obtained with coherent twinning superlattice nanowires, which holds great promise for optoelectronics and solar cell applications. To achieve crystal phase superlattice structures with controlled dimension of twinned and/or polytype regions in a nanoscale elemental semiconductor is challenging. We believe that, further understanding of the kinetics and thermodynamics of nanowire growth and knowledge of morphology and structure of the growth interface through in-situ monitoring, will aid the realisation of twinned phase superlattice or polytype superlattice structures in group IV nanowires.

Metal impurities in nanoscale system could also alter the band structure to convert an indirect bandgap semiconductor, such as Si and Ge, to direct bandgap semiconductor.[8, 9] Especially for Ge, the small energy separation of 140 meV between the indirect (L) and direct (Γ) conduction band valleys can be overcome by alloying with Sn or Pb. VLS growth processes with different catalysts and precursors can influence kinetic dependent metal incorporation in Ge (or Si) nanowires. Manipulation of growth temperature, choice of precursors and catalysts could lead towards $Ge_{1-x}Sn_x$ nanowires with higher a Sn content of greater than 10 at.%. Two stage growth

protocols involving kinetic dependent solute trapping at higher temperatures and subsequent eutectic dissolution of impurities at relatively low temperature could be applied to other doped or alloy nanowire systems (for example III-V nanowires, ternary alloy nanowires etc.) to create new and innovative nanomaterials for novel physics and devices. This impurity incorporated Ge material also addresses towards the ongoing demand for an active nanoscale material for group IV photonics. The demonstration of direct bandgap Si compatible nanowires will instigate a lot of initiative on fundamental research on band structure engineering of binary and ternary group IV alloy nanowires and implementation of these nanoscale materials in photic and electronic devices. Future focus could also be on the development of ternary nanoscale alloy materials in group IV regime. The great success of III-V quaternary semiconductors in decoupling strain and band-structure effects suggests that ternary compounds should have a similar impact in the group IV arena.

Acknowledgements

We acknowledge financial support from Science Foundation Ireland (SFI Grant: 14-IA-2513) and SFI International Strategic Co-operation Award (ISCA) India-Ireland program.

References:

[1] Bjork, M.T., et al., *One-dimensional steeplechase for electrons realized. Nano Letters,* **2002**. *2(2)*: p. 87-89.

[2] Li, Y., et al., *Nanowire electronic and optoelectronic devices. Materials Today,* **2006**. *9(10)*: p. 18-27.

[3] Leonard, F., et al., *Diameter-dependent electronic transport properties of Au-catalyst/Ge-nanowire Schottky diodes. Physical review letters*, **2009**. *102(10)*: p. 106805.

[4] Xiang, J., et al., *Ge/Si nanowire heterostructures as high-performance field-effect transistors. Nature*, **2006**. *441(7092)*: p. 489-493.

[5] Heath, J. and LeGoues, F., *A liquid solution synthesis of single crystal germanium quantum wires. Chem. Phys. Lett.*, **1993**. *208(3-4)*: p. 263-268.

[6] Tuan, H.Y., et al., *Germanium nanowire synthesis: An example of solid-phase seeded growth with nickel nanocrystals. Chem. Mater.*, **2005**. *17(23)*: p. 5705-5711.

[7] Petkov, N., et al., *Growth of ordered arrangements of one-dimensional germanium nanostructures with controllable crystallinities. Chem. Mater.*, **2008**. *20(5)*: p. 1902-1908.

[8] Lu, X.M., et al., *High yield solution-liquid-solid synthesis of germanium nanowires. J. Am. Chem. Soc.*, **2005**. *127(45)*: p. 15718-15719.

[9] Andzane, J., et al., *Two-Terminal Nanoelectromechanical Devices Based on Germanium Nanowires. Nano Lett.*, **2009**. *9(5)*: p. 1824-1829.

[10] Ziegler, K.J., et al., *Bistable nanoelectromechanical devices. Appl. Phys. Lett.*, **2004**. *84(20)*: p. 4074-4076.

[11] Chockla, A.M., et al., *Solution-Grown Germanium Nanowire Anodes for Lithium-Ion Batteries. ACS Appl. Mater. Inter.*, **2012**. *4(9)*: p. 4658-4664.

[12] Seo, M.H., et al., *High performance Ge nanowire anode sheathed with carbon for lithium rechargeable batteries. Energy Environ. Sci.*, **2011**. *4(2)*: p. 425-428.

[13] Chan, C.K., Zhang, X.F., and Cui, Y., *High capacity Li ion battery anodes using Ge nanowires. Nano Lett.*, **2008**. *8(1)*: p. 307-309.

[14] Burchhart, T., et al., *Atomic Scale Alignment of Copper-Germanide Contacts for Ge Nanowire Metal Oxide Field Effect Transistors. Nano Lett.*, **2009**. *9(11)*: p. 3739-3742.

[15] Garfunkel, E., et al., *PMSE 454-Germanium nanowires poly(3-hexylthiophene) composites for photovoltaic applications. Abstr. Pap. Am. Chem. S.*, **2008**. *236*.

[16] Nguyen, P., Ng, H., and Meyyappan, M., *Growth of individual vertical germanium nanowires. Adv. Mater.*, **2005**. *17(5)*: p. 549-553.

[17] Cullis, A., Canham, L., and Calcott, P., *The structural and luminescence properties of porous silicon. J. Appl. Phys.*, **1997**. *82*: p. 909.

[18] Wood, E.L. and Sansoz, F., *Growth and properties of coherent twinning superlattice nanowires. Nanoscale*, **2012**. *4(17)*: p. 5268-5276.

[19] Tsuzuki, H., et al., *Tailoring Electronic Transparency of Twin-Plane 1D Superlattices. ACS Nano*, **2011**. *5(7)*: p. 5519-5525.

[20] Sansoz, F., *Surface Faceting Dependence of Thermal Transport in Silicon Nanowires. Nano Letters*, **2011**. *11(12)*: p. 5378-5382.

[21] Algra, R.E., et al., *Twinning superlattices in indium phosphide nanowires. Nature*, **2008**. *456(7220)*: p. 369-372.

[22] Caroff, P., et al., *Controlled polytypic and twin-plane superlattices in III-V nanowires. Nature Nanotechnology*, **2009**. *4(1)*: p. 50-55.

[23] Ikonic, Z., Srivastava, G.P., and Inkson, J.C., *ELECTRONIC-STRUCTURE OF TWINNING SUPERLATTICES. Surface Science*, **1994**. *307*: p. 880-884.

[24] Ikonic, Z., Srivastava, G.P., and Inkson, J.C., *OPTICAL-PROPERTIES OF TWINNING SUPERLATTICES IN DIAMOND-TYPE AND ZINCBLENDE-TYPE SEMICONDUCTORS. Physical Review B*, **1995**. *52(19)*: p. 14078-14085.

[25] Xiong, S., et al., *Tunable thermal conductivity in silicon twinning superlattice nanowires. Physical Review B*, **2014**. *90(19)*: p. 195439.

[26] Hochbaum, A.I., et al., *Enhanced thermoelectric performance of rough silicon nanowires. Nature,* **2008**. *451(7175)*: p. 163-167.

[27] Wagner, R.S. and Ellis, W.C., *VAPOR-LIQUID-SOLID MECHANISM OF SINGLE CRYSTAL GROWTH (NEW METHOD GROWTH CATALYSIS FROM IMPURITY WHISKER EPITAXIAL + LARGE CRYSTALS SI E). Applied Physics Letters,* **1964**. *4(5)*: p. 89.

[28] Biswas, S., et al., *Inherent Control of Growth, Morphology, and Defect Formation in Germanium Nanowires. Nano Letters,* **2012**. *12(11)*: p. 5654-5663.

[29] Biswas, S., et al., *Diameter Controlled Germanium Nanowires with Lamellar Twinning and Polytypes. Chemistry of Materials*, **2015**.

[30] Davidson, F.M., et al., *Lamellar twinning in semiconductor nanowires. Journal of Physical Chemistry C,* **2007**. *111(7)*: p. 2929-2935.

[31] Johansson, J., et al., *Structural properties of (111)B-oriented III-V nanowires. Nature Materials,* **2006**. *5(7)*: p. 574-580.

[32] Su, Z., et al., *Crystal growth of Si nanowires and formation of longitudinal planar defects. Crystengcomm,* **2010**. *12(10)*: p. 2793-2798.

[33] Liu, X.H. and Wang, D.W., *Kinetically-Induced Hexagonality in Chemically Grown Silicon Nanowires. Nano Research,* **2009**. *2(7)*: p. 575-582.

[34] Conesa-Boj, S.n., et al., *Defect Formation in Ga-Catalyzed Silicon Nanowires. Crystal Growth & Design*, **2010**. *10(4)*: p. 1534-1543.

[35] Cayron, C., et al., *Odd electron diffraction patterns in silicon nanowires and silicon thin films explained by microtwins and nanotwins. Journal of Applied Crystallography,* **2009**. *42(2)*: p. 242-252.

[36] Dayeh, S.A., et al., *Growth, Defect Formation, and Morphology Control of Germanium-Silicon Semiconductor Nanowire Heterostructures. Nano Letters*, **2011**. *11(10)*: p. 4200-4206.

[37] Shin, N., Chi, M., and Filler, M.A., *Interplay between Defect Propagation and Surface Hydrogen in Silicon Nanowire Kinking Superstructures. ACS Nano*, **2014**. *8(4)*: p. 3829-3835.

[38] Morin, S.A. and Jin, S., *Screw Dislocation-Driven Epitaxial Solution Growth of ZnO Nanowires Seeded by Dislocations in GaN Substrates. Nano Letters*, **2010**. *10(9)*: p. 3459-3463.

[39] Barth, S., Boland, J.J., and Holmes, J.D., *Defect Transfer from Nanoparticles to Nanowires. Nano Letters*, **2011**. *11(4)*: p. 1550-1555.

[40] Major, S.S. and Grosskre.Jc, *THERMAL BEHAVIOR OF STACKING FAULTS IN SILVER FILMS. Japanese Journal of Applied Physics*, **1968**. *7(6)*: p. 574-&.

[41] Germain, V., et al., *Stacking faults in formation of silver nanodisks. Journal of Physical Chemistry B*, **2003**. *107(34)*: p. 8717-8720.

[42] Qi, W.H. and Lee, S.T., *Phase Stability, Melting, and Alloy Formation of Au-Ag Bimetallic Nanoparticles. Journal of Physical Chemistry C*, **2010**. *114(21)*: p. 9580-9587.

[43] Rupich, S.M., et al., *Size-Dependent Multiple Twinning in Nanocrystal Superlattices. Journal of the American Chemical Society*, **2010**. *132(1)*: p. 289-296.

[44] Hurle, D.T.J. and Rudolph, P., *A brief history of defect formation, segregation, faceting, and twinning in melt-grown semiconductors. Journal of Crystal Growth*, **2004**. *264(4)*: p. 550-564.

[45] Hurle, D.T.J., *A MECHANISM FOR TWIN FORMATION DURING CZOCHRALSKI AND ENCAPSULATED VERTICAL BRIDGMAN GROWTH OF III-V COMPOUND SEMICONDUCTORS. Journal of Crystal Growth*, **1995**. *147(3-4)*: p. 239-250.

[46] Arbiol, J., et al., *Influence of the (111) twinning on the formation of diamond cubic/diamond hexagonal heterostructures in Cu-catalyzed Si nanowires. Journal of Applied Physics*, **2008**. *104(6)*.

[47] Wang, Y., et al., *Epitaxial growth of silicon nanowires using an aluminium catalyst. Nature Nanotechnology*, **2006**. *1(3)*: p. 186-189.

[48] Conesa-Boj, S., et al., *Defect formation in Ga-catalyzed silicon nanowires. Crystal Growth & Design*, **2010**. *10(4)*: p. 1534-1543.

[49] Chou, Y.-C., et al., *Controlling the Growth of Si/Ge Nanowires and Heterojunctions Using Silver–Gold Alloy Catalysts. ACS nano*, **2012**. *6(7)*: p. 6407-6415.

[50] Shin, N., et al., *Rational Defect Introduction in Silicon Nanowires. Nano Letters*, **2013**. *13(5)*: p. 1928-1933.

[51] Shin, N., Chi, M., and Filler, M.A., *Sidewall Morphology-Dependent Formation of Multiple Twins in Si Nanowires. ACS Nano*, **2013**. *7(9)*: p. 8206-8213.

[52] Ross, F.M., Tersoff, J., and Reuter, M.C., *Sawtooth faceting in silicon nanowires. Physical review letters*, **2005**. *95(14)*.

[53] Jeon, N., Dayeh, S.A., and Lauhon, L.J., *Origin of Polytype Formation in VLS-Grown Ge Nanowires through Defect Generation and Nanowire Kinking. Nano Letters*, **2013**. *13(8)*: p. 3947-3952.

[54] Vincent, L., et al., *Novel Heterostructured Ge Nanowires Based on Polytype Transformation. Nano Letters*, **2014**. *14(8)*: p. 4828-4836.

[55] Akopian, N., et al., *Crystal Phase Quantum Dots. Nano Letters*, **2010**. *10(4)*: p. 1198-1201.

[56] Dillen, D.C., et al., *Raman spectroscopy and strain mapping in individual Ge-SixGe1-x core-shell nanowires. Physical Review B,* **2012**. *86(4)*.

[57] Lopezcruz, E. and Cardona, M., *RAMAN-SPECTRA OF 2 NEW MODIFICATIONS OF GERMANIUM - ALLO-GERMANIUM AND 4H-GE. Solid State Communications,* **1983**. *45(9)*: p. 787-789.

[58] Chen, W., et al., *Incorporation and redistribution of impurities into silicon nanowires during metal-particle-assisted growth. Nature communications,* **2014**. *5*.

[59] Moutanabbir, O., et al., *Colossal injection of catalyst atoms into silicon nanowires. Nature*, **2013**. *496(7443)*: p. 78-82.

[60] Biswas, S., et al., *Non-equilibrium induction of tin in germanium: towards direct bandgap Ge1-xSnx nanowires. Nature communications,* **2016**. *7*.

[61] Biswas, S., et al., *Manipulating the Growth Kinetics of Vapor–Liquid–Solid Propagated Ge Nanowires. Nano Lett.*, **2013**. *13*: p. 4044-4052.

[62] Biswas, S., et al., *In-situ Observations of Nanoscale Effects in Germanium Nanowire Growth with Ternary Eutectic Alloys. Small*, **2015**. *11(1)*: p. 103-111.

[63] Wang, H., et al., *Atomistics of vapour-liquid-solid nanowire growth. Nature communications*, **2013**. *4*: p. 1956-1956.

[64] Ciulik, J. and Notis, M.R., *THE AU-SN PHASE-DIAGRAM. Journal of Alloys and Compounds*, **1993**. *191(1)*: p. 71-78.

[65] Nakamura, J. and Natori, A., *Dielectric discontinuity at structural boundaries in Si. Applied Physics Letters,* **2006**. *89(5)*.