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HTML ABSTRACT + LINKS

High injection and carrier pile-up in lattice matched InGaAs/InP PN diodes for thermophotovoltaic applications

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This article analyzes and explains the observed temperature dependence of the forward dark current of lattice matched $In_{0.53}Ga_{0.47}As$ on InP diodes as a function of voltage. The experimental results show, at high temperatures, the characteristic current-voltage ($I-V$) curve corresponding to leakage, recombination, and diffusion currents, but at low temperatures an additional region is seen at high fields. We show that the onset of this region commences with high injection into the lower-doped base region. The high injection is shown by using simulation software to substantially alter the minority carrier concentration profile in the base, emitter and consequently the quasi-Fermi levels (QFL) at the base/window and the window/cap heterojunctions. We show that this QFL splitting and the associated electron ''pile-up'' (accumulation) at the window/emitter heterojunction leads to the observed pseudo-$n=2$ region of the current-voltage curve. We confirm this phenomenon by investigating the $I-V-T$ characteristics of diodes with an InGaAsP quaternary layer ($E_g=1$ eV) inserted between the InP window ($E_g=1.35$ eV) and the InGaAs emitter ($E_g=0.72$ eV) where it serves to reduce the barrier to injected electrons, thereby reducing the ''pile-up.'' We show, in this case that the high injection occurs at a higher voltage and lower temperature than for the ternary device, thereby confirming the role of the ''accumulation'' in the change of the $I-V$ characteristics from $n=1$ to pseudo-$n=2$ in the ternary latticed matched device. This is an important phenomenon for consideration in thermophotovoltaic applications. We, also show that the activation energy at medium and high voltages corresponds to the InP/InGaAs conduction band offset at the window/emitter heterointerface. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1644905]

I. INTRODUCTION

InGaAs/InP devices have applications in photodetection and photoemission and more recently in their application as thermophotovoltaic (TPV) convertors. TPV is very attractive because many of the losses associated with conventional photovoltaics such as nonabsorbed radiation from photons with energy smaller than the band gap of the active semiconductor and losses from thermalization of electron-hole pairs generated from photons with an energy larger than the band gap can be avoided with the use of so-called ''selective emitters,'' mirrors.[1] In an ideal world, with no losses, TPV cells can have theoretical efficiencies as high as 85%, under concentrated sunlight.[2] In practice, the highest efficiencies reached are much lower due to such factors as imperfections in the emitter, optical cavity and due to the intrinsic dark current in practical devices. Therefore, the minimization of this latter parameter among others is crucial to achieve high efficiency.

The dark current in a *p-n* diode is mainly a consequence of radiative and nonradiative losses. The radiative loss is generally attributed to the band–to–band recombination and the nonradiative losses to Shockley–Read–Hall and Auger recombination.

The aim of this work is to understand the nature of the dark current transport over a wide range of temperatures (80–330 K) and forward biases. A good understanding of this performance limiting parameter should enable us to enhance the efficiency of devices such as solar cells and photodiodes.

The $I-V$ characteristics (e.g., Figs. 1 and 2) at low and moderate voltages can be expressed as in Eq. (1) by two exponential functions (which includes series resistance R_S effect) and a third term due to shunt resistance R_{Sh}.

$$I=I_{01}\left[\exp\left(q\frac{V-R_SI}{n_1kT}\right)-1\right]+I_{02}\left[\exp\left(q\frac{V-R_SI}{n_2kT}\right)-1\right]+\frac{V-R_SI}{R_{\mathrm{Sh}}}. \tag{1}$$

Equation (1) above represents two parallel current transport mechanisms that occur in a *p-n* junction, namely, the diffusion current (I_1) that flows across the junction [first term in Eq. (1)] and the generation-recombination current (I_2) (second term). The effect of series resistance is incorporated by the use of the term R_SI and the role of the shunt resistance is effectively the leakage current term $(V-R_SI)/R_{\mathrm{Sh}}$. The terms n_1 and n_2 are the ideality factors. When the diode current is diffusion dominant in any voltage region, the ideality factor would equal 1 (corresponding to band–to–band recombination) and when recombination dominant to 2, the latter corresponds to a midgap state recombination.

I_{01}, the saturation current of the diffusion current term of Eq. (1), can be expressed, assuming low injection as Eq. (2)

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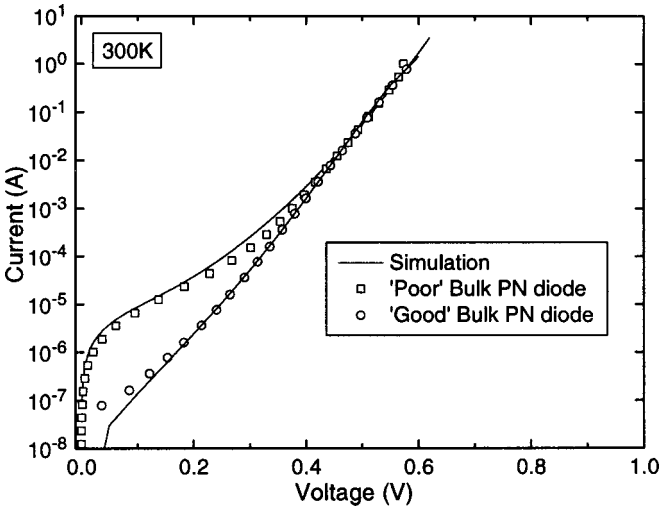


FIG. 1. Plot of the room temperature dark $I-V$ characteristics of a typical good and poor *pn* diode at room temperature. Note that the bulk *pn* diode characteristics at the high voltage end is identical, irrespective of the leakage due to handling and probing damage manifested at low voltages. Also shown are the theoretical curves for the poor and good *pn* diodes.

$$I_{01}=A\left[qn_i^2\frac{D_P}{N_D L_P}\frac{S_P\ \mathrm{Cosh}\frac{t}{L_P}+\frac{D_P}{L_P}\mathrm{Sinh}\frac{t}{L_P}}{\frac{D_P}{L_P}\mathrm{Cosh}\frac{t}{L_P}+S_P\ \mathrm{Sinh}\frac{t}{L_P}}\right.$$
$$\left.+qn_i^2\frac{D_n}{N_A L_n}\frac{S_n\ \mathrm{Cosh}\frac{x_j}{L_n}+\frac{D_n}{L_n}\mathrm{Sinh}\frac{x_j}{L_n}}{\frac{D_n}{L_n}\mathrm{Cosh}\frac{x_j}{L_n}+S_P\ \mathrm{Sinh}\frac{x_j}{L_n}}\right]. \qquad (2)$$

The first term of the square brackets on the right-hand side (RHS) of Eq. (2) is due to the holes injected into the active *n*-region and the second term due to electrons injected into the active *p*-region of a *p-n* junction in forward bias.

The saturation current I_{02} in Eq. (1) corresponds to the recombination-generation term. For ''good'' devices this recombination-generation contribution can be ignored, since

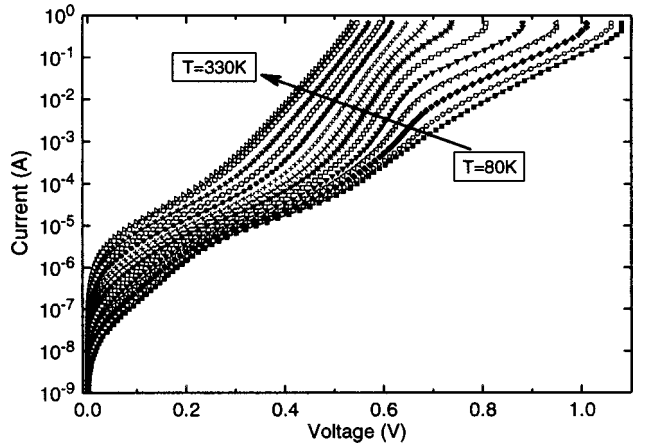


FIG. 2. Semilogarithmic plots of the dark $I-V$ characteristics of InGaAs mesa diodes at various temperatures from 80 to 330 K. The ''curling'' effect seen at high current is believed to be due to heating effects and this regime is ignored in this analysis.

TABLE I. The structure of ternary InGaAs and quaternary InGaAsP bulk devices.

Layer number	Material	Layer	Thickness (μm)	Doping level (cm^{-3})	Type
6	In(x)GaAs	Cap	0.3	1×10^{19}	P
5	InP	Window	0.1	2×10^{18}	P
4	InGaAsP	Intermediate	0.1	1×10^{18}	P
3	In(x)GaAs	Emitter	0.3	1×10^{19}	P
2	In(x)GaAs	Base	2.0	5×10^{17}	N
1	InP	Buffer	0.1	1×10^{18}	N

not only is it usually small but at the operating voltage (high biases) of TPV cells only the diffusion component is significant. However other mechanisms, e.g., Auger recombination, might be expected at the high operating voltage of these cells (close to open-circuit voltage). As the voltage is increased, a regime is reached when the above equations are not valid, i.e., the low injection condition, where the majority carrier density equals the thermal equilibrium values no longer holds and excess carriers dominate the electron and hole concentrations. That is to say that the injected carrier concentration exceeds the background doping concentration. The threshold voltage at which this high injection commences in a p^+n diode can be given by Eq. (3)

$$V_{\mathrm{th}}=2\frac{kT}{q}\ln\frac{N}{n_i}, \qquad (3)$$

where N is the ionized impurity concentration on the lower doped side of the *pn* diode and other symbols have their usual meaning. Our experimental $I-V-T$ curves show a change of slope at high biases/injection. The voltage at which this change in slope occurs is consistent with the voltage (V_{th}) given by Eq. (3) and with the aid of simulation software we demonstrate that this high injection substantially alters the minority carrier concentration profile in the base and emitter. This leads to the quasi-Fermi level (QFL) splitting and the associated electron ''pile-up'' at the window/emitter heterojunction. This chain of events will be shown to lead to the observed $n=2$ region, hereafter referred to as pseudo-$n=2$ region, at high bias conditions.

This concept of the splitting of the electron QFL at an abrupt heterojunction was proposed by Perlman and Feucht in 1964.[3] Lundstrom in 1984, suggested that the degree of splitting is given by the difference between the thermionic emission current across a heterojunction and the drift-diffusion current away from the junction.[4] More recently, many authors have used this concept in analytical models for heterojunction bipolar transistors and heterojunction bipolar photransistors.[5,6] Nelson *et al.* has employed this concept to explain the lower dark current measured in quantum well pin structures,[7] while Corkish and Honsberg have used PC1D solar cell simulation tool to demonstrate QFL variations at abrupt *p-n* heterojunctions in a range of doping levels.[8] In all these investigations the heterojunction consisted of a *p* and *n* doped layers. In our study of the InGaAs/InP TPV diodes (Table I) the QFL splitting will be shown to be at the p^+/p heterojunctions and due to the pile-up of charges as a result of the imbalance between the smaller thermionic current go-

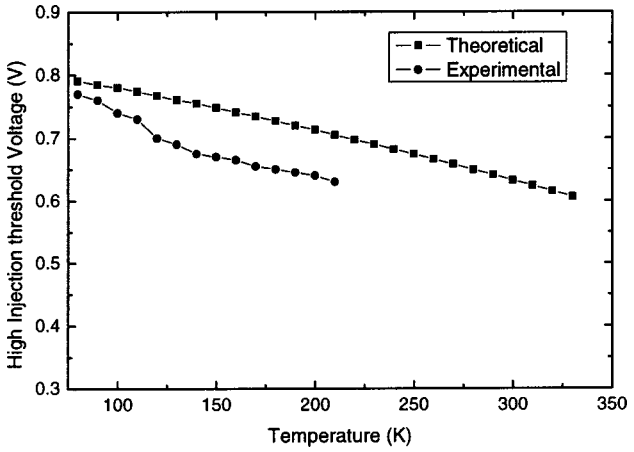


FIG. 3. Experimental and calculated threshold voltage for the onset of high injection in the 80–220 K range. Beyond 220 K, no experimental values are available as the maximum current sourcing was exceeded.

ing over the barrier and the larger incoming drift-diffusion current. The pile-up screens the applied voltage in forward bias leading to the observed and predicted $I-V$ characteristics. This hypothesis is justified by the analysis of the experimental data of devices with an intermediate energy band gap quaternary layer (InGaAsP).

Our approach to understand the experimental $I-V-T$ characteristics, in particular the pseudo-$n=2$ region, is to begin our work with a comparison of the theoretical value [from Eq. (3)] for the onset of high injection with that of the experimentally observed value (Fig. 3) and show that they are comparable. This is followed by a theoretical estimation of the injected carrier density as a function of bias (Fig. 4) for 300, 200, and 150 K using Eqs. (2) and (4). Figure 4 shows the transition from diffusion dominance to high injection. One can notice that the change over is as predicted in Fig. 3. We also show that this phenomenon sets in with hole injection to the lower doped *n*-base region (threshold voltage for electron injection is higher compared to hole injection at 150 K, in Fig. 4). This behavior, we postulate is not necessarily restricted to low temperatures but also prevails at room temperature. We confirm this and explain by inference the

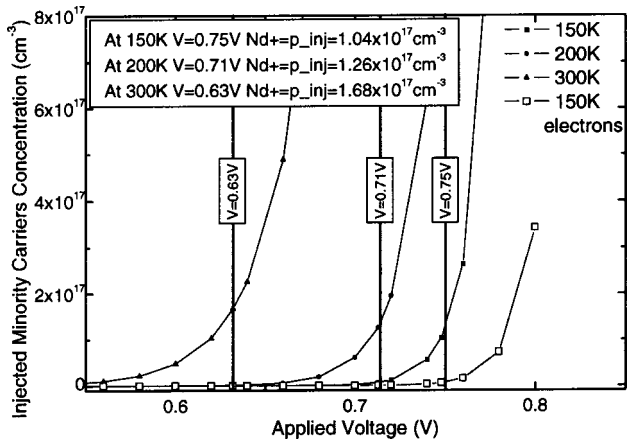


FIG. 4. Calculated injected hole minority carrier concentration as a function of voltage and temperature for 300, 200, and 150 K. Also shown in the injected electron carrier concentration for the 150 K temperature case.

observed data, with the use of band diagrams, charge concentration, and potential profiles obtained at room temperature using a simulation software. This is a valid approach to use, as the energy band diagram ($E_{V,C}$) is a plot of the band energies as a function of position and reflect both the heterostructure and also the electrostatic potential, $V(x)$, which in turn depends on the distribution of charge, $\rho(x)$. The latter, of course, depends on the current flow in the device, which is the experimental $I-V$ measurements we have carried out. Examination of these plots at the various interfaces/heterojunctions gives us a good insight to the behavior of the diode as manifested in the $I-V-T$ characteristics. We then show that the thermionic emission current at a given voltage and temperature is very much less than the diffusion current (at the heterojunctions) and that this imbalance leads to the splitting of the QFL. This in turn leads to the pile-up of electrons, and consequently the pseudo-$n=2$ and the "saturation" of the $I-V$ curve at high voltages. To further validate our theory, we measure the $I-V-T$ characteristics of diodes fabricated with an intermediate InGaAsP quaternary layer ($E_g=1$ eV) inserted between the window ($E_g=1.35$ eV) and the emitter ($E_g=0.72$ eV) where it lowers the barrier to electrons. In this case we show that the pseudo-$n=2$ region (change of slope) only appears at even higher voltages and lower temperatures, than in the case of the ternary latticed matched devices. This clearly demonstrates that the change of slope is due to the electron pile-up as a consequence of the large band offset between the InP window and the InGaAs emitter in the ternary devices. The absence of the $n=2$ region, beyond the $n=1$ region, for much of the temperature range studied in the structure with the quaternary layer is an important property for TPV applications. In this device with the quaternary layer, the ideality factor around the operating voltage is around 1 and consequently I_0 will be much lower than in the case of the ternary device where the operating voltage is in the pseudo-$n=2$ region, where I_0 is many orders of magnitude higher. This is an important feature for maximizing the open circuit voltage in TPV device operation.

II. DEVICE STRUCTURE, FABRICATION, AND EXPERIMENTAL SET-UP

The two structures (with and without the intermediate quaternary layer) studied are shown in Table I and were grown by metal-organic chemical-vapor deposition (MOCVD). These latticed matched structures are identical except that one of them has a *p*-type InGaAsP quaternary layer (layer 4 in Table I) inserted between the InP window and the InGaAs emitter.

Mesa devices of 1 mm diameter were fabricated using selective etchants. An annular *p*-metal (Ti–Pt–Au) contact was deposited onto the top InGaAs "cap" layer and the inner p^+-InGaAs material removed, exposing the *p*-InP window layer. A back metal contact (Au/Ge/Au/Ni/Au) was also deposited. Subsequently, a silicon nitride (SiN) passivation layer covering the mesa sidewalls (and the top metal) was deposited. The top metal contact area was then lithographically opened with the removal of the SiN from the annular ring.

Dark $I-V$ measurements were undertaken using a Keithley 2400 current-voltage source-meter, controlled by a computer. The samples were loaded onto a liquid nitrogen flow cryostat. A temperature controller regulates the temperature of the cryostat with a resolution of ± 0.1 K. All measurements were carried out using the four-wire technique to eliminate test fixture resistance effects. Series resistance is an important issue and could mask the true characteristics at high current densities. Great care needs to be taken to eliminate this effect. The simulations were carried out using a commercial software packages (PC1D and SILVACO).

III. RESULTS AND DISCUSSION

A. Dark current-voltage characteristics at room temperature of bulk InGaAs diodes

In Fig. 1 we present the room temperature dark current-voltage ($I-V$) characteristics of the ternary lattice matched device based on the structure given in Table I. The two experimental plots of the devices reflect typical diodes that were tested. The poor diode shows higher leakage current in the low voltage region. However, at high voltages the currents are identical. The higher leakage observed at the low voltages was found to arise mainly as a consequence of poor handling, probing, and dicing (sawing).[9] The other important characteristic to note is that there are distinct regions, corresponding to leakage, recombination, and diffusion currents. The recombination (nonradiative) region is characterized by an ideality factor (n) of 2 and the diffusion (radiative) region by $n=1$, as one would expect for nonradiative and radiative recombination, respectively.

To understand the transport properties at high currents, a necessary requirement for TPV operation, we measured the $I-V$ characteristics at high current/voltage and over a range of temperatures.

B. High injection *I–V* characteristics of ternary InGaAs mesa devices as a function of temperature

The dark current-voltage characteristics of the ternary bulk device, is shown in the semilogarithmic plots of Fig. 2. It is seen that they have a strong dependence on the bias voltage and temperature. The conventional regions of leakage, recombination, and diffusion are clearly evident at all temperatures. An additional region is seen in the bulk diode as the temperature is lowered (220–80 K). It is apparent from the low temperature curves that this region is beyond the $n=1$ region of the curve. The extracted ideality factor (n) of this additional region corresponds approximately to 2. It is not a recombination-generation process. The onset of the new $n=2$ region (beyond the $n=1$ region) is postulated to be due to high injection and charge pile-up.

Defining high injection as the instance when the injected carrier concentration is equal to the background concentration, we show that the experimental (from Fig. 2) and theoretical threshold voltages [derived from Eq. (3)] are in good agreement (Fig. 3). It is worth noting that high injection is a phenomenon that occurs when the applied voltage is such that the injected carriers exceeds the background ionized doping concentration and thus should not necessarily be confined to low temperatures as the results in Fig. 2 may suggest. The non-observance of high injection in our case at high temperature was due to reaching the maximum current sourcing capability of the current/voltage source used. Having correlated the experimental and the theoretical threshold voltages for the onset of high injection, we computed the injected minority carrier concentration as a function of applied voltage for three different temperatures using the first term on the RHS of Eq. (2). However, this requires prior knowledge of diffusion length and diffusion coefficient whose values are not universally established. More simply one could compute this with reasonable accuracy from Eq. (4). Figure 4 is a plot of injected carriers as function of bias using this equation

$$p_{\text{inj}}=\frac{n_i^2}{N_d^+}\exp\left(\frac{qV}{kT}\right). \tag{4}$$

The temperature dependence of n_i and N_d^+ has been taken into consideration in plotting the curves in Fig. 4. It is clear from the above plot that there is a transition region between the end of diffusion current dominance and the high injection dominance. For example, consider the 150 K temperature curve of Fig. 4, here the injected minority carrier concentration (holes) only equals the majority carrier concentration (electrons in the n-region) when the voltage is 0.75 V. However, it is clear from the plot that a substantial amount of minority carriers flow even at a voltage as low as 0.68 V (note that the experimental data for 150 K, shows a high injection threshold voltage of 0.67 V, Figs. 2 and 3). In Fig. 4, we also show for the 150 K case, that high electron injection only comes into consideration at even higher voltages, implying that the high carrier injection which gives rise to the pseudo-$n=2$ region seen in the $I-V$ characteristics at low temperatures in Fig. 1 is due to hole injection. So far, we have established the threshold voltage for the onset of high injection in a *pn* diode at different temperatures and showed that the experimental threshold voltage correlates well with that theoretical value. Further we have shown that this injection is due to minority carrier injection (holes) into the 5×10^{17} cm^{-3} doped N-base region.

In Fig. 2, we saw that with the onset of high injection, the current-voltage characteristic deviates from $n=1$ ideality factor to a ''pseudo''-$n=2$ value. To explore this, we simulated the energy band diagrams, quasi Fermi-level plots, electron and hole concentration plots, and potential diagrams of the *pn* structure in Table I. We used these simulated results to qualitatively illustrate our argument. Figure 5 shows the energy band diagram at three applied voltages: 0.65, 0.7, and 0.8 V at 300 K. Referring to the 0.65 V band diagram, one notices, as expected, the energy levels of the p-InGaAs cap layer and the p-InGaAs emitter layer are aligned (same material and dopant concentrations: Table I). However, as the bias is increased to 0.75 and 0.8 V these energy levels begin to separate, and this is clearly evident both for the (CB) and the valence band. This separation is reflected in the splitting of electron and hole QFL as shown in Fig. 6. We will return to the question of why this separation arises later in the text.

In Fig. 6, we note that the electron quasi-Fermi (EQFL) level is nearly constant throughout the junction for all four

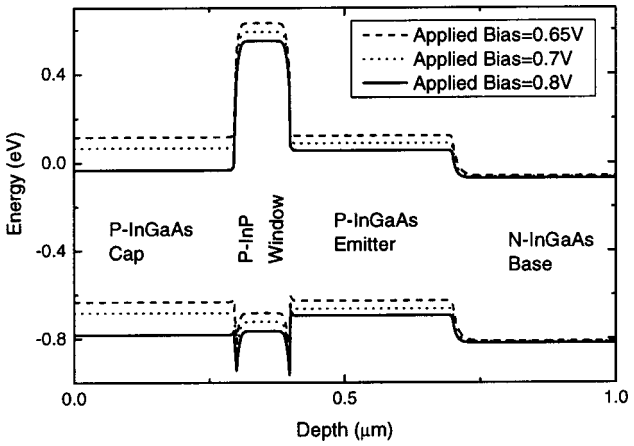


FIG. 5. Energy band diagram for InGaAs/InP PN structure (as given in Table I) under 0.65, 0.70, and 0.8 V forward bias. For better clarity, only the top 1 μm of the simulated band structure is shown.

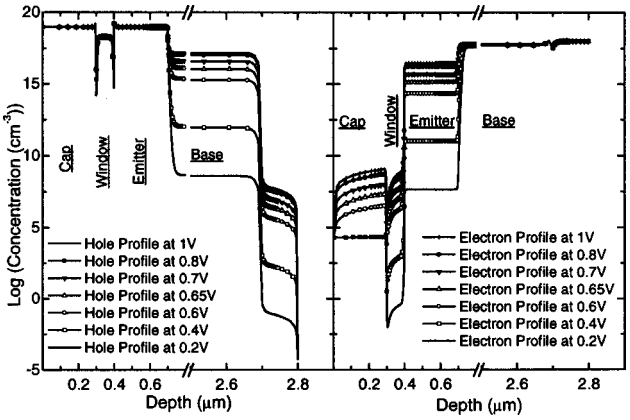


FIG. 7. Hole and electron concentrations vs depth as a function of bias voltage.

voltages presented except in the p-InP window/p-InGaAs cap layer where the QFL appears to move to more negative values with increasing forward bias. The hole quasi-Fermi-level (HQFL) is constant throughout the device from the cap layer to the base at 0.2 V bias. However, from 0.65 V onward the HQFL appears to increasingly split at the emitter/window and the window/cap interfaces. This suggests that the net carrier balance on either side of the said interfaces (p^+/p heterojunction) is different and increases with increasing voltage. It is also evident that the EQFL and HQFL are no longer superimposed within the cap layer for high voltages.

To confirm this, we looked at the concentration of electrons and holes throughout the device as the forward bias is increased. Figure 7 is a plot of the hole and electron concentrations. As one would expect the hole concentration is nearly constant and high in the p-InGaAs emitter layer irrespective of the bias. However, in the n-InGaAs base region, the concentration of holes minority carriers is increasing with forward bias. As the forward bias (0.2 to 0.6 V) is increased the minority hole concentration injected in the InGaAs base rises by about three orders of magnitude. Beyond 0.6 V this rise is increasingly less as seen in Fig. 7 and is seen to approach saturation at the very high voltages. Figure 7 also shows the electron concentration as a function of depth and applied voltage. It is clearly evident from this plot that the increase in electrons flowing into the p-InGaAs emitter region saturates at higher bias conditions as does the minority hole concentration flowing into the n-base region. One would expect the concentrations to increase with the forward bias, however, the hole and electron concentration saturation at higher voltages is not to be expected. To elucidate this we have analyzed the simulated potential diagram for the device. It is clearly evident from the potential diagram of Fig. 8 that when the bias is ranging from 0 to 0.6 V the voltage is fully applied across the junction. Indeed, the cap and the emitter layer potentials are at the same level. That is to say that any additional bias is entirely dropped across the junction. However, at 0.65 V and more clearly at 0.8 V, the cap and emitter potentials are no longer the same. This indicates that the incremental voltage is no longer fully dropped across the emitter/base junction. It is for this reason that the current beyond a certain applied voltage, defined and shown to correspond to the onset of high injection appears to deviate from the $n=1$ ideality factor and approaches a pseudoideality factor of $n=2$. This appears on the $I-V$ curve as a change in the slope.

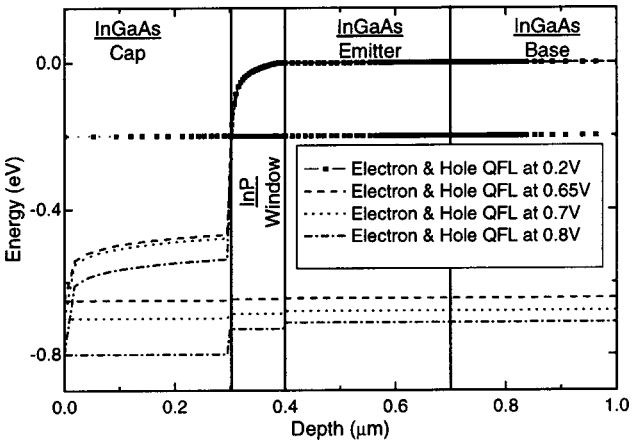


FIG. 6. Electron and hole QFL as a function of voltage. As the voltage increases the hole QFL is seen to split, i.e., not constant.

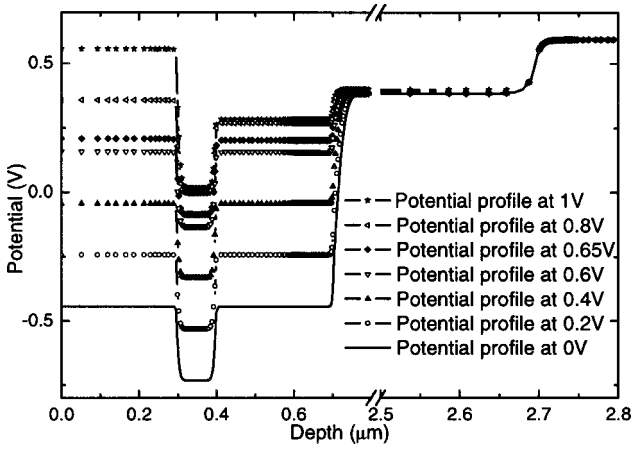


FIG. 8. Potential vs depth for the bulk InGaAs/InP structure at 300 K.

With the use of the simulation software, we have shown that the onset of the high injection at a temperature of 300 K, is as we have predicted earlier (sets in around 0.63 V). We have also shown that the change in the slope of the $I-V$ curve after high injection sets in, is due to the applied potential being not fully dropped at the junction. Finally, to explain the reason for the voltage not being dropped fully across the junction we invoke the concept of the splitting of the QFL. As can be seen from Table I, the structure is such that adjoining the p-InGaAs layer is the p-InP window layer, this heterojunction results in a large CB offset (Fig. 5) which prevents the free electrons from flowing through the emitter and then to the cap layer. The window layer being rather thick, it is not possible to have carriers tunneling across this barrier. The only route is by thermionic emission over the InP barrier. The thermionic current over such a heterojunction can be given by the following expression:[10]

$$I_{\text{th}} = AT^2 \exp - \left[\frac{\Delta E_C - (n-1)\delta_1 - \delta_2 + qV}{nkT} \right] \times \left[1 - \exp\left(- \frac{qV}{kT} \right) \right], \tag{5}$$

where ΔE_C is the CB offset and δ_1 and δ_2 are the QFL splits in the respective regions. The two terms represent the forward and reverse currents over the junction (barrier). For our structure at 300 K, and an applied voltage of 0.7 V, $\delta_1 = 0.48$ eV, $\delta_2 = 0$ and $n = 1.55$ (the above equation is very sensitive to the value of "n"), the thermionic current is ~ 1.6 A, while the diffusion current is calculated to be 126 A. Thus, we note that the thermionic emission current at a given voltage and temperature is very much less than the diffusion current flowing into the p-InGaAs emitter. It is this imbalance that leads to the splitting of the QFL. As a consequence of this imbalance, there is an accumulation of electrons at the window/emitter interface (on the emitter side). Consequently, this screens the junction from seeing the full extent of the applied voltage. In other words one could think of this as a sheet of negative charge which needs to be compensated by a sheet of positive charge, the latter coming from the applied positive forward bias at the cap layer. This results in the effect seen in the $I-V$ curve, i.e., the change of slope at high biases (and as we have shown experimentally, at low temperatures too).

With the aid of energy, potential, QFL and concentration diagrams, and Eqs. (2) and (5), we have demonstrated that the deviation from the $n=1$ regime to a pseudo-$n=2$ regime is due to the splitting of the QFL, resulting from an accumulation of charge at the hetero p^+/p interface. Moreover, we have shown that this accumulation is "compensated" by an increasing proportion of the applied forward bias, thereby leaving only a fraction of the applied voltage to be dropped across the active junction, thus inducing a "saturation" of the forward current at high voltages. To further support our argument, we show that the activation energy obtained from the $I-V-T$ at a high voltage (high injection regime) is totally consistent with the barrier that the electrons experience at the window/emitter heterointerface. Incidentally the holes see no barrier even though a splitting of the QFL exists.

TABLE II. Extracted n (fitted) and E_a values for three regions of interest and a range of temperatures

Voltage/field range	Ideality factor (n)	Activation energy (E_{ac}) (eV)
Low field (0.15–0.32 V)	1.99 (80–110 K)	0.165
	2.01 (120–170 K)	0.165
	2.06 (180–230 K)	0.19
	1.97 (230–270 K)	0.21
	1.95 (270–330 K)	0.23
Medium field (0.50–0.60 V)	1.05 (180–230 K)	0.75
	1.01 (230–270 K)	0.8
	1.01 (270–330 K)	0.84
High field (0.68 V)	2.02 (80–210 K)	0.44

C. Ideality factor (n) and activation energy (E_{ac})

From the Arrhenius plots of $\ln(I)$ versus $1/T$, we have extracted values for E_{ac} for the low, medium, and high field regions. Table II below shows the extracted values.

Considering, the two main regions of interest, we note that for the midfield range (0.5–0.6 V), the ideality factor (n) is equal to 1, corresponding to a diffusion current contribution. As with the low field case, the midfield ideality factor (n) is practically independent of temperature (see Table II) and the midfield activation energy of 750–840 meV, is in reasonable agreement with the band gap of $In_{0.53}Ga_{0.47}As$ which is around 0.72–0.76 eV. This establishes that process is diffusion (band–to–band recombination) dominant. At the high field (0.68 V), the low temperature ideality factor is equal to 2 (note this is a "pseudo"-n value) and the extracted activation energy is equal to 0.44 eV. This is in good agreement with the energy difference 0.5 eV between the p-InGaAs emitter CB and the p-InP CB observed in Fig. 5. The inference is that at high voltages/current we are in fact seeing the effect of the InP/InGaAs heterointerface as we hypothesised earlier.

To conclusively prove that this is in fact the case, we carried out $I-V-T$ measurements on diodes with a InGaAsP quaternary layer ($E_g = 1$ eV) inserted between the InP window and the InGaAs emitter layers. If our hypothesis is true, we expect the quaternary layer to assist with the forward current transport and as such not to observe the pseudo-$n=2$ region, until the devices were subjected to a much higher voltage and/or a lower temperature. Figure 9 is a plot of the $I-V-T$ characteristics of a typical diode with the InGaAsP quaternary layer. The inset in Fig. 9 presents for clarity a comparison between the latticed matched InGaAs $I-V$ curve at 180 K and the $I-V$ curve of the InGaAs with the InGaAsP quaternary layer, at the same temperature. It is obvious that the latter shows only the $n=1$ component, the pseudo-$n=2$ component is not present until much lower temperatures (120 K). This clearly demonstrates that the insertion of the quaternary layer has aided the forward current transport and no accumulation occurs until much lower temperatures and higher voltages. This, we believe conclusively proves that the pseudo-$n=2$ region is due to carrier accumulation, as a consequence of the carriers having to overcome the energy

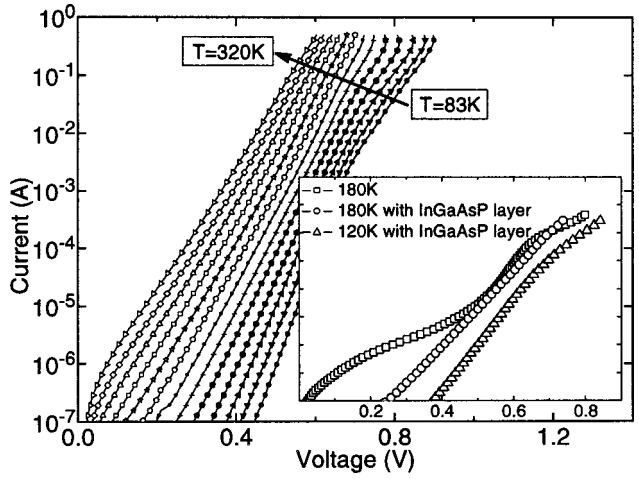


FIG. 9. A plot of current vs voltage in the temperature range 83 to 320 K for a 1 mm diameter mesa device with a quaternary InGaAsP layer inserted between the InP window and the InGaAs emitter, serving as a barrier reducing layer for electron transport in the forward direction. It is clearly evident that for much of the temperature range with the exception of very low temperatures, the pseudo-$n=2$ region is not present, no accumulation occurs for much of the temperature range. The inset clearly shows the onset of the pseudo-$n=2$ at lower temperature for the device with the InGaAsP layer as compared to the device without (the scale for the inset is the same as for the main plot).

barrier at the window/emitter heterointerface, and the associated high injection.

IV. CONCLUSION

We have studied the current-voltage characteristics of the latticed matched InGaAs diodes as a function of temperature. They have exhibited the expected regions, corresponding to leakage, recombination, and diffusion currents. Moreover, at low temperatures an additional region is observed at high fields. We have shown that the onset of this region commences with high injection into the lower doped base region. The high injection was shown with the aid of simulation tools to substantially alter the minority carrier concentration profile in the base, emitter, and consequently the QFL at the base/window and the window/cap heterojunctions. We have also shown that the high voltage activation energy coincides with the InP barrier at the p^+/p heterointerface leading to an electron accumulation at the window/emitter hetrojunction. The latter manifests as a pseudo-$n=2$ region of the current-voltage curve. We have confirmed this by investigating the $I-V-T$ characteristics of diodes with an InGaAsP quaternary layer ($E_g=1$ eV) inserted between the InP window ($E_g=1.35$ eV) and the InGaAs emitter ($E_g=0.72$ eV) where it aids the injected electrons to flow into the cap layer and thus to the external circuit, thereby reducing the accumulation at the window/emitter interface. However, at very high biases and very low temperatures (with much reduction of the thermionic emission current) this accumulation begins to surface even in devices with the quaternary InGaAsP layer. This unambiguously confirms the role of the accumulation being the reason for the change in the slope of the $I-V$ characteristics from $n=1$ to $n=2$ in the ternary latticed matched device at moderate temperatures and at very low temperatures in the case of the InGaAsP devices. This we believe is an important feature in designing device structures for TPV applications where we need a low dark current to maximize both the open circuit voltage and short circuit current.

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