Stress Modelling Of Multi Level Interconnect Schemes For Future Deep Submicron Device Generations

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Abstract

Copper and low dielctric constantant (k) materials are poised to become the dominant interconnect scheme for integrated circuits for the future because of the low resistance and capacitance that they offer which can improve circuit performance by more than 30 % over conventional interconnect schemes. This paper addresses the thermomechanical stresses in the Cu/Low k interconnect scheme through numerical simulation and identifies the locations of maximum stress in the structure with view to providing information on the impact that different dielectric materials have on the stress distribution in the interfaces between metals and dielectric layers.

1 Introduction

Copper is poised to take over as the main on-chip conductor in Ultra Large Scale Integrated circuit (ULSI) fabrication. Compared to aluminium, which was used exclusively up to this point as interconnect material, copper has a lower resistance. This is critically important in high-performance microprocessors and fast static RAMs, since it enables signals to move faster by reducing the RC time delay. Furthermore, the capacitance of the interconnect dielectric also can be reduced using low dielectric constant materials (low-k) for the Inter Metal Dielectric, and this also results in a reduction in the crosstalk between tracks as well as introducing a beneficial reduction of dielectric thickness requirement as a side effect.
Copper and low-k dielectrics represent a completely new material set for IC manufacturers. There is an absence of knowledge and experience of this material set and for this reason there is an understandable level of concern over the impact that it's introduction in an advanced technology could have. Furthermore, with the increase of device packing density and the decrease of device dimensions, mechanical stress has become an critical reliability issue which needs to be addressed as early as possible in the development of the copper low-k schemes.

1.1 Interconnect structure

In this work, copper and low-k multi level metal interconnect schemes considering different low-k dielectrics (SiLK and Aerogel), encapsulations for copper (tantalum, titanium, titanium nitride and silicon nitride) as well as different process geometries (barrier thickness and Aspect Ratio variations) have been studied. Finite Element Modelling simulations and associated materials characterisation has been used in order to evaluate the potential impact on device reliability due to thermomechanical stress. In these structures, stress levels which could easily lead to potential delamination or stress migration problems, have been identified and localised using two and three dimensional simulation techniques.

	Young's modulus (GPa)	TCE (10^{-6}/°C)	Poissons Ratio
Silicon	**130.2**	**3.0**	**0.28**
Copper	**129.8**	**17.0**	**0.343**
Ti	**116**	**8.6**	**0.32**
TiN	**600**	**9.4**	**0.25**
Ta	**186**	**6.3**	**0.34**
Si_3N_4	**150**	**1.0**	**0.25**
Aerogel	**0.005**	**3**	**0.2**
SiLK	**2**	**66**	**0.34**

Table .1. Mechanical properties of chosen materials

1.2 Experimental Details

A set of material properties were established from literature[1,2]and numerical 2D simulations were performed using the general purpose finite element package ANSYS[3-4]. A set of typical single damascene[5,6]. structures were implemented (see Fig. 1 and 2) combining copper as interconnect layer with encapsulation of titanium, titanium nitride and tantalum as metal barriers with thicknesses from 0.04 to 0.1μm, and silicon nitride as the dielectric barrier and thickness of 0.1μm. This encapsulation is surrounded by low-k (SiLK) or ultra-low-k (Aerogel) dielectrics, laying on top of a silicon substrate which is extended below the area of interest.
Figure 3 presents an example of stress results in the Y direction from simulations of a typical single damascene copper interconnect layer with 1:4 Aspect Ratio. In all the simulations the stress in the copper layer at room temperature tends to be tensile ($\sigma>0$) while all barriers, specially at corners, tend to be in compression ($\sigma<0$). This means that the higher levels of stress will be at the interface where the copper film and encapsulating barriers are in contact as well as in corners or where two different barriers are present at the same interface with copper. Delaminations at these interfaces have been observed to reduce the overall lifetime of the Cu interconnect to significantly less (~x2) than the x10 improvement expected over Al based

interconnect schemes,[6,7]. In general the stress levels achieved in the whole copper layer can be summarised in Table 2, where typical stress ranges are given.

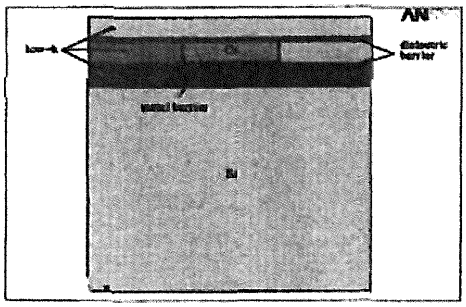

Figure 1. Representation of a typical 'Single Damascene' 2-D simulation

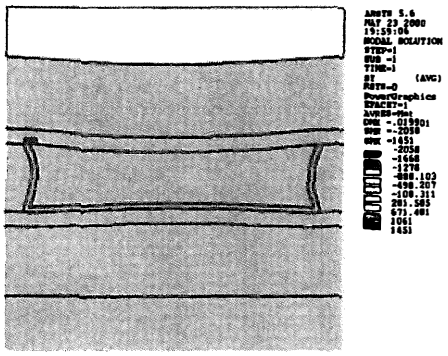

Figure 2 Stress in the Y direction for a copper layer of..1:4Aspect VIA , encapsulated by 40 nm of Ti andl 00 nm Si_3N_4 barriers using Aerogel as the intermetal dielectric

Encapsulation			σ_x (MPa)	σ_y (MPa)
Ti	Si_3N_4	SiLK	**(140,480)**	**(-88,260)**
TiN			**(172,614)**	**(176,495)**
Ta			**(125,533)**	**(72,317)**
Ti		Aerogel	**(-234,200)**	**(-108,281)**
TiN			**(-334,414)**	**(-159,796)**
Ta			**(-46,151)**	**(-171,400)**

Table 2. Stress range distribution at the copper layer for different encapsulations.

2 Conclusions

From this work, it is clear that the most reliable scheme would be the one made of copper, titanium or tantalum with SiLK. The use of titanium nitride leads to higher levels of tensile stress in the copper layer, because it is by far the most rigid material. Higher levels of stress in any structure multiply this effect where the structure presents special features (at interfaces, corners, etc.). In all schemes, the layer at the interface with barrier is in tension ($\sigma>0$) all along the centre of the layer and it is in compression ($\sigma<0$) at its corners (where the effect of barriers become dominant). So, in the Cu/TiN interface, the copper layer is experiencing differences in stress in the order of Giga Pascals over a few microns, while for the Cu/Ta interface this is

reduced to a few hundreds of Mega Pascals, almost one order of magnitude smaller. This can be seen to be a more relaxed scheme and has been identified as a more reliable structure. Stress levels in copper are always close to its ultimate tensile stress (221 MPa),. Therefore this situation may lead to a delamination occurring at the interfaces between the Cu and the barrier Also it can be shown that in general, and in both x and y directions, the use of Aerogel instead of SiLK as the intermetal dielectric has an effect on the stress distribution of copper, where part of the film, well beyond the interface, is also in compression. This can be explained by the intrinsic softness of Aerogel as a material, and because it is very fragile this leads to a general reduction in the stability of the scheme.

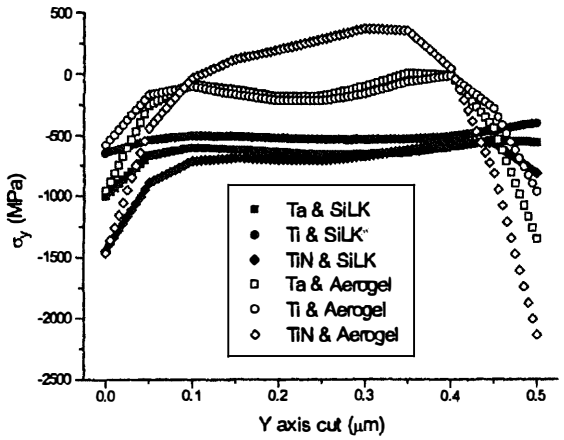

Figure 3 Stress distribution at the Y direction in 1:4 Aspect Ratio copper film at the interface with the metal barriers (Ta, Ti and TiN) for both intermetal dielectric (SiLK and Aerogel).

3 References

[1] C.G.M.DeOca M.Eng.Sc Thesis, National University of Ireand–Cork (NUIC) (2000)

[2] W.E.BeadleJ.C.C.Tsai, R.D.Plumber. Quick Reference Manual For Silicon Integrated Circuit Technology, John Wiley&SOns New York 1985

[3] Swanson Analysis Systems, Inc. P.O.Box 65, Johnston Road Houston,PA 15324 – 0065 Ansys Users Manual.

[4] ANSYS Inc 2001 Inc. P.O.Box 65, Johnston Road Houston,PA 15342 – 1300 Ansys Workbook July 1996.

[5]E.M.Zielinsky,S.W.Russell,,R.S.List,A.M.Wilson,C.Jin,K.J.Newton,J.P.Lu,W.Y.Hsu,V.C ordasco. Proc. IEEE Hong Kong Electron Devices Meeting 1997 pp 936-938

[6] A. I. Sauter, , PhD Thesis, Leand Stanford Junior University, USA. Feb. 1991

[7] S.Foley PhD Thesis NUIC . Irl 2000