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Charged Defect Quantification in $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ MOS Capacitors

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Abstract

This work focuses on the separation and quantification of fixed bulk oxide charge, fixed charge at the dielectric-semiconductor interface and interface state charge components in the $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$ metal oxide semiconductor system. The availability of atomic layer deposited Al_2O_3 dielectrics over *n* and *p* type $In_{0.53}Ga_{0.47}As$ with a range of thickness values opens up an experimental route for the determination of the interface state density (D_{it}) independently of the total fixed oxide charge using capacitance voltage measurements taken at 1MHz and -50^{o}C. Low temperature forming gas annealing significantly reduces the amount of fixed charge. The interface fixed charge at the interface is reduced from ~ $–8.5x10^{12}cm^{-2}$ pre anneal to ~ $-7.4x10^{11}$ cm^{-2} post anneal; the

bulk oxide charge is reduced from ~1.4x10^{19} cm^{-3} pre anneal to ~5x10^{18} cm^{-3} post anneal. The forming gas anneal also has a significant effect on the interface state charge, reducing its density from 1.3x10^{13}cm^{-2} pre anneal to 4x10^{12}cm^{-2} post anneal.

Introduction

Investigations of high-κ films deposited on high mobility substrates for higher performance or lower power applications are now routinely reported in the literature [1-5]. However, one major outstanding issue with these systems is the quantification of fixed charge at the dielectric-semiconductor interface, fixed charge in the bulk of the oxide and interface states [6]. There has also been much discussion of the validity of analysis of the interface state density of these high mobility semiconductor systems using techniques such as the conductance method [7], the high-low technique [8], the Berglund method [9] and the Terman method [10].

We have already reported on the nature of the fixed charge components in the atomic layer deposited (ALD)-Al_2O_3/*n* $In_{0.53}Ga_{0.47}As$ system [6]. The objective of this work is to extend on the results reported in [6] for MOS structures on *n* type $In_{0.53}Ga_{0.47}As$ to a study of the capacitance-voltage (CV) response of ALD-Al_2O_3/$In_{0.53}Ga_{0.47}As$/InP structures using both *p* and *n* doped $In_{0.53}Ga_{0.47}As$ epitaxial layers, where an analysis of the CV response of the *p* and *n* doped $In_{0.53}Ga_{0.47}As$ MOS structures provides an experimental route to separate the fixed charge and interface state components. The interface state density (D_{it}) is determined independently of the total fixed oxide charge,

building on previous experimental work using an alternative technique to the aforementioned, conventional methods.

Experimental

The samples used in this study were *n* and *p* type InP substrates with 2µm $In_{0.53}Ga_{0.47}As$ layers grown by Metal Organic Vapour Phase Epitaxy (MOVPE). The *n* type $In_{0.53}Ga_{0.47}As$ (S doped to ~$3.8x10^{17}cm^{-3}$) was grown on an 0.3µm InP buffer layer (S-doped $1.9\times10^{18}cm^{-3}$) on an InP (S doped ~3 to $8\times10^{18}cm^{-3}$) wafer. The *p* type $In_{0.53}Ga_{0.47}As$ (Zn doped to ~$4\times10^{17}cm^{-3}$) was grown on a 0.1µm InP buffer layer (Zn doped $1.5\times10^{18}cm^{-3}$), on an InP (Zn doped ~4 to $6\times10^{18}cm^{-3}$) wafer. Due to air exposure, all samples have an initial native oxide on the $In_{0.53}Ga_{0.47}As$ surface. The Al_2O_3 dielectric was deposited by atomic layer deposition at 270°C, using TMA ($Al_2(CH_3)_6$) and H_2O, the first pulse being that of the aluminum precursor. Al_2O_3 films with nominal thicknesses of 2, 5, 8, 11 and 15nm were deposited. No pre-gate-metal deposition annealing was carried out. Circular MOS capacitor formation was completed by e-beam deposition of 75nm of Pt through a shadow mask. The capacitors had diameters of 100, 150, 200 and 250µm. Forming gas annealing was carried out in an open tube furnace. In all cases the forming gas anneal consists of a continuous flow at 1 liter per minute of 5% H_2/95% N_2 ambient at atmospheric pressure at 350°C for 30 minutes. The samples were loaded into the furnace on a quartz boat once the required temperature was stable. When the annealing was complete, samples were removed immediately from the furnace and transferred off the quartz boat.

Results and Discussion

Figure 1 shows the high resolution transmission electron microscopy (HR-TEM) and high angle annular dark field scanning TEM (HAADF-STEM) images of the sample with a nominal 5nm thickness of atomic layer deposited Al_2O_3 on the untreated $In_{0.53}Ga_{0.47}As$ (100) surface. Following dielectric deposition, the HR-TEM images reveal variability in the interface region Al_2O_3 and the $In_{0.53}Ga_{0.47}As$ surface, when examining multiple images recorded on a given sample. Some regions, as shown in Figure 1 (b), do not have any interfacial oxide layer between the Al_2O_3 and the $In_{0.53}Ga_{0.47}As$ surface. This is in agreement with previous reports of the "self cleaning" phenomenon of the TMA precursor whereby some native oxides at the III-V surface are removed during the first cycles of the Al_2O_3 atomic layer deposition process [11-13]. However, other areas examined by HR-TEM, shown in Figure 1 (c) indicate the presence of an interface oxide with a variable thickness from (0-1nm). The results indicate variability in the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface properties, with a discontinuous interface oxide layer, consistent with previous reports on similar $Al_2O_3/In_{0.53}Ga_{0.47}As$ samples that detected a InO_x layer of non-constant thickness at the interface [14].

Table I tabulates the measured oxide thicknesses and the implied deposition amount per ALD cycle as determined by HR-TEM analysis. The average deposition rate (oxide thickness per number of ALD cycles) is calculated to be approximately 0.09nm per cycle. Using this deposition rate and the number of ALD cycles, the thickness of the dielectric film with nominal 15nm of Al_2O_3 is estimated to be ~20nm. The same thicknesses for

the samples with *p* type substrates are assumed, having been in the same ALD deposition runs.

It is expected that the total charge (Q_{tot}) in the high-κ/ $In_{0.53}Ga_{0.47}As$ system is composed of fixed oxide charge (Q_{fixed}) and the interface state contribution (Q_{it}), where the interface state charge density [C/cm^2] will depend on the position of the Fermi level at the Al_2O_3/ $In_{0.53}Ga_{0.47}As$ interface, the density of the interface states across the semiconductor band gap and on the nature of the interface defects (i.e. donor or acceptor). The fixed oxide charge can consist of a sheet charge contribution, which is typically located near the interface, $Q_{int,}$ expressed in units [C/cm^2], and/or a bulk oxide charge, Q_{bulk}, in units [C/cm^3] distributed throughout the Al_2O_3 layer.

The magnitude of the contribution of Q_{it} relative to Q_{tot} will depend on the surface potential, the doping type in the $In_{0.53}Ga_{0.47}As$ and the nature of the interface defects. For $In_{0.53}Ga_{0.47}As$ with a doping concentration of $4x10^{17}$ cm^{-3}, as studied in this work, the Fermi level (E_f) at flat band is close to the band edges, with E_c-E_f = 0.04eV and E_f-E_v = 0.04eV for the *n* and *p* doped $In_{0.53}Ga_{0.47}As$ respectively. Consequently, at the *flat band condition* (V_{fb}) in a high-κ/$In_{0.53}Ga_{0.47}As$ MOS structures, the interface states are primarily unoccupied for a *p* type substrate and primarily occupied for the *n* type substrate. If we consider the defects to be donor type, then the defects are neutral (full) for an *n* type substrate, but for a *p* type substrate the defects have a net associated positive charge (empty). If the interface defects are acceptor in nature, then at V_{fb} for an *n* type substrate the defects have a net associated negative charge (full) but for a *p* type substrate

the defects are neutral (empty). As a consequence, regardless of the nature of the interface defects, the magnitude of the *difference* in the V_{fb} and the subsequently calculated Q_{tot} for *n* and *p* type $In_{0.53}Ga_{0.47}As$ MOS systems at the flat band condition yields the interface state density (in units [cm^{-2}]). If both donor and acceptor like defects exist within the energy gap, then the V_{fb} difference will reflect the net interface charge associated with the donor and acceptor defects integrated across the energy gap.

In order to demonstrate the calculation the defect is assumed to be donor type, which is in agreement with recent work based on conductance analysis for similar systems [15, 16]. Then for a capacitor with an *n* type substrate with accumulation capacitance C_{ox} and corresponding metal semiconductor workfunction W_{msN}, V_{fb} is given by

$$V_{fbN} = W_{msN} - \frac{Q_{fixed}}{C_{ox}} \tag{1}$$

with the corresponding Q_{tot}:

$$Q_{tot} \approx Q_{fixed} = Q_{bulk}t_{ox} + Q_{int} \tag{2}$$

as the assumed donor type interface states are primarily uncharged, there will be no significant contribution from the interface state charge component (qD_{it}). C_{ox} is determined from

$$C_{ox} = \frac{\varepsilon_0 \kappa}{t_{ox}} \tag{3}$$

where ε_0 is the relative permittivity, t_{ox} is the physical thickness of the oxide and κ is the dielectric constant of the Al_2O_3 (8) as determined from the gradient of the capacitance equivalent thickness versus physical thickness for the *n* type samples.

For a capacitor with a *p* type substrate and corresponding metal semiconductor workfunction W_{msP}, V_{fb} is given by:

$$V_{fbP} = W_{msP} - \frac{Q_{fixed}}{C_{ox}} - \frac{qD_{it}}{C_{ox}} \qquad (4)$$

with the corresponding Q_{tot}:

$$Q_{tot} = Q_{fixed} + Q_{it} = Q_{bulk}t_{ox} + Q_{int} + qD_{it} \qquad (5)$$

whereby, at flatband voltage, the assumed donor type defect states are positively charged. Subtraction of Equations 1 and 4 or Equations 2 and 5, the difference of Q_{tot} for the *n* and *p* type samples, is related directly to the interface state density.

$$V_{fbN} - V_{fbP} = W_{msN} - \frac{Q_{fixed}}{C_{ox}} - W_{msP} + \frac{Q_{fixed}}{C_{ox}} + \frac{qD_{it}}{C_{ox}} = 0.668 + \frac{qD_{it}}{C_{ox}} \qquad (6)$$

$$Q_{totP} - Q_{totN} = Q_{bulk}t_{ox} + Q_{int} + qD_{it} - Q_{bulk}t_{ox} - Q_{int} + qD_{it} = qD_{it} \qquad (7)$$

with 0.668V representing the difference in the work function for *p* and *n* $In_{0.53}Ga_{0.14}As$ doped to a similar level ($4x10^{17}cm^{-3}$).

Thus the difference in the V_{fb} and Q_{tot} values for *n* and *p* doped $In_{0.53}Ga_{0.47}As$ can be used to separate the components of the fixed charge and the interface states. Once qD_{it} is known, Q_{fixed} can be evaluated from either the V_{fbN} or V_{fbP} values, or the gradient of Q_{tot} with respect to t_{ox}.

In order to minimize the interface defect capacitance contributions to the measured capacitance, the CV measurements were recorded at -50°C and 1 MHz. As predicted by the model proposed by Brammertz *et al*. [17], under these measurement conditions most of the interface traps will not be able to respond to the ac signal, so the interface trap

contribution to the capacitance can be neglected (for a capture cross section of $1x10^{17}$ cm^2, defects from E_v+0.075eV to E_c-0.675eV will act as fixed charge). Under these conditions, the interface states change occupancy in response to the slowly varying dc bias on the gate, and manifest themselves as a fixed charge component on the capacitance voltage profile and only affect the CV through a stretch-out of the capacitance along the gate voltage axis. The total amount of charge in the system can thus be investigated by comparing the theoretical V_{fb} and the actual V_{fb} at 1MHz, -50°C.

Figure 2 thus illustrates the capacitance versus voltage characteristics as a function of dielectric thickness at 1MHz measured at -50°C for (a) *n* type and (b) *p* type $In_{0.53}Ga_{0.47}As$, normalized to the maximum capacitance. There is a negative shift in the CV profiles as a function of increasing dielectric thickness consistent with a net positive fixed charge in the MOS system. Considering our previous results reported in [18], the nature of this bulk oxide fixed charge could be dependent on the dielectric itself. For example, in the case of the HfO_2 films in [18], the capacitance voltage characteristics shifted in a positive direction as a function of increasing oxide thickness, indicating a net negative charge in the oxide. It is also possible that the dielectric deposition technique could be influencing the nature of the bulk oxide charge, however an investigation of such effects is outside the scope of this paper.

Figure 3 shows the V_{fb} values and the corresponding total positive charge in the system for both *n* and *p* type $In_{0.53}Ga_{0.47}As$ and how they change as a function of dielectric thickness for the samples with Al_2O_3 thicknesses values 11.5nm, 14nm and 20nm. The

thicker Al_2O_3 films (11.5nm, 14mn and 20nm) were selected as they maximize the V_{fb} shift for a given level of oxide charge due to their lower gate oxide capacitance. The calculation of the total charge in Figure 3(b) inherently assumes all the charge is located at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. The oxide charge calculation is based on a Pt work function of 5.4eV [19].

A number of important conclusions can be drawn from Figures 3 (a) and (b):

- It is clear that the total amount of charge in the system increases with increasing oxide thickness, indicating that positive charge is distributed throughout the bulk of the Al_2O_3 film.
- The difference between the total charge in the system for *n* and *p* type $In_{0.53}Ga_{0.47}As$ reflects the net interface charge associated with the donor and/or acceptor defects integrated across the energy gap.
- The interface state density component appears to be constant within experimental limitations, and corresponds to an areal density of interface defects of $1.3x10^{13}cm^{-2}$.

The fixed oxide charge component can be quantified by considering the total charge in Figure 3(b). For the *n* type $In_{0.53}Ga_{0.47}As$ MOS samples, the data in Figure 3(b) corresponds to Equation 2 where the charged interface state component is negligible, allowing the presence of any near-interface fixed charge component to be highlighted. Equation 2 takes the form y=mx+c, where m is Q_{bulk} in units of $[C/cm^3]$ and Q_{int} is the y axis intercept where the physical thickness t_{ox} =0. Using a linear fit of the total charge

data in Figure 3(b), for the *n* type $In_{0.53}Ga_{0.47}As$ samples, the bulk and interface charge densities can be estimated. The subsequently determined estimates of the fixed charge components in the MOS capacitors are given in Table II.

The magnitude of the fixed charge components can also be estimated using the following parabolic representation of the V_{fb} versus dielectric physical thickness t_{ox}:

$$V_{fb} = W_{ms} - \frac{qQ_{\text{int}}}{C_{ox}} - qC_T \int_0^{t_{ox}} \frac{x}{d_{ox}} Q_{bulk}(x)dx = W_{ms} - \frac{qQ_{\text{int}}t_{ox}}{\varepsilon_o \varepsilon_{ox}} - \frac{qQ_{bulk}t_{ox}^2}{2\varepsilon_o \varepsilon_{ox}} \quad (7)$$

where C_T is the measured capacitance in accumulation. By fitting the above quadratic equation, the amount of fixed interface and bulk oxide charge can be estimated, using a standard polynomial fit, as shown in Figure 4. The flatband voltage is measured at 1MHz, -50°C. As the defects are assumed to be donor in nature, in the case of the *p* type samples, at V_{fb}, the total charge also contains the charged D_{it} component. As a consequence, for the determination of the Q_{fixed} term, the *n* $In_{0.53}Ga_{0.47}As$ samples are used at the flat band condition, where the charged interface state component is negligible at 1MHz, -50°C, and the flat band voltage shift is dominated by the presence of any bulk and interface fixed charge components. The values obtained are also shown in Table II.

The determined interface fixed charge component is negative, with a positive bulk oxide charge. This is in agreement with our recent study on the nature of the fixed charge in the Al_2O_3/*n* $In_{0.53}Ga_{0.47}As$ system [6]. As described in [6], first principles calculations and x-ray photoelectron spectroscopy results suggest that the bulk positive fixed charge

can be attributed to aluminum dangling bonds and the negative fixed charge at the oxide-semiconductor interface to oxygen dangling bonds in the Al_2O_3 layer.

In terms of the flatband voltages of the capacitors on *p* type $In_{0.53}Ga_{0.47}As$, the assumed donor interface defect levels are positively charged. Therefore, it is possible that, in the case of the *p* $In_{0.53}Ga_{0.47}As$, there is also negative fixed charge near the interface, but its contribution to V_{fb} is dominated by the positively charged donor type interface traps and the positive fixed charge distributed through the Al_2O_3 layer.

Figure 5 shows the capacitance voltage measurements for the thickness series following forming gas annealing at 350^{o}C for 30 minutes. The leakage current density for the sample with 2.4nm Al_2O_3 on *n* type $In_{0.53}Ga_{0.47}As$ after the FGA was too high for a reliable CV curve to be obtained for the rather large capacitor areas investigated. Following the FGA, significant passivation of the charge components occurs, with the CVs overlaying close to the ideal flat band voltage (V_{fb}) of ~0.2V (using a Pt work function of 5.4eV [19]) for all thicknesses, as shown in Figure 5(a) and (b). It is important to note however, that following the anneal, the thickness series on *p* type $In_{0.53}Ga_{0.47}As$ are still shifted more negative than the equivalent *n* type samples, consistent with the presence of some residual charged interface defects which are not fully passivated by the FGA process. This is also illustrated in Figure 6, where the V_{fb} versus oxide thickness and the corresponding total charge are plotted both pre and post FGA. The clear dependence of the total charge on the Al_2O_3 thickness for the as-deposited samples is removed after the FGA, indicating a reduction in the bulk oxide

positive charge component (Q_{bulk}) as a result of the FGA. It is also evident from Figure 6, that a difference between the total charge for the *p* and *n* $In_{0.53}Ga_{0.47}As$ MOS structures remains, indicating that the interface states are not fully passivated by the FGA process.

The samples prior to the FGA exhibited a significant variation of V_{fb} and total charge (Q_{tot}) with the Al_2O_3 thickness (t_{ox}), which allowed the bulk oxide charge (Q_{bulk}) and the fixed interface charge (Q_{int}) to be determined from the slope and the intercept of Q_{tot} versus t_{ox}, respectively. From Figure 6(b) it is evident that this approach cannot be utilized post FGA, as a linear variation of Q_{tot} versus t_{ox} is not measured. The density of the bulk charge components is estimated using the polynomial fitting of the V_{fb} versus oxide thickness following the anneal, shown in Figure 7. The resulting fixed and bulk oxide charges are shown in Table II. The polynomial fit indicates a reduction in both fixed charge components in the ALD-Al_2O_3 after the FGA process, with values of -$7.4x10^{11}cm^{-2}$ and $5x10^{18}cm^{-3}$ for the negative fixed interface charge and the bulk positive charge respectively. While significantly reduced after the FGA, the presence of Q_{bulk} is still evident through the reduction of V_{fb} for gate stacks with t_{ox}> 14nm. Table III summarizes the nature and density of the charge components in the Pt/ALD $Al_2O_3/In_{0.53}Ga_{0.47}As$/InP MOS capacitors with no anneal and following the forming gas anneal

Conclusion

Separation and quantification of the fixed bulk oxide charges and interface states in the Pt/Al_2O_3/$In_{0.53}Ga_{0.47}As$/InP MOS capacitors is reported, using an ALD-grown dielectric thickness series on *n* and *p* type untreated $In_{0.53}Ga_{0.47}As$ (100). The total interface state density (D_{it}) is determined independently of the total fixed oxide charge based on the evaluation of the flat band voltage V_{fb} at -50ºC and 1 MHz. The net integrated interface state density across the energy gap at the Al_2O_3/$In_{0.53}Ga_{0.47}As$ is ~$1.3x10^{13}cm^{-2}$ before forming gas annealing. Negative interface fixed charge exists near the Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface, with positive charge distributed through the bulk of the Al_2O_3. Low temperature forming gas annealing (350ºC, 30 minutes, 5% H_2/95% N_2) significantly reduces the amount of fixed charge in the system. The fixed charge at the interface is reduced from ~ $–8.5x10^{12}cm^{-2}$ pre anneal to ~ $-7.4x10^{11}$ cm^{-2} post anneal; the bulk oxide charge is reduced from ~$1.4x10^{19}$ cm^{-3} pre anneal to ~$5x10^{18}$ cm^{-3} post anneal. The forming gas anneal also significantly reduces the charged interface trap density, from $1.3x10^{13}cm^{-2}$ to $4x10^{12}cm^{-2}$; however, it does not eliminate all the defects at the high-κ/$In_{0.53}Ga_{0.47}As$ interface.

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Substrate	Nominal Thickness (nm)	No. of Cycles	Measured by HR-TEM (nm)	Deposition Rate (nm/cycle)
P	2	30	2.4	0.08
N	5	70	5.6	0.08
N	8	120	11.5	0.10
N	11	165	14.0	0.08

Table I

Method	Interface Fixed Charge cm^{-2}	Bulk Fixed Charge cm^{-3}
Pre FGA		
From V_{fb}	$-1x10^{13}$	$2x10^{19}$
From Q_{tot}	$-7x10^{12}$	$8x10^{18}$
Post FGA		
From V_{fb}	$-7.4x10^{11}$	$5x10^{18}$

Table II

Charge Component	Magnitude Pre Anneal	Magnitude Post Anneal	Comment
D_{it} [cm^{-2}]	$1.3\ x10^{13}$	$4\ x10^{12}$	Assumed Donor type
Q_{int}/q [cm^{-2}]	$-7x10^{12}$ to $-1x10^{13}$	$-\ 7.4x10^{11}$	Negative fixed charge assumed located near Al_2O_3/ $In_{0.53}Ga_{0.47}As$ interface
Q_{bulk}/q [cm^{-3}]	$8x10^{18}$ to $2x10^{19}$	$5x10^{18}$	Positive charge distributed throughout the Al_2O_3 film

Table III

Table I: Al_2O_3 thickness as measured by HR-TEM analysis. Using these measurements, the extracted deposition rate of 0.09nm allows an estimated thickness of 20nm for the nominal 15nm sample

Table II: Estimation of the bulk and interface fixed charge densities determined from the thickness series on *n* type $In_{0.53}Ga_{0.47}As$ /InP substrates pre and post the forming gas anneal

Table III: Summary of the charge components in the Pt/ALD $Al_2O_3/In_{0.53}Ga_{0.47}As$ system pre and post FGA anneal

Figure 1: (a) HR-TEM and (b), (c) HAADF-STEM image of the sample with 6nm (nominal 5nm) of Al_2O_3 on untreated $In_{0.53}Ga_{0.47}As$ surface. (b) and (c) highlight the inconsistent interlayer at different regions of the same sample.

Figure 2: Normalized capacitance voltage characteristics measured at 1MHz, -50°C for each thickness of Al_2O_3 on (a) *n* type and (b) *p* type $In_{0.53}Ga_{0.47}As$. The shaded region signifies the ideal V_{fb} using a Pt work function range of 5 to 5.6eV

Figure 3: (a) V_{fb} shift and (b) Total Charge in the $Al_2O_3/In_{0.53}Ga_{0.47}As$ system as a function of dielectric thickness clearly indicating the presence of bulk oxide charge.

Figure 4: V_{fb} vs physical thickness for *n* type $In_{0.53}Ga_{0.47}As$ MOS structures. The polynomial fitting allows an estimation of the interface fixed oxide charge components. V_{fb} was estimated at 1MHz and -50°C.

Figure 5: Normalized capacitance voltage characteristics measured at 1MHz, -50°C for each thickness of Al_2O_3 on (a) *n* type and (b) *p* type $In_{0.53}Ga_{0.47}As$ following forming gas anneal. The grey highlighted region is the expected range of V_{fb} based on a platinum workfunction in the range 5eV to 5.6eV.

Figure 6: (a) V_{fb} and (b) Total Charge in the $Al_2O_3/In_{0.53}Ga_{0.47}As$ system as a function of dielectric physical thickness with no anneal and with forming gas anneal at 350°C for 30 minutes.

Figure 7: V_{fb} vs physical thickness for *n* type $In_{0.53}Ga_{0.47}As$ with untreated surfaces after the forming gas anneal.

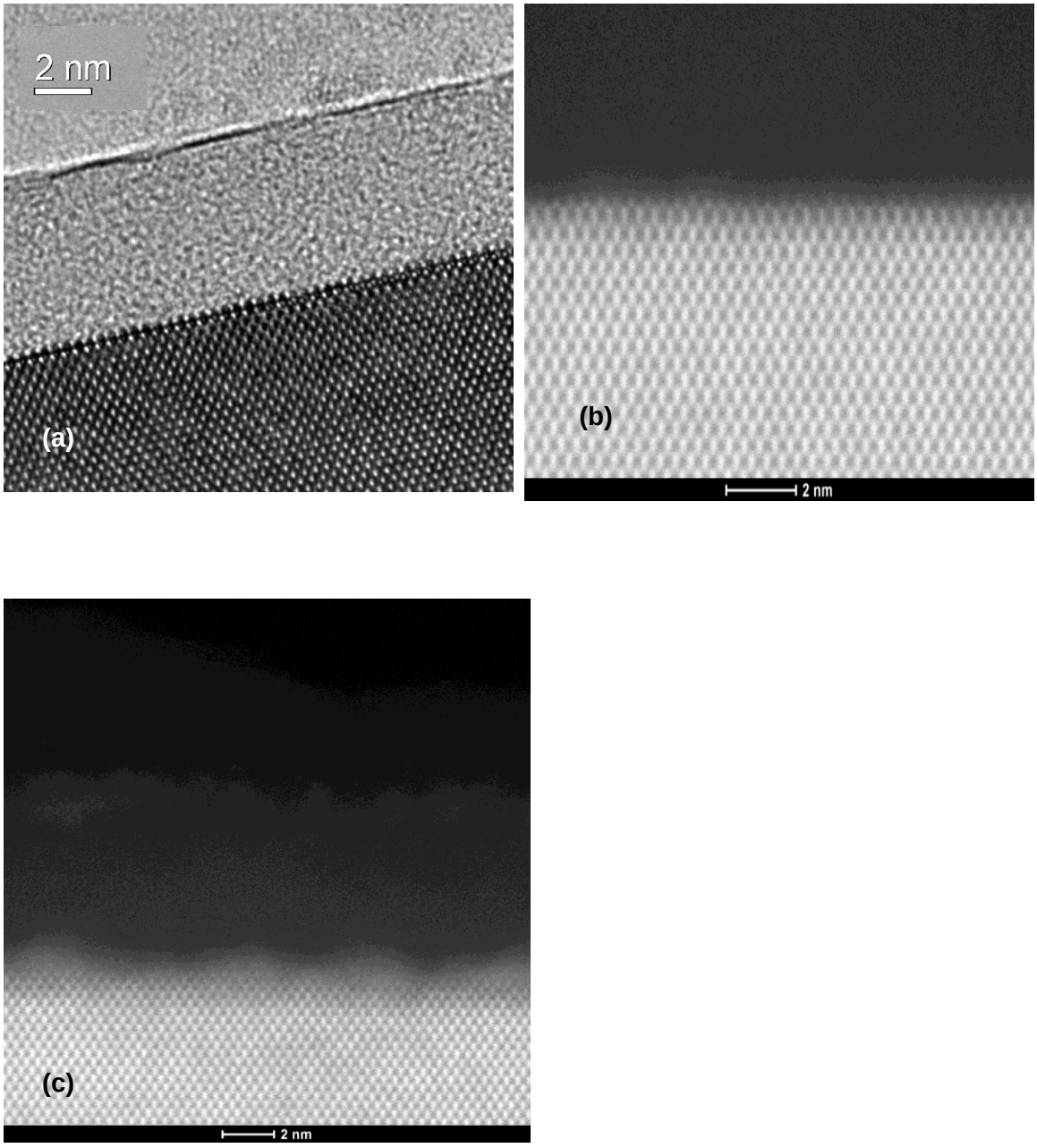


Figure 1

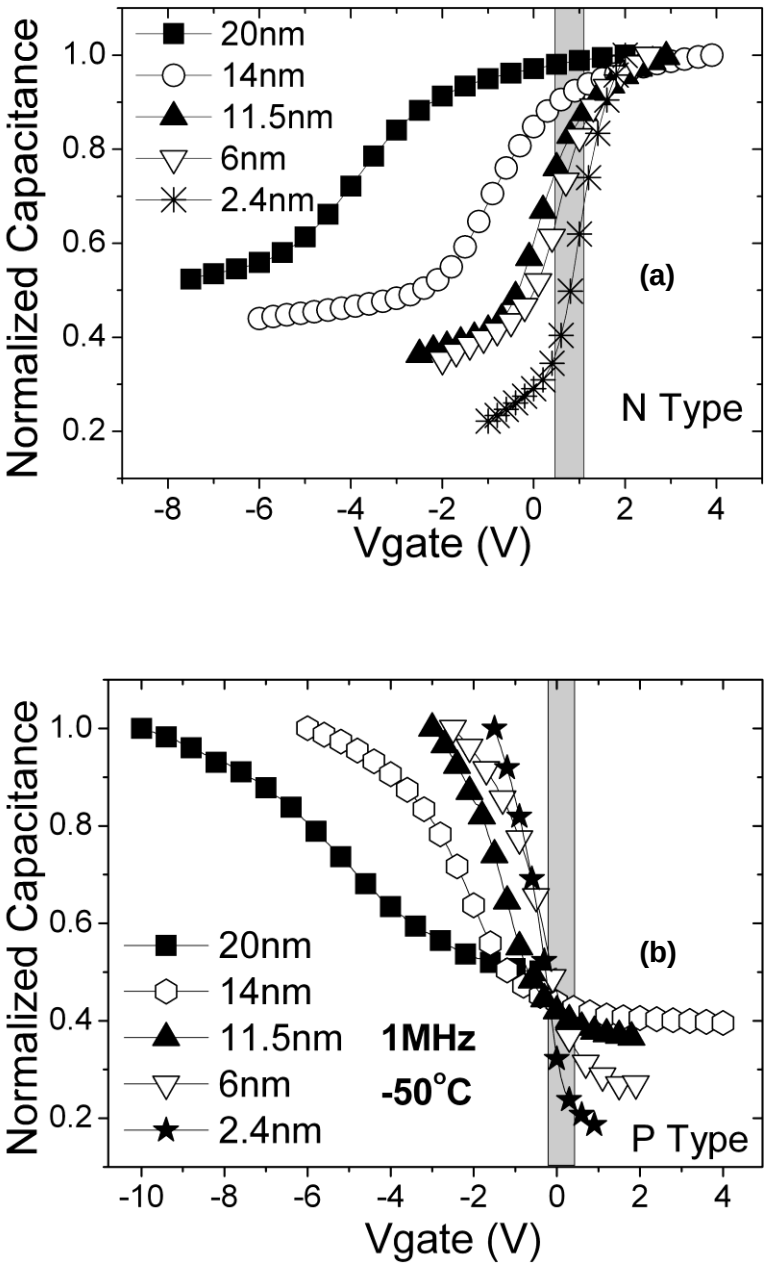
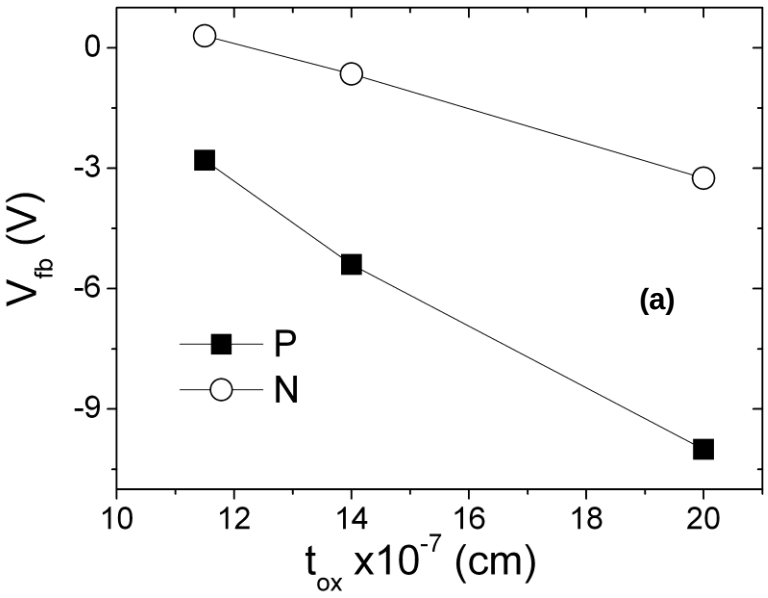

Normalized Capacitance
Vgate (V)
20nm
14nm
11.5nm
6nm
2.4nm
(a)
N Type
(b)
1MHz
-50°C
P Type

Figure 2


0
-3
-6
-9
V_{fb} (V)
(a)
P
N
10
12
14
16
18
20
t_{ox} x10^{-7} (cm)

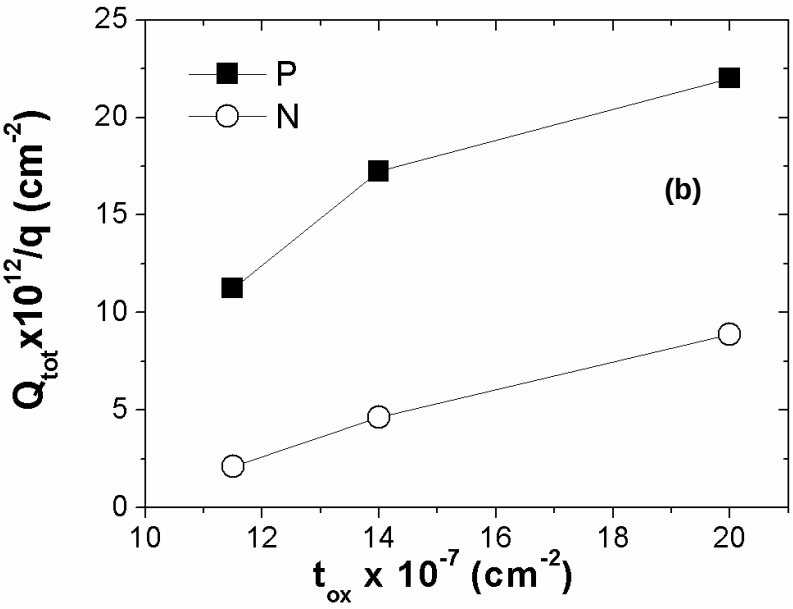

25
20
15
10
5
0
Q_{tot}x10^{12}/q (cm^{-2})
P
N
(b)
10
12
14
16
18
20
t_{ox} x 10^{-7} (cm^{-2})

Figure 3

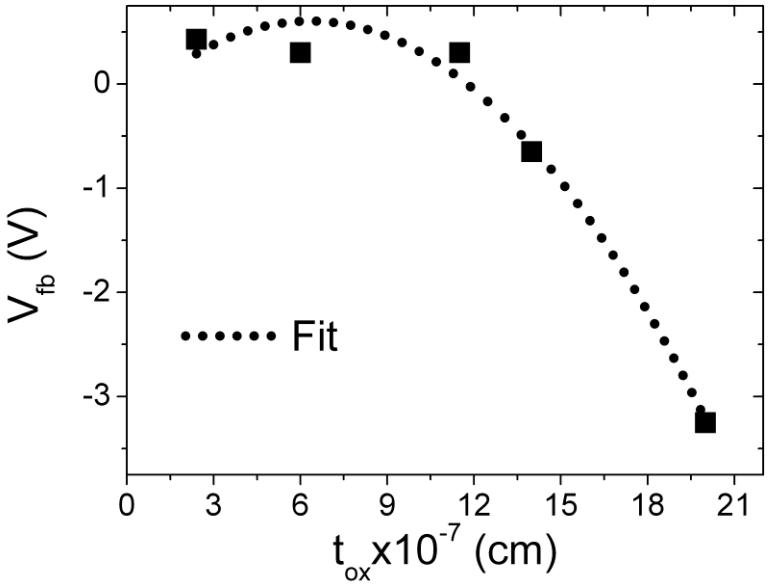


Figure 4

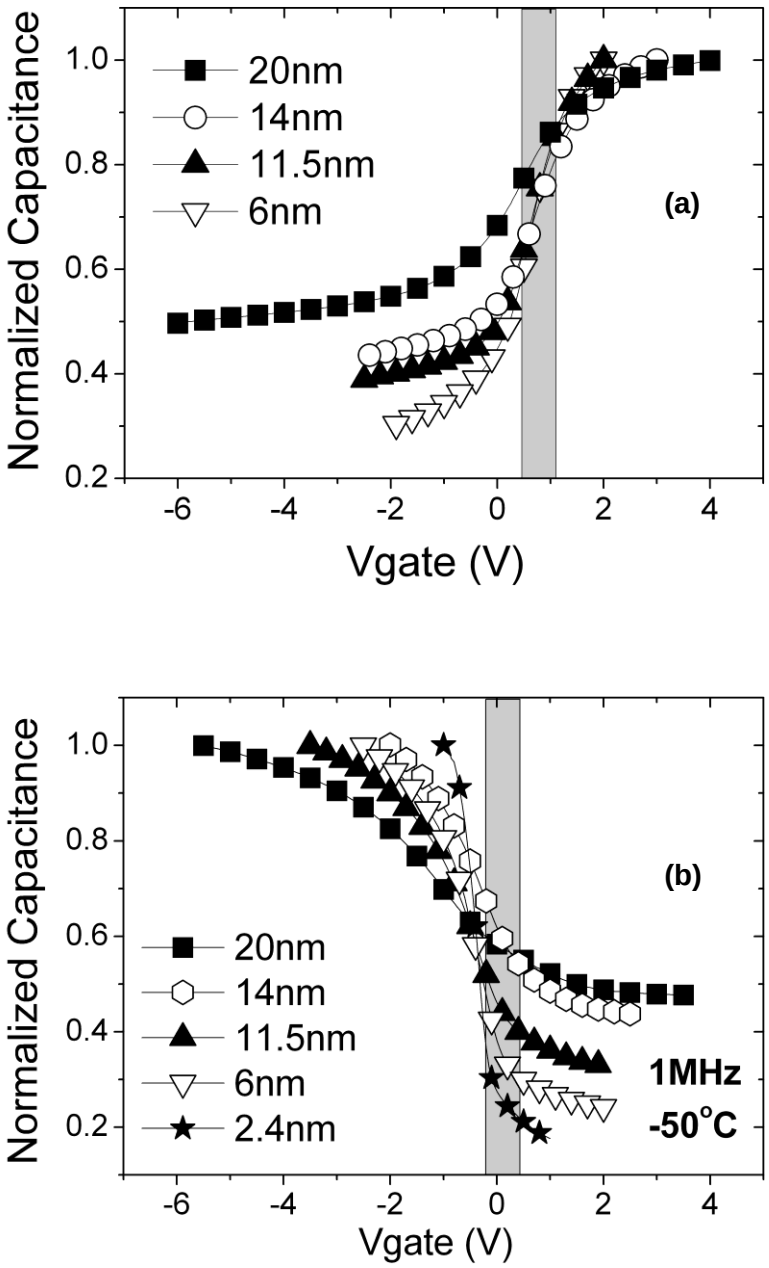

Normalized Capacitance
1.0
0.8
0.6
0.4
0.2
-6
-4
-2
0
2
4
Vgate (V)
20nm
14nm
11.5nm
6nm
(a)
Normalized Capacitance
1.0
0.8
0.6
0.4
0.2
-6
-4
-2
0
2
4
Vgate (V)
20nm
14nm
11.5nm
6nm
2.4nm
(b)
1MHz
-50°C

Figure 5

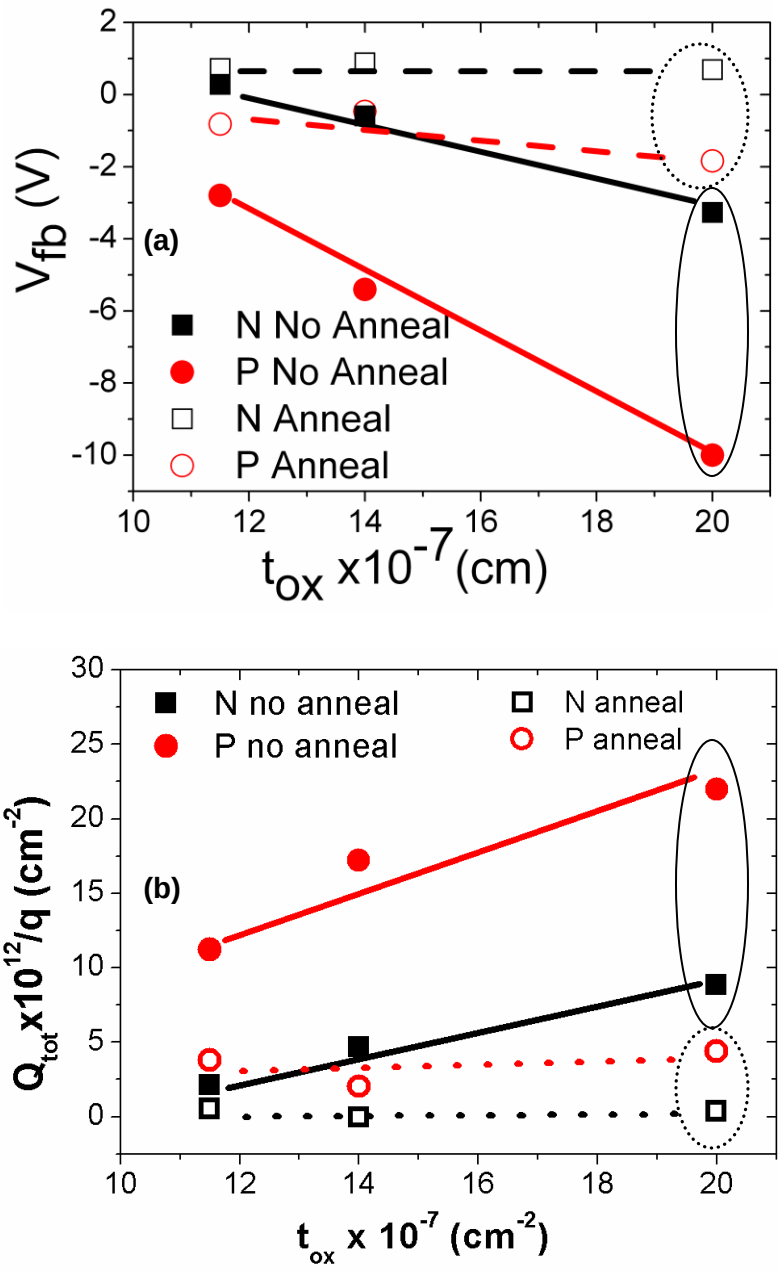

(a)
N No Anneal
P No Anneal
N Anneal
P Anneal
V_{fb} (V)
t_{ox} x10^{-7}(cm)
(b)
N no anneal
P no anneal
N anneal
P anneal
Q_{tot}x10^{12}/q (cm^{-2})
t_{ox} x 10^{-7} (cm^{-2})

Figure 6

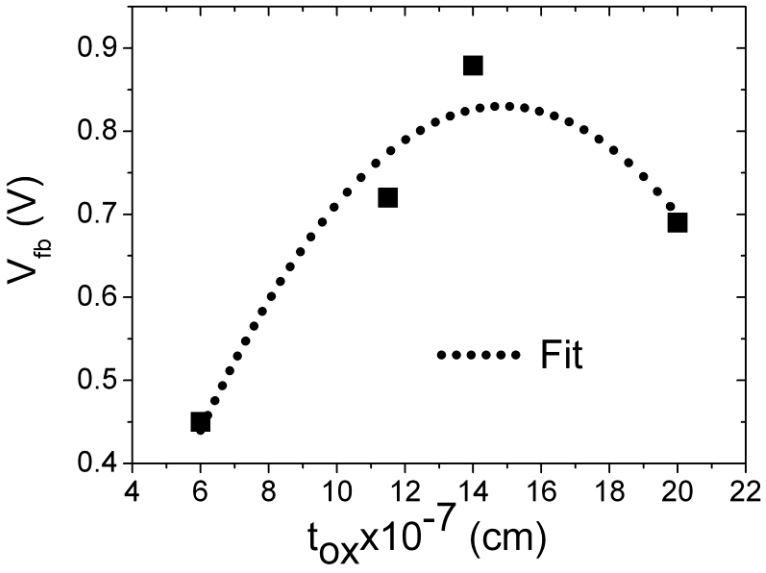


Figure 7