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Design Principles for Maximizing Photovoltage in Metal-Oxide-Protected Water-Splitting Photoanodes

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Abstract

Metal oxide protection layers for photoanodes may enable the development of large-scale solar fuel and solar chemical synthesis, but the poor photovoltages often reported to date will severely limit their performance. Here we report a novel observation of photovoltage loss associated with a charge extraction barrier imposed by the protection layer, and by eliminating it, achieve photovoltages as high as 630 mV, the maximum reported to date for water-splitting silicon photoanodes. The loss mechanism is systematically probed in MIS Schottky junction cells compared to buried junction p^+n cells, revealing the need to maintain a characteristic hole density at the semiconductor/insulator interface. A leaky capacitor model related to dielectric properties of the protective oxide explains this loss, achieving excellent agreement with the data. From these findings, we extract design principles for simultaneous optimization of built-in field, interface quality, and charge extraction to maximize the photovoltage of insulator-protected water splitting devices.

Introduction

Splitting water into hydrogen and oxygen is a key component of clean fuel and chemical synthesis

from solar energy. Water splitting using a photoelectrochemical junction was first demonstrated by Fujishima and Honda in 1972, and has since progressed significantly[1-7]. Metal-insulator-semiconductor (MIS) technology, a key materials driver of the information age[8], and the even simpler semiconductor-liquid junction are promising candidates for these applications, but the best materials have suffered from a lack of simultaneous efficiency and stability. In 2011, Chen et al. first used ultrathin (1-2 nm) ALD-TiO_2 to protect silicon anodes where conduction was limited by carrier tunnelling[9]. In 2013, Scheuermann et al. studied amorphous, as-deposited ALD-TiO_2 films up to 12 nm in thickness, finding bulk-limited conduction with a modest Ohmic loss, ~21 mV/nm of extra oxide, for p^+Si anodes oxidizing water in the dark[10]. A hole conduction model was proposed involving tunnelling through the ultrathin SiO_2 and hopping via traps in the TiO_2. More recently, Hu et al.[11] fabricated ALD-TiO_2 protected devices with similar conditions to those employed previously[9-10] coated with a nickel catalyst. They investigated thicker TiO_2, including films > 100 nm, and observed a photocurrent onset voltage during water oxidation that was essentially TiO_2 thickness-independent[11]. If the conduction mechanism is the same, as was proposed by Hu, the hole conductivity must be at least 4 orders of magnitude higher than in reference 10. The same group has also recently used ~ 1 nm ALD-TiO_2 to protect CdTe[12] and $BiVO_4$[13].

Despite enhanced TiO_2 conductivity, the silicon photovoltages achieved in those works[11-13] are ~400 mV or less, far below the theoretical maximum for silicon photovoltaics of 700-800 mV[14], the 740 mV record achieved with HIT (heterojunction with intrinsic layer) cells[15], or the highest MIS-water oxidation photovoltage of 550 mV[9]. Silicon is considered to be nearly ideal for the bottom-cell of a tandem device combined with a large band-gap (~1.8 eV) top cell[16]. However,

the silicon must provide >600 mV of photovoltage to be viable. Even with a perfect fill factor, the silicon photovoltages reported to date using highly-conductive TiO_2[11] fall far short. Additionally, it remains unclear if the reported influence of nickel coatings is generally applicable to ensuring high hole conductivity in TiO_2[11].

There is a need, therefore, to understand fundamental aspects of leaky protection layers as they pertain both to photovoltage and conductivity for the ultimate optimization of cell efficiency. Herein, we show why relatively insulating (capacitive), as distinct from highly conductive, oxide protection layers promote higher photovoltages, and present what we believe is the first report on insulator protection-layer thickness scaling on photovoltage. Based on the use of a buried p^+n silicon structure we demonstrate that the insulator thickness dependence of the photovoltage is removed and accomplish the highest photovoltage for a water oxidation silicon photoanode reported to date ~630 mV making the TiO_2 protected silicon cell viable for a tandem device. Finally, we show how these observations suggest general design principles for maximizing photovoltage in any insulator-protected architecture.

Results

Photovoltage loss in ALD-TiO_2 protected nSi MIS photoanodes

Three junction-types have been examined to date for water-splitting photoanodes: a) semiconductor-liquid junctions (SL, herein referred to as Type 0) requiring a stable semiconducting metal-oxide in contact with water; b) Schottky junctions either with a direct metal contact to the semiconductor[17-18] or with an interposed protective metal-oxide layer forming a metal-insulator-semiconductor (MIS or Type 1) structure[9-11]; and c) buried pn junctions (Type 2),

which likewise may[11] or may not[19] incorporate additional protective oxides. The fabrication complexity increases, in general, from Type 0 to 1 to 2 and as this report details, the extraction barrier induced by protection layers can be made to decrease accordingly for each type for the same insulator layers.

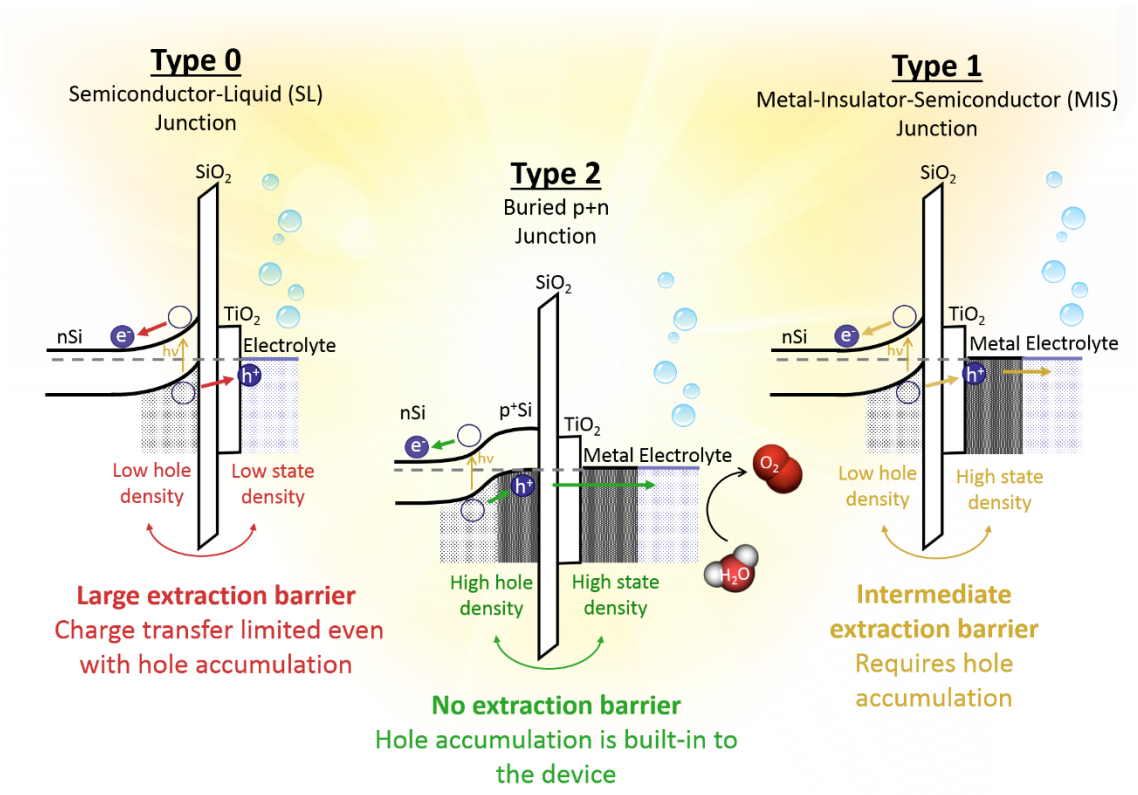


Figure 1 | Three junction types showing the extraction barrier imposed by the protection layer illustrated with silicon water-oxidation photoanodes. Three types of photoanode junctions have been employed in the literature, the Type 0 Semiconductor-Liquid (SL), Type I MIS Schottky, and Type II MIS p^+n junction. Here, each junction configuration is shown for a silicon cell protected by TiO_2. The insulators introduce a series resistance, which when located inside the junction constitutes an extraction barrier. Therefore, the density of holes at the interface and the density of states of the contact play a key role. In Type 0 cells, holes will be accumulated at the semiconductor/insulator interface during current flow, and charge transfer may still be

significantly limited due to a low density of states in the contact. Such a situation may arise from using electrolytes as well as non-metallic catalysts as the hole conduction mediator. In Type 1 cells, moderate hole accumulation is sufficient to efficiently extract minority carriers, but the photovoltage suffers a linear loss to accumulate those holes. In Type 2 cells, the p^+ region ensures a high hole concentration at the interface that is independent of illumination and bias resulting in no barrier to hole extraction. As a result, these cells exhibit no dependence of inferred photovoltage on the insulator thickness and accomplish record photovoltages at all oxide thicknesses and pH values studied.

Beginning in the 1970's, Green and coworkers discussed the utility of an inversion layer in so-called Conductor-Insulator-Semiconductor (CIS) solar cells (similar to the MIS structures discussed here) where an ultrathin insulator provides ideal passivation while being thin enough to allow unimpeded tunnel conduction[20-25]. Maintaining a high charge density at the semiconductor/oxide interface is desirable for all CIS cells: electrolyte-gated EIS cells (Type 0), metal-gated MIS cells (Type 1 and Type 2), and for semiconductor-gated cells (SIS) in which a degenerate semiconductor acts as the contact, as would be the case for a highly conductive (e.g. defect doped) TiO_2-nSi junction. The photovoltage produced by such junctions is controlled by the built-in voltage, which is calculated as the difference between the gate work function (whether electrolyte, metal, or degenerate semiconductor) and the work function of the base semiconductor modified by the presence of charges and interface fields[23]. The inversion layer's function in these cells was to screen states at the oxide/silicon interface[26] as well as facilitating minority carrier transport across the insulator. Green and colleagues specifically used minimally defective insulators of 1 to 3 nm, providing both near ideal surface passivation and narrow tunnel barriers[20-

[24]. In the present context, however, leaky insulators of much greater thickness are of interest as protection layers[10], motivating further study.

The original report of Type-1 nSi ALD-TiO_2 protection achieved good photovoltage with a tunnel oxide MIS[9]. The more recent reports with highly conductive TiO_2 may describe SIS junctions incorporating a Ni OER (oxidation evolution reaction) catalyst, the degenerate (defective) TiO_2, and an interfacial SiO_x[11]. Prior literature shows that large insulator trap densities can reduce MIS solar cell efficiency[18]. McDowell et al. have recently reported on highly conductive TiO_2 deposited by various methods with photovoltages between 150 and 350 mV[27]. They suggest that an nSi-TiO_2 SIS junction is formed, rather than a catalyst/oxide/silicon MIS junction. A highly conductive TiO_2 layer would screen the influence of the Ni catalyst workfunction[11], preventing it from setting the photovoltage. The workfunction of degenerate n-type TiO_2 will lie near the TiO_2 conduction band and is therefore unlikely to form a high photovoltage junction with nSi. Recent work by Mei et al.[28] also shows that a Ti metal layer between the TiO_2 and Si creates a highly conductive structure, perhaps by utilizing conduction band states directly, but the disadvantage to Type 1 voltage is the same, if not worse. Further, the Ti/Si interface is not stable, requiring precise high temperature annealing to avoid a resistive silicide[29-30].

In an effort to achieve good voltage and stability, a series of nSi photoanodes (Type 1) were fabricated with the Ir/ALD-TiO_2/SiO_2/Si layer sequence, independently varying the somewhat resistive TiO_2 and tunnel oxide SiO_2 independently. Iridium is chosen as the catalyst providing low water oxidation overpotential, stability at all pH, a high work function for optimal built-in voltage, and high density of states for optimal charge transport. Previous work[10-11] has

demonstrated that numerous other OER catalysts also exhibit advantageous work functions and high density of states for this Type 1 cell[10]. The photovoltage, herein defined as the difference between the overpotential to drive 1 mA/cm^2 through the illuminated nSi photoanode and dark p^+Si anode[31], is represented by the yellow, two-sided arrow in Figure 2-a. The thinnest as-deposited TiO_2 coatings yield photovoltages of 500-550 mV (Fig. 2-b). This value is between 150 and 400 mV higher than reported for highly-conductive TiO_2 protection layers on nSi[11, 27]. However, the inferred photovoltage decreases with increasing TiO_2 thickness to the point where it becomes negative (Fig. 2-c). By referencing the nSi (light) to the p^+Si (dark) overpotential for the same TiO_2 thickness, the oxide series resistance is removed, emphasizing that this component of the photovoltage loss is not due solely to Ohmic loss in the oxide.

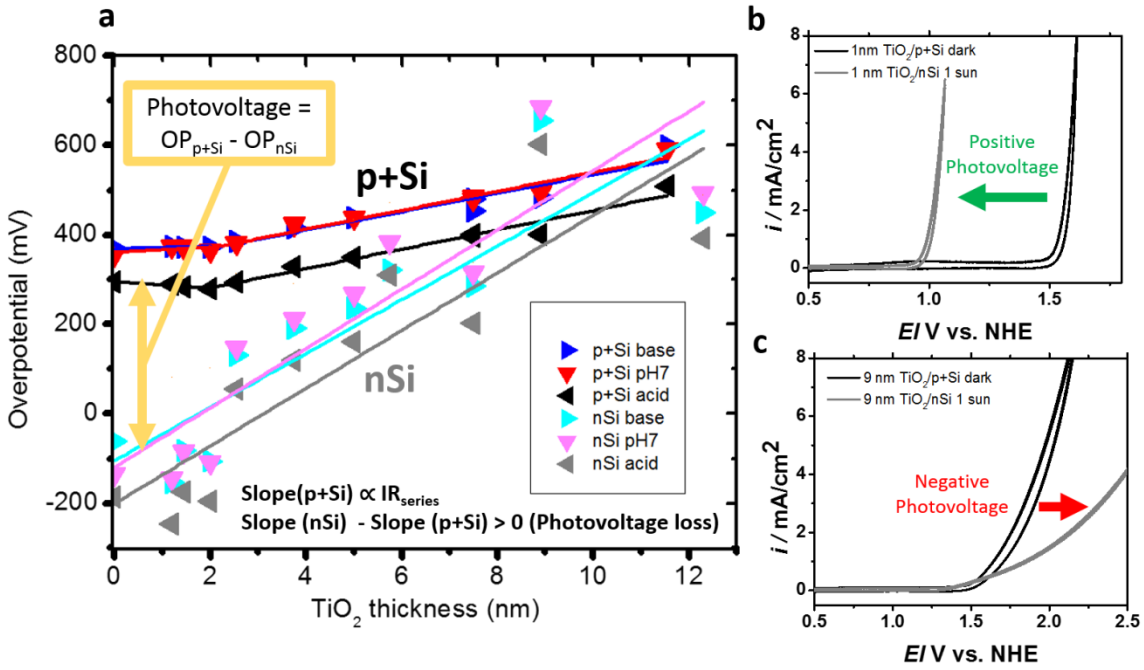


Figure 2 | Photovoltage loss in ALD-TiO_2 protected nSi MIS anodes. a – Water oxidation overpotential at 1 mA/cm^2 current density i.e. the potential w.r.t. to the thermodynamic potential $E^0(H_2O/O_2)$ at a pH of 14, 7, and 0 respectively. Device results are plotted as a function of TiO_2 thickness in Ir/TiO_2/SiO_2/p^+Si anodes in the dark compared to Ir/TiO_2/SiO_2/nSi photoanodes

under 1 sun illumination. The trends converge showing a decreasing photovoltage that starts, **b,** at a value > 500 mV and ends, **c,** with negative apparent photovoltages. Side panels are both for water oxidation in pH = 0 acid solution.

This thickness-dependent photovoltage loss is on order three times higher than the Ohmic loss in the reference p^+Si structure. To better understand this loss insulator fixed charge and Shockley-Read-Hall (SRH) recombination were investigated, two common factors affecting voltage. For fixed charge, a set of matching p-type MIS capacitors were fabricated (see supplementary Figure S1). Bulk positive or negative insulator charge can be observed as a parabolic shift of the flat band voltage (V_{FB}) with insulator thickness in either p-type or n-type silicon in capacitance-voltage (CV) analysis. When probing TiO_2, p-type silicon is the better candidate as lower leakage gives a more robust V_{FB} analysis. Figure S1 shows reasonable V_{FB} with no oxide thickness dependence, suggesting that fixed insulator charge is negligible and unchanging. Additionally, p^+Si anodes were measured electrochemically in dark and light to detect any light-induced charging. As shown (S2), no charging under illumination is observed.

To investigate SRH recombination, the reverse dark current was measured. An increase in the density of recombination-generation (R-G) centers will increase the rate of thermal generation of minority carriers increasing reverse saturation current, I_0. The measured reverse dark currents do not correlate with the low photovoltage devices, however. Rather, I_0 decreases with insulator thickness showing Ohmic behaviour with decreasing hole conductivity (Supplementary S3). Thus, neither of these factors, fixed charge in the oxide nor an increasing density of SRH recombination centers, is consistent with the observed decreasing photovoltage with increasing

oxide thickness.

Photovoltage loss also observed with interlayer SiO_2

Different SiO_2 interlayer thicknesses were also probed for photovoltage-dependence using slot-plane-antenna (SPA) plasma oxidation previously shown to give high quality tunnel oxide layers with precise thickness control[32-34]. Figure 3 shows the photovoltage-dependence with SiO_2 thickness both with and without ALD-TiO_2. In both cases, the photovoltage decreases with oxide thickness.

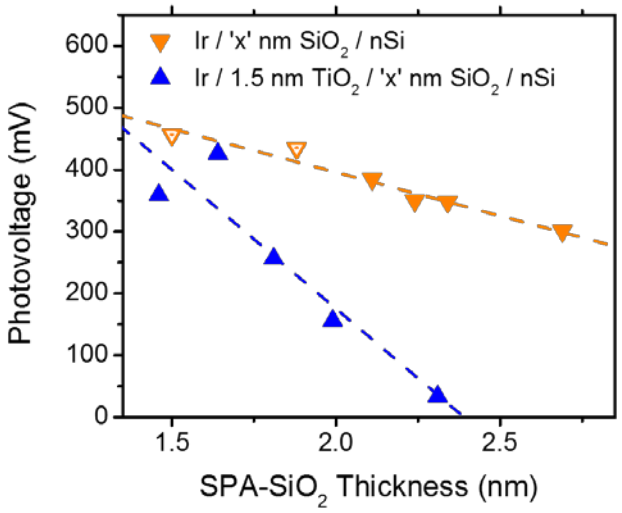


Figure 3 | Photovoltage loss observed with increasing thickness of the SiO_2 interlayer with and without TiO_2. The photovoltage decreases with thickness of the SiO_2 both with protective TiO_2 (blue) and without (orange). Anodes with less than 2 nm of SiO_2 and no protective TiO_2 (hollow orange markers) are highly unstable and the results are subject to error. It is possible that these devices have already degraded leading to an underestimation of the photovoltage loss with respect to thickness for Ir/SiO_2/nSi photoanodes (see Fig. S4). In all cases, the photovoltage decreases rapidly with SiO_2 interlayer thickness and, similar to the TiO_2 case, with a linear dependence on thickness, although the slope is much greater.

Simple metal / SiO_2 / Si devices also exhibit decreasing photovoltage with increasing oxide thickness. The ALD-TiO_2 used in this study is less resistive than the tunnel oxide SiO_2, but more resistive than the TiO_2 reported in reference 11. The fact that adding a second insulator (TiO_2) inside the junction increases the photovoltage loss at an equivalent SiO_2 thickness suggests the source of the photovoltage loss: a charge extraction barrier where greater voltage is required at greater oxide thicknesses to extract the same current from the device. This effect should be independent of any catalyst with a similar density of states, indicating that this loss is of general concern for MIS Type 1 photoelectrodes both those with and without additional protection layers[35].

Such a charge extraction barrier also relates to the observation that Type 0 liquid-junction cells capped with thicker oxides, where the charge must move into the electrolyte directly (as shown in Figure 1), also exhibit very low photovoltage. Type 0 TiO_2/SiO_2/nSi and SiO_2/nSi photoelectrochemical cells with a high work function electrolyte, ferri/ferrocyanide, exhibit essentially no photovoltage (Supplementary Fig. S5). The effect of decreasing photovoltage with electrical impedance within the junction is thus applicable to Type 0 and Type 1 cells alike with an increased penalty for a low density of states contact as in the Type 0 case.

Capacitor Model for Voltage Loss and Record Photovoltages with p^+n Buried Junctions

Previous work on MIS photovoltaics showed that inversion layer n-type MIS junctions could perform as well as p^+n buried junctions principally due to surface state screening[20-25]. In that work, the insulator was believed to promote ideal Schottky behaviour, which required only very

thin insulating layers with no benefit from thicker layers. To study this new regime where thicker layers provide benefit for device stability, Sentaurus[36] modelling software was used to simulate band diagrams of Schottky (Type 1) and p^+n (Type 2) photoanodes[37]. The Type 1 cell contains a surface inversion layer as result of the high workfunction catalyst, but the hole density is less than in a Type 2 cell, and is more sensitive to illumination and current flow. (Supplementary Fig. S6). The implanted p^+ region maintains high hole density on the interface, and the deeper it is placed, the more the interface charge is unaffected by operating conditions. However, if buried deeper than the minority carrier diffusion length (approximately 1 μm[38-39] for degenerate boron-doping ~10^{19} cm^{-3}) recombination will increase again.

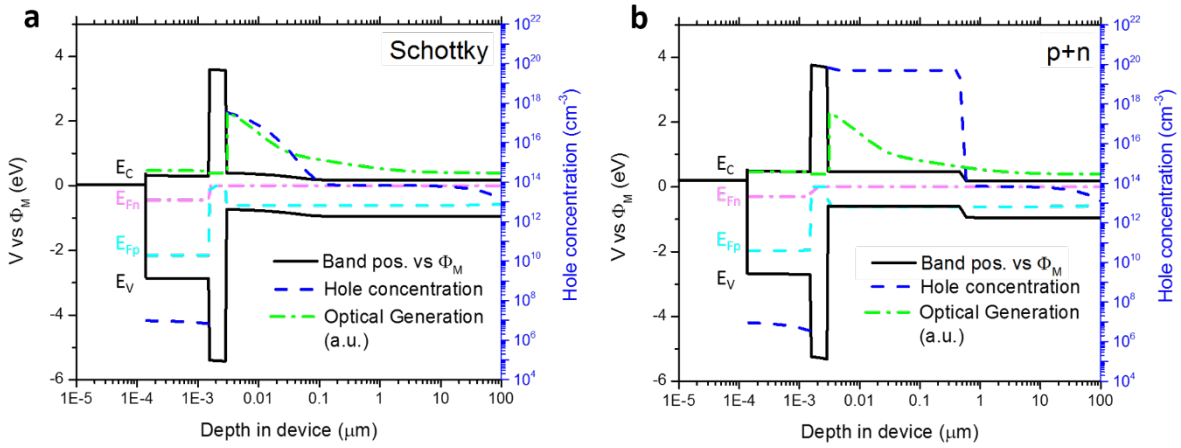


Figure 4 | Simulated band diagrams reveal differences between Type I Schottky junction structures and Type 2 p^+n buried junction structures. Band diagrams are simulated under 1 sun of AM 1.5G illumination and device operation at 1 mA/cm^2 for **a,** the Type 1 MIS Schottky and **b,** the Type 2 buried junction case. E_C and E_V denote the conduction band and valence band. E_{Fn} and E_{Fp} denote the quasi-electron and quasi-hole Fermi levels under illumination. The high work function metal creates a thin inversion layer of holes in the Type 1 nSi structure reaching 3e17 cm^{-3} at the interface, but it is insufficient to maintain a high hole density at the interface regardless of operating conditions compared to a 5e19 cm^{-3} implanted p^+ region. The optical

generation is shown here in arbitrary units. Full details and the integrated photogeneration can be found in Supplementary S7.

From this modelling, buried junction p^+nSi substrates were prepared with a high implantation dose ~5e19 cm^{-3} and junction depth below the 1 μm minority carrier diffusion length. The depth was characterized from an etched bevel and by SEM cross-section imaging, both methods yielding approximately 450 nm (S8-S9). Equivalent insulator layers and catalyst metal were deposited on these substrates, p^+Si, and nSi to compare the photovoltage-dependence of Type 1 and Type 2 structures. Capacitance-voltage analysis was carried out on these devices and on those in Figure 2, confirming that the nSi Type 1 structure does display an inversion layer at zero applied bias (Supplemental Information S10). As in Fig. 2, a large photovoltage loss relative to the p^+Si sample was observed with increasing TiO_2 thickness for Type 1, but Type 2 showed no loss relative to the p^+Si sample. Furthermore, record photovoltages were achieved across the thickness range studied.

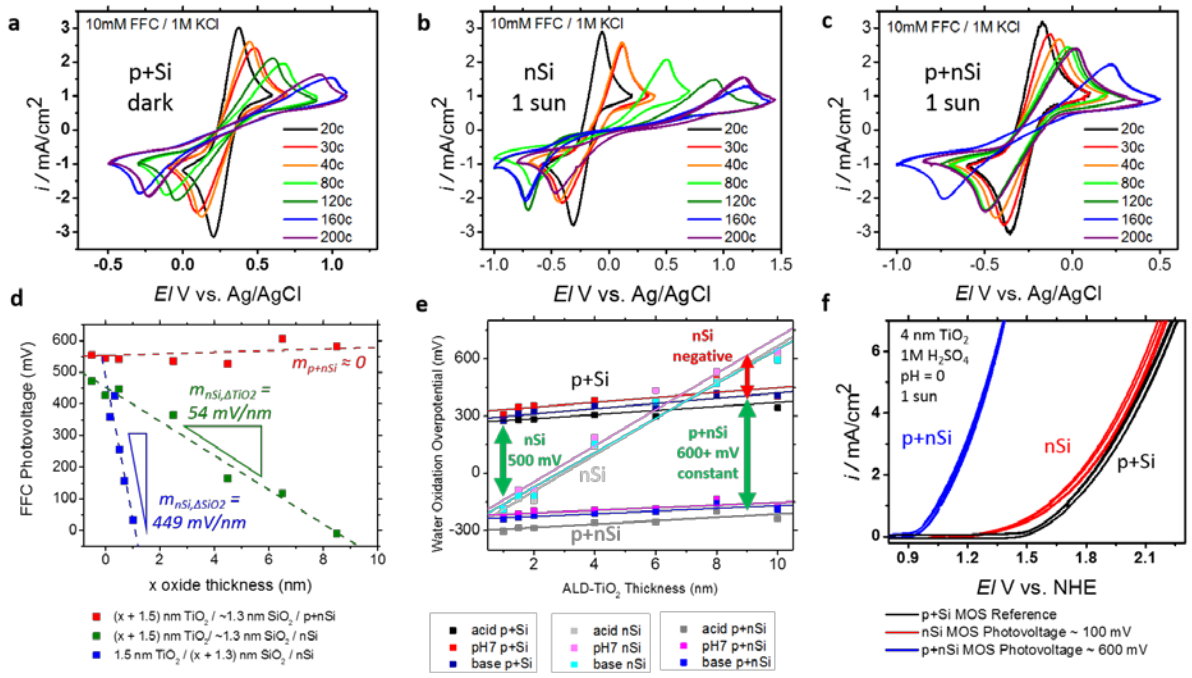


Figure 5 | Charge extraction photovoltage loss eliminated and record photovoltages achieved with Type 2 p^+n buried junction cells. Electrochemical performance of Ir / ALD-TiO_2 / SiO_2 / Si anode in ferro/ferrocyanide for **a,** p^+Si reference substrate **b,** nSi Type 1 MIS junction under 1 sun illumination and **c,** p^+nSi Type 2 buried junction under 1 sun. A large, asymmetric loss (asymmetric stretch out of the CV) is observed for Type 1 nSi MIS structures, compared to the p^+Si reference, that is eliminated in the Type 2 p^+n Si structure. **d,** This translates to a near constant photovoltage for Type 2 cells (■) compared to steep losses when increasing TiO_2 (■) or SiO_2 (■) in the Type 1 cell. **e,** For water oxidation, the same effect is observed where the Type 2 p^+nSi leads to a constant overpotential shift with respect to the p^+Si (dark) reference, corresponding to record photovoltages of 550 mV to > 600 mV at all pH values. In the Type 1 nSi cell, the inferred photovoltage goes from positive (↕) 500 mV to negative (↕) 200 mV. **f,** 4 nm TiO_2 water oxidation cyclic voltammetry showing ~ 100 mV photovoltage shift in the nSi MIS compared to ~ 600 mV shift for the equivalent p^+nSi MIS.

Cyclic voltammetry data for ferri/ferrocyanide (FFC) redox clearly show large asymmetric losses at positive potentials for the Type I nSi structure corresponding to the extraction barrier to holes (Fig. 5-b versus to Fig. 5-a). The p^+nSi series, alternatively, shows nearly identical ferri/ferrocyanide peak shapes as shown by p^+Si but shifted by large photovoltages that are independent of protective insulator thickness. Figure 5-d shows the improvement obtained with p^+nSi compared to Type 1 nSi, eliminating the loss and achieving photovoltages of over 600 mV versus both the ferri/ferrocyanide Nernstian cell potential and for water oxidation calculated as the shift between the p^+Si reference and photoanode at approximately zero current (Supplementary S14). The highest value is 607 mV in FFC and 630 mV in pH 7 solution with 8 nm of TiO_2. Similar values of 550 mV to >600 mV are achieved for all thicknesses and pH (Supplementary Table S15). The previous record for silicon water oxidation was 550 mV set with ultrathin TiO_2 on nSi using a post-ALD forming gas anneal[9]. Other leading results for stable MIS photoanodes include 410 mV with highly conductive TiO_2 on nSi and 520 mV on p^+nSi[11], 500 mV with Ni catalyst protecting nSi[17], and 500 mV with Ir/IrO_x or NiO_x protection of p^+nSi[18-19]. Another recent report using a p-type transparent oxide $NiCo_2O_4$ as the protection layer with the valence band aligned for hole transport achieves a photovoltage shift at 1mA/cm^2 of 506 mV vs the p^+Si reference, modelling a theoretical open circuit voltage of ~650 mV from the p^+n junction.[40] The record photovoltages obtained in this report using p^+nSi junctions stand in contrast to the negative apparent photovoltages for nSi MIS photoelectrolysis with protective layers of identical thickness.

These findings support the hypothesis that a charge extraction barrier introduced by interposed

insulators introduces the loss and that achieving a characteristic hole interface density for a given current density at the silicon/insulator interface is required. This is a requirement of Gauss' Law. A given hole interface density in the semiconductor Q_{si} sets the surface field in the semiconductor $E_{s.}$ This field in turn sets the field in the insulator $E_{i,}$ which controls the leakage current through the insulator. Therefore, a given insulator leakage current density requires a characteristic interface charge density:

$$Q_{si} = -\varepsilon_0 \varepsilon_s E_s = -\varepsilon_0 \varepsilon_i E_i \quad (2)$$

Equation 2 holds true assuming negligible fixed charge at the interface where ε_0 is the permittivity of free space, and ε_i and ε_s are the relative permitivities of the insulator and semiconductor. If, in general Type 1 structures, the surface charge is insufficient to achieve the needed photocurrent, a photovoltage penalty ΔV is incurred to increase the charge an amount ΔQ for a given insulator thickness t_i as given by equation (3) where A is the area:

$$\Delta V = \frac{\Delta Q}{C} = \frac{\Delta Q}{\varepsilon_0 \varepsilon_i A} t_i \quad (3)$$

This predicted linear relationship between photovoltage loss and insulator thickness agrees with our results. Further, the constant of proportionality depends on the dielectric properties of the insulators. By considering a bilayer TiO_2/SiO_2 structure, the model can be extended. Figure 5-d shows the empirical scaling of the photovoltage-dependence for TiO_2 and SiO_2 individually. These trends intersect representing the same device and necessarily the same surface charge. Taking the ratio of the partial derivatives about this shared point (Supplementary S16) yields equation (4), where *m* denotes the slope of the photovoltage loss (dV/dt_i):

$$\frac{m_{SiO2}}{m_{TiO2}} = \frac{\varepsilon_{TiO2}}{\varepsilon_{SiO2}} \quad (4)$$

Equation (4) states that the ratio of the photovoltage losses for Type 1 junctions as a function of TiO_2 and SiO_2 thickness, m_{TiO2} and m_{SiO2}, respectively, is equal to the inverse ratio of the insulators' dielectric constants. For ferri/ferrocyanide redox, the bilayer photovoltage-dependence w.r.t. SiO_2 is ~ 449 mV/nm and w.r.t. ALD-TiO_2 is ~ 54 mV/nm. We assume dielectric constants of 3.9[41] for SiO_2 and 32[42] for TiO_2 as previously measured for similar amorphous ALD-TiO_2. Predictions of the capacitor model and the observed empirical photovoltage scalings with TiO_2 and SiO_2 thickness are in excellent quantitative agreement (Table I).

Table I. Photovoltage loss and inverse dielectric constant ratios for TiO_2/SiO_2 Type 1 anodes

System	Photovoltage trend ratio	Inverse dielectric constant ratio
$\frac{\text{1.5 nm } TiO_2 \text{ / 'x' nm } SiO_2}{\text{'x' nm } TiO_2 \text{ / 1.3 nm } SiO_2}$	$\frac{449\ mV/nm}{54\ mV/nm} = 8.3$	$\frac{32}{3.9} = 8.2$

These results indicate the necessity of maintaining high minority-carrier interface charge density for efficient MIS operation with thicker protective insulators. This effect is not restricted to silicon as the semiconductor, and should not only be generally applicable to various metal-insulator-semiconductor systems, but also to electrolyte-insulator-semiconductor (EIS) and semiconductor-insulator-semiconductor (SIS) systems whenever conduction through thicker insulators is required. Consideration of these design principles allows one to understand the surprising result that record photovoltages in Type 2 p^+nSi structures and negative inferred photovoltages in Type 1 nSi structures are observed for identical insulator layers and OER catalyst.

Conclusions

In this report we have observed and quantified the photovoltage loss associated with insulator extraction barriers in MIS water-splitting cells based on n-type silicon, proposed a general model to understand and predict these losses, and fabricated cells using a p^+n silicon anode structure that overcomes this loss realizing record photovoltages at all insulator thicknesses studied, with a maximum of 630 mV. Understanding the protection layer's relationship to built-in field, interface quality, and charge extraction suggests a set of general design principles: **1 - Balance minimal insulator losses with a high quality interface to ensure high built-in field and low recombination.** High interface trap densities approaching ~1%, or ~10^{13} cm^{-2} states, may pin the Fermi level[43]. Alternatively, degenerate doping of an insulator changes the device to an SIS architecture, which can only achieve ideal built-in fields if the doped insulator maintains a high work function. Less defective insulators can provide ideal surface passivation and allow the high work function contact to set the field. For the nSi case, this report demonstrates photovoltages of 550 mV with an MIS, compared to ~400 mV photovoltage with highly conductive TiO_2[11]. **2 - Minimize charge extraction barriers to insure high photovoltage during current operation.** This can be accomplished by (a) reducing the insulator resistance within the junction or by (b) separating the insulator layers from the junction and keeping the interface charge density high using a Type 2 p^+n anode structure. **Reducing insulator resistance** must not compromise chemical, electrical, and thermal stability or diminish voltage. Further study is needed for generic and well-understood methods here. **Keeping the interface charge density high** promotes facile extraction across insulators. A Type 2 junction depth of ~450 nm with 5e10^{19} cm^{-3} hole concentration was sufficient to recover all photovoltage lost by corresponding Type 1 cells. The junction depth should not exceed the minority carrier diffusion length.

Materials and Methods

Heavily boron-doped (100) p-type silicon wafers (ρ=0.001-0.002 Ω·cm, thickness 505-545 μm) were used as conductive silicon substrates to study water oxidation in the dark. Moderately phosphorous-doped (100) n-type silicon wafers (ρ=0.14-0.24 Ω·cm, thickness 450 μm) were used for Type I MIS Schottky junction photoanodes. Buried junction devices were made with n-type silicon wafers and were subjected to a standard clean using a Semitool Spray Acid: first the wafers are subjected to ozone and DI water, then NH_4OH (2000:1) is added to help remove particles and organics, and lastly ozone, DI water, and HF (1150:1) are used to etch the chemical oxide and regenerate the surface oxide also removing any metallic species. The implant is performed with a 4×10^{15} cm^2 dose of boron at 15 keV. Following the implantation, the samples were annealed at 950°C for 40 minutes. The junction depth was characterized in two ways. First the surface was bevelled at a known angle through the p^+ surface region and the nSi was stained allowing for an optical measurement to determine the depth. This resulted in a calculated depth of 448 nm. Secondly, the p^+ region was preferentially etched using a HNO_3:HF solution and scanning electron microscopy (SEM) was utilized to directly measure a junction depth of ~460 nm. ALD-TiO_2 layers were deposited amorphous as deposited as detailed previously[44]. More details are also given in the supplementary.

Devices for SiO_2 thickness experiments were fabricated by slot-plan antenna (SPA) plasma oxidation. Before SiO_2 growth, prime grade Si (100) wafers were prepared using a three part clean: 10 minutes at 50°C in 5:1:1 H_2O:H_2O_2:NH_4OH to remove trace organics, 10 minutes at 50°C in 5:1:1 H_2O:H_2O_2:HCl to remove trace metal ions, and then 30 seconds in 2% HF to remove the silicon dioxide layer. The SiO_2 layer is regrown with precise thickness control using the slot plane

antenna (SPA) method, which utilizes radical oxidation to grow ultrathin oxide layers with reproducibility equal to or greater than that of thermal oxidation, and at significantly lower temperatures, achieving 0.7 to 1.0 % thickness non-uniformity for films of 1.5 nm to 10 nm thickness at temperatures as low as 400˚C[32-34].

Device simulations were performed using Synopsys Sentaurus (Version I-2013.12-SP1). Default material properties, found within the software, were used for both silicon and SiO_2. Doping densities and junction depths were set to the material values reported in the main body of the manuscript and supplementary for the silicon actually used. The material TiO_2 is not found within the Sentaurus default material database and therefore its material properties were added manually. Moderate n type doping of 1×10^{17} cm^{-3} was assumed. For the TiO_2 band structure we assumed an electron affinity of 4.2 eV[45] relative to vacuum and a bandgap of 3.2 eV[46]. Optical constants for TiO_2 were incorporated over the desired spectral range from previous literature values[47]. The default Sentaurus parameters were used for the Shockley-Read-Hall lifetimes of 10 μs and 3 μs for electrons and holes respectively. The front and back contact metals were iridium and aluminum respectively again reflecting the actual devices fabricated in this study. Modelling of the electrodes consisted of defining the work functions of each contact. We assumed a work function of 5.1 eV and 4.1 eV for iridium and aluminum respectively based on ranges for values of 5.0-5.67 eV and 4.06-4.26 reported in the literature[48]. Surface recombination velocities of 2.57×10^6 cm/s and 1.93×10^6 cm/s were assumed for electrons and holes respectively at the iridium-TiO_2 interface. This interface is modeled using the Schottky contact physics model built into Synopsys Sentaurus. For all materials we assume the presence of both SRH and radiative recombination defined by the models present in the Synopsys Sentaurus™ Device User Guide using the specified material properties listed above and those

included as default parameters in Synopsys Sentaurus material database. Optical generation was modelled using the Transfer Matrix Method (TMM) using a representative version of the AM1.5G spectrum. Description of optical generation models used by Sentaurus can be found within the Sentaurus^{TM} Device User Guide.

Further details are given in the Supplementary Information.

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Author Contributions

A.S. and J.L. prepared all samples and performed all measurements for the initial TiO_2

photovoltage series first observing the photovoltage loss. A.S. prepared all samples and performed all measurements for the SiO_2 photovoltage series, capacitance voltage measurements, and buried junction p^+nSi experiments. A.W. prepared all p^+n buried junction substrates and performed all physical characterization of these junctions. K.K. performed Sentaurus modelling for light absorption in Type I and Type II cells as well as simulating band diagrams. A.S. and K.K. maintained the ALD chamber for TiO_2 depositions and A.S. qualified and performed the runs. A.S., C.E.D.C. P.H. and P.C.M. designed the experiments and developed the solid state capacitor model to explain the loss. All authors helped in the preparation of the manuscript.

Additional Information

Supplementary Information accompanies this paper at (attached).

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35) The OER catalyst alone has been used to at least temporarily promote stability (nickel[17], nickel oxide[19], and iridium oxide[18]). Even if the need for additional oxide protection is lessened, an interfacial layer of SiO_2 remains for silicon substrates. Etching with HF(aq) leaves a hydrogen passivated surface, which is not ideal for subsequent film nucleation, often leading to islanded film growth and some SiO_2 regrowth. Further, it is difficult to completely remove SiO_2. Oxygen scavenging using reactive metal layers can decompose the SiO_2 layer[49], but some remains[50]. Thus, native oxides, in addition to protective oxides, play an important role in determining this photovoltage loss.

36) Sentaurus is a modeling software developed by Synposys Inc. Technical details are given in the methods section.

37) Hand drawn band diagrams are typically plotted with a convenient linear scale, where the metal and oxide layers are drawn to one scale, and the semiconductor junction is drawn on

a compressed linear scale so the band bending can be seen. These band diagrams are drawn correctly with a logarithmic x-axis, which makes the band bending appear to have an inflection point, but on a linear scale, the curvature is smooth and extended.

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