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A systematic study of $(NH_4)_2S$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ system for *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ epitaxial layers

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A systematic study of $(NH_4)_2S$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ system for *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ epitaxial layers

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In this work, we present the results of an investigation into the effectiveness of varying ammonium sulphide $(NH_4)_2S$ concentrations in the passivation of *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$. Samples were degreased and immersed in aqueous $(NH_4)_2S$ solutions of concentrations 22%, 10%, 5%, or 1% for 20 min at 295 K, immediately prior to atomic layer deposition of Al_2O_3. Multi-frequency capacitance-voltage (C-V) results on capacitor structures indicate that the lowest frequency dispersion over the bias range examined occurs for *n*-type and *p*-type devices treated with the 10%$(NH_4)_2S$ solution. The deleterious effect on device behavior of increased ambient exposure time after removal from 10%$(NH_4)_2S$ solution is also presented. Estimations of the interface state defect density (D_{it}) for the optimum 10%$(NH_4)_2S$ passivated $In_{0.53}Ga_{0.47}As$ devices extracted using an approximation to the conductance method, and also extracted using the temperature-modified high-low frequency C-V method, indicate that the same defect is present over *n*-type and *p*-type devices having an integrated D_{it} of $\sim 2.5\times10^{12}$ cm^{-2} ($\pm 1\times10^{12}$ cm^{-2}) with the peak density positioned in the middle of the $In_{0.53}Ga_{0.47}As$ band gap at approximately 0.37 eV ($\pm$0.03 eV) from the valence band edge. Both methods used for extracting D_{it} show very good agreement, providing evidence to support that the conductance method can be applied to devices incorporating high-*k* oxides on $In_{0.53}Ga_{0.47}As$. © *2011 American Institute of Physics*. [doi:10.1063/1.3533959]

I. INTRODUCTION

In order to continue complementary metal-oxide-semiconductor (CMOS) development beyond the 22 nm node, high-mobility III-V channel layers such as $In_{0.53}Ga_{0.47}As$, in combination with alternative gate oxides such as Al_2O_3, are currently under investigation. The interfacial chemistry for high-*k* materials on III-V substrates is more complex than the Si/SiO_2 system, with the possibility for competing bonding structures comprising more than one substrate element, and associated native oxides, to contribute to interfacial defects. This factor has been one of the main obstacles to the development of viable high-*k*/III-V devices, since a high interface state density (D_{it}) has a critical detrimental effect on device characteristics, and as such has motivated extensive research in trying to understand the cause of these defects, and on the passivation of the high-*k*/III-V interface in an attempt to reduce D_{it}.[1–7] One of the more common *ex situ* passivation techniques involves the use of sulfur based chemicals such as ammonium sulphide $(NH_4)_2S$.[8–12] Aqueous $(NH_4)_2S$ is widely used due to its' effectiveness at removing native oxides, and at improving the electrical characteristics of devices fabricated on $(NH_4)_2S$ treated surfaces.[5,6] In addition, passivation in $(NH_4)_2S$ solution is a relatively quick, cost-effective, and straight-forward process. However, there is little discussion in the literature regarding the optimization of the passivation procedure. Despite it being a simple process, there are a number of important parameters which can have a decisive bearing on the efficacy of the passivation, principal among these being: the surface pretreatment, if any, prior to immersion in the $(NH_4)_2S$ solution; the passivation time in the $(NH_4)_2S$ solution; the concentration of the $(NH_4)_2S$ solution; and the temperature of the $(NH_4)_2S$ solution. An extensive chemical and physical study, using x-ray photoelectron spectroscopy (XPS) and atomic force microscopy, by Brennan *et al.* investigated the optimum aqueous ammonium sulphide passivation conditions.[13] The results of that work established that an initial decrease followed by immersion for 20 min in a 10%$(NH_4)_2S$ solution at room temperature, was the most effective in terms of suppression of native oxide formation and in minimizing surface roughening effects. Given the positive results from that chemical and physical analysis, the principal aim of this work is to investigate the electrical char-

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acteristics of MOS devices to understand the effects of varying the $(NH_4)_2S$ concentration in the passivation of *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ surfaces prior to atomic layer deposition (ALD) of Al_2O_3. A secondary objective of this study is to utilize the electrical results from the MOS device exhibiting the best electrical characteristics, to perform a detailed comparison of the extracted D_{it} across the $In_{0.53}Ga_{0.47}As$ energy gap at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface using two different methods, the temperature modified high-low frequency C-V method and the more traditional approximation to the conductance method.

II. EXPERIMENTAL DETAILS

The $In_{0.53}Ga_{0.47}As$ epitaxial layers used in this work were either (1) ~2 μm *n*-type $In_{0.53}Ga_{0.47}As$ (S at ~4×10^{17} cm^{-3}) grown by MOVPE on heavily (S at ~2×10^{18} cm^{-3}) *n*-doped InP(100) wafers, or (2) ~2 μm *p*-type $In_{0.53}Ga_{0.47}As$ (Zn at ~4×10^{17} cm^{-3}) grown by MOVPE on heavily *p*-doped (Zn at ~2×10^{18} cm^{-3}) InP(100) wafers. Identical epitaxial layers and substrates were used previously in the chemical and physical study by Brennan *et al.*[13] Prior to immersion in aqueous $(NH_4)_2S$ solutions, all $In_{0.53}Ga_{0.47}As$ surfaces were initially degreased by sequentially rinsing for 1 min each in acetone, methanol, and isopropanol. $(NH_4)_2S$ concentrations of 22%, 10%, 5%, and 1% in deionized H_2O were used, and the $In_{0.53}Ga_{0.47}As$ surfaces were subjected to the dilute $(NH_4)_2S$ for 20 min, with the solution at room temperature (~295 K). Samples were introduced to the ALD chamber load lock (base pressure of less than 2×10^{-8} mbar) within ~7 min after removal from the aqueous $(NH_4)_2S$ solution, unless otherwise stated. This air exposure was kept as short as possible in an effort to minimize both native oxide regrowth and ambient contamination prior to Al_2O_3 growth (nominal thickness 8 nm). Gate contacts ~100 nm thick were formed by e-beam evaporation of Ni (60 nm), and Au (40 nm), through a shadow mask. For comparative purposes across all samples, the electrical tests were performed on capacitors of nominal 100 μm diameter, and in order to rule out variation due to any differences in the shadow masks used for metal deposition, the actual dimensions of the test devices were measured using an optical microscope for all samples. Multiple sites were examined in all cases to ensure the results are representative of device behavior. It is also noted that larger and smaller device areas were measured on all samples and the capacitance scaled as expected with area. Back metal contacts of Ti/Au (for *p*-type devices) and Au/Ge/Au/Ni/Au (for *n*-type devices) were deposited, followed by a 30 s rapid thermal anneal (RTA) at 623 K in N_2. The back metal contact formation was carried out to minimize any contribution of series resistance to the electrical results. The capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were recorded using a HP4284A LCR meter. The measurements at room temperature were performed on-wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry air, dark environment (dew point $\leq$203 K). Conventional transmission electron microscopy (TEM) samples were prepared using focused ion beam thinning procedures in an FEI 200 Workstation and examined at 200 kV in a JEOL2000FX.[14] Monochromated XPS was carried out using an Al $K\alpha$ (1486.7 eV) x-ray source with a linewidth of 0.25 eV and an Omicron 125 mm seven channel hemispherical analyzer with a pass energy of 15 eV and seven Channeltron detection system described elsewhere.[15] Core level photoemission spectra were taken of the As $2p_{3/2}$, Ga $2p_{3/2}$, In $3d_{5/2}$, C 1*s*, O 1*s*, S 2*p*, As 3*d*, Ga 3*d*, and In 4*d* regions after loading to ultrahigh vacuum and prior to both Al_2O_3 and metal deposition in order to determine the chemical composition of the initial interfacial region.

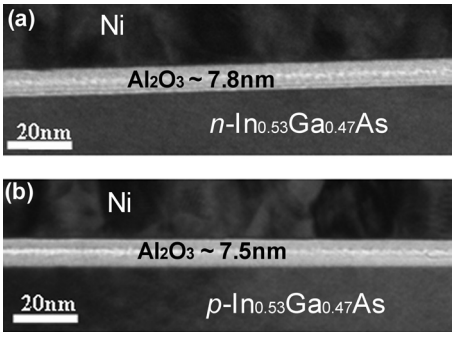


FIG. 1. Cross-sectional TEM micrographs of (a) 10%$(NH_4)_2S$ treated, Au/Ni/7.8 nm Al_2O_3/n-$In_{0.53}Ga_{0.47}As$/InP, and (b) 10%$(NH_4)_2S$ treated, Au/Ni/7.5nm Al_2O_3/p-$In_{0.53}Ga_{0.47}As$/InP device structures.

III. RESULTS AND DISCUSSION

TEM micrographs for *n*-type and *p*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ devices are shown in Figs. 1(a) and 1(b), respectively. These particular samples had received the 10%$(NH_4)_2S$ passivation prior to ALD deposition. The TEM results show that the actual physical thicknesses of the Al_2O_3 layers are close to the nominal value of 8 nm, and the ALD oxide layers exhibit good thickness uniformity over the area examined. The oxide layers also appear amorphous without any evidence of crystallite formation. In addition, it is noticeable that there is no visible roughening of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces from the 10%$(NH_4)_2S$ $In_{0.53}Ga_{0.47}As$ surface treatment. Roughening effects have been observed when higher concentrations (~22%), and temperatures (~333 K), of $(NH_4)_2S$ have been used, and in which case the $(NH_4)_2S$ may have partially etched the $In_{0.53}Ga_{0.47}As$ surface.[13,16] This is relevant to MOS field effect transistor (MOSFET) device transport properties as it is crucial to have as smooth an interface as possible because roughness at the oxide-semiconductor interface can result in surface scattering effects leading to reduced mobility. It is noted that there appears to be a band of lighter image contrast running through the center of the Al_2O_3 layer in both samples. In addition, this band was not observed in TEM micrographs taken from an area of the *n*-type sample with no gate metal (not shown), which may suggest that mechanical stress from the gate metal could be a contributing factor. However, the authors of this work have observed similar bands running through Al_2O_3 layers which were deposited in three independent ALD reactors. A detailed analysis of this

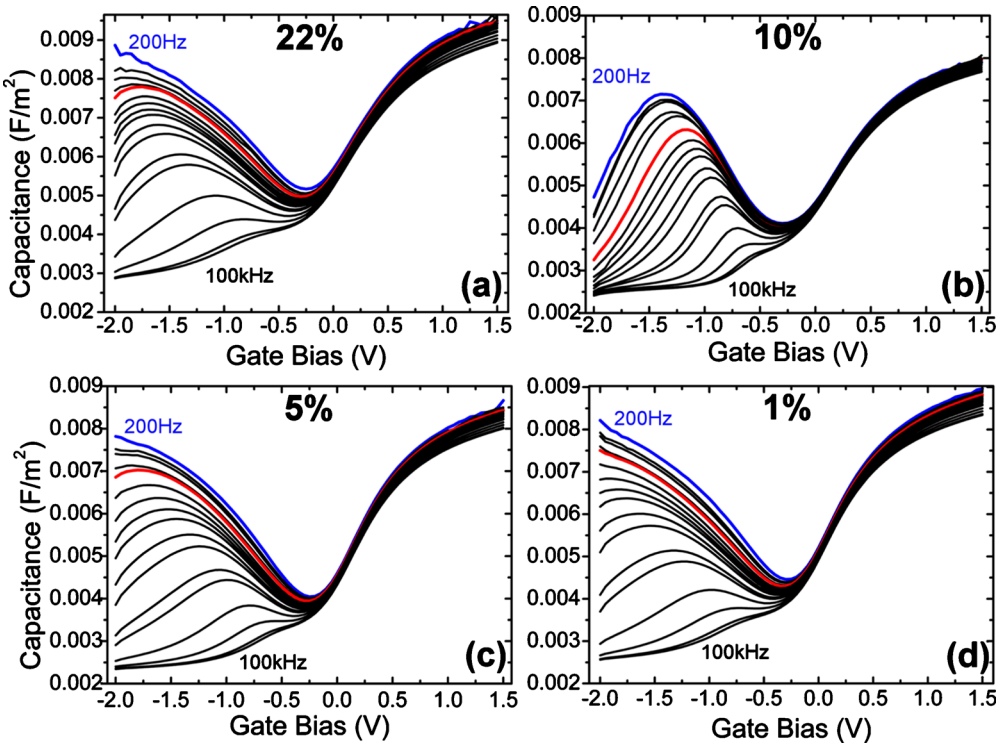


FIG. 2. (Color online) Room temperature C-V frequency variation (200 Hz to 100 kHz) of (a) 22%, (b) 10%, (c) 5%, and (d) 1%, $(NH_4)_2S$ treated, Au/Ni/~8 nm Al_2O_3/n-$In_{0.53}Ga_{0.47}As$/InP devices. All $In_{0.53}Ga_{0.47}As$ samples were introduced to the ALD chamber load lock as quickly as possible (<7 min) after removal from $(NH_4)_2S$ solution, in order to minimize ambient exposure. The actual diameters of the capacitor devices tested were: 118 μm, 106 μm, 106 μm, and 106 μm, for the 22%, 10%, 5%, and 1% samples, respectively. The frequencies measured and plotted above are as follows 200 Hz, 400 Hz, 500 Hz, 800 Hz, 1 kHz, 1.5 kHz, 2.0 kHz, 2.5 kHz, 3.0 kHz, 4 kHz, 5 kHz, 8 kHz, 10 kHz, 20 kHz, 40 kHz, 80 kHz, and 100 kHz. The 1 kHz curves have been highlighted in red to illustrate that a more accurate representation of the interface defect response is obtained by measuring down to 200 Hz.

effect is beyond the scope of this paper, and work is continuing to precisely identify the physical origin of this observation.

The C-V response at room temperature (295 K) with ac signal frequencies from 200 Hz to 100 kHz for the 22%, 10%, 5%, and 1%$(NH_4)_2S$ passivated *n*-type $In_{0.53}Ga_{0.47}As$ devices are shown in Figs. 2(a)–2(d), respectively. With regard to the 22%, 5%, and 1% devices, the frequency dispersion, with a broad peak response observed for V_{gate} in the range of −0.25 to −2 V, is typical of that commonly observed in the literature for *n*-type $In_{0.53}Ga_{0.47}As$.[2,5,7,17–19] This is characteristic of interface defects with a peak density at a specific energy in the $In_{0.53}Ga_{0.47}As$ band gap and is unlikely to be representative of true inversion at the Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ interface.[17] True inversion at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface would result in a constant capacitance as a function of V_{gate}, where the magnitude of this constant capacitance region increases with increasing temperature or decreasing measurement frequency up to a maximum value set by the oxide capacitance (C_{ox}).[20] A similar form of the C-V response observed in Figs. 2(a), 2(c), and 2(d), has been reported for different *n*-$In_{0.53}Ga_{0.47}As$ surface preparations, different high-*k* oxide layers, different high-*k* deposition methods, and for samples with and without interlayer oxides.[2,5,7,17–19] This indicates that the dominant interface defect originates from the $In_{0.53}Ga_{0.47}As$ surface, as opposed to the interfacial layer or high-*k* oxide, with vacancies or surface As-dimers as the possible origin of the interface states. However, for the 10% *n*-type device in Fig. 2(b), the C-V response is noticeably improved. There is a reduced response for the interface state related capacitance (C_{it}) at negative gate bias in terms of the peak magnitude and width, and it is significant that the C-V response goes through a peak and then decreases again as the gate bias approaches −2 V, even at 200 Hz. This is in contrast to the higher magnitude and broader profiles evident for the other three samples as seen in Figs. 2(a), 2(c), and 2(d). This suggests a reduction in the interface state density for the 10%$(NH_4)_2S$ surface treatment. It is also necessary here to stress the importance of measuring down to very low frequencies (200 Hz) in order to capture as much of the interface defect related response as possible. This allows for a more accurate determination of the interface state density as will be discussed later. It appears to be a common practice in much of the literature on this topic to only measure the C-V response down to 1 kHz. While this may give some useful information, and provide indications of device performance, it will also result in a significant underestimation of the extracted magnitude of the interface state defect density. In Figs. 2(a)–2(d), the 1 kHz C-V curves have been highlighted in red to illustrate that a more accurate representation of the interface defect response is obtained by measuring down to 200 Hz (blue curves). It should be noted that although all devices experienced a 30 s, 623 K RTA in N_2, for back contact formation, there has been no attempt as yet to anneal the samples in forming gas, an approach which has been shown to reduce interface defect concentrations on *n*-type $In_{0.53}Ga_{0.47}As$ MOS capacitor devices.[17,21,22] Therefore, po-

tential exists to further improve the C-V response of the 10% device to obtain results comparable with those recently reported by Kim *et al.*,[22] although it must be noted that in Kim's work the C-V response is only shown for a much more limited frequency range of 5 kHz and higher.

Another means to gauge the efficacy of the passivation treatment on the *n*-type $In_{0.53}Ga_{0.47}As$ devices is to compare the deviation of the measured accumulation capacitance from the expected theoretical capacitance. It has been reported for *n*-type $In_{0.53}Ga_{0.47}As$ that the theoretical C-V response is asymmetrical in shape, with a reduction in accumulation capacitance expected on *n*-type due to both the fact that the density of states in the $In_{0.53}Ga_{0.47}As$ conduction band (1.7×10^{17} cm^{-3}) is over one order of magnitude lower compared to the $In_{0.53}Ga_{0.47}As$ valence band (2.6×10^{18} cm^{-3}), and also due to charge quantization effects.[12,23,24] Brammertz *et al.*,[25] have reported that the inclusion of a large interface state distribution in the $In_{0.53}Ga_{0.47}As$ conduction band leads to an increase in the modeled theoretical accumulation capacitance, due to the capacitance contribution from these interface states. This is in agreement with C-V responses typically measured on *p*-type and *n*-type $In_{0.53}Ga_{0.47}As$ MOS structures which do not exhibit the asymmetry between the maximum accumulation capacitances. With regard to the samples in this work the theoretical capacitance has been calculated using a one dimensional self-consistent Poisson–Schrödinger C-V simulation.[26] This yields simulated theoretical values of accumulation capacitance (at $V_{gate}=1.5$ V) in the range 0.0065 to 0.007 F/m^2 for an ~8 nm thick Al_2O_3 film with dielectric constant values in the range 8 to 9. The simulated accumulation capacitance of 0.007 F/m^2 corresponds to a capacitance equivalent thickness (C_{et}) of 4.9 nm (assuming a dielectric constant for $SiO_2=3.9$). Based on the physical thickness of 7.8 nm for the Al_2O_3 and assuming dielectric constants for $Al_2O_3=9$ and for $SiO_2=3.9$, yields an equivalent oxide thickness (E_{ot}) of ~3.4 nm, which is 1.5 nm less than the simulated C_{et}. This can be accounted for by an E_{ot} correction which has been reported to be in the range of 1.1 nm to 1.5 nm for devices on $In_{0.53}Ga_{0.47}As$.[24]

It can be seen in the C-V responses in Fig. 2 that the actual measured accumulation capacitance at $V_{gate}=1.5$ V exceeds the simulated theoretical capacitance of 0.007 F/m^2 in all cases. The presence of interface states having energies aligned with the $In_{0.53}Ga_{0.47}As$ conduction band is the most likely explanation for the measured capacitance exceeding the theoretical capacitance for $Al_2O_3/n\text{-}In_{0.53}Ga_{0.47}As$ structures.[23–25] The difference between the measured and theoretical accumulation capacitance values, ΔC (in farad per square meter), is 0.0025, 0.0015, and 0.0020, for the 22%, 5%, and 1% passivated devices, respectively. This is reduced to 0.0009 for the 10% device and therefore the smallest deviation from the theoretical capacitance occurs for this sample. This provides evidence that for the 10% passivated device there is a reduction in the density of interface defects degenerate with the conduction band. The presence of such defects is technologically relevant for surface inversion mode *n*-channel $In_{0.53}Ga_{0.47}As$ MOSFETs, as beyond the threshold voltage, any additional charge applied to the gate will be partially compensated by charging of the interface defect level in the $In_{0.53}Ga_{0.47}As$ conduction band. The consequence will be a decrease in transconductance with gate voltage, and an apparent decrease in the inversion layer mobility. Both of these effects are observed experimentally in $In_{0.53}Ga_{0.47}As$ surface inversion mode *n*-channel MOSFETs.[27]

The C-V response at room temperature (295 K) with ac signal frequencies from 200 Hz to 100 kHz for the 22%, 10%, 5%, and 1% $(NH_4)_2S$ passivated *p*-type $In_{0.53}Ga_{0.47}As$ devices are shown in Figs. 3(a)–3(d), respectively. The C-V response at positive gate bias in this case is mainly attributable to interface state defects, not surface inversion where the capacitance becomes independent of the applied gate bias.[28] There does not appear to be a significant difference between the various aqueous $(NH_4)_2S$ concentrations in terms of their impact in reducing the interface defect response observed on all devices at $V_{gate} \sim 0.25$ V to 1.5 V. The clear improvement for the 10% treatment in reducing the defect response on *n*-type devices is not as noticeable in the *p*-type case. However, it is apparent in comparing the C-V curves shown in Fig. 2 that over the whole bias range investigated ($V_{gate}-2$ to 1.5 V) the 10% treated *p*-type device clearly exhibits the best characteristics in terms of having both the lowest frequency dispersion and the steepest transition from depletion to accumulation. It is particularly important in the case of these *p*-type devices to measure down to very low frequencies (200 Hz) in order to capture as much of the interface defect related response as possible. This is necessary in order to obtain a more accurate determination of the extracted interface state density as will be discussed later. In Figs. 3(a)–3(d), the 1 kHz curves have been highlighted in red to illustrate that a significantly better representation of the interface defect response is obtained by measuring down to 200 Hz (blue curves). It is also the case that the hysteresis measured around the flatband capacitance, C_{fb} at 100 kHz on *p*-type devices is approximately 15% higher for the other $(NH_4)_2S$ concentrations compared to the 10% passivated *p*-type device, which has a hysteresis of ~300 mV, as shown in Fig. 4. The hysteresis for all *n*-type devices is practically constant at ~80 mV for the different $(NH_4)_2S$ concentrations. Clockwise hysteresis was observed on *n*-type samples while anticlockwise hysteresis was observed on *p*-type samples. Note that the devices only experienced a 633 K, 30 s RTA in N_2 during metallization, and that no specific effort has been made to perform high temperature RTA as is common practice to reduce hysteresis levels.

As described in the experimental section, the time between removal of the $In_{0.53}Ga_{0.47}As$ sample from the aqueous $(NH_4)_2S$ solution and loading into the ALD chamber was minimized (typically under 7 min). Therefore, the samples saw as little exposure to ambient air and contaminants as was possible within the experimental setup. This was the case for all devices whose results are presented in Figs. 2 and 3. In order to investigate the effect of increased ambient exposure time, additional *n*-type and *p*-type samples were processed where the time between the removal of the InGaAs samples from a 10% $(NH_4)_2S$ solution to loading into the ALD chamber was extended to ~30 min. Figures 5(a) and 5(b) show the C-V response at room temperature (295 K) with ac signal

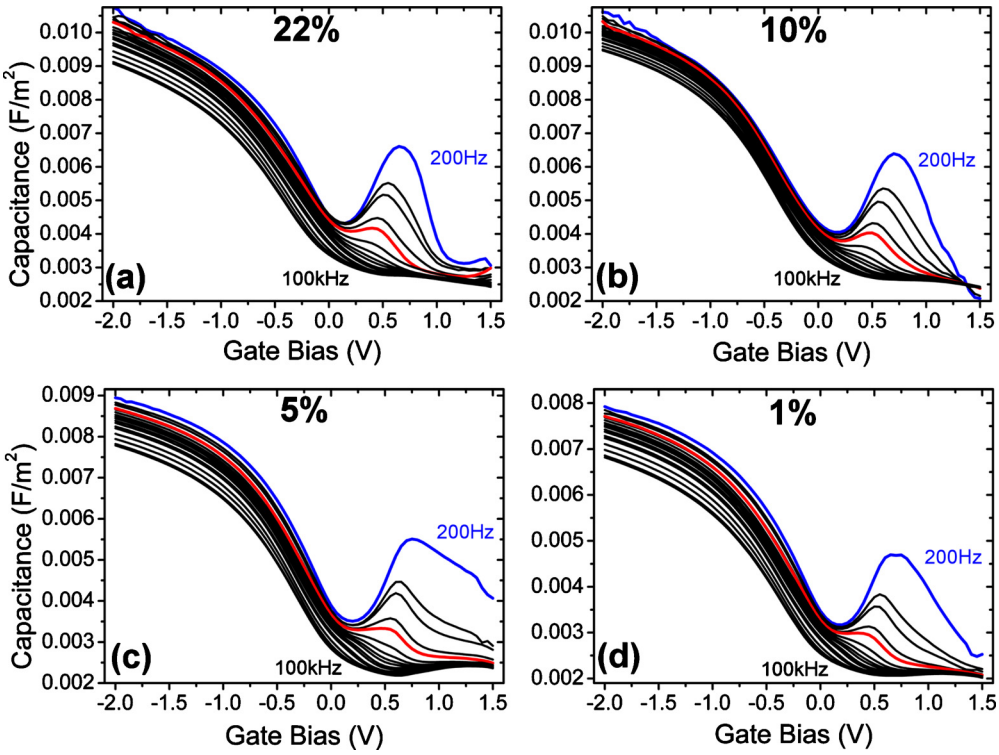


FIG. 3. (Color online) Room temperature C-V frequency variation (200 Hz to 100 kHz) of (a) 22%, (b) 10%, (c) 5%, and (d) 1%, $(NH_4)_2S$ treated, Au/Ni/~8 nm Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$/InP devices. All $In_{0.53}Ga_{0.47}As$ samples were introduced to the ALD chamber load lock as quickly as possible (<7 minutes) after removal from $(NH_4)_2S$ solution, in order to minimize ambient exposure. The actual diameters of the capacitor devices tested were: 111 μm, 113 μm, 110 μm, and 105 μm, for the 22%, 10%, 5%, and 1% samples, respectively. The frequencies measured and plotted above are as follows: 200 Hz, 400 Hz, 500 Hz, 800 Hz, 1 kHz, 1.5 kHz, 2.0 kHz, 2.5 kHz, 3.0 kHz, 4 kHz, 5 kHz, 8 kHz, 10 kHz, 20 kHz, 40 kHz, 80 kHz, and 100 kHz. The 1 kHz curves have been highlighted in red to illustrate that a more accurate representation of the interface defect response is obtained by measuring down to 200 Hz.

frequencies from 200 Hz to 100 kHz for the 10%$(NH_4)_2S$ passivated *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ devices with 30 min ambient exposure. In comparing the *n*-type C-V response in Fig. 5(a) of the sample with 30 min ambient exposure, with that in Fig. 2(b) of the sample with 7 min ambient exposure, it is immediately apparent that there is a significant increase in the C-V frequency dispersion and in the defect related response at negative gate bias for the device subjected to longer ambient exposure. The difference between the measured and theoretical accumulation capacitance values, ΔC (in farad per square meter), is 0.0020 for the 30 min exposure device, compared to just 0.0009 for the 7 min exposure device, which, as discussed previously, is suggestive of an increase in defects degenerate with the $In_{0.53}Ga_{0.47}As$ conduction band upon longer ambient exposure. In the case of the *p*-type MOS devices, a comparison of Figs. 5(b) and 3(b) also shows a clear increase in frequency dispersion over the entire bias range examined for the longer ambient ex-

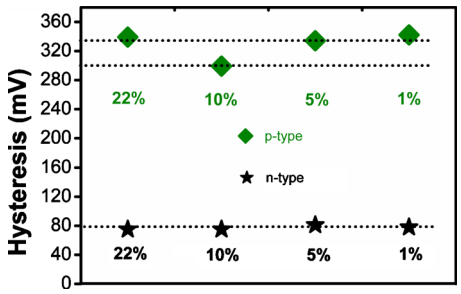


FIG. 4. (Color online) Hysteresis measured around C_{fb} at 100 kHz for all the $(NH_4)_2S$ passivated *n*-type and *p*-type samples examined in this study. The green diamond symbols represent the hysteresis values for the *p*-type devices and the star symbols represent the values for *n*-type devices. The dotted lines are guides for comparative purposes. The hysteresis measurements were performed by sweeping at 100 kHz from negative to positive gate bias for *n*-type devices (−2.0 to 1.5 V), and from positive to negative gate bias for *p*-type devices (1.5 to −2.0 V). There was no hold time in accumulation, and two consecutive sweeps were performed, with hysteresis values obtained from the second sweep.

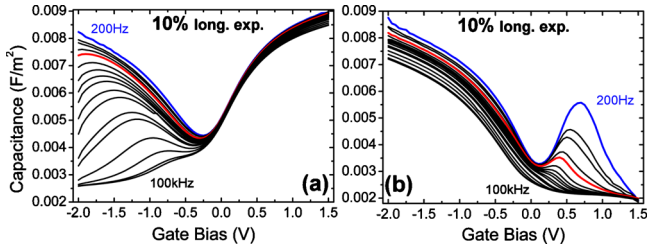


FIG. 5. (Color online) Room temperature C-V frequency variation (200 Hz to 100 kHz) of (a) 10%$(NH_4)_2S$ treated Au/Ni/Al_2O_3/*n*-$In_{0.53}Ga_{0.47}As$/InP, and (b) 10%$(NH_4)_2S$ treated Au/Ni/Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$/InP. In both these cases, the time between removal of the InGaAs sample from the 10%$(NH_4)_2S$ solution to loading to the ALD chamber load lock was increased to ~30 min. The actual diameters of the capacitor devices tested were: 114 μm, and 106 μm, for the *n*-type and *p*-type samples, respectively. The frequencies measured and plotted above are as follows: 200 Hz, 400 Hz, 500 Hz, 800 Hz, 1 kHz, 1.5 kHz, 2.0 kHz, 2.5 kHz, 3.0 kHz, 4 kHz, 5 kHz, 8 kHz, 10 kHz, 20 kHz, 40 kHz, 80 kHz, and 100 kHz. The 1 kHz curves are in red.

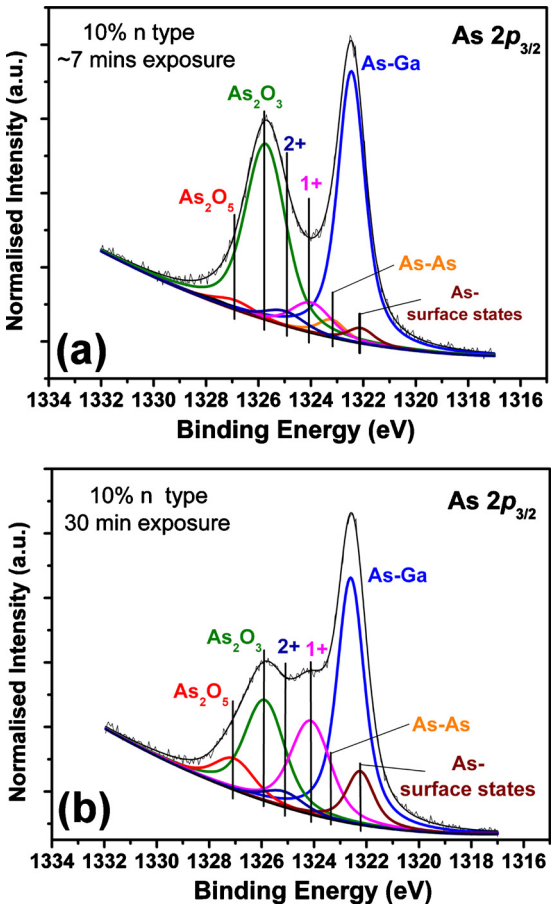


FIG. 6. (Color online) The As $2p$ core level x-ray photoelectron spectra of the (a) 7 min and (b) 30 min ambient exposed 10%$(NH_4)_2S$ n-$In_{0.53}Ga_{0.47}As$ samples. The *in situ* XPS was performed prior to ALD deposition.

posed sample. It is thus clear that extended ambient exposure post-passivation and prior to ALD deposition causes a significant degradation in device electrical properties on both n-type and p-type $In_{0.53}Ga_{0.47}As$.

Prior to ALD deposition, *in situ* XPS was also performed on the 10% passivated n-type samples after 7 and 30 min exposure times to atmosphere. The As $2p$ core level spectra of the 7 min and 30 min exposed n-$In_{0.53}Ga_{0.47}As$ samples are presented in Figs. 6(a) and 6(b), respectively. Peak fits were carried out using AANALYZER software,[29] so that all peaks could be fitted consecutively to provide the highest level of conformality between the spectra, using previously determined fitting parameters.[13,30] Both samples show the presence of As_2O_3, As_2O_5, elemental arsenic (identified as As–As), lower coordinated oxidation states labeled 2+ and 1+, tentatively ascribed to AsO and As_2O, respectively, as well as a peak corresponding to As surface states (dimers and possibly dangling bonds). The XPS results, as expected, show an increase in the total oxide levels for the longer exposed sample, with the most significant being that of the As_2O peak. As the As_2O state has been seen to form preferentially at the interface between the oxide and the substrate,[30] this could be evidence of the growth mechanism of the oxide, with As_2O forming initially, which then over time converts to form the other oxidation states, consistent with the growth of the As_2O_5 peak. It is also observed from the XPS spectra that there is marked increase in the As surface state related spectral feature for the sample exposed for 30 minutes as compared to the sample exposed for 7 minutes. This is potentially significant as a recent study by Robertson[31] identified As dimers as a possible source of interface defects at the oxide/III-V interface as detected previously using *in situ* XPS studies by Milojevic *et al.*[32] These again could be formed as a result of the oxide growth, with the formation of the As_2O causing a disruption of the interface.[33]

In the case of the n-type XPS samples analyzed here, the corresponding electrical characteristics after ALD and gate MOS device formations are seen in Fig. 2(b) for the 7 min exposure sample and Figs. 5(a) for the 30 min exposure sample. As discussed earlier, there is a noticeable increase in the interface defect C-V response at negative gate bias for the longer exposed device. It is possible that the increase in As surface states, as observed by XPS, could be a contributory factor to this. It must be pointed out that correlation of XPS and electrical results is difficult and while these results may provide a suggestion as to the origin of some interface defects responsible for the C-V response, a definitive statement cannot be made as to the real significance of the role of As surface states. The presence of Ga and In surface states are also much more difficult to identify with XPS due to a smaller binding energy separation between the peaks, as well as reduced surface sensitivity due to the lower binding energies involved. It is the case that physical identification of interface defects at the oxide/III-V interface remains one of the most challenging topics in this field, where significantly more analysis in areas such as electron spin resonance would be extremely helpful toward atomic identification of the interface defects.

It has been seen thus far that in terms of overall device electrical performance the 10%$(NH_4)_2S$ passivation is superior on both n-type and p-type $In_{0.53}Ga_{0.47}As$ to that of the other $(NH_4)_2S$ concentrations (1%, 5%, and 22%) examined. This is in agreement with the results of the chemical and physical investigations performed by Brennan *et al.*[13] One possible explanation for this is that the lower $(NH_4)_2S$ concentrations (1% and 5%) provide insufficient protection to the $In_{0.53}Ga_{0.47}As$ surface to prevent significant reoxidation during the 7 min ambient exposure, while the much higher 22% concentration leads to increased surface roughness and consequently a degradation in device performance. It is possible that there is a transition point at a $(NH_4)_2S$ concentration of ~10%, where the passivation is effective in suppressing significant reoxidation without introducing the detrimental effects of higher $In_{0.53}Ga_{0.47}As$ surface roughness. It has also been established at this point that minimizing the ambient exposure time after removal from the $(NH_4)_2S$ solution prior to ALD is critical to device performance. Given that they exhibited the most promising electrical properties within this sample set, a detailed examination of the interface state density and profiles is presented for the n-type and p-type $In_{0.53}Ga_{0.47}As$ devices which had received the 10%$(NH_4)_2S$ treatment with minimal exposure post-passivation. To this end, characterization of the interface state density was performed using two approaches: a

temperature-modified version of the high-low frequency C-V technique; and an approximation to the more traditional conductance method. This provides a useful comparison of these two methods to characterize D_{it} for the oxide/$In_{0.53}Ga_{0.47}As$ system. Moreover, if the peak position and magnitude of the D_{it} obtained with the two methods is comparable, this will provide a higher level of confidence in terms of the D_{it} values obtained, which is important for the high-k/$In_{0.53}Ga_{0.47}As$ system, where the validity of the conventional C-V and G-V approaches remains an issue of discussion. This analysis will focus on the characterization of midgap interface defects, and does not encapsulate defects degenerate with the $In_{0.53}Ga_{0.47}As$ conduction band discussed earlier for n-type $In_{0.53}Ga_{0.47}As$ devices.

The first method used to estimate D_{it} is a temperature-modified version of the "combined high-low frequency C-V method," as discussed in Nicollian and Brews.[34] At low frequency, the interface traps have time to respond to the slowly changing ac signal and therefore add a capacitance to the measured low frequency C-V curve, C_{LF}. In this work C_{LF} was taken at a frequency of 40 Hz and at room temperature (~295 K). In this regard, it is worth emphasizing again the importance of the earlier point about measuring to as low a frequency as possible in order to maximize the interface state response. By contrast, at high frequencies interface defect states cannot respond in any significant way to the ac signal and therefore they contribute little or no capacitance to the high frequency C-V measurement, C_{HF}. In this work, a slight modification to the high-low frequency C-V method is performed in that a high frequency curve at a reduced temperature is chosen where the interface defect response is minimized further, and a more accurate D_{it} can therefore be extracted. Thus, the C_{HF} is taken at 1 MHz and a temperature of 220 K in this work. The capacitance associated with the interface states can be extracted using Eq. (1), and the D_{it} estimation is obtained using Eq. (2). As stated by Nicollian and Brews, one of the advantages of using this method is that minimal assumptions regarding material properties are required, and D_{it} is estimated simply and directly from measured C-V curves without the need for simulation.[34] One significant caveat for employing this method, which is particularly important for narrow band gap materials such as $In_{0.53}Ga_{0.47}As$, is that it will only work effectively where C_{LF} is chosen for a sample where the capacitance associated with the interface state contribution goes through a peak within the gate bias range examined. This is the case for the samples used in this study with the 10%$(NH_4)_2S$ passivation, as can be seen for the 200 Hz curves in Figs. 2(b) and 3(b). For samples with higher D_{it} where the interface defect related response does not pass through a peak at low frequency [e.g., see Fig. 3(a)] the method is not as effective, as it is difficult to distinguish between interface defects and a minority carrier contribution

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}, \tag{1}$$

$$D_{it} = \frac{C_{it}}{q}. \tag{2}$$

The second method used here to estimate D_{it} is the more commonly used approximation to the conductance method.[34,35] The equivalent parallel conductance (G_p/ω) is estimated from the measured conductance (G_m), and measured capacitance (C_m) against voltage sweep, using Eq. (3) below, where ω is the fixed angular frequency, and C_{ox} is the oxide capacitance.[34,35] One issue in particular for $In_{0.53}Ga_{0.47}As$ devices is which value to use for C_{ox} in this characterization. This is not particularly significant for the p-type samples where the accumulation capacitance is very close to the expected C_{ox}. However, it is relevant in the case of the n-type samples where the measured accumulation capacitance (~0.008 F/m^2) is lower than the expected C_{ox}. For these samples, the C_{ox} value should be ~0.0108 F/m^2, using the Al_2O_3 thickness determined by TEM and assuming an Al_2O_3 dielectric constant of k=9, and this calculated C_{ox} as opposed to the measured accumulation capacitance is used in the determination of interface state density for the n-type samples (C_{ox} of 0.0108 F/m^2 is also used in the analysis of the p-type samples). The equivalent parallel conductance, G_p, was converted to peak interface state density using the approximation in Eq. (4), which assumes zero deviation in surface potential band bending, and where q is the electronic charge

$$\left(\frac{G_p}{\omega}\right) = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}, \tag{3}$$

$$D_{it} = \left(\frac{G_p}{\omega}\right) \times \left(\frac{1}{0.4 \times q}\right). \tag{4}$$

The D_{it} profiles versus gate bias are shown for 10% passivated devices on n-type and p-type $In_{0.53}Ga_{0.47}As$ in Figs. 7(a) and 7(b), respectively. First with regard to Fig. 7(a) it is obvious that there is good agreement between the D_{it} estimated from the temperature modified high-low method and the approximation to the conductance method. The magnitude of the D_{it} is higher in the case of the conductance-based technique, while the position and profile of the peaks are very similar. In the case of the p-type devices in Fig. 7(b), there is again close agreement in terms of the peak profile while the magnitude is also a little higher for the conductance-based technique. This provides strong evidence that both of these methods are valid routes to extracting D_{it} for structures incorporating a high-k oxide layer on $In_{0.53}Ga_{0.47}As$, provided appropriate caution is used in their application. The fact that both methods employed here make minimal assumptions regarding material properties (only assumption being k=9 for Al_2O_3 to calculate C_{ox}) and the profiles are simply extracted from actual electrical measurements gives further confidence that the profiles presented are truly representative of the device behavior. It is also a significant result that the peak magnitude and position of the extracted D_{it} using the conductance method, which utilizes both measured capacitance and extracted parallel conductance data, yields very similar results to the D_{it} extracted

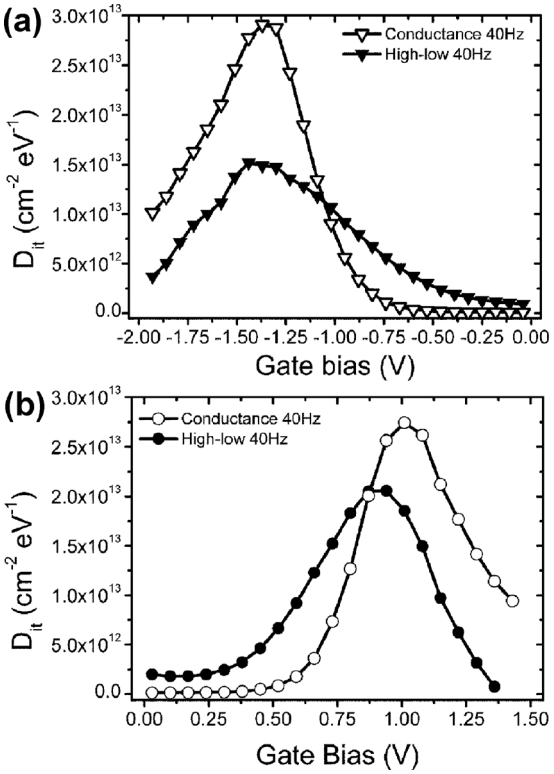


FIG. 7. D_{it} profiles vs gate bias extracted from the high-low frequency C-V method, and the conductance method, for 10%$(NH_4)_2S$ passivated devices on (a) *n*-type and (b) *p*-type $In_{0.53}Ga_{0.47}As$ devices. It is seen that there is good agreement between the conductance and high-low methods in determining the peak profile and magnitude.

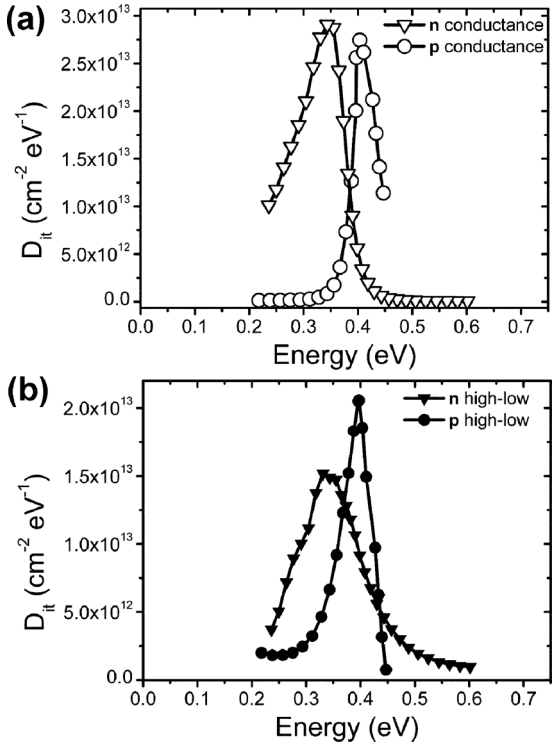


FIG. 8. Interface state density profiles for 10%$(NH_4)_2S$ passivated *n*-type and *p*-type devices extracted using (a) the conductance method, and (b) the high-low method, and plotted vs $In_{0.53}Ga_{0.47}As$ band gap energy.

independently using the high-low frequency C-V method, which uses only measured capacitance data. This provides evidence to support that the extraction of D_{it} using the conductance method is valid for high-*k* on $In_{0.53}Ga_{0.47}As$.

Given that D_{it} profiles versus gate bias have thus far been obtained using two independent approaches, the high-low frequency C-V method and the conductance method, it follows that a natural extension of this analysis is obtain the D_{it} profile versus the $In_{0.53}Ga_{0.47}As$ energy gap. Recent studies in the literature employed alternative methods to those used in the present work in order to determine D_{it} versus energy profiles for high-k/$In_{0.53}Ga_{0.47}As$ system. Brammertz *et al.*[12] used an admittance spectroscopy technique, while Ali *et al.*[36] employed an equivalent circuit model. In the case of Ali *et al.* the peak D_{it} was estimated at an energy of approximately $E_v+0.4$ eV, while in both works the reported peak D_{it} magnitudes were in the range 7×10^{12} cm^{-2} eV^{-1} to 5×10^{13} cm^{-2} eV^{-1}. In the case of the samples in the present work, if we consider that at high frequency (1 MHz) and low temperature (~220 K) that the interface state contribution is negligible, then it follows that the measured capacitance is comprised of the semiconductor capacitance, C_s, in series with the oxide capacitance, C_{ox}. Therefore, it is possible to calculate the semiconductor depletion width and hence the semiconductor potential. This in turn allows the calculation of a corresponding energy position for the D_{it} profiles plotted versus gate bias in Figs. 7(a) and 7(b).[34] Using the procedure described above the D_{it} profiles versus $In_{0.53}Ga_{0.47}As$ band gap energy are plotted in Figs. 8(a) and 8(b) [Note: the measured minimum capacitance at high frequency, 1 MHz, and low temperature, −50 °C, was used to obtain more accurate doping concentrations, yielding $\sim2.9\times10^{17}$ cm^{-3} for the 10% *n*-type sample, and $\sim3.6\times10^{17}$ cm^{-3} for the 10% *p*-type sample. These values are very close to the nominal doping of 4.0×10^{17} cm^{-3} and within the expected doping error range, and the actual measured doping values were used in the analysis for these samples to provide greater accuracy in the extraction of the D_{it} profiles. High frequency and low temperature was used in order to minimize any contribution of interface states to the measured minimum capacitance. It is also noted that employing these doping concentrations V_{fb} (@ 100 kHz) values of 0.40 V, and −0.62 V, were obtained for the 10% *n*-type and 10% *p*-type samples respectively]. Table I summarizes the energy positions of the peak D_{it} with respect to the valence band edge, and the integrated D_{it} values were obtained by integrating over the range $E_v+\sim0.2$ eV to $E_v+\sim0.65$ eV for *n*-type and *p*-type devices. It is seen in comparing Figs. 8(a) and 8(b) that there is good agreement between the conductance method and high-

TABLE I. Summary of the integrated D_{it} values obtained by integrating over the range $E_v+\sim0.2$ eV to $E_v+\sim0.65$ eV, and also the energy positions of peak D_{it} with respect to the valence band edge, for *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ devices.

	Integrated D_{it} (cm^{-2})		Defect energy (eV)	
	n -type	*p* -type	n-type	p-type
High-low	2.4×10^{12}	1.6×10^{12}	Ev+0.34	Ev+0.40
Conductance	3.4×10^{12}	1.6×10^{12}	Ev+0.34	Ev+0.40

low frequency C-V method in terms of the extracted peak profiles and magnitudes. The conductance method and high-low method yield identical values for the peak D_{it} energy position over *n*-type (E_v+0.34 eV), and over *p*-type (E_v +0.40 eV). While there is a slight difference in the peak energy position when comparing *n*-type and *p*-type, it is possible that it is within expected experimental error for this type of characterization. It has been reported that in estimating the energy position for defects on Si-based devices that the error in the peak position can be of the order of ±0.05 eV.[37] It is seen in Fig. 8(a) and in Table I that the D_{it} magnitude extracted using the conductance method is almost identical for *n*-type and *p*-type devices. The similarity in D_{it} magnitude over *n*-type and *p*-type is also evident for D_{it} extracted from the high-low frequency C-V method, see Fig. 8(b) and Table I. Given the similarity in the magnitude of the integrated D_{it}, as well as the proximity of the estimated peak positions, it is likely that the same defect is being observed over *n*-type and *p*-type devices for the samples investigated in this work. Assuming that it is indeed the same defect these results indicate it has an integrated D_{it} of $\sim 2.5 \times 10^{12}$ cm^{-2} ($\pm 1 \times 10^{12}$ cm^{-2}), positioned in the middle of the InGaAs band gap, at approximately 0.37 eV (±0.03 eV) from the valence band edge.

IV. CONCLUSIONS

In this investigation into the effectiveness of varying ammonium sulphide $(NH_4)_2S$ concentrations (from 1% to 22%) in the passivation of *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$, multi-frequency C-V results indicated that the lowest frequency dispersion over the bias range examined occurs for *n*-type and *p*-type devices treated in 10%$(NH_4)_2S$ solution. It has also been shown that there is a deleterious effect on device behavior for increased ambient exposure time after removal from 10%$(NH_4)_2S$ solution and that XPS analysis has detected changes in the composition of the regrown oxide on this timescale. Estimations of interface state density, D_{it}, extracted from an approximation to the conductance method, and independently from the temperature-modified high-low frequency C-V method, show very good agreement both in terms of magnitude and characteristic peak profile for the optimum 10%$(NH_4)_2S$ passivated $In_{0.53}Ga_{0.47}As$ devices. This indicates that the conductance method can be applied to devices incorporating high-*k* oxides on $In_{0.53}Ga_{0.47}As$. Results suggest that the same defect is observed over these *n*-type and *p*-type devices having an integrated D_{it} of $\sim 2.5 \times 10^{12}$ cm^{-2} ($\pm 1 \times 10^{12}$ cm^{-2}), positioned in the middle of the $In_{0.53}Ga_{0.47}As$ band gap, with the peak density approximately 0.37 eV (±0.03 eV) from the valence band edge.

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