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JSS Focus Issue on Thermoelectric Materials & Devices

# Scientific and Technical Challenges in Thermal Transport and Thermoelectric Materials and Devices

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This paper considers the state-of-the-art and open scientific and technological questions in thermoelectric materials and devices, from phonon engineering and scattering methods, to new and complex materials and their thermoelectric behavior. The paper also describes recent approaches to create structural and compositional material systems designed to enhance the thermoelectric figure of merit and power factors. We also summarize and contextualize recent advances in the use of superlattice structures and porosity or roughness to influence phonon scattering mechanisms and detail some advances in integrated thermoelectric materials for generators and coolers for thermally stable photonic devices.

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Controlling heat transport, dissipation and its conversion to other forms of energy are major research drivers for both materials researchers and device/product specialists alike.[1,2] In parallel, nanoscale materials developments have provided insight and evidence for unusual and sometimes scalable phonon scattering phenomena to cause significant thermal conductivity suppression, often while maintaining electron conductivity in materials where electron specific heat contributions and other effects are controlled, such that relatively high thermoelectric figures of merit ($ZT$) can be obtained. The figure of merit $ZT = S^2\sigma T/\kappa$, where $S = -\Delta V/\Delta T$ is the Seebeck coefficient ($\Delta V$ is the voltage difference caused by a temperature difference $\Delta T$), $\sigma$ is the electrical conductivity and $\kappa$ is the thermal conductivity. Research and development in chip- or system-level cooling continuously provides the impetus for many of these developments, from semiconductor material cooling within a high clock-speed chip, to system level cooling of processors and data-farm thermal management.

In tandem with thermal conductivity and transport control in materials and modules, is the necessity for understanding how material size, composition, structure and arrangement can alter phonon and heat transport, so that other research questions and technological advancements can be tackled. For instance, the required local (electrical) heating for phase change materials and memristors depends on thermal transport, heat dissipation and cooling to set the resistance memory or switching behavior. Annealing, sintering, and a host of other thermal treatments can influence and modify the physical properties of nanomaterial assemblies and thin films. The control and exploitation of these effects requires accurate measurement and interpretation of thermal transport to describe the important changes to composition, structure and arrangement caused at elevated temperature. There are many more cases where a more detailed understanding of heating and cooling for reasons other than power generation or thermoelectric control are important. In many cases, the experimental measurements are state-of-the-art and the modifications to the nature of the materials can often be very complex.[3] We summarize some of the main advancements in material modification that specifically cause changes to thermal and electrical behavior, to maximize the Seebeck coefficient and especially $ZT$. For a detailed overview of nanoscale thermal transport, we refer the reader to two important reviews from Cahill et al.[4,5] For brevity in this paper only, the references in those articles give a comprehensive account of the development in the field.

For on-chip level high processing power computing and large scale data farms, controlling heat dissipation is critical. Photonic systems are also susceptible to thermal fluctuations. In semiconductor-based light emitters, the emission (intensity, frequency, etc.) are affected by thermal fluctuations within the semiconducting media. The limit in clock-speed in the last few years was in part due to module power densities exceeding 10 W cm$^{-2}$, which would then require liquid cooling as opposed to fan-based air circulation - hence the evolution of multicore processors at similar power input. This approach produced unforeseen hotspots, with an order of magnitude jump in power density above the threshold that would ordinarily require liquid cooling. Prasher, Venkatsubramanian and colleagues[6] applied Peltier thermoelectrics to solve hot spot cooling in very small modules and chips, but integration and packing still remain challenging. This is especially true in photonics where the local heat fundamentally affects the performance and stability of the light emitter. Here, we summarize perspectives and approaches currently being taken to solve this particular issue.

## Effects Contributing Specifically to $ZT$ Enhancement

The pursuit of improving the thermoelectric figure of merit, $ZT$, of materials, the key performance indicator for transforming thermal energy into electric energy and vice versa, has been an endeavor for decades.[7] To address the challenge, scientists were eager to break the compromise between thermal and electrical properties via developing or indeed, nanostructuring, a wide range of materials that were intrinsically promising.

Bulk complex materials developed by alloying elements, usually try to interweave phonon-glass-like poor thermal transport with electron-crystal-like rich electron transport, the so-called phonon-

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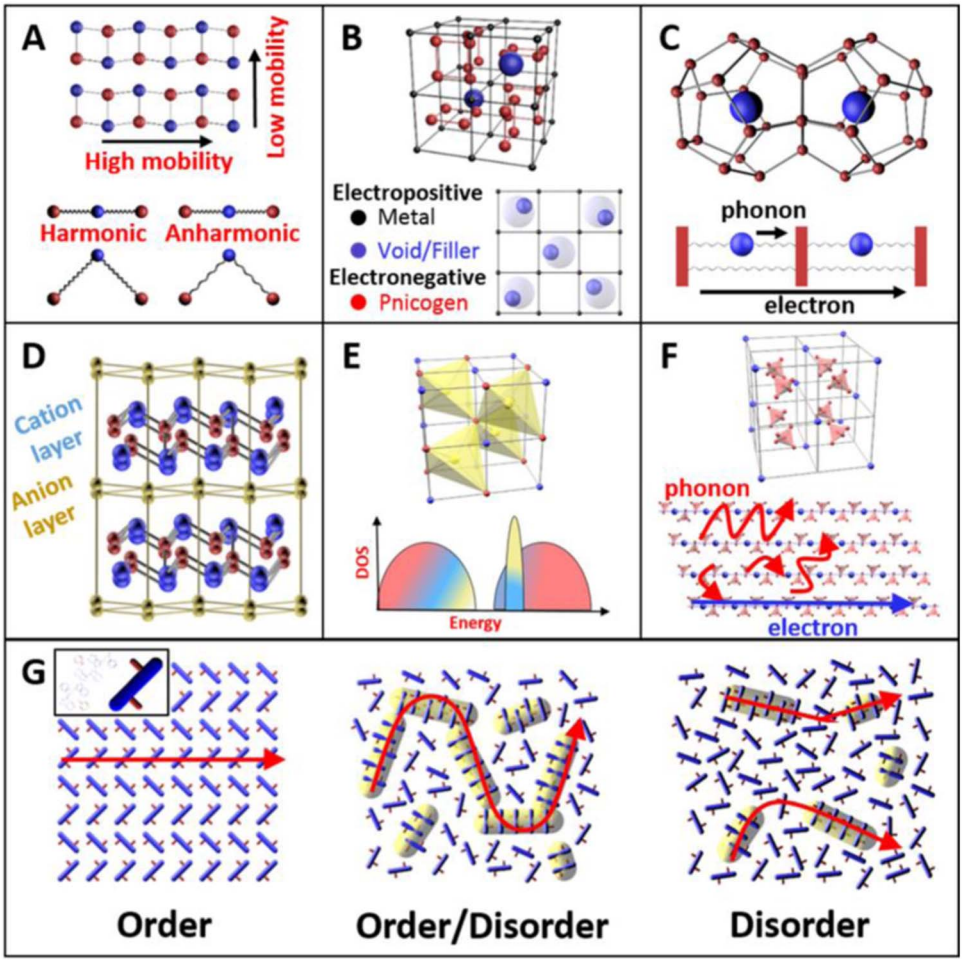



**Figure 1.** The materials for improving the thermoelectric figure of merit *ZT*: (A) chalcogenides,[10] (B) skutterudites,[11] (C) clathrates,[12] (D) Zintl phases,[13] (E) half-Heusler compounds,[14] (F) phonon-liquid electron-crystal,[8] and (G) OTE material with regions showing order, order/disorder and disorder between molecules.[15]

glass electron-crystal (PGEC) idea, to achieve a high *ZT*.[3] These concepts are represented in Fig. 1, showing for example, (*i*) chalcogenides offer anharmonic and anisotropic bonding to block phonons and to transmit electrons, (*ii*) skutterudites comprise elements with low electronegativity differences to enable high carrier mobility and to generate strong scattering against lattice phonon propagation, (*iii*) clathrates allocate metal atoms within coordinated cages to scatter phonons but not electrons, (*iv*) Zintl phases contain ionically and covalently bonded atoms to simultaneously reduce thermal conductivity and enable high carrier mobility, and (*v*) Half-Heusler compounds combine narrow band-gap and sharp density of electronic states (DOS) to enhance the power factor. An alternative to PGEC is the phonon-liquid electron-crystal, where sub-stoichiometric $Cu_{2-x}Se$ serves a matrix of ordered Se atoms as crystalline pathways for carriers and disordered Cu ions as scatter centers for phonons, thus achieving low lattice thermal conductivity and high electrical conductivity.[8]

It is also worth noting that solution-processed organic thermoelectric (OTE) materials formed by polycrystalline domains within disordered structures offer a new framework for manipulating *ZT*.[9]

In particular, properly aligned polycrystalline domains can result in enhanced charge-carrier transport, while disordered structures can result in highly anisotropic heat-carrier transport, thus leading to *ZT* comparable to inorganic materials at room temperature. Without the constraints of lattice-matching to create graded materials, the flexibility of hybridizing organic-inorganic nanocomposites to tailor material composition, could enable the transition from 'efficiency-driven' to 'deployment-driven' thermoelectric material designs. Additionally, the possibility of using low-cost solution processes to print and create device architectures on a large-scale and as flexible modular devices augers well for energy harvesting of waste heat in wearable technologies. This transition expands the applicability of OTEs to cover a new wide range of applications such as large array wireless sensor network for agricultural applications, body-energy harvesters, sensors or heaters for wearable electronics, and DNA cyclers or cooling bags for biomedical applications.

## Power Factor Enhancement

While the vast majority of studies in thermoelectrics have been focused on reducing lattice thermal conductivity using nano- or complex structures, it is increasingly evident that improving the power factor ($S^2\sigma$) is also feasible and perhaps even indispensable to ultimately achieve much higher *ZT*. One of the first approaches to improve the power factor has been focused on the quantum confinement effect, proposed in the landmark papers by Hicks and Dresselhaus in 1993.[16,17] This is due to a sharp and asymmetric density of state (DOS) near the Fermi level ($E_F$) in low-dimensional materials (Fig. 2a), such as quantum dots, quantum wires, and quantum wells. However, experimental demonstration of high power factor in quantum structures has been challenging, in part because the structures have to be exceedingly small to possess the quantum effect (at least around room temperature). Also, $E_F$ has to be located at the right position to yield both high *S* and power factor.[16–18] Nevertheless, power factor enhancement has

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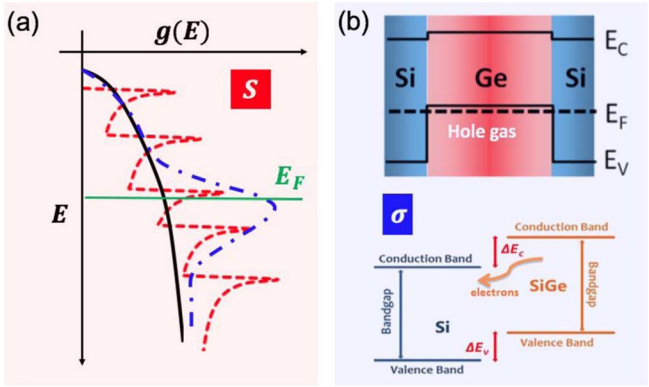



**Figure 2.** Strategies to enhance the power factor ($S^2\sigma$). (a) A highly asymmetric density of state ($g(E)$) around the Fermi energy ($E_F$) can lead to $S$ values higher than the bulk case (solid line). Strategies include using the quantum confinement effect to introduce discrete $g(E)$ (dashed line)[16,17] and introducing a resonant level (dash-dot line) via doping.[25] (b) Enhanced mobility ($E_F$) and electrical conductivity (σ) via modulation doping in Ge-Si core-shell nanowires[26] (top) and SiGe-Si nanocomposite[27] (bottom). (b) Reprinted with permission from Refs. 26 and 27.

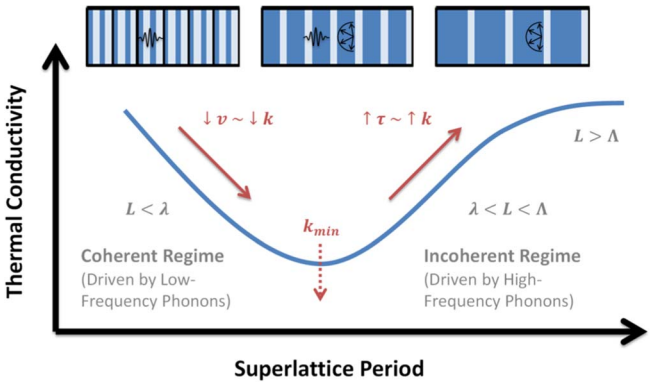



**Figure 3.** Thermal conductivity as a function of superlattice period. When the superlattice period ($L$) is smaller than the phonon wavelength (λ), an increase in the superlattice period leads to a decrease in the group velocity ($v$), which reduces the thermal conductivity ($k$). Where the superlattice period is greater than the phonon wavelength, an increase in the superlattice period leads to an increase in the relaxation time (τ), which increases the thermal conductivity until the superlattice period becomes comparable to the phonon mean free path (Λ). The interplay of coherent scattering by low-frequency phonons and incoherent scattering by high-frequency phonons leads to the minimum thermal conductivity ($k_{min}$), which can be further reduced below the amorphous limit by maximizing the mass mismatch or by invoking phonon localization via randomly distributed quantum dots or a random multilayer structure.

been observed in $Si/Si_{1-x}Ge_x$[19] and $PbTe/Pb_{1-x}Eu_xTe$[20] quantum well superlattices. In a two-dimensional electron gas in $SrTi_{0.8}Ni_{0.2}O_3$, a five-fold enhancement in $S$ over the bulk value was observed.[21]

There are also several other strategies that have shown tremendous promise in improving the power factor. One approach is to explore novel band structures in semiconductors, either by engineering the effective mass ($m^*$) or increasing the degeneracy of the bands. As an example, Pei et al. showed enhanced $S$ and power factor in Na-doped PbTe due to lighter effective hole mass.[22] Pei et al. also achieved high $ZT$ via the convergence of multiple valleys in doped $PbTe_{1-x}Se_x$ alloys.[23] Another strategy is to introduce a resonance in $g(E)$ at the $E_F$ to increase the value of $S$ and the power factor, over the bulk values. Mahan and Sofo[24] showed that a δ-function-like transport distribution would maximize the power factor and $ZT$.

In reality, 'a Lorentizan of very narrow width' would most closely resemble the δ-function, as in the case of $f$-level electronic states in $YbAl_3$.[24] Another notable example is through 'resonant doping' (Fig. 2a), which has been demonstrated in Tl-doped PbTe[28] and In-doped SnTe,[29] and has been reviewed by Heremans et al.[25] Similarly, in InAs nanowires (with 50-70 nm diameter), Wu et al.[30] observed a large power factor below 20 K, which was attributed to the quantum-dot-like states presented in the non-uniform nanowires.

In addition to large $S$, proper interfacial engineering could also lead to high carrier mobility (μ) for enhanced power factor. This is due to the formation of accumulated free carriers confined in the space charge regime (i.e., 2D or 1D electron or hole gas), in which a strong ionized impurity scattering is absent. By using Ge-Si core-shell nanowires, Moon et al.[26] utilized hole gas confined at interface between the nominally un-doped Ge core and doped Si shell to achieve enhanced mobility μ (Fig. 2b). Along with the bulk-like Seebeck coefficient in the nanowires with diameter down to ~11 nm, they showed a higher maximum power factor compared to optimal bulk Ge. Higher carrier mobility has also been achieved in bulk thermoelectric nanocomposites by 3D modulation doping, in which the dopants are only located in one type of two specific nanograins while the conduction in the other grain type is achieved through charge carrier spill-over from the doped grains (Fig. 2b), leading to higher $S^2\sigma$[31] and $ZT$[27] compared to the case of uniform doping.

The examples discussed above highlight the feasibility of substantially enhancing the power factor through various strategies. By combining these routes with the lattice thermal conductivity reduction approaches, it is entirely plausible to achieve higher thermoelectric figure of merit $ZT$.

## Pushing the Lower Limit of Thermal Transport Using Superlattices

Due to exceptional capabilities of controlling material parameters and dimensions, superlattices have served as a model system to address fundamental questions regarding thermal transport mechanisms. In particular, the role of phonon coherence and the unique size dependence (Fig. 3) have attracted much attention in the recent literature.[32,33] In the coherent regime, where the superlattice period ($L$) is smaller than the phonon wavelength (λ), or the phonon coherence length, an increase in the superlattice period leads to less phonon tunneling and a decrease in the group velocity ($v$), which reduces the thermal conductivity ($k$). In the incoherent regime, where the superlattice period is greater than the phonon wavelength, an increase in the superlattice period leads to less interfacial scattering and an increase in the relaxation time (τ), which increases the thermal conductivity until the superlattice period becomes comparable to the phonon mean free path (Λ). The interplay of coherent and incoherent phenomena results in the minimum thermal conductivity ($k_{min}$), which can be a critical target for designing thermoelectric materials. Recent studies suggest a further reduction of the minimum thermal conductivity of superlattices is possible beyond the random alloy limit or the amorphous limit by modulating the mass mismatch[34] and atomic interactions of constituent materials, introducing random scattering sites such as quantum dots[35] and interfacial disorder, or using a random multilayer structure.[36] These strategies are designed to stop the propagation of phonons over a broad spectrum and invoke phonon localization. The superlattices with controlled material parameters and dimensions provide novel pathways of pushing the lower limit of thermal transport and advancing breakthroughs in thermoelectric applications.

## The Curious Case of Rough Silicon Nanowires

The attractiveness of silicon for thermoelectric materials is partly the same for all its uses. It is an earth-abundant inorganic material, well-established the microelectronics industry, based on useful electronic and optical properties and the method of growth and crystal quality. Si has a high thermal conductivity (~150 W $m^{-1}$ $K^{-1}$) and so has not been used for thermoelectric devices. Si nanostructures, especially rough edged nanowires, have shown significant suppression of the thermal conductivity, even below the Casimir limit without

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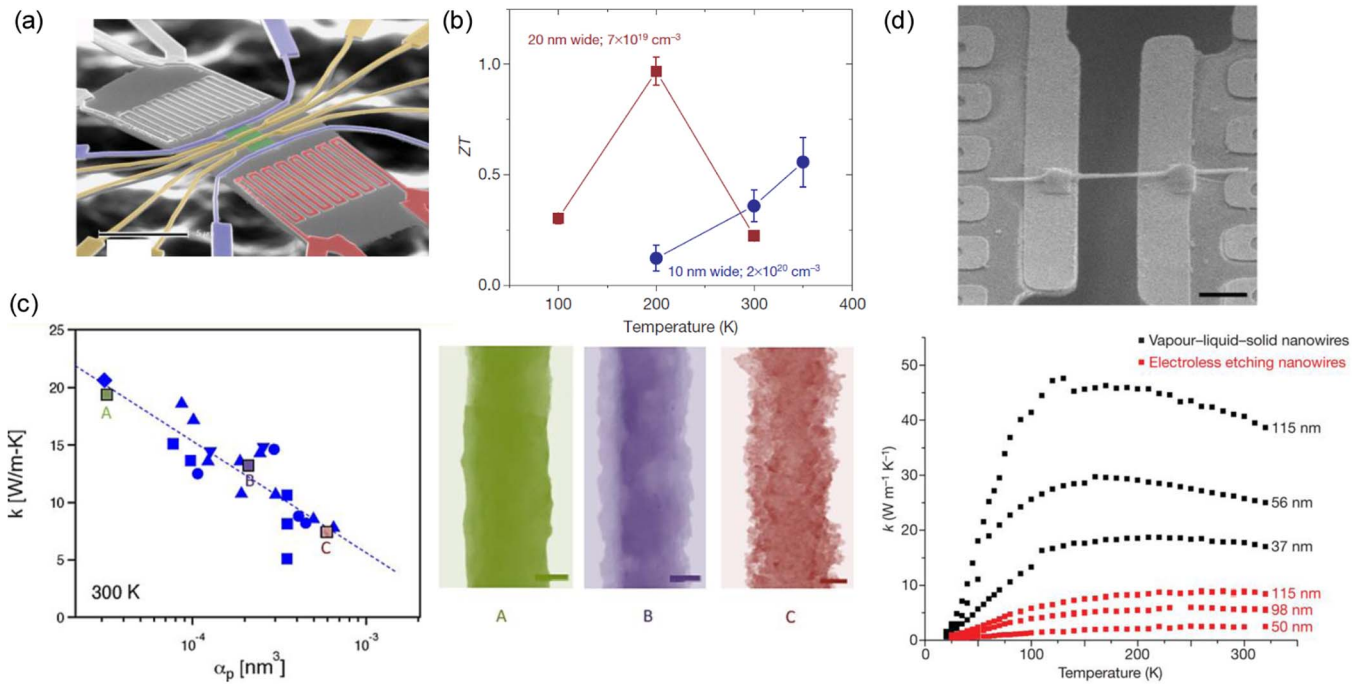



**Figure 4.** (a) False-color image of a suspended platform shows the central green area of the Si nanowire array and electrodes used to quantify the temperature difference across the nanowire array. Joule heating and four-point probe electrical conductivity measurements. Reproduced from Ref. 40 with permission from Nature Publishing Group, 2008. (b) Temperature dependence of *ZT* for two different groups of nanowires with different cross-sectional area and p-doping levels The 20-nm-wide and 10-nm-wide nanowires have a thermopower that is dominated by phonon contributions, and electronic contributions, respectively. (c) Thermal conductivity as a function of $\alpha_p$ (a parameter the author use to captures the roughness structure over the relevant phonon scattering band) at 300 K, respectively. As $\alpha_p$ increases, the wires are rougher, with wavelengths in the 1−100 nm range and the thermal conductivity drops significantly. Reproduced from Ref. 44 with permission from the American Chemical Society, 2012. (d) An SEM image of a Pt-bonded EE Si nanowire (taken at 52° tilt angle). The Pt thin film loops near both ends of the bridging wire are part of the resistive heating and sensing coils on opposite suspended membranes. Scale bar, 2 μm. The temperature-dependent κ of VLS (black squares; reproduced from Ref. 46) and EE nanowires (red squares). The peak κ of the VLS nanowires is 175–200 K, while that of the EE nanowires is above 250 K. The data in this graph are from EE nanowires synthesized from low-doped wafers. Reproduce from Ref. 41 with permission from Nature Publishing Group, 2008.

adverse effect on the electrical conductivity (at least within a single NW compared to an array or film of NWs).

Si NWs that exhibit unusually low thermal conductivity are typically relieved from bulk Si wafers by metal-assisted chemical etching.[37–39] This etching mechanism has a rate that is defined by the semiconductor-solution interface bias, doping type and concentration, and relieves either mesoporous NWs or the more common rough NWs. The thermal conductivity reduction seems to be robust, seen in many separate investigations, but the mechanisms of the suppression has been described as 'controversial'. Some papers report an interplay between the physics of phononic waves and the band of correlated wavelengths of roughness features on the outer surface, causing enhanced phonon scattering. Briefly, researchers have spent considerable time to understand why the thermal conductivity (lattice contribution of Si) can be suppressed by nearly two orders of magnitude to 1.6 W m$^{-1}$ K$^{-1}$[40,41] very close to the amorphous limit for Si (1 W m$^{-1}$ K$^{-1}$) - a crystalline NW can behave like a phonon glass (Fig. 4). Importantly, this thermal conductivity reduction occurs while the electrical conductivity is maintained. However, some comments are appropriate for this observation. The mean free paths for electrons are significantly shorter than for phonons. Second, rough Si NWs must retain a solid crystalline core to avoid porosity or defect-induced increase in resistivity. For etching of bulk wafers, rough NW are most common from p-type Si, where electrons are minority carriers. A narrow range of low-doped n-type wafers can provide sufficient hole ($h^+$) concentration at the semiconductor surface to promote fast etching and the relief of the rough surface. In other words, the *ZT* values from rough Si NW may be tuned or improved further by controlling doping concentration and type to maintain electronic conductivity while minimizing electron specific heat and contribution to thermal conductivity. Then, by controlling surface roughness to screen phonons in a manner that minimizes efficient heat conduction by phonon transport, an optimum thermoelectric response from Si NWs may be achieved. Readers are referred to several publications[5,40–45] where the roughness characterization and parameters are correlated and ascribed to phonon scattering mechanisms invoked to explain thermal conductivity suppression below the Casimir limit in crystalline Si.

Among all detailed studies on rough Si NWs, from roughness wavelength influence to phonon boundary scattering mechanisms and NW diameter effect etc., most measurements have been close to room temperature, or with temperature difference sufficient to test the influence of the NW roughness on thermal conductivity via Seebeck determination or thermal diffusivity. The thermoelectric characteristics of Si NWs at high temperature were, until now, not available and in part because of experimental considerations such as convective or radiative heat dissipation. Additionally, Umklapp scattering, high-frequency modes and optical phonons, and multiphonon processes[47,48] are often characteristic of silicon at high temperature, and have not been assessed in many of the thermoelectric reports of rough Si NWs. The involvement of these processes at or within the 'active' rough surface of a NW is as yet undefined or examined in detail - questions remain as to how these effect manifest in phonon transport or scattering effects that cause significant thermal conductivity reduction. There have only been investigated in recent reports, one up to 700 K[49] where the thermal conductivity was measured directly and optical phonon contribution determined by calculation, and another where Raman scattering was used to confirm optical phonon activity and lower group velocity multiphonon processes in rough Si NWs up to 1173 K, during heating and cooling.[50] In time, we believe the true convergent mechanisms that underpin the reason for conductivity

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suppression will be found, and once route maybe to increase this roughness, inside the NW as well as on the surface, to test the temperature dependent characteristics of phonon scattering in such NWs, without a solid crystalline core and with phonon scattering and confinement possible in all crystallographic directions. Surface undulations in these systems may provide a general route for other semiconducting thermoelectric materials as a way of suppressing thermal conductivity by enhancing phonon scattering by means other than size or dimensional reduction, particularly if the material is mono-elemental or simple in composition compared to other exotic thermoelectric compounds.

### Thermoelectric Devices for Near Room Temperature Applications

A thermoelectric device can be used either as a generator (TEG) to scavenge waste heat into usable electricity or as a thermoelectric cooler (TEC) for the thermal management of a heat generating device. For wider applications of these devices the fabrication technique for volume production has to be adopted. Traditional discrete devices are large and expensive. Cast slugs of thermoelectric material are used during fabrication limiting the number of thermocouple pairs available and resulting in low output voltages. These materials have low thermal resistances and low reliability. Efficiency and power density for discrete TE energy harvesters are not economically viable and parasitic heat loss is also an issue. The processing required to generate the long, vertical TE legs is complex, involving several steps including powder synthesis, alloying, sintering, dicing, interconnect and braze, and module assembly. Additionally, yield and system integration pose significant difficulties. Use of thin film thermoelectrics to build micro-thermoelectric generator (μTEG) are being explored as an alternative to discrete energy harvesters. They have advantages in terms of processing, scaling and cost. However, current thin film devices still rely on thick films of $Bi_2Te_3$ (40 μm) and on expensive device assembly processes.

One option may be to electroplate thermoelectric (TE) materials, which offers several advantages compared to the conventional methods for volume production. Several approaches have been explored to fabricate a TE device using electroplating. A μTEG can be classified depending on its design specifications, in particular to heat flow (in-plane or cross-plane) through the device and the layout of the thermocouple (laterally or vertically).

Figure 5 shows the schematic diagrams,[51] explaining the different types of TEG devices, namely, lateral/lateral type; vertical/lateral type and vertical/vertical type. Among all the three types, the vertical/vertical type of setup has proved to be comparatively more advantageous. In a vertical setup, higher packaging densities of the material can be achieved. The main advantages of a cross-plane setup are, low-electrical resistance, no parasitic heat flow through the substrate, improved thermal contact and the possibility of higher integration densities and output power. The state-of-art devices are primarily cross-plane devices (vertical/vertical type).

The first TE electroplated micro device fabrication was carried out by Jet Propulsion Laboratories (JPL) in 1998. To date, there have been several combinations and complex fabrication techniques that have been used to decrease the limitations and improve the performance of the device. Wojtas et al. developed a device with a module ZT of 0.1, delivering a power output of 126.3 mW $cm^{-3}$ by maintaining a temperature difference of 95 K.[52] This integration not only increased the net power but also decreased the TE leg size, which aids in reduced relevance of thermal conductivity in TE material with decreased contact resistance.

A flip chip bonded μTEG was developed by Roth et al. by using n-type $Bi_2Te_3$ and p-type $Sb_2Te_3$ TE legs, which were pulse plated with an average height of 10 μm.[53] The whole system was annealed for 100 h at 250°C in tellurium atmosphere, which is industrially not feasible. However, the measured output power of the system was 166 μW at a temperature difference of 46 K. In 2014, Jung et al. fabricated a Bi-Te based TEG by tuning the atomic ratio of Bi in the electroplated

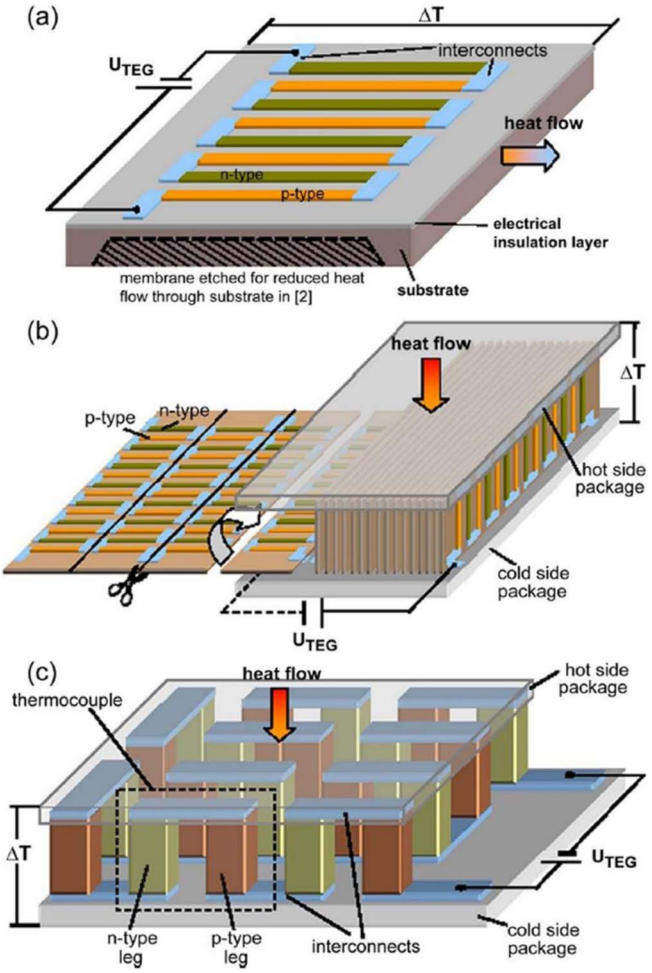



**Figure 5.** Different designs of micro-TEG a) lateral/lateral type; b) vertical/later type c) vertical/vertical type.

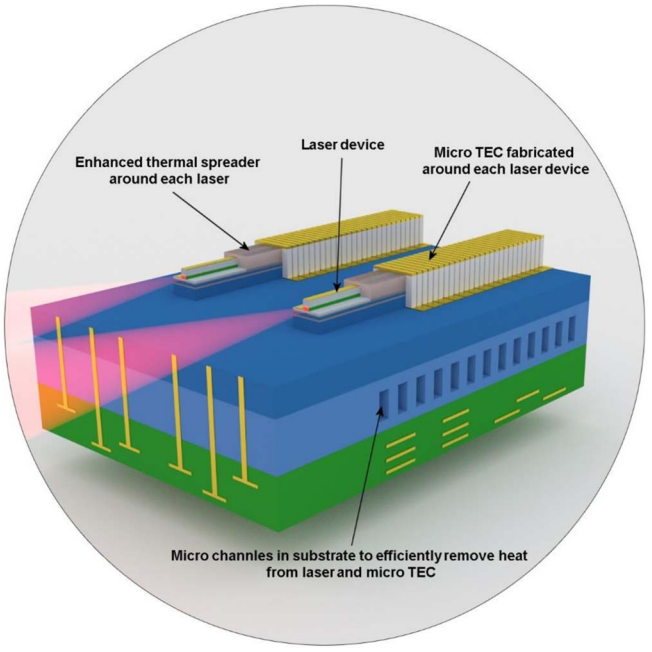



**Figure 6.** High-level schematic of the thermally integrated photonics system (TIPS) architecture. Note that the image shown here focuses on the thermal solution around the heat-generating device (laser) and does not show the overall package design.[54]

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film with addition of ethylene glycol (EG) in the electrolyte (for n-type 0% EG and for p-type 30% v/v EG). The power generated from a p-n leg pair was 24.36 nW at a temperature difference of 10 K. It is expected that with this module an output power of 2.39 μW $cm^{-2}$ can be generated. The major reason for a low power output was the high contact resistance, which is always a priority consideration for integrated, direct electrically contacted thermoelectric materials, generators and coolers.

### Thermally Integrated Thermoelectric Cooling for Photonics

One of the applications for thermoelectric coolers is to remove heat from optoelectronic devices (lasers, modulators, amplifiers), which generate extremely high heat flux levels (∼1 kW $cm^{-2}$) but have stringent requirements, where the temperature control should have a precision better than ±0.1°C. Current state-of-the-art photonic integrated circuits (PICs) employ macro TEC where the optoelectronic devices are placed on top of a large thermoelectric cooler. These devices are cooled down below room temperature and then small heaters near the vicinity of these devices are used to fine tune the operating temperature of individual devices to maintain consistent and precise emission wavelengths. This method is energy inefficient and will not be able to meet the ever-growing (40-80× by 2020) data traffic challenge, which requires high-density integration of optoelectronic devices.

Therefore, there is a genuine requirement to develop an efficient heat spreader to reduce the high heat flux (∼1 kW $cm^{-2}$) to a more manageable level (0.1 kW $cm^{-2}$), which can be accepted by a micro-thermoelectric coolers (μTEC, Fig. 6) that can be fabricated directly around the optoelectronic devices. The vision is to integrate AlN heat spreaders, μTEC and micro-fluidics (μFluidics) with optoelectronic devices in order to precisely and autonomously control individual device temperature and thus, device performance, in terms of wavelength and optical output power, to enable system-on-a-chip integration.[54] In terms of thermoelectric coolers, materials with high thermoelectric efficiency near room temperature (e.g., $Bi_2Te_3$-based composites), which can be developed directly on wafers and compatible with semiconductor fabrication process and do not require complicated and long processing time, are desirable. Electroplating of these materials directly at wafer scale is way forward in realizing this vision of μTEC in the application of thermal management of photonic devices.

### Summary and Outlook

There are theoretical grounds for some optimism that materials with $ZT > 3$ will be more common, but values $> 1$ at reasonably low temperatures are available but not commonplace yet. Fundamentally, there are many new material systems in which additional phonon scattering mechanisms contribute to those already designed by composition, structure or deposition arrangement that can reduce thermal conductivity significantly. The cause of beneficial phonon scattering can stem from less defined surface features such as roughness or impurities, as well as well-defined structure such as crystalline superlattices. A superposition of several material parameters may be possible for semiconducting compounds and materials that includes surface or boundary scattering as a general additional phonon scattering contributor.

Thankfully, there now exists and defined effort for computational screening and examination of materials, to predict, classify and explain thermal and electronic conductivity and specific heat, among other attributes, as a function of composition, growth and crystal structure. These methods are excellent for specific materials and for comparatively assessing their thermoelectric properties.[55] When done in tandem with methods that examine superstructure and arrangements of materials, porosity (random or patterned) so that material thermal conductivity may be further suppressed while ensuring the power factor and *ZT* are enhanced, the community may be able to more quickly apply state of the art experimental infrastructures to confirm these advances. Interfaces are crucial, and a defined examination of heat transfer mechanisms or retardation across interfaces and the factors that influence the electron-phonon coupling either side of important interfaces. Density functional theory and molecular dynamics approaches,[56] when coupled, may provide a powerful way of assessing thermal interface materials and the nature of enhanced thermal conductivity suppression between materials, or between interfaces with defined 'gaps'.

The performance of thermoelectric devices on the other hand, largely depends on the internal resistances as well as the performance of the p- and n-type materials, and this is likely to be a function of how they are grown or deposited. In recent years, research is ongoing[57–59] to decrease these interface resistances but still it is a long way to achieve proper interface materials, which will be easy to fabricate and will be reliable for temperature cycling. Like contact resistance as a fundamental limitation to power efficiency in electronic device structures, it similarly plays a role in thermoelectric devices and maintain balanced as well as low contact resistances to both p- and n-type type materials is a challenge for energy harvesting systems where useful power generation from waste heat (body heat temperature levels in wearable technology as a primary example) is important. Equally, there is a need to develop thick and efficient electrodeposited compound materials for a better performance of thermoelectric devices for chip and light emitter cooling and stabilization, respectively. Challenges remain in achieving the efficiency for both p- and n-type electroplated materials similar to the their bulk counterparts.[60] The reduction of the surface roughness[61,62] and annealing time[63] of electrodeposited films and thereby improving the processability for the development of efficient micro thermoelectric devices will pave the way for future applications of these thermoelectric modules both as thermoelectric coolers as well as generators.

Lastly, phonon transport mechanisms and device level architectures, interface materials, and all materials chemistry and engineering that are critical to the next advance,[64] have a powerful gamut of experimental techniques to make accurate measurements or thermal properties. The convective and radiative nature of heat, and the parameters that govern thermal transport are always as importance a consideration and the powerful analysis and understanding derived from such measurements.

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