

Title	The understanding, control, and application of polycrystalline compound semiconductor thin films
Authors	Curran, Anya
Publication date	2023
Original Citation	Curran, A. 2023. The understanding, control, and application of polycrystalline compound semiconductor thin films. PhD Thesis, University College Cork.
Type of publication	Doctoral thesis
Rights	© 2023, Anya Curran. - https://creativecommons.org/licenses/by-nc-nd/4.0/
Download date	2026-09-19 15:18:00
Item downloaded from	https://hdl.handle.net/10468/14988

Ollscoil na hÉireann, Corcaigh
National University of Ireland, Cork



UCC

Coláiste na hOllscoile Corcaigh, Éire
University College Cork, Ireland

**The Understanding, Control, and Application of
Polycrystalline Compound Semiconductor Thin Films**

Thesis presented by

Anya Curran, B.Sc.

for the degree of

Doctor of Philosophy

Tyndall National Institute

School of Chemistry

Head of School: Prof. Anita Maguire

Supervisors: Dr Farzan Gity, Prof. Paul K. Hurley, and Prof.
Colm O'Dwyer

26-07-2023

Declaration

This is to certify that the work I am submitting is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents. I have read and understood the regulation of University College Cork concerning plagiarism and intellectual property.

Digital signature: *Anya Curran*

Contents

List of Figures	v
List of Tables	xi
Glossary	xiii
0.1 List of Publications Related to Thesis	2
0.2 List of Publications Not Related to Thesis	3
0.3 List of Conference Presentations & Proceedings	3
1 Introduction	7
1.1 Background and Motivation	7
1.2 III-V Materials	15
1.2.1 Why III-Vs?	15
1.2.2 III-V Material Substrates	18
1.2.3 Fermi Level Pinning and Gate Stack Engineering	20
1.2.4 Alternatives to III-V Materials	27
1.3 Current State of the Art	29
1.3.1 III-V Transistors	29
1.3.2 Mobility of Low Temperature Grown Materials	32
1.4 Thesis Outline	35
Bibliography	37
2 Low-Temperature Grown Polycrystalline Indium Arsenide	66
2.1 Abstract	68
2.2 Introduction	68
2.3 Experimental	70
2.4 Results and Discussion	72
2.4.1 InAs Material Properties	72

2.4.2	Surface Treatments	82
2.5	Benchmarking	85
2.6	Conclusions	85
	Bibliography	88
3	Polycrystalline InAs MOSFETs	94
3.1	Abstract	96
3.2	Introduction	96
3.3	Experimental	97
3.4	Results and Discussion	98
3.4.1	Top-Gated Poly InAs Junctionless Transistors	98
3.4.2	Dual-Gated Poly InAs Junctionless Transistors	106
3.5	Benchmarking	120
3.6	Conclusions	121
	Bibliography	123
4	Low-Temperature Grown Polycrystalline Gallium Antimonide	130
4.1	Abstract	132
4.2	Introduction	132
4.3	Experimental	134
4.4	Results and Discussion	135
4.4.1	Structural and Electronic Properties at Room Temperature	135
4.4.2	Temperature Dependent Properties	148
4.5	Benchmarking	155
4.6	Conclusions	155
	Bibliography	158
5	Thin Film Polycrystalline GaSb MOSFETs	166
5.1	Abstract	167
5.2	Introduction	167
5.3	Experimental	169
5.4	Results and Discussion	170
5.4.1	cTLM Results	170
5.4.2	Back-gated Device Results	173
5.4.3	50nm GaSb on a Tyndall Silicon Substrate	183
5.4.4	Top-gated Device Results	187
5.4.5	Dual-Gated Device Results	189

5.5	Benchmarking	192
5.6	Conclusions	193
	Bibliography	195
6	Conclusions and Future Work	199
6.1	Outlook and Future Work	199
A	Hall Effect Measurement method	204
B	Resistivity Extraction from circular Transmission Line Measurement (cTLM)	212
C	InAs Buried Channel Devices	215

List of Figures

1.1	Historical trend for number of transistors per chip [3] (adapted from Nature with reuse license 5576901298181) and recent data from processors designed by industry leading companies.	8
1.2	Manifestation of short channel effects/Drain-Induced Barrier Lowering (DIBL) in device characteristics [7] ©2012 IEEE. . .	10
1.3	Traditional von Neumann architecture schematic.	12
1.4	3D integration examples involving (a) Complementary Metal Oxide Semiconductor (CMOS) over CMOS by wafer bonding [11] ©2016 IEEE, (b) <i>n</i> -type Metal Oxide Semiconductor (<i>n</i> -MOS) over <i>p</i> -type Metal Oxide Semiconductor (<i>p</i> -MOS) [12] ©2017 IEEE, and (c) embedding of active components in back-end-of-line (BEOL) [13].	14
1.5	Schematic representation of (a) crystalline, (b) polycrystalline, and (c) amorphous materials.	17
1.6	Cross-sectional Transmission Electron Microscopy (XTEM) images of the interface between InGaAs and Atomic Layer Deposition (ALD) deposited HfO ₂ where the InGaAs has received (a) no treatment, (b) H ₂ S at 350°C, (c) H ₂ S at 200°C, (d) H ₂ S at 50°C, and (e) (NH ₄) ₂ S [47] (reused from Journal of Applied Physics with reuse license 5576901485460).	22
1.7	Band bending in MOS structure.	25
1.8	(a) Output and (b) transfer characteristics for two InGaAs nanowire transistors with and without Forming Gas Anneal (FGA) [70] (reused from Applied Physics Letters with reuse license 5576910086647).	27
1.9	Hole hall mobility vs maximum fabrication temperature [119–133].	34

1.10	Electron hall mobility vs maximum fabrication temperature [134–147].	34
2.1	Schematic representation of the “droplet epitaxy” growth process.	73
2.2	(a&b) XTEM images of nominally 25 nm poly InAs film grown at 475°C directly on a glass substrate. (c) Temperature dependent Hall effect measurements of 25 nm poly InAs film on glass. Measurements taken in AC mode, with magnetic field of 0.6 T	75
2.3	(a) Plot of one line taken during an Atomic Force Microscopy (AFM) scan of the 25 nm InAs on glass, and (b) a plot of height vs frequency.	78
2.4	XTEM images of (a&b) 25 nm poly GaAs + 25 nm poly InAs on glass (where the red line indicates position of the interface), and (c) 25 nm poly InAs directly on glass.	81
2.5	(a) Schematic cTLM structure layout from which electrical measurements were taken. (b) Specific contact resistance, (c) sheet resistivity, (d) transfer length, and (e) resistivity for a 25 nm poly InAs film which received each of the surface treatments, and a reference sample which received no surface treatment.	84
2.6	Results from polycrystalline InAs films in this work compared to results from the literature [16–29].	86
3.1	(a) Schematic cross-section of the film structure in the channel region of the device, and (b) plan-view of device layout. . . .	99
3.2	(a) Device output and (b) transfer characteristics at room temperature. (c) Field-effect mobility, and (d) carrier concentration extracted from transconductance. The device dimensions and bias conditions are shown in the inset of each figure. . . .	102
3.3	Transfer characteristics of (a) 25 nm GaAs + 25nm Zn-doped InAs(P) on a Si/SiO ₂ , (b) 25 nm Zn-doped InAs(P) grown directly on glass, and (c) 25 nm Zn-doped InAs directly on Si/SiO ₂ . Structures through the channel region are shown beside each transfer characteristic.	104

3.4	I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} for (a) 25 nm GaAs + 25 nm Zn-doped InAs(P), and (b) 25 nm Zn-doped poly InAs on glass. Schematics of the sample taken through the gate stack are shown beside the corresponding results.	105
3.5	Time-Of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS) results showing level of (a) Ga, (b) In, and (c) As vs depth from the surface, taken from sample shown in 3.4a.	107
3.6	TOF-SIMS results showing the depth profile of In in a sample consisting of 25 nm Zn-doped InAs(P) directly on an Si/SiO ₂ substrate.	108
3.7	Maximum depletion width vs carrier concentration for InAs films. Inset: equation used for plotting.	109
3.8	(a) I_{OFF} dependence on channel length for 25 nm InAs grown directly on glass, with V_{DS} values shown ($V_{GS} = 5V$). (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} vs gate length for the same sample ($V_{DS} = 1 V$, $I_{ON} V_{GS} = 5 V$, $I_{OFF} V_{GS} = -5V$). Note: the channel length (L_{ch}) is the separation between the source and drain contacts and the gate length is the width of the gate metal (see Figure 3.1b).	111
3.9	(a) Transfer characteristics of 25 nm Zn-doped InAs film on Si/SiO ₂ . (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} taken from the same measurements.	113
3.10	Output characteristics of 25 nm Zn-doped InAs film on Si/SiO ₂	114
3.11	(a) Transfer characteristics of 25 nm Zn-doped InAs film on Si/SiO ₂ at variable temperatures. (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} taken from the same measurements.	115
3.12	(a) Transfer characteristics of 25 nm Zn-doped InAs film on Si/SiO ₂ with back gate potential shown in inset. (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} taken from the same measurements and shown vs back gate potential. I_{ON} was taken at a top gate voltage of +5 V and I_{OFF} was taken at a top gate voltage of -6 V. Output characteristics with (c) a constant back-gate voltage of 0V and (d) a constant top-gate voltage of 2 V. Device dimensions are shown in inset.	117
3.13	Transfer characteristics of 25 nm Zn-doped InAs film on Si/SiO ₂ channel device with different ratios of back-gate to top-gate voltage.	118

4.1	Scanning Electron Microscopy (SEM) images of (a) 50 nm GaSb on SiO ₂ , (b) 150 nm GaSb on SiO ₂ , (c) 250 nm GaSb on SiO ₂ , (d) 50 nm GaSb on SI GaAs, (e) 50 nm GaAs + 50 nm GaSb on SiO ₂ , and (f) 50 nm GaAs + 50 nm GaSb on Semi-Insulating (SI) GaAs. All scale bars are 1 μ m.	138
4.2	XTEM image of a larger area of the 50 nm GaSb on Si/SiO ₂ lamella.	139
4.3	(a) Scanning Transmission Electron Microscopy (STEM) image of nominally 50 nm poly GaSb on SiO ₂ . EDX analysis showing presence of (b) Ga-L, (c) Sb-L, and (d) As-K.	139
4.4	XTEM images of (a) 50 nm GaSb on SiO ₂ , (b) 250 nm GaSb on SiO ₂ , and (c) 50 nm GaAs + 50 nm GaSb on SiO ₂ . (d) STEM image of 50 nm GaAs + 50 nm GaSb on SiO ₂	143
4.5	Energy-Dispersive X-Ray (EDX) analysis on layers of heterostructure on SiO ₂	144
4.6	X-Ray Diffraction (XRD) of 50 nm GaAs + 50 nm GaSb on SiO ₂ , 50 nm GaSb on SiO ₂ , and 50 nm GaAs + 50 nm GaSb on GaAs.	145
4.7	SEM images of 50 nm GaAs + 50 nm GaSb heterostructures on SiO ₂ with (a) no Zn, and Zn/Ga ratios of (b) 0.025, (c) 0.25, and (d) 2.5.	147
4.8	Repeated resistivity measurements of (a) 50 nm GaSb and (b) 250 nm GaSb on a Si/SiO ₂ substrate. Excitation current is shown in inset.	149
4.9	Resistivity vs Temperature for 250 nm GaSb on Si/SiO ₂ . Inset lists stage of measurement in order they were performed. . . .	150
4.10	Carrier mobility and concentration of (a) 250 nm GaSb on a SI GaAs substrate, (b) 250 nm GaSb on a Si/SiO ₂ substrate, and (c) 50 nm GaAs + 50 nm GaSb on a Si/SiO ₂ substrate. .	151
4.11	(a) log, log plot of mobility vs temperature for 250nm GaSb on Si/SiO ₂ , and (b) natural log of conductivity vs $T^{-1/4}$ for 50 nm GaAs + 50 nm GaSb on SiO ₂	154
4.12	Results from polycrystalline and amorphous GaSb films in this work compared to results from the literature [16, 30–43]. . . .	156
5.1	Schematic of junctionless transistor device layout.	170
5.2	Schematic of circular Transmission Line Measurement (cTLM) structure layout.	171

5.3	Back-gated IV characteristics of transistors with a channel material of (a) 50 nm, (b) 150 nm, and (c) 250 nm GaSb on Si/SiO ₂ . (d) The values for I_{ON} and I_{OFF} vs nominal film thickness for each sample.	176
5.4	I_{DS} - V_{DS} output curves for devices with GaSb channel thickness of (a) 50 nm, (b) 150 nm, and (c) 250 nm.	177
5.5	Pre and post oxide deposition IV characteristics of samples with GaSb channel thickness of (a) 50 nm, (b) 150 nm, and (c) 250 nm.	180
5.6	Temperature dependent I_{DS} - V_{GS} of 50 nm GaSb sample (a) pre and (b) post surface treatment and oxide deposition. Comparison of I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} ratio (c) pre and (d) post. . .	181
5.7	(a) Transfer characteristics of 50 nm GaSb film on Tyndall Si/SiO ₂ substrate. (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} taken from the same measurements. I_{ON} is taken at $V_{GS} = -40$ V, and I_{OFF} is taken at $V_{GS} = 40$ V.	185
5.8	Output characteristics of 50 nm GaSb film on Tyndall Si/SiO ₂ substrate.	185
5.9	(a) Transfer characteristics of 50 nm GaSb film on Tyndall Si/SiO ₂ substrate at variable temperature. (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} taken from the same measurements.	187
5.10	Maximum depletion width vs carrier concentration for GaSb. Inset: Equation used for calculations and plotting.	188
5.11	(a) IV measurement of 50 nm GaSb on SiO ₂ using only the top-gate, prior to annealing. (b) IV measurement of the same film and device using both gates. Back-gate potential range is shown in graph.	190
5.12	Sheet resistivity values determined through cTLM measurements for the 150 nm sample vs “back-gate” voltage.	191
5.13	Dual-gated transfer characteristics of devices whose channels are (a) 50 nm and (b) 250 nm polycrystalline GaSb.	192
A.1	Picture of the Hall Effect Measurement System.	205
A.2	Varying applied current for GaSb film on SiO ₂ displaying a breakdown of the oxide and coupling to the substrate at higher applied currents. Direct measurement of the substrate is included for comparison.	207

A.3	Picture of sample holder for room temperature insert in the Hall Measurement System.	208
A.4	Example of results table generated during resistivity measurements.	209
A.5	Picture of sample holder for Closed Cycle Refrigerator (CCR) insert in the Hall Measurement System.	211
B.1	(a) Schematic of cTLM structure layout. (b) Representative IV curve of cTLM structures at different gaps, and (c) representative R_{TOT} graphs before and after correction vs gap. . . .	213
C.1	Schematic of a buried channel and device structure.	217
C.2	Transfer characteristics of AlInAs/InAs/AlInAs buried channel devices.	219
C.3	Schematic of a buried channel structure device adapted from the literature (6).	220

List of Tables

1.1	Electrical properties of silicon and commonly used III-V materials [17].	16
1.2	Examples of functional n -type III-V based transistors from the literature.	31
1.3	Examples of functional p -type III-V based transistors from the literature.	32
2.1	Room temperature Hall effect measurement results of poly InAs films of 10 nm or 25 nm nominal thickness, with or without prior 25nm poly GaAs buffer layer, grown on glass.	79
2.2	Room temperature Hall effect measurement results of poly GaAs + Zn-doped InAs(P) grown on SiO ₂	82
3.1	Hall effect measurement results of 25 nm Zn-doped InAs on SiO ₂	112
3.2	Transfer characteristics data for 25 nm Zn-doped InAs film on Si/SiO ₂ pre and post top gating. Device dimensions are $L_{ch} = 10 \mu\text{m}$, $W_{ch} = 5 \mu\text{m}$, and $L_{gate} = 4 \mu\text{m}$	119
3.3	Examples of functional n -type III-V based transistors from the literature with results from this chapter included for comparison.	122
4.1	Room-temperature Hall effect measurement results of GaSb on SiO ₂	140
4.2	Room-temperature Hall effect measurement results of GaSb on GaAs.	141
4.3	Room temperature Hall effect measurement results for 50 nm GaAs + 50 nm GaSb films with varying Zn incorporation. . .	148

5.1	Comparison of resistivity data extracted from circular Transmission Line Measurement (cTLM) and Hall effect measurements.	173
5.2	cTLM results from GaSb devices post oxide deposition, with comparison to pre oxide results and Hall measurements.	182
5.3	Pre- and post-annealing cTLM results for 50 nm GaSb on SiO ₂	183
5.4	Comparison of gate voltage difference for different temperatures, taken at 10 ⁻⁹ A on each side of the hysteresis of transfer characteristics in Figure 5.9.	186
5.5	Examples of functional <i>p</i> -type III-V based transistors from the literature compared with devices fabricated in this chapter.	193
C.1	X-ray Photoelectron Spectroscopy (XPS) results of Al containing InAs films at no tilt and 60° tilt	218

Glossary

***n*-MOS** *n*-type Metal Oxide Semiconductor

***p*-MOS** *p*-type Metal Oxide Semiconductor

AFM Atomic Force Microscopy

ALD Atomic Layer Deposition

BEOL back-end-of-line

BOE Buffered Oxide Etch

CCR Closed Cycle Refrigerator

CMOS Complementary Metal Oxide Semiconductor

CMP Chemical Mechanical Polishing

cTLM circular Transmission Line Measurement

CVD Chemical Vapour Deposition

DEZn Diethyl Zinc

DIBL Drain-Induced Barrier Lowering

EDX Energy-Dispersive X-Ray

FET Field Effect Transistor

FGA Forming Gas Anneal

FIB Focussed Ion Beam

IC Integrated Circuit

MOS Metal-Oxide Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MOVPE Metalorganic Vapour Phase Epitaxy

NW Nanowire

QW Quantum Well

SEM Scanning Electron Microscopy

SI Semi-Insulating

STEM Scanning Transmission Electron Microscopy

TEGa Triethyl Gallium

TEM Transmission Electron Microscopy

TFET Tunnelling Field Effect Transistor

TMA Trimethyl Aluminium

TMGa Trimethyl Gallium

TMIn Trimethyl Indium

TMSb Trimethyl Antimonide

TOF-SIMS Time-Of-Flight Secondary Ion Mass Spectrometry

XOI Semiconductor-on-Insulator

XPS X-ray Photoelectron Spectroscopy

XRD X-Ray Diffraction

XTEM Cross-sectional Transmission Electron Microscopy

Acknowledgements

Thank you firstly to my supervisors, Prof. Paul Hurley, Dr Farzan Gity, and Prof. Colm O'Dwyer for their help and guidance for the five plus years I've been working on this thesis. Their helpfulness and kindness on a professional and personal level have been exceptional, especially in the last few years when a proverbial spanner was thrown in the works.

Thank you to Dr Scott Monaghan for his invaluable advice and knowledge on the Hall measurement system and the interpretation of the results, and thank you to Dr Jun Lin for taking over as the equipment responsible for this important piece of equipment during the latter stages of my PhD research.

Thank you to Dr Karim Cherkaoui for always knowing what is wrong with the probe station and more importantly knowing how to fix it.

Thank you to Dr Ray Duffy for advice on careers and organisation for the thesis. Always direct, to the point!

Thanks also to my friends and family for help with and distraction from this thesis.

0.1 List of Publications Related to Thesis

- ◇ **A. Curran**, A. Gocalinska, A. Pescaglini, E. Secco, E. Mura, K. Thomas, R. E. Nagle, B. Sheehan, I. M. Povey, E. Pelucchi, C. O'Dwyer, P. K. Hurley, and F. Gity, Structural and electronic properties of polycrystalline InAs thin films deposited on silicon dioxide and glass at temperatures below 500°C, Crystals 11(2), 2021, DOI: 10.3390/cryst11020160.
- ◇ **A. Curran**, F. Gity, A. Gocalinska, E. Mura, R. E. Nagle, M. Schmidt, B. Sheehan, E. Pelucchi, C. O'Dwyer, P. K. Hurley, High Hole Mobility Polycrystalline GaSb Thin Films, Crystals 11(11), 2021, DOI: 10.3390/cryst11111348.
- ◇ A. Gocalinska, A. Pescaglini, E. Secco, E. Mura, K. Thomas, **A. Curran**, F. Gity, R. Nagle, M. Schmidt, P. P. Michałowski, P. K. Hurley, I. Povey, E. Pelucchi, Next generation low temperature polycrystalline materials for above IC electronics. High mobility n- and p-type III-V metalorganic vapour phase epitaxy thin films on amorphous substrates, Journal of Physics: Photonics 2(2), 2020, DOI: 10.1088/2515-7647/ab7557.

0.2 List of Publications Not Related to Thesis

- ◇ F. Gity, F. Meaney, **A. Curran**, P. Hurley, S. Fahy, R. Duffy, L. Ansari, Doping of ultra-thin Si films: Combined first-principles calculations and experimental study, Journal of Applied Physics 129(1), 2021, DOI: 10.1063/5.0035693

0.3 List of Conference Presentations & Proceedings

- ◇ **A. Curran**, E. Secco, A. Pescaglini, A. Gocalinska, E. Mura, K. Thomas, R. Nagle, I. M. Povey, E. Pelucchi, C. O'Dwyer, P. K. Hurley, and F. Gity, Investigating Polycrystalline III-V Thin Films as Channel Materials for “Above IC” Logic and Memory Applications, presented at ECS AiMES Conference, 2nd October 2018, Cancun, Mexico, abstract DOI: 10.1149/ma2018-02/34/1165.
- ◇ **A. Curran**, F. Gity, A. Gocalinska, E. Mura, R. E. Nagle, M. Schmidt, B. Sheehan, E. Pelucchi, C. O'Dwyer, P. K. Hurley, Investigating the Structural and Electronic Properties of Polycrystalline GaSb Thin Films Grown on SiO₂, poster presented at 50th IEEE Semiconductor Interface Specialists Conference, December 2019, San Diego, USA.

Abstract

In this thesis, low-temperature grown polycrystalline III-V materials are investigated for their potential as channel materials for devices located in the back-end-of-line (BEOL) of integrated circuits. The key aims of this thesis are to demonstrate high carrier mobility III-V materials grown at low temperatures on silicon/amorphous substrates, and to fabricate functional transistor devices using these polycrystalline/amorphous III-V films as channel materials. There are very few reports of low temperature grown polycrystalline III-V materials available in the literature and so this thesis is well placed to add substantial knowledge to the field.

Both an *n*-type (InAs) and a *p*-type (GaSb) material are investigated. The poly III-V films are grown on Si/SiO₂, glass, or Semi-Insulating (SI) GaAs substrates. For the intended implementation in the BEOL, it is necessary to stick to a restrained thermal budget, with maximum temperatures generally being <500°C. Growth of III-V materials on silicon substrates is an important step towards their integration with silicon-based electronics. Growth at these reduced temperatures and on amorphous substrates such as SiO₂ are large challenges to overcome while maintaining a reasonable carrier mobility. It is also important to develop *n*- and *p*-type options so that these materials can be implemented in low-power Complementary Metal Oxide Semiconductor (CMOS) type architectures.

Material properties of the films as grown are explored through Scanning Electron Microscopy (SEM), Atomic Force Microscopy (AFM), Transmission Electron Microscopy (TEM) and Cross-sectional Transmission Electron Microscopy (XTEM), and Hall Effect measurements. The Hall Effect measurements indicate that both of these materials have high carrier concentrations independent of intentional doping or a high-temperature dopant activation step and display high carrier mobilities despite their polycrystalline or amorphous nature. Electron mobility values in polycrystalline InAs are found to be $100 \text{ cm}^2/\text{Vs}$ at room temperature for InAs grown directly on a glass substrate, and values reaching $155 \text{ cm}^2/\text{Vs}$ for a heterostructure including the polycrystalline InAs film. Hole mobilities in the polycrystalline GaSb films are found to be up to $66 \text{ cm}^2/\text{Vs}$ for a film grown directly on SiO_2 and $299 \text{ cm}^2/\text{Vs}$ for a film grown directly on SI GaAs. An amorphous GaSb layer which is part of a heterostructure on SiO_2 is found to have a hole mobility of $9.1 \text{ cm}^2/\text{Vs}$. These results are compared against those found in the literature and found to exceed many, while being competitive with those that are grown at higher temperatures, on crystalline substrates, or to greater thicknesses. All of these are self-imposed limits to keep the material growth suitable for devices in the BEOL, so to be competitive with mobilities obtained without these limitations is a very important and positive result. Development of both *n*- and *p*-type semiconductor options is a vital component of this field of research and the *p*-type mobilities reported in this thesis compare partic-

ularly well with those reported in the literature.

Junctionless transistor devices are fabricated, with full processing steps described. Both *n*- and *p*-type functional devices are demonstrated, and analysis of the device characteristics is performed to determine limiting factors and mechanisms at play. Analysis is performed on the devices at different stages of the device processing to understand the effect on the semiconducting material. The highest I_{ON}/I_{OFF} values are achieved at -50°C for both types of devices, with 10^4 achieved for *n*-type devices, and 550 achieved for *p*-type devices. These results are compared against those found in the literature. Recommendations for future implementation of these materials into high-performance devices are made based on the results generated in this thesis. This includes the recommendation to grow thicker films and develop a Chemical Mechanical Polishing (CMP) process to thin them back down, ideally creating a thinner yet more continuous film, and to conduct some systematic studies of the gate stack process for the transistor devices.

Low-temperature grown polycrystalline and amorphous materials show great potential as high carrier mobility materials which can be implemented into silicon-based electronics in the BEOL where a low thermal budget is required for device processing.

Chapter 1

Introduction

1.1 Background and Motivation

Eighteen years after the invention of the transistor (for which John Bardeen, Walter Brattain, and William Shockley were awarded the Nobel prize in physics, 1956), Gordon Moore made his bold prediction that the number of transistors in an integrated circuit would double every year (later revised to every two years). This prediction, known as Moore's Law, held true for many years, with advances in the technology being made almost exclusively through dimensional scaling of the components. Dennard scaling mathematically described the factors for different device and circuit parameters [1]. Now the definition of Moore's law has been made somewhat more ambiguous to facilitate the concept of "more Moore", and Dennard scaling has become mostly obsolete [2]. Figure 1.1 shows the historical trend in number of tran-

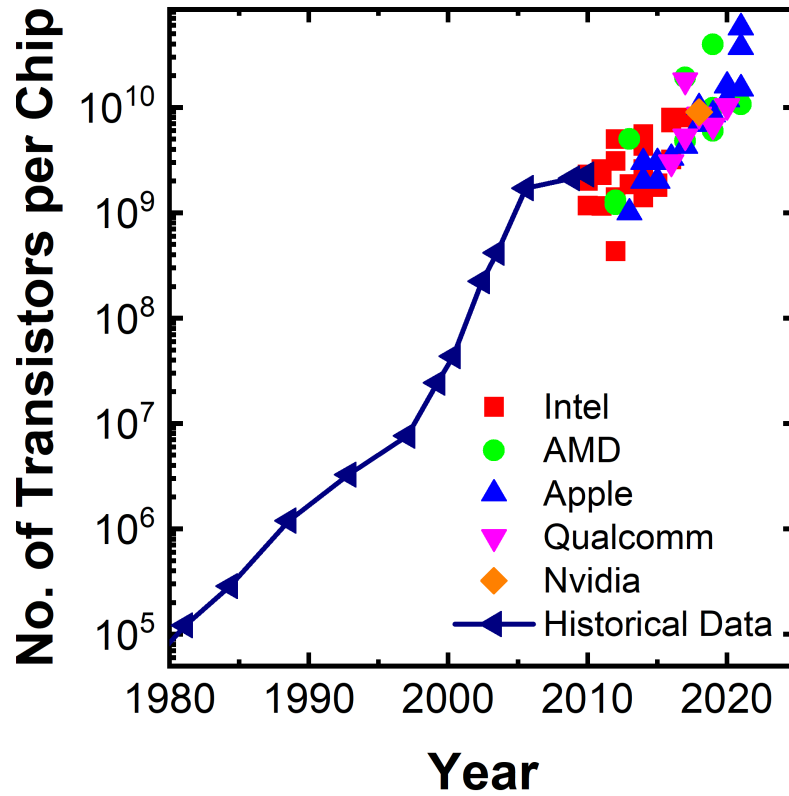


Figure 1.1: Historical trend for number of transistors per chip [3] (adapted from Nature with reuse license 5576901298181) and recent data from processors designed by industry leading companies.

sistors per chip from circa 1980 to 2010 [3], followed by data from 2010 to 2021 for several industry leading companies. The data shows a linear trend on a log scale, which is in agreement with Gordon Moore’s consistent doubling prediction.

As dimensional scaling of components began to reach fundamental limits, innovations were made to push these limits further down the road and con-

tinue the exponential increase in the number of transistors per chip as shown in Figure 1.1. These innovations included strained silicon channels to increase carrier mobility, high- κ gate oxides to replace SiO_2 , and re-introducing metal gate contacts. Implementation of these new technologies mitigated effects such as mobility deterioration due to higher fields in the transistor channel, and excessive leakage through the gate stack [4]. It has been shown that strained silicon can achieve an improvement over bulk Si of around 2x for electron mobility and up to 10x for hole mobility [5], while high- κ dielectrics can reduce the gate leakage by around 6 orders of magnitude [6].

Short channel effects have also become impossible to ignore as the source to drain separation reduces below 100nm. Short channel effects occur when the depletion regions associated with the area under the source and drain encroach upon the channel to an extent where the gate no longer fully controls the channel. This manifests itself in two main ways: Drain-Induced Barrier Lowering (DIBL), whereby the threshold voltage is decreased by an increasing drain voltage, and the degradation of the subthreshold slope. Both of these increase the leakage from a device [3]. Figure 1.2 shows how these effects manifest in the I_D - V_G and I_D - V_D characteristics of a device [7], where I_D is the current measured at the drain, V_G is the voltage measured at the gate, V_D is the voltage measured at the drain, V_t is the threshold voltage, and DIBL is drain induced barrier lowering. These effects can be alleviated to some degree by novel device structures which implement a multi-gate ar-

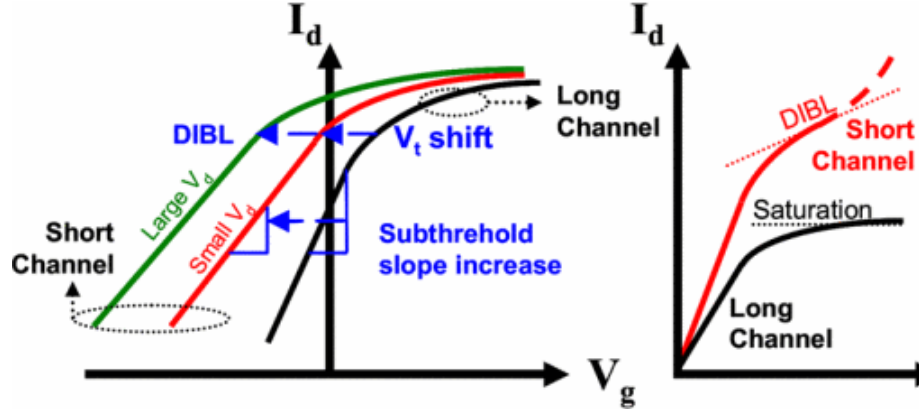


Figure 1.2: Manifestation of short channel effects/DIBL in device characteristics [7] ©2012 IEEE.

chitecture [3, 4].

Power consumption of devices in an Integrated Circuit (IC) is an increasingly important issue to overcome [8], especially with increasing device density on chip. There are two components of a device's power consumption:

1. Active power consumption
2. Subthreshold power consumption

The equations governing these components are shown below [9].

$$P_{\text{act}} = C \cdot V_{\text{DD}}^2 \cdot f \quad (1.1.1)$$

Where P_{act} is the active power consumption of the device, C is the load capacitance, V_{DD} is the supply voltage, and f is the operation frequency. Here we can see that a reduction in supply voltage will decrease the active

power consumption greatly due to the squared term.

$$P_{\text{sub}} = V_{\text{DD}} \cdot I_{\text{OFF}} \quad (1.1.2)$$

Where P_{sub} is the subthreshold power consumption of the device, V_{DD} is the supply voltage, and I_{OFF} is the OFF-state current. Here, we see again that reduction of the supply voltage will still cause a reduction in the power consumption. I_{OFF} should also be well controlled, and shows that a steep subthreshold slope is important for high performance Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology.

There are also system level difficulties which must be overcome in modern computing. Namely, the latency and power losses introduced through the separation of logic and memory components, and the long bus lengths between them. Figure 1.3 shows the traditional von Neumann architecture, which implements this separation [10], where I is current, R is resistance, P is power, ρ is resistivity, L is bus length, A is area, and CPU is central processing unit. The equations in the image show the relationship of bus length to the power dissipation. Clearly, a reduction in bus length will not only improve latency, but also decrease power dissipation.

If components continue to be implemented in a 2D plane, bus lengths between devices will not be improved upon. A possible method to bypass this

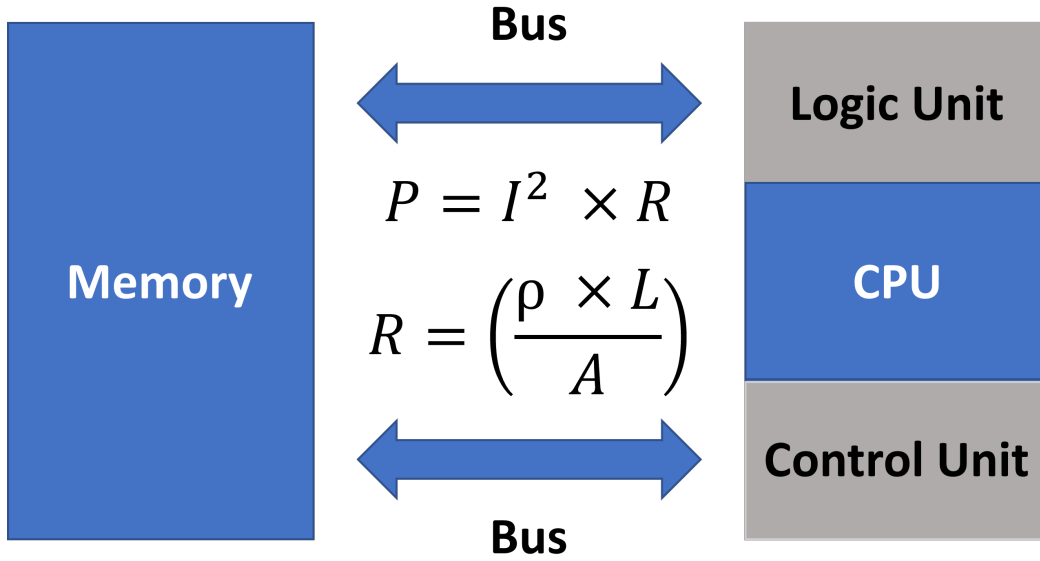
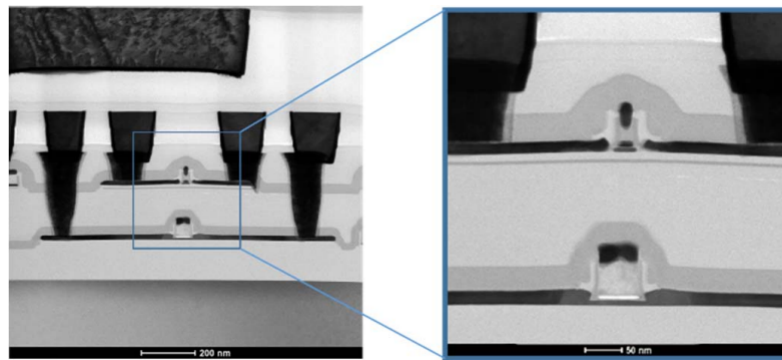


Figure 1.3: Traditional von Neumann architecture schematic.

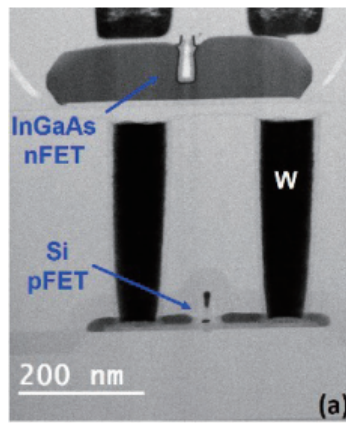
issue is 3D integration of active components. There are a number of ways to achieve this structure; however, this thesis will focus on what is commonly referred to as monolithic or sequential integration, where the different components are grown/fabricated one after the other on the same wafer. Figure 1.4 shows a variety of approaches to achieving monolithic 3D integration. Figure 1.4a shows Complementary Metal Oxide Semiconductor (CMOS) over CMOS achieved through wafer bonding [11], Figure 1.4b shows *n*-type Metal Oxide Semiconductor (*n*-MOS) over *p*-type Metal Oxide Semiconductor (*p*-MOS) [12], while Figure 1.4c shows logic and memory embedded in the back-end-of-line (BEOL) [13]. There are positives associated with each method; however, these often involve novel procedures and fabrication methods, which would

require an overhaul of current set up in an industrial environment. The method depicted in Figure 1.4c allows for conventional fabrication processes of deposition and etching to be maintained, before planarization and fabrication of the BEOL embedded devices. This approach avoids the need for large area wafer to wafer bonding. However, this upper layer must be fabricated under conditions compatible with this “above IC” level i.e., at lower temperatures than many steps in conventional semiconductor processing usually require, such as epitaxial regrowth (typically around 600°C) and dopant activation (up to 1000°C).

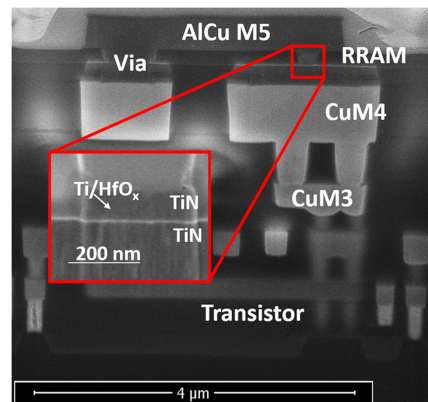
During conventional IC fabrication, many steps require higher temperatures than are compatible with the lower thermal budget required for BEOL integration (usually <500°C). At these lower temperatures, it is difficult to create high quality, consistent, and dependable devices [14]. In this thesis, materials which do not require intentional doping, and therefore no high-temperature dopant activation step, are explored as options for devices integrated into the BEOL. Here, these are polycrystalline and amorphous III-V thin films.



(a)



(b)



(c)

Figure 1.4: 3D integration examples involving (a) CMOS over CMOS by wafer bonding [11] ©2016 IEEE, (b) *n*-MOS over *p*-MOS [12] ©2017 IEEE, and (c) embedding of active components in BEOL [13].

1.2 III-V Materials

1.2.1 Why III-Vs?

III-V materials have long been investigated as a replacement channel material for traditional silicon electronics. III-Vs have the potential to achieve high performance devices with high ON-currents and switching speed at lower operating voltages due to their significantly higher carrier mobilities when compared to silicon [15, 16]. This is hugely beneficial for future technologies due to the emergence of power constrained scaling [8]. Table 1.1 shows some parameters of commonly used III-V materials compared to silicon. While III-V materials exhibit improved electron mobility, they still suffer from a disparity between n - and p -type mobilities, with varying degrees of severity. Some offer similar or improved hole mobilities to silicon, a key challenge for next generation materials, as p -type technologies lag the development of their n -type counterparts.

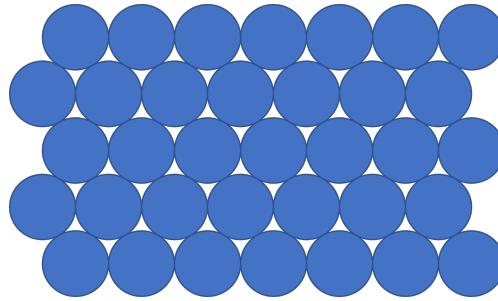
In this thesis, polycrystalline and amorphous III-V materials are investigated, as they can be grown within parameters suitable for BEOL integration in silicon-based electronics i.e., low-temperature growth ($<500^{\circ}\text{C}$) on silicon substrates. Figure 1.5 shows a schematic representation of different levels of crystallinity in a material. The main difference is the extent of periodicity in the film. A fully crystalline sample (Figure 1.5a) will have long range periodicity throughout the entire film, a polycrystalline sample (Figure 1.5b) will

Material	Electron Mobility [cm^2/Vs]	Hole Mobility [cm^2/Vs]	Ratio of n to p Mobility	Band Gap [eV]
Si	1,400	450	3.1	1.12
InP	5,400	200	27	1.34
GaAs	8,500	400	21.3	1.42
$\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$	14,000	300	46	0.75
InAs	40,000	500	80	0.35
GaSb	3,000	1,000	3	0.72
InSb	77,000	850	91	0.17
GaN	1,000	200	5	3.2

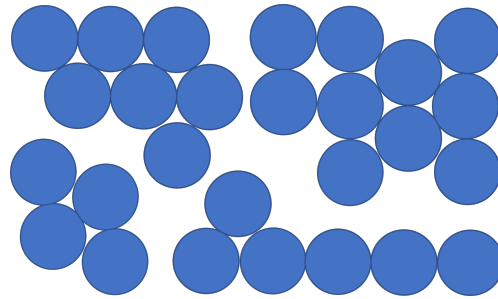
Table 1.1: Electrical properties of silicon and commonly used III-V materials [17].

have shorter range periodicity within the crystal “grains” present in the film, and an amorphous sample (Figure 1.5c) will lack periodicity entirely. It is clear from this structure that there are additional factors affecting properties and performance in polycrystalline films when compared to a crystalline one, including grain size and effects at grain boundaries [18–20]. Properties such as carrier mobility are generally degraded as crystallinity is lost. For this reason, III-Vs are promising candidates for polycrystalline and amorphous films with acceptable mobilities, as their initial bulk crystalline value are relatively high.

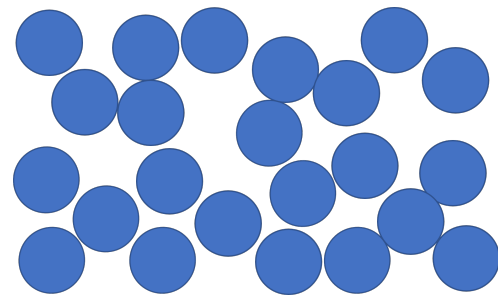
Polycrystalline and amorphous materials are also of interest for use in flexible electronics, which are usually formed on substrates which are not compatible with high-temperature processes [21–23]. This creates a need for balancing low-temperature processes with the quality of the electrical characteristics,



(a)



(b)



(c)

Figure 1.5: Schematic representation of (a) crystalline, (b) polycrystalline, and (c) amorphous materials.

which tend to be poor [24]. The grain boundary properties of polycrystalline materials can sometimes be favourable, however, due to the nature of polycrystalline materials, there can be excessive variation from one device to another, which is only exacerbated by the continuing trend of device miniaturization. For this reason, amorphous materials may be preferable, however they exhibit a greater deterioration in some key performance indicators such as carrier mobility [25].

To replace silicon in commercial consumer electronics, a new technology which requires a large overhaul in processing methods will have to represent a larger improvement on the current state of the art, as well as tangible proof of further generations with additional significant improvements in the near future [15]. Otherwise, the necessary investment would not be justified. To achieve this stipulation, III-V materials must overcome a number of fundamental challenges, outlined in Sections 1.2.2 and 1.2.3.

1.2.2 III-V Material Substrates

As is evident from Tables 1.2 and 1.3, the most commonly chosen substrates for III-V film growth are III-V wafers. For commercial consumer electronics, this represents a significant increase in cost, which is generally incompatible with the market [16]. This is stark contrast to silicon, which is available at relatively low cost, and in the large wafer sizes used in commercial large-scale production. It is most likely that III-V materials will not replace

silicon entirely, but be integrated alongside silicon-based electronics, meaning growth on silicon substrates is an important step towards commercial viability [26, 27]. III-V wafers are commonly used as substrates for III-V materials, as these materials generally have a large lattice offset with silicon, as well as a higher thermal expansion coefficient. This causes difficulty in forming a high-quality III-V film with low defect density on silicon, which is the ubiquitous substrate in modern electronics [16].

The lattice mismatch between III-V materials and the substrate causes threading dislocations in the material which can extend all the way to the surface of the film, and misfit dislocations at the interface of the film and the substrate [28]. The difference in thermal expansion coefficients can cause tensile strain in the III-V film as it cools post growth, causing the emergence of edge dislocations [29, 30]. Lattice mismatch issues have been mitigated to some degree in the literature using buffer or nucleation layers directly on the substrate prior to semiconductor deposition [28, 29, 31, 32], or novel growth mechanisms such as core-shell nano-pillars [33, 34]. A buffer layer method can also be employed to alleviate the issue of growing polar materials e.g. GaSb on non-polar silicon [35–38]. However, all of these methods ultimately require additional steps during the growth process.

A key aim of this thesis is to demonstrate polycrystalline and amorphous III-V materials, grown on amorphous/silicon substrates, which possess high

carrier mobilities.

1.2.3 Fermi Level Pinning and Gate Stack Engineering

Native Oxide Removal and Surface Passivation

The next large challenge for integration of III-V materials is the engineering of a suitable gate stack for high performance devices. These devices will be required to avoid the use of metal to channel Schottky barrier contacts, as these result in large gate leakage [26], and instead implement the high- κ /metal contact stack found in modern high performance silicon devices. The native oxides of III-V materials are not suitable for use as gate oxides, unlike silicon's native oxide, due to instability, high levels of defects, and a non-abrupt, rough interface [39]. The interaction of the III-V surface with oxygen results in Fermi level pinning at the surface as the defective interface between the III-V material and its oxide forms. Fermi level pinning restricts the ability to move the Fermi level through the band gap at the III-V/oxide surface using the gate voltage, thereby limiting the transistor functionality. This issue must be approached using two steps:

1. The removal of the III-V native oxide and passivation of the resulting surface.
2. The selection and deposition of a suitable high-quality gate oxide.

The goal of this is to form a gate stack with a III-V/high- κ /metal contact formation, with minimal interface defects and electrically active defects in

the high- κ oxide.

Removal of the surface oxide and passivation of the resulting surface can be achieved in many ways. Surface treatment/passivation can be performed ex- or in-situ in relation to where the oxide deposition will be carried out. In-situ is preferable as the regrowth of oxides on the III-V surface is rapid on re-exposure to air. Some of the most common methods employed to remove native oxides/passivate the III-V surface are sulfurization [40], nitridation [41–43], phosphor passivation [44], and HCl [45, 46]. Sulfurization is the method used in this thesis, and so will be discussed in more detail. Figure 1.6 shows Cross-sectional Transmission Electron Microscopy (XTEM) images of the interface of InGaAs with HfO₂ deposited by Atomic Layer Deposition (ALD) [47] which has undergone a sulfurization treatment at range of temperatures using either H₂S or an aqueous solution of (NH₄)₂S. While an interfacial layer is present in all samples, compared to the sample with no treatment in Figure 1.6a, the rest of the samples exhibit a reduced interfacial layer thickness. The HfO₂ layer thickness is also found to be closer to the nominal value when a surface treatment is employed.

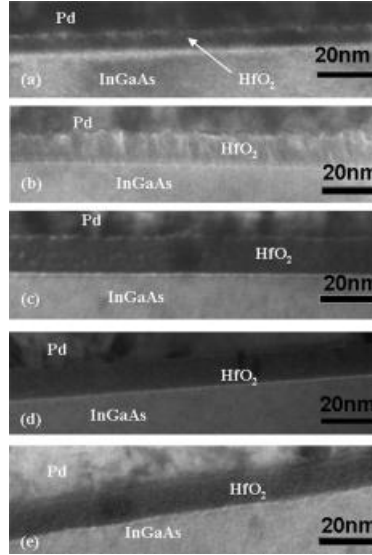


Figure 1.6: XTEM images of the interface between InGaAs and ALD deposited HfO_2 where the InGaAs has received (a) no treatment, (b) H_2S at 350°C , (c) H_2S at 200°C , (d) H_2S at 50°C , and (e) $(\text{NH}_4)_2\text{S}$ [47] (reused from Journal of Applied Physics with reuse license 5576901485460).

An aqueous solution of $(\text{NH}_4)_2\text{S}$ is often used to achieve sulfurization [47–52]. The $(\text{NH}_4)_2\text{S}$ solution etches the native oxides and sulfurizes the surface of the III-V film; however, the parameters of the surface treatment should be carefully controlled as the etching mechanism which removes the native oxides on the surface can continue etching and damage the film beneath. An etching or roughening of the surface will have a negative effect on the resulting devices due to a less ideal interface between the semiconductor and the gate oxide, causing scattering and a reduction in carrier mobility in the devices [48]. This roughening or etching effect can be mitigated through dilution of the $(\text{NH}_4)_2\text{S}$ solution to achieve the optimal level of sulfurization,

which will protect the surface [49]. Ammonium sulphide treatment is normally performed ex-situ, with the sample being moved into the tool where the gate oxide will be deposited afterwards. It has been shown that increased time between the surface treatment and the deposition of the oxide is not favourable for the electrical characteristics of the resultant device, however, under 10mins appears to still yield good results, as inferred from capacitance-voltage characterisation [48]. Sulfurization can also be achieved using a H_2S exposure, which is possible to implement ex- or in-situ [47, 53–56].

The ALD process itself can be used to remove native oxides on the III-V surface while depositing a suitable gate dielectric. ALD deposition of Al_2O_3 using a Trimethyl Aluminium (TMA) precursor has been shown to have a self-cleaning effect on the III-V surface [57, 58]. However, this appears to be limited to the removal of a few monolayers of native oxide, and so must not be relied on exclusively [59, 60]. If III-V devices are to be effectively scaled, they will also require a higher- κ gate dielectric than Al_2O_3 . This can be achieved by growing a thin layer of Al_2O_3 , followed by a high- κ dielectric such as HfO_2 [61–64]. Al_2O_3 also acts as a barrier for diffusion, improving the quality of the oxide which is deposited on top [65]. This effect is favourable as it is an in-situ technique, and can be combined with an ex-situ technique to achieve superior results.

Gate Metal Choice for Junctionless Transistors

In this thesis, the polycrystalline/amorphous III-V materials are implemented in junctionless transistor device architectures. This device architecture is well placed to utilize the conductivity of the high mobility polycrystalline/amorphous III-V films. These devices are turned off through depletion of the channel. Full depletion of the channel can be achieved at zero bias by engineering the workfunction difference between the semiconducting channel and the gate metal [66]. Figure 1.7 shows the band bending which occurs when a metal, an oxide, and a semiconductor are brought together from being separate to constituting a Metal-Oxide Semiconductor (MOS) structure. To deplete the channel at zero bias, the workfunction of the metal should be picked based on the workfunction of the semiconductor and also the majority carrier type.

Figure 1.7 shows the band bending case for a p -type semiconductor. Here we see that if the p -type film is to be depleted, a metal with a smaller value workfunction than the semiconductor should be chosen. This will result in movement of electrons from the metal into the semiconductor, effectively depleting it of holes and turning off the transistor. For an n -type semiconductor, this will be the opposite, requiring a metal which has a larger value workfunction than that of the semiconductor, so that the electrons will move from the semiconductor into the metal, depleting the channel of electrons.

This workfunction engineering of course has some practical limitations during

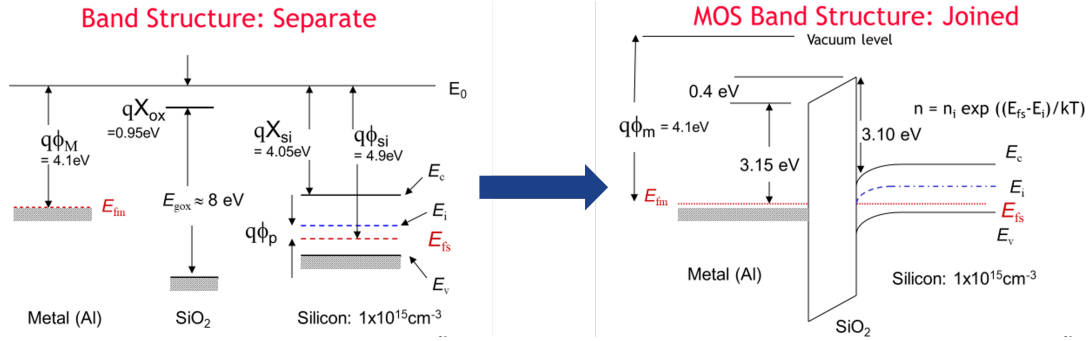


Figure 1.7: Band bending in MOS structure.

fabrication. These include:

1. It is difficult to accurately determine the workfunction of the semiconductor, especially considering the polycrystalline nature of the films in this thesis.
2. Most metals display a range of workfunction values depending on a number of factors, including deposition method.
3. Practically, we are not able to choose any metal. We are limited by those available in the lab, and those that will not react with the surface.

However, these difficulties can be overcome to some extent, as the gate voltage can also be used to deplete the channel if full depletion has not occurred after the gate metal has been deposited.

Annealing

After the gate stack has been designed and fabricated, the properties may not be exactly as desired. These properties can be seen to occur even in

devices where the III-V surface is considered unpinned. It is found to be due to defects (border traps) in the oxide layer, interface traps between the III-V channel and the oxide, and gap states which occur either in the channel or at the interface [67, 68]. Border traps in the ALD deposited gate oxide are defined by a volume density rather than the areal density of interface traps, and can cause tunnelling between carriers in the III-V channel and the trap states in the oxide. They can be identified by their large range of time constants, a weak temperature dependence [69], and the presence of frequency dispersion in the accumulation capacitance of MOS structures. Device characteristics can be further improved by annealing, which addresses to various extents the issues mentioned here.

The effects and benefits of a Forming Gas Anneal (FGA) have been extensively studied in the literature for gate stacks consisting of a III-V channel with an Al_2O_3 gate oxide [70–78]. Figure 1.8 shows how a FGA effects the transfer and output characteristics of a device [70]. The FGA is very effective at removing border traps in the oxide, and also removes some of the influence of interface traps between the oxide and the channel and the gap states in the bulk of the III-V semiconductor which are responsible for carrier generation/recombination in the channel [67]. The efficacy of other anneal methods such as H_2/Ar [79], N_2 or H_2 [78, 80], high pressure H_2 [81], and vacuum annealing [82] have also been demonstrated for improving electrical performance of devices due to gate stack optimization.

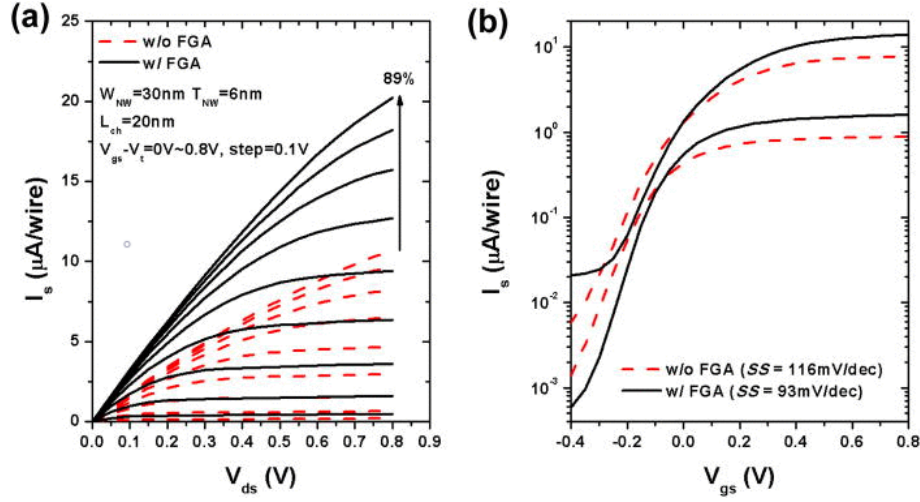


Figure 1.8: (a) Output and (b) transfer characteristics for two InGaAs nanowire transistors with and without FGA [70] (reused from Applied Physics Letters with reuse license 5576910086647).

A key aim of this thesis is to implement these methods for gate stack fabrication to produce functional transistor devices with polycrystalline/amorphous III-V channel materials.

1.2.4 Alternatives to III-V Materials

While this thesis focuses on the benefits and implementation of III-V materials, it is important to note that there are other avenues of research ongoing in an attempt to provide alternative materials which can be grown at low temperatures. 2D materials are perhaps the most prolific alternative studied in the literature and so will be discussed briefly here.

2D Materials

2D materials is an umbrella term referring to a large range of materials where one of their dimensions confined to one layer. This described 2D structure can result in properties and tunability that are not observed in the corresponding bulk material [83].

Graphene largely instigated the substantial research interest in 2D materials. The van der Waals forces holding together the carbon layers in a graphene sheet are relatively weak, allowing single layers to be exfoliated [84]. These layers exhibit many favourable properties including exceptional thermal and electrical conductivity and carrier mobility, coupled with mechanical strength. These properties are due to the overlapping sp^2 hybrid orbital bonds which delocalize over the graphene sheet [85]. Despite these positive attributes, graphene is also characterised by a zero bandgap, which makes it impractical for use in transistor devices as described in this thesis.

2D Transition Metal Dichalcogenides (TMD) materials show more potential for use in transistors and related devices. TMDs exhibit a bandgap which is tunable with thickness, along with other distinctive electrical and optical properties which arise from quantum confinement and surface effects as the materials transition from 3D to 2D [86]. TMDs also offer huge variation in composition in the form MX_2 (where M represents the transition metal and X represents a chalcogen), each one offering its own unique properties. Some

of the most studied examples of TMDs in the literature include MoS₂ [87–90] and PtSe₂ [91–94].

The weakness of 2D materials stems from the difficulty in performing large area growth. Most studies consist of growth of the material with subsequent transfer to another substrate for further studies [95]. To truly become a viable option for use in consumer electronics, this difficulty must be addressed.

1.3 Current State of the Art

To effectively assess the advancements and contributions made through the work presented in this thesis, it is necessary to compare the results to results from the literature. As there is not a large abundance of work on polycrystalline/amorphous III-V materials in the literature, there are crystalline III-V materials and other low temperature grown materials included in this collection of data from the literature. This should be considered when directly comparing the materials to each other.

1.3.1 III-V Transistors

The two III-V materials implemented in this thesis are InAs and GaSb. The native hole concentration in GaSb is found to originate from anti-site defects

[96]. InAs exhibits a high electron density due to a 2D electron gas present on the surface of the semiconductor [97]. This 2D electron gas is different to the normal semiconductor considered in traditional semiconductor physics. Therefore, it is useful to know that there are no fundamental problems with producing functional InAs based transistors. Tables 1.2 and 1.3 present results for III-V based transistors, including InAs and GaSb, showing that functional devices using these materials are fundamentally achievable. Many different types of transistor type are demonstrated, including Nanowire (NW) Field Effect Transistor (FET), Semiconductor-on-Insulator (XOI) FET, Tunneling Field Effect Transistor (TFET), buried channel structures, Quantum Well (QW) devices, and finFETs.

Tables 1.2 and 1.3 shows that the performance and characteristics of transistors fabricated using III-V materials are widely variable, depending strongly on the type of transistor architecture and the substrate. It is clear that in general, both the ON- and OFF-current densities can be improved upon. In particular, the p -type III-V transistors in Table 1.3 are not very impressive in I_{ON}/I_{OFF} values. This is expected, as in most technologies, the p -type components lag the development of their n -type counterparts. It is important to emphasise that the III-V channel materials presented in Tables 1.2 and 1.3 are crystalline materials with growth temperature typically $>500^{\circ}\text{C}$.

III-V Material	I_{ON} ($\mu A/\mu m$)	I_{OFF} ($\mu A/\mu m$)	I_{ON}/I_{OFF}	SS (mV/dec)	Transistor Type	Growth Substrate	Year	Institution	Reference
InAs	33	0.002	1×10^4	-	NW FET	AlGaSb	2018	Kyung Hee University	[98]
InAs	60	0.002	1×10^4	72	XOI FET	GaSb	2013	University of California, Berkley	[99]
InAs	0.2	0.001	100	190	XOI TFET	AlGaSb	2011	University of California, Berkley	[100]
InAs/ In-GaAs	330	0.1	1000	85	Vertical MOSFET	Si	2017	Lund University	[101]
InAs/ In-GaAsSb/ GaSb	10.3	0.001	1×10^4	48	NW TFET	InAs	2017	Lund University	[102]
InAs	30	0.003	1×10^4	126	NW n FET	GeOI	2015	National University of Singapore	[103]
InGaAs	50	5×10^{-5}	1×10^6	86	TFET	InP	2010	University of Texas	[104]
InGaAs	0.7	9×10^{-7}	1×10^6	57	TFET	InP	2017	University of Tokyo	[105]
GaAsSb/ InGaAs	0.002	3×10^{-6}	1000	-	Vertical TFET	InP	2019	University of Tokyo	[106]
InGaAs/ InAs/ InGaAs	6	6×10^{-6}	1×10^6	107	Buried Channel MOSFET	InP	2011	University of Texas	[107]
InP	0.02	5×10^{-8}	4×10^6	70	MOSFET	InP	2019	University of California	[108]
InAs	0.6	80	133	90	MOSFET	InP	2018	University of California	[109]
$In_{0.7}Ga_{0.3}As$	10	0.001	1×10^4	114	QW	InP	2015	Penn State University	[110]
InAs	10	5×10^{-4}	2×10^4	87	QW	InP	2015	Penn State University	[110]
InAs	10	7×10^{-4}	1.5×10^4	92	Dual QW	InP	2015	Penn State University	[110]
InAs	40	0.02	2000	148	FinFET	InAs	2016	TSMC, Leuven	[111]
InAs	-	-	2×10^4	84	nMOS	SiO_2	2012	University of California, Berkley	[112]
InAs	0.2	0.002	100	-	nMOSFET	InAs	2014	University of Tokyo	[113]

Table 1.2: Examples of functional n -type III-V based transistors from the literature.

III-V Material	I_{ON} ($\mu A/\mu m$)	I_{OFF} ($\mu A/\mu m$)	I_{ON}/I_{OFF}	SS (mV/dec)	Transistor Type	Growth Substrate	Year	Institution	Reference
GaSb	20	0.03	700	224	NW MOS-FET	InAs	2020	Lund University	[114]
InGaSb	100	2	50	260	finFET	GaAs	2017	MIT	[115]
GaSb	10	0.002	5000	188	NW <i>p</i> FET	GeOI	2015	National University of Singapore	[103]
GaSb	20	0.02	1000	-	pMOSFET	GaSb	2014	National Tsing Hua University	[116]
InGaSb	-	-	100	156	pMOS	SiO ₂	2012	University of California, Berkley	[112]
GaSb	0.2	0.002	100	-	pMOSFET	InAs	2014	The University of Tokyo	[113]

Table 1.3: Examples of functional *p*-type III-V based transistors from the literature.

1.3.2 Mobility of Low Temperature Grown Materials

Mobility is one of the most important parameters of a semiconducting material, as it determines how it will perform in a field effect device. A high mobility increases the drive current and can also be utilised to reduce the supply voltage to operate at lower fields without compromising on performance [117]. This in turn would reduce the power dissipation [8].

Growth of high quality semiconducting materials with high mobility is usually performed at temperatures which are incompatible with the low thermal budget necessary for BEOL integration. The BEOL thermal budget limit is typically below 550°C [118]. This is also due to optimization of the carrier concentration which involves doping and dopant activation. Figures 1.9 and 1.10 show the hole and electron room temperature Hall mobility vs their max-

imum temperature experienced during the growth process. In later chapters where the mobility of the studied materials are extracted, they will be added to these graphs as benchmarking. It should be remembered when looking at these graphs that the films are grown on different substrates and to different thicknesses than the samples examined in this thesis. Any of these differences will be discussed in more detail when comparing to the films in this thesis.

It is clear from these graphs that low temperature grown *p*-type materials suffer from lower carrier mobilities than their *n*-type counterparts. It is noted from these graphs that there are very few reports of low temperature grown polycrystalline III-V materials. There are two reports of InAs and poly In-GaAs, and the single paper on poly GaSb was grown around 750°C; however, none of these papers fabricate devices using the films. The combination of relatively high electron and hole mobility combined with the very limited published literature was the motivation for this study exploring the electron and hole mobility in low temperature grown III-V materials on amorphous substrates, and taking the grown films through to full device structures.

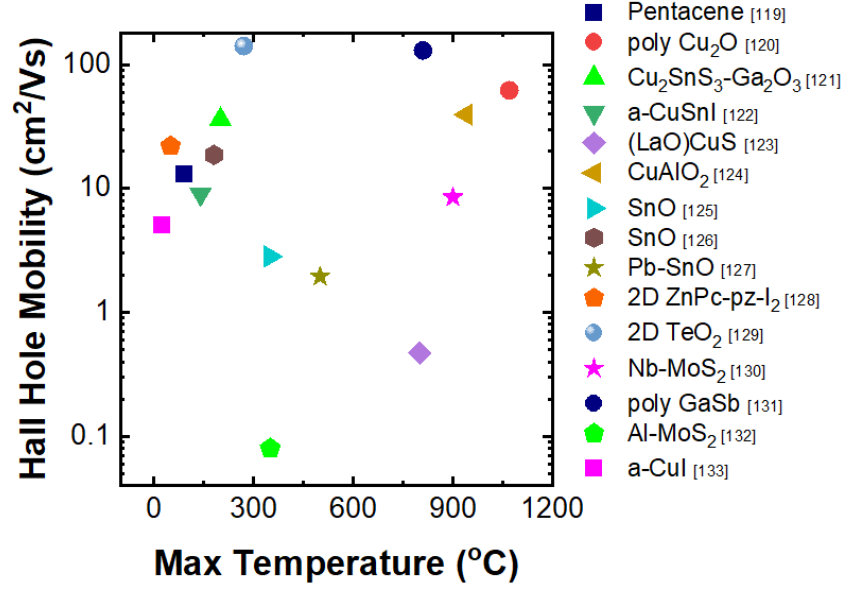


Figure 1.9: Hole hall mobility vs maximum fabrication temperature [119–133].

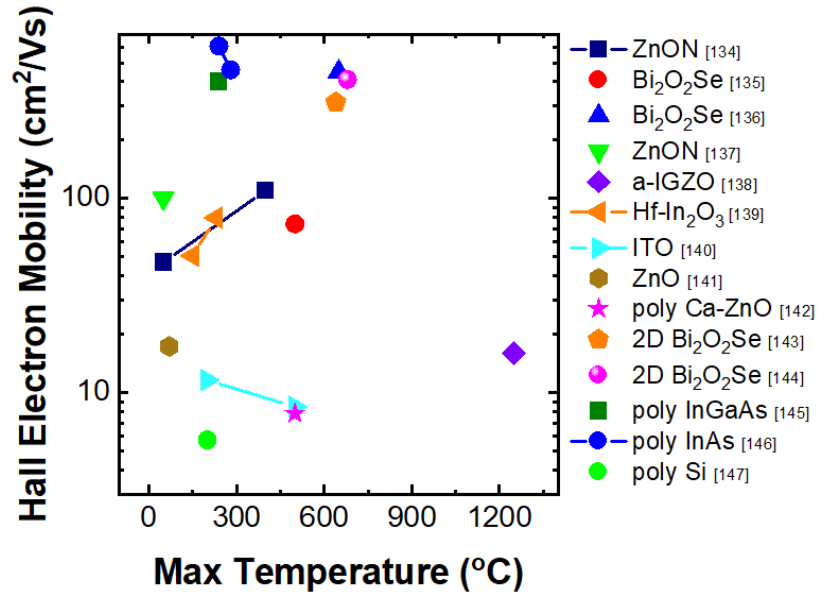


Figure 1.10: Electron hall mobility vs maximum fabrication temperature [134–147].

1.4 Thesis Outline

This thesis covers analysis and characterisation of III-V thin films, along with fabrication and analysis of transistor test devices.

Chapter 2 covers the properties of polycrystalline InAs thin films grown by Metalorganic Vapour Phase Epitaxy (MOVPE) on glass and Si/SiO₂ substrates, where the growth temperature is 475°C. This includes a study of the microstructure of the films using Transmission Electron Microscopy (TEM) and an investigation of the electronic properties of the InAs thin films using current-voltage analysis and variable temperature Hall effect measurements.

Chapter 3 covers the fabrication and analysis of transistor test devices fabricated using the InAs films studied in Chapter 2. Device fabrication process is described and current-voltage measurement results are presented. The factors limiting the I_{ON}/I_{OFF} ratio are investigated, and advice for future implementation of this material into device structures is given.

Chapter 4 covers the properties of polycrystalline and amorphous GaSb thin films grown by MOVPE on Si/SiO₂ and Semi-Insulating (SI) GaAs substrates at 475°C. The structural properties of the films are studied through Scanning Electron Microscopy (SEM) and XTEM analysis, while the transport properties are investigated through Hall effect measurements at room and variable

temperature. Level of crystallinity is determined through X-Ray Diffraction (XRD) measurements.

Chapter 5 covers the fabrication and analysis of transistor test devices fabricated using the polycrystalline and amorphous GaSb films studied in Chapter 4. The fabrication process steps are described and the resulting devices are measured and their results presented.

Bibliography

- [1] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, “Design of ion-implanted MOSFET’s with very small physical dimensions,” *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, 1974.
- [2] M. Bohr, “A 30 year retrospective on Dennard’s MOSFET scaling paper,” *IEEE Solid-State Circuits Society Newsletter*, vol. 12, no. 1, pp. 11–13, 2007.
- [3] I. Ferain, C. A. Colinge, and J.-P. Colinge, “Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors,” *Nature*, vol. 479, no. 7373, pp. 310–316, 2011.
- [4] R. Chau, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, “Integrated nanoelectronics for the future,” *Nature materials*, vol. 6, no. 11, pp. 810–812, 2007.
- [5] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, “Strained Si, SiGe, and Ge channels for high-mobility

-
- metal-oxide-semiconductor field-effect transistors,” *Journal of applied physics*, vol. 97, no. 1, p. 1, 2005.
- [6] E. Gusev, D. A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P. Jamison, D. Neumayer, *et al.*, “Ultrathin high- κ gate stacks for advanced CMOS devices,” in *International Electron Devices Meeting. Technical Digest (Cat. No. 01CH37224)*, pp. 20–1, IEEE, 2001.
- [7] T. Dutta, Q. Rafhay, R. Clerc, J. Lacord, S. Monfray, G. Pananakakis, F. Boeuf, and G. Ghibaudo, “Origins of the short channel effects increase in III-V nMOSFET technologies,” in *2012 13th International Conference on Ultimate Integration on Silicon (ULIS)*, pp. 25–28, IEEE, 2012.
- [8] D. J. Frank, “Power-constrained CMOS scaling limits,” *IBM Journal of Research and Development*, vol. 46, no. 2.3, pp. 235–244, 2002.
- [9] E. J. Nowak, “Maintaining the benefits of CMOS scaling when scaling bogs down,” *IBM Journal of Research and Development*, vol. 46, no. 2.3, pp. 169–180, 2002.
- [10] J. Von Neumann, “First draft of a report on the EDVAC,” *IEEE Annals of the History of Computing*, vol. 15, no. 4, pp. 27–75, 1993.
- [11] L. Brunet, P. Batude, C. Fenouillet-Béranger, P. Besombes, L. Hortemel, F. Ponthenier, B. Previtali, C. Tabone, A. Royer, C. Agrafeil,

- et al.*, “First demonstration of a CMOS over CMOS 3D VLSI Cool-Cube™ integration on 300mm wafers,” in *2016 IEEE Symposium on VLSI Technology*, pp. 1–2, IEEE, 2016.
- [12] V. Deshpande, H. Hahn, E. O’Connor, Y. Baumgartner, M. Sousa, D. Caimi, H. Boutry, J. Widiez, L. Brévard, C. Le Royer, *et al.*, “First demonstration of 3D SRAM through 3D monolithic integration of In-GaAs *n*-FinFETs on FDSOI Si CMOS with inter-layer contacts,” in *2017 Symposium on VLSI Technology*, pp. T74–T75, IEEE, 2017.
- [13] T. Dalgaty, M. Payvand, F. Moro, D. R. Ly, F. Pebay-Peyroula, J. Casas, G. Indiveri, and E. Vianello, “Hybrid neuromorphic circuits exploiting non-conventional properties of RRAM for massively parallel local plasticity mechanisms,” *APL Materials*, vol. 7, no. 8, p. 081125, 2019.
- [14] S. Datta, S. Dutta, B. Grisafe, J. Smith, S. Srinivasa, and H. Ye, “Back-end-of-line compatible transistors for monolithic 3-D integration,” *IEEE Micro*, vol. 39, no. 6, pp. 8–15, 2019.
- [15] J. A. Del Alamo, “Nanometre-scale electronics with III–V compound semiconductors,” *Nature*, vol. 479, no. 7373, pp. 317–323, 2011.
- [16] K. Takei, M. Madsen, H. Fang, R. Kapadia, S. Chuang, H. S. Kim, C.-H. Liu, E. Plis, J. Nah, S. Krishna, *et al.*, “Nanoscale InGaSb het-

- erostructure membranes on Si substrates for high hole mobility transistors,” *Nano letters*, vol. 12, no. 4, pp. 2060–2066, 2012.
- [17] T. Gougousi, “Atomic layer deposition of high- κ dielectrics on III–V semiconductor surfaces,” *Progress in Crystal Growth and Characterization of Materials*, vol. 62, no. 4, pp. 1–21, 2016.
- [18] G. Harbeke, *Polycrystalline Semiconductors: Physical Properties and Applications: Proceedings of the International School of Materials Science and Technology at the Ettore Majorana Centre, Erice, Italy, July 1–15, 1984*, vol. 57. Springer Science & Business Media, 2012.
- [19] V. Šnejdar and J. Jerhot, “Electrical conductivity of polycrystalline semiconductors,” *Thin Solid Films*, vol. 37, no. 3, pp. 303–316, 1976.
- [20] F. Greuter and G. Blatter, “Electrical properties of grain boundaries in polycrystalline compound semiconductors,” *Semiconductor Science and Technology*, vol. 5, no. 2, p. 111, 1990.
- [21] T.-C. Chang, Y.-C. Tsao, P.-H. Chen, M.-C. Tai, S.-P. Huang, W.-C. Su, and G.-F. Chen, “Flexible low-temperature polycrystalline silicon thin-film transistors,” *Materials Today Advances*, vol. 5, p. 100040, 2020.
- [22] L. Wang, S. Chen, W. Li, K. Wang, Z. Lou, and G. Shen, “Grain-boundary-induced drastic sensing performance enhancement

-
- of polycrystalline-microwire printed gas sensors,” *Advanced Materials*, vol. 31, no. 4, p. 1804583, 2019.
- [23] G. Qin, H.-C. Yuan, H. Yang, W. Zhou, and Z. Ma, “High-performance flexible thin-film transistors fabricated using print-transferrable polycrystalline silicon membranes on a plastic substrate,” *Semiconductor Science and Technology*, vol. 26, no. 2, p. 025005, 2010.
- [24] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, “Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors,” *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.
- [25] J. Singh and K. Shimakawa, “Advances in amorphous semiconductors,” pp. 1–20, 2003.
- [26] R. Chau, S. Datta, and A. Majumdar, “Opportunities and challenges of III-V nanoelectronics for future high-speed, low-power logic applications,” in *IEEE Compound Semiconductor Integrated Circuit Symposium, 2005.*, pp. 17–20, IEEE, 2005.
- [27] M. Heyns and W. Tsai, “Ultimate scaling of CMOS logic devices with Ge and III–V materials,” *MRS bulletin*, vol. 34, no. 7, pp. 485–492, 2009.
- [28] Y. Furukawa, H. Yonezu, K. Ojima, K. Samonji, Y. Fujimoto, K. Momose, and K. Aiki, “Control of N content of GaPN grown by molecular

- beam epitaxy and growth of GaPN lattice matched to Si (100) substrate,” *Japanese journal of applied physics*, vol. 41, no. 2R, p. 528, 2002.
- [29] H. Yonezu, “Control of structural defects in group III–V–N alloys grown on Si,” *Semiconductor science and technology*, vol. 17, no. 8, p. 762, 2002.
- [30] V. Yang, M. Groenert, C. Leitz, A. Pitera, M. Currie, and E. A. Fitzgerald, “Crack formation in GaAs heteroepitaxial films on Si and SiGe virtual substrates,” *Journal of applied physics*, vol. 93, no. 7, pp. 3859–3865, 2003.
- [31] M. Feifel, J. Ohlmann, J. Benick, M. Hermle, J. Belz, A. Beyer, K. Volz, T. Hannappel, A. W. Bett, D. Lackner, *et al.*, “Direct growth of III–V/silicon triple-junction solar cells with 19.7% efficiency,” *IEEE Journal of Photovoltaics*, vol. 8, no. 6, pp. 1590–1595, 2018.
- [32] J. Li, J. Lin, and H. Jiang, “Growth of III-nitride photonic structures on large area silicon substrates,” *Applied physics letters*, vol. 88, no. 17, p. 171909, 2006.
- [33] K. W. Ng, W. S. Ko, T.-T. D. Tran, R. Chen, M. V. Nazarenko, F. Lu, V. G. Dubrovskii, M. Kamp, A. Forchel, and C. J. Chang-Hasnain, “Unconventional growth mechanism for monolithic integration of III–V on silicon,” *ACS nano*, vol. 7, no. 1, pp. 100–107, 2013.

-
- [34] M. Moewe, L. C. Chuang, S. Crankshaw, K. W. Ng, and C. Chang-Hasnain, “Core-shell InGaAs/GaAs quantum well nanoneedles grown on silicon with silicon-transparent emission,” *Optics express*, vol. 17, no. 10, pp. 7831–7836, 2009.
- [35] M. T. H. Ha, S. H. Huynh, H. B. Do, T. A. Nguyen, Q. H. Luc, C. T. Lee, and E. Y. Chang, “Entirely relaxed lattice-mismatched GaSb/GaAs/Si (001) heterostructure grown via metalorganic chemical vapor deposition,” *Applied Physics Express*, vol. 11, no. 5, p. 051202, 2018.
- [36] S. H. Vajargah, S. Ghanad-Tavakoli, J. Preston, R. Kleiman, and G. Botton, “Growth mechanisms of GaSb heteroepitaxial films on Si with an AlSb buffer layer,” *Journal of Applied Physics*, vol. 114, no. 11, p. 113101, 2013.
- [37] K. Akahane, N. Yamamoto, S.-i. Gozu, and N. Ohtani, “Heteroepitaxial growth of GaSb on Si (0 0 1) substrates,” *Journal of crystal growth*, vol. 264, no. 1-3, pp. 21–25, 2004.
- [38] K. H. Yoen, J. D. Song, E. H. Lee, H. J. Jang, M. H. Bae, J. Y. Kim, I. K. Han, and W. J. Choi, “The growth of GaSb/Al_{0.33}Ga_{0.67}Sb MQW on *n*-silicon (1 0 0) with Al_{0.66}Ga_{0.34}Sb/AlSb SPS layers,” *Materials Research Bulletin*, vol. 57, pp. 152–155, 2014.
- [39] W. Spicer, I. Lindau, P. Skeath, and C. Su, “Unified defect model and

- beyond,” *Journal of Vacuum Science and Technology*, vol. 17, no. 5, pp. 1019–1027, 1980.
- [40] N. Barbouth, Y. Berthier, J. Oudar, J.-M. Moison, and M. Bensoussan, “The first steps of the sulfurization of III–V compounds,” *Journal of The Electrochemical Society*, vol. 133, no. 8, p. 1663, 1986.
- [41] F. Capasso and G. Williams, “A proposed hydrogenation/nitridization passivation mechanism for GaAs and other III–V semiconductor devices, including InGaAs long wavelength photodetectors,” *Journal of The Electrochemical Society*, vol. 129, no. 4, p. 821, 1982.
- [42] T. Hoshii, S. Lee, R. Suzuki, N. Taoka, M. Yokoyama, H. Yamada, M. Hata, T. Yasuda, M. Takenaka, and S. Takagi, “Reduction in interface state density of $\text{Al}_2\text{O}_3/\text{InGaAs}$ metal-oxide-semiconductor interfaces by InGaAs surface nitridation,” *Journal of Applied Physics*, vol. 112, no. 7, p. 073702, 2012.
- [43] T. Hoshii, M. Yokoyama, H. Yamada, M. Hata, T. Yasuda, M. Takenaka, and S. Takagi, “Impact of InGaAs surface nitridation on interface properties of InGaAs metal-oxide-semiconductor capacitors using electron cyclotron resonance plasma sputtering SiO_2 ,” *Applied Physics Letters*, vol. 97, no. 13, p. 132102, 2010.
- [44] J. Lin, S. Lee, H.-J. Oh, W. Yang, G. Lo, D. Kwong, and D. Chi, “Plasma PH_3 -passivated high mobility inversion InGaAs MOSFET fab-

- ricated with self-aligned gate-first process and HfO_2/TaN gate stack,” in *2008 IEEE International Electron Devices Meeting*, pp. 1–4, IEEE, 2008.
- [45] V. Kesler, V. Seleznev, A. Kovchavtsev, and A. Guzev, “Composition, morphology and surface recombination rate of HCl –isopropanol treated and vacuum annealed $\text{InAs}(1\ 1\ 1)\text{a}$ surfaces,” *Applied surface science*, vol. 256, no. 14, pp. 4626–4632, 2010.
- [46] S. A. Jewett and A. Ivanisevic, “Wet-chemical passivation of InAs : toward surfaces with high stability and low toxicity,” *Accounts of chemical research*, vol. 45, no. 9, pp. 1451–1459, 2012.
- [47] R. D. Long, É. O’Connor, S. B. Newcomb, S. Monaghan, K. Cherkaoui, P. Casey, G. Hughes, K. K. Thomas, F. Chalvet, I. M. Povey, *et al.*, “Structural analysis, elemental profiling, and electrical characterization of HfO_2 thin films deposited on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces by atomic layer deposition,” *Journal of Applied Physics*, vol. 106, no. 8, p. 084508, 2009.
- [48] É. O’Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, *et al.*, “A systematic study of $(\text{NH}_4)_2\text{S}$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ system for n -type and p -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial layers,” *Journal of Applied Physics*, vol. 109, no. 2, p. 024101, 2011.

-
- [49] A. Gin, Y. Wei, A. Hood, A. Bajowala, V. Yazdanpanah, M. Razeghi, and M. Tidrow, "Ammonium sulfide passivation of type-II InAs/GaSb superlattice photodiodes," *Applied physics letters*, vol. 84, no. 12, pp. 2037–2039, 2004.
- [50] N. Eassa, D. Murape, J. Neethling, R. Betz, E. Coetsee, H. Swart, A. Venter, and J. Botha, "Chalcogen based treatment of InAs with $(\text{NH}_4)_2\text{S}/(\text{NH}_4)_2\text{SO}_4$," *Surface science*, vol. 605, no. 11-12, pp. 994–999, 2011.
- [51] U. Peralagu, I. M. Povey, P. Carolan, J. Lin, R. Contreras-Guerrero, R. Droopad, P. K. Hurley, and I. G. Thayne, "Electrical and physical characterization of the $\text{Al}_2\text{O}_3/p\text{-GaSb}$ interface for 1%, 5%, 10%, and 22% $(\text{NH}_4)_2\text{S}$ surface treatments," *Applied Physics Letters*, vol. 105, no. 16, p. 162907, 2014.
- [52] N. Goel, P. Majhi, C. Chui, W. Tsai, D. Choi, and J. Harris, "InGaAs metal-oxide-semiconductor capacitors with HfO_2 gate dielectric grown by atomic-layer deposition," *Applied physics letters*, vol. 89, no. 16, p. 163517, 2006.
- [53] É. O'Connor, R. D. Long, K. Cherkaoui, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, P. K. Hurley, B. Brennan, G. Hughes, *et al.*, "In situ H_2S passivation of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ metal-oxide-semiconductor capacitors with atomic-layer deposited HfO_2 gate dielectric," *Applied Physics Letters*, vol. 92, no. 2, p. 022902, 2008.

- [54] N. Yoshida, S. Chichibu, T. Akane, M. Totsuka, H. Uji, S. Matsumoto, and H. Higuchi, “Surface passivation of GaAs using ArF excimer laser in a H₂S gas ambient,” *Applied physics letters*, vol. 63, no. 22, pp. 3035–3037, 1993.
- [55] J. Herman and F. Terry Jr, “Hydrogen sulfide plasma passivation of gallium arsenide,” *Applied physics letters*, vol. 60, no. 6, pp. 716–717, 1992.
- [56] A. Kapila, X. Si, and V. Malhotra, “Electrical properties of the SiN_x/InP interface passivated using H₂S,” *Applied physics letters*, vol. 62, no. 18, pp. 2259–2261, 1993.
- [57] S. Klejna and S. D. Elliott, “First-principles modeling of the “clean-up” of native oxides during atomic layer deposition onto III–V substrates,” *The Journal of Physical Chemistry C*, vol. 116, no. 1, pp. 643–654, 2012.
- [58] M. Milojevic, C. Hinkle, F. Aguirre-Tostado, H. Kim, E. Vogel, J. Kim, and R. Wallace, “Half-cycle atomic layer deposition reaction studies of Al₂O₃ on (NH₄)₂S passivated GaAs (100) surfaces,” *Applied Physics Letters*, vol. 93, no. 25, p. 252905, 2008.
- [59] M. Tallarida, C. Adelman, A. Delabie, S. Van Elshocht, M. Caymax, and D. Schmei er, “Surface chemistry and Fermi level movement dur-

- ing the self-cleaning of GaAs by trimethyl-aluminum,” *Applied Physics Letters*, vol. 99, no. 4, p. 042906, 2011.
- [60] B. Brennan, H. Dong, D. Zhernokletov, J. Kim, and R. M. Wallace, “Surface and interfacial reaction study of half cycle atomic layer deposited Al_2O_3 on chemically treated InP surfaces,” *Applied Physics Express*, vol. 4, no. 12, p. 125701, 2011.
- [61] S. Monaghan, A. O’Mahony, K. Cherkaoui, É. O’Connor, I. Povey, M. Nolan, D. O’Connell, M. Pemble, P. Hurley, G. Provenzano, *et al.*, “Electrical analysis of three-stage passivated $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors with varying HfO_2 thicknesses and incorporating an Al_2O_3 interface control layer,” *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 29, no. 1, p. 01A807, 2011.
- [62] M. M. Frank, “ HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition,” *Applied Physics Letters*, vol. 86, no. 15.
- [63] W.-J. Hsueh, C.-Y. Chen, C.-M. Chang, J.-I. Chyi, and M.-L. Huang, “Effects of GaSb surface preparation on the characteristics of $\text{HfO}_2/\text{Al}_2\text{O}_3/\text{GaSb}$ metal-oxide-semiconductor capacitors prepared by atomic layer deposition,” *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 35, no. 1, p. 01B106, 2017.
- [64] L.-f. Wu, Y.-m. Zhang, H.-l. Lu, and Y.-m. Zhang, “Interfacial and elec-

- trical characterization of $\text{HfO}_2/\text{Al}_2\text{O}_3/\text{InAlAs}$ structures,” *Japanese Journal of Applied Physics*, vol. 54, no. 11, p. 110303, 2015.
- [65] T. Nishimura, T. Okazawa, Y. Hoshino, Y. Kido, K. Iwamoto, K. Tominaga, T. Nabatame, T. Yasuda, and A. Toriumi, “Atomic scale characterization of $\text{HfO}_2/\text{Al}_2\text{O}_3$ thin films grown on nitrated and oxidized Si substrates,” *Journal of applied physics*, vol. 96, no. 11, pp. 6113–6119, 2004.
- [66] J.-P. Colinge, A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, and P. Razavi, “Junctionless nanowire transistor (JNT): Properties and design guidelines,” *Solid-State Electronics*, vol. 65, pp. 33–37, 2011.
- [67] E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, “Border traps in $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (100) gate stacks and their passivation by hydrogen anneals,” *Applied physics letters*, vol. 96, no. 1, p. 012906, 2010.
- [68] V. Djara, T. O’Regan, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O’Connor, I. Povey, D. O’Connell, M. Pemble, and P. Hurley, “Electrically active interface defects in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system,” *Microelectronic engineering*, vol. 109, pp. 182–188, 2013.
- [69] Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. Rodwell, and Y. Taur, “A distributed model for border

-
- traps in Al_2O_3 - InGaAs MOS devices,” *IEEE Electron Device Letters*, vol. 32, no. 4, pp. 485–487, 2011.
- [70] M. Si, J. J. Gu, X. Wang, J. Shao, X. Li, M. J. Manfra, R. G. Gordon, and P. D. Ye, “Effects of forming gas anneal on ultrathin InGaAs nanowire metal-oxide-semiconductor field-effect transistors,” *Applied Physics Letters*, vol. 102, no. 9, p. 093505, 2013.
- [71] B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle, and P. C. McIntyre, “Origin and passivation of fixed charge in atomic layer deposited aluminum oxide gate insulators on chemically treated InGaAs substrates,” *Applied physics letters*, vol. 96, no. 15, p. 152908, 2010.
- [72] A. Alian, C. Merckling, G. Brammertz, M. Meuris, M. Heyns, and K. De Meyer, “InGaAs MOS transistors fabricated through a digital-etch gate-recess process and the influence of forming gas anneal on their electrical behavior,” *ECS Journal of Solid State Science and Technology*, vol. 1, no. 6, p. P310, 2012.
- [73] V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O’Connor, I. M. Povey, D. O’Connell, M. E. Pemble, and P. K. Hurley, “Impact of forming gas annealing on the performance of surface-channel $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs with an ALD Al_2O_3 gate dielectric,” *IEEE transactions on electron devices*, vol. 59, no. 4, p. 1084, 2012.

- [74] K. Tang, R. Winter, L. Zhang, R. Droopad, M. Eizenberg, and P. C. McIntyre, “Border trap reduction in $\text{Al}_2\text{O}_3/\text{InGaAs}$ gate stacks,” *Applied Physics Letters*, vol. 107, no. 20, p. 202102, 2015.
- [75] Z. Zhu, J. Svensson, A. Jönsson, and L.-E. Wernersson, “Performance enhancement of GaSb vertical nanowire p -type MOSFETs on Si by rapid thermal annealing,” *Nanotechnology*, vol. 33, no. 7, p. 075202, 2021.
- [76] A. Nainani, T. Irisawa, Z. Yuan, B. R. Bennett, J. B. Boos, Y. Nishi, and K. C. Saraswat, “Optimization of the $\text{Al}_2\text{O}_3/\text{GaSb}$ interface and a high-mobility GaSb pMOSFET,” *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3407–3415, 2011.
- [77] Z. Yuan, A. Kumar, C.-Y. Chen, A. Nainani, B. R. Bennett, J. B. Boos, and K. C. Saraswat, “Antimonide-based heterostructure p -channel MOSFETs with Ni-alloy source/drain,” *IEEE electron device letters*, vol. 34, no. 11, pp. 1367–1369, 2013.
- [78] X. Zhao, C. Heidelberger, E. Fitzgerald, W. Lu, A. Vardi, and J. Del Alamo, “Sub-10 nm diameter InGaAs vertical nanowire MOSFETs,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, pp. 17–2, IEEE, 2017.
- [79] V. Djara, L. Czornomaz, V. Deshpande, N. Daix, E. Uccelli, D. Caimi, M. Sousa, and J. Fompeyrine, “Tri-gate InGaAs-OI junctionless FETs

- with PE-ALD Al_2O_3 gate dielectric and H_2/Ar anneal,” *Solid-State Electronics*, vol. 115, pp. 103–108, 2016.
- [80] H. Trinh, E. Y. Chang, P.-W. Wu, Y. Wong, C. Chang, Y. Hsieh, C. Yu, H. Nguyen, Y. Lin, K. Lin, *et al.*, “The influences of surface treatment and gas annealing conditions on the inversion behaviors of the atomic-layer-deposition $\text{Al}_2\text{O}_3/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor capacitor,” *Applied Physics Letters*, vol. 97, no. 4, p. 042903, 2010.
- [81] T.-W. Kim, H.-M. Kwon, S. H. Shin, C.-S. Shin, W.-K. Park, E. Chiu, M. Rivera, J. I. Lew, D. Veksler, T. Orzali, *et al.*, “Impact of H_2 high-pressure annealing onto InGaAs quantum-well metal-oxide-semiconductor field-effect transistors with $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate-stack,” *IEEE Electron Device Letters*, vol. 36, no. 7, pp. 672–674, 2015.
- [82] L. Czornomaz, M. El Kazzi, M. Hopstaken, D. Caimi, P. Mächler, C. Rossel, M. Bjoerk, C. Marchiori, H. Siegwart, and J. Fompeyrine, “CMOS compatible self-aligned S/D regions for implant-free InGaAs MOSFETs,” *Solid-State Electronics*, vol. 74, pp. 71–76, 2012.
- [83] A. Gupta, T. Sakthivel, and S. Seal, “Recent development in 2d materials beyond graphene,” *Progress in Materials Science*, vol. 73, pp. 44–126, 2015.
- [84] J. Jiang, J. H. Chu, and K. Banerjee, “Cmos-compatible doped-multilayer-graphene interconnects for next-generation vlsi,” in *2018*

-
- IEEE International Electron Devices Meeting (IEDM)*, pp. 34–5, IEEE, 2018.
- [85] D. G. Papageorgiou, I. A. Kinloch, and R. J. Young, “Mechanical properties of graphene and graphene-based nanocomposites,” *Progress in materials science*, vol. 90, pp. 75–127, 2017.
- [86] W. Choi, N. Choudhary, G. H. Han, J. Park, D. Akinwande, and Y. H. Lee, “Recent development of two-dimensional transition metal dichalcogenides and their applications,” *Materials Today*, vol. 20, no. 3, pp. 116–130, 2017.
- [87] R. Yang, H. Li, K. K. Smithe, T. R. Kim, K. Okabe, E. Pop, J. A. Fan, and H.-S. P. Wong, “2d molybdenum disulfide (mos 2) transistors driving rrams with 1t1r configuration,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, pp. 19–5, IEEE, 2017.
- [88] J. Zheng, X. Yan, Z. Lu, H. Qiu, G. Xu, X. Zhou, P. Wang, X. Pan, K. Liu, and L. Jiao, “High-mobility multilayered mos2 flakes with low contact resistance grown by chemical vapor deposition,” *Advanced Materials*, vol. 29, no. 13, p. 1604540, 2017.
- [89] M. Mattinen, F. Gity, E. Coleman, J. F. Vonk, M. A. Verheijen, R. Duffy, W. M. Kessels, and A. A. Bol, “Atomic layer deposition of large-area polycrystalline transition metal dichalcogenides from 100° c

- through control of plasma chemistry,” *Chemistry of Materials*, vol. 34, no. 16, pp. 7280–7292, 2022.
- [90] J. Lin, S. Monaghan, N. Sakhuja, F. Gity, R. K. Jha, E. M. Coleman, J. Connolly, C. P. Cullen, L. A. Walsh, T. Mannarino, *et al.*, “Large-area growth of mos2 at temperatures compatible with integrating back-end-of-line functionality,” *2D Materials*, vol. 8, no. 2, p. 025008, 2020.
- [91] L. Ansari, S. Monaghan, N. McEvoy, C. Ó. Coileáin, C. P. Cullen, J. Lin, R. Siris, T. Stimpel-Lindner, K. F. Burke, G. Mirabelli, *et al.*, “Quantum confinement-induced semimetal-to-semiconductor evolution in large-area ultra-thin ptse2 films grown at 400° c,” *npj 2D Materials and Applications*, vol. 3, no. 1, p. 33, 2019.
- [92] Y. Wang, L. Li, W. Yao, S. Song, J. Sun, J. Pan, X. Ren, C. Li, E. Okunishi, Y.-Q. Wang, *et al.*, “Monolayer ptse2, a new semiconducting transition-metal-dichalcogenide, epitaxially grown by direct selenization of pt,” *Nano letters*, vol. 15, no. 6, pp. 4013–4018, 2015.
- [93] Y. Zhao, J. Qiao, Z. Yu, P. Yu, K. Xu, S. P. Lau, W. Zhou, Z. Liu, X. Wang, W. Ji, *et al.*, “High-electron-mobility and air-stable 2d layered ptse2 fets,” *Advanced Materials*, vol. 29, no. 5, p. 1604230, 2017.
- [94] H. Xu, H. Zhang, Y. Liu, S. Zhang, Y. Sun, Z. Guo, Y. Sheng, X. Wang, C. Luo, X. Wu, *et al.*, “Controlled doping of wafer-scale ptse2 films

- for device application,” *Advanced Functional Materials*, vol. 29, no. 4, p. 1805614, 2019.
- [95] K. S. Novoselov, D. Jiang, F. Schedin, T. Booth, V. Khotkevich, S. Morozov, and A. K. Geim, “Two-dimensional atomic crystals,” *Proceedings of the National Academy of Sciences*, vol. 102, no. 30, pp. 10451–10453, 2005.
- [96] P. Dutta, H. Bhat, and V. Kumar, “The physics and technology of gallium antimonide: An emerging optoelectronic material,” *Journal of applied physics*, vol. 81, no. 9, pp. 5821–5870, 1997.
- [97] J. Weber, A. Janotti, and C. Van de Walle, “Intrinsic and extrinsic causes of electron accumulation layers on InAs surfaces,” *Applied Physics Letters*, vol. 97, no. 19, p. 192106, 2010.
- [98] S. H. Lee, S.-H. Shin, M. Madsen, K. Takei, J. Nah, and M. H. Lee, “A soft lithographic approach to fabricate InAs nanowire field-effect transistors,” *Scientific reports*, vol. 8, no. 1, pp. 1–6, 2018.
- [99] K. Takei, R. Kapadia, H. Fang, E. Plis, S. Krishna, and A. Javey, “High quality interfaces of InAs-on-insulator field-effect transistors with ZrO_2 gate dielectrics,” *Applied Physics Letters*, vol. 102, no. 15, p. 153513, 2013.
- [100] A. C. Ford, C. W. Yeung, S. Chuang, H. S. Kim, E. Plis, S. Krishna, C. Hu, and A. Javey, “Ultrathin body InAs tunneling field-effect

- transistors on Si substrates,” *Applied Physics Letters*, vol. 98, no. 11, p. 113105, 2011.
- [101] O.-P. Kilpi, J. Svensson, J. Wu, A. R. Persson, R. Wallenberg, E. Lind, and L.-E. Wernersson, “Vertical InAs/InGaAs heterostructure metal–oxide–semiconductor field-effect transistors on Si,” *Nano letters*, vol. 17, no. 10, pp. 6006–6010, 2017.
- [102] E. Memisevic, M. Hellenbrand, E. Lind, A. R. Persson, S. Sant, A. Schenk, J. Svensson, R. Wallenberg, and L.-E. Wernersson, “Individual defects in InAs/InGaAsSb/GaSb nanowire tunnel field-effect transistors operating below 60 mV/decade,” *Nano letters*, vol. 17, no. 7, pp. 4373–4380, 2017.
- [103] K.-H. Goh, K.-H. Tan, S. Yadav, S.-F. Yoon, G. Liang, X. Gong, Y.-C. Yeo, *et al.*, “Gate-all-around CMOS (InAs *n*-FET and GaSb *p*-FET) based on vertically-stacked nanowires on a Si platform, enabled by extremely-thin buffer layer technology and common gate stack and contact modules,” in *2015 IEEE International Electron Devices Meeting (IEDM)*, pp. 15–4, IEEE, 2015.
- [104] H. Zhao, Y. Chen, Y. Wang, F. Zhou, F. Xue, and J. Lee, “In_{0.7}Ga_{0.3}As tunneling field-effect transistors with an I_{on} of 50 $\mu\text{A}/\mu\text{m}$ and a sub-threshold swing of 86 mV/dec using HfO₂ gate oxide,” *IEEE Electron Device Letters*, vol. 31, no. 12, pp. 1392–1394, 2010.

- [105] D.-H. Ahn, S.-H. Yoon, M. Takenaka, and S. Takagi, “Effects of $\text{HfO}_2/\text{Al}_2\text{O}_3$ gate stacks on electrical performance of planar $\text{In}_x\text{Ga}_{1-x}\text{As}$ tunneling field-effect transistors,” *Applied Physics Express*, vol. 10, no. 8, p. 084201, 2017.
- [106] T. Gotow, M. Mitsuhashi, T. Hoshi, H. Sugiyama, M. Takenaka, and S. Takagi, “Performance enhancement of p - $\text{GaAs}_{0.51}\text{Sb}_{0.49}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ hetero-junction vertical tunneling field-effect transistors with abrupt source impurity profile,” *Journal of Applied Physics*, vol. 126, no. 21, p. 214502, 2019.
- [107] F. Xue, H. Zhao, Y.-T. Chen, Y. Wang, F. Zhou, and J. C. Lee, “InAs inserted InGaAs buried channel metal-oxide-semiconductor field-effect-transistors with atomic-layer-deposited gate dielectric,” *Applied Physics Letters*, vol. 98, no. 8, p. 082106, 2011.
- [108] H.-Y. Tseng and Y. Fang, “InP MOSFETs exhibiting record 70 mV/dec subthreshold swing,” in *2019 Device Research Conference (DRC)*, pp. 183–184, IEEE, 2019.
- [109] J. Wu, Y. Fang, B. Markman, H.-Y. Tseng, and M. J. Rodwell, “ $L_g=30\text{nm}$ InAs channel MOSFETs exhibiting $f_{\text{max}}=410\text{ GHz}$ and $f_t=357\text{GHz}$,” *IEEE Electron Device Letters*, vol. 39, no. 4, pp. 472–475, 2018.
- [110] A. V. Thathachary, N. Agrawal, K. Bhuwalka, M. Cantoro, Y. Heo,

- G. Lavallee, S. Maeda, and S. Datta, “Indium arsenide (InAs) single and dual quantum-well heterostructure FinFETs,” in *2015 Symposium on VLSI Technology (VLSI Technology)*, pp. T208–T209, IEEE, 2015.
- [111] R. Oxland, X. Li, S. Chang, S. Wang, T. Vasen, P. Ramvall, R. Contreras-Guerrero, J. Rojas-Ramirez, M. Holland, G. Doornbos, *et al.*, “InAs FinFETs with $H_{\text{fin}} = 20$ nm fabricated using a top-down etch process,” *IEEE Electron Device Letters*, vol. 37, no. 3, pp. 261–264, 2016.
- [112] J. Nah, H. Fang, C. Wang, K. Takei, M. H. Lee, E. Plis, S. Krishna, and A. Javey, “III–V complementary metal–oxide–semiconductor electronics on silicon substrates,” *Nano letters*, vol. 12, no. 7, pp. 3592–3595, 2012.
- [113] M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, “III–V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on Si,” in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*, pp. 1–2, IEEE, 2014.
- [114] A. Jönsson, J. Svensson, E. Lind, and L.-E. Wernersson, “Gate-length dependence of vertical GaSb nanowire p -MOSFETs on Si,” *IEEE Transactions on Electron Devices*, vol. 67, no. 10, pp. 4118–4122, 2020.
- [115] W. Lu, I. Roh, D.-M. Geum, S.-H. Kim, J. Song, L. Kong, and J. A. del Alamo, “10-nm fin-width InGaSb p -channel self-aligned FinFETs

- using antimonide-compatible digital etch,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, pp. 17–7, IEEE, 2017.
- [116] R. Chu, T. Chiang, W. Hsueh, K. Chen, K. Lin, G. Brown, J. Chyi, J. Kwo, and M. Hong, “Passivation of GaSb using molecular beam epitaxy Y_2O_3 to achieve low interfacial trap density and high-performance self-aligned inversion-channel p-metal-oxide-semiconductor field-effect-transistors,” *Applied Physics Letters*, vol. 105, no. 18, p. 182106, 2014.
- [117] M. Myronov, “Molecular beam epitaxy of high mobility silicon, silicon germanium and germanium quantum well heterostructures,” in *Molecular Beam Epitaxy*, pp. 37–54, Elsevier, 2018.
- [118] C. Fenouillet-Beranger, B. Mathieu, B. Previtali, M. Samson, N. Rambal, V. Benevent, S. Kerdiles, J. Barnes, D. Barge, P. Besson, *et al.*, “New insights on bottom layer thermal stability and laser annealing promises for high performance 3D VLSI,” in *2014 IEEE International Electron Devices Meeting*, pp. 27–5, IEEE, 2014.
- [119] Y.-J. Lin, H.-Y. Tsao, and D.-S. Liu, “Hall-effect mobility of pentacene films prepared by the thermal evaporating method with different substrate temperature,” *Applied Physics Letters*, vol. 101, no. 1, p. 013302, 2012.
- [120] Y. S. Lee, M. T. Winkler, S. C. Siah, R. Brandt, and T. Buonassisi, “Hall mobility of cuprous oxide thin films deposited by reactive direct-

- current magnetron sputtering,” *Applied Physics Letters*, vol. 98, no. 19, p. 192115, 2011.
- [121] J. Kim, H.-M. Kim, S. Cho, C. Avis, and J. Jang, “High hall mobility p -type $\text{Cu}_2\text{SnS}_3\text{-Ga}_2\text{O}_3$ with a high work function,” *Advanced Functional Materials*, vol. 28, no. 34, p. 1802941, 2018.
- [122] T. Jun, J. Kim, M. Sasase, and H. Hosono, “Material design of p -type transparent amorphous semiconductor, Cu-Sn-I ,” *Advanced Materials*, vol. 30, no. 12, p. 1706573, 2018.
- [123] H. Hiramatsu, M. Orita, M. Hirano, K. Ueda, and H. Hosono, “Electrical conductivity control in transparent p -type (LaO) CuS thin films prepared by rf sputtering,” *Journal of applied physics*, vol. 91, no. 11, pp. 9177–9181, 2002.
- [124] Z. Yao, B. He, L. Zhang, C. Zhuang, T. Ng, S. Liu, M. Vogel, A. Kumar, W. Zhang, C. Lee, *et al.*, “Energy band engineering and controlled p -type conductivity of CuAlO_2 thin films by nonisovalent Cu-O alloying,” *Applied Physics Letters*, vol. 100, no. 6, p. 062102, 2012.
- [125] H.-N. Lee, H.-J. Kim, and C.-K. Kim, “ p -channel tin monoxide thin film transistor fabricated by vacuum thermal evaporation,” *Japanese Journal of Applied Physics*, vol. 49, no. 2R, p. 020202, 2010.
- [126] J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato, U. Schwingenschloögl, and H. N. Alshareef, “Record mobility in trans-

- parent *p*-type tin monoxide films and devices by phase engineering,” *ACS nano*, vol. 7, no. 6, pp. 5160–5167, 2013.
- [127] M. Liao, Z. Xiao, F.-Y. Ran, H. Kumomi, T. Kamiya, and H. Hosono, “Effects of Pb doping on hole transport properties and thin-film transistor characteristics of SnO thin films,” *ECS Journal of Solid State Science and Technology*, vol. 4, no. 3, p. Q26, 2015.
- [128] M. Wang, M. Wang, H.-H. Lin, M. Ballabio, H. Zhong, M. Bonn, S. Zhou, T. Heine, E. Cánovas, R. Dong, *et al.*, “High-mobility semiconducting two-dimensional conjugated covalent organic frameworks with *p*-type doping,” *Journal of the American Chemical Society*, vol. 142, no. 52, pp. 21622–21627, 2020.
- [129] A. Zavabeti, P. Aukarasereenont, H. Tuohey, N. Syed, A. Jannat, A. Elbourne, K. A. Messalea, B. Y. Zhang, B. J. Murdoch, J. G. Partridge, *et al.*, “High-mobility *p*-type semiconducting two-dimensional -TeO₂,” *Nature Electronics*, vol. 4, no. 4, pp. 277–283, 2021.
- [130] M. R. Laskar, D. N. Nath, L. Ma, E. W. Lee, C. H. Lee, T. Kent, Z. Yang, R. Mishra, M. A. Roldan, J.-C. Idrobo, *et al.*, “*p*-type doping of MoS₂ thin films using Nb,” *Applied Physics Letters*, vol. 104, no. 9, p. 092104, 2014.
- [131] Q. Zaixiang, S. Yun, H. Weiyu, H. Qing, and L. Changjian, “Polycrys-

- talline GaSb thin films grown by co-evaporation,” *Journal of Semiconductors*, vol. 30, no. 3, p. 033004, 2009.
- [132] V. Vandalon, M. A. Verheijen, W. M. Kessels, and A. A. Bol, “Atomic layer deposition of Al-doped MoS₂: Synthesizing a *p*-type 2D semiconductor with tunable carrier density,” *ACS applied nano materials*, vol. 3, no. 10, pp. 10200–10208, 2020.
- [133] A. Liu, H. Zhu, W.-T. Park, S.-J. Kang, Y. Xu, M.-G. Kim, and Y.-Y. Noh, “Room-temperature solution-synthesized *p*-type copper (I) iodide semiconductors for transparent thin-film transistors and complementary electronics,” *Advanced Materials*, vol. 30, no. 34, p. 1802379, 2018.
- [134] Y. Ye, R. Lim, and J. M. White, “High mobility amorphous zinc oxynitride semiconductor material for thin film transistors,” *Journal of applied physics*, vol. 106, no. 7, p. 074512, 2009.
- [135] C. Zhang, J. Wu, Y. Sun, C. Tan, T. Li, T. Tu, Y. Zhang, Y. Liang, X. Zhou, P. Gao, *et al.*, “High-mobility flexible oxyselenide thin-film transistors prepared by a solution-assisted method,” *Journal of the American Chemical Society*, vol. 142, no. 6, pp. 2726–2731, 2020.
- [136] J. Wu, H. Yuan, M. Meng, C. Chen, Y. Sun, Z. Chen, W. Dang, C. Tan, Y. Liu, J. Yin, *et al.*, “High electron mobility and quantum

- oscillations in non-encapsulated ultrathin semiconducting $\text{Bi}_2\text{O}_2\text{Se}$,” *Nature nanotechnology*, vol. 12, no. 6, pp. 530–534, 2017.
- [137] E. Lee, A. Benayad, T. Shin, H. Lee, D.-S. Ko, T. S. Kim, K. S. Son, M. Ryu, S. Jeon, and G.-S. Park, “Nanocrystalline ZnON; high mobility and low band gap semiconductor material for high performance switch transistor and image sensor application,” *Scientific reports*, vol. 4, no. 1, pp. 1–8, 2014.
- [138] A. Suresh, P. Gollakota, P. Wellenius, A. Dhawan, and J. F. Muth, “Transparent, high mobility InGaZnO thin films deposited by PLD,” *Thin Solid Films*, vol. 516, no. 7, pp. 1326–1329, 2008.
- [139] G. Wang, C. Shi, L. Zhao, H. Diao, and W. Wang, “Transparent conductive Hf-doped In_2O_3 thin films by rf sputtering technique at low temperature annealing,” *Applied Surface Science*, vol. 399, pp. 716–720, 2017.
- [140] S.-G. Ban, K.-T. Kim, B. D. Choi, J.-W. Jo, Y.-H. Kim, A. Facchetti, M.-G. Kim, and S. K. Park, “Low-temperature postfunctionalization of highly conductive oxide thin-films toward solution-based large-scale electronics,” *ACS applied materials & interfaces*, vol. 9, no. 31, pp. 26191–26200, 2017.
- [141] C. Tsakonas, V. Kuznetsov, W. Cranton, N. Kalfagiannis, K. Abusabee, D. Koutsogeorgis, N. Abeywickrama, and P. Edwards, “Low

- temperature sputter-deposited ZnO films with enhanced Hall mobility using excimer laser post-processing,” *Journal of Physics D: Applied Physics*, vol. 50, no. 48, p. 485306, 2017.
- [142] H. Mahdhi, K. Djessas, and Z. B. Ayadi, “Synthesis and characteristics of Ca-doped ZnO thin films by rf magnetron sputtering at low temperature,” *Materials Letters*, vol. 214, pp. 10–14, 2018.
- [143] J. Wu, C. Tan, Z. Tan, Y. Liu, J. Yin, W. Dang, M. Wang, and H. Peng, “Controlled synthesis of high-mobility atomically thin bismuth oxyse-lenide crystals,” *Nano letters*, vol. 17, no. 5, pp. 3021–3026, 2017.
- [144] J. Wu, C. Qiu, H. Fu, S. Chen, C. Zhang, Z. Dou, C. Tan, T. Tu, T. Li, Y. Zhang, *et al.*, “Low residual carrier concentration and high mobility in 2D semiconducting BiOSe,” *Nano letters*, vol. 19, no. 1, pp. 197–202, 2018.
- [145] Y. Kajikawa, T. Okuzako, S. Takami, and M. Takushima, “Electrical properties of polycrystalline GaInAs thin films,” *Thin Solid Films*, vol. 519, no. 1, pp. 136–144, 2010.
- [146] M. Takushima, Y. Kajikawa, Y. Kuya, M. Shiba, and K. Ohnishi, “Low-temperature growth of InAs on glass and plastic film substrates by molecular-beam deposition,” *Japanese Journal of Applied Physics*, vol. 47, no. 3R, p. 1469, 2008.

- [147] S.-h. Lee, J.-s. Jung, S.-s. Lee, S.-b. Lee, and N.-m. Hwang, “Low temperature deposition of polycrystalline silicon thin films on a flexible polymer substrate by hot wire chemical vapor deposition,” *Journal of Crystal Growth*, vol. 453, pp. 151–157, 2016.

Chapter 2

Low-Temperature Grown Polycrystalline Indium Arsenide

This chapter is adapted from the following conference presentation and journal publications:

- **A. Curran**, E. Secco, A. Pescaglini, A. Gocalinska, E. Mura, K. Thomas, R. Nagle, I. M. Povey, E. Pelucchi, C. O'Dwyer, P. K. Hurley, and F. Gity, Investigating Polycrystalline III-V Thin Films as Channel Materials for “Above IC” Logic and Memory Applications, presented at ECS AiMES Conference, 2nd October 2018, Cancun, Mexico, abstract DOI: 10.1149/ma2018-02/34/1165.

- **A. Curran**, A. Gocalinska, A. Pescaglini, E. Secco, E. Mura, K. Thomas, R. E. Nagle, B. Sheehan, I. M. Povey, E. Pelucchi, C. O'Dwyer, P. K. Hurley, and F. Gity, Structural and electronic properties of polycrystalline InAs thin films deposited on silicon dioxide and glass at temperatures below 500°C, *Crystals* 11(2), 2021, DOI: 10.3390/cryst11020160.
- A. Gocalinska, A. Pescaglini, E. Secco, E. Mura, K. Thomas, **A. Curran**, F. Gity, R. Nagle, M. Schmidt, P. P. Michałowski, P. K. Hurley, I. Povey, E. Pelucchi, Next generation low temperature polycrystalline materials for above IC electronics. High mobility n- and p-type III-V metalorganic vapour phase epitaxy thin films on amorphous substrates, *Journal of Physics: Photonics* 2(2), 2020, DOI: 10.1088/2515-7647/ab7557.

Author contributions:

A. Curran - experimental planning, Hall analysis, Transmission Electron Microscopy (TEM) analysis, device fabrication, electrical characterisation

E. Secco - III-V film growth

A. Pescaglini - III-V film growth

A. Gocalinska - III-V film growth and Atomic Force Microscopy (AFM)

E. Mura - Hall effect analysis

K. Thomas - III-V film growth

R. E. Nagle - Scanning Electron Microscopy (SEM) imaging

B. Sheehan - TEM analysis

I. M. Povey - Atomic Layer Deposition (ALD) oxide growth

E. Pelucchi - concept, design of experiment

C. O'Dwyer - analysis, supervision

P. K. Hurley - analysis, design of experiment, concept, supervision

F. Gity - concept, design of experiment, device processing, supervision

2.1 Abstract

Polycrystalline indium arsenide (poly InAs) thin films grown at 475°C by Metalorganic Vapour Phase Epitaxy (MOVPE) are explored as possible candidates for low temperature grown semiconducting materials. Structural and transport properties of the films are reported, with electron mobilities of 100 cm²/Vs achieved at room temperature, and values reaching 155 cm²/Vs for a heterostructure including the polycrystalline InAs film. Temperature dependent Hall effect measurements are performed to find the dominant limiting factor of mobility in the film. Surface treatments are tested in preparation for device fabrication.

2.2 Introduction

Low temperature grown (<500°C) semiconducting materials have garnered much attention in recent years for a number of applications such as flexi-

ble/wearable electronics, display technologies, and back-end-of-line (BEOL) integration. For these applications, high temperature processing may not be compatible with the substrate type, or previously deposited layers [1]. During conventional device processing, dopant activation is often the highest temperature step, indicating a need for semiconducting materials which do not require high temperature dopant activation. Several different materials are being explored for these purposes, including InGaZnO [2], InSnO [3], and 2D materials [4, 5].

InAs is known to exhibit a high surface electron density in the absence of any intentional doping. This 2D electron gas on the surface of crystalline InAs has been postulated to originate from In adatoms and adsorption of H adatoms [6]. The 2D electron gas reported for crystalline InAs suggests that polycrystalline InAs may be a potential candidate for low temperature processing. Further to this, if a dopant is required, *n*- and *p*-type dopant activation energies in InAs are very low (0.02 eV for Si and 0.01 eV for Zn, which are *n*- and *p*-type dopants respectively), and as a consequence, dopant activation can occur during growth without the need for a subsequent high temperature dopant activation step [7]. III-V materials have the added benefit of higher carrier velocities than Si. In InAs electron mobilities are $\geq 40,000$ cm²/Vs, resulting in the potential to allow for a decrease in operating voltage without compromising switching speed [8].

It has been shown that poly InAs can be grown at low temperatures on amorphous substrates (SiO_2 and glass), and through Zn doping, can even achieve p -type mobilities of $>5 \text{ cm}^2/\text{Vs}$, with no optimization [9]. This is an important consideration if this material is to be implemented in lower-power friendly Complementary Metal Oxide Semiconductor (CMOS) architectures in the future. In this chapter we investigate whether low temperature grown (max temperature $<500^\circ\text{C}$) poly InAs also exhibits a high electron density on the surface without intentional doping. In addition, the dominant mechanism limiting the carrier mobility is investigated, and the effect of surface treatments on the contact resistivity of poly InAs is studied.

2.3 Experimental

Growth of III-V films described in this section was carried out by members of the Epitaxy and Physics of Nanostructures group in Tyndall. Poly InAs films (nominally 10-100 nm thick) were grown by MOVPE on corning “smartphone grade” glass and Si/ SiO_2 substrates at 475°C , using In droplets as nucleation sites. Precursors used were Trimethyl Indium (TMIn) and arsine (AsH_3). For selected samples, a polycrystalline GaAs buffer layer was added to form a GaAs/InAs heterostructure. The same “droplet epitaxy” technique was employed (see 2.1), using Trimethyl Gallium (TMGa) or Triethyl Gallium (TEGa) and arsine precursors. For samples containing zinc or phosphorus, Diethyl Zinc (DEZn) or phosphine (PH_3) precursors were used.

AFM was also carried out by members of the Epitaxy and Physics of Nanostructures group in Tyndall. Measurements were performed using a Veeco Multimode V AFM in tapping/non-contact mode in air and at room temperature.

SEM images were taken using an FEI Quanta 650 FEG SEM. The elemental composition of the films was studied through Energy-Dispersive X-Ray (EDX) analysis, using an Oxford Instruments X-Max EDX. This was performed while the sample was in the SEM vacuum chamber, allowing for elemental chemical analysis of the film. Samples were prepared for Cross-sectional Transmission Electron Microscopy (XTEM) using a Dual Beam Focussed Ion Beam (FIB) Helios NanoLab 600i. Carbon and platinum protective layers were deposited before the lamella was removed and thinned to <200 nm thickness. TEM analysis was performed using a JEOL JEM-2100.

Hall effect measurements presented in this chapter were performed at room temperature unless otherwise stated and were measured on a LakeShore Model 8404 AC/DC Hall effect measurement system. Samples for Hall effect measurements were 1×1 cm² and were cut from the centre of the substrates loaded for film growth to avoid any growth on the edge of the sample causing conduction through the substrate. The back of each sample was tested with a multimeter to confirm that the substrate was not contributing to con-

duction. The van der Pauw configuration was used for these measurements. A detailed description of the Hall Effect measurement system and method can be found in Appendix A. Hall effect measurement results were obtained for one piece of each sample and so no statistical data can be presented for measured mobilities and carrier concentrations.

To test the efficacy of a variety of surface treatments, wet dips in a variety of chemicals were performed before deposition of metal contacts through metal evaporation. Electrical characteristics were measured using a semiconductor device parameter analyser Agilent B1500, and a semi-automatic Cascade probe station.

2.4 Results and Discussion

2.4.1 InAs Material Properties

A range of InAs film thicknesses (10-100 nm) were grown on SiO₂ and glass to study the properties of the InAs film. Using a nominally 25 nm film, the expected polycrystalline nature of the InAs film was confirmed by XTEM, and EDX analysis was used to confirm that the composition of the lamella used for imaging was InAs. Figure 2.1 shows a schematic representation of the “droplet epitaxy” growth process employed by the Epitaxy and Physics of Nanostructures group in Tyndall. In Figure 2.1, a heterostructure growth is shown. For the InAs films directly on insulator, the process is the same,

with the exception of the GaAs step.

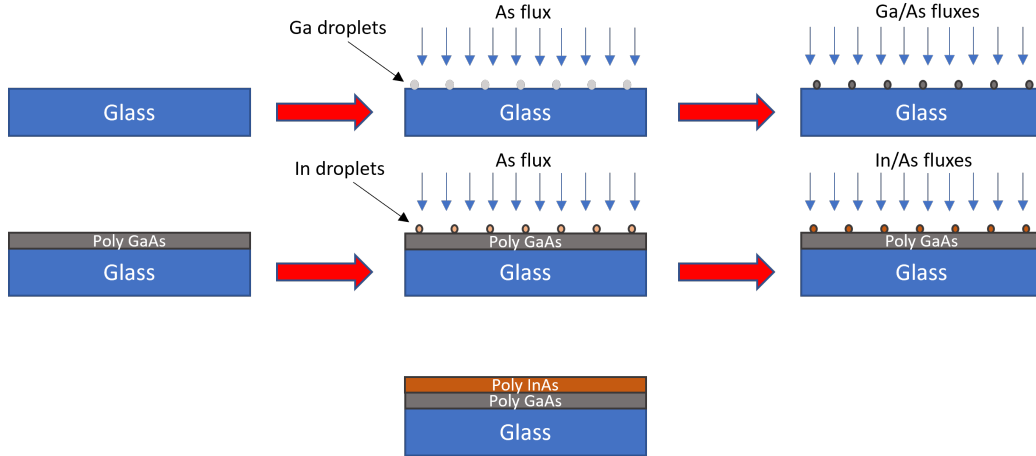


Figure 2.1: Schematic representation of the “droplet epitaxy” growth process.

Figure 2.2 shows a cross-section of the nominally 25 nm film, with lamella thickness of <200 nm. The poly InAs film appears continuous, with some local areas where the film does not have complete closure, possibly resulting in the difference in contrast seen towards the right-hand side of Figure 2.2a. There is also a contrast difference in the area between the substrate and the InAs film. The area shown in Figure 2.2b was used to determine the average thickness of the film as deposited. The maximum and minimum thicknesses were 55.5 nm and 40.9 nm respectively, with the average thickness determined to be 49.5 nm, with a standard deviation of 4.6 nm. Grain size can be determined from the XTEM image, and is seen to be in the order of 10s of nanometres.

Despite the film not being entirely uniform in the cross-sectional image of

the TEM lamella, it was possible to measure an electron mobility of $100 \text{ cm}^2/\text{Vs}$ at room temperature, suggesting that there are percolation paths present in the 3D geometry. Figure 2.2c shows the temperature dependence of the carrier mobility and concentration in poly InAs, determined by Hall effect measurements over a temperature range of 125-400 K. As expected, the majority carrier type is electrons. The carrier mobility in the poly InAs film is seen to be almost independent of temperature. This is unlike what is usually seen in bulk crystalline InAs, where the electron mobility decreases with temperature [10]. Based on the Matthiessen Rule [11], the equation governing total mobility can be expressed as:

$$\frac{1}{\mu_T} = \frac{1}{\mu_{phon}} + \frac{1}{\mu_Q} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{gb}} \quad (2.4.1)$$

This equation indicates the different factors which can limit the total mobility of a film:

1. phonon scattering (μ_{phon})
2. Coulomb interactions (μ_Q)
3. surface roughness (μ_{sr})
4. thermionic emission over grain boundaries (μ_{gb})

As surface roughness is the only factor of the three which is not strongly temperature dependent [12], we can conclude that this is the dominant factor limiting carrier mobility in the poly InAs film.

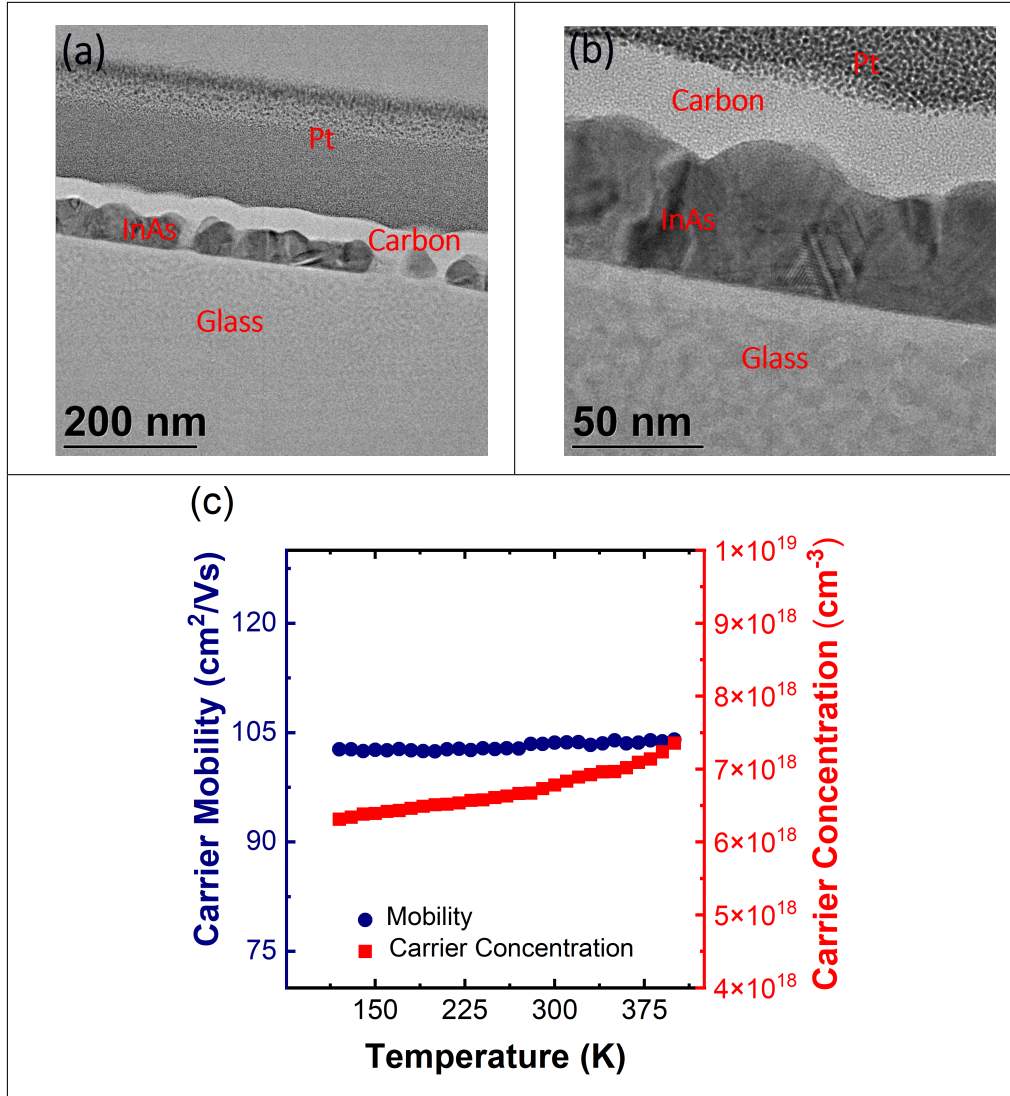


Figure 2.2: (a&b) XTEM images of nominally 25 nm poly InAs film grown at 475°C directly on a glass substrate. (c) Temperature dependent Hall effect measurements of 25 nm poly InAs film on glass. Measurements taken in AC mode, with magnetic field of 0.6 T

It is well known that the mobility of polycrystalline silicon is limited by grain boundary scattering. It is observed that a poly silicon film with lower doping

shows an increase in mobility with temperature (due to thermionic emission over potential grain boundaries), while a poly silicon film with higher doping shows a decrease in mobility with temperature (phonon limited) as the grain boundary defects are saturated and the potential barrier at the grain boundary regions tends to zero [13]. If the unintentionally doped poly InAs described in this chapter behaved in the same way, we would expect the mobility to increase with temperature at the higher temperature range as the potential barrier is removed and the mobility becomes phonon limited. However, we do not observe this, as due to our high electron concentration (and smaller bandgap than silicon) the grain boundaries are saturated and the dominant factor limiting the mobility is surface roughness, with the mobility remaining relatively constant over the entire measurement range of temperatures as a result.

Figure 2.3 shows AFM results for the film whose results are shown in Figure 2.2. When looking at the heights presented in the Figures, it is important to remember that the zero they are measured from may not be from the substrate. This means that the height is not the total thickness of the film and should only be taken as an indicator of the variation over the area measured. This explains why the peak in frequency (i.e. how often the height is recorded during the scan, normalised) vs height in Figure 2.3b is at a lower value than the average thickness determined using the XTEM image in Figure 2.2b. While AFM is a useful technique and gave good topographical information,

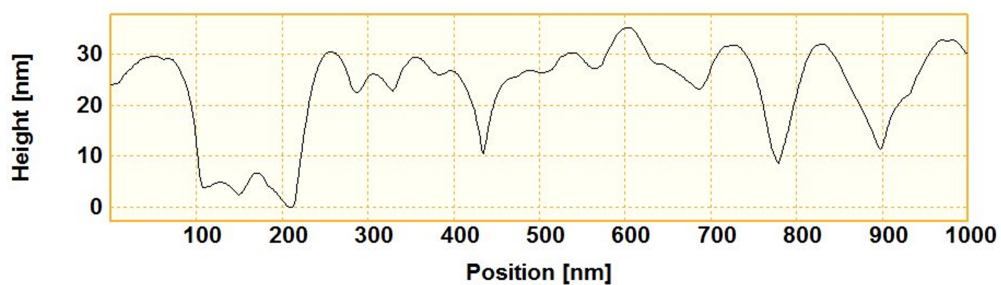
it was not as useful as a combination of SEM and XTEM in determining actual thickness of the film and continuity. For this reason, SEM and XTEM results are mainly focussed on for film morphology analysis in the rest of this thesis.

Efforts were made to improve the quality of the poly InAs thin films with a view to implementation in transistor test devices. The benefits of depositing a poly GaAs layer prior to poly InAs such as minimizing roughness and improving continuity have been discussed at length in previous publications by the Nanomaterials and Devices group and the Epitaxy and Physics of Nanostructures group [9]. These benefits are evident from the Hall effect measurement results shown in Table 2.1, as the nominally 10 nm poly InAs film grown directly on a glass substrate was not capable of being measured using the Hall effect apparatus because it lacked sufficient continuity to obtain reliable data (whereas the 10nm film with GaAs buffer layer could be measured). This was due to two factors:

1. The lack of continuity and variation over the area of the sample meant that when the geometry averaging step of the measurement was reached, the difference between each geometry was too great for the average value to accurately represent the film.
2. The lack of continuity also causes a high resistance film, which needs large lead voltages (up to 100 V) to push even a very low current

(a)

Line No: 272



(b)

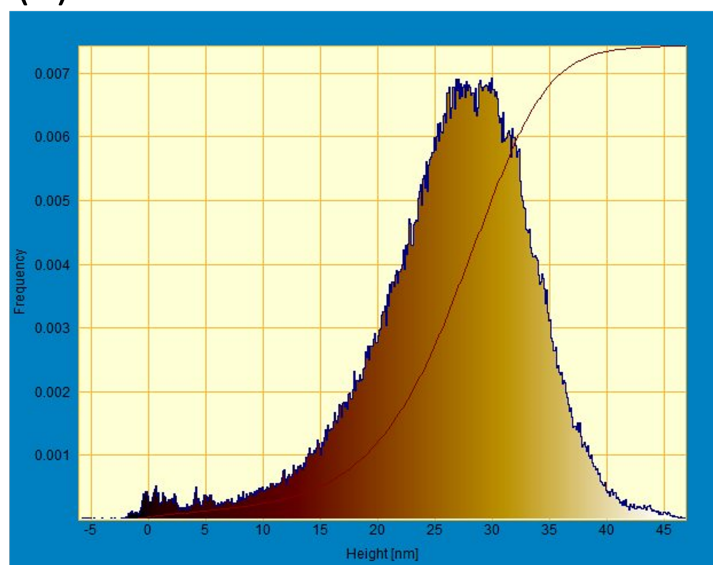


Figure 2.3: (a) Plot of one line taken during an AFM scan of the 25 nm InAs on glass, and (b) a plot of height vs frequency.

through the film (in the range 1 nA-1 μ A). When only a low current can be used, it is difficult to obtain a reasonable separation of the charges in the film, meaning that the Hall voltage is low (the Hall voltage is proportional to the applied current), and the measurement is not reliable.

When a 25 nm poly GaAs buffer layer was deposited prior to 10 nm poly InAs growth, the continuity was improved, allowing for determination of carrier mobility and concentration through Hall effect measurements. It is noted that a contribution to the carrier concentration and mobility from the 25 nm GaAs buffer layer can be discarded, as this layer measured in isolation yields a carrier concentration of 10^{16} cm^{-3} and an electron mobility of $0.14 \text{ cm}^2/\text{Vs}$.

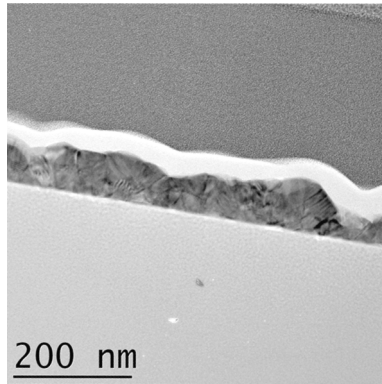
Film Details	Carrier Mobility (cm^2/Vs)	Carrier Concentration (cm^{-3})
25nm InAs	73	7.0×10^{18}
25nm GaAs + 10nm InAs	29	9.6×10^{18}
25nm GaAs + 25nm InAs	155	8.0×10^{18}

Table 2.1: Room temperature Hall effect measurement results of poly InAs films of 10 nm or 25 nm nominal thickness, with or without prior 25nm poly GaAs buffer layer, grown on glass.

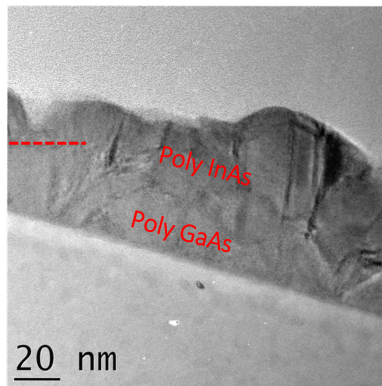
Figure 2.4 shows XTEM images of 25 nm poly GaAs + 25 nm poly InAs film on glass, with InAs directly on glass as a comparison, further highlighting the benefits of the heterostructure formation. Figure 2.4a shows greater uniformity than that possessed by the nominally 25 nm film in Figure 2.2a,

where both scale bars are 200 nm. Figure 2.4b was used to calculate the average thickness of the two layers of the heterostructure. The poly GaAs buffer layer was found to have an average thickness of 30 nm, with a standard deviation of 3.6 nm, while the poly InAs layer was found to have an average thickness of 26 nm, with a standard deviation of 9.8 nm.

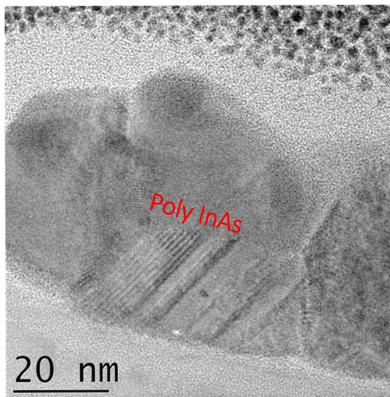
As these films were intended for use in a junctionless transistor architecture [14], there was concern that the carrier concentrations measured in the InAs film (Table 2.1) would be too high to allow the full depletion of the channel, which is necessary to turn off the transistor [15]. For this reason, Zn was incorporated as a *p*-type dopant into the poly InAs film during growth. This Zn incorporation effectively modulated the carrier concentration in the poly InAs thin films by 3 orders of magnitude with no significant reduction in mobility evident. Table 2 shows Hall effect measurement results of poly GaAs + Zn-doped poly InAs(P) with varying InAs thicknesses (10-100 nm nominal thicknesses). Phosphorus was included as a surfactant during the growth process. Interestingly these poly InAs films showed the traditionally expected scaling of sheet carrier concentration with thickness, meaning that there was not exclusively a surface charge present as had been seen in the literature, but also a contribution from a bulk charge in the poly InAs film.



(a)



(b)



(c)

Figure 2.4: XTEM images of (a&b) 25 nm poly GaAs + 25 nm poly InAs on glass (where the red line indicates position of the interface), and (c) 25 nm poly InAs directly on glass.

Film Thick- ness (nm)	Carrier Mobil- ity (cm^2/Vs)	Carrier Conc (cm^{-3})	Sheet Carrier Conc (cm^{-2})
10	24.6	2.5×10^{16}	2.5×10^{10}
25	61.6	5.22×10^{16}	1.3×10^{11}
100	103.4	4.6×10^{16}	4.5×10^{11}

Table 2.2: Room temperature Hall effect measurement results of poly GaAs + Zn-doped InAs(P) grown on SiO_2 .

2.4.2 Surface Treatments

As discussed in Section 1.2.3, exposure of InAs to air is expected to result in oxide formation on the surface, and subsequent Fermi level pinning. Unlike silicon's native oxide, III-V counterparts are not suitable for use as gate oxides, and so must be removed to allow for suitable gate oxide deposition. The effect of a number of surface treatments designed to remove native oxides and/or passivate the InAs surface prior to metal contact deposition were studied. Post treatment properties were extracted from circular Transmission Line Measurement (cTLM) results, and presented in Figure 2.5. The process of extracting the data is explained in greater detail in Appendix B. The cTLM test structure design is shown in Figure 2.5a, where the blue areas represent the contact metal. A Buffered Oxide Etch (BOE) treatment caused the specific contact resistance to increase compared to a sample which had received no treatment. Treatment with HCl achieved a clear improvement in electrical characteristics, however a combination of BOE/HCl/ $(\text{NH}_4)_2\text{S}$ resulted in consistently superior electrical results compared to those of the sample which received no treatment, and the samples which received BOE or

HCl treatments in isolation. The value of specific contact resistance obtained for the sample which received the BOE/HCl/(NH₄)₂S, 1.78x10⁻⁸ Ω·cm², is an acceptable specific contact resistance even for commercial devices. The high carrier concentration of the films is a major reason for this, along with a contribution from the relative roughness of the film, which effectively increases the area of the contact.

Taking figures from the Hall results for a 25 nm poly InAs film directly on a glass substrate in Table 2.1, mobility is 73 cm²/Vs and carrier concentration is 7x10¹⁸ cm⁻³. Therefore, resistivity should be equal to:

$$Resistivity = \frac{1}{\sigma} = \frac{1}{q \cdot \mu \cdot n} + \frac{1}{q \cdot 73 \cdot (7 \cdot 10^{18})} \quad (2.4.2)$$

Here σ represents the conductivity of the semiconductor, q is electronic charge, μ is carrier mobility, and n is carrier concentration. This comes out to be 0.01 Ω·cm, which is in good agreement with the results shown in Figure 2.5e. These results are from large area (Hall) and small area (cTLM) techniques, so this agreement is a strong verification of results, fabrication, and testing methods. These results also show that the nature of the surface of the polycrystalline InAs film can be changed drastically using wet chemical surface treatments which do not affect the bulk properties. The methods of surface treatment and the effects on the III-V surface are discussed in Section 1.2.3.

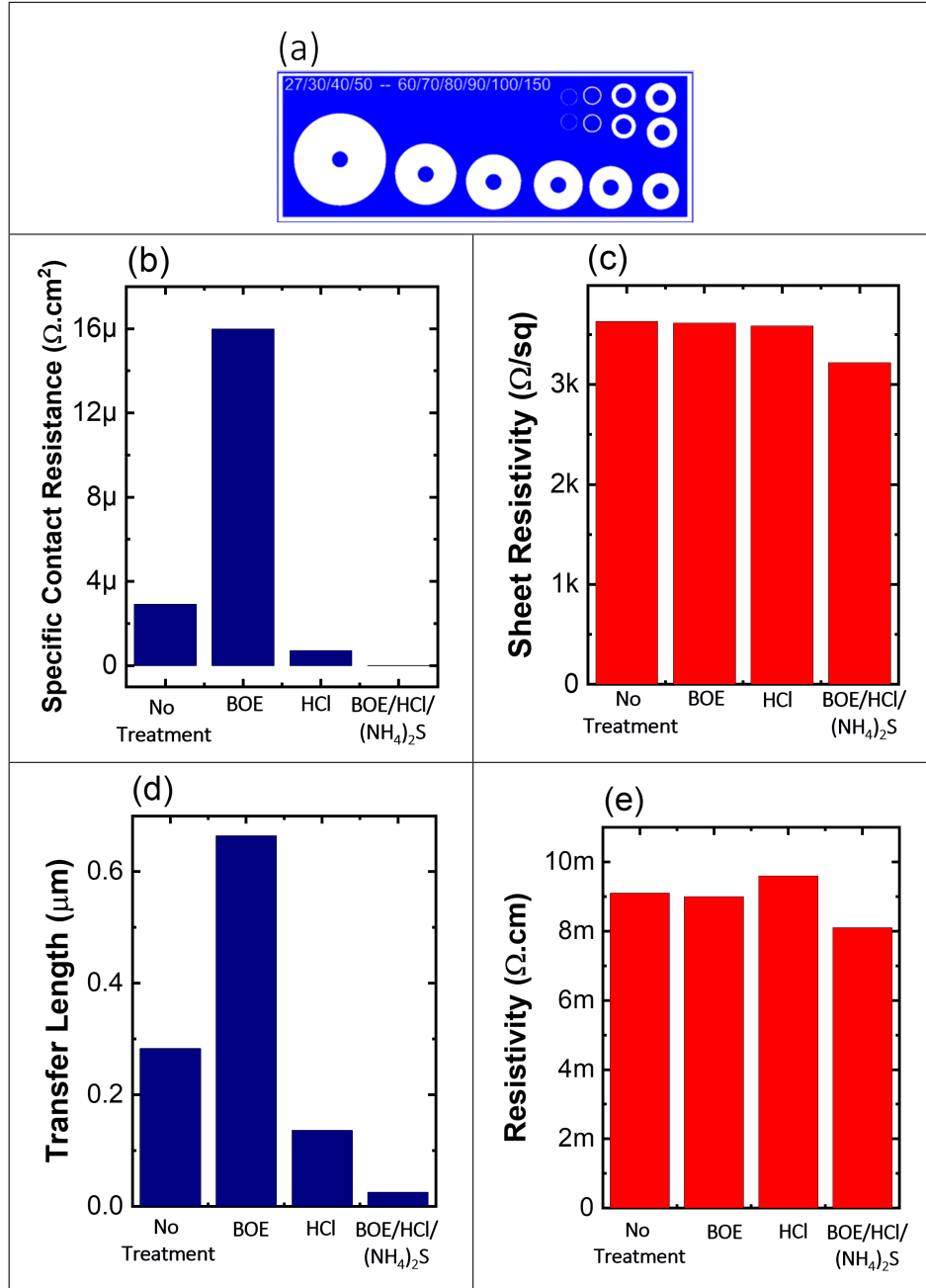


Figure 2.5: (a) Schematic cTLM structure layout from which electrical measurements were taken. (b) Specific contact resistance, (c) sheet resistivity, (d) transfer length, and (e) resistivity for a 25 nm poly InAs film which received each of the surface treatments, and a reference sample which received no surface treatment.

2.5 Benchmarking

Figure 2.6 shows the graph included in Section 1.3.2, with the films from this chapter included as comparison. The polycrystalline InAs compares relatively favourably to other published works shown here. The two polycrystalline examples with higher mobilities - InAs [16] and InGaAs [17] - are both also grown on amorphous or plastic substrates, however they are much thicker than the films grown in this work ($>1\ \mu\text{m}$). From the results for polycrystalline InAs in this Chapter, it is clear that the mobility is dependent on thickness, and it is possible to achieve higher mobilities in thicker films. For device applications, thinner films are more favourable. The three $\text{Bi}_2\text{O}_2\text{Se}$ results with higher mobilities than this work [18–20], are from the same group and are all grown on a crystalline substrate. It is easier to grow a high quality film on a crystalline substrate rather than the amorphous substrates demonstrated in this chapter. For potential implementation, it is important to be able to grow films on a Si/SiO₂ substrate, as this is the ubiquitous substrate in modern electronics.

2.6 Conclusions

We have shown the ability of low temperature grown (below 500°C) poly InAs thin films to achieve remarkable electron mobilities when measured at room temperature (approx. $100\text{cm}^2/\text{Vs}$). A room temperature Hall mobility of $155\text{cm}^2/\text{Vs}$ was achieved for a heterostructure consisting of 25 nm poly

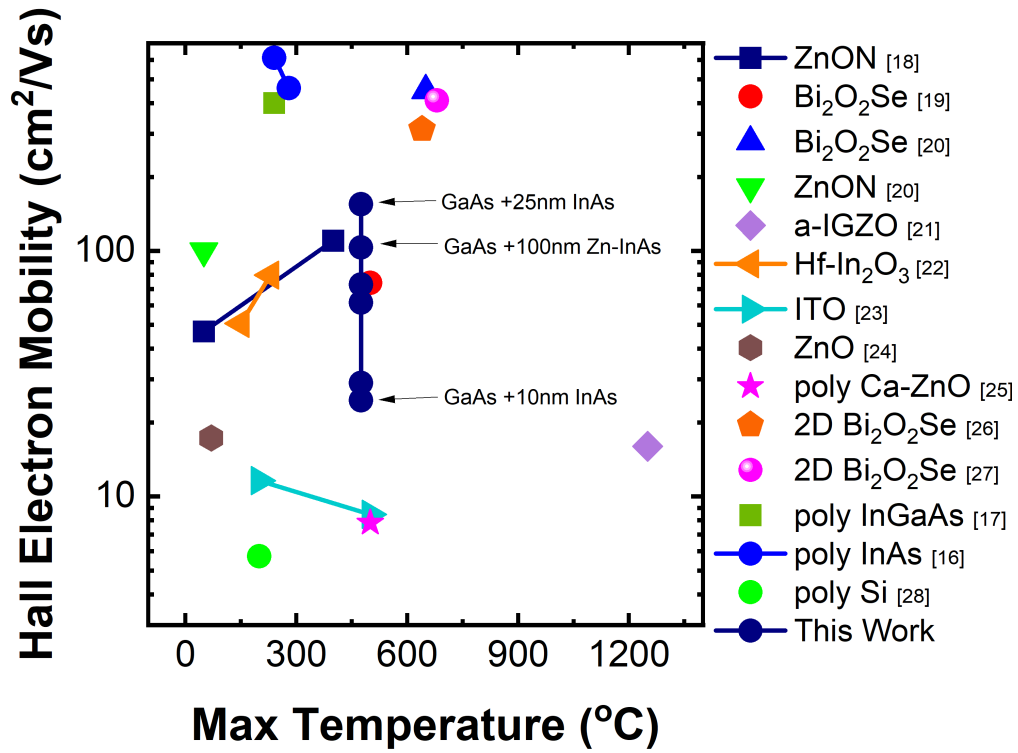


Figure 2.6: Results from polycrystalline InAs films in this work compared to results from the literature [16–29].

GaAs + 25 nm poly InAs on glass (Table 2.1) exceeds reported Hall mobility values of many other low temperature grown thin film materials, including polycrystalline silicon [29], Hf-doped In_2O_3 [25], ITO [26], and ZnO [27, 28]. Temperature dependent Hall effect measurements determined that the limiting factor of the mobility in the poly InAs film is surface roughness. The effect of a number of surface treatments on the contact resistance and a number of other parameters were studied. These films show potential as high electron mobility materials for use in transistor type devices.

Bibliography

- [1] S. Datta, S. Dutta, B. Grisafe, J. Smith, S. Srinivasa, and H. Ye, “Back-end-of-line compatible transistors for monolithic 3-D integration,” *IEEE Micro*, vol. 39, no. 6, pp. 8–15, 2019.
- [2] J. Troughton and D. Atkinson, “Amorphous InGaZnO and metal oxide semiconductor devices: an overview and current status,” *Journal of Materials Chemistry C*, vol. 7, no. 40, pp. 12388–12414, 2019.
- [3] C. E. Kim and I. Yun, “Device characteristics of Ti–InSnO thin film transistors with modulated double and triple channel structures,” *Thin solid films*, vol. 537, pp. 275–278, 2013.
- [4] R. Yang, H. Li, K. K. Smithe, T. R. Kim, K. Okabe, E. Pop, J. A. Fan, and H.-S. P. Wong, “2D molybdenum disulfide (MoS_2) transistors driving RRAMs with 1T1R configuration,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, pp. 19–5, IEEE, 2017.
- [5] J. Zheng, X. Yan, Z. Lu, H. Qiu, G. Xu, X. Zhou, P. Wang, X. Pan, K. Liu, and L. Jiao, “High-mobility multilayered MoS_2 flakes with low

- contact resistance grown by chemical vapor deposition,” *Advanced Materials*, vol. 29, no. 13, p. 1604540, 2017.
- [6] J. Weber, A. Janotti, and C. Van de Walle, “Intrinsic and extrinsic causes of electron accumulation layers on InAs surfaces,” *Applied Physics Letters*, vol. 97, no. 19, p. 192106, 2010.
- [7] M. Guseva, N. Zotova, A. Koval, and D. Nasledov, “Behavior of group IV elements introduced into indium arsenide by ion implantation,” tech. rep., AF Ioffe Physicotechnical Institute, Academy of Sciences of the USSR, Leningrad, 1974.
- [8] J. A. Del Alamo, “Nanometre-scale electronics with III–V compound semiconductors,” *Nature*, vol. 479, no. 7373, pp. 317–323, 2011.
- [9] A. Gocalinska, A. Pescaglini, E. Secco, E. E. Mura, K. Thomas, A. Curran, F. Gity, R. Nagle, M. Schmidt, P. P. Michałowski, *et al.*, “Next generation low temperature polycrystalline materials for above IC electronics. high mobility *n*-and *p*-type III–V metalorganic vapour phase epitaxy thin films on amorphous substrates,” *Journal of Physics: Photonics*, vol. 2, no. 2, p. 025003, 2020.
- [10] D. Rode, “Low-field electron transport,” in *Semiconductors and semimetals*, vol. 10, pp. 1–89, Elsevier, 1975.
- [11] A. Matthiessen and C. Vogt, “IV. on the influence of temperature on

- the electric conducting-power of alloys,” *Philosophical Transactions of the Royal Society of London*, no. 154, pp. 167–200, 1864.
- [12] T. Ando, A. B. Fowler, and F. Stern, “Electronic properties of two-dimensional systems,” *Reviews of Modern Physics*, vol. 54, no. 2, p. 437, 1982.
- [13] J. Y. Seto, “The electrical properties of polycrystalline silicon films,” *Journal of Applied Physics*, vol. 46, no. 12, pp. 5247–5254, 1975.
- [14] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O’Neill, A. Blake, M. White, *et al.*, “Nanowire transistors without junctions,” *Nature nanotechnology*, vol. 5, no. 3, pp. 225–229, 2010.
- [15] J.-P. Colinge, A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, and P. Razavi, “Junctionless nanowire transistor (JNT): Properties and design guidelines,” *Solid-State Electronics*, vol. 65, pp. 33–37, 2011.
- [16] M. Takushima, Y. Kajikawa, Y. Kuya, M. Shiba, and K. Ohnishi, “Low-temperature growth of InAs on glass and plastic film substrates by molecular-beam deposition,” *Japanese Journal of Applied Physics*, vol. 47, no. 3R, p. 1469, 2008.
- [17] Y. Kajikawa, T. Okuzako, S. Takami, and M. Takushima, “Electri-

- cal properties of polycrystalline GaInAs thin films,” *Thin Solid Films*, vol. 519, no. 1, pp. 136–144, 2010.
- [18] J. Wu, C. Qiu, H. Fu, S. Chen, C. Zhang, Z. Dou, C. Tan, T. Tu, T. Li, Y. Zhang, *et al.*, “Low residual carrier concentration and high mobility in 2D semiconducting BiOSe,” *Nano letters*, vol. 19, no. 1, pp. 197–202, 2018.
- [19] J. Wu, C. Tan, Z. Tan, Y. Liu, J. Yin, W. Dang, M. Wang, and H. Peng, “Controlled synthesis of high-mobility atomically thin bismuth oxyse-lenide crystals,” *Nano letters*, vol. 17, no. 5, pp. 3021–3026, 2017.
- [20] J. Wu, H. Yuan, M. Meng, C. Chen, Y. Sun, Z. Chen, W. Dang, C. Tan, Y. Liu, J. Yin, *et al.*, “High electron mobility and quantum oscillations in non-encapsulated ultrathin semiconducting Bi₂O₂Se,” *Nature nanotechnology*, vol. 12, no. 6, pp. 530–534, 2017.
- [21] Y. Ye, R. Lim, and J. M. White, “High mobility amorphous zinc oxynitride semiconductor material for thin film transistors,” *Journal of applied physics*, vol. 106, no. 7, p. 074512, 2009.
- [22] C. Zhang, J. Wu, Y. Sun, C. Tan, T. Li, T. Tu, Y. Zhang, Y. Liang, X. Zhou, P. Gao, *et al.*, “High-mobility flexible oxyselenide thin-film transistors prepared by a solution-assisted method,” *Journal of the American Chemical Society*, vol. 142, no. 6, pp. 2726–2731, 2020.

-
- [23] E. Lee, A. Benayad, T. Shin, H. Lee, D.-S. Ko, T. S. Kim, K. S. Son, M. Ryu, S. Jeon, and G.-S. Park, “Nanocrystalline ZnON; high mobility and low band gap semiconductor material for high performance switch transistor and image sensor application,” *Scientific reports*, vol. 4, no. 1, pp. 1–8, 2014.
- [24] A. Suresh, P. Gollakota, P. Wellenius, A. Dhawan, and J. F. Muth, “Transparent, high mobility InGaZnO thin films deposited by PLD,” *Thin Solid Films*, vol. 516, no. 7, pp. 1326–1329, 2008.
- [25] G. Wang, C. Shi, L. Zhao, H. Diao, and W. Wang, “Transparent conductive Hf-doped In₂O₃ thin films by RF sputtering technique at low temperature annealing,” *Applied Surface Science*, vol. 399, pp. 716–720, 2017.
- [26] S.-G. Ban, K.-T. Kim, B. D. Choi, J.-W. Jo, Y.-H. Kim, A. Facchetti, M.-G. Kim, and S. K. Park, “Low-temperature postfunctionalization of highly conductive oxide thin-films toward solution-based large-scale electronics,” *ACS applied materials & interfaces*, vol. 9, no. 31, pp. 26191–26200, 2017.
- [27] C. Tsakonas, V. Kuznetsov, W. Cranton, N. Kalfagiannis, K. Abusabee, D. Koutsogeorgis, N. Abeywickrama, and P. Edwards, “Low temperature sputter-deposited ZnO films with enhanced hall mobility using excimer laser post-processing,” *Journal of Physics D: Applied Physics*, vol. 50, no. 48, p. 485306, 2017.

- [28] H. Mahdhi, K. Djessas, and Z. B. Ayadi, “Synthesis and characteristics of Ca-doped ZnO thin films by rf magnetron sputtering at low temperature,” *Materials Letters*, vol. 214, pp. 10–14, 2018.
- [29] S.-h. Lee, J.-s. Jung, S.-s. Lee, S.-b. Lee, and N.-m. Hwang, “Low temperature deposition of polycrystalline silicon thin films on a flexible polymer substrate by hot wire chemical vapor deposition,” *Journal of Crystal Growth*, vol. 453, pp. 151–157, 2016.

Chapter 3

Polycrystalline InAs MOSFETs

This chapter is adapted from the following conference presentation and journal publications:

1. **A. Curran**, E. Secco, A. Pescaglini, A. Gocalinska, E. Mura, K. Thomas, R. Nagle, I. M. Povey, E. Pelucchi, C. O'Dwyer, P. K. Hurley, and F. Gity, Investigating Polycrystalline III-V Thin Films as Channel Materials for “Above IC” Logic and Memory Applications, presented at ECS AiMES Conference, 2nd October 2018, Cancun, Mexico, abstract DOI: 10.1149/ma2018-02/34/1165.
2. **A. Curran**, A. Gocalinska, A. Pescaglini, E. Secco, E. Mura, K. Thomas, R. E. Nagle, B. Sheehan, I. M. Povey, E. Pelucchi, C. O'Dwyer, P. K. Hurley, and F. Gity, Structural and electronic properties of polycrystalline InAs thin films deposited on silicon dioxide and glass at temperatures below 500°C, Crystals 11(2), 2021, DOI: 10.3390/cryst11020160.

3. A. Gocalinska, A. Pescaglini, E. Secco, E. Mura, K. Thomas, **A. Curran**, F. Gity, R. Nagle, M. Schmidt, P. P. Michałowski, P. K. Hurley, I. Povey, E. Pelucchi, Next generation low temperature polycrystalline materials for above IC electronics. High mobility n- and p-type III-V metalorganic vapour phase epitaxy thin films on amorphous substrates, Journal of Physics: Photonics 2(2), 2020, DOI: 10.1088/2515-7647/ab7557.

Author contributions:

A. Curran - experimental planning, Hall analysis, Transmission Electron Microscopy (TEM) analysis, device fabrication, electrical characterisation

E. Secco - III-V film growth

A. Pescaglini - III-V film growth

A. Gocalinska - III-V film growth and Atomic Force Microscopy (AFM)

K. Thomas - III-V film growth

R. E. Nagle - Scanning Electron Microscopy (SEM) imaging

B. Sheehan - TEM analysis

I. M. Povey - Atomic Layer Deposition (ALD) oxide growth

E. Pelucchi - concept, design of experiment

C. O'Dwyer - analysis, supervision

P. K. Hurley - analysis, design of experiment, concept, supervision

F. Gity - concept, design of experiment, device processing, supervision

3.1 Abstract

Poly InAs films described in Chapter 2 are explored as a low temperature n -channel semiconductor material in a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) structure. Test structures fabricated with an Al_2O_3 top-gate dielectric show that transistor-type behaviour is possible when poly InAs films are implemented as the channel material. A maximum $I_{\text{ON}}/I_{\text{OFF}}$ 1.3×10^4 is achieved at -50°C , and $I_{\text{ON}}/I_{\text{OFF}} = 363$ at room temperature for back-gated devices. Factors limiting the $I_{\text{ON}}/I_{\text{OFF}}$ ratio are investigated, and different device structures are explored as solutions, including dual-gated and buried-channel architectures. Recommendations are made for the future implementation of poly InAs.

3.2 Introduction

As described in Section 1.1, there is an ever-increasing need for low temperature grown materials which can be used as channel materials in transistor-type devices. The poly InAs films were optimized for use in a junctionless transistor architecture using Zn counter-doping to reduce the carrier concentration [1]. Junctionless transistors are a favourable architecture in the era of ultra-scaling, as they do not require an extreme doping gradient under the source and drain contacts leading into the channel [2]. However, there are many considerations that must be put into the careful design of these devices.

In this chapter we investigate the properties of these devices and compare them to those found in the literature. Although a 2D electron gas marks a departure from traditional transistor physics, functional InAs thin film transistors have been demonstrated through a process of bonding crystalline InAs to a silicon substrate [3, 4]. Direct growth on a silicon substrate will mark an important step towards poly InAs based devices which can be integrated in the back-end-of-line (BEOL).

3.3 Experimental

Top-gated transistor test devices were fabricated, utilizing the poly InAs films as their channel material. Patterning of contacts was achieved using photolithography. Source/drain contact metal Au(14 nm):Ge(14 nm):Au(14 nm): Ni(11 nm):Au(200 nm) was deposited by e-beam evaporation, and defined using a standard lift-off process. The definition of the channel and source/drain regions was performed using a wet etch of 20:1 $\text{C}_6\text{H}_5\text{O}_7:\text{H}_2\text{O}_2$ (etch rate >2 nm/s). Surface passivation was achieved using a 10 min dip in room temperature 10% $(\text{NH}_4)_2\text{S}$ [5]. Following the surface treatment, 15 nm Al_2O_3 gate dielectric was deposited by ALD using Trimethyl Aluminium (TMA) precursor and H_2O , followed by 200 nm palladium (Pd) gate contact, deposited by e-beam evaporation. Electrical characteristics of the devices, both at room temperature and variable temperatures, were extracted using a semiconductor device parameter analyser Agilent B1500,

and a semi-automatic Cascade probe station. Electrical results for devices presented in the chapter were chosen as they either represented the “best” results achieved, or were devices capable of being measured on multiple samples to allow for comparison.

Time-Of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS) was performed, and the results analysed, in Intel Ireland.

3.4 Results and Discussion

3.4.1 Top-Gated Poly InAs Junctionless Transistors

Top-gated transistor test devices were fabricated using a heterostructure consisting of 25 nm poly GaAs + 10 nm Zn-doped poly InAs(P) as the channel material. As mentioned previously, phosphorus was included as a surfactant during the growth process. Figure 3.1a shows a schematic of the film structure taken through the gate stack, and Figure 3.1b shows a schematic plan-view representation of the device structures fabricated, where L_{ch} is the length of the channel, L_{g} is the length of the gate, and W_{ch} is the width of the channel.

Based on previous research [5], it was decided to omit BOE and HCl treatments (described in Section 2.4.2) prior to gate oxide deposition during top-gated transistor device fabrication and proceed with $(\text{NH}_4)_2\text{S}$ alone. Am-

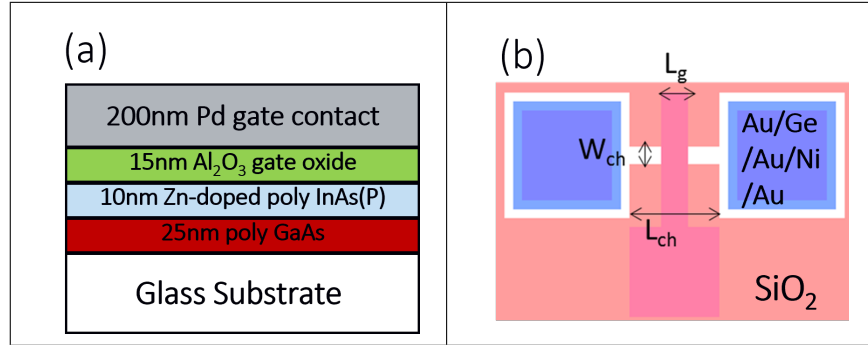


Figure 3.1: (a) Schematic cross-section of the film structure in the channel region of the device, and (b) plan-view of device layout.

monium sulfide has been shown to remove InAs surface oxides, however it can have deleterious effects, damaging the patterns previously etched, and forming an undercut. These effects are mitigated through the sulfurization of the surface by the $(NH_4)_2S$ itself, and dilution of the $(NH_4)_2S$ solution before use [6]. For this reason, a 10 min dip in a 10% $(NH_4)_2S$ solution was used as the surface treatment of the poly InAs film [5]. Following the etching of the GaAs/InAs to form the active area of the device, and surface treatment, the Al₂O₃ top oxide was formed by ALD. The ALD process is also reported to be effective for reducing or removing native oxides present on the III-V surface [7].

Electrical characterisation was performed on the top-gated transistor test devices, These are presented in Figure 3.2, where L_{ch} is the channel length, W_{ch} is the channel width, L_{gate} is the length of the gate, V_{GS} is the voltage as measured at the gate, I_{DS} is the current as measured at the drain, and V_{DS}

is the voltage as measured at the drain. Output characteristics, Figure 3.2a, show classical transistor behaviour with clear linear and saturation regions whose onset vary with V_{GS} . Transfer characteristics are shown in Figure 3.2b. The clockwise hysteresis observed in the transfer characteristics, see Figure 3.2, originates from trapping and de-trapping of electrons in the Al_2O_3 gate oxide. It is evident that the drain-source current can be modulated using the gate voltage, and I_{ON}/I_{OFF} of 90 is achieved at room temperature. The threshold voltage for this device was determined by extrapolation from the maximum transconductance and is found to be -2.16 V. Field effect mobility is calculated using the transconductance from:

$$g_m = \frac{W}{L} \cdot \mu \cdot C_{ox} \cdot V_{DS} \quad (3.4.1)$$

where g_m is the transconductance, W is the width of the channel, L is the length of the channel, μ is the carrier mobility, C_{ox} is the oxide capacitance and V_{DS} is the voltage measured at the drain. The total resistance (V_{DS}/I_{DS}) is extracted as a function of V_{GS} . From the resistance and channel dimensions, resistivity, and hence conductivity, is calculated. Using the formula for conductivity the carrier concentration can be calculated:

$$\sigma = n \cdot \mu \cdot q \quad (3.4.2)$$

where σ is the conductivity, n is the carrier concentration, μ is the carrier mobility and q is the electronic charge. As the parameters from which it is

extracted are functions of V_{GS} (the voltage as measured at the gate), carrier concentration is also V_{GS} dependent.

Carrier mobility and concentration values for this film were measured through Hall effect measurements prior to device processing and were found to be $18 \text{ cm}^2/\text{Vs}$ and $7.7 \times 10^{15} \text{ cm}^{-3}$, respectively. Field effect mobility, Figure 3.2c, peaks at around $7 \text{ cm}^2/\text{Vs}$, exhibiting a reduction in mobility compared to the Hall effect measurements, as expected for the transistor structure. The carrier concentration, Figure 3.2d, is in excess of the $7.7 \times 10^{15} \text{ cm}^{-3}$ determined from Hall analysis. The increase in the electron concentration is consistent with the observation from other works that ALD deposited Al_2O_3 , prior to any post deposition annealing, exhibits a net positive fixed oxide charge density for film thickness values above 5 nm. Based on values previously reported [8], the 15 nm Al_2O_3 would exhibit an equivalent net positive charge density of around $5.5 \times 10^{12} \text{ cm}^{-2}$ at the InAs/ Al_2O_3 interface. The corresponding electrostatically induced negative charge in the InAs of $5.5 \times 10^{12} \text{ cm}^{-2}$ is equivalent to $5.5 \times 10^{18} \text{ cm}^{-3}$ based on the nominal thickness of the 10 nm poly InAs film. This is consistent with the levels of channel charge determined for the InAs transistor around the threshold voltage.

While the drain-source current values above the threshold voltage are in good agreement with Hall mobility value prior to device processing, the OFF-state current limits the I_{ON}/I_{OFF} ratio of the device. The origin of

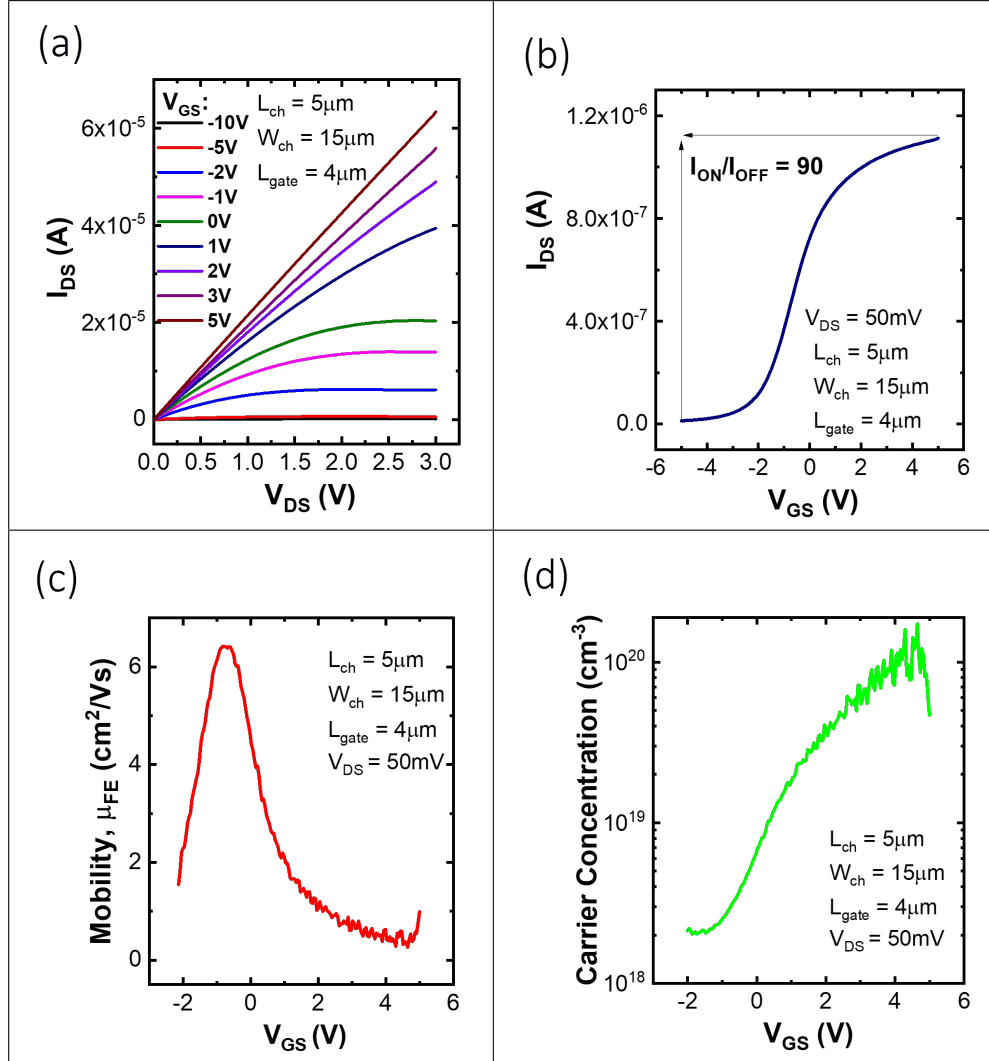


Figure 3.2: (a) Device output and (b) transfer characteristics at room temperature. (c) Field-effect mobility, and (d) carrier concentration extracted from transconductance. The device dimensions and bias conditions are shown in the inset of each figure.

the OFF-state current was investigated by varying the substrate and InAs parameters. Transistor test devices with Si/SiO₂ or glass substrates, and the presence/absence of a poly GaAs buffer layer were tested to rule out either of these variables as detrimental to the I_{ON}/I_{OFF} ratio. All the samples shown in Figure 3.3 exhibited comparable values of: gate modulation, hysteresis in the transfer characteristics, and a I_{ON}/I_{OFF} ratio when measured at room temperature. This ruled out the substrate and parasitic conductance through the GaAs buffer layer as the cause of the high OFF-state current.

Temperature dependent current-voltage measurements were performed to gain further understanding of the physical process limiting the I_{ON}/I_{OFF} ratio. Results are presented for InAs channel transistors. Schematic cross-section of each sample is shown with the corresponding variation of I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} with temperature in Figure 3.4. From these results, it is noted that the I_{ON}/I_{OFF} ratio is much more temperature dependent for the sample with a poly GaAs buffer layer than that without, with the higher values for each being >250 and around 10 respectively.

When components of the I_{ON}/I_{OFF} ratio are separated out, the difference in the final ratio is seen to be due to a lower I_{OFF} for the sample with a poly GaAs buffer layer. I_{ON} is comparable in both samples and is not observed to be strongly temperature dependent. One possible explanation for this is potential Ga incorporation into the poly InAs channel during growth, widening

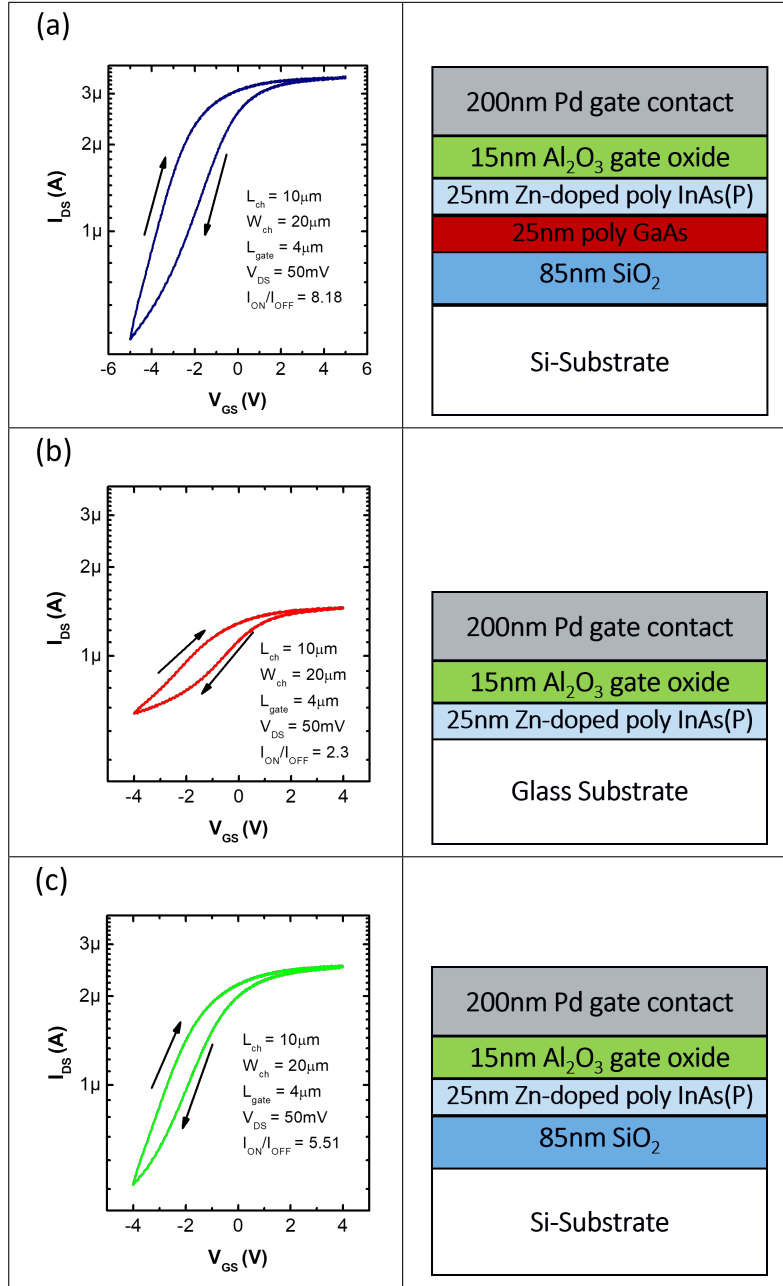


Figure 3.3: Transfer characteristics of (a) 25 nm GaAs + 25nm Zn-doped InAs(P) on a Si/ SiO_2 , (b) 25 nm Zn-doped InAs(P) grown directly on glass, and (c) 25 nm Zn-doped InAs directly on Si/ SiO_2 . Structures through the channel region are shown beside each transfer characteristic.

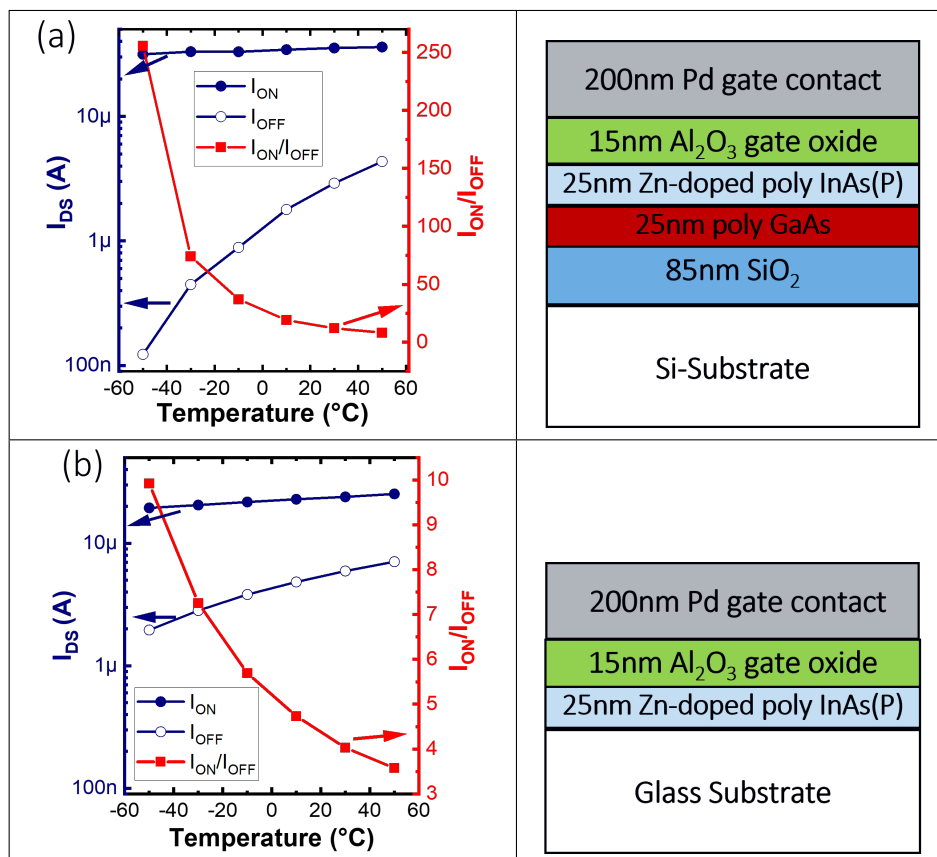


Figure 3.4: I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} for (a) 25 nm GaAs + 25 nm Zn-doped InAs(P), and (b) 25 nm Zn-doped poly InAs on glass. Schematics of the sample taken through the gate stack are shown beside the corresponding results.

the energy gap due to the larger bandgap of GaAs (1.4 eV) compared to InAs (0.36 eV), and thereby allowing a lower I_{OFF} to be achieved. The presence of a low level of Ga in the InAs channel was confirmed through TOF-SIMS. The results of this analysis are shown in Figure 3.5. During TOF-SIMS, an elemental depth profile of a number of different elements was generated. It was known that due to the roughness of the film, the nominal thickness would differ somewhat from the actual thickness. Using the nominal thicknesses as a rough guide (as seen in Cross-sectional Transmission Electron Microscopy (XTEM) images e.g. Fig 2.4 the actual thickness of the layers differs from the nominal thickness), and looking at the depth profile of each element, the approximate depth of each layer was determined (marked by blue lines in the images). There is a sharp drop-off in the level of In present at the level which was assigned as the interface between InAs and GaAs. Arsenic (Figure 3.5c) peaks throughout the two layers, and the peak of the In (Figure 3.5b) has relatively sharp drop-offs on either side, whereas Ga (Figure 3.5a) levels peak somewhat into the depth region assigned to InAs. Importantly, it is clear that there is an overlap in the peaks of Ga and In, indicating mixing of InAs and GaAs at the interface.

3.4.2 Dual-Gated Poly InAs Junctionless Transistors

Both of the nominally 25 nm films shown in Figure 3.4 failed to achieve similarly high room temperature $I_{\text{ON}}/I_{\text{OFF}}$ ratios as the 10 nm films shown in Figure 3.2. It has been shown that In diffusion into the SiO_2 layer can

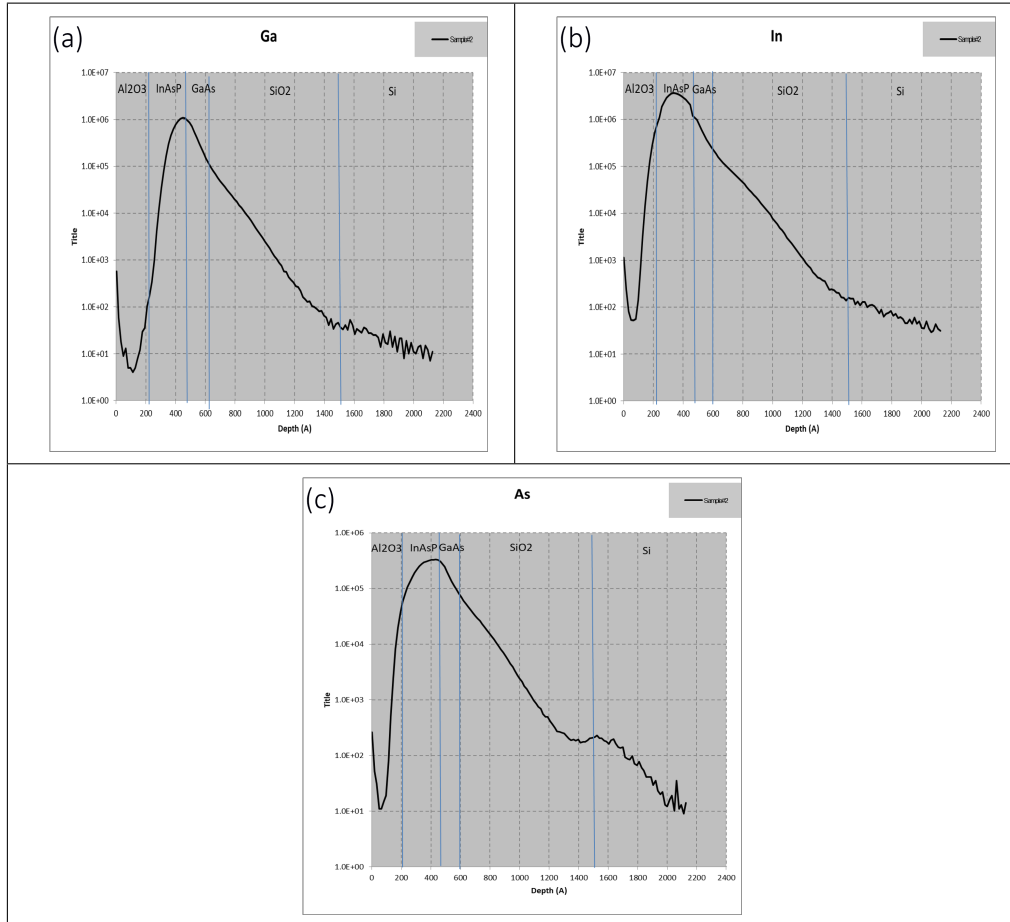


Figure 3.5: TOF-SIMS results showing level of (a) Ga, (b) In, and (c) As vs depth from the surface, taken from sample shown in 3.4a.

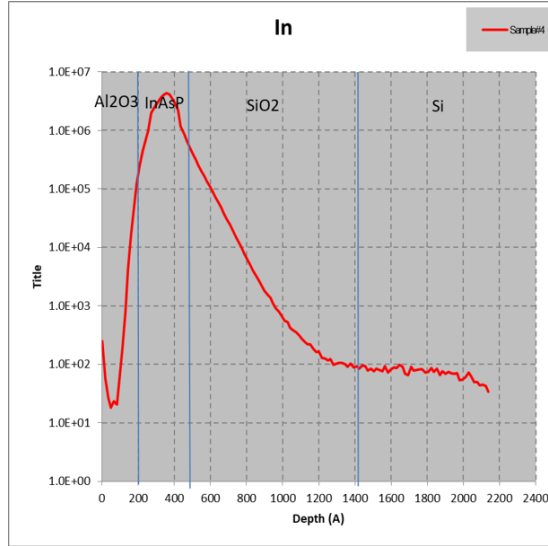


Figure 3.6: TOF-SIMS results showing the depth profile of In in a sample consisting of 25 nm Zn-doped InAs(P) directly on an Si/SiO₂ substrate.

occur during growth at certain temperatures [9]. This could create a conductive path outside the control of the gate; however, this possibility was ruled out due to the lower temperatures used during the growth compared to the cited paper (the paper studies film growth temperatures in the range of 800-1000°C), and the TOF-SIMS results for the sample pictured in Figure 3.3, which are shown in Figure 3.6. These results show no evidence of In diffusion into the SiO₂ layer.

The theoretical maximum depletion width vs carrier concentration is shown in Figure 3.7, and the equation used is shown in the inset. For the carrier concentrations present in these films, the maximum depletion width is comparable to the nominal thicknesses of the InAs films. However, from the

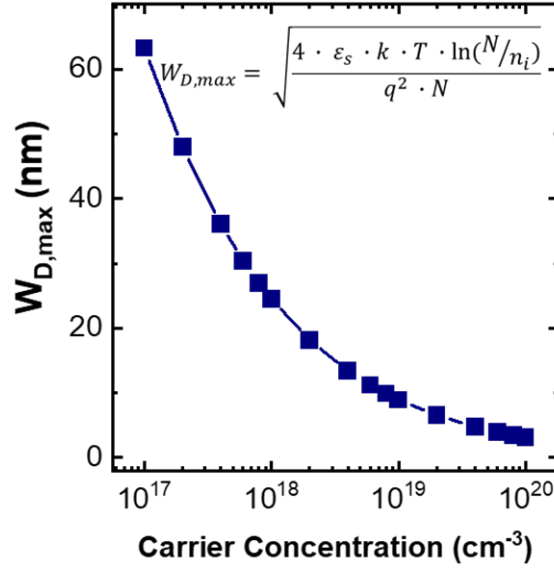


Figure 3.7: Maximum depletion width vs carrier concentration for InAs films. Inset: equation used for plotting.

XTEM images (see Figure 2.2 in Chapter 2) we know that the actual thickness can be greater than the nominal thickness. From Figure 3.2, we also know that the carrier concentration is strongly field dependent and increases by around 2 orders of magnitude over the gate bias range of -2 V to +5 V (10^{18} - 10^{20}).

Based on the information in Figure 3.7 and the decrease in I_{ON}/I_{OFF} with increasing InAs film thickness, the possibility that the channel was not being fully depleted was investigated. If the InAs layer is not fully depleted, this would leave a resistive conduction path at the InAs/substrate or InAs/GaAs interface, which is not modulated by the top-gate voltage. Figure 3.8a shows

the I_{OFF} dependence on channel length for the 25 nm Zn-doped InAs sample on glass. The I_{OFF} vs L relationship shows a slope close to -1, implying a $1/L$ relationship, which would be expected for a resistor. The I_{OFF} proportional to $1/L$ is also obtained for the 25 nm Zn-doped InAs(P) with a GaAs buffer layer. As can be seen from the device architecture shown in Figure 3.1b, the ratio of gate length to channel length can be varied. Measurements were conducted over a range of gate lengths with fixed channel length and width to determine how efficiently the gate was controlling the channel. Results from the sample consisting of 25 nm Zn-doped InAs(P) grown directly on glass, shown in Figure 3.4b, are plotted in Figure 3.8b. This figure shows that the greater the proportion of the channel that is gated, the greater the $I_{\text{ON}}/I_{\text{OFF}}$ ratio, with both I_{ON} and I_{OFF} components being affected. However, when the entirety of the channel is gated, i.e., both L_{ch} and $L_{\text{gate}} = 50 \mu\text{m}$, I_{OFF} is still significantly higher than expected for this film. Due to this, and the resistor-like behaviour in Figure 3.8a, it can be concluded that the channel is not being entirely depleted.

For this reason, it was decided to fabricate and test dual gated devices. This structure should, in theory, double the maximum depletion width possible, potentially alleviating the incomplete depletion of the total channel thickness. As the films were grown directly on the substrate, it was necessary to select a film which had been grown on SiO_2 and did not have a GaAs buffer layer, so that back-gating through the substrate could be achieved. A

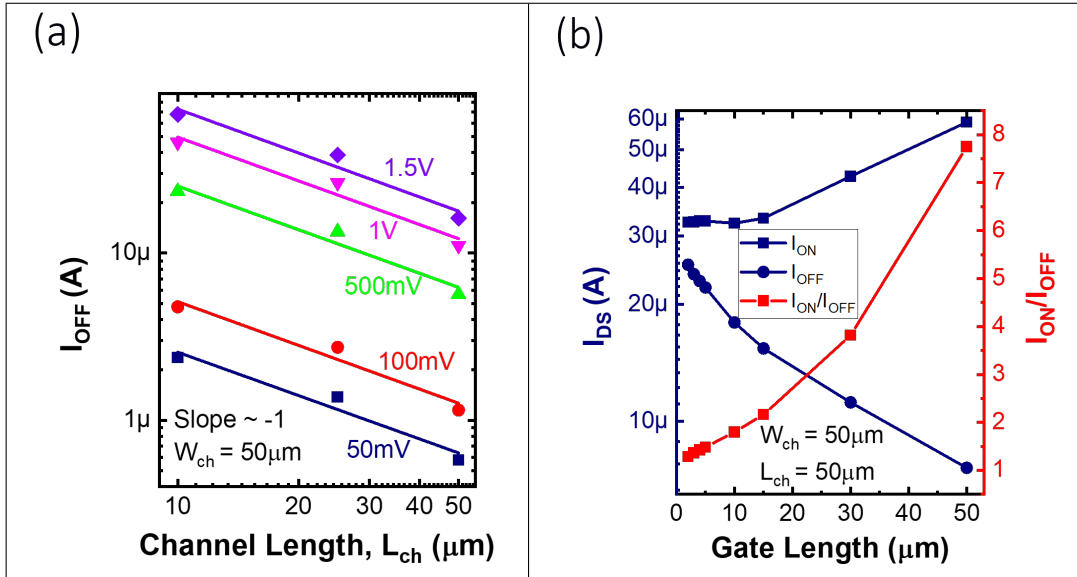


Figure 3.8: (a) I_{OFF} dependence on channel length for 25 nm InAs grown directly on glass, with V_{DS} values shown ($V_{\text{GS}} = 5\text{V}$). (b) I_{ON} , I_{OFF} , and $I_{\text{ON}}/I_{\text{OFF}}$ vs gate length for the same sample ($V_{\text{DS}} = 1\text{ V}$, I_{ON} $V_{\text{GS}} = 5\text{ V}$, I_{OFF} $V_{\text{GS}} = -5\text{V}$). Note: the channel length (L_{ch}) is the separation between the source and drain contacts and the gate length is the width of the gate metal (see Figure 3.1b).

25 nm Zn-doped InAs film on Si/SiO₂ was chosen as the Zn doping reduces the carrier concentration in the film, which is favourable for depletion of the channel. Table 3.1 shows the Hall effect measurement results from the film chosen for dual gated device fabrication. It is clear that the Zn-doping has decreased the carrier concentration in the film by over an order of magnitude when compared to the concentrations shown in Table 2.1. This is beneficial for achieving full depletion of the channel.

Film	Mobility (cm ² /Vs)	Carrier Conc (cm ⁻³)	Resistivity (Ω·cm)
25nm Zn-doped InAs	83.3	3.56x10 ¹⁷	0.21

Table 3.1: Hall effect measurement results of 25 nm Zn-doped InAs on SiO₂.

Figure 3.9a shows back-gated transfer characteristics of the InAs sample, prior to any surface treatments or oxide deposition, measured at room temperature. These measurements resulted in a I_{ON}/I_{OFF} ratio around 3-4 times higher than the sample shown in Figure 3.3c. When comparing the measurements taken with the same V_{DS} , it's evident that this increase is due to a lower I_{OFF} , with the I_{ON} being relatively comparable. This could be because this sample did not yet have a top oxide, the deposition of which results in an increase in carrier concentration, making it more difficult to deplete the channel. However, if this were the case, it would be expected to display a higher I_{ON} also. It has been shown that mobility decreases with an increase in carrier concentration in bulk InAs [10]. As there were no major changes in growth procedure between the two films, this could explain the difference

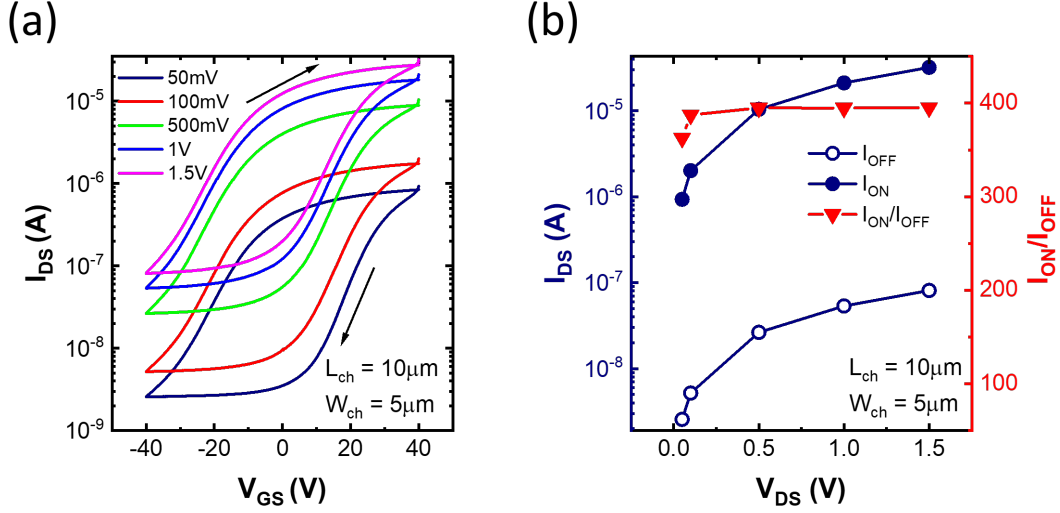


Figure 3.9: (a) Transfer characteristics of 25 nm Zn-doped InAs film on Si/SiO₂. (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} taken from the same measurements.

in results. There is a large clockwise hysteresis present in all of the measurements which is indicative of electron trapping and de-trapping. For the samples shown in Figure 3.3, electron trapping and de-trapping in the Al₂O₃ was deemed to be responsible for the observed hysteresis. Here, the sample has not received a surface treatment or gate dielectric deposition. The hysteresis is also much larger than in the samples shown in Figure 3.3, suggesting that the mechanism of electron trapping and de-trapping is different. It is likely happening at the surface where native oxides are present. These are removed during the surface treatment, and so this effect would not be prominent in the samples which have received the surface treatment. Figure 3.9b shows the I_{ON}/I_{OFF} ratios at different V_{DS} , with the two components separated out.

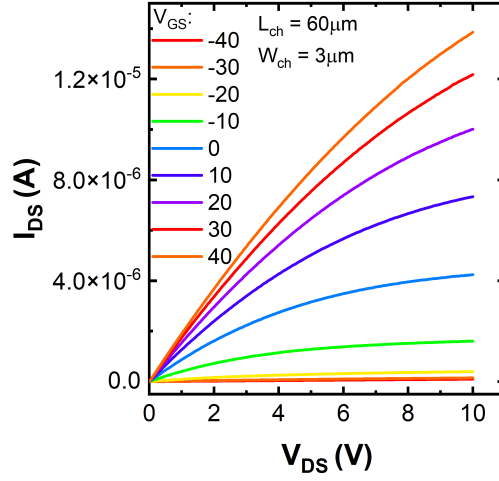


Figure 3.10: Output characteristics of 25 nm Zn-doped InAs film on Si/SiO₂.

Back-gated output characteristics for the InAs film are shown in Figure 3.10. These results show similar “classical transistor” behaviour to the top-gated results shown in Figure 3.2a.

Temperature dependent back-gated measurements were also carried out on the sample whose results are shown in Figure 3.9. The sample showed a similar pattern as to that shown in Figure 3.4, whereby I_{ON} is minimally affected by temperature, I_{OFF} is strongly affected by temperature, and I_{ON}/I_{OFF} decreases with increasing temperature. This sample again showed a large improvement on the I_{ON}/I_{OFF} values previously seen, reaching up to 1.3×10^4 at -50°C . This improvement is mainly seen in the I_{OFF} , implying once again that the greater carrier concentration caused by deposition of the gate oxide

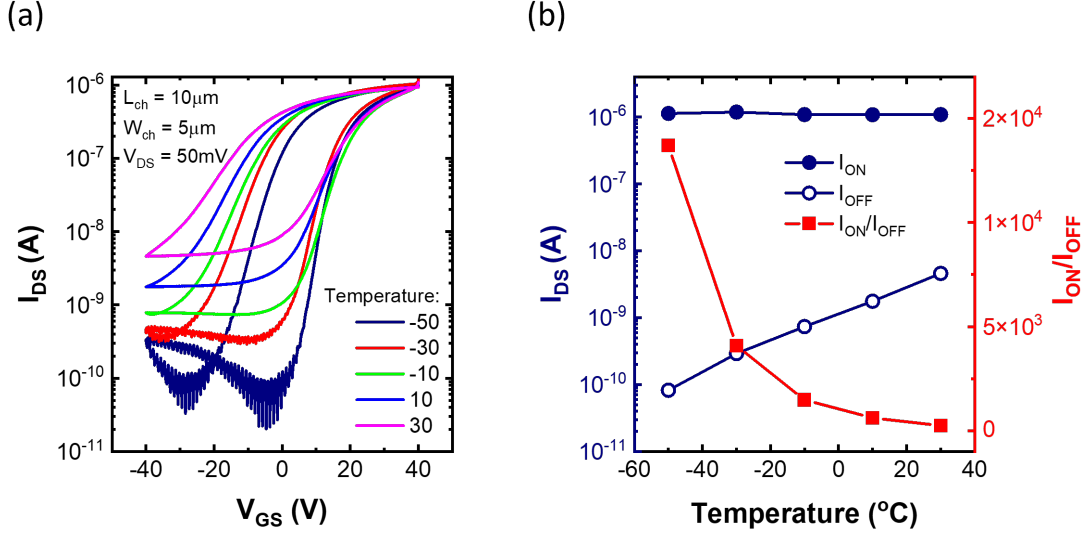


Figure 3.11: (a) Transfer characteristics of 25 nm Zn-doped InAs film on Si/SiO₂ at variable temperatures. (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} taken from the same measurements.

is detrimental to the OFF-current of these devices.

As with the previous top-gated InAs transistors, described in Section 3.4.1, a 10 minute dip in 10% (NH₄)₂S was performed before deposition of the 20 nm Al₂O₃ gate dielectric by ALD. An annealing step was carried out to improve the properties of the gate oxide and the interface between the oxide and the channel. Based on previous research [11], a 30 minute Forming Gas Anneal (FGA) at 300°C was chosen.

Figure 3.12 shows the results of dual gating the Zn-doped InAs channel at room temperature. Figure 3.12a shows the transfer characteristics when the

top gate is swept from +5 V to -6 V, with the back gate being held at a constant potential indicated by the legend. It is clear that the large hysteresis present in the transfer characteristics in Figure 3.9 before top-gating has been significantly reduced, confirming that it is a result of trapping and de-trapping in the native oxide formed at the top InAs surface. The I_{ON}/I_{OFF} ratio is comparable to that prior to top-gating, however it is achieved over a much smaller range of gate voltage. For devices with the same dimensions (see Table 3.2 for summary) the OFF-state current has been reduced from $5.14 \times 10^{-4} \mu\text{A}/\mu\text{m}$ for back-gate only to $1.12 \times 10^{-4} \mu\text{A}/\mu\text{m}$ with both gates. However, the ON-state current has also been reduced from $0.19 \mu\text{A}/\mu\text{m}$ to $0.019 \mu\text{A}/\mu\text{m}$. This could be partly due to the workfunction of the gate metal depleting the channel of carriers, however, it is more likely due to the fact that when the back gate is swept it electrostatically dopes the source and drain regions, reducing the contact resistance and allowing for a higher ON-current. From Figure 3.12b, it can be seen that the potential at which the back gate is held has a large influence on the transfer characteristics, particularly the OFF-state current.

The measurements were performed in the manner described above due to the nature of the oxides on each side of the channel. For a typical dual-gated structure, both gates would have a specifically designed gate stack, however, while the top-gate in these devices is specifically designed, the back-gate is contacted through the substrate and the thicker SiO_2 oxide acts as the gate

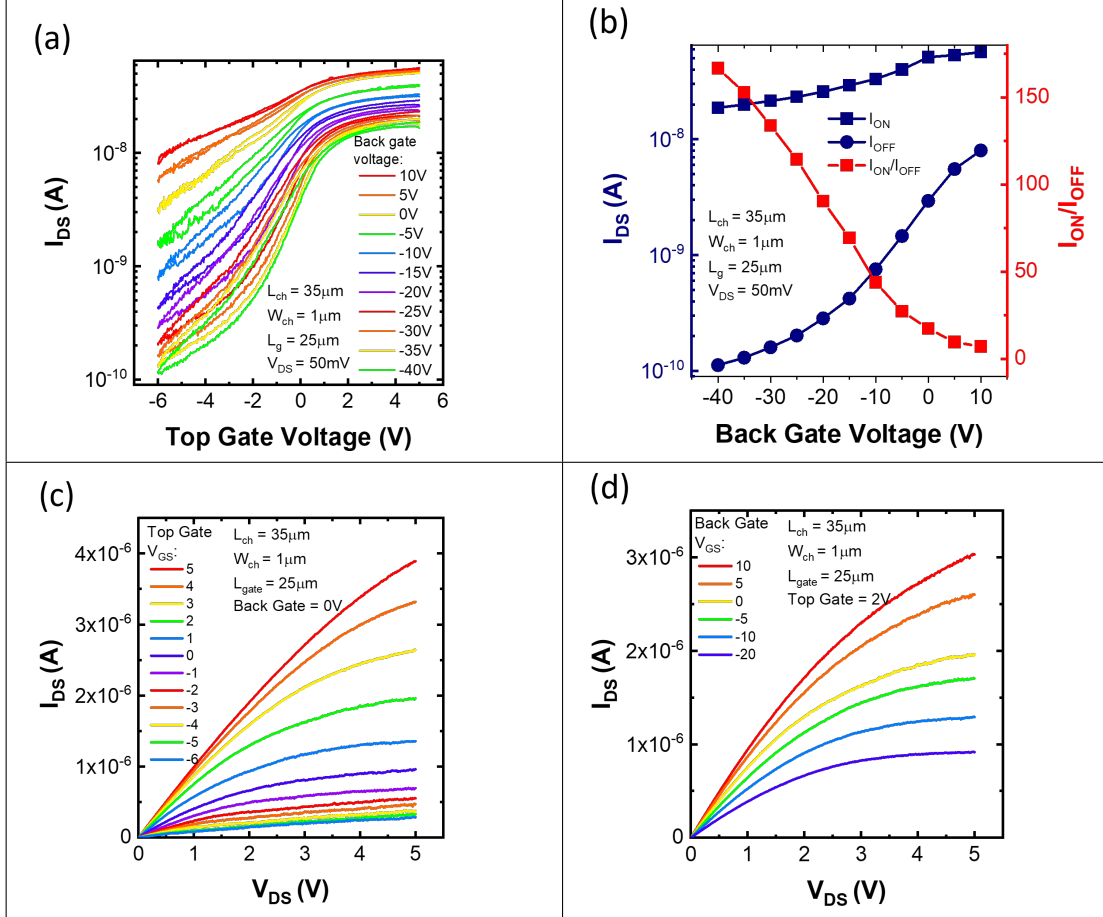


Figure 3.12: (a) Transfer characteristics of 25 nm Zn-doped InAs film on Si/SiO₂ with back gate potential shown in inset. (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} taken from the same measurements and shown vs back gate potential. I_{ON} was taken at a top gate voltage of +5 V and I_{OFF} was taken at a top gate voltage of -6 V. Output characteristics with (c) a constant back-gate voltage of 0V and (d) a constant top-gate voltage of 2 V. Device dimensions are shown in inset.

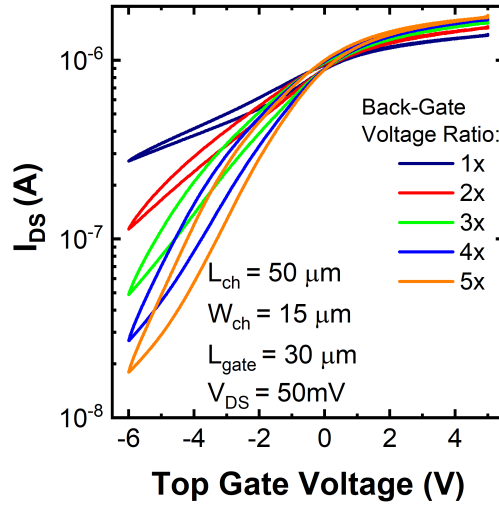


Figure 3.13: Transfer characteristics of 25 nm Zn-doped InAs film on Si/SiO₂ channel device with different ratios of back-gate to top-gate voltage.

dielectric. Further measurements were performed with a more typical set up of shorting both gates, however a ratio was implemented to allow the back-gate to be swept over a wider range at the same time as the top-gate sweep. Figure 3.13 shows the resulting transfer characteristics for a device with different ratios of the gate voltages included for comparison. It is clear that a wider sweep of the back gate along with the top-gate voltage is the optimal condition for higher I_{ON}/I_{OFF} ratios, with the OFF-current being particularly affected by the back-gate sweep range. The highest I_{ON}/I_{OFF} ratio, 100, is achieved when the back-gate is swept 5x the range of the top-gate. The transfer characteristics still display a clockwise hysteresis, albeit significantly reduced compared to the back-gate only results in Figure 3.9a.

A device with different dimensions than the back-gated results was chosen for Figure 3.12 and 3.13 as these gave the best I_{ON}/I_{OFF} values, however a direct comparison of the same devices (dimensions the same as results shown in Figure 3.9) pre and post top gating and with shorted gates can be seen in Table 3.2. A subthreshold swing value is not presented for the shorted gates measurement as there are two sweeps of different ranges for the gate voltage against which this value could be calculated. Transfer characteristics measured at -50°C are also presented for comparison purposes. Here we see that the back-gate only measurement prior to top-gating maintains about an order of magnitude improvement on the I_{ON}/I_{OFF} value compared to any of the top-gated results. The improved values for the back-gate only are seen to be mainly due to a lower I_{OFF} value. This would likely be easier to achieve prior to top gating as the Al_2O_3 gate dielectric induces a higher electron density in the InAs channel, making it more difficult to deplete.

Gating	Temp ($^{\circ}\text{C}$)	I_{ON} ($\mu\text{A}/\mu\text{m}$)	I_{OFF} ($\mu\text{A}/\mu\text{m}$)	I_{ON}/I_{OFF}	SS (mV/dec)
Back-gated	RT	0.19	5.14×10^{-4}	363	10896
Dual-gated	RT	0.091	6.43×10^{-3}	14	4347
Shorted Gates	RT	0.46	6.68×10^{-3}	69	-
Back-gated	-50	0.23	4.06×10^{-6}	1.3×10^4	4166
Shorted Gates	-50	0.48	1.7×10^{-4}	2.83×10^3	-

Table 3.2: Transfer characteristics data for 25 nm Zn-doped InAs film on Si/SiO₂ pre and post top gating. Device dimensions are $L_{ch} = 10 \mu\text{m}$, $W_{ch} = 5 \mu\text{m}$, and $L_{gate} = 4 \mu\text{m}$.

An attempt at fabricating and measuring InAs buried channel devices is discussed in Appendix C.

3.5 Benchmarking

Table 3.3 shows a selection of the devices fabricated and measured in this chapter compared to devices demonstrated in the literature. When making this comparison it is important to remember that the materials in this chapter are polycrystalline and grown on amorphous substrates. All the other reports are for crystalline InAs channels. As discussed in Section 1.2.1, there are additional factors affecting the performance and adding to the defect density for polycrystalline materials when compared to crystalline, including grain size/orientation and effects at the grain boundaries [12–14]. The table highlights the following effects of moving from a crystalline channel to a polycrystalline InAs channel formed on SiO₂ or glass below 500°C:

1. A degradation in the subthreshold slope resulting from an increased density of interface and oxide defects and defects within the energy gap of the InAs. Note that for our samples the oxides are also thicker, which degrades the subthreshold slope via the equation:

$$S = \frac{kT}{q} \cdot \ln 10 \cdot \left(1 + \frac{(C_D + C_{it})}{C_{ox}} \right) \quad (3.5.1)$$

For this reason, the subthreshold figures in Table 3.3 are presented as

$SS \cdot C_{ox}$ to allow for a more accurate comparison.

2. A reduction of the ON current due to the reduced mobility compared to crystalline InAs.
3. Comparable OFF state currents can be achieved.

3.6 Conclusions

Surface treatments and device processing methods were developed, resulting in functional top-gated transistor test structures based on the polycrystalline InAs thin films. Through temperature dependent measurements, it was found that I_{OFF} limits the final I_{ON}/I_{OFF} ratio. The OFF-state current originates from incomplete depletion of the full InAs layer thickness, indicating the use of thinner poly InAs films, combined with planarization techniques should be used to maximise the performance of this semiconductor channel for applications where the thermal budget is restricted. Dual-gating managed to achieve better electrostatic control of the channel, seen by the improvement in subthreshold swing. A device where both gates have well engineered stacks will achieve the greatest control. Finally, it is noted that there is considerable scope for III-V heterostructure designs in conjunction with the low temperature grown poly InAs thin films to optimise the device performance for applications including flexible wearable electronics, display technologies, and back-end-of-line integration.

III-V Material	L (μm)	I _{ON} ($\mu\text{A}/\mu\text{m}$)	V _{ON} (V)	I _{OFF} ($\mu\text{A}/\mu\text{m}$)	V _{OFF} (V)	V _{DS} (V)	I _{ON} /I _{OFF}	SS-C _{ox} ($\frac{\text{e}^{-\text{A}}}{\text{dec}\cdot\text{m}^2} \cdot 10^{-3}$)	Device Type	Growth Substrate	Year	Ref
InAs	7.4	33	5	0.002	-1	0.5	1x10 ⁴	-	NW FET	AlGaSb	2018	[15]
InAs	7.2	60	0.4	0.002	-0.5	0.5	1x10 ⁴	1.4	XOI FET	GaSb	2013	[4]
InAs	2.5	0.2	1	0.001	-0.1	0.1	100	4.62	XOI TFET	AlGaSb	2011	[16]
InAs/ In-GaAs	0.26	330	0.8	0.1	-0.4	0.5	1000	9.59	Vertical MOS-FET	Si	2017	[17]
InAs/ In-GaAsSb/ GaSb	0.25	10.3	0.3	0.001	-0.1	0.3	1x10 ⁴	1.1	NW TFET	InAs	2017	[18]
InAs	0.02	30	1	0.003	-0.75	0.05	1x10 ⁴	2.01	NW nFET	GeOI	2015	[19]
InGaAs	0.1	50	2	0.005	-0.5	0.05	1x10 ⁴	2.47	TFET	InP	2010	[20]
InGaAs	100	0.7	0.8	9x10 ⁻⁷	-0.2	0.1	1x10 ⁶	17.9	TFET	InP	2017	[21]
GaAsSb/ InGaAs	0.5	0.002	1	3x10 ⁻⁶	-1	0.05	1000	-	Vertical TFET	InP	2019	[22]
InGaAs/ InAs/ InGaAs	50	6	1	6x10 ⁻⁶	-0.25	0.05	1x10 ⁶	1.07	Buried Channel MOS-FET	InP	2011	[23]
InP	1	20	0	5x10 ⁻⁵	2	0.23	4x10 ⁵	3.03	MOSFET	InP	2019	[24]
InAs	0.03	80	0.6	0.6	-0.2	0.5	133	5.84	MOSFET	InP	2018	[25]
In _{0.7} Ga _{0.3} As	2	10	0.5	0.001	-0.2	0.05	1x10 ⁴	4.66	QW	InP	2015	[26]
InAs	2	10	0.5	5x10 ⁻⁴	-0.2	0.05	2x10 ⁴	3.55	QW	InP	2015	[26]
InAs	2	10	0.5	7x10 ⁻⁴	-0.2	0.05	1.5x10 ⁴	3.76	Dual QW	InP	2015	[26]
InAs	1	40	0.5	0.02	-0.5	0.5	2000	5.76	FinFET	InAs	2016	[27]
InAs	2.85	-	1	-	0	1	2x10 ⁴	1.64	nMOS	SiO ₂	2012	[28]
InAs	50	0.2	2	0.002	-1.5	0.05	100	-	nMOS	InAs	2014	[29]
GaAs + 10nm Zn-InAs(P)	5	0.074	5	8.3x10 ⁻⁴	-5	0.05	90	11.4	Top-Gate Junctionless	Glass	2018	This Work
25nm poly Zn-InAs	10	0.19	40	5.14x10 ⁻⁴	-40	0.05	363	43.4	Back-gate Junctionless	SiO ₂	2021	This Work
25nm poly Zn-InAs	35	0.019	5	1.12x10 ⁻⁴	-6	0.05	167	8.36	Dual-Gate Junctionless	SiO ₂	2022	This Work

Table 3.3: Examples of functional *n*-type III-V based transistors from the literature with results from this chapter included for comparison.

Bibliography

- [1] J.-P. Colinge, A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, and P. Razavi, “Junctionless nanowire transistor (JNT): Properties and design guidelines,” *Solid-State Electronics*, vol. 65, pp. 33–37, 2011.
- [2] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O’Neill, A. Blake, M. White, *et al.*, “Nanowire transistors without junctions,” *Nature nanotechnology*, vol. 5, no. 3, pp. 225–229, 2010.
- [3] S.-H. Kim, M. Yokoyama, R. Nakane, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi, “High performance tri-gate extremely thin-body InAs-On-Insulator MOSFETs with high short channel effect immunity and V_{th} tunability,” *IEEE Transactions on Electron Devices*, vol. 61, no. 5, pp. 1354–1360, 2014.
- [4] K. Takei, R. Kapadia, H. Fang, E. Plis, S. Krishna, and A. Javey, “High quality interfaces of InAs-on-insulator field-effect transistors with ZrO_2

-
- gate dielectrics,” *Applied Physics Letters*, vol. 102, no. 15, p. 153513, 2013.
- [5] É. O’Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, *et al.*, “A systematic study of $(\text{NH}_4)_2\text{S}$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ system for n -type and p -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial layers,” *Journal of Applied Physics*, vol. 109, no. 2, p. 024101, 2011.
- [6] A. Gin, Y. Wei, A. Hood, A. Bajowala, V. Yazdanpanah, M. Razeghi, and M. Tidrow, “Ammonium sulfide passivation of type-II InAs/GaSb superlattice photodiodes,” *Applied physics letters*, vol. 84, no. 12, pp. 2037–2039, 2004.
- [7] S. Monaghan, A. O’Mahony, K. Cherkaoui, É. O’Connor, I. Povey, M. Nolan, D. O’Connell, M. Pemble, P. Hurley, G. Provenzano, *et al.*, “Electrical analysis of three-stage passivated $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors with varying HfO_2 thicknesses and incorporating an Al_2O_3 interface control layer,” *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 29, no. 1, p. 01A807, 2011.
- [8] P. K. Hurley, É. O’Connor, V. Djara, S. Monaghan, I. M. Povey, R. D. Long, B. Sheehan, J. Lin, P. C. McIntyre, B. Brennan, *et al.*, “The characterization and passivation of fixed oxide charges and interface states

- in the $\text{Al}_2\text{O}_3/\text{InGaAs}$ MOS system,” *IEEE Transactions on Device and Materials Reliability*, vol. 13, no. 4, pp. 429–443, 2013.
- [9] S. Solmi, A. Parisini, M. Bersani, D. Giubertoni, V. Soncini, G. Carnevale, A. Benvenuti, and A. Marmioli, “Investigation on indium diffusion in silicon,” *Journal of applied physics*, vol. 92, no. 3, pp. 1361–1366, 2002.
- [10] V. Karataev, M. Milvidskii, N. Rytova, and V. Fistul, “Compensation in n -type InAs,” *Soviet Physics-Semiconductors*, vol. 11, no. 9, pp. 1009–1011, 1977.
- [11] V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O’Connor, I. M. Povey, D. O’Connell, M. E. Pemble, and P. K. Hurley, “Impact of forming gas annealing on the performance of surface-channel $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs with an ALD Al_2O_3 gate dielectric,” *IEEE transactions on electron devices*, vol. 59, no. 4, p. 1084, 2012.
- [12] G. Harbeke, *Polycrystalline Semiconductors: Physical Properties and Applications: Proceedings of the International School of Materials Science and Technology at the Ettore Majorana Centre, Erice, Italy, July 1–15, 1984*, vol. 57. Springer Science & Business Media, 2012.
- [13] V. Šnejdar and J. Jerhot, “Electrical conductivity of polycrystalline semiconductors,” *Thin Solid Films*, vol. 37, no. 3, pp. 303–316, 1976.

- [14] F. Greuter and G. Blatter, “Electrical properties of grain boundaries in polycrystalline compound semiconductors,” *Semiconductor Science and Technology*, vol. 5, no. 2, p. 111, 1990.
- [15] S. H. Lee, S.-H. Shin, M. Madsen, K. Takei, J. Nah, and M. H. Lee, “A soft lithographic approach to fabricate InAs nanowire field-effect transistors,” *Scientific Reports*, vol. 8, no. 1, pp. 1–6, 2018.
- [16] A. C. Ford, C. W. Yeung, S. Chuang, H. S. Kim, E. Plis, S. Krishna, C. Hu, and A. Javey, “Ultrathin body InAs tunneling field-effect transistors on Si substrates,” *Applied Physics Letters*, vol. 98, no. 11, p. 113105, 2011.
- [17] O.-P. Kilpi, J. Svensson, J. Wu, A. R. Persson, R. Wallenberg, E. Lind, and L.-E. Wernersson, “Vertical InAs/InGaAs heterostructure metal–oxide–semiconductor field-effect transistors on Si,” *Nano letters*, vol. 17, no. 10, pp. 6006–6010, 2017.
- [18] E. Memisevic, M. Hellenbrand, E. Lind, A. R. Persson, S. Sant, A. Schenk, J. Svensson, R. Wallenberg, and L.-E. Wernersson, “Individual defects in InAs/InGaAsSb/GaSb nanowire tunnel field-effect transistors operating below 60 mV/decade,” *Nano letters*, vol. 17, no. 7, pp. 4373–4380, 2017.
- [19] K.-H. Goh, K.-H. Tan, S. Yadav, S.-F. Yoon, G. Liang, X. Gong, Y.-C. Yeo, *et al.*, “Gate-all-around CMOS (InAs n-FET and GaSb p-FET)

- based on vertically-stacked nanowires on a Si platform, enabled by extremely-thin buffer layer technology and common gate stack and contact modules,” in *2015 IEEE International Electron Devices Meeting (IEDM)*, pp. 15–4, IEEE, 2015.
- [20] H. Zhao, Y. Chen, Y. Wang, F. Zhou, F. Xue, and J. Lee, “In_{0.7}Ga_{0.3}As tunneling field-effect transistors with an I_{on} of 50 $\mu\text{A}/\mu\text{m}$ and a sub-threshold swing of 86 mV/dec using HfO₂ gate oxide,” *IEEE Electron Device Letters*, vol. 31, no. 12, pp. 1392–1394, 2010.
- [21] D.-H. Ahn, S.-H. Yoon, M. Takenaka, and S. Takagi, “Effects of HfO₂/Al₂O₃ gate stacks on electrical performance of planar In_xGa_{1-x}As tunneling field-effect transistors,” *Applied Physics Express*, vol. 10, no. 8, p. 084201, 2017.
- [22] T. Gotow, M. Mitsuhashi, T. Hoshi, H. Sugiyama, M. Takenaka, and S. Takagi, “Performance enhancement of p -GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As hetero-junction vertical tunneling field-effect transistors with abrupt source impurity profile,” *Journal of Applied Physics*, vol. 126, no. 21, p. 214502, 2019.
- [23] F. Xue, H. Zhao, Y.-T. Chen, Y. Wang, F. Zhou, and J. C. Lee, “InAs inserted InGaAs buried channel metal-oxide-semiconductor field-effect-transistors with atomic-layer-deposited gate dielectric,” *Applied Physics Letters*, vol. 98, no. 8, p. 082106, 2011.

- [24] H.-Y. Tseng, Y. Fang, S. Zhong, and M. J. Rodwell, “InP MOSFETs exhibiting record 70 mV/dec subthreshold swing,” in *2019 Device Research Conference (DRC)*, pp. 183–184, IEEE, 2019.
- [25] J. Wu, Y. Fang, B. Markman, H.-Y. Tseng, and M. J. Rodwell, “ $L_g=30\text{nm}$ InAs channel MOSFETs exhibiting $f_{\text{max}}=410$ GHz and $f_t=357$ GHz,” *IEEE Electron Device Letters*, vol. 39, no. 4, pp. 472–475, 2018.
- [26] A. V. Thathachary, N. Agrawal, K. Bhuvalka, M. Cantoro, Y. Heo, G. Lavallee, S. Maeda, and S. Datta, “Indium arsenide (InAs) single and dual quantum-well heterostructure FinFETs,” in *2015 Symposium on VLSI Technology (VLSI Technology)*, pp. T208–T209, IEEE, 2015.
- [27] R. Oxland, X. Li, S. Chang, S. Wang, T. Vasen, P. Ramvall, R. Contreras-Guerrero, J. Rojas-Ramirez, M. Holland, G. Doornbos, *et al.*, “InAs FinFETs with $H_{\text{fin}}=20$ nm fabricated using a top-down etch process,” *IEEE Electron Device Letters*, vol. 37, no. 3, pp. 261–264, 2016.
- [28] J. Nah, H. Fang, C. Wang, K. Takei, M. H. Lee, E. Plis, S. Krishna, and A. Javey, “III–V complementary metal–oxide–semiconductor electronics on silicon substrates,” *Nano letters*, vol. 12, no. 7, pp. 3592–3595, 2012.
- [29] M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, “III–V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on

Si,” in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*, pp. 1–2, IEEE, 2014.

Chapter 4

Low-Temperature Grown Polycrystalline Gallium Antimonide

This chapter is adapted from the following conference presentation and journal publications:

1. **A. Curran**, F. Gity, A. Gocalinska, E. Mura, R. E. Nagle, M. Schmidt, B. Sheehan, E. Pelucchi, C. O'Dwyer, P. K. Hurley, Investigating the Structural and Electronic Properties of Polycrystalline GaSb Thin Films Grown on SiO₂, poster presented at 50th IEEE Semiconductor Interface Specialists Conference, December 2019, San Diego, USA.
2. **A. Curran**, F. Gity, A. Gocalinska, E. Mura, R. E. Nagle, M. Schmidt,

B. Sheehan, E. Pelucchi, C. O'Dwyer, P. K. Hurley, High Hole Mobility Polycrystalline GaSb Thin Films, *Cyrstals* 11(11), 2021.

3. A. Gocalinska, A. Pescaglini, E. Secco, E. Mura, K. Thomas, **A. Curran**, F. Gity, R. Nagle, M. Schmidt, P. P. Michałowski, P. K. Hurley, I. Povey, E. Pelucchi, Next generation low temperature polycrystalline materials for above IC electronics. High mobility n- and p-type III-V metalorganic vapour phase epitaxy thin films on amorphous substrates, *Journal of Physics: Photonics* 2(2), 2020.

Author contributions:

A. Curran - experimental planning, Hall analysis, Transmission Electron Microscopy (TEM) analysis, device fabrication, electrical characterisation

A. Gocalinska - III-V film growth

M. Schmidt - TEM imaging

R. E. Nagle - Scanning Electron Microscopy (SEM) imaging

B. Sheehan - TEM analysis

I. M. Povey - Atomic Layer Deposition (ALD) oxide growth

E. Pelucchi - concept, design of experiment

C. O'Dwyer - analysis, supervision

P. K. Hurley - analysis, design of experiment, concept, supervision

F. Gity - concept, design of experiment, device processing, supervision

4.1 Abstract

In this chapter, we report on structural and electronic properties of polycrystalline GaSb films (50-250 nm) deposited on p^+ Si/SiO₂ by Metalorganic Vapour Phase Epitaxy (MOVPE) at 475°C. GaSb films grown on Semi-Insulating (SI) GaAs substrates are included as comparative samples. In all cases, the unintentionally doped GaSb is p -type, with hole concentrations in the range of 2×10^{16} - 2×10^{17} cm⁻³. Exceptional hole mobilities are measured for poly GaSb on SiO₂ in the range of 9-66 cm²/Vs, exceeding reported values of many other low temperature grown semiconductors. Mobility of 9.1 cm²/Vs is achieved for an amorphous GaSb layer in a poly GaAs/amorphous GaSb heterostructure. Mechanisms limiting the mobility in the GaSb thin films are investigated. Low temperature grown GaSb films demonstrate potential for implementation in p -channel devices for above IC implementation.

4.2 Introduction

Since the invention of the transistor, advancements in the technology have almost exclusively been achieved through dimensional scaling of components. As described in Section 1.1, 3D integration has emerged as a path towards increasing transistor density and decreasing power consumption and latency without being solely dependent on dimensional scaling [1, 2]. In this thesis we explore materials designed for heterogeneous integration architectures,

which must conform to certain standards, including a low thermal budget.

There has been success reported in the literature in achieving low temperature grown materials with high electron mobilities, including metal oxides [3, 4], metal oxide heterojunctions [5], and 2D materials [6, 7]. However, if these materials are to be implemented in Complementary Metal Oxide Semiconductor (CMOS) architectures, *p*-type counterparts must be developed. While metal oxides have many options for *n*- and *p*-type semiconductors, low temperature grown *p*-type options do not exhibit impressive hole mobilities [8]. Organic semiconductors also provide some *p*-type options, however, for a number of reasons, they also do not possess high mobilities [9].

In this chapter, we investigate low temperature ($<500^{\circ}\text{C}$) grown poly and amorphous GaSb thin films. All the films are found to be *p*-type, and no intentional doping or dopant activation is required, thereby allowing us to circumvent this traditionally high-temperature step. The native hole concentration in GaSb is found to originate from Ga vacancies and anti-site defects [10]. Antimony-containing compounds possess the highest bulk mobilities of all III-Vs, and a bulk hole mobility which is double that of silicon (Table 1.1). For CMOS configurations, dimensions of the *n*-type and *p*-type components are proportional to the *n*- and *p*-type mobilities. GaSb has a relatively low *n*- to *p*-type ratio compared to other materials (Table 1.1), making it an attractive candidate for these types of applications [11]. Growing polar

GaSb on non-polar SiO₂ has traditionally proven difficult [12], but a MOVPE “droplet epitaxy” method has been shown to work [13].

4.3 Experimental

Growth of III-V films described in this section was carried out by members of the Epitaxy and Physics of Nanostructures group in Tyndall. Poly GaSb thin films were grown by MOVPE at 475°C using droplets of either GaAs or GaSb as nucleation sites. The precursors used were Ga(C₂H₅)₃, Sb(CH₃)₃ and AsH₃. In samples where a GaAs buffer layer was added to the structure, AsH₃ was also used as the arsenic source. Doping with Zn was achieved using a Diethyl Zinc (DEZn) precursor with varying fluxes (mol min⁻¹). Corresponding Zn/III growth ratios are given for any samples in the text for which Zn doping was implemented. For each deposition, an Si/SiO₂ substrate was loaded, along with a SI GaAs reference substrate.

SEM images were taken using an FEI Quanta 650 FEG SEM. Samples were prepared for Cross-sectional Transmission Electron Microscopy (XTEM) using a Dual Beam Focussed Ion Beam (FIB) FEI Helios NanoLab 600i. Platinum protective layers were deposited, with or without a prior carbon layer, before the lamella was removed and thinned to <200 nm thickness. TEM analysis was performed using a JEOL JEM-2100.

Hall effect measurements presented in this chapter were performed at room temperature unless otherwise stated, and were measured on a LakeShore Model 8404 AC/DC Hall effect measurement system. Samples for Hall effect measurements were 1 cm x 1 cm and a van der Pauw configuration was used. A detailed description of the Hall Effect measurement system and method can be found in Appendix A. Hall effect measurement results were obtained for one piece of each sample and so no statistical data can be presented for measured mobilities and carrier concentrations.

4.4 Results and Discussion

4.4.1 Structural and Electronic Properties at Room Temperature

First, different nominal thicknesses of poly GaSb films were investigated for morphology, actual thickness, and continuity. The growth process was carried out in the same manner as the schematic representation shown in Figure 2.1, except using the precursors described in Section 4.3. Figures 4.1a-c show SEM images of poly GaSb films of 50, 150 and 250 nm nominal thickness, grown on SiO₂. It is clear from Figure 4.1a that the nominally 50 nm film on SiO₂ is not uniform across the area shown in the image, with some areas which appear to be gaps to oxide. The prevalence of gaps to oxide is visible in the wider view XTEM image in Figure 4.2. Both the nominally

150 nm (Figure 4.1b), and 250 nm (Figure 4.1c) poly GaSb films on SiO₂ show a similar morphology, consisting of a relatively even layer, followed by nanowire-like growth. For the 150 nm sample, the “continuous” layer is thinner, and appears less uniform than that of the 250 nm sample. The green text in both Figure 4.1b and c show measurements taken during SEM imaging, which can be used to estimate the difference in dimensions between the films. One of the measurements allow the estimation of the oxide thickness which is found to be approximately 110 nm. A measurement of the “continuous” layer for both films shows 154 nm for the 250 nm film and 114 nm for the 150 nm film, however, this is only one measurement per film so should be taken as representative only. The measurement of the nanowire-like growths shows similar dimensions in both films at around 600-700 nm. The formations present on the surface of the 50 nm sample in Figure 4.1a appear to be individual, elongated crystallites. These are also present on the surface of the more continuous 150 and 250 nm samples in Figures 4.1a and b, where the domed tops indicate a “pulled up” growth method [13].

Figure 4.1d shows a reference sample of 50 nm GaSb on a SI GaAs substrate. For device applications, thinner and smoother films are preferable. Using SEM images, there is a visual reduction in roughness observable between the 50 nm sample on SiO₂ and 50 nm GaSb on the SI GaAs substrate. An attempt to emulate this effect on the SiO₂ substrate was made by depositing a poly GaAs buffer layer prior to GaSb growth. Figures 4.1e-f show

samples where this method was used on an SiO_2 and SI GaAs substrate respectively. Implementation of the poly GaAs buffer layer shows a clear improvement in uniformity and continuity for the poly GaSb layer on both substrates.

The elemental makeup of the nominally 50 nm film on SiO_2 was investigated using Scanning Transmission Electron Microscopy (STEM) and Energy-Dispersive X-Ray (EDX), shown in Figure 4.3. The area where EDX analysis was performed is indicated by an orange box in Figure 4.3a. It is evident that Ga and Sb are distributed throughout the film as would be expected (see Figure 4.3b-c), however there is also clearly As present at the substrate surface, and some distance into the film (approx. 30 nm), (see Figure 4.3d). This likely originated from GaAs droplets used during the nucleation step of the growth procedure.

Room temperature Hall effect measurement results for samples on the silicon substrate are shown in Table 4.1. The nominally 250 nm GaSb film on SiO_2 returns an impressive hole mobility of $66.5 \text{ cm}^2/\text{Vs}$ which far exceeds reported values for oxide semiconductors [8, 14], and 2D materials [15, 16] grown at $<500^\circ\text{C}$ on amorphous substrates. There is not a significant difference between hole mobility results for 50 nm and 150 nm films (24.2 and $22.9 \text{ cm}^2/\text{Vs}$ respectively), suggesting that complete film continuity is achieved somewhere between the nominally 150 and 250 nm thicknesses. Table 4.2

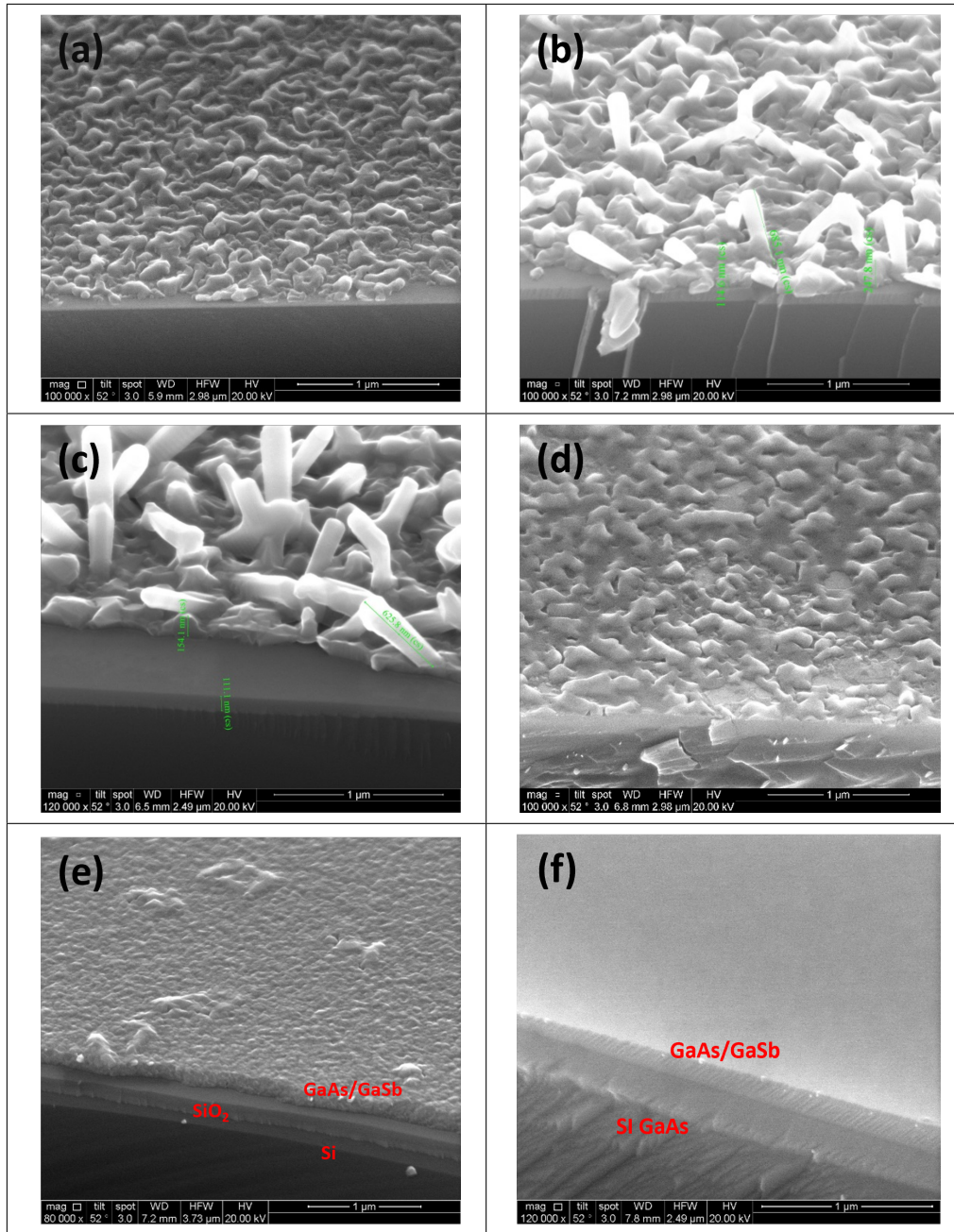


Figure 4.1: SEM images of (a) 50 nm GaSb on SiO₂, (b) 150 nm GaSb on SiO₂, (c) 250 nm GaSb on SiO₂, (d) 50 nm GaSb on SI GaAs, (e) 50 nm GaAs + 50 nm GaSb on SiO₂, and (f) 50 nm GaAs + 50 nm GaSb on SI GaAs. All scale bars are 1 μm.

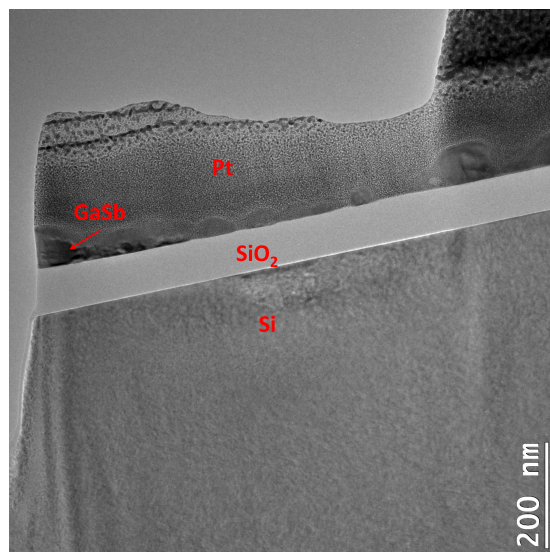


Figure 4.2: XTEM image of a larger area of the 50 nm GaSb on Si/SiO₂ lamella.

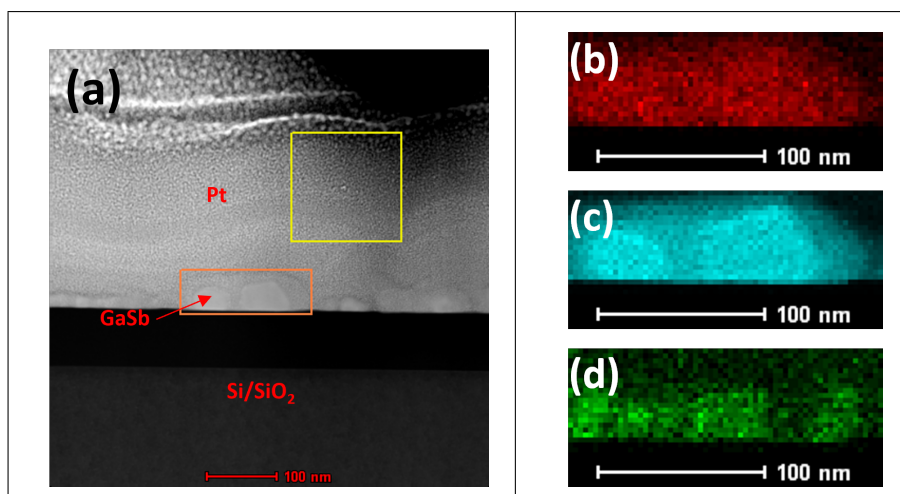


Figure 4.3: (a) STEM image of nominally 50 nm poly GaSb on SiO₂. EDX analysis showing presence of (b) Ga-L, (c) Sb-L, and (d) As-K.

shows the room temperature Hall effect results for the corresponding samples in Table 4.1, but on a SI GaAs substrate. The samples grown on the SI GaAs substrates display higher mobilities than any of the samples grown on Si/SiO₂. This is expected, as on the crystalline GaAs substrate traditional epitaxy can occur during film growth, resulting in a higher quality film. For the films on GaAs, the mobility increases with thickness, without the large jump in mobility seen between the 150 and 250 nm films on SiO₂, which was also seen as an indication of the onset of continuity.

Interestingly, despite the visual improvement in uniformity and continuity for the film on SiO₂ with a GaAs buffer layer, Figure 4.1e, compared to the sample without, Figure 4.1a, the carrier mobility is reduced from 24.2 cm²/Vs for the sample without the poly GaAs buffer layer to 9.1 cm²/Vs for the same film with a 50 nm GaAs buffer layer (Table 4.1).

GaSb Thickness (nm)	Mobility (cm²/Vs)	Carrier Conc (cm⁻³)	Sheet Carrier Conc (cm⁻²)
50	24.2	1.98x10 ¹⁶	9.92x10 ¹⁰
150	22.9	2.17x10 ¹⁷	3.26x10 ¹²
250	66.5	1.84x10 ¹⁷	4.6x10 ¹²
50 (+50nm GaAs)	9.1	1.37x10 ¹⁷	1.65x10 ¹²

Table 4.1: Room-temperature Hall effect measurement results of GaSb on SiO₂.

To investigate this surprising result, and to gain further knowledge of the actual thickness and structure of other films, XTEM was performed. Figure

GaSb Thickness (nm)	Mobility (cm²/Vs)	Carrier Conc (cm⁻³)	Sheet Carrier Conc (cm⁻²)
50	76.8	8.54x10 ¹⁷	4.27x10 ¹²
150	172	3.9x10 ¹⁷	5.92x10 ¹²
250	293.2	1.17x10 ¹⁷	2.92x10 ¹²
50 (+50nm GaAs)	218.57	3.3x10 ¹⁷	1.65x10 ¹²

Table 4.2: Room-temperature Hall effect measurement results of GaSb on GaAs.

4.4a shows a representative area of the nominally 50 nm film on SiO₂. The XTEM images confirmed the polycrystalline nature of the GaSb film on the substrate; however, it is evident that there is a lack of continuity in the area of the lamella shown in the image. Taking Hall mobility results from this film into account (Table 4.1) it is reasonable to assume that there are 3D percolation paths present in this film, allowing for carrier transport. 250 nm GaSb on SiO₂, Figure 4.4b, is also confirmed to be polycrystalline. From the cross section, the continuous layer seen in the SEM images is also evident, along with the subsequent nanowire-like growth. For the 250 nm GaSb film, the average thickness of the continuous portion of the film was calculated using the area shown in Figure 4.4 and found to be 124 nm, with a standard deviation of 56.6 nm.

Figure 4.4c shows the 50 nm GaAs + 50 nm GaSb on SiO₂ which exhibited reduced mobility (Table 4.1). The XTEM image shows that while the initial nominally 50 nm GaAs layer is polycrystalline, the subsequent nominally 50 nm GaSb does not display a polycrystalline nature, and in fact

appears to be amorphous. This would explain the drop in mobility between the film without the GaAs layer which is polycrystalline, and the film with the GaAs layer which is amorphous. The STEM image, Figure 4.4d, gives a wider view of the overall topography of the two layers. The GaAs layer has a saw-tooth shape consistent with $\{111\}$ facets [17], while the amorphous GaSb layer fills in the facets, and has an overall smoothing effect. This amorphization which occurs only when the GaSb is grown on a poly GaAs layer could be due to the lattice mismatch between the two crystal structures, which is 7.8% [18]. EDX analysis was used while in STEM mode to confirm that the elemental make-up of the two layers in the heterostructure was as expected. The sampled areas and their respective spectrums are shown in Figure 4.5. The copper peaks evident in both spectra result from the TEM grid which holds the lamella in the chamber.

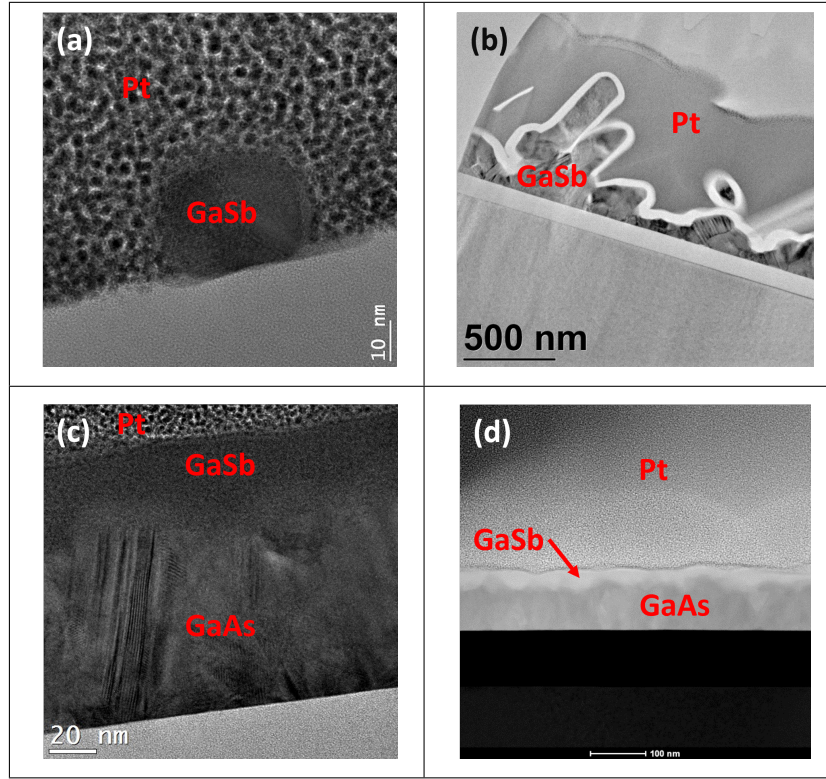


Figure 4.4: XTEM images of (a) 50 nm GaSb on SiO₂, (b) 250 nm GaSb on SiO₂, and (c) 50 nm GaAs + 50 nm GaSb on SiO₂. (d) STEM image of 50 nm GaAs + 50 nm GaSb on SiO₂.

To determine if the amorphous GaSb observed was a true result, or if the layer had been amorphized during preparation for TEM with a FIB (which uses a gallium beam), X-Ray Diffraction (XRD) analysis was performed on part of the sample which had not gone through preparation on the FIB. Figure 4.6 shows the resulting spectrum compared against two other samples. GaAs peaks from the buffer layer are intense and indicate a film which is polycrystalline in nature with regions of good quality crystalline GaAs. Some weak peaks could be associated with GaSb, suggesting there may be

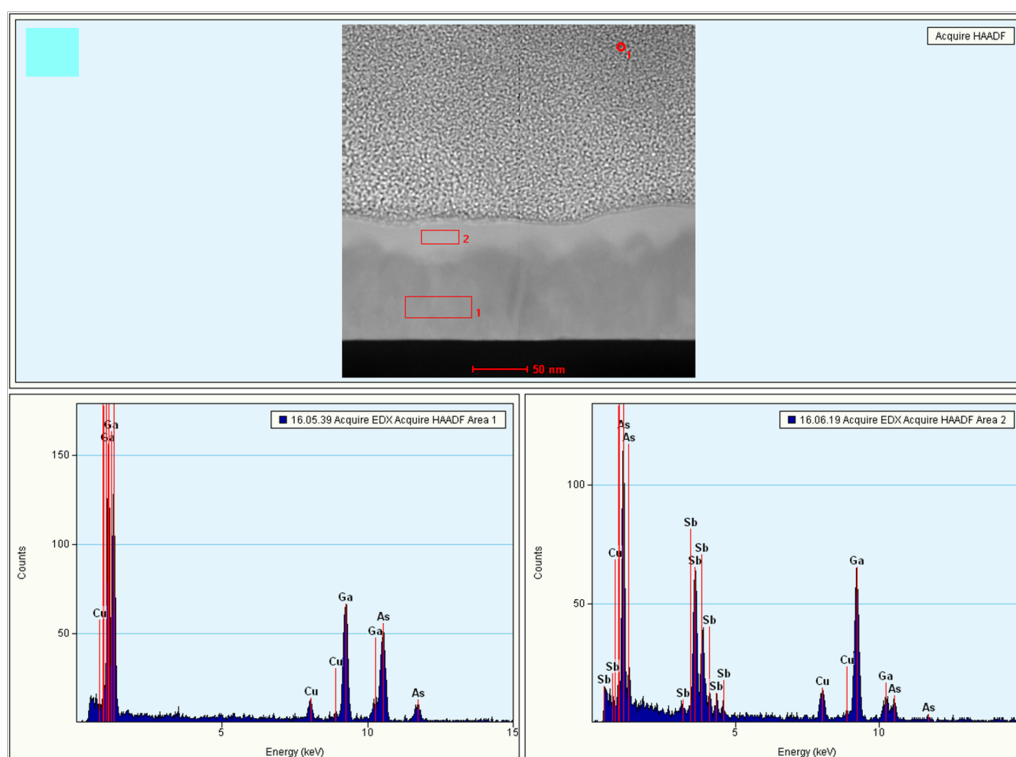


Figure 4.5: EDX analysis on layers of heterostructure on SiO₂

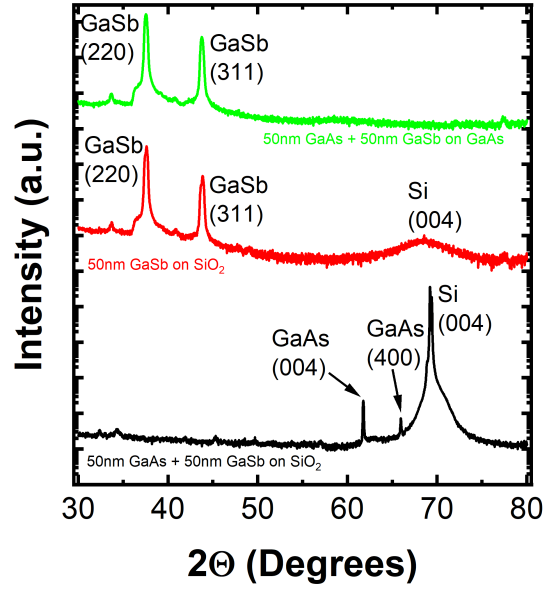


Figure 4.6: XRD of 50 nm GaAs + 50 nm GaSb on SiO₂, 50 nm GaSb on SiO₂, and 50 nm GaAs + 50 nm GaSb on GaAs.

very small regions with some amount of crystallinity. However, the dominant phase of the GaSb layer is amorphous, confirming the results from XTEM. XRD was also carried out on samples consisting of 50 nm GaSb on SiO₂ and 50 nm GaAs + 50 nm GaSb on SI GaAs. Both samples show strong peaks for crystalline GaSb phases. This showed that it was not the thickness of the amorphous layer causing an inability to detect GaSb, as the 50 nm GaSb directly on SiO₂ is a similar thickness and less uniform. It also demonstrated that the substrate was important, as the same heterostructure on SI GaAs did not produce an amorphous layer of GaSb.

Another attempt to improve surface roughness and increase the film unifor-

mity, especially at lower thicknesses, was made by using a surfactant during the film growth. Zn is a *p*-type dopant in GaSb and has been shown to affect the surface morphology of films when it is implemented in the growth process [19]. This method was used in conjunction with a poly GaAs buffer layer, which had already been shown to have a smoothing effect on the grown films. All films consist of a 50 nm GaAs + 50 nm GaSb heterostructure, where the Zn incorporation in the GaSb layer varies. A range of Zn fluxes were studied, with SEM images of the resulting films with their respective Zn/Ga growth ratios shown in Figure 4.7. While the film with the lowest Zn/Ga ratio of 0.025, Figure 4.7b, shows a reduction in surface roughness compared to the film with no Zn incorporation, Figure 4.7a, as the Zn/Ga ratio increases, Figures 4.7c-d, the surface begins to become roughened. This was thought to be because of the competing effects of the DEZn and Trimethyl Antimonide (TMSb) [13] (which has a similar effect in arsenides [20]) inhibiting the deposition of the film.

Room temperature Hall effect measurements were performed on the films containing Zn. Results of these measurements are shown in Table 4.3. When Zn was introduced, the carrier concentration increased by around 2 orders of magnitude, as was expected due to its *p*-type dopant nature. As the carrier concentration of the films increased, the carrier mobility decreased. In bulk GaSb, the hole mobility is shown to drop by 3x when the hole concentration increases by two orders of magnitude, as seen in these films [21]. The sample

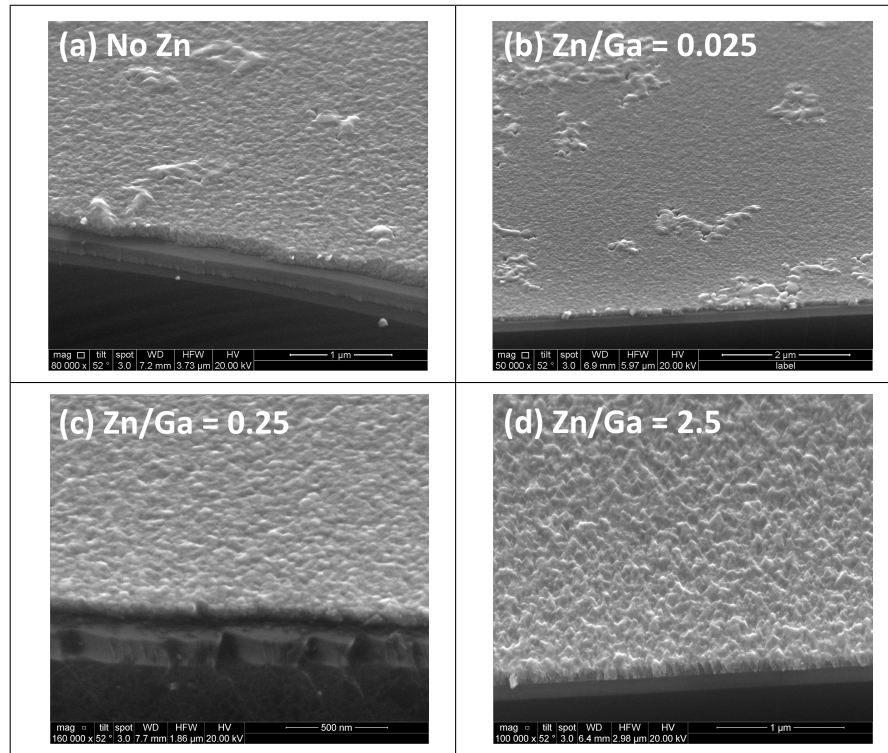


Figure 4.7: SEM images of 50 nm GaAs + 50 nm GaSb heterostructures on SiO₂ with (a) no Zn, and Zn/Ga ratios of (b) 0.025, (c) 0.25, and (d) 2.5.

which had a Zn/Ga ratio of 2.5 was extremely difficult to measure using the Hall effect apparatus as a satisfactory Hall voltage could not be achieved (see A for detailed description). The related Hall mobility and other results shown for this particular sample in Table 4.3 should be taken as indicative only, and are included only to show the observed trend.

Zn/Ga Ratio	Mobility (cm²/Vs)	Carrier Conc (cm⁻³)	Sheet Carrier Conc (cm⁻²)	Hall Voltage (V)
0	9.1	1.37x10 ¹⁷	1.65x10 ¹²	6.45x10 ⁻⁴
0.025	3.88	4.19x10 ¹⁷	2.09x10 ¹²	2.54x10 ⁻⁴
0.25	4.04	1.89x10 ¹⁸	9.46x10 ¹²	8.98x10 ⁻⁵
2.5	0.7	1.77x10 ¹⁹	8.87x10 ¹³	7.78x10 ⁻⁶

Table 4.3: Room temperature Hall effect measurement results for 50 nm GaAs + 50 nm GaSb films with varying Zn incorporation.

4.4.2 Temperature Dependent Properties

Temperature dependent Hall effect results require repeated measurements at a variety of temperatures. From room temperature measurements, it had been observed that repeated electrical measurement induced an increase in the resistivity of the GaSb films. Figure 4.8 illustrates this effect for a 50 nm film directly on SiO₂ (Figure 4.8a) and a 250 nm film (Figure 4.8b) directly on SiO₂. The fact that the effect is much more pronounced for the 50 nm film is consistent with the effect occurring due to changes in the density of fixed charge and/or interface states in the native oxide on the GaSb surface and at the GaSb/native oxide interface. The 50 nm film has a greater proportion

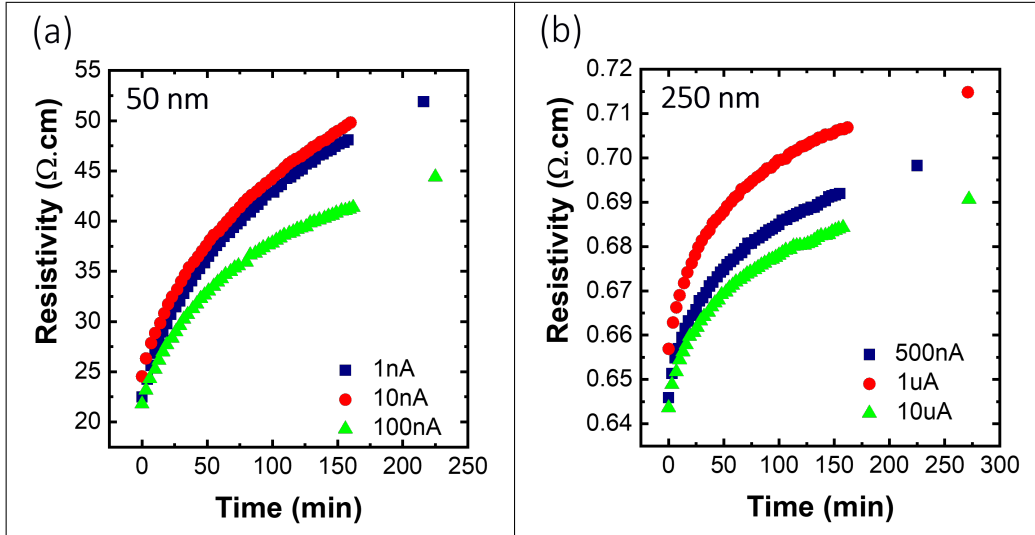


Figure 4.8: Repeated resistivity measurements of (a) 50 nm GaSb and (b) 250 nm GaSb on a Si/SiO₂ substrate. Excitation current is shown in inset.

of surface to bulk compared to the 250 nm film. Different excitation currents were used for the resistivity measurements, with their values being shown in the inset of Figure 4.8.

It was thought that this effect could mask the temperature dependent results, as the resistance measurement is used for the mobility calculation. For this reason, the temperature dependent measurements were done in a loop, so that the decreasing and increasing direction can be compared. Figure 4.9 shows this measurement for the 250 nm film. It is clear that the measurements on the decreasing and increasing direction are very similar. It is reasonable to assume from this measurement that the effect of temperature masks the effect of repeated measurements for this film.

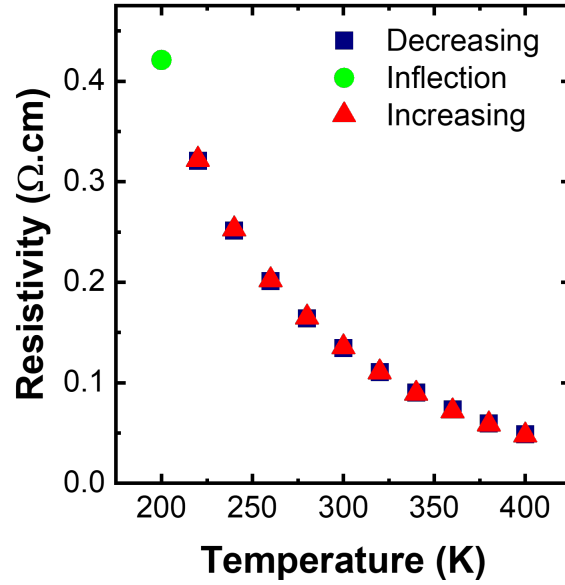


Figure 4.9: Resistivity vs Temperature for 250 nm GaSb on Si/SiO₂. Inset lists stage of measurement in order they were performed.

To understand the mechanisms and limitations of the hole mobility in the poly GaSb films, temperature dependent Hall effect measurements were performed on nominally 250 nm GaSb films on SiO₂ and SI GaAs, along with the 50 nm GaAs + 50 nm GaSb on SiO₂ sample. The resultant plots are shown in Figure 4.10. It is evident from the data that the dominant scattering mechanism limiting the mobility is different for GaSb grown directly on a SI GaAs substrate (Figure 4.10a), than for GaSb grown directly on a SiO₂ substrate (Figure 4.10b). For GaSb on a SI GaAs substrate (Figure 4.10a), mobility decreases and carrier concentration increases as temperature increases. This observation is consistent with phonon scattering [22].

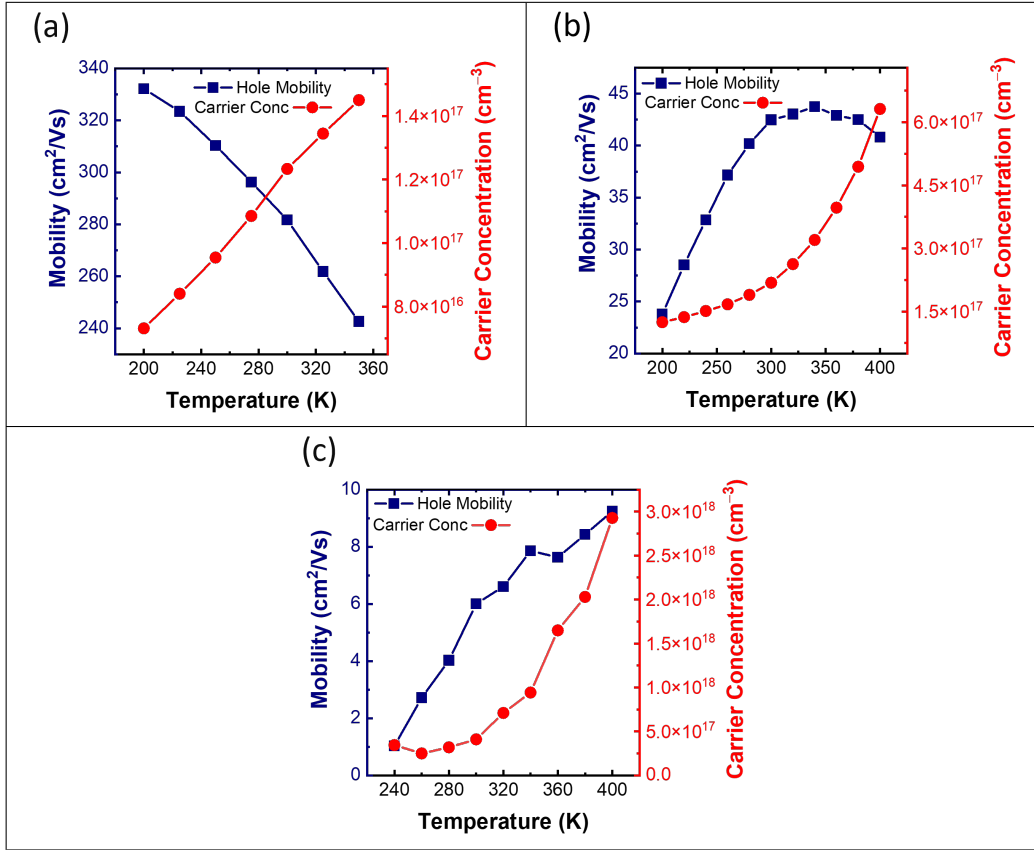


Figure 4.10: Carrier mobility and concentration of (a) 250 nm GaSb on a SI GaAs substrate, (b) 250 nm GaSb on a Si/SiO₂ substrate, and (c) 50 nm GaAs + 50 nm GaSb on a Si/SiO₂ substrate.

For GaSb grown directly on SiO₂ (Figure 4.10b), and for the 50 nm GaAs + 50 nm GaSb heterostructure (Figure 4.10c), both carrier mobility and concentration increase with increasing temperature. This could be related to thermionic emission over grain boundary potential barriers [23], or Coulombic scattering [24].

Further analysis was performed on the temperature dependent results of the 250 nm GaSb on SiO₂ and 50 nm GaAs + 50 nm GaSb on SiO₂, where the exact mechanism limiting the mobility was not as clearly obvious as the 250 nm GaSb film on SI GaAs. The 250 nm GaSb film on SiO₂ shows an initially linear region and then begins to turn over at higher temperatures, transitioning into another region with a different limiting mechanism. The following equation shows the temperature dependence of Coulombic scattering limited mobility:

$$\mu_{disl} = \frac{30 \cdot \sqrt{2\pi} \cdot \epsilon^2 \cdot a^2 \cdot (kT)^{3/2}}{N_{disl} \cdot e^3 \cdot f^2 \cdot \lambda_D \cdot \sqrt{m}} \quad (4.4.1)$$

where ϵ is the dielectric constant, a is the distance between centres, k is the Boltzmann constant, N_{disl} is the concentration of dislocations, f is the occupation rate of the centres, λ_D is the Debye screening length, e is the electronic charge, and m is the effective mass [25]. From this equation, we can see that Coulombic scattering limited mobility should increase with a slope of 3/2 as temperature increases on a log, log scale. This is close to the experimental value of 1.57 which is observed for 250 nm GaSb on SiO₂ between 200 and 280 K, Figure 4.11a. The observation that the mobility begins to turn over in Figure 4.10b and tends towards a negative slope as temperature continues to increase is consistent with previous observation in the literature [24]. This transition is due to the mobility becoming phonon scattering limited at

higher temperatures.

Figure 4.11b shows the natural log of the conductivity obtained from the Hall effect measurement plotted against $T^{-1/4}$ for the sample comprised of 50 nm GaAs + 50 nm GaSb on a Si/SiO₂ substrate. This results in a linear plot, which is consistent with 3D variable range hopping limited mobility. Mott's Law [26] shows the following relationship:

$$\ln \sigma = A - \left(\frac{T_0}{T} \right)^{1/4} \quad (4.4.2)$$

From this equation, we can see that the slope of the $\ln$ conductivity vs $T^{-1/4}$ graph should be equal to $T_0^{1/4}$. This yields a value for T_0 of 4.3×10^8 K, which is similar to previously reported values for amorphous Germanium [27] and poly-Si [28]. T_0 is defined as:

$$T_0 = \frac{\beta}{k \cdot g(\mu) \cdot a^3} \quad (4.4.3)$$

where $g(\mu)$ is the density of states at the Fermi level, a is the localization of

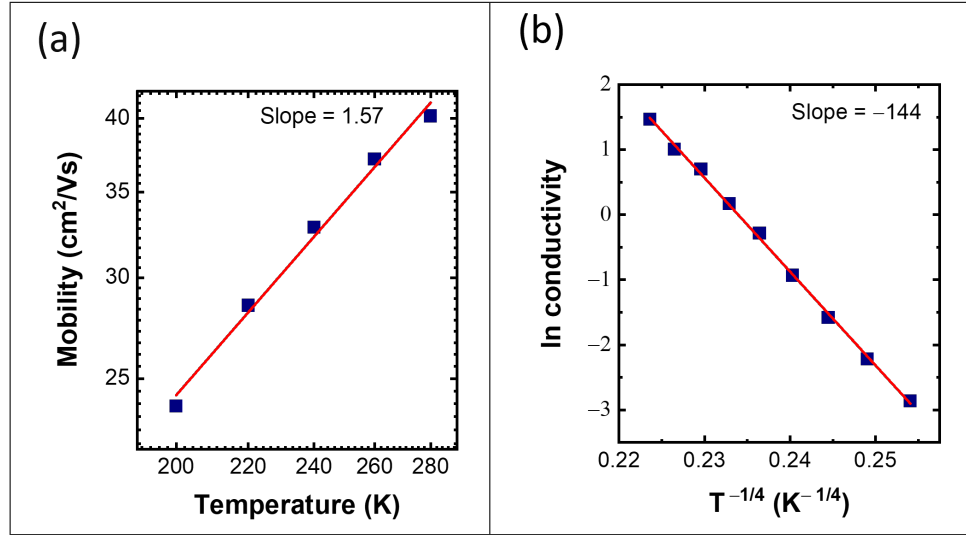


Figure 4.11: (a) log, log plot of mobility vs temperature for 250nm GaSb on Si/SiO₂, and (b) natural log of conductivity vs $T^{-1/4}$ for 50 nm GaAs + 50 nm GaSb on SiO₂.

the states near the Fermi level, and β is a numerical coefficient [29]. Variable range hopping occurs when the temperature is sufficiently low enough that the resistances between neighbouring states become greater than far-away states which exist in a narrow energy band near the Fermi level. As the temperature decreases, the average hopping distance increases with $T^{-1/4}$ [29].

The results presented in this section show that the dominant mechanism limiting the mobility in GaSb films depends on the level of crystallinity present in the film. The crystalline SI GaAs substrate allows for traditional epitaxy to take place to some extent, resulting in a relatively high level of crystallinity

in the film. The films grown directly on SiO_2 are fully polycrystalline, while the film with a GaAs buffer layer on SiO_2 is amorphous. Each of the films described has a different level of crystallinity, and also a different mechanism limiting the mobility.

4.5 Benchmarking

Figure 4.12 shows the graph included in Section 1.3.2, with the films from this chapter included as comparison. The polycrystalline and amorphous GaSb films from this work compare favourably to the films found in the literature, especially taking into account the amorphous substrate half of the samples are grown on. The two amorphous films of CuSnI [30] and CuI [31] have lower mobilities than the amorphous film presented here, though they are also grown at lower temperature. The poly GaSb comparison from literature [32] shows a high mobility on a glass substrate, however involves higher growth temperatures, and the films are thicker, at around 1,000 nm. From our results, we can see that mobility increases substantially with thickness (Tables 4.1 and 4.2).

4.6 Conclusions

We have demonstrated high hole mobility polycrystalline ($66.5 \text{ cm}^2/\text{Vs}$) and amorphous ($9.1 \text{ cm}^2/\text{Vs}$) GaSb grown on amorphous substrates. The hole

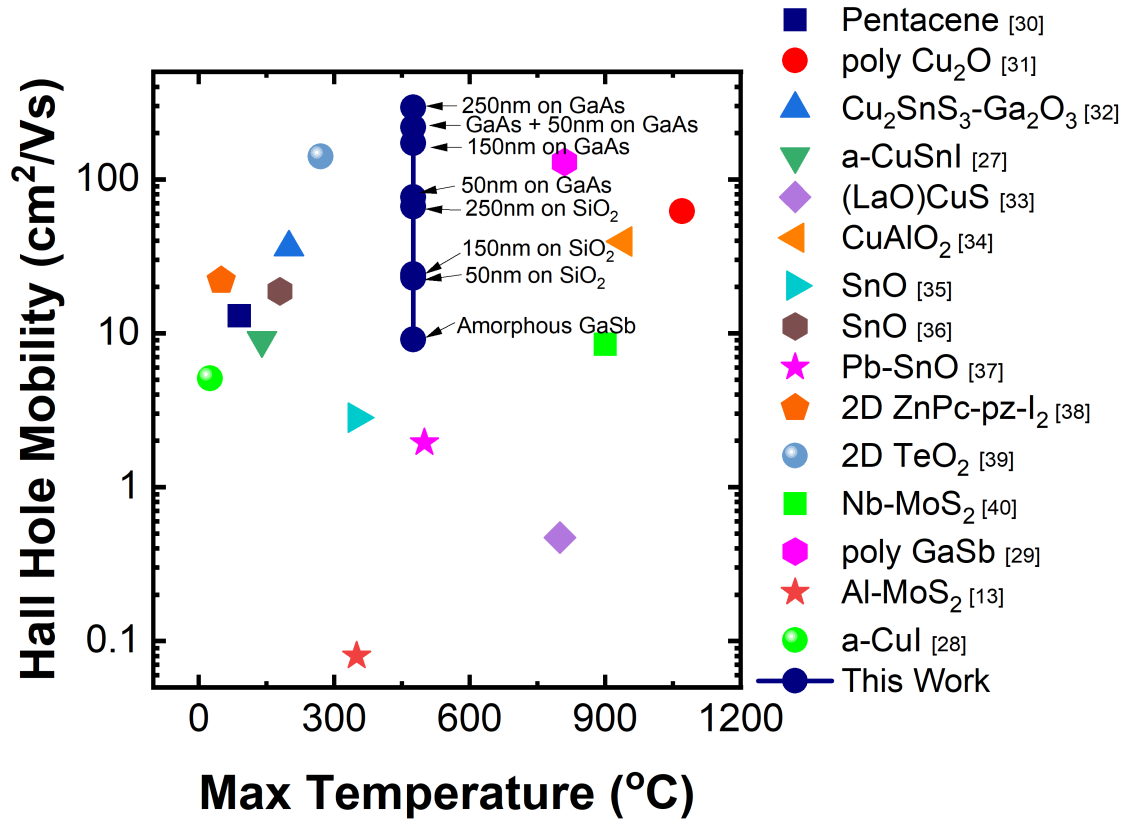


Figure 4.12: Results from polycrystalline and amorphous GaSb films in this work compared to results from the literature [16, 30–43].

mobility of $9.1 \text{ cm}^2/\text{Vs}$ obtained for the amorphous GaSb as part of a GaAs/GaSb heterostructure exceeds previously reported hole mobilities for amorphous semiconductors on amorphous substrates [30, 31, 44]. Factors limiting the hole mobility in the GaSb films were investigated through temperature dependent Hall effect measurements. The dominant limiting factor was found to vary depending on the substrate and presence/absence of a GaAs buffer layer. For GaSb directly on GaAs, the mobility was phonon limited, GaSb directly on SiO_2 had a Coulomb scattering limited mobility, and the amorphous GaSb film with a GaAs buffer layer on SiO_2 displayed a mobility which was variable range hopping limited. Both the polycrystalline and the amorphous GaSb films studied in this chapter show promising potential as high hole mobility semiconductor materials grown below 500°C , compatible with back-end-of-line (BEOL) integration.

Bibliography

- [1] S. Datta, S. Dutta, B. Grisafe, J. Smith, S. Srinivasa, and H. Ye, “Back-end-of-line compatible transistors for monolithic 3-D integration,” *IEEE Micro*, vol. 39, no. 6, pp. 8–15, 2019.
- [2] H.-S. P. Wong and S. Salahuddin, “Memory leads the way to better computing,” *Nature nanotechnology*, vol. 10, no. 3, pp. 191–194, 2015.
- [3] M. Esro, G. Vourlias, C. Somerton, W. I. Milne, and G. Adamopoulos, “High-mobility ZnO thin film transistors based on solution-processed hafnium oxide gate dielectrics,” *Advanced Functional Materials*, vol. 25, no. 1, pp. 134–141, 2015.
- [4] C. W. Shih, A. Chin, C. F. Lu, and W. F. Su, “Remarkably high mobility ultra-thin-film metal-oxide transistor with strongly overlapped orbitals,” *Scientific reports*, vol. 6, no. 1, pp. 1–6, 2016.
- [5] H. Faber, S. Das, Y.-H. Lin, N. Pliatsikas, K. Zhao, T. Kehagias, G. Dimitrakopoulos, A. Amassian, P. A. Patsalas, and T. D. Anthopoulos, “Heterojunction oxide thin-film transistors with unprecedented elec-

- tron mobility grown from solution,” *Science advances*, vol. 3, no. 3, p. e1602640, 2017.
- [6] J. Zheng, X. Yan, Z. Lu, H. Qiu, G. Xu, X. Zhou, P. Wang, X. Pan, K. Liu, and L. Jiao, “High-mobility multilayered MoS₂ flakes with low contact resistance grown by chemical vapor deposition,” *Advanced Materials*, vol. 29, no. 13, p. 1604540, 2017.
- [7] R. Yang, H. Li, K. K. Smithe, T. R. Kim, K. Okabe, E. Pop, J. A. Fan, and H.-S. P. Wong, “2D molybdenum disulfide (MoS₂) transistors driving RRAMs with 1T1R configuration,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, pp. 19–5, IEEE, 2017.
- [8] Z. Wang, P. K. Nayak, J. A. Caraveo-Frescas, and H. N. Alshareef, “Recent developments in *p*-type oxide semiconductor materials and devices,” *Advanced Materials*, vol. 28, no. 20, pp. 3831–3892, 2016.
- [9] Ş. Atahan-Evrenk and A. Aspuru-Guzik, “Prediction and theoretical characterization of *p*-type organic semiconductor crystals for field-effect transistor applications,” *Prediction and Calculation of Crystal Structures*, pp. 95–138, 2014.
- [10] P. Dutta, H. Bhat, and V. Kumar, “The physics and technology of gallium antimonide: An emerging optoelectronic material,” *Journal of applied physics*, vol. 81, no. 9, pp. 5821–5870, 1997.

-
- [11] A. Nainani, T. Irisawa, Z. Yuan, B. R. Bennett, J. B. Boos, Y. Nishi, and K. C. Saraswat, “Optimization of the $\text{Al}_2\text{O}_3/\text{GaSb}$ interface and a high-mobility GaSb p MOSFET,” *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3407–3415, 2011.
- [12] M. T. H. Ha, S. H. Huynh, H. B. Do, T. A. Nguyen, Q. H. Luc, C. T. Lee, and E. Y. Chang, “Entirely relaxed lattice-mismatched GaSb/GaAs/Si (001) heterostructure grown via metalorganic chemical vapor deposition,” *Applied Physics Express*, vol. 11, no. 5, p. 051202, 2018.
- [13] A. Gocalinska, A. Pescaglini, E. Secco, E. E. Mura, K. Thomas, A. Curran, F. Gity, R. Nagle, M. Schmidt, P. P. Michałowski, *et al.*, “Next generation low temperature polycrystalline materials for above IC electronics. high mobility n -and p -type III–V metalorganic vapour phase epitaxy thin films on amorphous substrates,” *Journal of Physics: Photonics*, vol. 2, no. 2, p. 025003, 2020.
- [14] C. W. Shih, A. Chin, C. F. Lu, and W. F. Su, “Remarkably high hole mobility metal-oxide thin-film transistors,” *Scientific reports*, vol. 8, no. 1, pp. 1–6, 2018.
- [15] K. J. Saji, K. Tian, M. Snure, and A. Tiwari, “2D tin monoxide—an unexplored p -type van der waals semiconductor: material characteristics and field effect transistors,” *Advanced Electronic Materials*, vol. 2, no. 4, p. 1500453, 2016.

-
- [16] V. Vandalon, M. A. Verheijen, W. M. Kessels, and A. A. Bol, “Atomic layer deposition of Al-doped MoS₂: Synthesizing a *p*-type 2D semiconductor with tunable carrier density,” *ACS applied nano materials*, vol. 3, no. 10, pp. 10200–10208, 2020.
- [17] F. Minari and B. Billia, “Mixed cells in directional solidification of In-doped GaAs; cellular profile and shape-induced stresses,” *Journal of crystal growth*, vol. 140, no. 3-4, pp. 264–276, 1994.
- [18] S. Huang, G. Balakrishnan, A. Khoshakhlagh, A. Jallipalli, L. Dawson, and D. Huffaker, “Strain relief by periodic misfit arrays for low defect density GaSb on GaAs,” *Applied physics letters*, vol. 88, no. 13, p. 131911, 2006.
- [19] A. Gocalinska, M. Manganaro, E. Pelucchi, and D. Vvedensky, “Surface organization of homoepitaxial InP films grown by metalorganic vapor-phase epitaxy,” *Physical Review B*, vol. 86, no. 16, p. 165307, 2012.
- [20] A. Gocalinska, M. Manganaro, and E. Pelucchi, “Suppression of threading defects formation during Sb-assisted metamorphic buffer growth in InAs/InGaAs/InP structure,” *Applied Physics Letters*, vol. 100, no. 15, p. 152112, 2012.
- [21] J. Wiley, “Mobility of holes in III-V compounds,” in *Semiconductors and semimetals*, vol. 10, pp. 91–174, Elsevier, 1975.

-
- [22] K. Nakashima, “Electrical and optical studies in gallium antimonide,” *Japanese Journal of Applied Physics*, vol. 20, no. 6, p. 1085, 1981.
- [23] J. Y. Seto, “The electrical properties of polycrystalline silicon films,” *Journal of Applied Physics*, vol. 46, no. 12, pp. 5247–5254, 1975.
- [24] H. Ng, D. Doppalapudi, T. Moustakas, N. Weimann, and L. Eastman, “The role of dislocation scattering in *n*-type GaN films,” *Applied physics letters*, vol. 73, no. 6, pp. 821–823, 1998.
- [25] B. Pödör, “Electron mobility in plastically deformed germanium,” *physica status solidi (b)*, vol. 16, no. 2, pp. K167–K170, 1966.
- [26] N. F. Mott, “Conduction in non-crystalline materials: III. localized states in a pseudogap and near extremities of conduction and valence bands,” *Philosophical Magazine*, vol. 19, no. 160, pp. 835–852, 1969.
- [27] A. J. Lewis, “Conductivity and thermoelectric power of amorphous germanium and amorphous silicon,” *Physical Review B*, vol. 13, no. 6, p. 2565, 1976.
- [28] L.-P. Scheller and N. Nickel, “Charge transport in polycrystalline silicon thin-films on glass substrates,” *Journal of Applied Physics*, vol. 112, no. 1, p. 013713, 2012.
- [29] B. I. Shklovskii and A. L. Efros, “Variable-range hopping conduction,” in *Electronic properties of doped semiconductors*, pp. 202–227, Springer, 1984.

-
- [30] T. Jun, J. Kim, M. Sasase, and H. Hosono, "Material design of p -type transparent amorphous semiconductor, Cu-Sn-I," *Advanced Materials*, vol. 30, no. 12, p. 1706573, 2018.
- [31] A. Liu, H. Zhu, W.-T. Park, S.-J. Kang, Y. Xu, M.-G. Kim, and Y.-Y. Noh, "Room-temperature solution-synthesized p -type copper (I) iodide semiconductors for transparent thin-film transistors and complementary electronics," *Advanced Materials*, vol. 30, no. 34, p. 1802379, 2018.
- [32] Q. Zaixiang, S. Yun, H. Weiyu, H. Qing, and L. Changjian, "Polycrystalline GaSb thin films grown by co-evaporation," *Journal of Semiconductors*, vol. 30, no. 3, p. 033004, 2009.
- [33] Y.-J. Lin, H.-Y. Tsao, and D.-S. Liu, "Hall-effect mobility of pentacene films prepared by the thermal evaporating method with different substrate temperature," *Applied Physics Letters*, vol. 101, no. 1, p. 013302, 2012.
- [34] Y. S. Lee, M. T. Winkler, S. C. Siah, R. Brandt, and T. Buonassisi, "Hall mobility of cuprous oxide thin films deposited by reactive direct-current magnetron sputtering," *Applied Physics Letters*, vol. 98, no. 19, p. 192115, 2011.
- [35] J. Kim, H.-M. Kim, S. Cho, C. Avis, and J. Jang, "High hall mobility p -type $\text{Cu}_2\text{SnS}_3\text{-Ga}_2\text{O}_3$ with a high work function," *Advanced Functional Materials*, vol. 28, no. 34, p. 1802941, 2018.

-
- [36] H. Hiramatsu, M. Orita, M. Hirano, K. Ueda, and H. Hosono, “Electrical conductivity control in transparent p -type (LaO) CuS thin films prepared by rf sputtering,” *Journal of applied physics*, vol. 91, no. 11, pp. 9177–9181, 2002.
- [37] Z. Yao, B. He, L. Zhang, C. Zhuang, T. Ng, S. Liu, M. Vogel, A. Kumar, W. Zhang, C. Lee, *et al.*, “Energy band engineering and controlled p -type conductivity of CuAlO₂ thin films by nonisovalent Cu-O alloying,” *Applied Physics Letters*, vol. 100, no. 6, p. 062102, 2012.
- [38] H.-N. Lee, H.-J. Kim, and C.-K. Kim, “ p -channel tin monoxide thin film transistor fabricated by vacuum thermal evaporation,” *Japanese Journal of Applied Physics*, vol. 49, no. 2R, p. 020202, 2010.
- [39] J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato, U. Schwingenschloögl, and H. N. Alshareef, “Record mobility in transparent p -type tin monoxide films and devices by phase engineering,” *ACS nano*, vol. 7, no. 6, pp. 5160–5167, 2013.
- [40] M. Liao, Z. Xiao, F.-Y. Ran, H. Kumomi, T. Kamiya, and H. Hosono, “Effects of Pb doping on hole transport properties and thin-film transistor characteristics of SnO thin films,” *ECS Journal of Solid State Science and Technology*, vol. 4, no. 3, p. Q26, 2015.
- [41] M. Wang, M. Wang, H.-H. Lin, M. Ballabio, H. Zhong, M. Bonn, S. Zhou, T. Heine, E. Cánovas, R. Dong, *et al.*, “High-mobility semicon-

- ducting two-dimensional conjugated covalent organic frameworks with *p*-type doping,” *Journal of the American Chemical Society*, vol. 142, no. 52, pp. 21622–21627, 2020.
- [42] A. Zavabeti, P. Aukarasereenont, H. Tuohey, N. Syed, A. Jannat, A. Elbourne, K. A. Messalea, B. Y. Zhang, B. J. Murdoch, J. G. Partridge, *et al.*, “High-mobility *p*-type semiconducting two-dimensional TeO₂,” *Nature Electronics*, vol. 4, no. 4, pp. 277–283, 2021.
- [43] M. R. Laskar, D. N. Nath, L. Ma, E. W. Lee, C. H. Lee, T. Kent, Z. Yang, R. Mishra, M. A. Roldan, J.-C. Idrobo, *et al.*, “*p*-type doping of MoS₂ thin films using Nb,” *Applied Physics Letters*, vol. 104, no. 9, p. 092104, 2014.
- [44] W. Xu, J. Zhang, Y. Li, L. Zhang, L. Chen, D. Zhu, P. Cao, W. Liu, S. Han, X. Liu, *et al.*, “*p*-type transparent amorphous oxide thin-film transistors using low-temperature solution-processed nickel oxide,” *Journal of Alloys and Compounds*, vol. 806, pp. 40–51, 2019.

Chapter 5

Thin Film Polycrystalline GaSb MOSFETs

Author contributions:

A. Curran - experimental planning, Hall analysis, Transmission Electron Microscopy (TEM) analysis, device fabrication, electrical characterisation

A. Gocalinska - III-V film growth

M. Schmidt - TEM imaging

R. E. Nagle - Scanning Electron Microscopy (SEM) imaging

B. Sheehan - TEM analysis

I. M. Povey - Atomic Layer Deposition (ALD) oxide growth

E. Pelucchi - concept, design of experiment

C. O'Dwyer - analysis, supervision

P. K. Hurley - analysis, design of experiment, concept, supervision

F. Gity - concept, design of experiment, device processing, supervision

5.1 Abstract

Low temperature grown ($<500^{\circ}\text{C}$) polycrystalline (poly) GaSb is implemented as a channel material in transistor test devices. Three samples are studied in detail, with channel materials consisting of poly GaSb with nominal thickness of 50, 150 and 250 nm. Full processing steps are developed and described. The transistor test devices are studied at different stages of the processing to understand the effect on the transistor characteristics. The highest $I_{\text{ON}}/I_{\text{OFF}}$ ratio for any of the devices is achieved for 50 nm GaSb on SiO_2 , reaching a value of 205 at room temperature and 550 at -50°C . Top-gated transistors were formed using a 20nm Al_2O_3 gate dielectric and a Pd gate metal contact.

5.2 Introduction

The need for low temperature grown materials, and particularly *p*-type materials, for monolithic 3D integration has been discussed in detail in Section 1.1 and Section 4.2. In this chapter we attempt to fabricate and characterise devices made utilising the polycrystalline and amorphous *p*-type GaSb films which have previously been characterised in Chapter 4.

GaSb shows promise for *p*-type devices due to its high hole mobilities. High mobility materials have the potential to replace silicon in traditional devices, thereby lowering the supply voltage required without making sacrifices elsewhere e.g., I_{ON}/I_{OFF} ratios. Power density on chip is one of the greatest problems encountered with aggressive dimensional scaling of devices, but also one which could be mitigated through a reduction in the supply voltage [1], as power dissipation on chip is proportional to the supply voltage.

GaSb *p*-type channel MOSFETs have been demonstrated in the literature [2–5]. Growing polar GaSb on amorphous and non-polar SiO_2 is a difficult task, but one that must be overcome if III-V materials are to be economically viable for consumer electronics, due to the higher costs associated with III-V substrates [6]. Of the demonstrations in the literature referenced above, two are grown on silicon substrates, and only one on SiO_2 [2]. In the case of [2], the GaSb nanowires were grown by a Chemical Vapour Deposition (CVD) process at 670°C and were subsequently drop cast onto a silicon substrate with 600nm of SiO_2 . When these GaSb nanowire MOSFETs were measured, the transfer characteristics exhibited I_{ON}/I_{OFF} values <2 at room temperature, and temperatures $<42\text{ K}$ were required for I_{ON}/I_{OFF} values $>10^4$.

Junctionless transistor architectures are implemented for the GaSb devices in this chapter. This device design is advantageous for modern electronics as

the source and drain regions do not require doping gradients into the channel. With decreasing device dimensions, this doping gradient becomes steeper and more challenging to engineer [7]. With traditional doping methods, the average doping concentration can be precisely controlled; however, this cannot be said for the location of the atoms themselves. As dimensions of the device decreases, the uncertainty of the position of the dopant atoms becomes significant [1]. In a junctionless transistor, the workfunction of the gate metal and the gate voltage are exploited to deplete the channel of carriers [8] and yield a nominally OFF device.

5.3 Experimental

The poly GaSb films were grown by Metalorganic Vapour Phase Epitaxy (MOVPE) as described in Section 4.3. Junctionless transistor devices were fabricated by first patterning and depositing source and drain metal contacts (10 nm Ti: 200 nm Au). Next the channel region was defined and isolated using a wet etch of $\text{1HNO}_3\text{:3C}_6\text{H}_8\text{O}_7$. A surface treatment consisting of a 5 minute dip in $(\text{NH}_4)_2\text{S}$ was used prior to 20 nm Al_2O_3 gate dielectric deposition by ALD. Top-gating was achieved through photolithography patterning, 40 nm Pd deposition by metal evaporation, and a standard lift-off procedure. Figure 5.1 shows a schematic representation of the resulting transistor device layout.

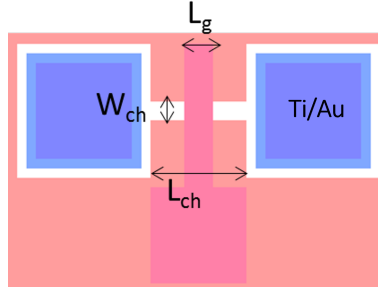


Figure 5.1: Schematic of junctionless transistor device layout.

Device characteristics were measured on a Cascade semi-automatic prober at room temperature or variable temperatures using an Agilent B1500 device parameter analyser. Electrical results for devices presented in the chapter were chosen as they either represented the “best” results achieved, or were devices capable of being measured on multiple samples to allow for comparison.

5.4 Results and Discussion

5.4.1 cTLM Results

Hall measurement results for the GaSb films used for the transistors discussed in this chapter are presented in Section 4.4.1. The sheet resistivity determined through Hall effect measurements involves a relatively large area sample (1 cm x 1 cm piece) when compared to the devices to be fabricated ($\mu\text{m} \times \mu\text{m}$). There is considerable non-uniformity in the poly GaSb films over smaller areas (Figure 4.1), and so it was important to check whether these

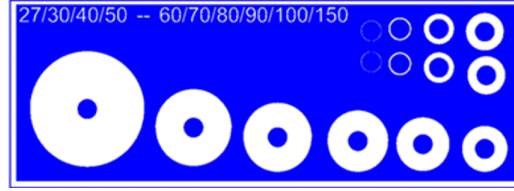


Figure 5.2: Schematic of cTLM structure layout.

large area measurements held true over dimensions more closely resembling the devices which were to be fabricated. To achieve this, circular Transmission Line Measurement (cTLM) structures were fabricated on the GaSb films, a schematic of this structure is shown in Figure 5.2 where the blue areas represent Ti:Au metal contacts. A detailed description of how these sheet resistivities were extracted can be found in Appendix B. The results are shown in Table 5.1. It is evident from Table 5.1 that the figures for sheet resistivity found through Hall effect measurements and cTLM measurements are in impressive agreement. This agreement between large area (Hall effect) and small area (cTLM) methods provides evidence that the techniques of extracting this data are reliable, and that the sample has not been adversely affected during the processing steps necessary to fabricate these structures.

Interestingly, the 50 nm GaSb sample on the substrate provided by an industry partner for this project could not have its values determined through cTLM. This was because the GaSb lacked sufficient continuity to produce the trend needed for calculating the parameters of the film. However, a 50 nm GaSb sample grown on a Si/SiO₂ substrate produced in Tyndall could

be measured and have its parameters extracted using this technique. The substrate produced in Tyndall has a thinner oxide than the substrates provided by industry (85 nm thermally grown oxide for the Tyndall substrate versus an approximately 110 nm thick oxide for the industry substrate). This observation follows from the previous findings in Chapter 4, that the substrate has a strong influence on the quality and properties of the GaSb film. This particular result was discovered after device processing on the 50 nm sample on the industry silicon substrate had been completed, and as the 150 nm and 250 nm samples are grown on this substrate also, for the purpose of comparison, this sample is used for the device results presented in this section (excluding cTLM results for 50 nm GaSb in Table 5.1 and Table 5.3). Results from the devices fabricated with the 50 nm GaSb on the Tyndall silicon substrate are presented in Section 5.4.3 for completeness.

The specific contact resistivity is also presented in Table 5.1, and these values follow the trend of the resistivity in the films themselves, with higher levels of sheet resistivity resulting in larger values for specific contact resistivity. The values for specific contact resistivity are quite high compared to what would be acceptable in an industry context, however these values could probably be improved by a treatment to remove the native oxides on the surface before depositing the metal contacts, as was shown for the InAs films in Section 2.4.2.

Film Details	cTLM: ρ_c ($\Omega \cdot \text{cm}^2$)	cTLM: Sheet Res (Ω/sq)	Hall: Sheet Res (Ω/sq)
50nm GaSb on SiO ₂ /Si	0.85	2.08x10 ⁶	2.6x10 ⁶
150nm GaSb on SiO ₂ /Si	0.033	8.27x10 ⁴	8.37x10 ⁴
250nm GaSb on SiO ₂ /Si	0.027	2.19x10 ⁴	1.9x10 ⁴
GaAs + GaSb on SiO ₂ /Si	0.05	4.56x10 ⁵	4.17x10 ⁵
150nm GaSb on GaAs	0.024	7.36x10 ³	6.13x10 ³
250nm GaSb on GaAs	0.0016	5.48x10 ³	6.56x10 ³
GaAs + GaSb on GaAs	0.006	1.29x10 ⁴	1.73x10 ⁴

Table 5.1: Comparison of resistivity data extracted from cTLM and Hall effect measurements.

5.4.2 Back-gated Device Results

Source/drain metal contacts were deposited, and the channel region was defined using photolithography followed by a wet etch consisting of 1HNO₃:3C₆H₈O₇ [9]. This wet etch was tested on un-patterned pieces of the samples to determine the ideal duration of the etch. This was necessary as the etch was designed for crystalline GaSb, rather than polycrystalline or amorphous ones studied here. An etch which is selective to certain crystal orientations will still etch laterally to some degree in these films. Time periods from 30 s to 2 minutes were tested and Energy-Dispersive X-Ray (EDX) was performed to check if there was GaSb still present on the surface. It was found that the minimum time necessary for GaSb to not be detected on the surface was 1 minute, and this duration was selected to minimise the lateral etching of the channel region which would result in narrowing of the channel compared to the intended and labelled dimensions.

When the channels were defined, it was possible to back-gate some of the structures grown on the silicon substrate. This was not possible for any of the samples with a GaAs buffer layer, as this proved too resistive to back-gate through. Figure 5.3 shows the IV characteristics of three samples which were capable of being back-gated. From Figure 5.3, it is clear that the thicker the film, the harder it is to deplete and effectively turn off the transistor. This results in the 50 nm GaSb film having the highest room temperature I_{ON}/I_{OFF} at 205. The 50 nm GaSb devices showed significant variation across the area of the sample (approx 1 cm²) that was not evident for the 150 or 250 nm samples. This was expected due to the non-uniformity observed in Figure ??a. While the 50 nm GaSb film had the highest I_{ON}/I_{OFF} , the absolute value of the ON-current is not particularly high at around 0.1 nA/ μ m. The 250 nm GaSb film device, Figure 5.3c, has the lowest I_{ON}/I_{OFF} ratio, however it has the highest I_{ON} of all the devices at $>1.2 \mu$ A. This is important to consider as through top-gating with a thinner oxide and a specifically selected gate metal, depletion of the channel can be improved, thereby improving the I_{OFF} value, however the I_{ON} value is dependent on the intrinsic properties of the film and cannot be so easily altered. The 150 nm film device, Figure 5.3b, has neither a particularly impressive I_{ON} nor I_{ON}/I_{OFF} ratio. Figure 5.3d shows the values for I_{ON} and I_{OFF} vs channel thickness. It is clear from this plot that I_{OFF} is much more dependent on film thickness than I_{ON} . The anti-clockwise hysteresis present in all of the transfer characteristics is indicative of hole trapping. The charge trapping for all the devices in Figure 5.3 was

found to be in the range of $5\text{-}6.5 \times 10^{13} \text{ cm}^{-2}$.

The back-gated output characteristics of the same samples as shown in Figure 5.3 are shown in Figure 5.4. The 50 nm GaSb sample, Figure 5.4a, shows some saturation as would be expected for classical transistor behaviour. Neither of the 150 or 250 nm samples show any saturation despite the large range of the V_{DS} sweep. This behaviour could be mitigated through top-gating. The relatively linear nature of the I_{DS} - V_{DS} curves for the 150 nm and 250 nm samples indicated relatively good ohmic behaviour of the Ti:Au contacts to the GaSb channel.

The GaSb surface is expected to form native oxides when left exposed to air. These oxides can result in Fermi level pinning at the surface, making it difficult to modulate the Fermi level using the gate voltage. To mitigate this, III-V semiconductors should receive a surface treatment/passivation and deposition of a suitable gate oxide before a gate contact is put down. Based on previous research [10], it was decided to perform a surface treatment with a 1% solution of $(\text{NH}_4)_2\text{S}$ before ALD of the gate dielectric, 20 nm Al_2O_3 . There was some concern that due to the polycrystalline or amorphous nature of the films, the slight etching effect of the surface treatment may significantly change the properties and thickness of the film or change the dimensions of the channel regions. For this reason, test pieces of the sample were dipped into the solution for different durations, and then checked under the SEM

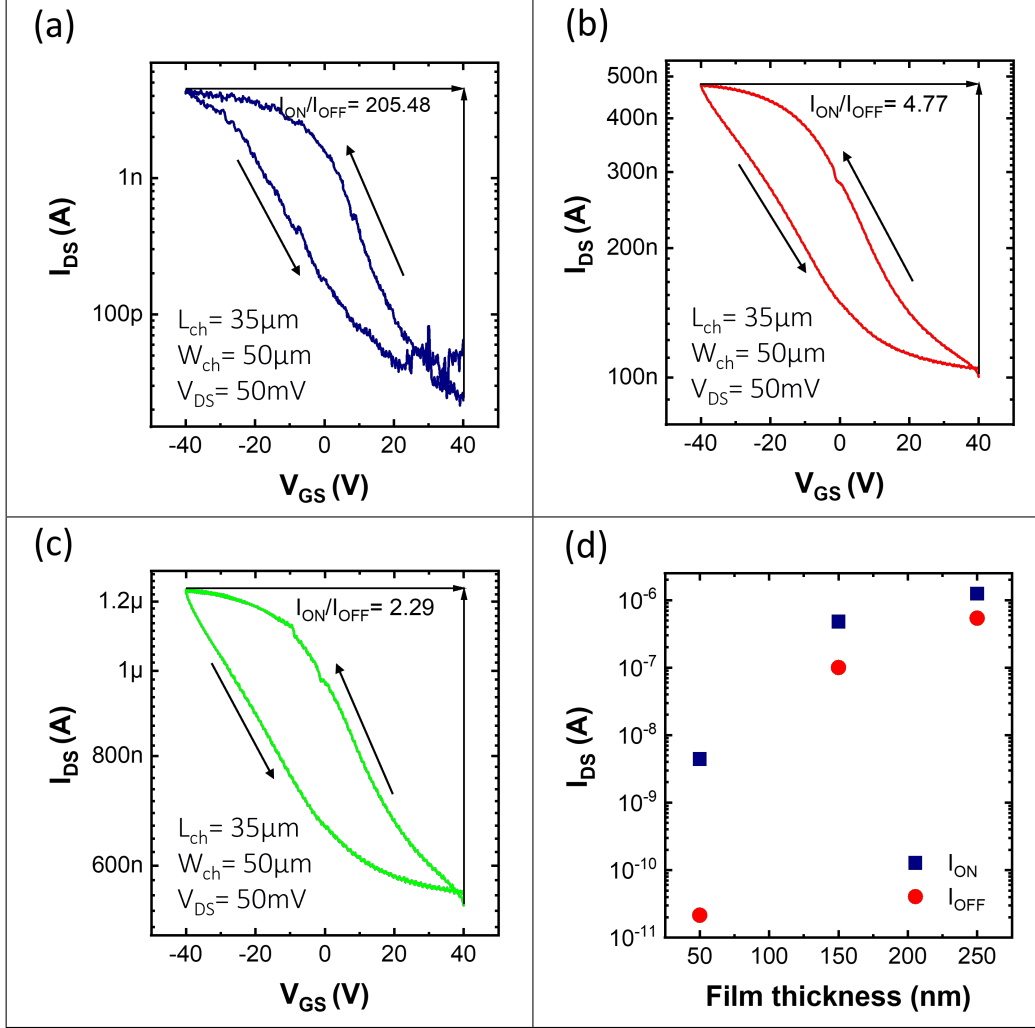


Figure 5.3: Back-gated IV characteristics of transistors with a channel material of (a) 50 nm, (b) 150 nm, and (c) 250 nm GaSb on Si/SiO₂. (d) The values for I_{ON} and I_{OFF} vs nominal film thickness for each sample.

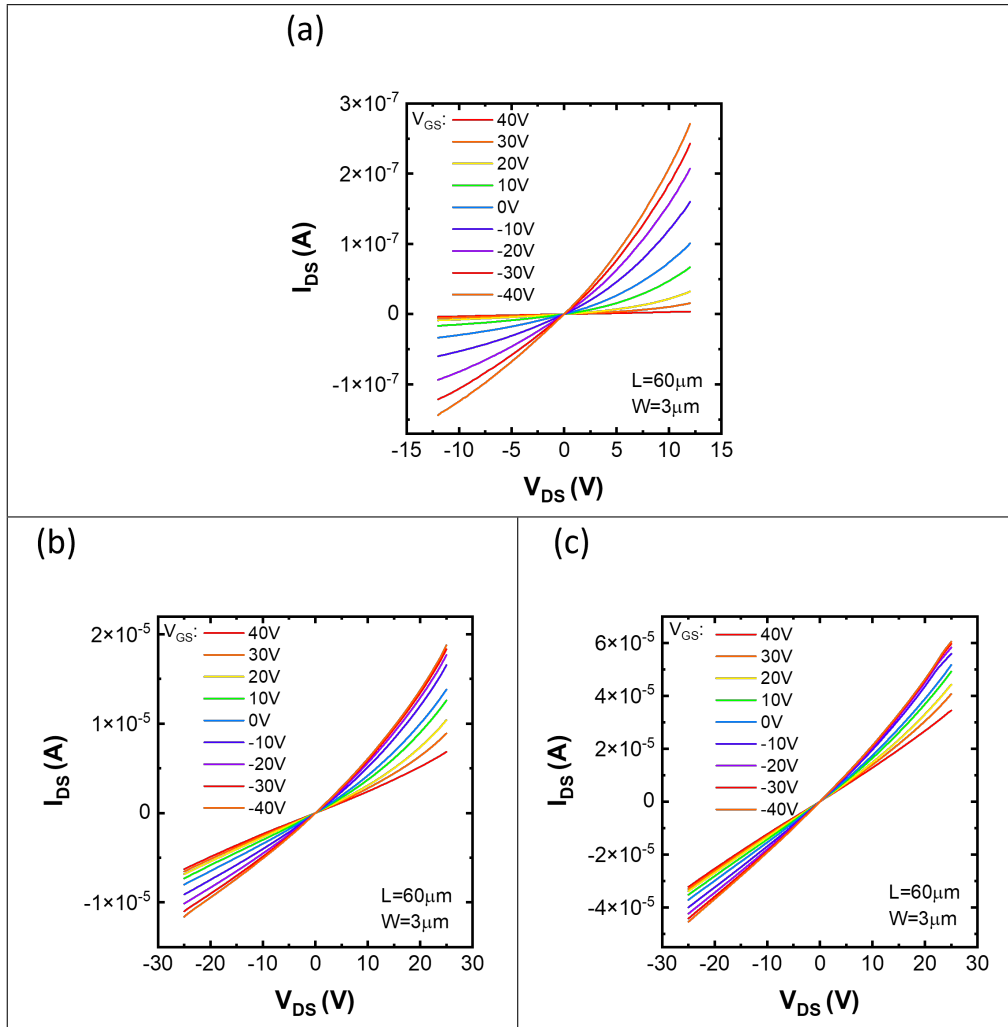


Figure 5.4: I_{DS} - V_{DS} output curves for devices with GaSb channel thickness of (a) 50 nm, (b) 150 nm, and (c) 250 nm.

for changes in structure/composition when compared to a reference piece. It was decided that a 5-minute dip in the solution was the optimal duration.

Back-gated transfer characteristics were measured before and after oxide deposition and are shown in Figure 5.5. There was some variation in the measured current values across all the samples analysed, so examples which represent the majority of the measurements for each sample are shown in Figure 5.5. Considering firstly the 50 nm sample (Figure 5.5a), the I_{ON} is slightly increased. The dramatic effect of the top Al_2O_3 layer is the reduction in the I_{ON}/I_{OFF} ratio, which is a result of a consistently higher I_{OFF} following the Al_2O_3 deposition. The other significant observation is that following the top oxide deposition there is a dramatic reduction in the I_{DS} vs V_{GS} hysteresis. The 150 nm and 250 nm samples showed generally similar results, with both I_{ON} and I_{OFF} increasing compared to the prior measurements and a reduction in the I_{DS} vs V_{GS} hysteresis. Considering the increase in I_{ON} following the Al_2O_3 deposition, this was an unexpected result as usually the Al_2O_3 oxide deposited by ALD will have a net positive charge for film thickness values larger than 5 nm, which would induce a negative charge in the channel [11]. For a p -channel device, this would mean a reduction in carrier concentration, which should cause a reduction in conductivity. This experimental observation indicates that for the 20nm Al_2O_3 deposition on the poly GaSb, the net oxide charge is negative. Considering the marked reduction in device hysteresis after the top oxide formation, this suggests that the trapping causing

the hysteresis was occurring at the channel surface and was mitigated by the surface treatment. The anti-clockwise hysteresis present prior to the oxide deposition was indicative of hole trapping, reducing the conductivity on the backward sweep.

Temperature dependent transfer characteristics were measured on the 50 nm sample before and after surface treatment and oxide deposition are shown in Figure 5.6. The reduction in hysteresis and I_{ON}/I_{OFF} ratio between Figure 5.6a and Figure 5.6b is evident at every temperature. In Figure 5.6c the pre surface treatment and oxide deposition sample reaches the highest I_{ON}/I_{OFF} ratio seen in the GaSb devices thus far, 550 at -50°C . This ratio decreases continually as temperature increases. I_{OFF} is much more strongly temperature dependent than I_{ON} . Figure 5.6d shows that post surface treatment and oxide deposition, the strong dependence on temperature is absent. I_{ON} and I_{OFF} continually increase with temperature increasing, except for one outlier at 30°C . There is not a clear trend of I_{ON}/I_{OFF} with temperature post oxide deposition. This indicates that different mechanisms are controlling the current at ON and OFF states post-oxide as compared to pre-oxide. The activation energy of the OFF-current changes from 1.98eV prior to oxide deposition to 0.5eV post oxide deposition.

The cTLM structures on the samples were remeasured to see how the fundamental properties of the film and the structures had changed. Results of

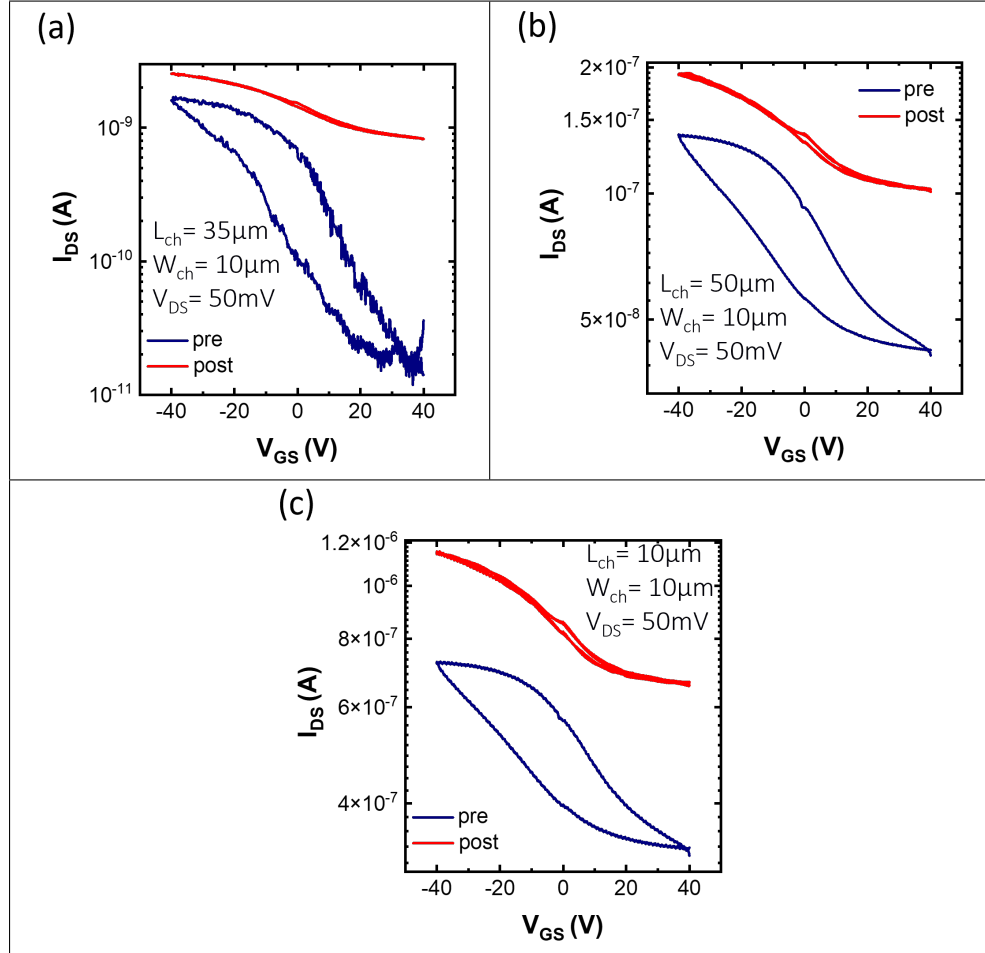


Figure 5.5: Pre and post oxide deposition IV characteristics of samples with GaSb channel thickness of (a) 50 nm, (b) 150 nm, and (c) 250 nm.

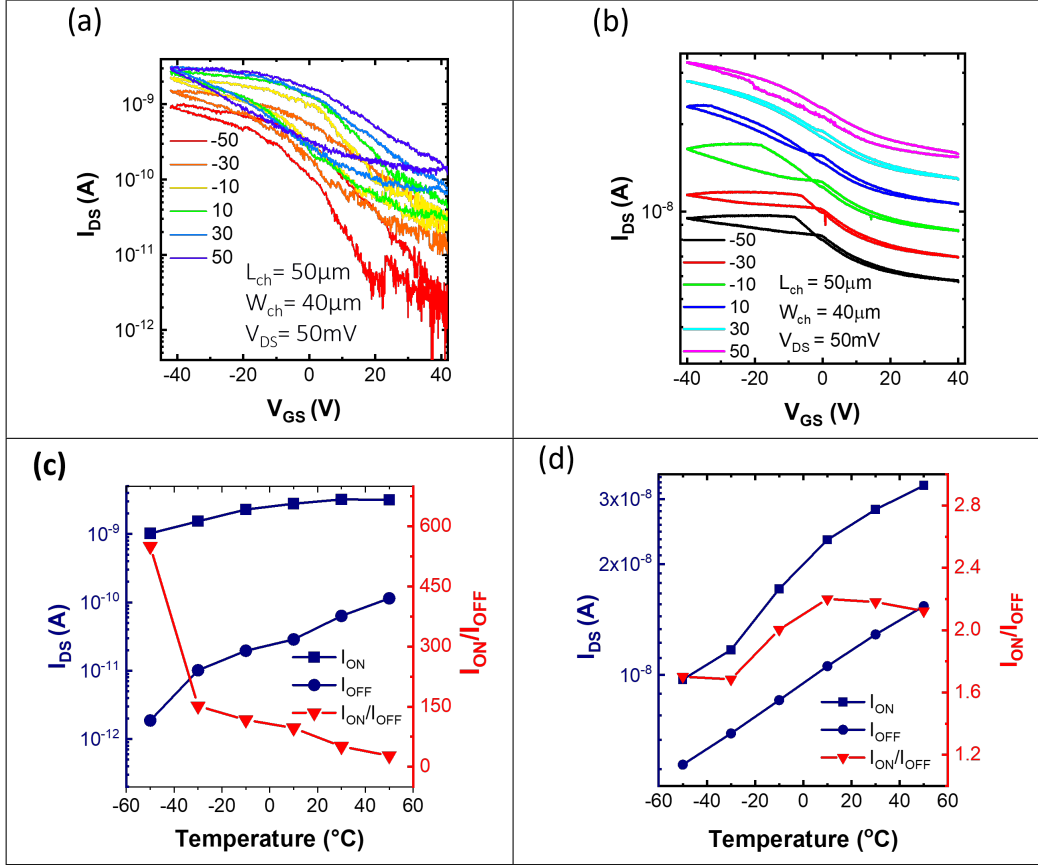


Figure 5.6: Temperature dependent I_{DS} - V_{GS} of 50 nm GaSb sample (a) pre and (b) post surface treatment and oxide deposition. Comparison of I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} ratio (c) pre and (d) post.

Parameter	150nm on SiO ₂	250nm on SiO ₂	GaAs + GaSb on SiO ₂
ρ_c pre ($\Omega\cdot\text{cm}^2$)	2.35×10^{-2}	1.58×10^{-3}	6×10^{-3}
ρ_c post ($\Omega\cdot\text{cm}^2$)	2.89×10^{-4}	3.7×10^{-5}	N/A
R_{sh} pre (Ω/sq)	7.36×10^3	5.48×10^3	1.29×10^4
R_{sh} post (Ω/sq)	2.56×10^4	3.23×10^4	2.79×10^5
R_{sh} Hall (Ω/sq)	6.13×10^3	6.56×10^3	1.73×10^4

Table 5.2: cTLM results from GaSb devices post oxide deposition, with comparison to pre oxide results and Hall measurements.

these measurements are presented in Table 5.2. In contrast to the prior measurements, results of which are presented in Table 5.1, the 50 nm GaAs + 50 nm GaSb had a negative y-intercept on the R_{TOT} vs gap, which cannot be a true result. As only the contact resistivity is calculated from the y-intercept, the sheet resistivity has been presented in the table (calculated from the slope of the graph), though it should only be taken as indicative. The sheet resistance increased pre and post surface treatment and oxide deposition. This shows that the oxide deposition had the expected effect - inducing negative charge, thereby decreasing the conductivity of the p -channel. Interestingly, the specific contact resistance decreased after oxide deposition, and it is this decrease in the specific contact resistance which resulted in the increase in drain current (see Figure 5.5), despite the increase in sheet resistance.

It was thought that the specific contact resistivity might have significantly decreased due to an “annealing” effect on the Ti:Au source/drain contacts during the ALD process (250°C). This was tested by taking a piece of 50nm GaSb on the Tyndall SiO₂ substrate with Ti:Au contacts and exposing it to

Description	R_{sh} (Ω/sq)	R_c (Ω)	ρ_c ($\Omega\cdot\text{cm}^2$)	L_t (μm)
Pre-anneal	2.3×10^6	9.8×10^4	1	6.68
Post-anneal	3.12×10^6	5.7×10^4	0.26	2.86

Table 5.3: Pre- and post-annealing cTLM results for 50 nm GaSb on SiO_2 .

a similar temperature and duration to the sample which had been through ALD process, however without the added effect of the top-oxide deposition. The annealing parameters chosen to replicate this as closely as possible were 250°C for 2.5 hours in an Argon environment. The results from the sample before and after the “annealing” process are shown in Table 5.3. The same trend in contact resistance is evident in this data as was seen in the samples which had undergone oxide deposition, though the specific contact resistivity only decreases by one order of magnitude compared to two for ALD samples. The 50 nm samples are not completely uniform so the contact resistivity may not be as strongly affected by changes in the interface between the contact and the film i.e., not all of the metal contact is in contact with the film. The sheet resistance of the film is also not significantly affected, which is expected as no oxide has been deposited on this sample, meaning no associated charge has been induced in the semiconductor.

5.4.3 50nm GaSb on a Tyndall Silicon Substrate

As discussed in Section 5.4.1, the 50 nm GaSb sample on the industry substrate (p^+ Si with an approx. 110 nm SiO_2 oxide) was not capable of having its parameters determined through cTLM. However, a 50 nm sample grown

on a Tyndall silicon substrate during the same growth run was capable of producing usable cTLM data. Devices were processed on this sample. Ni:Au source/drain contacts were patterned and defined using a standard lift-off procedure. The channel was defined and etched using the same wet etch as the other devices, $1\text{HNO}_3:3\text{C}_6\text{H}_8\text{O}_7$. Back-gated device results prior to any surface treatments or gate oxide deposition are shown in Figure 5.7. The film does not display a significant difference in $I_{\text{ON}}/I_{\text{OFF}}$ ratio. This could be due to the fact that the greater level of continuity allows for a higher I_{ON} , however is detrimental to the ability to fully deplete the channel, meaning I_{OFF} is degraded. Figure 5.7a shows the anti-clockwise hysteresis present in these measurements. This behaviour does not appear to be dependent on V_{DS} .

Back-gated output characteristics of the 50nm GaSb film on the Tyndall SiO_2 substrate are shown in Figure 5.8. These characteristics are very similar to those of the 50 nm film on the industry SiO_2 substrate shown in Figure 5.4a, with the current levels being only marginally lower for devices with the same dimensions.

Temperature dependent back-gated measurements were also carried out on the devices fabricated using this sample. The results from these measurements are shown in Figure 5.9. The temperature dependent measurements show the same trend as the sample on the industry silicon, whereby the

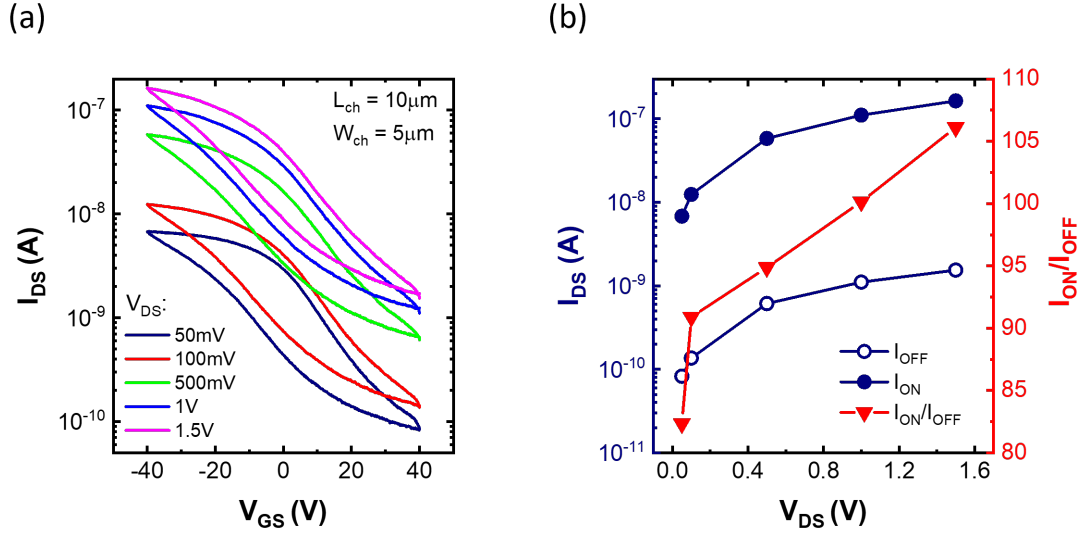


Figure 5.7: (a) Transfer characteristics of 50 nm GaSb film on Tyndall Si/SiO₂ substrate. (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} taken from the same measurements. I_{ON} is taken at $V_{GS} = -40$ V, and I_{OFF} is taken at $V_{GS} = 40$ V.

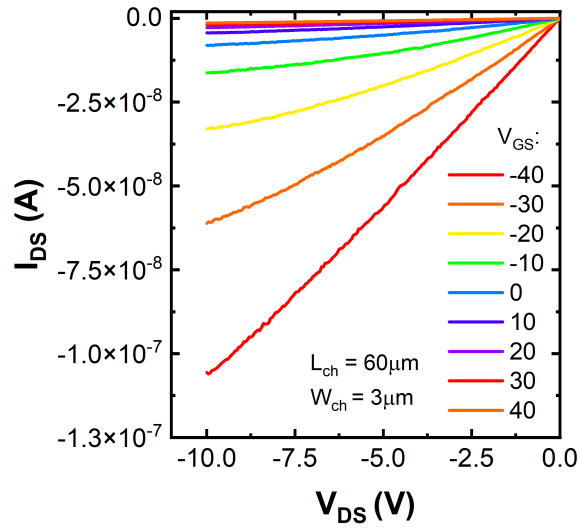


Figure 5.8: Output characteristics of 50 nm GaSb film on Tyndall Si/SiO₂ substrate.

Measurement Temperature (degrees C)	Voltage Difference (V)
30	20.9
10	17.5
-10	11.7
-30	8
-50	8

Table 5.4: Comparison of gate voltage difference for different temperatures, taken at 10^{-9} A on each side of the hysteresis of transfer characteristics in Figure 5.9.

I_{ON}/I_{OFF} ratio decreases with increasing temperature, mostly due to a change in I_{OFF} . From Figure 5.9a, it is clear that the anti-clockwise hysteresis present in the IVs reduced significantly in the measurements performed at -30°C and -50°C compared to the measurements performed at higher temperatures. This shows that the mechanism for hole trapping in the GaSb films which have not undergone any surface treatments or oxide deposition is thermally activated. Table 5.4 shows the gate voltage difference for each of the temperatures between the two sides of the hysteresis when taken at a drain voltage of 10^{-9} A. This clearly shows the dependence of the hysteresis on measurement temperature. This clearly shows the dependence of the hysteresis on measurement temperature and suggests that the mechanism for hole trapping in the GaSb films which have not undergone any surface treatments or oxide deposition is thermally activated.

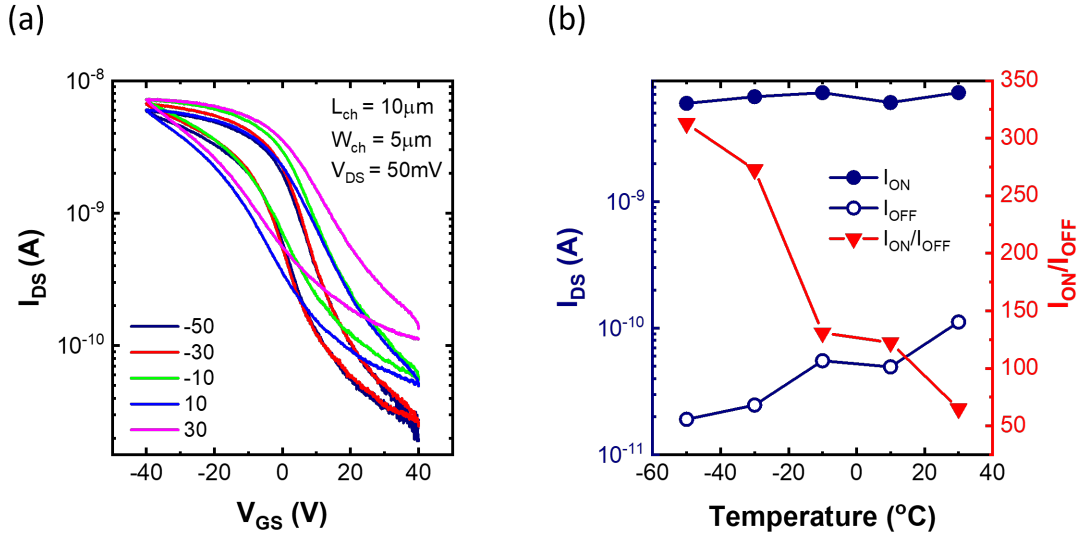


Figure 5.9: (a) Transfer characteristics of 50 nm GaSb film on Tyndall Si/SiO₂ substrate at variable temperature. (b) I_{ON} , I_{OFF} , and I_{ON}/I_{OFF} taken from the same measurements.

5.4.4 Top-gated Device Results

While it proved difficult to fully deplete the InAs channel devices in Chapter 3, due to the lower carrier concentration in the GaSb films, this was not predicted to be an issue for these devices once they had a well-engineered gate stack compared to the back-gating through the lowly doped substrate (hole concentration = 1.17×10^{15}) with a thick oxide layer (around 110 nm of SiO₂). The calculated maximum depletion width vs carrier concentration is shown in Figure 5.10. The GaSb films have carrier concentrations in the range of 10^{16} - 10^{17} cm⁻³. From Figure 5.10, we can conclude that it should be possible to fully deplete the channel thicknesses used for these devices, especially as the actual thickness deviates from the nominal thickness, with

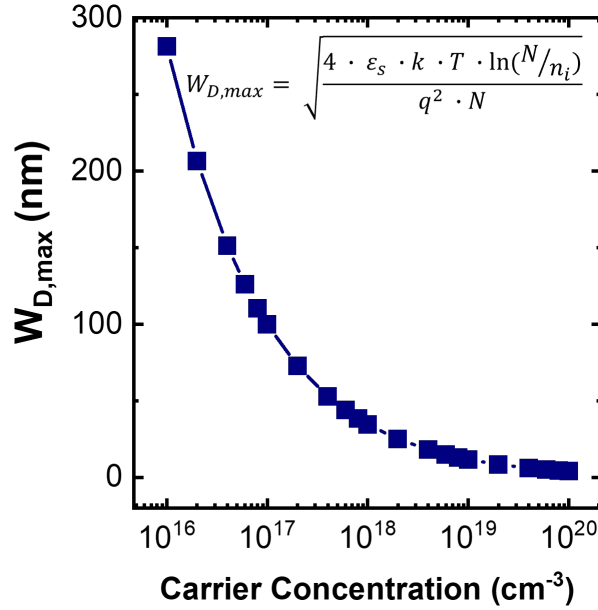


Figure 5.10: Maximum depletion width vs carrier concentration for GaSb. Inset: Equation used for calculations and plotting.

significant areas being thinner than the nominal value, allowing for easier depletion. This would be compounded by the possibility of dual gating, as with InAs devices in Chapter 3, thereby depleting from the top and bottom of the channel at the same time, and essentially doubling the maximum depletion width possible.

A 40 nm Pd gate contact was deposited by metal evaporation using patterning by photolithography and a standard lift-off procedure. Initial measurements on the top-gated devices showed that modulation of the current using the top-gate voltage was not possible whether the back gate was also implemented or not. It was observed that the gate oxide would break down

at relatively low top-gate voltages (around 2 V). This effect could be mitigated by employing the back-gate voltage, where bias was applied through the chuck and held at a constant level for the duration of the voltage sweep of the top gate. However, as this is a relatively low voltage for oxide breakdown of a 20 nm Al_2O_3 layer deposited by ALD, it was deemed necessary to anneal the samples.

5.4.5 Dual-Gated Device Results

As explored for the InAs devices in Section 3.4.2, dual-gating was employed as a method to improve the device characteristics of the GaSb transistors. Again, the method by which this could be achieved was holding the back gate at a set potential while sweeping the top-gate voltage. As discussed in Section 5.4.4, when the top-gate metal was first deposited, it was impossible to modulate the drain current using the top-gate voltage. An attempt at this top-gated measurement using the 50 nm GaSb on SiO_2 is shown in Figure 5.11a. Using the bottom-gate voltage, it was possible to cause some level of modulation in the current, however only at the negative voltages. This effect is shown in Figure 5.11b.

This phenomenon makes more sense when the device structure (shown in Figure 5.1) is considered more carefully. There is an area between the gate and the source/drain contacts where the channel is un-gated. This area of GaSb, unlike that under the source/drain contacts, has been exposed to the

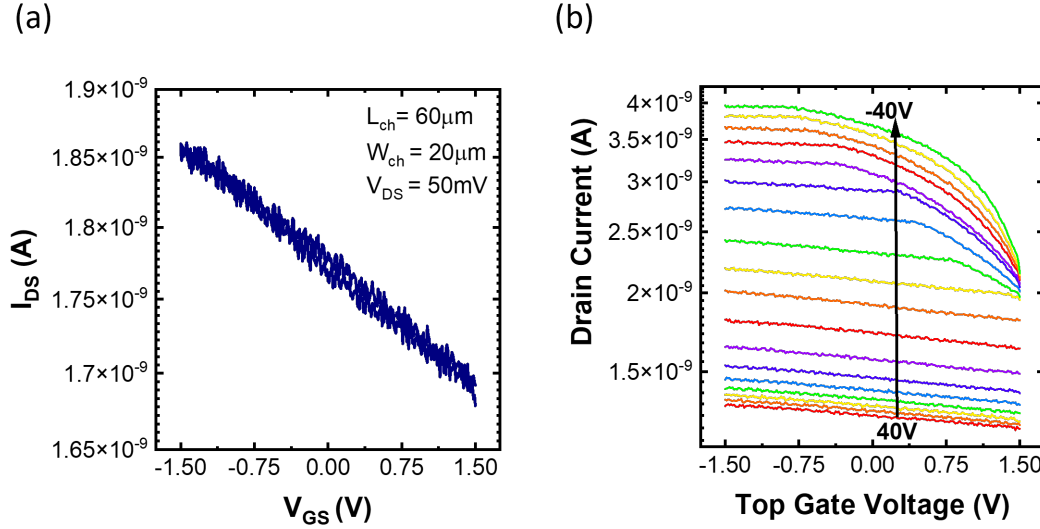


Figure 5.11: (a) IV measurement of 50 nm GaSb on SiO_2 using only the top-gate, prior to annealing. (b) IV measurement of the same film and device using both gates. Back-gate potential range is shown in graph.

oxide deposition, and therefore has had negative charge induced, lowering the conductivity. This creates something resembling an n-p-n junction along the length of the channel. When the back-gate potential is applied at a sufficiently negative voltage, it can induce enough charge in the channel that it overcomes the negative charge induced by the oxide, thereby allowing the top-gate to modulate the channel current somewhat.

Figure 5.12 shows sheet resistivity determined through cTLM measurements. The voltage on the substrate was varied to demonstrate the effect on the sheet resistivity of the channel. It is clear from these measurements that the voltage on the substrate effects the sheet resistivity of the film, with more negative voltages reducing the sheet resistivity. This discovery was another

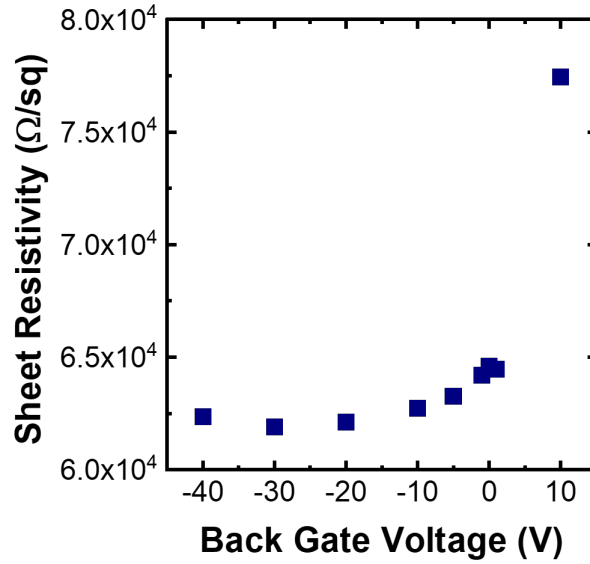


Figure 5.12: Sheet resistivity values determined through cTLM measurements for the 150 nm sample vs “back-gate” voltage.

reason why it was decided to anneal the samples, as this method can be used to reduce interface charges and charges induced by the deposited oxide. Based on previous research [12], a Forming Gas Anneal (FGA) at 300°C for 30 minutes was chosen.

Figure 5.13 shows the transfer characteristics of dual-gated devices with 50 nm or 250 nm GaSb film channels. These measurements were taken with the two gates swept at the same time, with the ratio of back-gate to top-gate voltage shown in the graph legend. While it is clear that the method of sweeping both gates simultaneously has improved upon the method of holding the back-gate at a constant potential and only sweeping the top-gate (see Figure 5.11) the $I_{\text{ON}}/I_{\text{OFF}}$ ratio still remains degraded for the 50 nm

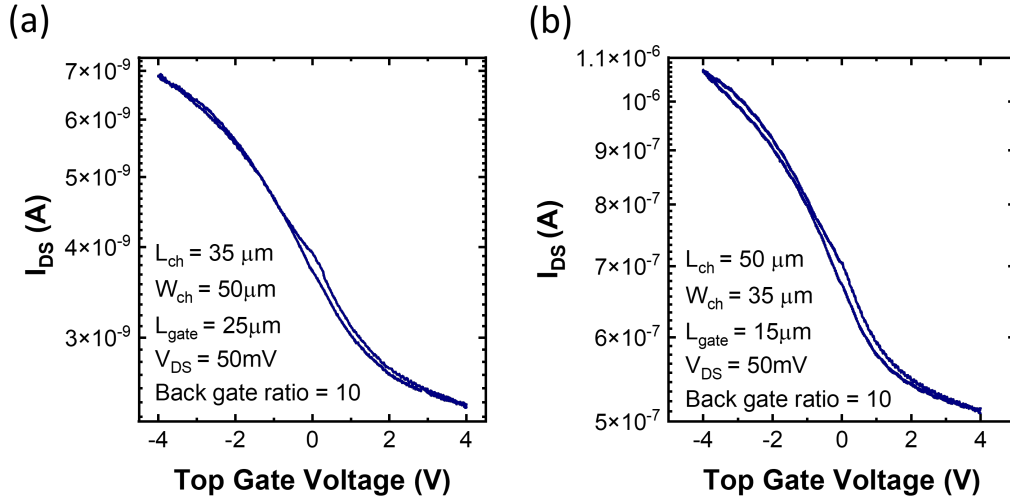


Figure 5.13: Dual-gated transfer characteristics of devices whose channels are (a) 50 nm and (b) 250 nm polycrystalline GaSb.

GaSb sample, while reaching the same values as prior to top-gating for the 250 nm sample. A ratio of 1:10 was chosen for the top- to back-gate voltage ratio based on the C_{ox} ratio between the two different oxides with different thicknesses and also what could be achieved without damaging the device (breaking through the top oxide) or causing excessive leakage. From these results we can conclude that the FGA did not have the level of effect that was hoped for in improving the performance of the top-gate stack.

5.5 Benchmarking

Table 5.5 shows devices fabricated and measured in this chapter compared to devices demonstrated in the literature. When making this comparison it is important to remember that the materials in this chapter are polycrystalline

Thin Film Polycrystalline GaSb MOSFETs

III-V Material	L (μm)	I_{ON} ($\mu\text{A}/\mu\text{m}$)	V_{ON} (V)	I_{OFF} ($\mu\text{A}/\mu\text{m}$)	V_{OFF} (V)	V_{DS} (V)	$I_{\text{ON}}/I_{\text{OFF}}$	$SS \cdot C_{\text{ox}}$ ($\frac{\text{s}}{\text{cm}^2} \cdot 10^{-3}$)	Device Type	Growth Substrate	Year	Ref
GaSb	0.06	20	-1	0.03	0.5	0.5	700	3.37	NW MOS-FET	InAs	2020	[3]
InGaSb	0.02	100	-0.5	2	0.5	0.5	50	5.92	finFET	GaAs	2017	[13]
GaSb	0.5	10	-1.5	0.002	-0.25	0.05	5000	2.99	NW pFET	GeOI	2015	[14]
GaSb	1	20	-1.5	0.02	0	0.05	1000	-	pMOS	GaSb	2014	[15]
InGaSb	2.6	-	-1	-	0	1	100	3.04	pMOS	SiO ₂	2012	[16]
GaSb	50	0.2	-4	0.002	0	0.05	100	-	pMOS	InAs	2014	[17]
poly GaSb	35	8.9×10^{-5}	-40	4.3×10^{-7}	40	0.05	205	66.2	Junction-less transistor	SiO ₂	2021	This Work

Table 5.5: Examples of functional p -type III-V based transistors from the literature compared with devices fabricated in this chapter.

or amorphous and grown on amorphous substrates. The ON-current for the 50 nm GaSb film is not impressive compared to the other devices shown in this table, however the OFF-current is much better, and the $I_{\text{ON}}/I_{\text{OFF}}$ ratio is comparable. The subthreshold swing for the back-gated device is very high due to the thick oxide (approx 110 nm) on the silicon substrate.

5.6 Conclusions

In this chapter, functional GaSb devices have been demonstrated, with the highest room temperature $I_{\text{ON}}/I_{\text{OFF}}$ of 205 being achieved for a 50 nm poly GaSb film on Si/SiO₂ substrate, and the highest overall $I_{\text{ON}}/I_{\text{OFF}}$ of 550 being achieved for the same sample at -50°C. While the 50 nm film on Si/SiO₂ had the greatest $I_{\text{ON}}/I_{\text{OFF}}$ ratios, it could not achieve an impressive ON current. The 250 nm GaSb film could achieve a reasonable ON current, however not the $I_{\text{ON}}/I_{\text{OFF}}$ ratio. This indicates, like the InAs films, a thicker overgrowth with subsequent planarization would be beneficial for achieving

the high ON current that the continuity of the 250 nm film could achieve, with the $I_{\text{ON}}/I_{\text{OFF}}$ values that the thinner 50 nm film could achieve. Benchmarking against other *p*-type III-V material transistors from the literature shows that the $I_{\text{ON}}/I_{\text{OFF}}$ value achieved in this chapter is comparable to other devices fabricated with a SiO_2 growth substrate, and also to those grown on III-V wafers. These findings show that there is scope and clear pathways to improve device performance, such as growth of thicker films with subsequent thinning to improve continuity in the channel material, and systematic studies of suitable gate stacks for these devices. The results in this chapter however already demonstrate that these high hole mobility films have great potential for implementation in devices integrated in the back-end-of-line (BEOL).

Bibliography

- [1] D. J. Frank, “Power-constrained CMOS scaling limits,” *IBM Journal of Research and Development*, vol. 46, no. 2.3, pp. 235–244, 2002.
- [2] G. Xu, S. Huang, X. Wang, B. Yu, H. Zhang, T. Yang, H. Xu, and L. Dai, “Synthesis, properties, and top-gated metal–oxide–semiconductor field-effect transistors of p -type GaSb nanowires,” *RSC advances*, vol. 3, no. 43, pp. 19834–19839, 2013.
- [3] A. Jönsson, J. Svensson, E. Lind, and L.-E. Wernersson, “Gate-length dependence of vertical GaSb nanowire p -MOSFETs on Si,” *IEEE Transactions on Electron Devices*, vol. 67, no. 10, pp. 4118–4122, 2020.
- [4] M. Yokoyama, K. Nishi, S. Kim, H. Yokoyama, M. Takenaka, and S. Takagi, “Self-aligned Ni-GaSb source/drain junctions for GaSb p -channel metal-oxide-semiconductor field-effect transistors,” *Applied Physics Letters*, vol. 104, no. 9, p. 093509, 2014.
- [5] M.-L. Tsai, Y.-P. Chang, and C.-H. Chien, “Enhancing the thermal sta-

- bility of GaSb Schottky-barrier MOSFET with Pt source/drain,” *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 939–942, 2018.
- [6] K. Takei, M. Madsen, H. Fang, R. Kapadia, S. Chuang, H. S. Kim, C.-H. Liu, E. Plis, J. Nah, S. Krishna, *et al.*, “Nanoscale InGaSb heterostructure membranes on Si substrates for high hole mobility transistors,” *Nano letters*, vol. 12, no. 4, pp. 2060–2066, 2012.
- [7] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O’Neill, A. Blake, M. White, *et al.*, “Nanowire transistors without junctions,” *Nature nanotechnology*, vol. 5, no. 3, pp. 225–229, 2010.
- [8] J.-P. Colinge, A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, and P. Razavi, “Junctionless nanowire transistor (JNT): Properties and design guidelines,” *Solid-State Electronics*, vol. 65, pp. 33–37, 2011.
- [9] E. Papis-Polakowska, “Surface treatment of GaSb and related materials for the processing of mid-infrared semiconductor devices,” *Electron Technology: Internet Journal*, vol. 37, no. 4, pp. 1–34, 2005.
- [10] U. Peralagu, I. M. Povey, P. Carolan, J. Lin, R. Contreras-Guerrero, R. Droopad, P. K. Hurley, and I. G. Thayne, “Electrical and physical characterization of the $\text{Al}_2\text{O}_3/p\text{-GaSb}$ interface for 1%, 5%, 10%,

- and 22%(NH₄)₂S surface treatments,” *Applied Physics Letters*, vol. 105, no. 16, p. 162907, 2014.
- [11] J. Lin, Y. Y. Gomeniuk, S. Monaghan, I. M. Povey, K. Cherkaoui, É. O’Connor, M. Power, and P. K. Hurley, “An investigation of capacitance-voltage hysteresis in metal/high-k/In_{0.53}Ga_{0.47}As metal-oxide-semiconductor capacitors,” *Journal of Applied Physics*, vol. 114, no. 14, p. 144105, 2013.
- [12] V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O’Connor, I. M. Povey, D. O’Connell, M. E. Pemble, and P. K. Hurley, “Impact of forming gas annealing on the performance of surface-channel In_{0.53}Ga_{0.47}As MOSFETs with an ALD Al₂O₃ gate dielectric,” *IEEE transactions on electron devices*, vol. 59, no. 4, p. 1084, 2012.
- [13] W. Lu, I. Roh, D.-M. Geum, S.-H. Kim, J. Song, L. Kong, and J. A. del Alamo, “10-nm fin-width InGaSb *p*-channel self-aligned FinFETs using antimonide-compatible digital etch,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, pp. 17–7, IEEE, 2017.
- [14] K.-H. Goh, K.-H. Tan, S. Yadav, S.-F. Yoon, G. Liang, X. Gong, Y.-C. Yeo, *et al.*, “Gate-all-around CMOS (InAs *n*-FET and GaSb *p*-FET) based on vertically-stacked nanowires on a Si platform, enabled by extremely-thin buffer layer technology and common gate stack and contact modules,” in *2015 IEEE International Electron Devices Meeting (IEDM)*, pp. 15–4, IEEE, 2015.

- [15] R. Chu, T. Chiang, W. Hsueh, K. Chen, K. Lin, G. Brown, J. Chyi, J. Kwo, and M. Hong, “Passivation of GaSb using molecular beam epitaxy Y_2O_3 to achieve low interfacial trap density and high-performance self-aligned inversion-channel p -metal-oxide-semiconductor field-effect-transistors,” *Applied Physics Letters*, vol. 105, no. 18, p. 182106, 2014.
- [16] J. Nah, H. Fang, C. Wang, K. Takei, M. H. Lee, E. Plis, S. Krishna, and A. Javey, “III–V complementary metal–oxide–semiconductor electronics on silicon substrates,” *Nano letters*, vol. 12, no. 7, pp. 3592–3595, 2012.
- [17] M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, “III–V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on Si,” in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*, pp. 1–2, IEEE, 2014.

Chapter 6

Conclusions and Future Work

6.1 Outlook and Future Work

This thesis has reported on polycrystalline and amorphous III-V materials grown at 475°C. This thermal budget constraint is necessary if materials are to be implemented in the back-end-of-line (BEOL) above previously formed logic and memory devices. Room temperature mobilities are competitive compared to materials in the literature grown at similar temperatures, and generally exceed those of similar thicknesses and those grown on amorphous silicon substrates. Successfully demonstrating films with impressive electron and hole mobilities and functional devices made from these materials while operating within the restrictions imposed by the intended future use in 3D integrated Integrated Circuit (IC)s, comprises an important step towards achieving this goal. To this point, many of the impressive results from III-V

materials were from those not grown on silicon substrates.

An *n*-type polycrystalline InAs material has been demonstrated, with room temperature mobilities of approximately $100\text{cm}^2/\text{Vs}$ and $155\text{cm}^2/\text{Vs}$ for a heterostructure containing InAs. The mechanism limiting the mobility in these films was investigated through temperature dependent Hall effect measurements. It was found that the mobility did not have a strong dependence on temperature and so was concluded to be limited by surface roughness.

Functional *n*-type junctionless transistors were fabricated using the InAs films as the channel material. The devices were characterised electrically and the results were analysed. $I_{\text{ON}}/I_{\text{OFF}}$ values of up to 363 were achieved at room temperature and up to 1.3×10^4 at -50°C . Temperature dependent measurements were utilised to investigate the limiting factor for the $I_{\text{ON}}/I_{\text{OFF}}$ ratio. Through this analysis, it was found that incomplete depletion of the device was limiting the final ratio. For this reason, it can be concluded that thinner films are preferable for device applications.

Polycrystalline GaSb films were fabricated with room temperature hole mobilities reaching $66\text{cm}^2/\text{Vs}$ for a film on SiO_2 and up to $299\text{cm}^2/\text{Vs}$ for a film on crystalline Semi-Insulating (SI) GaAs. An amorphous GaSb film was also studied as part of a heterostructure. This amorphous film achieved a room temperature hole mobility of $9.1\text{cm}^2/\text{Vs}$. The amorphous film also

showed improved continuity and smoothness compared to the polycrystalline GaSb films of comparative thickness studied in the same chapter. Reduced roughness and improved continuity are attributes beneficial to device implementation. The hole mobilities achieved with these films exceed many of those found in the literature, and are a particularly important result due to development of *p*-type materials generally lagging that of *n*-type.

Device processing of *p*-type of junctionless transistor devices with varying thicknesses polycrystalline GaSb on SiO₂ as the channel material was developed and performed. Electrical characterisation was carried out at different stages of the device processing to gain understanding of the effects on the material. This produced functional devices with I_{ON}/I_{OFF} ratios of up to 205 at room temperature and 550 at -50°C. From the results of this research, recommendations can be made for future improvements of devices which utilise poly and amorphous GaSb as their channel material.

One path to explore would be the growth of films to a thickness which exceeds the critical thickness needed to achieve continuity, with a subsequent Chemical Mechanical Polishing (CMP) step to remove the nanowire like growth seen for the 250nm GaSb film in Figure 4.1. This process could also be useful for the InAs films, which experience a similar problem of a relatively thick critical thickness for onset of continuity if grown directly on the substrate. The difficulty with this process is of course the design of a suitable recipe

for each material, along with the control and resolution necessary to achieve nanometre precision. The bulk of the literature deals with removing microns of material as quickly as possible, which is unsuitable for this application.

For the device design and fabrication, there were not many duplicate samples of thin films. This made it difficult to perform systematic studies of certain steps of the fabrication without consuming the entirety of the sample in the process. For this reason, past literature and studies were depended on heavily. In the future, it would be wise to perform some systematic studies of these processes on polycrystalline and amorphous III-V films to truly optimise the fabrication process.

Finally, it is noted that the materials presented in this thesis show considerable promise for use as high mobility, low temperature grown semiconductors for use in BEOL applications. High mobilities are shown for samples grown on amorphous substrates, which is important for future integration with silicon electronics. It has also been demonstrated that these semiconductors can be used as channel materials in functional junctionless transistor devices, achieving good ON-current values. With further systematic studies as mentioned above, it should be possible to achieve impressive OFF-current and I_{ON}/I_{OFF} values as well. Both an n - and p -type option have been demonstrated in this thesis, which is an important consideration due to the need for both types in Complementary Metal Oxide Semiconductor (CMOS) ar-

chitectures.

Appendix A

Hall Effect Measurement method

This Appendix describes in detail the way by which the Lakeshore AC/DC Hall Effect Measurement System measures and calculates the material properties such as resistivity, carrier concentration, and carrier mobility which are presented in this thesis.

Figure A.1 shows a picture of the Hall Effect Measurement System used for this thesis. The sample is inserted vertically on a sample holder between the two magnetic poles to the left and right.

The Hall Effect measurement can be generally split into two separate measurements:

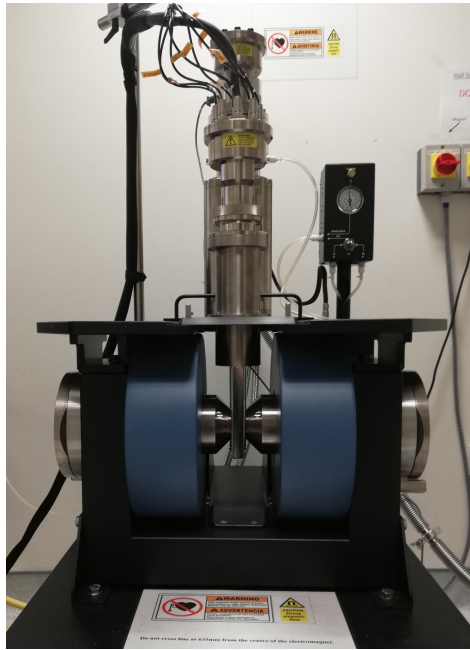


Figure A.1: Picture of the Hall Effect Measurement System.

1. A 2-point resistivity measurement
2. The Hall Effect measurement itself

The resistivity and the carrier concentration of the film are measured directly (using the film thickness manually inputted by the user), while the carrier mobility is calculated using these two figures along with the input film thickness and measured Hall voltage.

For both stages of the measurement, the current which is to be forced through the film must be chosen by the user. This is an important consideration as a high enough current is needed to result in separation of the charges. An “ac-

ceptable” Hall voltage for this apparatus is usually considered to be above 20×10^{-6} V. The Hall voltage is related to the chosen current through the following equation:

$$V_H = \frac{I \cdot B}{t \cdot n \cdot q} \quad (\text{A.0.1})$$

where I is the current chosen by the user, B is the magnetic field which is constant (the actual value depends on the type of measurement being performed), t is the film thickness, n is the carrier concentration, and q is the charge of an electron.

Though a sufficiently high current must be used, it is important not to pick a current which is too high, as this will lead to too high a lead voltage or punching through the oxide and coupling to the substrate (in the case where a conductive substrate is used). This effect was observed in a sample grown on Si/SiO₂, with the results shown in Figure A.2. As the thickness is manually inputted, it is clear where the software begins calculating for a film which is a few orders of magnitude thicker than the value used in the calculations, and the sheet values become similar to those of the substrate. These results are compared to the Hall Effect measurement results for a piece of the substrate which had its oxide etched and was measured directly.

The resistivity measurement is the first which is performed on the sample. This involves placing four contacts onto the corners of the sample, which

Applied Current	1 μ A	10mA	50mA	100mA	Tyndall Substrate Test
Hall mobility (cm ² /Vs)	24.2	27.75	33.83	32.6	39.4
Carrier Type	P	P	P	P	P
Carrier conc (1/cm ³)	1.98E16	6.82E23	5.65E23	5.89E23	4.62E19
Sheet carrier conc (1/cm ²)	9.92E10	3.41E18	2.83E18	2.94E18	2.42E18
Resistivity (Ω .cm)	12.99	3.3E-7	3.26E-7	3.25E-7	3.44E-3
Sheet resistivity (Ω /sq)	2.6E6	6.6E-2	6.52E-2	6.5E-2	6.52E-2

Figure A.2: Varying applied current for GaSb film on SiO₂ displaying a breakdown of the oxide and coupling to the substrate at higher applied currents. Direct measurement of the substrate is included for comparison.

should be cut to be as square as possible. The resistivity measurement is performed by forcing the current through two of the contacts which are next to each other, and measuring the resultant voltage between the two contacts opposite. This is performed around the edges of the sample until an average value can be reached. This stage not only includes a resistivity result, but also generates an F-value, a measurement of the uniformity/symmetry of the sample. Ideally, this value should be unity, however often it is not, and if it is below a certain value (0.95), the measurement will be considered relatively inaccurate by the software. This is because a Hall effect measurement in this measurement configuration, the van der Pauw configuration, makes a number of assumptions, including uniformity of the sample.

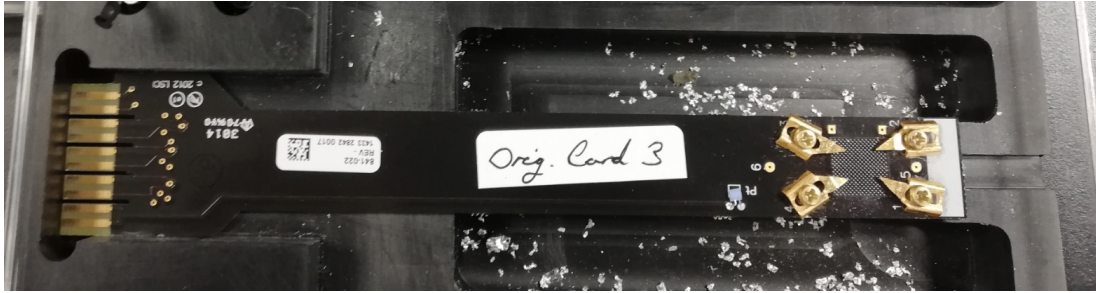


Figure A.3: Picture of sample holder for room temperature insert in the Hall Measurement System.

Figure A.3 shows a picture the room temperature insert holder in which the square sample is placed and held, with the four corner contact numbers labelled in the photo. The four pins contact the sample and hold it in place for when the card is placed vertically into the system.

Figure A.4 shows a sample of the results pdf generated by the system when doing the resistivity measurement. The numbers under the geometry indicate how the measurement is performed. The first two indicate the contacts between which the current is being forced and the second two indicate the contacts between which the voltage is being measured. Each geometry is averaged, with an average resistivity figure and an F value being calculated for Geometry A and Geometry B. The agreement between these final figures determines whether the resistivity measurement is deemed “acceptable” by the software. The F value is calculated automatically by the software and is a transcendental function of the two measured resistances.

Average measurements (I+)		Geometry A		Geometry B	
		R2134	R3241	R4312	R1423
	Voltage [V]	1.43925E-2	1.77621E-2	1.44626E-2	1.78448E-2
	Standard deviation of voltage [V]	3.17197E-6	3.08974E-6	2.30162E-6	2.67101E-6
	Current [A]	1.00012E-5	1.00012E-5	1.00012E-5	1.00012E-5
	Standard deviation of current [A]	1.06861E-10	1.45370E-10	1.65315E-10	1.58771E-10
	Current lead voltage [DC V]	1.91470E-1	1.82033E-1	2.02231E-1	2.18948E-1

Average measurements (I-)		Geometry A		Geometry B	
		R2134	R3241	R4312	R1423
	Voltage [V]	-1.44495E-2	-1.78033E-2	-1.44726E-2	-1.78255E-2
	Standard deviation of voltage [V]	1.82254E-6	2.23825E-6	1.97871E-6	2.48050E-6
	Current [A]	-1.00006E-5	-1.00006E-5	-1.00006E-5	-1.00006E-5
	Standard deviation of current [A]	1.76827E-10	1.52363E-10	1.24769E-10	1.50508E-10
	Current lead voltage [DC V]	-1.91605E-1	-1.82205E-1	-2.02413E-1	-2.19030E-1

Figure A.4: Example of results table generated during resistivity measurements.

The resistivity data alone can give an interesting insight into the properties of a film, as it essentially a measurement of the conductivity. The conductivity was used to determine that variable range hopping was the factor limiting the hole mobility in the amorphous GaSb film described in Section 4.4.2. However, to separate the components of the conductivity, the carrier concentration and mobility, and to determine the majority carrier type, a Hall Effect measurement must be made.

A Hall Effect measurement involves, once again, a current chosen by the user being forced through the film; however, this time a magnetic field is also applied to the sample, perpendicular to the electrical current. This causes a separation of the charges in the plane perpendicular to both the current and the magnetic field. The direction of the resulting voltage indicates the ma-

majority charge carrier type i.e., a negative voltage for electrons and a positive voltage for holes. The carrier concentration is determined directly from the Hall Voltage through the equation shown in A.0.1. This information combined with the resistivity results can then be used to determine the carrier mobility, as the conductivity is the inverse of the resistivity.

Where temperature dependent Hall Effect results are desired, a different sample insert is required, called the Closed Cycle Refrigerator (CCR) insert. This insert requires the magnetic poles to be further apart, lowering the maximum field possible, which must be taken into account when setting the current level, as it may need to compensate for the lower magnetic field in achieving an acceptable Hall Voltage. This insert is attached to a pump and a compressor which allow the temperature to be controlled in a range of 10-400 K. The temperature setting is controlled through the software. A different sample holder is used, pictured in Figure A.5, where the contacts must be wire bonded to the sample.

When there are difficulties in measuring a sample, for example, a sample whose resistivity is too high to force a reasonable current without creating an unreasonable lead voltage, an AC measurement may be performed. Here, the AC term refers to the magnetic field and in this mode a lower value must be used. Similar to the CCR measurements, this must be taken into account when picking a current, however, in an AC measurement, the sensitivity and

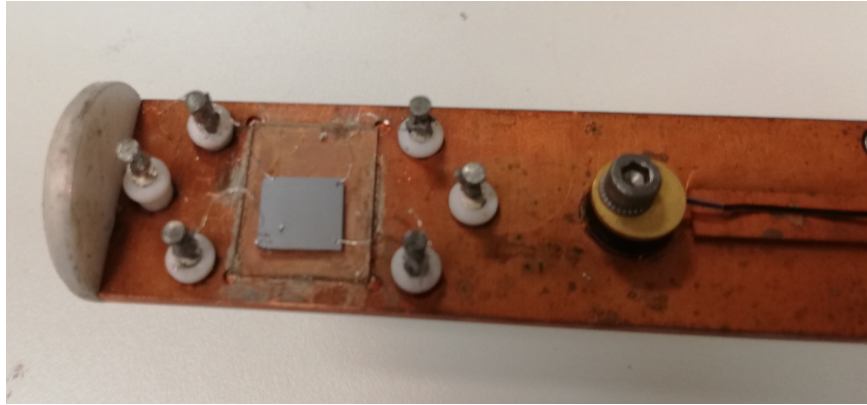


Figure A.5: Picture of sample holder for CCR insert in the Hall Measurement System.

the gain should also be considered. The AC method is a powerful tool for samples where the small values for the Hall Voltage are difficult to separate from the background noise. A lock-in amplifier is used to generate a sinusoidal magnetic field at a chosen frequency and then measure the amplitude and phase of the filtered AC signal. Here, filtered refers to the signal after interaction with the sample. These measurements are extremely useful, however require more time and optimization of the measurement parameters compared to the DC measurement.

Appendix B

Resistivity Extraction from circular Transmission Line Measurement (cTLM)

This Appendix describes in detail the way by which the cTLMs in this thesis were analysed to find the resistivity of the films studied.

The layout of the cTLM structures is shown in Figure B.1a, where the blue area is a metal contact and the white is the semiconducting film. The data shown in this Appendix is for a GaSb film, however the same method is used for the InAs films. A representative cTLM IV measurement is shown in Figure B.1b, which shows the expected linear behaviour. Figure B.1c shows a representative plot of total resistance and total corrected resistance. The

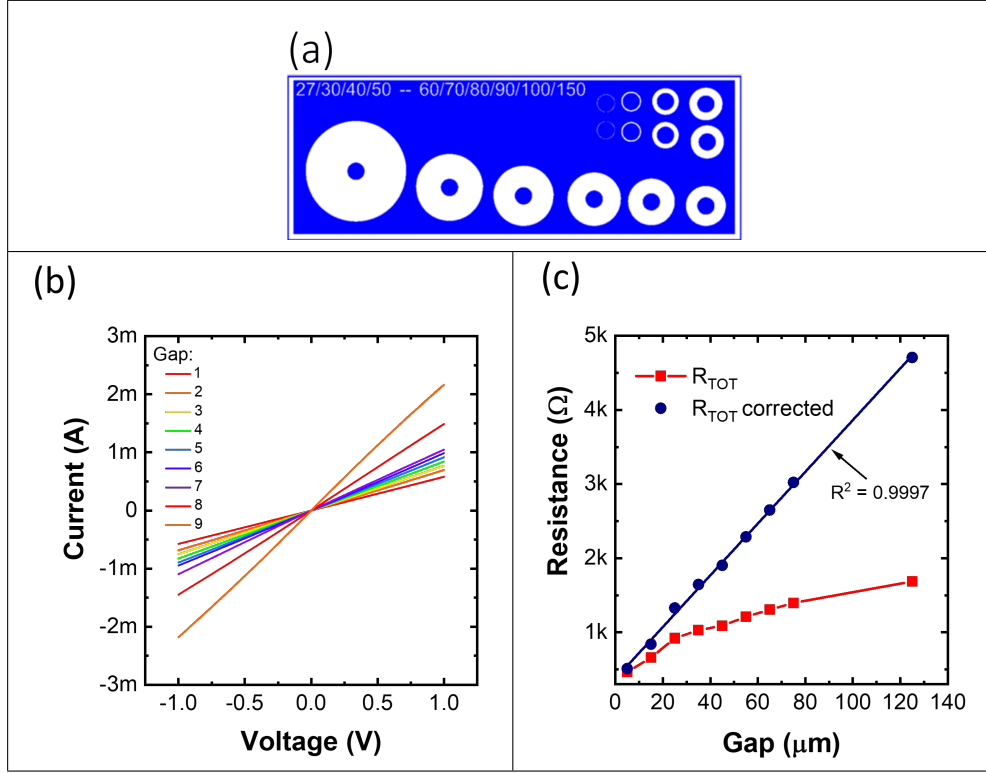


Figure B.1: (a) Schematic of cTLM structure layout. (b) Representative IV curve of cTLM structures at different gaps, and (c) representative R_{TOT} graphs before and after correction vs gap.

correction factor for cTLM results takes into account the circular geometry and spreading of the current as it travels across the gap between metal contacts, and is calculated using:

$$CorrectionFactor = \frac{inner - radius}{outer - radius} \cdot \ln \left(1 + \frac{outer - radius}{inner - radius} \right) \quad (B.0.1)$$

The corrected R_{TOT} data was used to calculate the specific contact resistivity and the sheet resistivity of the material itself. The sheet resistivity is calculated from the slope of the graph, while the contact resistance is taken from the y-axis intercept (where the gap between contacts would be zero) and divided by two. The contact resistivity is this value normalised to area. The transfer length can be calculated from the x-axis intercept.

Appendix C

InAs Buried Channel Devices

This Appendix describes an attempt at fabricating buried channel devices with an InAs channel.

Buried channel devices are a possible solution to many issues for III-V channel material devices (1). Firstly, specifically for the poly InAs films studied in Chapter 2, the mobility is surface roughness limited. This can be mitigated through the buried channel structure where the conducting layer is sandwiched between two wide bandgap layers. Here, the vertical boundaries of the conductive channel depend on a doping profile rather than the termination of the film itself. Secondly, for all III-Vs, the interface between the channel and the oxide results in roughness and interface states which can cause Coulomb scattering and remote phonon scattering, lowering the mobility in the channel (2).

This buried channel structure was achieved using Al incorporation into InAs to widen the bandgap. The growth of these films by Metalorganic Vapour Phase Epitaxy (MOVPE) was carried out by the Epitaxy and Physics of Nanostructures group in Tyndall. The level of Al in the InAs was graded from the highest level at the substrate, down to the lowest (0%) for the channel region, and back up to the highest level at the surface of the film. A similar film structure has been demonstrated in the literature and shown to produce functional devices (3-6). This previous work has an InGaAs channel, with layers of InAlAs either side. These structures are also formed on a III-V substrate, InP. Here, we try to fabricate a similar structure, where the substrate is silicon and the channel is InAs. A schematic representation of the film and device structure fabricated is shown in Figure C.1, where the percentages represent the percentage of Al present in a sample with a nominal maximum Al value of 50%.

X-ray Photoelectron Spectroscopy (XPS) was performed, and the results analysed, in University of Limerick. XPS was used to estimate the actual concentration of Al present at the surface of the films. A 60° tilt measurement was also performed, which allows determination of change in concentration when sampling depth is decreased i.e., when the measurement is more surface dominated. There was a considerable amount of organics detected by XPS on the surface of the samples. This is likely due to exposure to air and

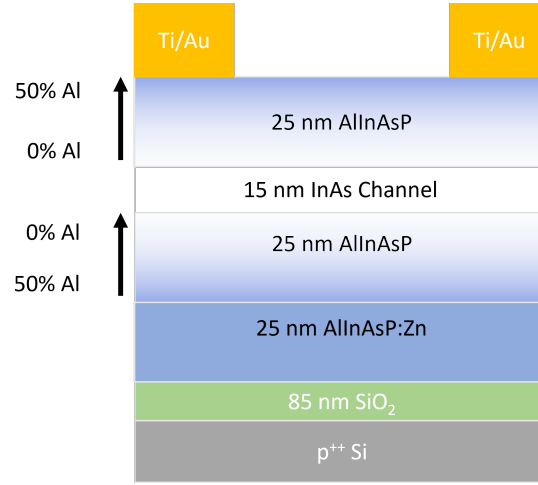


Figure C.1: Schematic of a buried channel and device structure.

related contamination. The organics are clearly present on the surface, as the associated concentration increased 2-4x between the non tilted measurement and the 60° tilted measurement. The species detected include C-C, C-O, and O-C=O. The other elements (with contribution from organics removed) are adjusted for lattice position (these dopant atoms are expected to replace As in the crystal lattice), and the results of this analysis are shown in Table C.1. It is clear from the results that the actual concentration of incorporated Al differs greatly from the nominal values, and surprisingly only shows a higher concentration at the surface of the film grown at lower temperature. This is unexpected, as the gradation is designed such that the surface should display the highest level of Al incorporation i.e., the entirety of the nominal value of either 30% or 50% should be present at the surface exposed to air as well as the surface at the interface between the substrate and the film. As the Al is incorporated to increase the bandgap around the channel, this lower level of

incorporation could compromise the intended function of the structure.

Sample Description	Element	No Tilt - % Conc	60° Tilt - % Conc
50% AlInAsP:Zn - 475°C	In	100	100
	As	80.8	87.63
	Al	13.4	8.74
	Zn	5.7	3.63
30% AlInAsP:Zn - 475°C	In	100	100
	As	83	86.67
	Al	11.5	9.69
	Zn	5.5	3.44
50% AlInAsP:Zn - 455°C	In	100	100
	As	83.8	79.02
	Al	9.6	16.76
	Zn	6.7	4.23

Table C.1: XPS results of Al containing InAs films at no tilt and 60° tilt

Back-gated device results from these samples are shown in Figure C.2. All of these samples have a nominal channel thickness (where there is no Al doping present) of 15 nm. It is clear from the hystereses present in the transfer characteristics that there is a large amount of charge trapping in the devices. The sample with nominally 50% Al grown at 455°C shows the best I_{ON}/I_{OFF} ratio at 26. This sample also showed the greatest level of Al incorporation towards the surface of the film when tested by XPS. However, none of these devices showed greater I_{ON}/I_{OFF} or improvements in drive current or subthreshold slope when compared to the devices without a buried channel structure (e.g., device shown in Figure 3.2). As the doping is graded, it is reasonable to assume that the levels measured at the surface using XPS represent the highest levels present in the structure. If this is the case, the actual thickness of the

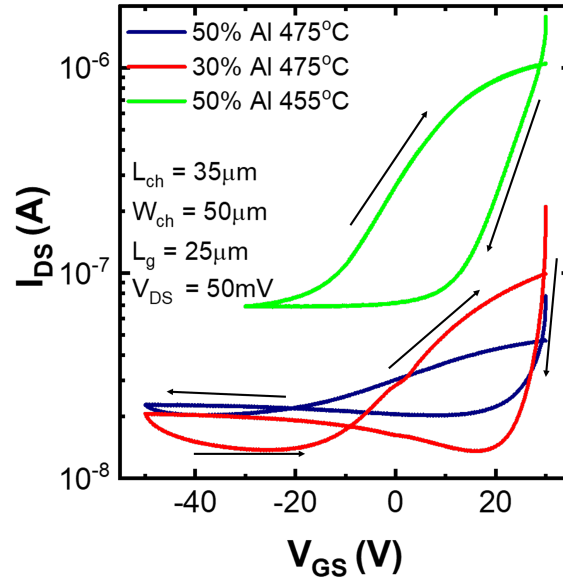


Figure C.2: Transfer characteristics of AlInAs/InAs/AlInAs buried channel devices.

effective channel could be more than intended. This could cause the issue of not being able to fully deplete the entire thickness of the conductive channel, as seen with the non-buried channel devices previously studied. Other possibilities include the AlInAs layers being too thick to gate through effectively and unintentional doping in the AlInAs layers.

To improve the functionality of the buried channel devices the incorporation of Al into the doped regions must be increased. This means a method of more accurately controlling Al incorporation in the films during growth must be achieved, and it is possible that the graded structure is not the optimal way to achieve a buried channel. Removal of the initial 25 nm AlInAs layer

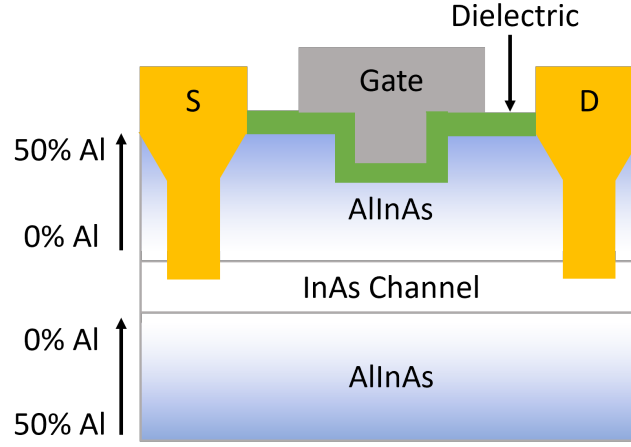


Figure C.3: Schematic of a buried channel structure device adapted from the literature (6).

grown prior the gradation would also help to achieve more effective back-gating through the substrate. Top-gated devices could also be fabricated as the back-gating through the substrate has to gate through the 85 nm SiO_2 and the wider band-gap AlInAs layer below the conductive channel. It would also be advisable to try additional improvements to the device structure, such as partially etching the wider bandgap layers to allow source and drain metal contacting directly to the conducting channel and fabricating a partially recessed metal gate contact. Such a device structure is shown in Figure C.3. The schematic has been adapted from the literature (6) where a similar device architecture has been fabricated.

(1) H. Shang, M. M. Frank, E. P. Gusev, J. O. Chu, S. W. Bedell, K. W. Guarini, and M. Jeong, “Germanium channel MOSFETs: Opportunities and

Challenges,” *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 377-386, 2006.

(2) S.-H. Kim, M. Yokoyama, R. Nakane, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi, “High Performance Tri-Gate Extremely Thin-Body InAs-On-Insulator MOSFETs with High Short Channel Effect Immunity and V_{th} Tunability,” *IEEE Transactions on Electron Devices*, vol. 61, no. 5, pp. 1354-1360, 2014.

(3) F. Xue, H. Zhao, Y.-T. Chen, Y. Wang, F. Zhou, and J. C. Lee, “InAs inserted InGaAs buried channel metal-oxide-semiconductor field-effect-transistors with atomic-layer-deposited gate dielectric,” *Applied Physics Letters*, vol. 98, no. 8, p. 082106, 2011.

(4) S. J. Bentley, M. Holland, X. Li, G. W. Paterson, H. Zhou, and O. Ignatova, “Electron Mobility in Surface-and-Buried-Channel Flatband $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs With ALD Al_2O_3 Gate Dielectric,” *IEEE Electron Device Letters*, vol. 32, no. 4, pp. 494-496, 2011.

(5) Y. Sun, E. W. Kiewra, J. P. De Souza, J. J. Bucchignano, K. E. Fogel, D. K. Sadana, and G. G. Shahidi, “Scaling of $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ buried-channel MOSFETs,” *2008 IEEE International Electron Devices Meeting*, pp. 1-4, IEEE, 2008.

- (6) Y. Sun, E. W. Kiewra, S. J. Koester, N. Ruiz, A. Callegari, K. E. Fogel, D. K. Sadana, J. Fompeyrine, D. J. Webb, J.-P. Locquet, *et. al.*, “Enhancement-mode buried-channel $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ MOSFETs with high- κ gate dielectrics,” *IEEE electron device letters*, vol. 28, no. 6, pp. 473-475, 2007.