CORA Cork Open Research Archive
Cartlann Taighde Oscailte Chorcaí

Title	Improvement in top-gate MoS2 transistor performance due to high quality backside Al2O3 layer
Authors	Bolshakov, Pavel;Zhao, Peng;Azcatl, Angelica;Hurley, Paul K.;Wallace, Robert M.;Young, Chadwin D.
Publication date	2017-07-21
Original Citation	Bolshakov, P., Zhao, P., Azcatl, A., Hurley, P. K., Wallace, R. M. and Young, C. D. (2017) 'Improvement in top-gate MoS2 transistor performance due to high quality backside Al2O3 layer', Applied Physics Letters, 111(3), pp. 032110. doi:10.1063/1.4995242
Type of publication	Article (peer-reviewed)
Link to publisher's version	10.1063/1.4995242
Rights	© 2017, AIP Publishing. This article may be downloaded for personal use only. Any other use requires prior permission of the author and AIP Publishing. The following article appeared in Appl. Phys. Lett. 111, 032110 (2017) and may be found at http://aip.scitation.org/doi/pdf/10.1063/1.4995242
Download date	2026-11-04 07:13:41
Item downloaded from	https://hdl.handle.net/10468/4278

UCC
University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

Improvement in top-gate MoS_2 transistor performance due to high quality backside Al_2O_3 layer

Pavel Bolshakov, Peng Zhao, Angelica Azcatl, Paul K. Hurley, Robert M. Wallace, and Chadwin D. Young

Citation: Appl. Phys. Lett. **111**, 032110 (2017); doi: 10.1063/1.4995242
View online: http://dx.doi.org/10.1063/1.4995242
View Table of Contents: http://aip.scitation.org/toc/apl/111/3
Published by the American Institute of Physics

Articles you may be interested in

Enhanced radiative emission from monolayer MoS_2 films using a single plasmonic dimer nanoantenna
Applied Physics Letters **111**, 031101 (2017); 10.1063/1.4993427

As-grown two-dimensional MoS_2 based photodetectors with naturally formed contacts
Applied Physics Letters **110**, 261109 (2017); 10.1063/1.4990968

Strong dopant dependence of electric transport in ion-gated MoS_2
Applied Physics Letters **111**, 013106 (2017); 10.1063/1.4992477

Annealing, temperature, and bias-induced threshold voltage instabilities in integrated E/D-mode InAlN/GaN MOS HEMTs
Applied Physics Letters **111**, 033506 (2017); 10.1063/1.4995235

High free carrier concentration in p-GaN grown on AlN substrates
Applied Physics Letters **111**, 032109 (2017); 10.1063/1.4995239

Chemical vapor deposition of monolayer MoS_2 directly on ultrathin Al_2O_3 for low-power electronics
Applied Physics Letters **110**, 053101 (2017); 10.1063/1.4975064



Improvement in top-gate MoS_2 transistor performance due to high quality backside Al_2O_3 layer

Pavel Bolshakov,[1] Peng Zhao,[1] Angelica Azcatl,[1] Paul K. Hurley,[2] Robert M. Wallace,[1] and Chadwin D. Young[1]
[1]*Department of Materials Science and Engineering, The University of Texas at Dallas, 800 West Campbell Road, Richardson, Texas 75080, USA*
[2]*Tyndall National Institute, University College Cork, Lee Maltings Complex, Dyke Parade, Mardyke, Cork, Ireland*

(Received 24 February 2017; accepted 8 July 2017; published online 21 July 2017)

A high quality Al_2O_3 layer is developed to achieve high performance in top-gate MoS_2 transistors. Compared with top-gate MoS_2 field effect transistors on a SiO_2 layer, the intrinsic mobility and subthreshold slope were greatly improved in high-k backside layer devices. A forming gas anneal is found to enhance device performance due to a reduction in the charge trap density of the backside dielectric. The major improvements in device performance are ascribed to the forming gas anneal and the high-k dielectric screening effect of the backside Al_2O_3 layer. Top-gate devices built upon these stacks exhibit a near-ideal subthreshold slope of ~69 mV/dec and a high Y-Function extracted intrinsic carrier mobility (μ_o) of 145 $cm^2/V{\cdot}s$, indicating a positive influence on top-gate device performance even without any backside bias. *Published by AIP Publishing.*
[http://dx.doi.org/10.1063/1.4995242]

Transition metal dichalcogenides (TMDs) are at the forefront of research as possible semiconductor channels in low-power, high-mobility devices.[1–4] Molybdenum disulfide (MoS_2), one of the most studied TMDs, is an attractive 2D material with a thickness dependent band gap that has shown high device performance in a traditional top-gate field effect transistor (FET) structure.[5–7] Previous studies have shown high on/off ratios (~10^8), high mobility values (>200 cm^2/Vs), and low subthreshold swing (~74 mV/dec) for top-gate MoS_2 devices, typically on SiO_2.[8] The utilization of SiO_2 is often due to exfoliated MoS_2 having a high optical contrast on SiO_2 dielectric, allowing for quicker and easier detection of flakes. Recent studies have demonstrated the effects of high-k dielectrics on back-gated transistors with improvements in device performance attributed to the dielectric screening effect.[9–11] However, a dearth of quality capacitance data to ensure a high-quality dielectric has been reported, which oftentimes can result in extraction of improper mobility values due to a high capacitance. Some studies also prefer a dual gate structure, while others have suggested that there is an advantage to sweeping only the back gate due to improper assumptions about top gate capacitance, which has stirred much debate.[12–14] The top gate capacitance is generally assumed to be between the active device channel and the gate over channel area, resulting in appropriate mobility extraction. This study demonstrates the effect of a high quality annealed Al_2O_3 backside layer for top gate transistors where the I_{ON}/I_{OFF} ratio is ~10^6, the field effect mobility is ~33 cm^2/Vs, and the subthreshold slope (SS) is ~69 mV/dec, without any back gate bias.

Al_2O_3 (~15 nm) dielectric films were deposited on p-Si wafers by atomic layer deposition (ALD). Metal-oxide-semiconductor capacitors (Metal-Al_2O_3-Si) were fabricated to provide a proper understanding of the quality of these films. By photolithography, top electrodes (Cr/Au, 20/150 nm) with various areas were fabricated with a lift-off process. A forming gas ("FG":5%H_2/95%N_2) anneal at 400 °C at 1 bar was performed to establish the anneal impact on interface traps,[15] and Al (150 nm) was deposited on the back of the wafer to reduce the series resistance. For the MoS_2 field effect transistors (FETs), scotch tape was used to mechanically exfoliate untreated MoS_2 on top of Al_2O_3. By photolithography, the source/drain was defined on a few layer MoS_2 flake, and then, Cr/Au (20 nm/150 nm) was deposited by thermal evaporation under high-vacuum (10^{-6} mbar), followed by a lift-off process. This back-gate device was then FG annealed with pre- and post-anneal I-V measurements. After the post-anneal measurements, 15 min of *in-situ* UV-ozone functionalization treatment was performed, and then, 4 nm of HfO_2 was deposited at 200 °C using an ALD tetrakis-ethylmethylamino hafnium (TEMA-Hf)/H_2O process.[16] The combination of the FG anneal and the UV/O_3 functionalization of the MoS_2 surface is anticipated to reduce residual, process-induced contamination from lithography prior to gate dielectric formation.[16–18] The final step involved the high-vacuum deposition of a Cr/Au top gate using the same process as the source/drain, converting the back-gate device into a top-gate 3-terminal FET. The same fabrication flow was used on devices with a SiO_2 backside layer for proper device comparison.

From frequency dependent C-V measurements of Al_2O_3 MOSCAPs [Figs. 1(a) and 1(b)] ranging from 500 Hz to 1 MHz, we were able to determine the optimum annealing temperature to achieve low frequency dispersion in the depletion region, typically attributed to interface traps (Q_{it}), and in the accumulation region, typically attributed to the series resistance (R_s), with the former being the most impacted by the FG annealing. First, FG anneals at 200 °C, 300 °C, and 400 °C were performed with C-V measurements done after each anneal. Interface trap density (D_{it}) extraction [Fig. 1(c)] using the High-Low Frequency method (see

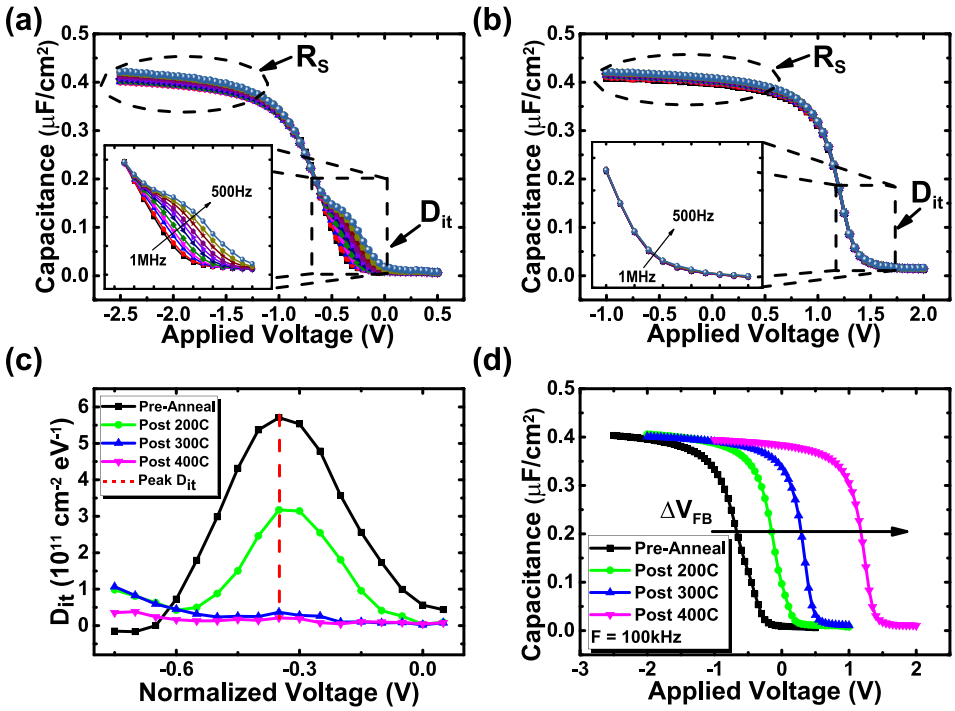


FIG. 1. (a) Frequency dependent C-V before annealing with evidence of high dispersion and (b) frequency dependent C-V post 400 °C FG anneal with a significant reduction in dispersion. (c) High-low frequency interface trap density (D_{it}) extraction for a range of subsequent anneal temperatures and (d) the flat-band voltage shift accompanying each subsequent anneal.

supplementary material),[19] a technique well suited for MOS capacitors, shows a significant reduction from the peak D_{it} of 5.7×10^{11} cm^{-2} eV^{-1} of pre-annealed Al_2O_3 to an extremely low D_{it} of 2×10^{10} $cm^{-2}eV^{-1}$ post 400 °C anneal. The flat-band voltage shift (ΔV_{FB}), typically attributed to a reduction of fixed oxide charges (Q_f), post anneal [Fig. 1(d)] was another indicator of optimal annealing temperature as any subsequent anneals after 400 °C did not yield any further shift. While some recent publications claim to have good dielectric properties, the associated C-V data indicate high frequency dispersion[11] and/or D_{it} extraction using widely critiqued methods.[20,21] These discrepancies can lead to improper extraction of device parameters and especially an overestimation of field effect mobility.

With a high quality Al_2O_3 backside dielectric layer, back-gate devices with an MoS_2 channel can be used to demonstrate the effect of the FG anneal in terms of device performance. Several back-gate FETs were thus fabricated on a high-k backside layer in order to study the effect of the FG anneal. While the MoS_2 flakes were untreated and therefore had sulfur vacancies, among other likely defects and impurities,[22,23] the thickness of each flake was ~4–5 nm, approximated using the optical interference contrast method, in order to keep the variability low. The I-V characteristics of the devices were measured pre- and post-anneal at 400 °C, with the statistics (8 back-gate FETs) of the I_{ON}/I_{OFF} ratio and SS_{MIN} shown in Fig. 2(a). A favorable trend is shown with an increase in I_{ON}/I_{OFF} and a decrease in SS_{MIN} attributed to the beneficial effects of the anneal on the Al_2O_3 layer. With an average I_{ON}/I_{OFF} ratio of $\sim 10^3$ and SS_{MIN} of ~270 mV/dec pre-anneal, the devices' performance greatly improved with an average I_{ON}/I_{OFF} ratio of $\sim 10^6$ and SS_{MIN} of ~117 mV/dec post-anneal. This increase in performance can be attributed to not only passivation but also a potential reduction in impurities at the backside MoS_2/Al_2O_3 interface. In Fig. 2(b), I_D-V_D indicates a non-linear behavior pre-anneal and more linear behavior post-anneal, suggesting that annealing also has a beneficial effect on the contacts, not just the dielectric, potentially removing the need for sulfur passivation treatments.[24–26] It is noted that with back-gate devices, proper C_{OX} extraction from C-V measurements is nearly impossible due to the high capacitance resulting from the

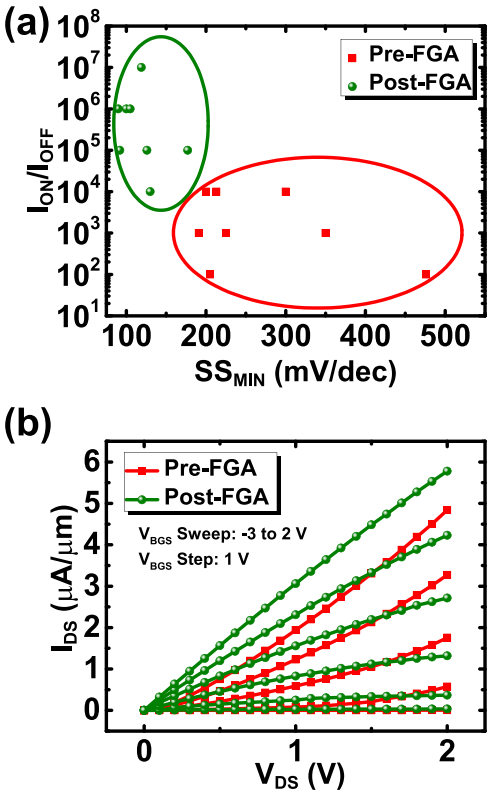


FIG. 2. (a) Statistics of back-gated FETs pre- and post-FG anneal in terms I_{ON}/I_{OFF} and SS_{min}, demonstrating a beneficial trend in device performance as a result of an effect of the anneal on the high-k backside layer for a total of 8 devices. (b) I_D-V_D pre-FG anneal and post-FG anneal shows a beneficial effect on the contacts with a conversion from non-linear to linear curves.

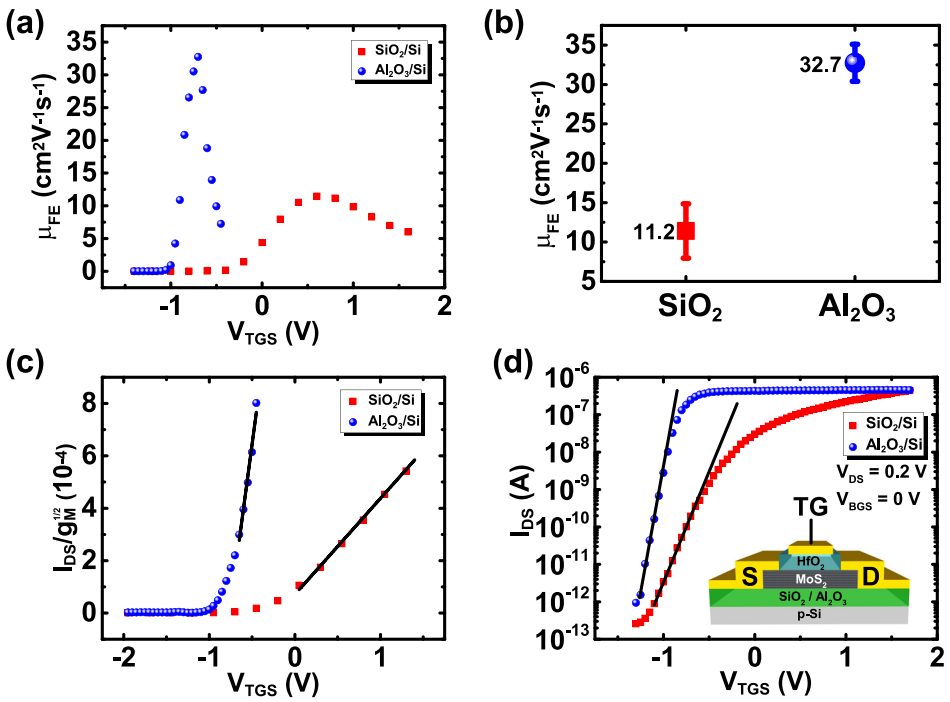


FIG. 3. (a) Field effect mobility comparison between a top-gate FET on a pre-annealed Al_2O_3 layer and an SiO_2 layer with the (b) mobility statistics for the 4 best top-gate FET devices for each Al_2O_3 and SiO_2 backside layer. (c) Y-Function extraction for top-gate devices on Al_2O_3 and SiO_2 with (d) I_{DS}-V_{TGS} characteristics of devices on Al_2O_3 and SiO_2, demonstrating an increase in mobility and a decrease in SS due to a high-k backside layer with the inset showing a cross-section of a top-gate structure.

large area of the source/drain pads that dwarf the MoS_2 gate channel capacitance, nor would it be appropriate to extract D_{it} using the subthreshold slope expression due to the uncertainty in C_{OX} and C_{bulk}.[19,27] With parameters such as the field effect mobility (μ_{FE}) reliant on C_{OX} for proper extraction, the proper device evaluation of the back-gate FET is limited, especially since its applicability to current CMOS technology is essentially non-existent. In order to properly compare the effect of the Al_2O_3 backside layer on device performance, a top-gate FET structure is needed.

Conversion from a back-gate to a top-gate device structure allows continuous evaluation of the same MoS_2 channel,[28] especially if it demonstrates high device performance as a back-gate device. With the backside dielectric layer already exposed to a 400 °C FG anneal, a top-gate HfO_2 dielectric was deposited after the MoS_2 flake was treated using a UV-ozone functionalization treatment and a top-gate (Cr/Au) was deposited under high-vacuum thereafter. Top-gated devices on a SiO_2 layer went through the same process, and two comparable devices were chosen for characterization. In Fig. 3(a), the field effect mobility extraction (see supplementary material) for each top-gate device with a peak μ_{FE} of $\sim$11 $cm^2\ V^{-1}s^{-1}$ for the device on the SiO_2 layer and a peak μ_{FE} of $\sim$33 $cm^2V^{-1}s^{-1}$ for the device on the Al_2O_3 layer shows $\sim$3× improvement in mobility. Mobility statistics for several top-gate devices [(Fig. 3(b)] demonstrates a similar trend across multiple devices (4 for each backside layer). This indicates that even without any backside bias, the dielectric layer upon which the top-gate device rests has an effect on its overall performance.

In order to compensate for the contact resistance, the extraction of intrinsic carrier mobility, as well as the contact resistance and threshold voltage, using the Y-Function Method (see supplementary material) in Fig. 3(c) can be reliably used.[29,30] The extracted parameters of the contact resistance (R_C) for top-gate devices on SiO_2 and Al_2O_3 layers are $\sim$28 kΩ·μm and $\sim$24 kΩ·μm, respectively. This may account for the low drive current of both devices, suggesting that lowering R_C may be able to further enhance the device performance.[31] The intrinsic mobilities (μ_o) for the device with SiO_2 and Al_2O_3 layers are 38 $cm^2\ V^{-1}s^{-1}$ and 145 $cm^2\ V^{-1}s^{-1}$, respectively, which is 4× higher due to a high-k backside layer.[32] With the observation of the device performance enhancement, these results suggest that there is an advantage in using backside dielectrics for 2D materials other than the traditional SiO_2. The subthreshold slope (SS) also shows a major improvement with an SS_{MIN} of $\sim$154 mV/dec for a device on a SiO_2 layer and a near-ideal SS_{MIN} of $\sim$69 mV/dec, a record high, for a device on a high quality Al_2O_3 layer. This indicates that a good choice of a backside dielectric layer for top-gate MoS_2 FETs can provide high device performance without any backside bias. Further improvement depends on the quality of the MoS_2 flakes/channel, as a reduction in defects and impurities would also yield a better channel for a device.[33]

A highly robust Al_2O_3 back-gate layer for high-k top-gate MoS_2 FETs has substantially improved device performance. We were able to reduce the interface trap density through the use of a forming gas anneal and achieve a near-ideal subthreshold slope of $\sim$69 mV/dec, as well as a high intrinsic carrier mobility of $\sim$145 $cm^2\ V^{-1}s^{-1}$, which is $\sim$4× higher than its SiO_2 counterpart. The improved device performance can be attributed to the FG anneal of the MoS_2/Al_2O_3 interface and the resultant high-k dielectric screening effect. This study emphasizes the effects of the backside dielectric layer on top-gate device performance, a significant component which must to be thoroughly understood in order to apply TMDs to current CMOS technology.

See supplementary material for the methods used for the extraction of interface trap density (D_{it}), subthreshold slope, and field effect mobility (μ_{FE}) and the Y-Function method

for the extraction of intrinsic carrier mobility (μ_o) and contact resistance (R_C), as well as the top-gate device cross-section and top-view optical image.

This work was supported in part by the US/Ireland R&D Partnership (UNITE) under the NSF award ECCS-1407765 and the Center for Low Energy Systems Technology (LEAST), one of the six SRC STARnet Centers, sponsored by MARCO and DARPA.

[1]S. Das and J. Appenzeller, Appl. Phys. Lett. **103**, 103501 (2013).
[2]H. Y. Chang, S. Yang, J. Lee, L. Tao, W. S. Hwang, D. Jena, N. Lu, and D. Akinwande, ACS Nano **7**, 5446 (2013).
[3]H. Wang, L. Yu, Y. H. Lee, W. Fang, A. Hsu, P. Herring, M. Chin, M. Dubey, L. J. Li, J. Kong, and T. Palacios, in *Tech. Dig. - Int. Electron Devices Meet. IEDM* (2012), p. 4.6.1–4.6.4.
[4]L. Yu, D. El-Damak, S. Ha, X. Ling, Y. Lin, A. Zubair, Y. Zhang, Y.-H. Lee, J. Kong, A. Chandrakasan, and T. Palacios, in *2015 IEEE International Electron Devices Meeting* (IEEE, 2015), pp. 32.3.1–32.3.4.
[5]R. Kappera, D. Voiry, S. E. Yalcin, B. Branch, G. Gupta, A. D. Mohite, and M. Chhowalla, Nat. Mater. **13**, 1128 (2014).
[6]X. Zou, J. Wang, C.-H. Chiu, Y. Wu, X. Xiao, C. Jiang, W.-W. Wu, L. Mai, T. Chen, J. Li, J. C. Ho, and L. Liao, Adv. Mater. **26**, 6255 (2014).
[7]S. J. McDonnell and R. M. Wallace, Thin Solid Films **616**, 482 (2016).
[8]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nat. Nanotechnol. **6**, 147 (2011).
[9]T. Li, B. Wan, G. Du, B. Zhang, and Z. Zeng, AIP Adv. **5**, 57102 (2015).
[10]J. Kang, W. Liu, and K. Banerjee, Appl. Phys. Lett. **104**, 93106 (2014).
[11]K. L. Ganapathi, S. Bhattacharjee, S. Mohan, and N. Bhat, IEEE Electron Device Lett. **37**, 797 (2016).
[12]M. S. Fuhrer and J. Hone, Nat. Nanotechnol. **8**, 146 (2013).
[13]B. Radisavljevic and A. Kis, Nat. Nanotechnol. **8**, 147 (2013).
[14]H. Liu and P. D. Ye, IEEE Electron Device Lett. **33**, 546 (2012).
[15]P. Zhao, A. Azcatl, P. Bolshakov, J. Moon, C. L. Hinkle, P. K. Hurley, R. M. Wallace, and C. D. Young, J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom. **35**, 01A118 (2017).
[16]A. Azcatl, S. McDonnell, K. C. Santosh, X. Peng, H. Dong, X. Qin, R. Addou, G. I. Mordi, N. Lu, J. Kim, M. J. Kim, K. Cho, and R. M. Wallace, Appl. Phys. Lett. **104**, 111601 (2014).
[17]A. Azcatl, S. KC, X. Peng, N. Lu, S. McDonnell, X. Qin, F. de Dios, R. Addou, J. Kim, M. J. Kim, K. Cho, and R. M. Wallace, 2D Mater. **2**, 14004 (2015).
[18]S. McDonnell, B. Brennan, A. Azcatl, N. Lu, H. Dong, C. Buie, J. Kim, C. L. Hinkle, M. J. Kim, and R. M. Wallace, ACS Nano **7**, 10354 (2013).
[19]D. K. Schroder, *Semiconductor Material and Device Characterization* (IEEE Press, 2006).
[20]G. I. Zebrev, E. V. Melnik, and D. K. Batmanova, in *Proceedings of 2012 28th International Conference on Microelectronics* (IEEE, 2012), pp. 335–338.
[21]R. Engel-Herbert, Y. Hwang, and S. Stemmer, J. Appl. Phys. **108**, 124101 (2010).
[22]R. Addou, L. Colombo, and R. M. Wallace, ACS Appl. Mater. Interfaces **7**, 11921 (2015).
[23]R. Addou, S. McDonnell, D. Barrera, Z. Guo, A. Azcatl, J. Wang, H. Zhu, C. L. Hinkle, M. Quevedo-Lopez, H. N. Alshareef, L. Colombo, J. W. P. Hsu, and R. M. Wallace, ACS Nano **9**, 9124 (2015).
[24]S. Bhattacharjee, K. L. Ganapathi, D. N. Nath, and N. Bhat, IEEE Trans. Electron Devices **63**, 2556 (2016).
[25]K. Cho, M. Min, T.-Y. Kim, H. Jeong, J. Pak, J.-K. Kim, J. Jang, S. J. Yun, Y. H. Lee, W.-K. Hong, and T. Lee, ACS Nano **9**, 8044 (2015).
[26]M. Amani, D.-H. Lien, D. Kiriya, J. Xiao, A. Azcatl, J. Noh, S. R. Madhvapathy, R. Addou, S. KC, M. Dubey, K. Cho, R. M. Wallace, S.-C. Lee, J.-H. He, J. W. Ager, X. Zhang, E. Yablonovitch, and A. Javey, Science **350**, 1065–1068 (2015).
[27]S. Kim, A. Konar, W.-S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.-B. Yoo, J.-Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Choi, and K. Kim, Nat. Commun. **3**, 1011 (2012).
[28]M. Takenaka, Y. Ozawa, J. Han, and S. Takagi, in *2016 IEEE International Electron Devices Meeting* (IEEE, 2016), pp. 5.8.1–5.8.4.
[29]D. Fleury, A. Cros, H. Brut, and G. Ghibaudo, in *2008 IEEE International Conference Microelectronic Test Structures* (IEEE, 2008), pp. 160–165.
[30]S. Bhattacharjee, K. L. Ganapathi, D. N. Nath, and N. Bhat, IEEE Electron Device Lett. **37**, 119 (2016).
[31]C. D. English, G. Shine, V. E. Dorgan, K. C. Saraswat, and E. Pop, Nano Lett. **16**, 3824 (2016).
[32]A. Konar, T. Fang, and D. Jena, Phys. Rev. B **82**, 115452 (2010).
[33]C. M. Smyth, R. Addou, S. McDonnell, C. L. Hinkle, and R. M. Wallace, J. Phys. Chem. C **120**, 14719 (2016).