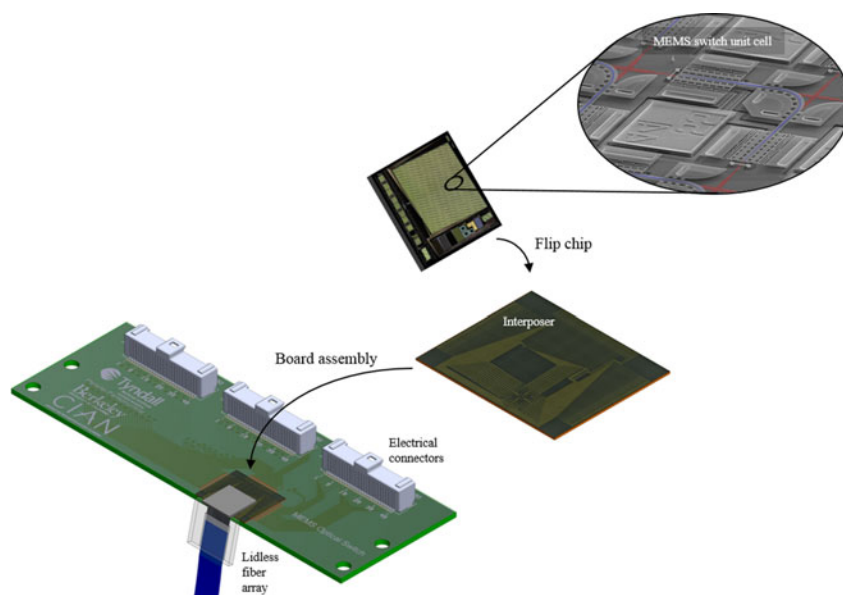| Title | Flip chip packaging of digital silicon photonics MEMS Switch for cloud computing and data centre |
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# Flip Chip Packaging of Digital Silicon Photonics MEMS Switch for Cloud Computing and Data Centre

*(Invited Paper)*

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**Abstract:**   We report on the flip chip packaging of Micro-Electro-Mechanical System
(MEMS)-based digital silicon photonic switching device and the characterization results
of 12 × 12 switching ports. The challenges in packaging $N^2$ electrical and 2N optical in-
terconnections are addressed with single-layer electrical redistribution lines of 25 $\mu$m line
width and space on aluminum nitride interposer and 13° polished 64-channel lidless fiber
array (FA) with a pitch of 127 $\mu$m. 50 $\mu$m diameter solder spheres are laser-jetted onto the
electrical bond pads surrounded by suspended MEMS actuators on the device before flux-
less flip-chip bonding. A lidless FA is finally coupled near-vertically onto the device gratings
using a 6-degree-of-freedom (6-DOF) alignment system. Fiber-to-grating coupler loss of
4.25 dB/facet, $10^{-11}$ bit error rate (BER) through the longest optical path, and 0.4 $\mu$s switch
reconfiguration time have been demonstrated using 10 Gb/s Ethernet data stream.

**Index Terms:** Flip chip, interposer, micro-electro-mechanical system (MEMS) packaging,
optical switches, silicon photonics.

## 1. Introduction

Demand for cloud computing and content-rich applications has led to massive growth in data traffic
managed by data centre. With an expected three-fold data traffic growth from 135 zettabytes in 2014

to 500 zettabytes by 2019 [1], data centre operation is undergoing a paradigm shift in the network architecture. Up to recent years, CMOS electronics, which are data rate and protocol dependent, have been responsible for traditional data traffic routing. Commonly known as OEO switching, there are three components involved in the switching operation. Incoming optical signals are first converted into the electrical signal (OE conversion) before switching operation in the electrical domain and finally reconverted back into optical signals (EO conversion). Scaling up of data centre to adapt to the growth in data traffic becomes increasingly challenging as any expansion requires the addition or replacement of OE and EO converter modules. As a result, the management of system size, power consumption and hardware cost becomes challenging.

Fortunately, progress in silicon photonics since the first demonstration of silicon-on-insulator (SOI) waveguides in 1985 [2]–[4] has now made data switching in the optical domain (OOO switching) possible. Large scale integrated photonic switches can be realized on silicon at low cost and with high yield leveraging the advanced manufacturing processes adopted in complementary metal-oxide-semiconductor (CMOS) industry. Higher degrees of freedom available in the optical domain allow a tremendous increase in bandwidth per fiber and the data processed in the switch fabric [5]–[8]. In fact, close to 75 % of the data traffic is transferred between servers in the data centre [1], making OOO switching systems more attractive. Over the years, there have been a variety of optical switching fabric proposed and demonstrated based on electro-optic [9], [10], thermo-optic [11]–[15] and three-dimensional (3-D) MEMS [16], [17] switching mechanisms. 3–D MEMS switch has merits for low optical loss, scalability and polarization insensitivity, but it is slow with millisecond response time. Previous integrated switches are based on cascaded multi-stage switching architecture, therefore the optical loss is quickly increased as the switch size scales up. While photonics device design and fabrication based on SOI have made tremendous progress, packaging of these devices continues to meet various technical challenges [18]–[21] and more so when MEMS structures are involved [22]–[25].

Recently, the team at UC Berkeley has developed 50 $\times$ 50 and 64 $\times$ 64 digital silicon photonic MEMS switches with sub-microsecond switching times, low on-chip losses and broad optical bandwidths [26]–[28]. In general, for an N $\times$ N digital switching device, there are $N^2$ electrical interconnects (excluding grounds) and 2N optical interconnects. We have previously demonstrated that a N $\times$ N silicon photonic MEMS switch matrix with $N^2$ individual switch unit cells can be electrically interfaced using a row-column addressing method, exploiting the inherent hysteresis of the electrostatic MEMS actuator [29]. This reduces the required electrical interface to 2N contacts, which is compatible with standard wire bonding. However, this approach relies on a tradeoff between ease of integration and achievable switching speed, as the individual switch unit cells can only be addressed sequentially. In order to fully harness the sub-microsecond switching time, individual addressing of $N^2$ electrical contacts is required. This poses major electrical routing challenges for packaging due to the density of these interconnects. Similarly, 2N optical interconnects will lead to a large fiber array for external coupling, considering the typical pitches of 127 $\mu$m and 250 $\mu$m. Depending on the manufacturing tolerances, there can be channel-to-channel pitch variations and these can accumulate and lead to high insertion losses. Large fiber array alignment onto optical interconnects also poses additional challenges, as a precise 6-degree-of-freedom (6-DOF) control is needed to minimize the insertion loss variations from one end of the array to another. Finally, suspended MEMS near electrical interconnects do not allow the use of material that can leave residues such as solder flux [30], [31] and polymer resin such as glob top or underfill near them due to interference.

In this article, we report in detail the electrical and optical packaging of the 50 $\times$ 50 switch device and its associated challenges. We selected a sub-array of 12 $\times$ 12 switches in this first packaging demonstration, using single layer electrical redistribution lines (RDL) ceramic interposers to fan-out the 146 electrical interconnects (including grounds) through flip-chip configuration. An angle polished lidless fiber array (FA), consisting of 64 SMF-28 and spaced at 127 $\mu$m was used for optical coupling. The optical transmission characteristics such as bit error rate (BER) and
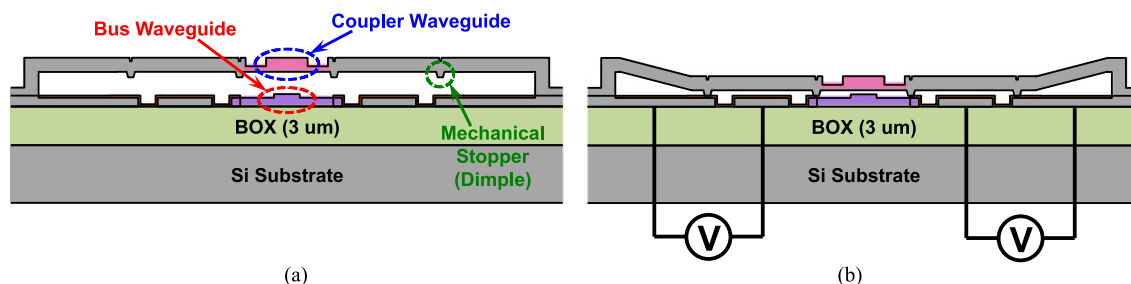
Fig. 1. Schematics of MEMS switch unit cell depicting coupler and bus waveguides, the mechanical stoppers and their operating principle during (a) OFF state and (b) ON state.
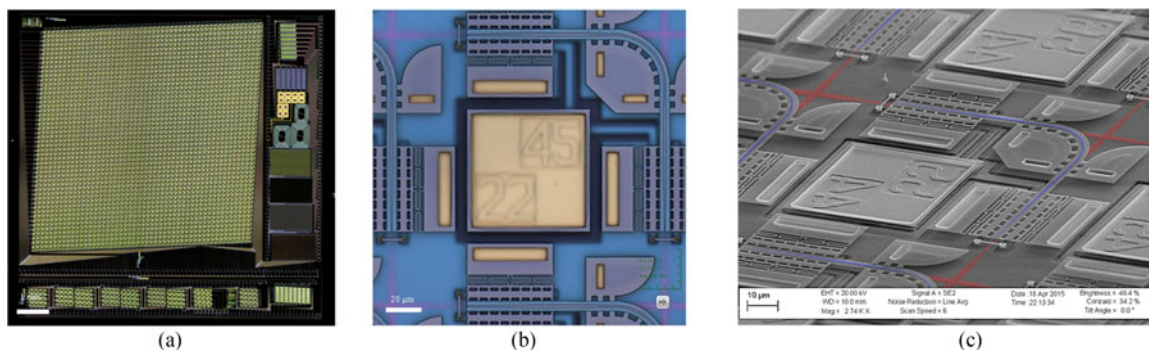


Fig. 2. (a) Overview of the 50 × 50 switching device used in packaging demonstration and a switch unit cell under (b) optical and (c) scanning electron microscope (SEM).

reconfiguration time of the packaged switch were finally measured using 10 Gb/s Ethernet data streams.

## 2. Overview of Digital Silicon Photonic MEMS Switch

The operating principle of the silicon photonic MEMS switch is illustrated in Fig. 1. The switching element consists of a pair of adiabatic couplers suspended above the bus waveguides. When the device is under OFF state, the adiabatic couplers are suspended at 1 $\mu$m above the bus waveguides and do not interfere with the light propagation within the bus waveguides. When a voltage is supplied (ON state), the initially suspended adiabatic couplers are pulled down by the integrated MEMS actuators electrostatically, allowing light coupling from the bus waveguides to the first adiabatic couplers. After a 90° turn, light is coupled to orthogonal bus waveguides through the second adiabatic couplers. Mechanical stoppers patterned by photolithography define the coupling distance between adiabatic couplers and bus waveguides precisely. The optical insertion loss and crosstalk are independent of the bias voltage applied to the MEMS actuators. The intrinsic digital operation of MEMS actuators enables large scale digital switching operations and we have observed a good reliability that the switch can operate over ten billion cycles without failures [27].

Fig. 2 shows the 50 × 50 switching device selected for the first optical and electrical packaging demonstration. 2500 silicon photonic switches are monolithically integrated on SOI, within an area of 7.6 mm × 7.6 mm. Each pair of suspended MEMS actuators (top and right of Fig. 2(b)) are controlled by the bond pad in the centre. This switching architecture is highly scalable as light passes through only one switching element regardless of the switch size. The grating couplers implemented on the switch device have a uniform pitch of 640 nm and a duty cycle of 50 % for optimum coupling of TE-polarized light. Although this device was designed for TE-polarized light, it has been reported that polarization insensitive switches can be demonstrated using the same silicon photonic MEMS switching architecture [32]. Device level characterisation has shown a

sub-microsecond switching time (approximately 3 orders of magnitude faster than commercial 3-D MEMS switches), broad spectral bandwidth (1400 – 1700 nm), high extinction ratio (>50 dB) and digital switching characteristic.

## 3. Electrical Packaging

### 3.1. Electrical Design

In order to realize the full potential of the switching device, there is a need to address the large number of electrical ports. For instance, an N × N switching device will require $N^2$ electrical interconnects at the test board interfacing the device and end user. Density of electrical bond pads to be connected and their locations in the centre of the device do not allow straightforward wire bonding onto the test board as long wires can lead to sagging and shorting. Exposed and suspended MEMS structures located at the four corners of electrical bond pads also limit the application of glob top (typically used in electronic packaging) to keep the wires rigid and in place. On the other hand, there is a mismatch between the device and printed circuit board (PCB) design rules, making direct flip-chip bonding onto the board challenging. At the same time, difference in coefficient of thermal expansion (CTE) between silicon (2.9 ppm/K) and PCB (FR4, 14 ppm/K) could lead to reliability issues especially when underfills are not used.

In this first packaging demonstration, we selected a sub-array of 12 × 12 (out of 50 × 50) switching cells for faster assembly, which results in 146 electrical interconnects (including ground pads). Instead of a direct flip-chip-bonding onto the PCB, a 250 $\mu$m thick aluminum nitride (AlN, 4.5 ppm/K) interposer was used as an intermediate substrate between the device and board to minimize CTE mismatches. Unlike wire bonding, flip-chip requires a mirrored bond pad orientation on the substrate, thus the design convention (device face up or face down) should be decided at the beginning and consistently followed. This is particularly important for non-symmetrical pad-array configuration. Based on the device layout, only 3 edges of the interposer can be used to populate the electrical bond pads connecting to the PCB, as optical interconnections are needed at one of the edges. Single metal layer electrical redistribution lines (RDL) were designed using 25 $\mu$m line width and space specification to fan-out the 146 electrical interconnects from the device. This design resulted from the decision to connect every alternate bond pad from the device, effectively doubling the pad pitch from 145 $\mu$m to 290 $\mu$m thus relaxing the routing density. Titanium/platinum/gold (Ti/Pt/Au) was selected as the preferred RDL metallization on the interposer to reduce transmission line resistance. The number of switching cells can be readily expanded / scaled up with the use of multi-layer RDL or finer line width and space RDL design rule available with advanced silicon and glass interposers. Simplistically speaking, assuming similar line widths of 25 $\mu$m, two metallization layers will be required should the number of electrical interconnect be doubled from 146 to 292 (assuming that the pad pitch remains the same), and this will add to the manufacturing cost as well.

At the same time, a two-layer PCB was also designed to connect the 146 electrical lines from the device, with the bond pads arranged in staggered fashion to match the pad pitch of the interposer. This minimizes the wire bonding length and prevents overlapping and sagging of bond wires, thus preventing shorts. The bond pads were finished with electroless nickel immersion gold (ENIG) for wire joint reliability. Three pluggable electrical sockets, each capable of taking 50 discrete electrical wires, were placed at one side of the PCB and served as the interface for testing and characterisation. The final design of the ceramic interposer and PCB are shown in Fig. 3. The electrical designs were then matched and confirmed with optical designs before components manufacturing were committed.

### 3.2. Electrical Assembly

Prior to flip chip assembly, 50 $\mu$m diameter solder spheres made of tin-silver-copper (SAC 305, Duksan Hi-Metal Co. Ltd.) were laser jetted onto the device bond pads using PacTech SB$^2$-SM (Fig. 4(a)). The jetting process was automated by generating a rhombus shape bond map, defining
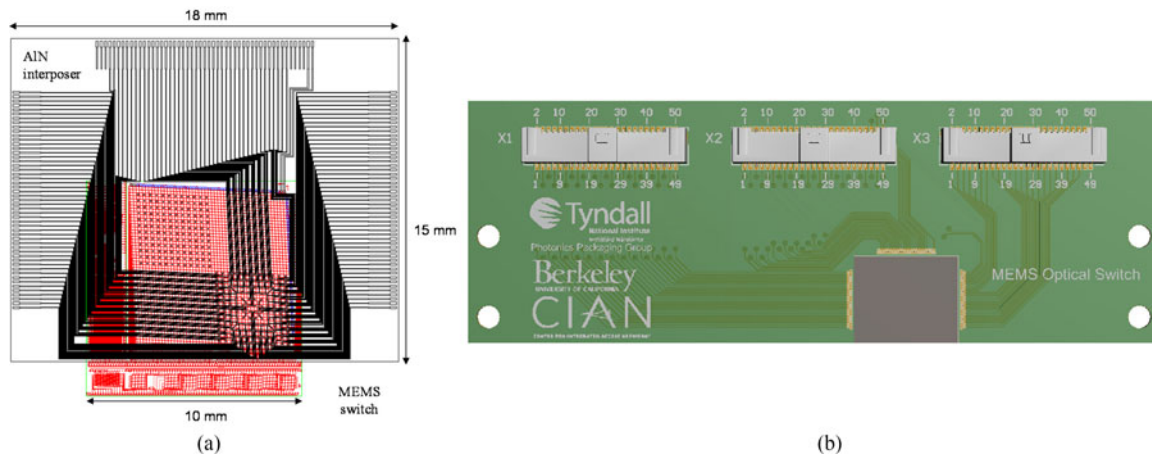
Fig. 3. Design of (a) ceramic interposer to fan-out 12 × 12 electrical interconnects located at the bottom right quadrant of the device and (b) printed circuit board (PCB) assembly with staggered wire bond pads.
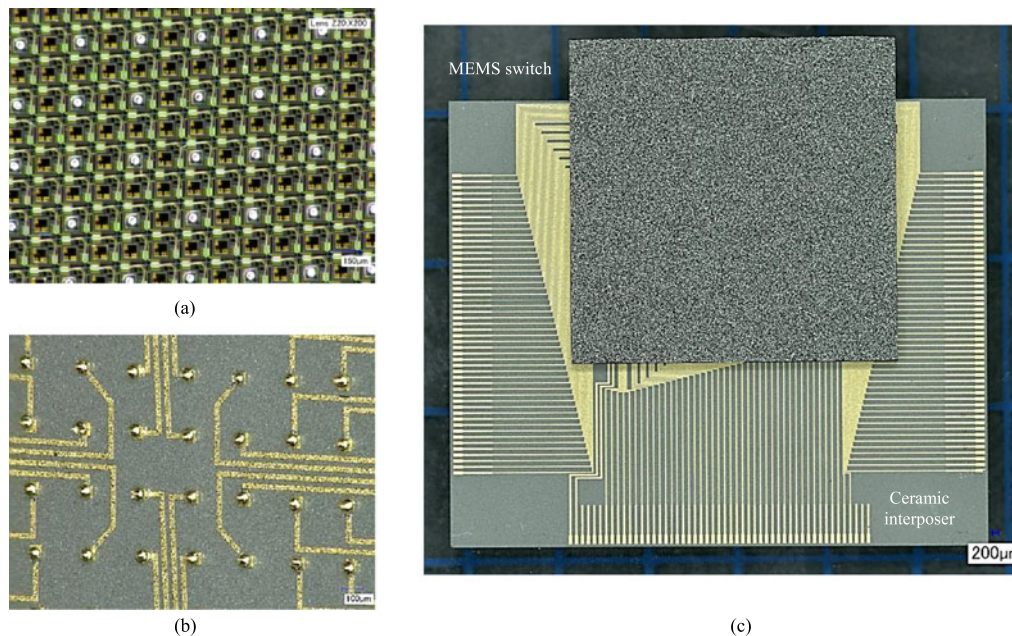


Fig. 4. (a) Solder (SAC 305) bumps on switch device and (b) gold (Au) stud bumps on ceramic interposer and (c) flip chip assembly of the device on interposer.

the coordinates where a solder bump was required on the device. Gold stud bumps were also made on an AlN interposer using 0.8 mil wires and coined (flattened) for co-planarity and flip-chip height control (Fig. 4(b)). The device was then flipped and aligned onto AlN interposer using a Finetech flip chip bonder and reflowed at a peak temperature of 260 °C within a $N_2$ enclosure. Fluxless reflow was used to prevent residue on MEMS actuators and optical gratings. Similarly no capillary underfill was used to improve solder joint strength in order to prevent gap filling within MEMS actuators and obstruct their motions. The reflowed assembly is shown in Fig. 4(c).

Assembled component (device and interposer) was then attached onto PCB using thermal epoxy, making sure that the pads on the interposer were aligned properly with those on the PCB (Fig. 5(a)). Electrical connections to test sockets were finally formed between the interposer and PCB through gold wires and protected with glob top (Fig. 5(b)). The board was finally attached onto a carrier
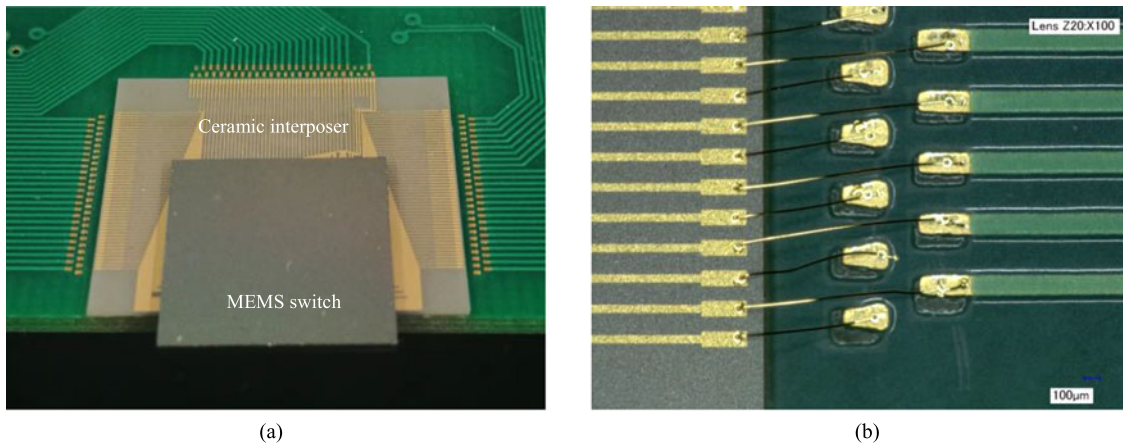
Fig. 5. (a) Flip-chip assembly bonded onto PCB and (b) gold wires connecting AlN interposer to PCB.
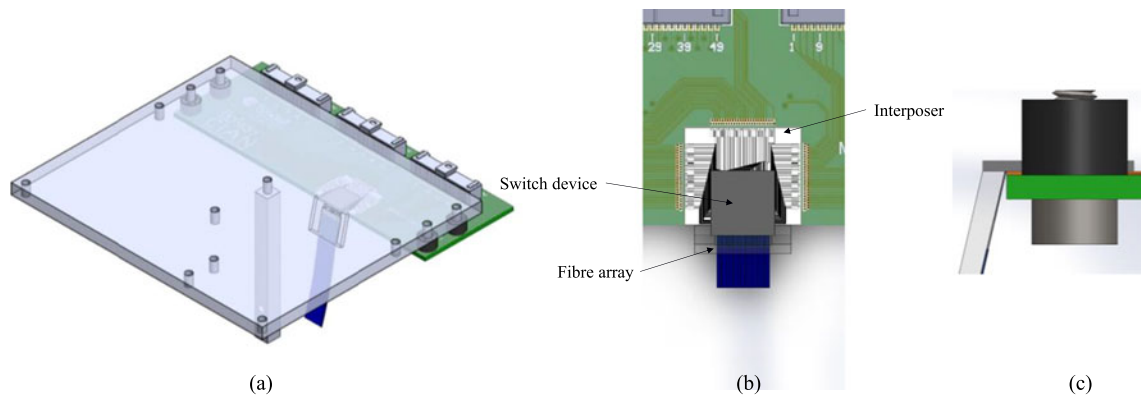


Fig. 6. 3-D Solidworks models showing (a) the expected package assembly with its mechanical housing and fiber support post, (b) top view of the model showing FA alignment onto device, interposer and PCB and (c) side view of the model showing that only a lidless fiber will be able to couple to the device gratings due to proximity to interposer edge.

made for optical packaging. Optical coupling is typically processed as the final packaging step due to sensitivity in index-matching resin to temperature. Glass-transition-temperatures ($T_g$) of these materials are generally lower than those used for electronic encapsulation and molding. Process temperatures above $T_g$ soften the resin, leading to optical alignment issues [33].

## 4. Optical Packaging

### 4.1. Optical Design

Similar to electrical packaging, there is also a need to address the large number of 2N optical interconnects needed for an N × N switching device. In this packaging demonstration, there are 36 optical ports serving as input, through and drop ports which can only be accessed using a 64-channel FA, owing to the device configuration. The PCB, FA and mechanical housing were put together using SolidWorks in 3-dimensions (3-D) during the design stage to confirm the optical assembly (Fig. 6). The model made clear that the close proximity between the grating couplers and the interposer edge would not allow a typical FA to reach the couplers. Although a planar coupling approach would have solved this issue, a high polished angle (51.5°) FA cannot be fabricated due to the large array size. High angle polishing, in which individual fiber are resin-fixed on the V-groove,
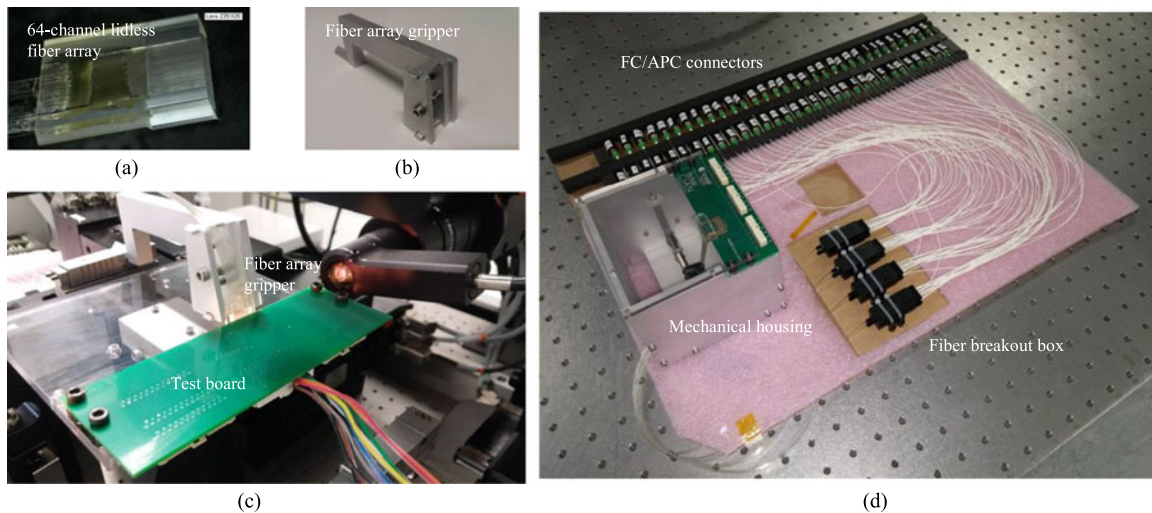
Fig. 7. (a) Lidless FA and (b) the FA gripper used during (c) active alignment. (d) The fully assembled optical switch package completed with mechanical housing.

proved to be challenging as some fiber peel off was observed. Thus, a 13° polished lidless FA was used instead.

### 4.2. Optical Assembly

After electrical assembly, the lidless 64-channel FA (Fig. 7(a)) was coupled near-vertically to the device gratings through active alignment using a 6-DOF alignment system from Newport Corp (Fig. 7(c)). A gripper capable of handling a large FA was used (Fig. 7(b)). Due to the large width of FA, the alignment process becomes more challenging even with the assistance of shunts on the device. The FA had to be slowly adjusted to make sure that it was parallel to the gratings plane, because a larger gap between FA and grating couplers will lead to higher insertion loss. Passive optical coupling solutions such as optical proximity coupling [34], [35] or evanescent coupling [36] therefore become attractive especially when large numbers of coupling channel are required. Index-matching resin (NOA 61, Norland) was then applied to fill the air gap between the FA and grating couplers before finishing with OP-4-20632 (Dymax) at the edges for mechanical strength. Extra care and precise dispensing of optical resin were needed to prevent the resin from flowing into the flip-chip gap. Finally, a fiber post was attached onto the carrier, fixed with room-temperature-curing resin and transferred to a mechanical housing to maintain the integrity of the FA. The fully assembled silicon photonic switch package is shown in Fig. 7(d). The packaging assembly had been designed for ease of characterisation using long fiber terminated with FC/APC connectors. For commercial application, MTP or MPO connectors can be used as optical fiber termination to keep the package lean.

## 5. Results And Analysis

### 5.1. Electrical and Optical Assembly

In order to confirm the flip-chip alignment after reflow, samples were analyzed through nondestructive and destructive methods. Nondestructive methods such X-ray imaging allows a quick confirmation of the alignment after reflow process. On the other hand, destructive methods such as mechanical polishing can provide more information, including solder joint quality, assembly height and bump height variations across the flip chip assembly. Further analysis after mechanical polishing can also be done using scanning electron microscopy (SEM) and energy dispersive x-ray microscopy (EDX) to study the solder joint microstructures and reveal fine cracks and delamination
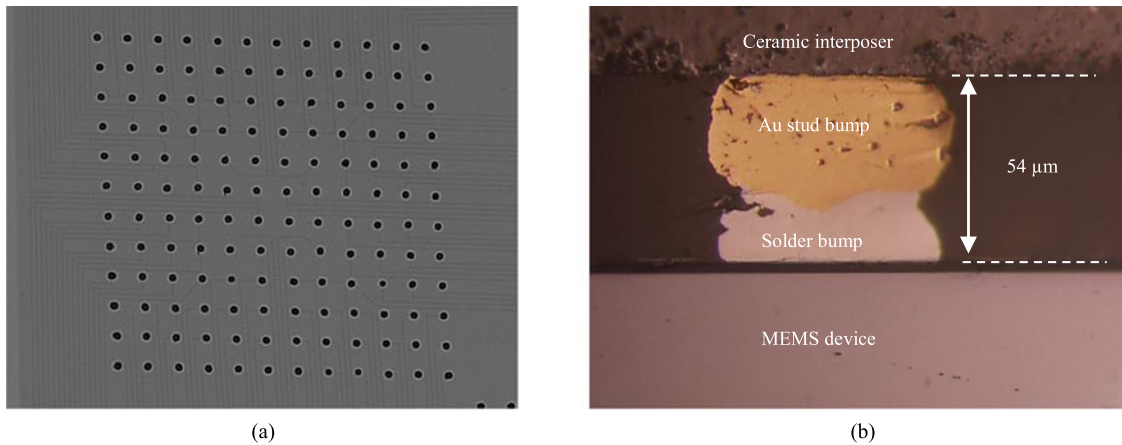
Fig. 8. (a) X-ray of flip chip assembly and (b) mechanical cross-section showing Au stud and solder bump alignment.
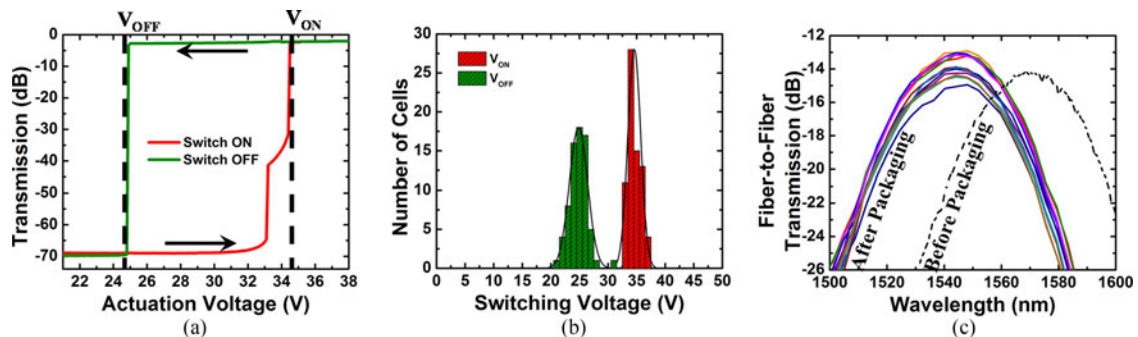


Fig. 9. (a) Measured transmission as a function of bias voltage of a switch cell, (b) switching voltage distribution of 70 MEMS switch cells and (c) fiber-to-fiber transmissions of various switch path.

not immediately clear through optical microscopy. Fig. 8(a) shows an x-ray image of the flip-chip assembly, in which solder bumps on the device were properly aligned with the stud bumps on the interposer. Mechanical polishing of the assembly confirmed the bump alignment, the solder-stud joint quality and the assembly height (Fig. 8(b)).

Subsequently, the fully assembled package was tested and analyzed. The MEMS actuations were driven using a Keithley 2400 power supply by varying the voltage only. Input light source was supplied by a 1550 nm peak superluminescent diode (SLD) and the fiber-to-fiber transmissions were measured using an Anritsu MS9710C spectrum analyser. Fig. 9(a) showed the transmission characteristics of a switch cell as a function of bias voltage. The OFF- and ON- state switching voltages were measured to be 34.6 V and 24.8 V with standard deviations of 1.1 V and 1.6 V respectively (Fig. 9(b)). The 10 V difference between OFF- and ON- state voltages is due to intrinsic bias hysteresis of the gap-closing actuators. Meanwhile fiber-to-coupler loss was measured to be 4.25 dB / facet and fiber-to-fiber transmissions between 12.9 dB to 14.5 dB near 1550 nm were recorded (Fig. 9(c)). The variation in fiber-to-fiber transmission was due to the optical path length difference of the $12 \times 12$ ports being analyzed.

## 5.2. System Characterisation

Finally, system level characterisation was performed on the package to analyse the switching performance. For bit error rate (BER) experiment, a 10 Gb/s Ethernet data stream was generated by a Virtex-6 FPGA and drove an enhanced small form-factor pluggable (SFP+) transceiver module. The optical data stream from the SFP+ module was inserted to the switch package. The output
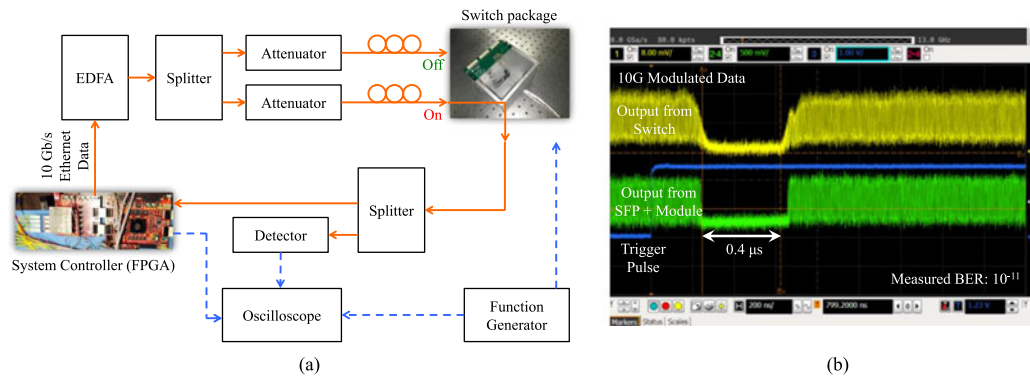
Fig. 10. (a) Block diagram of system level characterization and (b) switching performance with 10 Gb/s data stream.

signal from the package was sent to the SFP+ module on the FPGA to measure BER. For the longest optical path switching configuration (worst case), BER was measured to be $10^{-11}$. For switch reconfiguration experiment, we used the system experiment setup shown in Fig. 10(a). The optical data stream was split and sent to two input ports of the switch package. In the stream paths, EDFA and attenuators were used to compensate the split loss and recover the output power of the SPF+ module for each stream. Two switch cells were controlled to select one of two input streams and send it to an output port. The output stream from the package was split and monitored by a linear detector [yellow trace in Fig 10(b)] and a SPF+ module on the FPGA board [green trace in Fig. 10(b)]. Physical switch reconfiguration time of the package was recorded to be 0.4 $\mu$s.

## 6. Conclusion

The first MEMS-based silicon photonic switch package has been demonstrated using a flip-chip configuration. The packaging challenges ($N^2$ electrical and 2N optical interconnects) are addressed with the use of 25 $\mu$m line width / space RDL on ceramic interposer and lidless fiber array (FA) consisting of 64 SMF-28 fibers spaced at 127 $\mu$m. A fluxless reflow with laser jetted solder bumps has demonstrated good alignment between the device and interposer. A fiber-to-grating coupler loss of 4.25 dB / facet and an average switching ON voltage of 34.6 V with a standard deviation of 1.1 V had been recorded. The worst case bit-error-rate (BER) of the package was $10^{-11}$ while the switch reconfiguration time was 0.4 $\mu$s using a 10 Gb/s Ethernet data stream.

Future work includes expanding the number of packaged port counts using multi-layer RDL glass interposer and pitch reducing fiber-to-device planar coupling array. Passive optical coupling solution based on evanescent transmission is also in the work and will be demonstrated in the future. This approach will allow high density and large scale optical / electrical interconnects to be incorporated on silicon photonics devices. It will also allow heterogenous integration of electronic and photonic components into a system-in-package (SiP) for the age of "Internet of Everything".

## Acknowledgment

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