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# Investigation of electrically active defects at the interface of high-k dielectrics and compound semiconductors

A thesis presented to

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by

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**Declaration**

The work in this thesis has been carried out by me at the Tyndall National Institute, University College Cork, Ireland. Any work carried out by my colleagues or collaborators is clearly indicated. This work not been submitted for another degree, either at University College Cork or elsewhere.


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Éamon O'Connor                                                        Date

## List of Acroynms

3-D           3-dimensional

a.c           alternating current

AFM           Atomic Force Microscopy

ALD           Atomic Layer Deposition

$a$-Si           amorphous Silicon

CV           Capacitance-Voltage

CMOS           Complementary Metal-Oxide-Semiconductor

CVD           Chemical Vapor Deposition

DC           Direct Current

e-beam           electron-beam

EOT           Equivalent Oxide Thickness

FET           Field Effect Transistor

FGA           Forming Gas ($H_2/N_2$) Anneal

GV           Conductance-Voltage

IV           Current-Voltage

ITRS           International Technology Roadmap for Semiconductors

MBE           Molecular beam Epitaxy

MOS           Metal-Oxide-Semiconductor

| | |
|---|---|
| MOSCAP | Metal-Oxide-Semiconductor Capacitor |
| MOSFET | Metal-Oxide-Semiconductor Field Effect Transistor |
| MOVPE | Metal-Organic Vapor Phase Epitaxy |
| | |
| PECVD | Plasma Enhanced Chemical Vapour Deposition |
| PVD | Physical Vapour Deposition |
| | |
| RMS | Root Mean Square |
| RTA | Rapid Thermal Anneal |
| | |
| SEM | Scanning Electron Microscopy |
| SOI | Silicon on Insulator |
| SS | Subthreshold Swing |
| | |
| TEM | Transmission Electron Microscopy |
| TMA | Trimethyl-Aluminum [$Al(CH_3)_3$] |
| | |
| UHV | Ultra High Vacuum |
| | |
| XPS | X-Ray Photoelectron Spectroscopy |

**List of Symbols**

| | |
|---|---|
| A | Device Area [m$^2$] |
| | |
| C | Capacitance [F/m$^2$] |
| $C_D$ | Depletion Layer Capacitance [F/m$^2$] |
| $C_{et}$ | Capacitance Equivalent Thickness [F/m$^2$] |
| $C_{fb}$ | Flat-band Capacitance [F/m$^2$] |
| $C_{HF}$ | High-Frequency Capacitance [F/m$^2$] |
| $C_{it}$ | Interface State Capacitance [F/m$^2$] |
| $C_{LF}$ | Low-Frequency Capacitance [F/m$^2$] |
| $C_m$ | Measured Capacitance [F/m$^2$] |
| $C_{min-meas}$ | Measured Minimum Capacitance [F/m$^2$] |
| $C_{min-theor}$ | Theoretical Minimum Capacitance [F/m$^2$] |
| $C_{ox}$ | Oxide Capacitance [F/m$^2$] |
| | |
| $D_{it}$ | Interface State Density [cm$^{-2}$eV$^{-1}$] |
| | |
| $E_A$ | Activation Energy [eV] |
| $E_C$ | Conduction Band Edge [eV] |
| $E_f$ | Fermi level [eV] |
| $E_{f-M}$ | Metal Fermi Level [eV] |
| $E_g$ | Energy Bandgap [eV] |
| $\varepsilon_0$ | Permittivity of Free Space [F/m] |
| $\varepsilon_s$ | Semiconductor Dielectric Constant |
| $E_V$ | Valence Band Edge [eV] |

| | |
|---|---|
| $f_p$ | Parallel Conductance Peak Frequency [Hz] |
| $G$ | Conductance [S] |
| $G_m$ | Measured Conductance [S/m$^2$] |
| $G_p$ | Parallel Conductance [F/m$^2$] |
| $I_{OFF}$ | Off-state current [A/m$^2$] |
| $k$ | Dielectric Constant (or relative permittivity) |
| $k_B$ | Boltzmann Constant [J/K] |
| $L$ | MOSFET Gate Length [m] |
| $N_D$ | Semiconductor Dopant Density [m$^{-3}$] |
| $n_i$ | Intrinsic Carrier Density [m$^{-3}$] |
| $q$ | Electron Charge [C] |
| $Q_{fixed}$ | Fixed Oxide Charge [C/m$^2$] |
| $Q_{it}$ | Interface State Charge [C/m$^2$] |
| $t_{ox}$ | Oxide Thickness [m] |
| $\tau_g$ | Minority Carrier Generation Lifetime [s] |
| $V$ | Voltage [V] |
| $V_{DD}$ | Supply Voltage [V] |
| $V_{fb}$ | Flat-band Voltage [V] |
| $V_{gate}$ | Gate Bias [V] |

$V_T$          Threshold Voltage [V]


$\omega$          Angular Frequency [rad/s]

$W$          MOSFET Gate Width [m]

$W_f$          Metal Work Function [eV]


$x_{d\text{-}max}$          Maximum Depletion Width [m]

**Abstract**

As silicon based devices in integrated circuits reach the fundamental limits of dimensional scaling there is a growing research interest in the use of high electron mobility channel materials, such as indium gallium arsenide (InGaAs), in conjunction with high dielectric constant (high-$k$) gate oxides for Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) based devices. The motivation for the use of high mobility channel materials is to reduce the overall power dissipation in integrated circuits while also providing improved performance. For the successful implementation of high mobility channel materials in large volume manufacturing, it will be essential to gain a more complete understanding of electrically active defect states in the high-$k$/InGaAs MOS system which forms the gate stack of the MOSFET. The work presented in this PhD thesis details the characterization of MOS devices incorporating high-k dielectrics on III-V semiconductor substrates. The analysis examines the role of the semiconductor substrate, optimization of device passivation procedures, and analysis of electrically active interface defect states at the high-$k$/InGaAs interface primarily through the capacitance-voltage (CV) and conductance-voltage (GV) response of the InGaAs MOS system as a function of frequency and temperature.

Given one of the primary motivations for introducing these III-V materials is to take advantage of their mobility, one factor of interest is to examine $In_xGa_{1-x}As$ channels with varying indium concentrations, as a higher indium concentration increases the electron mobility. Of additional significance is how the modification of the $In_xGa_{1-x}As$ bandgap with varying In concentration affects device performance in terms of interface defect concentration ($D_{it}$) at the high-$k$/$In_xGa_{1-x}As$ interface. To this end, the structural and electrical properties of $HfO_2$ films on GaAs and $In_xGa_{1-x}As$ substrates for x: 0, 0.15, 0.30, and 0.53, were examined. A large dispersion of accumulation capacitance was observed for *n*-type GaAs and low In content (x = 0.30, 0.15) $In_xGa_{1-x}As$ epitaxial layers, the electrical behaviour being dominated by an interface state defect response. By contrast, comparison of the capacitance voltage characteristics at 295K and cooled to 77K indicates that it is possible to achieve true

accumulation for an $In_{0.53}Ga_{0.47}As$ MOS structure. The defect responsible for the accumulation dispersion has a minimum density of $2.5 \times 10^{13}$ cm$^{-2}$, with an energy level $\geq 0.75$ eV above the valence band in the $HfO_2/In_xGa_{1-x}As$ system, where the defect energy with respect to the valence band does not change with the composition of the $In_xGa_{1-x}As$. A post-gate metallization $325^{o}C$ forming gas anneal was found to reduce the interface state concentration ($D_{it,}$) at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface, as determined from both CV curves, and analysis of the conductance response versus frequency. As true surface accumulation was only achieved for MOS structures formed on $In_xGa_{1-x}As$ with a 53% In concentration (x=0.53), the remaining chapters of the thesis focused on $In_{0.53}Ga_{0.47}As$ lattice matched to InP substrates.

A wide range of passivation approaches have been investigated in order to improve the characteristics of the high-k/III-V interface. Among these are solution based approaches, one of the more popular methods being immersion of the III-V surface in an ammonium sulfide, $(NH_4)_2S$, solution prior to oxide deposition. However, there has not been a clear discussion in terms of optimization of the $(NH_4)_2S$ passivation procedure with different research groups using a variety of pre-treatments, $(NH_4)_2S$ concentrations, and immersion times. Therefore, a systematic study was performed to optimize an ammonium sulphide $(NH_4)_2S$ surface passivation technique for $In_{0.53}Ga_{0.47}As$. $(NH_4)_2S$ concentrations (ranging from 1% to 22%) were investigated, with multi-frequency CV results indicating that the lowest frequency dispersion over the bias range examined occurred for *n* and *p*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$ devices treated in the 10% $(NH_4)_2S$ solution. A deleterious effect on device electrical behaviour of prolonged ambient exposure post $In_{0.53}Ga_{0.47}As$ surface passivation was identified. Physical analysis of identical films performed using XPS supported this observation through changes in the composition of the re-grown oxide. Estimations of interface state density, $D_{it}$, extracted using the Conductance Method, and the High-Low Capacitance-Voltage Method, show very good agreement both in terms of magnitude and characteristic peak profile for the optimum 10% $(NH_4)_2S$ passivated $In_{0.53}Ga_{0.47}As$ devices. The results suggest that these *n*-type and *p*-type devices have an integrated $D_{it}$ of $\sim 2.5 \times 10^{12}$ cm$^{-2}$ ($\pm 1 \times 10^{12}$

cm$^{-2}$) across the In$_{0.53}$Ga$_{0.47}$As energy gap, with the peak density approximately 0.37eV ($\pm 0.03$ eV) from the valence band edge.

Despite a large research effort worldwide over a number of years, very few studies to date have demonstrated results indicating genuine surface inversion at the high-$k$/In$_{0.53}$Ga$_{0.47}$As interface, owing primarily to the high D$_{it}$ typically observed in these devices. Achieving free Fermi level modulation across the bandgap in devices incorporating high-$k$ on In$_{0.53}$Ga$_{0.47}$As, has presented one of the major obstacles to the introduction of this materials system in commercial applications. Following an optimized 10% (NH$_4$)$_2$S treatment with minimal ambient exposure pre-ALD, a clear minority carrier response was observed for both $n$-type and $p$-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOS devices in this work. Multi-frequency CV and GV characteristics of the devices exhibited a number of signature features consistent with inversion of the In$_{0.53}$Ga$_{0.47}$As surface. Analogous behavior was observed at fixed frequency with varying measurement temperature. An Arrhenius extraction of activation energies for the minority carrier response indicated a transition from a generation-recombination regime at lower temperature to a diffusion controlled response at elevated temperatures, for both $n$-type and $p$-type devices. Also, MOS capacitors were fabricated on $n$ and $p$-In$_{0.53}$Ga$_{0.47}$As with semiconductor doping concentrations ranging over two orders of magnitude from ~1x10$^{16}$cm$^{-3}$ to ~2x10$^{18}$cm$^{-3}$. It was clearly observed for both $n$ and $p$-In$_{0.53}$Ga$_{0.47}$As devices that the measured C$_{min}$ increases as doping concentration increases, and that the measured C$_{min}$ is in very good agreement with the theoretical value calculated by assuming an inverted surface. Taken as a whole, these observations are consistent with a D$_{it}$ which is sufficiently reduced for the $n$-type and $p$-type devices examined in this work to permit the Fermi level to be swept across the band gap at the In$_{0.53}$Ga$_{0.47}$As/Al$_2$O$_3$ interface.

The oxide capacitance, C$_{ox}$, is an important parameter in general for device analysis, for example in many common D$_{it}$ extraction methods. Therefore an experimental method to determine C$_{ox}$ accurately would be of great benefit for device analysis purposes, particularly for narrow bandgap systems such as In$_{0.53}$Ga$_{0.47}$As. Experimental observations for In$_{0.53}$Ga$_{0.47}$As devices in this work indicated that in

strong inversion the peak magnitudes of $G/\omega$ and $-\omega dC/d\omega$ are equal, with the peaks being coincident at the transition frequency, $\omega_m$. Physics based simulations exhibited near-identical behavior. The observation of this unique relationship offers an experimental route to estimate the value of oxide capacitance, $C_{ox}$. Mathematical derivations performed using an equivalent circuit model yielded expressions of $C_{ox}^2/2(C_{ox}+C_D)$ for $(G/\omega)_{max}$ and $(-\omega dC/d\omega)_{max}$, where $C_D$ is the semiconductor depletion capacitance. This provides a straightforward method for more accurate determination of $C_{ox}$ not only for III-V based devices, but for MOS systems in general. The usefulness of this relationship was demonstrated by varying the experimental $C_{ox}$ of samples through the use of a range of $Al_2O_3$ thicknesses (4nm, 8nm, and 12nm) on $n$ and $p$-type $In_{0.53}Ga_{0.47}As$. The expression derived for $(G/\omega)_{max}$ was found to provide an accurate fit to the $C_{ox}$ measured from CV at low frequency over the thickness range, providing a practical example of the application of this relationship and it's benefits particularly with regard to lower $E_{ot}$ devices. In addition it was found that a post gate metallization forming gas anneal leads to a reduction in the measured transition frequency. This is inversely proportional to the minority carrier generation lifetime, which was extracted through simulations from the measured $\omega_m$ values. This provides another metric to assess improvements in device quality as an increase in the minority carrier generation lifetime indicates a reduction in the density of bulk defects responsible for the minority carrier response in the generation-recombination regime.

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# Chapter 1

## 1. Background and Motivation

### 1.1. Introduction

The purpose of this chapter is to place in context the motivation for exploring the devices and materials systems studied in this thesis. A brief overview of the history of complementary metal-oxide-semiconductor (CMOS) transistor development is presented. In addition current trends in terms of the materials and device concepts being considered for future CMOS generations are outlined. An overview of the content of the thesis is also described.

### 1.2. Moore's Law

The last forty years have seen dramatic developments in computing power, information storage and digital communication technologies. This progress has been fuelled primarily by on-going miniaturisation of the metal oxide semiconductor field effect transistors (MOSFETs), which are the fundamental switching elements of integrated circuits. A schematic of a traditional *n*-MOSFET structure is shown in Figure 1.1, where W is the width of the device and L is the gate length. The thickness of the gate oxide employed as a dielectric in the structure is usually referred to as $t_{ox}$. The scaling of MOSFET gate length dimensions from values of around 10 $\mu$m in the early 1970's to values of around 65nm in 2007 was achieved without changing the basic device concept or the silicon and silicon dioxide ($SiO_2$) materials which constitute the device.
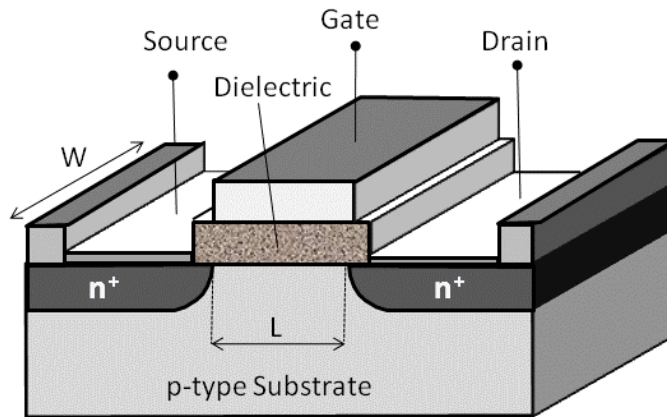
Figure 1.1 Schematic of traditional *n*-MOSFET. L and W are the device length and width respectively.

In 1965 Gordon Moore predicted that the density of transistors on a single chip would double every 18 months.[1] While a reduction in transistor size has obvious benefits in terms of footprint, allowing greater functionality per chip, the work of Dennard *et al.* also demonstrated attendant advantages in that as devices are scaled their logic characteristics also improve.[2] Decades of scaling have therefore resulted in vast improvements in switching speed, switching power, and supply voltage reduction. In recent years however it became clear that further scaling would not be possible using conventional device architectures and materials. A plateau was reached in this respect owing to the fact that device dimensions were now reduced to values where issues such as short channel effects become significant.[3, 4] Additionally, and of fundamental importance as consumer demand for low-power electronics increases is the fact that the density of devices per chip has reached levels where the power dissipation per chip is a major issue. The use of techniques such as strained Si was introduced at the 90nm and 65nm technology nodes to offset some of the problems associated with these shrinking device dimensions. One of the disadvantages in this respect was posed by ultra-thin $SiO_2$ layers, the thickness of which was now approaching 1.2 nm, equating to just a few atomic layers. Direct electron tunneling

through the gate oxide becomes a major problem at this thickness, resulting in high leakage currents and inevitably higher power consumption. In fact the off-state power dissipation becomes comparable to the active power dissipation, which is an unsustainable situation and requires impractical solutions in terms of cooling and packaging. Additionally, the impact of such tunneling currents raised serious concerns about reliability and lifetime issues in utilization of such thin oxide layers. In order to continue to meet targets set by Moore's Law a more revolutionary approach was required.

### 1.3. Incorporation of high-*k* dielectrics

The 45nm node marked the greatest shift in the history of MOSFET development in terms of its material composition. Intel introduced an oxide layer with a dielectric constant ($k$) higher than that of $SiO_2$ (3.9). For ease of nomenclature all materials with k>3.9 are usually referred to as high-*k* dielectrics. The source-drain current of a MOSFET is largely dependent on the capacitance of the MOS gate stack at the heart of an FET device. The rationale for incorporating a high-*k* material can be easily understood using the relationship in Equation 1.1, where C is capacitance, $\varepsilon_0$ is the permittivity of free space, $k$ is the dielectric constant (or relative permittivity) of the dielectric, A is the area of the capacitor, and $t_{ox}$ is the oxide thickness.

$$C = \frac{\varepsilon_o kA}{t_{ox}} \qquad \text{[EQ. 1.1]}$$

It is obvious that an equivalent capacitance density can be achieved using a thicker oxide with a higher dielectric constant. Therefore, given that tunneling current decreases exponentially with distance, this offers the potential to incorporate a thicker oxide layer in the MOSFET structure to eliminate some of the issues associated with excessive ultra-thin gate oxide leakage. A useful term is the Equivalent Oxide Thickness (EOT) which refers to the theoretical thickness of $SiO_2$ which would be required to achieve an equivalent capacitance density to that using a high-*k* dielectric.

$$EOT = \frac{3.9}{k_{high-k}} t_{high-k} \qquad \text{[EQ. 1.2]}$$

Incorporation of high-$k$ materials in CMOS posed a number of formidable challenges, not only as the existing $SiO_2$/Si technology was decades into its development, but also in that the industry had benefited enormously from a number of fortuitous and remarkable properties of $SiO_2$ on Si. Research into high-$k$ oxides exploded in the late 1990's and early 2000's and a review paper by Wilk $et$ $al$,[5] identified a number of key attributes required for any $SiO_2$ replacement. Among these were: permittivity; band offsets and insulating properties; thermodynamic stability; morphology; interface quality; process compatibility; reliability. $SiO_2$ is stable up to $1000^{o}C$, critical for example in terms of thermal budget for source/drain implants. In terms of processing, $SiO_2$ was ideal as it was possible to thermally oxidize the Si to form $SiO_2$, giving the added benefits of near ideal stoichiometry, excellent film morphology with a smooth interface with Si, and a very low density of interface defects ($D_{it}$). $SiO_2$ also remained amorphous to high temperature, which avoided the issue of grain boundaries forming in the oxide to promote leakage pathways. One other important asset of the $SiO_2$/Si system was its etch selectivity, which was critical as device dimensions reduced exponentially, and it was possible to pattern to the nanometer scale.
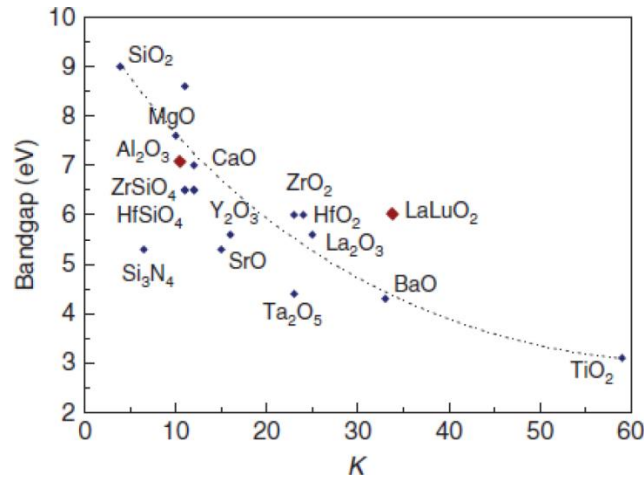


Figure 1.2 A plot of bandgap versus dielectric constant for a selection of the high-$k$ candidate materials.[6]

Some of the prominent high-$k$ options, and a plot of their band-gap versus permittivity, are seen in Figure 1.2.[6] As research into high-$k$ materials progressed, the primary difficulties associated with their use became apparent. In terms of processing, the existing polysilicon gate was unsuitable for use with high-$k$, necessitating the use of metal gates in order to prevent reactions at the high-$k$ polysilicon interface affecting device performance. Some complications in this regard stem from the fact that if a single gate metal is chosen then it would have to have a work function suitable for $n$-MOS and $p$-MOS, and if different gate metals were tailored for each this would induce extra processing complexity.

As the advantage of thermal oxide growth of the native oxide was lost, another issue became the deposition method on Si to be used for the high-$k$ oxides. Thermally grown oxides are of higher quality than deposited oxides. Physical Vapour Deposition (PVD), Chemical Vapour Deposition (CVD), and Atomic Layer Deposition (ALD) were considered as possible techniques for high-$k$. ALD became one of the more popular methods adopted for research purposes. ALD operates in a sequence of alternating half-cycles where gaseous precursors are introduced to a vacuum deposition chamber in isolation. One pulse carries the metal associated with the high-$k$ oxide (e.g., Al or Hf) and the second pulse carries the oxidant species. As the first gaseous precursor is injected it is chemisorbed on to the heated substrate. A
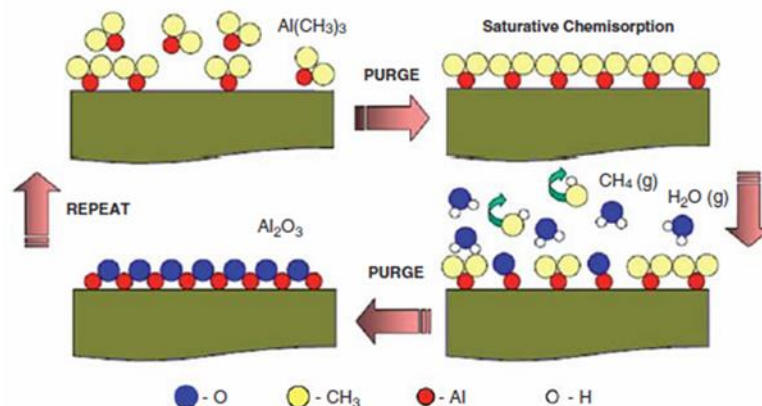


Figure 1.3 A schematic showing a typical pulse-purge sequence in the deposition of $Al_2O_3$, using $Al(CH_3)_3$ and $H_2O$ as precursors, from the review of Wallace *et al*.[11]

purge pulse is then used to remove physisorbed unreacted precursor and gas phase by-products. The whole process is repeated using the second precursor to complete an ALD cycle. This results in highly controllable self-limiting monolayer growth. Another important advantage is that it results in highly conformal films, making it suitable for complex structures and small feature sizes, ideal for CMOS. A typical pulse-purge sequence for deposition of $Al_2O_3$, using $Al(CH_3)_3$ and $H_2O$ as precursors, is shown in the schematic from the review of Wallace *et al* in Figure 1.3.[11] However, one drawback is that the use of precursors in the ALD of high-*k* oxides can introduce impurities in the oxide film originating from the precursor ligands. Defects in the oxide can lead to trapping of charges within the oxide layer, inducing threshold voltage shifts in MOSFET devices, and affecting reliability. Further it has been reported that remote phonon scattering effects from charges in the high-*k* can lead to a mobility reduction for devices incorporating high-*k* on Si.

One of the most significant problems associated with the incorporation of high-*k* materials was that interface defect densities at the interface of high-*k* with Si tended to be higher than those obtained for $SiO_2$/Si. In that system so called dangling bond defects ($P_b$ type defects) were known to exist originating from the Si surface, adversely affecting device performance. However these could be reduced significantly by annealing in forming gas ($H_2$/$N_2$), resulting in very low defect densities of the order of mid $10^{10}\,cm^{-2}\,eV^{-1}$. It is very difficult to achieve comparable densities at the interface of high-*k* directly on Si. A higher $D_{it}$ at the interface degrades the subthreshold slope (SS) of a MOSFET device, which impinges on its switching performance. In addition interface defects compromise MOSFET mobility values due to Coulomb scattering effects. Annealing of the defects is not as straightforward as for the $SiO_2$/Si case, as there are greater thermal budget constraints on high-*k* oxides. For example $HfO_2$ tends to crystallize at temperatures as low as $350^{o}C$ to $500^{o}C$. Any roughening at the interface due to thermal degradation will also deleteriously affect mobility.

It was indeed a remarkable feat that Intel overcame many of the engineering obstacles with the introduction of their 45 nm node device, incorporating $HfO_2$ in the MOSFET gate stack which became the first high-$k$ material used in mainstream CMOS manufacture. One point to make in this regard is that it was found that a very thin $SiO_2$ layer was required at the interface between the Si and the $HfO_2$, see Figure 1.4. The incorporation of this layer was deemed necessary to offset some of the aforementioned issues. This means the interface is still effectively $SiO_2$ on Si, which negates some of the mobility reduction introduced by high-$k$ due to surface roughening, Coulomb scattering due to interface defects, and remote phonon scattering due to defects in the high-$k$ film.[7] However this now raises one of the main concerns originally mooted for high-$k$, ie. whether the scaling benefits would last for more than one technology generation. Continued EOT scaling requires thinning of the $HfO_2$ and this $SiO_2$ interlayer, yet the screening benefits of the interlayer are inhibited with reducing thickness. Therefore some opinion formed in the field that while the introduction of high-$k$ was a stepping stone, an even more drastic step in terms of material composition was needed.
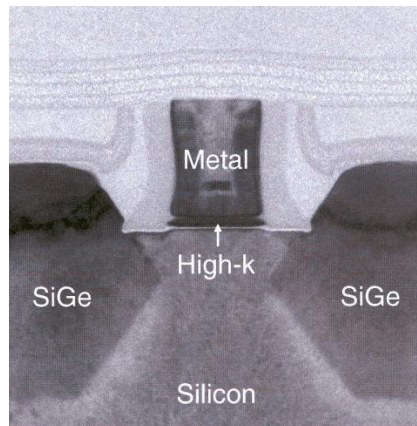


Figure 1.4 SEM image showing the device structure for the 45nm node device introduced by Intel in 2007, the first device in mainstream CMOS manufacture incorporating a high-$k$ dielectric. The device also utilized a metal gate, and a thin $SiO_2$ layer is visible between the $HfO_2$ high-$k$ layer and the Si channel.[8]

## 1.4. High mobility semiconductors

Some of the critical requirements for future generations according to the International Technology Roadmap for Semiconductors (ITRS) were summarized in a recent review article by Thayne *et al.*.[9, 10] Given the stringent criteria for device performance beyond the 15 nm technology generation it is foreseen that replacing silicon with high mobility channels will be the next major materials revolution. Using high mobility channel materials allows for a reduction in operating voltage, leading to reduced power dissipation, and their incorporation potentially combats some of the mobility reductions mentioned previously for high-*k*/Si systems. Therefore in recent years, materials with a higher mobility than Si have been researched as the channel layer for future MOSFET design. Table 1.1 summarizes the electron and hole mobilities for a range of semiconductor materials. For the case of *n*-channel devices, high electron mobility is desirable, with GaAs among the materials fulfilling this requirement and in the case of $In_{0.53}Ga_{0.47}As$ the increase is around one order of magnitude when compared to Si. It is notable that the hole mobility of $In_{0.53}Ga_{0.47}As$ is not exceptional, which is one of the reasons why Ge is also under consideration for use as a *p*-channel, with its hole mobility being over four times higher than that of Si. Therefore one potential approach to maintain the scaling roadmap is the heterogeneous integration onto a silicon platform of these high mobility semiconductors, using Ge for *p* channel devices and III-V compound semiconductors for the complementary *n* channel devices. As the work presented in this thesis is conducted primarily for devices incorporating oxides on GaAs and $In_{0.53}Ga_{0.47}As$ surfaces, the discussion here will focus on these materials.

| Material | Si | Ge | GaAs | $In_{0.53}Ga_{0.47}As$ | InAs | InSb |
|---|---|---|---|---|---|---|
| Electron Mobility ($cm^2$/Vs) | 1400 | 3900 | 8500 | 14000 | 40000 | 78000 |
| Hole mobility ($cm^2$/Vs) | 450 | 1900 | 400 | 300 | 500 | 850 |

Table 1.1 Electron and hole mobilities for a number of semiconductor materials

### 1.5. Challenges for incorporation of high-*k* on III-V

One of the primary challenges with regard to incorporation of high-*k* materials on III-V semiconductors is that there tends to be a high density of defects at the interface of the dielectric and the semiconductor, with the majority of studies reporting values in excess of $10^{12}\,cm^{-2}eV^{-1}$, compared to ~ mid-$10^{10}\,cm^{-2}\,eV^{-1}$ for $SiO_2$/Si. Unfortunately, there are no beneficial native oxides on III-V. As already discussed, the incorporation of high-*k* on Si was fraught with difficulties at the interface, which were not entirely resolved as Intel incorporated a $SiO_2$ layer in their 45nm technology. The problem is now even more complicated in that you have a high-*k* layer in contact with a compound semiconductor. If you compare for example the ideal case of a $SiO_2$ on Si interface with that of one comprised of $HfO_2$ on $In_{0.53}Ga_{0.47}As$, you venture from a materials system where two elements are present to one where you have five distinct elements, and therefore a far greater propensity for defect formation.[11] Competition between these elements leads to a greater range of potential interfacial oxides at the high-*k*/III-V interface. Formation of multiple oxide states, some of which are unstable are thought to be one of the main contributors to the poor interfacial properties observed for this materials system.

The level of $D_{it}$ observed historically for devices incorporating dielectrics on GaAs, being over two orders of magnitude higher than that for $SiO_2$/Si systems, has typically meant that it is not possible to modulate the Fermi level to achieve free movement of charge carriers within the GaAs channel layer. Note that more specific discussion of electrical characteristics of devices relevant to this thesis work is presented in Chapter 2. Despite over three decades of research, even at the time of writing relatively few studies have demonstrated acceptable results for dielectrics on GaAs. Callegari *et al* observed an improvement for MOS devices by using a plasma clean treatment on the GaAs surface and then depositing a gallium oxide film by e-beam evaporation.[12] Passlack *et al* deposited a $Ga_2O$ layer on GaAs by molecular beam epitaxy (MBE).[13] However, deposition approaches such as e-beam and MBE are not particularly suited for expansion to a full manufacturing process.

More recently the incorporation of amorphous silicon (*a*-Si) capping layers has shown promising results.[14, 15] DeSouza *et al* performed a study using different techniques to deposit the *a*-Si layer, e-beam evaporation, MBE, and plasma enhanced chemical vapor deposition (PECVD). Significantly this was only successful using the PECVD method, which is notable for being a hydrogen rich environment. Therefore it was surmised that hydrogenation of the surface was key to the improved electrical characteristics. As mentioned before H based anneals such as forming gas annealing are routinely used for Si based devices. Hinkle *et al*, using a similar PECVD *a*-Si layer on GaAs, attempted to correlate an improvement in the electrical characteristics with physical characterization of oxide species at the interface via X-Ray Photoelectron Spectroscopy (XPS). Such correlation of electrical and physical properties is far from trivial, but can help provide valuable understanding of high-*k*/III-V interfaces, and remains an area somewhat under-explored in the literature. It is worth stating that achieving comparable results with high-*k* layers deposited on GaAs in the absence of the interlayers mentioned above remains elusive.

With regard to $In_xGa_{1-x}As$, lower indium content films (x<0.53) are usually formed by epitaxial growth on GaAs, while higher indium content layers (x≥0.53), such as $In_{0.53}Ga_{0.47}As$, are typically grown on InP by employing metal organic vapour phase epitaxy (MOVPE).[16] The latter has garnered much favour in research over the last number of years as $In_{0.53}Ga_{0.47}As$ can be grown lattice matched to the underlying InP, and this results in high-quality epitaxial layers with a low density of structural defects. Additionally MOVPE is viewed as being more suitable than MBE for large scale wafer production.

Various techniques have been used in an attempt to passivate the high-*k*/$In_xGa_{1-x}As$ interface. A common approach due to its relative simplicity is to use wet chemical treatments to remove native oxide species prior to deposition of the dielectric. A wide range of wet chemical solutions have been employed: dilutions of ammonium hydroxide ($NH_4OH$) in either HCl or water[17, 18]; acid cleans such as sulphuric ($H_2SO_4$), hydrofluoric (HF), and hydrochloric (HCl)[19]; and aqueous solutions of ammonium sulfide, $(NH_4)_2S$, which was frequently used in the past for

InP and GaAs has become one of the most popular solution based passivation methods.[20, 21, 22] Another technique has been to flow hydrogen sulfide ($H_2S$) gas over the $In_{0.53}Ga_{0.47}As$ surface at the end of MOVPE growth in an effort to passivate the surface using atomic H and S.[23] Obviously, given that subsequent oxide deposition is performed ex-situ following the aforementioned treatments, the efficiency of the passivation can be compromised somewhat by the exposure to ambient conditions during the transfer to the oxide deposition system.

A rather different approach has been to deposit interface passivation layers on $In_{0.53}Ga_{0.47}As$ prior to ALD of the high-$k$, in an attempt to suppress formation of oxides on $In_{0.53}Ga_{0.47}As$ and to yield an improved interface compared to that of high-$k$ directly on $In_{0.53}Ga_{0.47}As$. In that vein, groups have also adopted the $a$-Si passivation layers mentioned earlier for GaAs for use in their $In_{0.53}Ga_{0.47}As$ devices. [24,25, 26] Other groups have utilized "capping" layers, which are deposited in-situ after the $In_{0.53}Ga_{0.47}As$ epitaxial growth and thus are designed to prevent any oxidation and preserve the integrity of the surface. InP is one such capping layer that has been deposited in-situ after $In_{0.53}Ga_{0.47}As$ growth.[27] These thin InP layers have a suitable bandgap, prevent uncontrolled oxidation of the $In_{0.53}Ga_{0.47}As$ surface, and also have the benefit of moving the critical interface so that carriers in the $In_{0.53}Ga_{0.47}As$ channel are less susceptible to the influence of defects. Zhao *et al.* reported an improvement in $In_{0.53}Ga_{0.47}As$ MOSFET characteristics on inclusion of a 4nm thick InP capping layer. Intel have also reported the use of a 2nm InP capping layer on a $In_{0.7}Ga_{0.3}As$ channel.[28] A slight variant on this idea has also been used whereby a sacrificial arsenic capping layer is formed at the end of the InGaAs epitaxial growth. This is subsequently desorbed in-situ at high temperature in the same chamber used for dielectric deposition.[29, 30,31]

While a wide variety of high-$k$ dielectrics have been examined, such as $HfO_2$[22, 23], $LaAlO_3$[29], $Si_3N_4$[32,33], $Ga_2O_3/Gd_{0.25}Ga_{0.15}O_6$[34], and $Sr_2TaO_6$[35], $Al_2O_3$ has emerged as one of the most heavily investigated oxide layers for both GaAs and $In_{0.53}Ga_{0.47}As$. One of the main reasons for the focus on $Al_2O_3$ is due to the reported "self-cleaning" effect during ALD deposition of $Al_2O_3$ from the $Al(CH_3)$, (trimethylaluminium,

TMA) precursor. Numerous reports in the literature indicate that growth of $Al_2O_3$ using TMA evidently results in either the removal of interfacial oxide species, or their conversion to $Al_2O_3$ during the ALD process.[36, 37, 38] One of the contributory factors to this is thought to be the reactivity of the TMA precursor itself.[39] By contrast this is not observed using the most common precursors used for ALD deposition of $HfO_2$ on III-V, and therefore some interfacial oxide layers typically remain. As a consequence electrical characteristics indicate a higher $D_{it}$ for similar devices utilizing $HfO_2$ compared to $Al_2O_3$. Although the dielectric constant of $Al_2O_3$ is relatively modest (in the range 7 to 9), its potential to from a good interface with III-V semiconductors has sustained interest in its use. Indeed recently, one route to compensate for the *k*-value of $Al_2O_3$ in order to achieve the EOT scaling necessary has been to use a bi-layer gate stack, whereby a thin $Al_2O_3$ layer is used to improve the interface and a higher dielectric constant material such as $HfO_2$ is then deposited for EOT scaling purposes.[40, 41]

## 1.6. Co-integration of Ge and III-V materials on a Si based platform

As mentioned earlier a possible evolution for CMOS is utilizing III-V materials for *n*-channel devices and Ge for *p*-channel devices. For economic and practical reasons it will be necessary to combine the benefits of these new materials with well-established Si manufacturing processes, requiring co-integration of Ge and III-V FETS on the same Si substrate. The use of large diameter Si wafers is cost effective, and realistically the new technologies must fit in with the existing Si based manufacturing platform to make use of the extensive tool set developed by industry in this regard. Co-integration of III-V and Ge on Si poses difficulties perhaps as significant as any other for their viability as a future materials system. III-V materials in particular differ significantly from Si with regard to crystal structure, lattice properties, and coefficient of thermal expansion. It is envisaged that Ge and $In_xGa_{1-x}As$ (x > 0.53) active areas will be co-integrated at a nanometer lateral scale on the same large size Si wafer (300 or 400 mm). Different methods are being considered to obtain such

hybrid substrates, be it with selective epitaxy, also called aspect ratio trapping,[42] or with direct wafer bonding.[43, 44] The differing thermal stabilities of Ge, $In_xGa_{1-x}As$, and Si, come into play regardless of which method is used. The melting point of Ge is for example about 940°C, 500°C lower than silicon, and $In_xGa_{1-x}As$ tends to decompose above 600°C. This potentially introduces tremendous processing complexity in that anneals intended for either Ge $p$-FET or $In_xGa_{1-x}As$ $n$-FET must be compatible in order to not exceed the thermal tolerance of the other material. It is possible that techniques such as milli-second annealing will therefore also be a key technology to enable the co-integration of Ge and $In_xGa_{1-x}As$. Some progress is being made in this area, as evident in a recent report by Czornomaz $et$ $al.$ of IBM,[44] see Figure 1.5 below. The nanoscale co-integration of such materials with differing lattice constants and thermal budget constraints, while maintaining a sufficiently low density of structural defects remains one of the most significant challenges in this field.
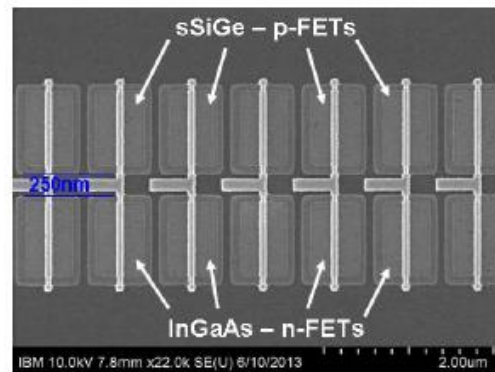


Figure 1.5 Top-view SEM image from the work of Czornomaz $et$ $al.$[44] at IBM showing dense co-integration of co-planar nano-scaled SiGe based $p$-FETs and InGaAs based $n$-FETs on a Si substrate.

## 1.7. Use of novel device architectures

It is worth briefly mentioning that in addition to the increasing movement towards incorporation of new materials, there is also large effort being invested in the design of new transistor architectures in the drive for continued scaling. In a recent review article, Thayne *et al*[16] described some of the alternative architectures being investigated for planar III-V devices and described some of the considerations justifying these approaches.
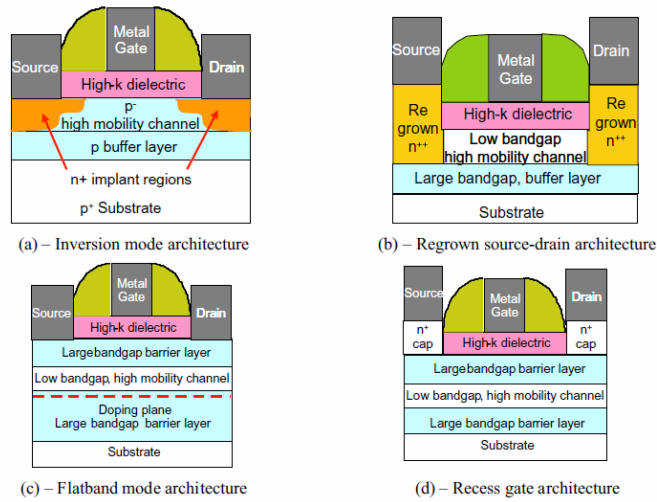


Figure 1.6 A sample of some of the device architectures reported in the literature for III-V based devices, as discussed by Thayne *et al.*[16]

Even for Si-based devices, Intel has already moved away from the traditional two-dimensional, planar MOSFET design to the use of a three-dimensional (3-D) multiple gate architecture they introduced at the 22nm node in 2011.[45] These so-called Tri-gate devices offer improved electrostatic control compared to their planar counterparts, while the tradeoff to be overcome in this case was that the introduction of such a device architecture obviously entailed very significant design complexity as well as manufacturing challenges.[46] Figure 1.7 shows a schematic of a Tri-Gate architecture, alongside which an SEM of a processed device shows the gate and fin structures. A number of groups have also recently explored using such 3-D architectures for III-V channel materials.[47,48]
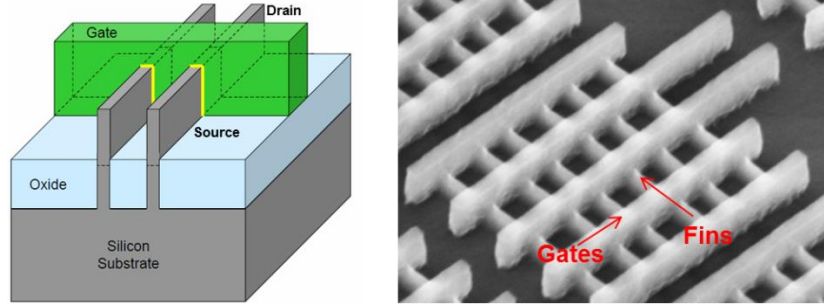
Figure 1.7 Schematic of device structure and SEM showing gates and fins in an Intel Tri-gate 22nm node device.[49]

## 1.8. Thesis Outline

As mentioned in the previous section there are a range of challenges associated with the incorporation of III-V based channel materials into a CMOS process. The research work described in this thesis is focused on the high-$k$/In$_x$Ga$_{1-x}$As gate stack, and covers issues associated primarily with the characterization, understanding, and control, of electrically active interface defects.

The electrically active interface defects are investigated through the fabrication and characterization of MOS devices incorporating high-$k$ dielectrics on III-V semiconductors. As alluded to earlier, MOS capacitors serve as ideal test structures to evaluate a number of passivation methods designed to reduce D$_{it}$ at the high-$k$/III-V interface. This includes techniques to passivate the III-V epitaxial surface prior to ALD deposition of the high-$k$, and annealing performed after gate metal deposition. Obviously MOS devices can be fabricated more quickly and easily than MOSFETs, which typically require multiple process flows, and this enables MOS devices to be used to efficiently screen numerous passivation approaches. In addition, analysis of MOS structures allows some understanding of the fundamental behavior of the high-$k$/III-V system in the absence of any complicating effects on device performance that are introduced during the multiple processing steps inherent in a MOSFET fabrication

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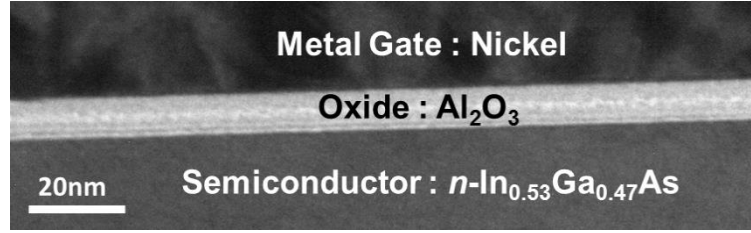
Figure 1.7 Transmission Electron Spectroscopy (TEM) image of a Ni/Al$_2$O$_3$/$n$-In$_{0.53}$Ga$_{0.47}$As, Metal-Oxide-Semiconductor (MOS) structure, typical of that explored in this thesis.

flow. Obviously it is important that the results obtained on MOS devices be relevant in a wider context. An MOS stack is at the heart of a traditional MOSFET device so therefore improvements observed for MOS devices should ideally be transferable to related MOSFET devices. A cross sectional transmission electron microscopy (TEM) image of a typical gate stack structure examined in this thesis is shown in Figure 1.7.

In Chapter 2 some basic theory is presented to provide an overview of the electrical characteristics expected for a MOS system. This encompasses the responses for an ideal system, and also a description of the effect of various defects and oxide charges on device electrical characteristics. An emphasis is placed on the non-idealities and electrical characterization methods most relevant to the discussion of the experimental MOS devices in the subsequent chapters of the thesis.

In the first experimental chapter of the thesis [Chapter 3], the effect of varying the % indium composition in the In$_x$Ga$_{1-x}$As (x: 0, 0.15, 0.30, 0.53) semiconductor epitaxial layer was investigated. From a technological perspective there is an interest to examine In$_x$Ga$_{1-x}$As channels with varying indium concentrations, as a higher indium concentration increases the electron mobility, however, it also reduces the band gap, which can increase off-state currents. From a scientific perspective, how D$_{it}$ values change with the indium percentage is also of interest, as it is possible that certain interface defects will move out of the In$_x$Ga$_{1-x}$As energy gap with increasing indium content. For the samples in this study, HfO$_2$ films served as the high-$k$ gate oxide. Devices were characterized over a wide temperature range, 77K to 295K, to examine the influence of interface defects on the electrical response of the MOS

devices as the bandgap varies with % indium content. Additionally, the effect of forming gas annealing on defect densities at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface was examined.

The experimental results and analysis in Chapter 3, indicated that with ALD based high-$k$ oxide deposition it was only possible to achieve a genuine surface accumulation in $n$-$In_xGa_{1-x}As$ MOS with 53% indium, and as a consequence the remainder of the thesis work focused primarily on utilizing $In_{0.53}Ga_{0.47}As$ as a semiconductor layer. A common passivation technique used for III-V surfaces is immersion in an ammonium sulfide solution, and a study was performed to investigate the effect of varying the passivation parameters [Chapter 4]. Various concentrations of $(NH_4)_2S$ were used and the optimum condition was assessed based on the electrical and physical characteristics of the devices. In addition a comparison was performed of the Conductance Method and the High-Low Capacitance Voltage Method to compare the $D_{it}$ extracted using the two approaches.

Further optimization of the passivation technique was used to fabricate MOS devices, again incorporating $Al_2O_3$ on $In_{0.53}Ga_{0.47}As$, where $D_{it}$ values were reduced to levels allowing genuine surface inversion to be achieved in both $n$ and $p$ type $In_{0.53}Ga_{0.47}As/Al_2O_3$ MOS. Techniques developed by Nicollian and Brews[50] were used to analyze the signatures of, and mechanisms for, the minority carrier response observed over $n$-type and $p$-type substrates in inversion [Chapter 5]. In addition the effect of the $In_{0.53}Ga_{0.47}As$ epitaxial doping concentration on the inversion responses was studied through use of $n$- and $p$-type $In_{0.53}Ga_{0.47}As$ with doping concentrations varying over two orders of magnitude.

In Chapter 6 the analysis of the $In_{0.53}Ga_{0.47}As/Al_2O_3$ MOS inversion response was extended on the basis of an experimental observation indicating a unique relationship between the capacitance and conductance in strong inversion [Chapter 6]. This chapter also indicates how these new observations can have a practical application to the extraction of the oxide capacitance ($C_{ox}$), which can be particularly challenging in the case of $In_{0.53}Ga_{0.47}As$ based MOS structures. The effect of $t_{ox}$ and FGA on the

minority carrier responses was also studied. Finally, the main findings of the thesis are summarized with some suggestions on possible future work [Chapter 7].

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# Chapter 2

## 2. Charged defect components in the MOS system: Influence on the capacitance-voltage and conductance-voltage response, and methods for defect density quantification

### 2.1.    Introduction

The aim of this chapter is to provide a brief overview of the electrical characteristics of MOS devices, both in terms of the behaviour expected in the ideal case and the influence of defects and charges in the system. There are a vast number of textbooks explaining the physics of MOS devices in great detail.[1,2,3,4,5] Therefore, the intention here is not to replicate this theory but to present a selected number of points salient to the analysis presented later in this thesis on the experimental samples. The samples in the thesis are examined primarily through electrical measurements of the capacitance and conductance responses of MOS devices as a function of the applied gate bias, signal frequency, and temperature. This allows the characterization of some non-idealities that can affect the electrical performance, primary among these being defects at the interface between the dielectric and the semiconductor, fixed charges in the oxide bulk, and so-called border-traps which are charge trapping sites in the oxide in proximity to the semiconductor.

### 2.2.    Capacitance-Voltage Response of MOS capacitors

Figure 2.1 shows a schematic representation of the ideal CV response associated with the primary modes of MOS capacitor operation, ie, accumulation, depletion, and inversion. The corresponding energy band diagrams are also shown with an
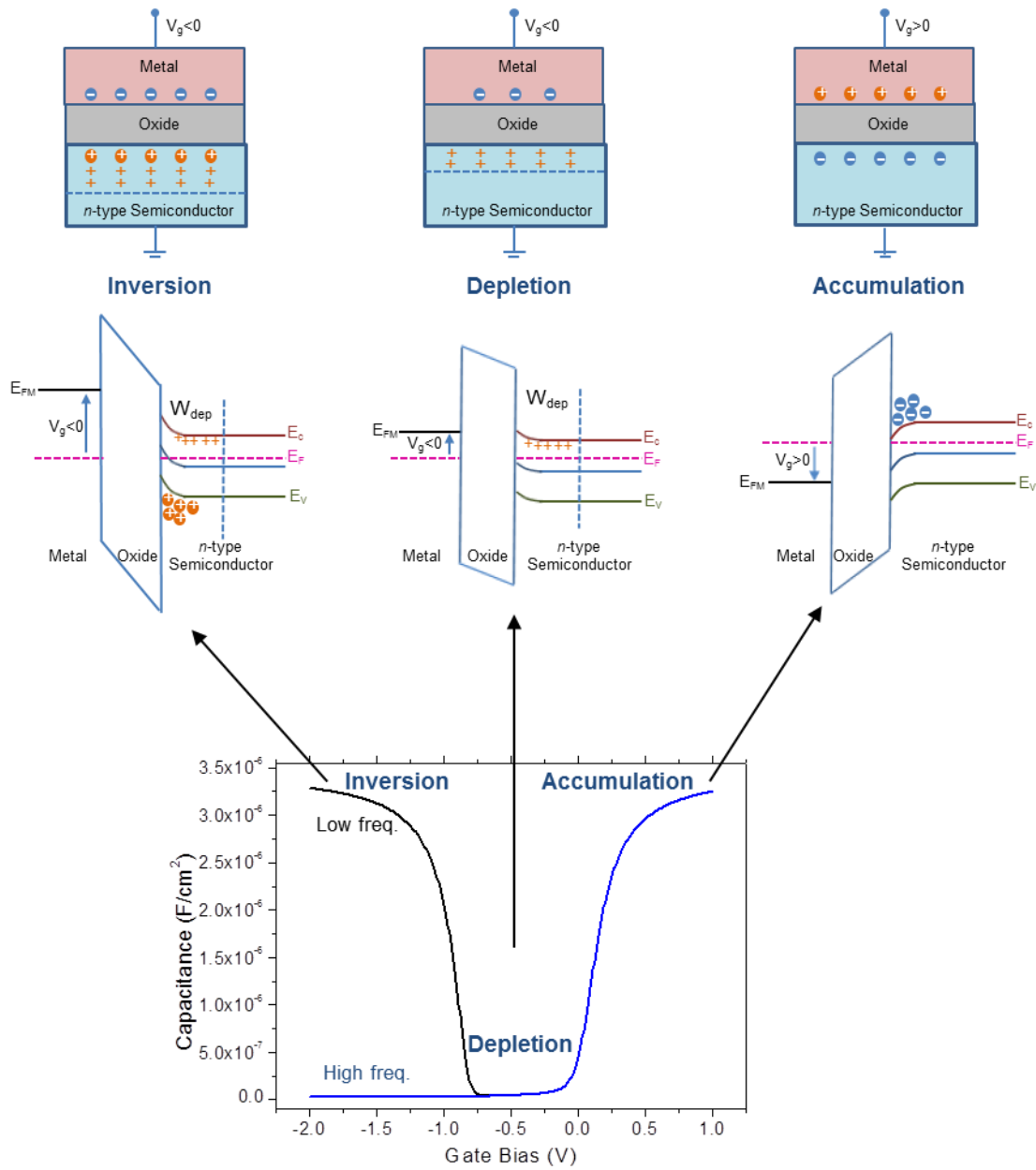
Figure 2.1: *Top*: Illustrative schematic of MOS device structure indicating charges under the gate with different gate bias conditions. *Middle*: Corresponding energy band diagrams illustrating band bending in the MOS system. *Bottom*: Curve illustrating the Capacitance-Voltage response associated with three primary modes of MOS device behavior, ie. accumulation, depletion, and the high and low frequency response in inversion.

illustration of the charges under the gate stack for each condition. The case shown is for an *n*-type semiconductor layer. When the layers are brought into contact with each other, band bending occurs at the semiconductor-oxide interface due to differences in the work functions of the metal and semiconductor. The application of a positive gate bias attracts electrons to the semiconductor surface, resulting in accumulation of majority carriers at the interface. When the gate bias is reduced to a negative value the bands will begin to bend in the opposite direction, marking the onset of depletion. With further reduction in gate bias, more holes are attracted to the semiconductor surface, with this population of minority carriers leading to the inversion regime.

## 2.3. Simulated CV response: Effect of interface defect states, oxide charge and border traps

Typically, experimental MOS devices are characterized by applying a direct current (DC) bias to the capacitor structure, with a small signal alternating current (a.c) signal superimposed. The frequency of this ac signal can then be varied to examine the frequency dependent characteristics of the device. This is particularly relevant to defects at the oxide-semiconductor interface, normally referred to as interface defects, which have a strong dependence on the frequency of the applied signal, and also on measurement temperature. The influence of such defects on the electrical performance of devices will depend on their characteristic peak energy and distribution with respect to the semiconductor bandgap.

Figure 2.2 presents simulated multi-frequency CV curves for an *n*-type Si MOS. Although the case presented is for Si the same general theory is relevant for III-V semiconductors. These simulation results were performed utilizing a Synopsys Sentaurus Device Simulator. Figure 2.2 (a) shows the CV profiles expected assuming zero contribution from interface states, fixed oxide charges, or border traps, in the MOS system. In the accumulation region, ideally no dispersion is observed with variation in the a.c signal frequency, and there is a steep transition into depletion. In

the inversion region, one sees the CV initially rise and then plateau with increasing negative gate bias. The value of the capacitance in this plateau region reduces with increasing frequency, approaching a minimum capacitance at high frequency. In real devices this frequency dependent behavior is due to generation and supply of minority carriers through mid-gap defects in the bulk of the semiconductor. Note that
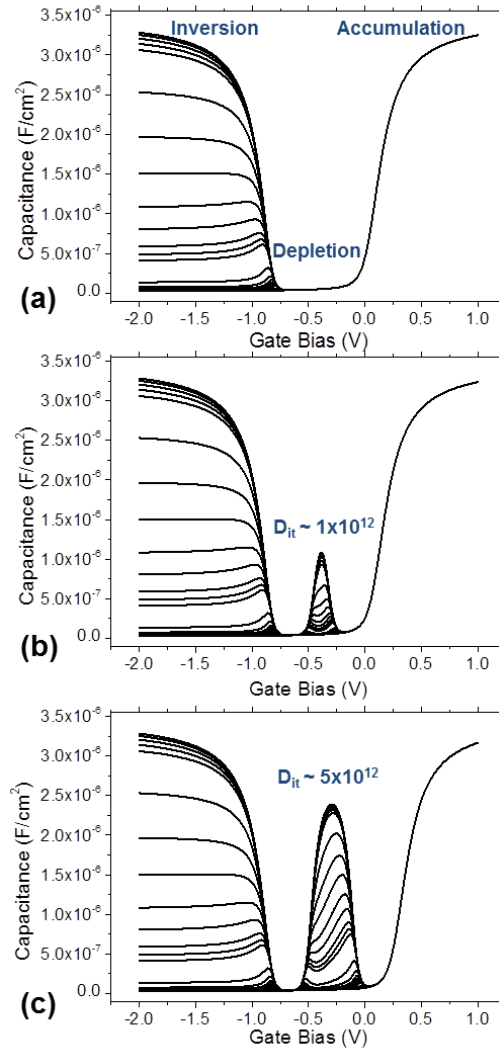


Figure 2.2 Simulated multi-frequency (100Hz to 1MHz) CV characteristics for an $n$-type Si MOS device. The simulation parameters assumed a 1nm EOT, a doping of $1x10^{16}cm^{-3}$, and a minority carrier generation lifetime of 10pS. The simulation results were provided by Dr. Rafael Rios, of Intel Components Research, who utilized a Synopsys Sentaurus Device Simulator.

in modern Si the quality of the semiconductor results in a low density of defects with the result that the minority carrier generation lifetime is typically high ($\sim\mu$s), and therefore an increase in inversion capacitance is not observed at frequencies normally used in practical measurement conditions, being 20Hz to 1MHz. However the generation lifetime input to the simulation has been reduced here ($\sim$ ps) for illustrative purposes.

Figure 2.2(b) shows simulated CV results with an interface state density of $1\times10^{12}cm^2$, located at a mid-gap energy. The effect of the interface defects having a peak density at a specific energy in the semiconductor bandgap is to cause a distortion in the CV, manifesting as a peak due to a capacitance contribution, $C_{it}$, from charging of the defects. It is noted that even a single energy level defect, as in the simulation, causes a broad frequency dependent feature in the CV response. The reason for this is because the simulation is at room temperature, and the defect occupancy is set by the Fermi-Dirac function. The low frequency capacitance limit of the $C_{it}$ response is $q[dN_{it}/d\phi_s]$ and $N_{it}$ as a function of $\Phi_s$ is set by the Fermi-Dirac function. Therefore, a single energy level defect yields a broad feature in the CV as shown in Figure 2.2 (b). The capacitance will move through a peak as the Fermi level moves through the defect at the oxide/semiconductor interface, and at a sufficiently low frequency, all the defects can follow the ac signal, and the result is a quasi-static CV response of the interface defect. As the frequency increases the ac response of the interface states is suppressed. Additionally, the peak capacitance will occur at a bias closer to the accumulation region with increasing ac signal frequency, if the defect response is primarily associated with majority carriers. This feature can be used to determine if the defect response is primarily interacting with the majority or the minority carriers in the semiconductor. This behavior is also reflected in the conductance-voltage (GV) responses (not shown). Figure 2.2 (c) shows the effect of increasing the $D_{it}$ to $5\times10^{12}cm^2eV^{-1}$, and the peak response increases accordingly. These simulations are for a single energy level defect. However, if the simulation is based on a Gaussian $D_{it}$ energy distribution peaked about a specific energy, the same salient features are observed in the CV response, the difference being that the voltage range over which the frequency dependent distortion is measured is increased.

It is noted that the bandgap of $In_{0.53}Ga_{0.47}As$ is reduced compared to Si. Therefore for a given Gaussian $D_{it}$ distribution, the energy range of the $D_{it}$ distribution is spread over a larger percentage of the energy gap. If the $D_{it}$ value increases significantly, then it is noted that the distortion associated with the $D_{it}$ response can be smeared, such that it extends into the region of the CV corresponding to the onset of the inversion response. Therefore this results in a complication in differentiating the capacitance contribution due to the $D_{it}$ and that due to inversion of the semiconductor surface. In fact, for the majority of published literature for the $In_{0.53}Ga_{0.47}As$ MOS system, a very high $D_{it}$ has resulted in a situation where it is not possible, within the bias range applied, to move the surface Fermi level past the $D_{it}$ response and therefore surface inversion cannot be achieved.

While interface defects are sensitive to the variation in frequency of the applied ac signal, and measurement temperature, they also affect the CV in their response to the varying DC bias. This typically manifests as a stretch out in the CV as illustrated in Figure 2.3. This compares the high frequency (1 MHz) CV curves for two $Pd/Al_2O_3/n$-$In_{0.53}Ga_{0.47}As$ devices, with an 8nm ALD $Al_2O_3$ layer, which are nominally identical except that in one case the $In_{0.53}Ga_{0.47}As$ surface was left
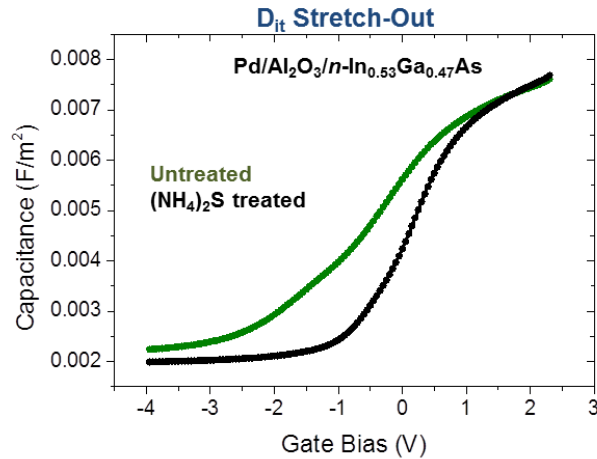


Figure 2.3 Comparison of the stretch-out in the measured 1MHz high-frequency CV due to $D_{it}$ response to DC gate bias. One of the $Pd/Al_2O_3/n$-$In_{0.53}Ga_{0.47}As$ devices deliberately received no surface passivation prior to ALD to generate a higher level of $D_{it}$ in the sample. The $Al_2O_3$ is 8nm thick.

untreated prior to ALD, and in the other case the $In_{0.53}Ga_{0.47}As$ surface received a $(NH_4)_2S$ passivation. The untreated sample has, as expected, higher levels of $D_{it}$ than the $(NH_4)_2S$ treated sample, which is also reflected in the multi-frequency CV and GV (not shown). The $D_{it}$ response as a function of DC gate bias is better compared at high frequency (1MHz) where the interface states do not have time to respond to the ac signal frequency. Therefore the increased stretching of the CV along the gate voltage axis for the untreated sample can be attributed to the filling or emptying of interface states with the slow variation in DC bias on the gate, due to higher $D_{it}$ in this device. It is noted that any charge trapping in defects within the oxide, will also result in a CV stretch out along the gate voltage axis, so this method cannot distinguish between interface states and defects in the oxide which can trap charge. High levels of $D_{it}$, and of defects located within the interfacial transition layer between the semiconductor and the bulk oxide, is a common issue in general for III-V devices. It is noted that in the experimental data in Figure 2.3, the $D_{it}$ distribution will not be a mono-energetic level, as shown in the examples in Figure 2.2, but will most probably result from a distribution of $D_{it}$ across the energy gap. Another consideration with regard to measuring III-V devices is that this stretch-out effect must be factored in to the bias range selected for the CV measurement, particularly where $D_{it}$ is present, and even more critically for lower EOT devices. This is because selecting too wide a DC bias range can in fact degrade the samples and increase the observed stretch-out, thus distorting interpretation of the results.

Charge within the oxide layer which does not respond to the applied gate bias is termed fixed oxide charge. This is usually identified via a parallel shift in the CV characteristic along the gate voltage axis, with the direction of the shift being opposite in polarity to the charge type, ie. a positive shift in voltage corresponds to negative fixed oxide charge. Frequently anneals are used to attempt to remove such charge from oxide films. As a practical example, Figure 2.4 compares the 1MHz CV curves for the same $Au/Ni/Al_2O_3/n$-$In_{0.53}Ga_{0.47}As$ device both prior to and following a $275^{o}C$ anneal in forming gas (FGA). The pre-FGA curve is negatively shifted compared to
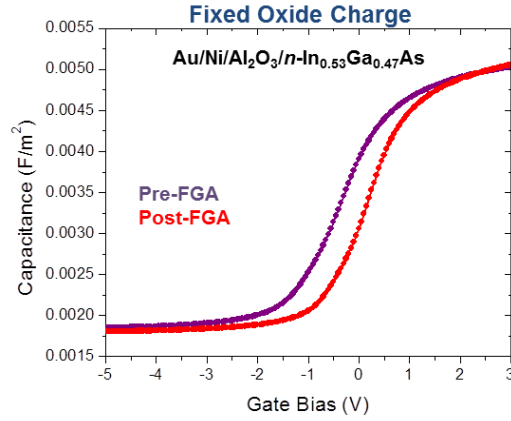
Figure 2.4 Comparison of the measured 1MHz high-frequency CV prior to and following FGA of the same Au/Ni/Al$_2$O$_3$/$n$-In$_{0.53}$Ga$_{0.47}$As sample. The pre-FGA curve is negatively shifted compared to that post-FGA, indicating removal of positive fixed charge during the anneal. The Al$_2$O$_3$ is 12nm thick. The FGA was performed post-gate metallization (275$^o$C, 30 mins).

the CV post-FGA, indicating removal of positive fixed charge during the FGA process.

A further consideration is the presence of charge trapping sites in the gate oxide, arising from defects within the oxide layer. These are referred to as so-called "border traps" and have energies aligned with the valence and conduction bands of the semiconductor such that they can communicate with these bands via a tunneling
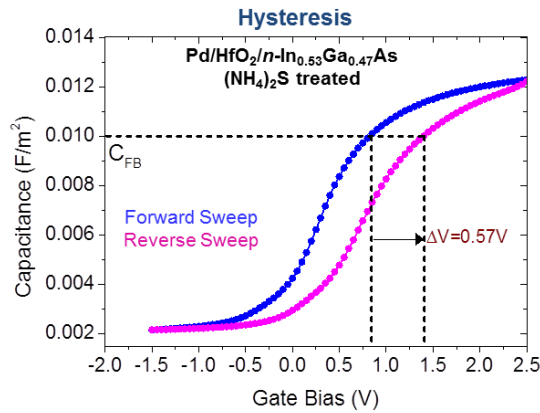


Figure 2.5 1MHz bi-directional CV sweep for a Pd/HfO$_2$/$n$-In$_{0.53}$Ga$_{0.47}$As sample. Clockwise hysteresis of ~ 0.57V is measured around the flatband voltage in this case.

process. Injection of electrons or holes from the substrate or the gate can occur into these charge trapping sites in the oxide. This can manifest as hysteresis due to trapping or de-trapping of charge in these defects.[6] In order to measure hysteresis, usually a bi-directional sweep of the gate bias is performed. The charge trapping or de-trapping is related to the observed shift between the CV curve generated from the forward and reverse sweeps. An example is shown above in Figure 2.5 for a Pd/HfO$_2$/$n$-In$_{0.53}$Ga$_{0.47}$As device. Additionally, in recent literature reports some of the frequency dispersion in the accumulation region for In$_{0.53}$Ga$_{0.47}$As devices has been attributed to these border traps.[7] Figure 2.6 shows a multi-frequency CV response for a Pd/Al$_2$O$_3$/$n$-In$_{0.53}$Ga$_{0.47}$As device. Stretch out is observed as in Figure 2.3 for the same sample, as well as a D$_{it}$ response typical of that observed for $n$-In$_{0.53}$Ga$_{0.47}$As at negative gate bias. There is also a noticeable dispersion of accumulation capacitance with frequency, and it is thought that a contributor to this is a tunneling process whereby border traps having energy levels aligned with the In$_{0.53}$Ga$_{0.47}$As conduction band allows tunneling of carriers into and out of these traps, as indicated by the schematic in Figure 2.6. Given it is a tunneling process this is exponentially dependent on the distance of any such traps from the interface, and also the process should be temperature independent.
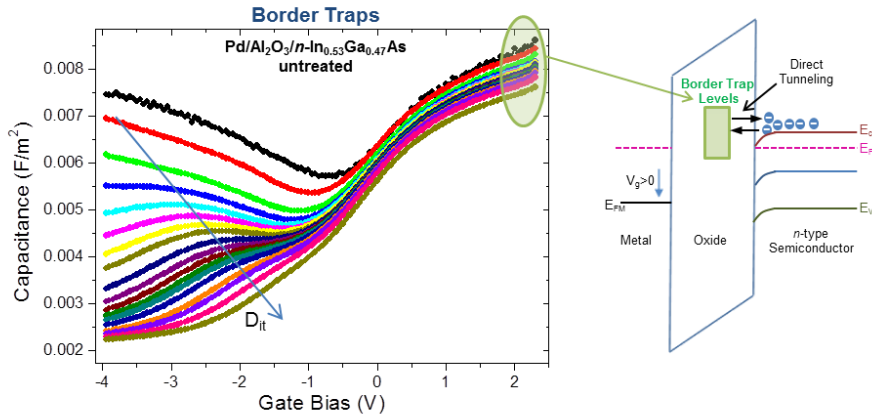


Figure 2.6 Multi-frequency CV (1kHz to 1MHz) for a Pd/Al$_2$O$_3$/$n$-In$_{0.53}$Ga$_{0.47}$As sample, which received no In$_{0.53}$Ga$_{0.47}$As surface passivation pre-ALD. On the right-hand side is a schematic of a band diagram, showing the mechanism for direct tunneling of electrons in and out of border traps in the oxide, thought to be a contributing factor to the observed dispersion of capacitance with frequency in the MOS device.

## 2.4. The effect of very high $D_{it}$ level on the MOS CV response

As alluded to in the previous chapter, historically it has been an enormous challenge to produce devices incorporating GaAs as a channel layer with acceptable electrical characteristics. Due to the high levels of $D_{it}$ for such structures a very pronounced frequency dispersion is routinely observed, an example of which is shown in Figure 2.7 for a Pd/Si$_3$N$_4$/GaAs device.[8] The CV at low frequency approaches $C_{ox}$ only because of the high capacitance contribution from interface states, $C_{it}$. As the frequency is increased less interface states respond so the contribution is reduced and at 1MHz the CV is almost flat, which is an indicator that very few free carriers are present and that it is not possible to achieve true accumulation for these devices. Figure 2.8 shows an example of one of the few approaches which has been successful to date in solving this issue. Hinkle *et al* generated samples with and without an amorphous Si interface passivation layer.[9] With the *a*-Si layer behavior more consistent with true accumulation is observed, and as mentioned previously this is thought to be due to hydrogenation of the GaAs surface during PECVD deposition of *a*-Si.
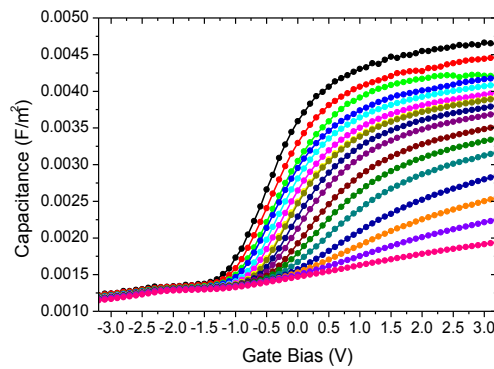


Figure 2.7 Multi-frequency (20Hz to 1MHz) CV responses for a Pd/Si$_3$N$_4$/*n*-GaAs device.
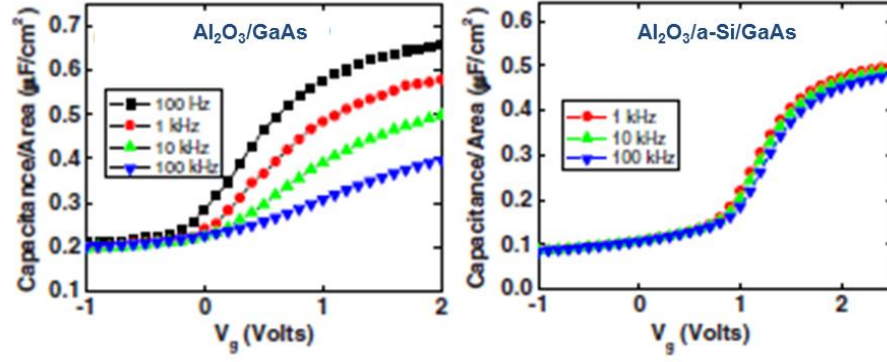
Figure 2.8 Effect of incorporation of PECVD deposited *a*-Si interface passivation layer on accumulation dispersion of $Al_2O_3$/GaAs MOS devices as published by Hinkle *et al.*[9]

## 2.5. Evaluation of $D_{it}$: Conductance Method and High-Low CV Method

A number of different methods have been used to quantify the interface state density in MOS devices, among them being the Terman method, the Conductance method, the Berglund Method, and the High-Low Capacitance method.[4] There remains much discussion in the literature regarding the respective merits or otherwise in applying such methods to high-k/III-V systems. Two of these methods are used in this thesis so further discussion is limited to the Conductance Method and the High-Low method.

The High-Low Capacitance-Voltage method allows extraction of $D_{it}$ just from the measured CV responses of MOS devices. At low frequency it is assumed that the interface traps have time to respond to the slowly changing ac signal and therefore add a capacitance to the measured low frequency CV curve, $C_{LF}$. For this purpose it is worth measuring to as low a frequency as possible in order to maximize the interface state response. By contrast, at high frequencies interface defect states cannot respond in any significant way to the ac signal and therefore they contribute little or no capacitance to the high frequency CV measurement, $C_{HF}$. In both the low and high frequency cases, the interface states respond to the slowly varying DC bias on the gate. As an illustration Figure 2.9 shows the 40Hz and 1MHz CV curves for a Au/Ni/$Al_2O_3$/*n*-$In_{0.53}Ga_{0.47}As$ device, showing a large peak at low frequency

associated with an interface defect response. This $C_{it}$ attributed to interface states can be extracted at each gate bias using Equation [2.1], and the corresponding $D_{it}$ estimation is obtained using Equation [2.2]. As stated by Nicollian and Brews, one of the advantages of using this method is that no assumptions regarding material properties are required, and $D_{it}$ is estimated simply and directly from measured CV curves without the need for simulation. One caveat for employing this method, which is particularly important for narrow band gap materials such as $In_{0.53}Ga_{0.47}As$, is that it will work most effectively where $C_{LF}$ is chosen for a sample where the capacitance associated with the interface state contribution goes through a peak within the gate bias range examined. If the CV does not go through a peak it could be the case that the $D_{it}$ is so high such that the peak value has not been attained and the $D_{it}$ will thereby be underestimated. Further, in the presence of a minority carrier response it is possible that $D_{it}$ could be overestimated, as it becomes difficult to distinguish the $D_{it}$ response from the inversion behavior.

$$C_{it} = \left( \frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left( \frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1}$$ [EQ. 2.1]

$$D_{it} = \frac{C_{it}}{q}$$ [EQ. 2.2]
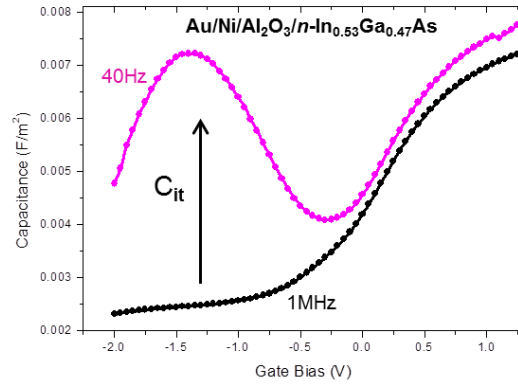


Figure 2.9 Illustration of $C_{it}$ contribution at low frequency for a Au/Ni/Al$_2$O$_3$/$n$-In$_{0.53}$Ga$_{0.47}$As device.

The second method used in the thesis to estimate $D_{it}$ is the Conductance Method.[10] This utilizes conductance losses measured in MOS devices arising from a change in occupancy of interface state defects with variations in the applied ac signal frequency. One can either apply what is known the Full Conductance Method, or an approximation to the Conductance Method. Application of the Full Conductance Method involves measuring the capacitance and conductance at a constant gate voltage while the frequency is swept logarithmically. A voltage range over which to step the gate bias is usually estimated based on where a distortion due to $D_{it}$ is observed in the conventional multi-frequency CV responses. The equivalent parallel conductance ($G_p/\omega$) is estimated from the measured conductance ($G_m$), and measured capacitance ($C_m$) against frequency sweep, for each gate bias point, using equation [2.3] below, where $\omega$ is the fixed angular frequency, and $C_{ox}$ is the oxide capacitance. The equivalent parallel conductance, $G_p$, is converted to peak interface state density using the approximation in Equation [2.4] where $q$ is the electronic charge, and $f_d[\sigma_s]$ is a function of the standard deviation of the surface potential, $\sigma_s$.

$$\left\langle \frac{G_p}{\omega} \right\rangle = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}$$  [EQ. 2.3]

$$D_{it} = \left( \frac{Gp}{\omega} \right) \times \left( \frac{1}{f_d[\sigma_s] \times q} \right)$$   [EQ. 2.4]

The Full Conductance Method also takes into account the profile of the peak through a ratio of the amplitude change of the $G_p/\omega$ curve at the peak frequency, $f_p$, and a point at either $5f_p$ or $0.2f_p$. This is then used to calculate what standard deviation of substrate band bending ($\sigma_s$) is applicable in order to calculate $f_d[\sigma_s]$ for the $D_{it}$ extraction. Figure 2.10 (a) shows $G_p/\omega$ versus $\ln(\omega)$ curves for a *n*-Si device used in development of the technique by Nicollian and Brews.[4] The approach in fitting the peak is also illustrated in Figure 2.10 (b).
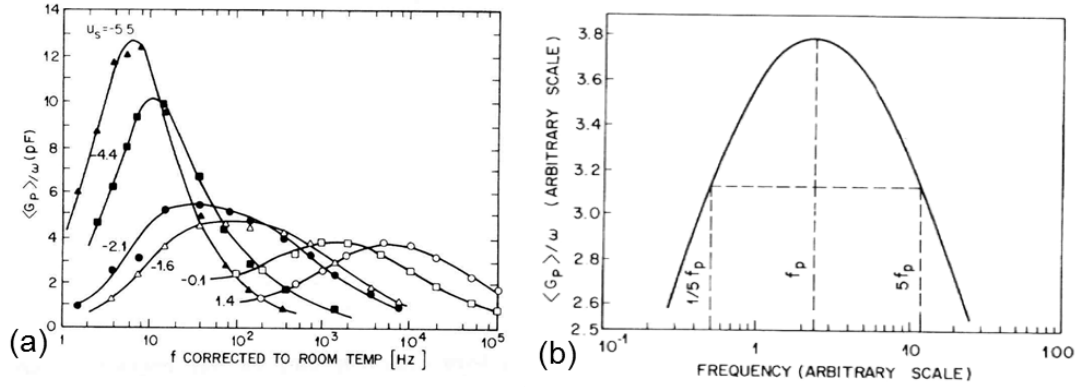
Figure 2.10 (a) $G_p/\omega$ versus $\ln(\omega)$ curves at different gate bias points for a $SiO_2/n$-Si device using the Conductance Mehod as published by Nicollian and Brews.[4] (b) Plot showing how the width and amplitude of the $G_p/\omega$ peak profile is used to estimate standard deviation of band bending for the $D_{it}$ extraction.

For ease of analysis, an approximation to the Conductance Method can also be used to estimate $D_{it}$. In this case zero standard deviation of band bending is assumed yielding a value of 0.4 for $f_d[\sigma_s]$ in Equation [2.4] to estimate $D_{it}$. Also one can also utilize conventional CV and GV measurements where the frequency is fixed and the gate bias is swept. An example of such GV curves is shown in Figure 2.11, and this conductance can also be converted to $G_p$ using Equation 2.3. It is noted that this is consistent with behaviour associated with an interface defect described earlier as indicated by the conductance moving through a peak, with this peak occurring at a gate bias closer to the accumulation region with increasing frequency. One must take into account in this case what bias range the analysis is valid for, and also whether using the full voltage sweeps stresses the devices to affect $D_{it}$. Both the approximation to the Conductance Method and the Full Conductance Method are used at various points in this thesis.

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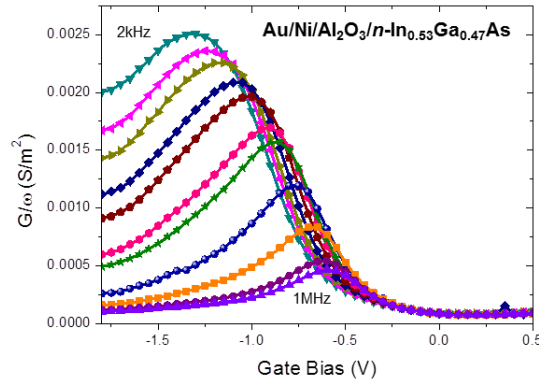
Figure 2.11 Multi-frequency (2kHz to 1MHz) GV reponses for a Au/Ni/Al$_2$O3/$n$-In$_{0.53}$Ga$_{0.47}$As device.

## 2.6. Conclusions

An overview of some of the primary non-idealities present for MOS systems, and their effect on device electrical characteristics was presented. For narrow band-gap semiconductors like In$_{0.53}$Ga$_{0.47}$As the analysis of the device characteristics can be non-trivial, which is complicated by the fact that D$_{it}$ levels are often two orders of magnitude higher than that encountered for Si based devices. In addition, given that understanding of III-V systems is still evolving, one must use caution in the application of techniques established for Si based systems and in the subsequent interpretation and evaluation of high-$k$/III-V device electrical behaviour.

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# Chapter 3

## 3. Temperature and frequency dependent electrical characterization of HfO$_2$/In$_x$Ga$_{1-x}$As interfaces

### 3.1. Introduction

As described in Chapter 1 the interface chemistry for high-$k$ materials on III-V substrates is more complex than that of the SiO$_2$/Si system,[1] with the possibility for more than one substrate element, and its native oxides, to contribute to interfacial defects. The detrimental effect of high interface state density (D$_{it}$) on device characteristics has motivated extensive research on passivation of the high-$k$/III-V interface in an attempt to reduce D$_{it}$.[2, 3,4,5,6,7]

In this chapter the electrical properties of atomic layer deposited (ALD) HfO$_2$ thin films on $n$-type GaAs or In$_x$Ga$_{1-x}$As (x= 0.53, 0.30, 0.15) substrates with Pd metal gates are examined. The motivation for this approach is to assess whether the change of energy gap from GaAs (~ 1.42 eV) to In$_{0.53}$Ga$_{0.47}$As (~ 0.75 eV) is reflected in a change of electrically active interface defects. This is determined through measurement of the Capacitance-Voltage (CV) and Conductance-Voltage (GV) responses of the devices as a function of frequency (1 kHz to 1 MHz) and temperature (77K to 295K). D$_{it}$ analysis for Pd/HfO$_2$/$n$-In$_{0.53}$Ga$_{0.47}$As/InP structures using the conductance method developed for the SiO$_2$/Si system is also presented.[8] The effect of post-metallization low temperature forming gas annealing (FGA) on the electrical properties of Pd/HfO$_2$/$n$-In$_{0.53}$Ga$_{0.47}$As/InP structures is examined.

## 3.2. Experimental Details

HfO$_2$/In$_x$Ga$_{1-x}$As MOS capacitors were fabricated utilizing substrates having the following indium (In) concentrations: 53%, 30%, 15%, and 0% (i.e. GaAs). The In$_x$Ga$_{1-x}$As (x= 0.53, 0.15) epitaxial layers were grown by metal organic vapour phase epitaxy (MOVPE), as was the InP buffer layer, whereas the In$_{0.30}$Ga$_{0.70}$As epitaxial layer and all GaAs layers were grown by molecular beam epitaxy (MBE). In the case of the GaAs (Si: 5x10$^{17}$) sample no subsequent growth of a buffer layer was performed. The details on the In$_x$Ga$_{1-x}$As epitaxial layer thickness and doping concentration, and the thickness and doping of the buffer layers are provided in Table 3.1.

The HfO$_2$ layers were deposited ex-situ in an ALD reactor at 250$^o$C by alternating pulses of H$_2$O and the HfO$_2$ precursor TDMA-Hf (Hf[N(CH$_3$)$_2$]$_4$), the first pulse being that of the Hf precursor. The nominal target thickness for the ALD films was 9 nm. Capacitor structures were completed by vacuum evaporation of ~ 100 nm of Pd (deposition rate ~ 2.5 Å/s) using a lift-off process. Ni, Ge, and Au were deposited, followed by a 350$^o$C, 30s, anneal in N$_2$, to form ohmic back contacts prior

| TABLE 3.1. Substrates and Epitaxial Layer Details | | | |
|:---:|:---:|:---:|:---:|
| **In %** | **Substrate** | **Buffer Layer** | **Epitaxial layer** |
| 53 | InP (100) S: (1-3)x10$^{18}$/cm$^3$ | 0.3$\mu$m InP S: 2x10$^{18}$/cm$^3$ MOVPE | 2$\mu$m, In$_{0.53}$Ga$_{0.47}$As S: 2x10$^{17}$/cm$^3$ MOVPE |
| 30 | GaAs (100) Si: 5x10$^{17}$/cm$^3$ | 0.35$\mu$m GaAs Si: 5x10$^{17}$/cm$^3$ MBE | 50 nm Si: 5x10$^{17}$/cm$^3$ MBE |
| 15 | GaAs (100) Si: 5x10$^{17}$/cm$^3$ | 1$\mu$m GaAs Si: 5x10$^{17}$/cm$^3$ MBE | 30 nm Si: 1x10$^{17}$/cm$^3$ MOVPE |
| 0 | GaAs (100) Si: 5x10$^{17}$/cm$^3$ | ------ | ------- |

to 77K CV measurements. No difference was found in the capacitance dispersion pre- and post-ohmic contact formation, indicating it does not influence the CV characteristics discussed. In the cases where ex-situ three-stage passivation was performed prior to ALD growth the procedure was as follows: 3.7% HCl, 3 minutes at $25^{o}$C; 3% NH$_4$OH, 3 minutes at $25^{o}$C; 1% (NH$_4$)$_2$S, 5 minutes at $75^{o}$C; rinse in deionized water; blow dry wafers with N$_2$.[9] For samples subjected to forming gas annealing (5%H$_2$/95%N$_2$) it was performed cumulatively after gate metallization, at $250^{o}$C and $325^{o}$C for 30 minutes. The capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were recorded using a HP4284A LCR meter. The measurements at room temperature were performed on-wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry air, dark environment (dew point ≤203K). Conventional transmission electron microscopy (TEM) samples were prepared using focused ion beam (FIB) thinning procedures in an FEI 200 Workstation and examined at 200kV in a JEOL 2000FX. Measurements at liquid nitrogen temperatures (~77K) were performed on-wafer in a cryogenic probe station.

### 3.3.  Structural Analysis

TEM analysis was performed on the MOS device stacks to determine the thickness of the HfO$_2$ layer, and to investigate if any interlayer (IL) oxides exist between the III-V substrate and the HfO$_2$ layer. The TEM is also useful in determining whether there is any difference in the quality of the semiconductor epitaxial layers with varying In content. The TEM micrographs presented in Figures 3.1 (a) to (d) are for ALD deposition on the In$_x$Ga$_{1-x}$As native oxides, where no three stage pre-treatment prior to the ALD HfO$_2$ was performed.
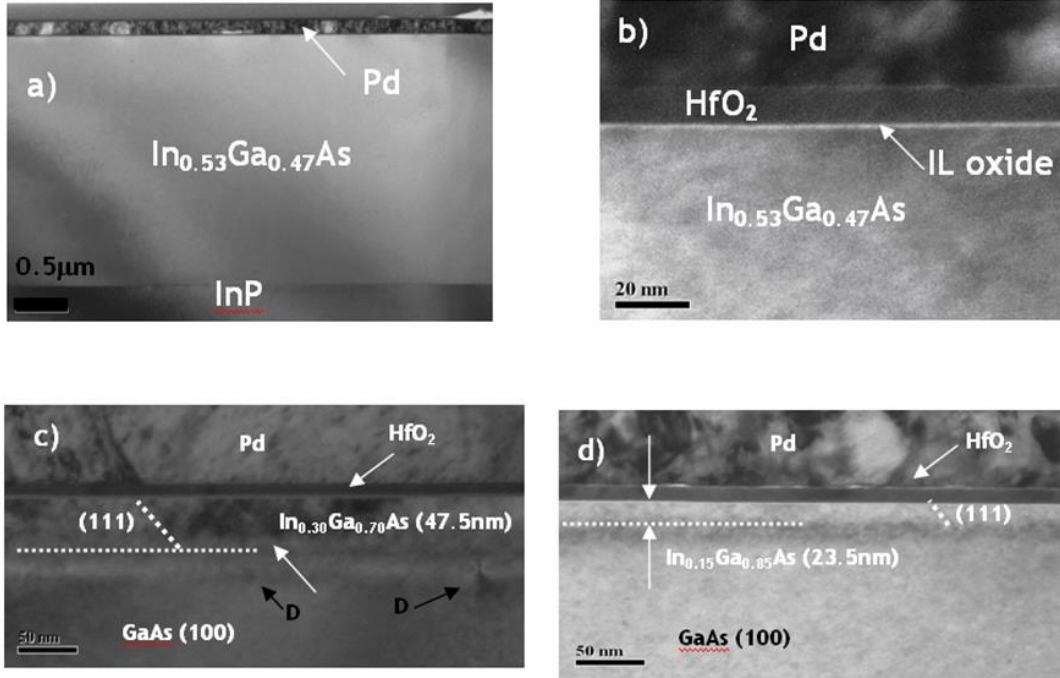
Figure 3.1. Transmission electron micrographs of: (a) Pd/HfO$_2$/In$_{0.53}$Ga$_{0.47}$As/InP structure, illustrating the InP(100) substrate, the In$_{0.53}$Ga$_{0.47}$As layer (2.095$\mu$m) and the Pd gate layer (~120nm). The HfO$_2$ thin film is not visible at the magnification level in this TEM cross section.; (b) higher magnification image of the Pd/HfO$_2$/In$_{0.53}$Ga$_{0.47}$As/InP structure, illustrating the 9.5 nm HfO$_2$ layer, and a 1.0nm IL oxide between the HfO$_2$ layer and the In$_{0.53}$Ga$_{0.47}$As substrate; (c) Pd/HfO$_2$/In$_{0.30}$Ga$_{0.70}$As/GaAs structure, indicating a 47.5nm In$_{0.30}$Ga$_{0.70}$As layer containing (111) stacking faults (white dotted line), and dislocations (D). Note: defects appear to extend into the GaAs(100) substrate. The HfO$_2$ layer is 9.3nm with a 0.9nm IL oxide, (d) Pd/HfO$_2$/In$_{0.15}$Ga$_{0.85}$As/GaAs structure, indicating a 23.5nm In$_{0.15}$Ga$_{0.85}$As layer containing (111) stacking faults (white dotted line). The HfO$_2$ layer is 14.0 nm with a 1.1 nm IL oxide. This TEM imaging and sample preparation was performed by Simon Newcomb of Glebe Scientific Ltd.

As seen in Figure 3.1(a) there is no evidence of defects in the In$_{0.53}$Ga$_{0.47}$As (2.095 $\mu$m) epitaxial layer on the InP (100) substrate. This is unsurprising as the 53% In concentration layer is lattice matched to InP. No defects are detected in the In$_{0.53}$Ga$_{0.47}$As epitaxial layer for a range of cross sectional images. TEM performed on the Pd/HfO$_2$/GaAs structure also indicated no defects in the GaAs substrate (not shown). In Figure 3.1(b) a higher magnification image of the Pd/HfO$_2$/In$_{0.53}$Ga$_{0.47}$As/InP structure, shows the HfO$_2$ layer (9.5nm) and the presence of a (1.0nm) IL oxide between the HfO$_2$ layer and the In$_{0.53}$Ga$_{0.47}$As substrate. For all

samples investigated an interlayer (IL) oxide is observed between the ALD $HfO_2$ film and the $In_xGa_{1-x}As$ substrate, with a thickness ranging from 0.9 to 1.3nm. The IL oxide thickness was not affected in samples which received the three stage surface pre-treatment prior to the ALD, and in that case it is possible that some native oxide regrowth occurred during the time interval between removal of the samples from the treatment solution to loading to the ALD chamber, during which the semiconductor surface was exposed to ambient. The IL oxide appears to be fully amorphous, however examination of the TEM micrographs suggests that the $HfO_2$ layer is a mixed amorphous/crystalline film, with evidence of crystallites extending through the film from the IL oxide to the Pd metal gate. These samples underwent no post-ALD deposition annealing, thus suggesting that the partial crystallization of the $HfO_2$ film on these $In_xGa_{1-x}As$ substrates possibly occurs during the ALD growth at $250^oC$.

TEM micrographs for the $In_{0.30}Ga_{0.70}As$ and $In_{0.15}Ga_{0.85}As$ layers grown on GaAs (100) are plotted in Figure 3.1 (c) and (d) respectively. These both exhibit a higher density of defects in the InGaAs layer. This is expected as the layer thickness of 47.5 nm for the $In_{0.30}Ga_{0.70}As$ sample is well in excess of the critical thickness of 12 nm for growth of this InGaAs composition on GaAs.[10,11,12] It is also the case that the layer thickness of 23.5 nm for the $In_{0.15}Ga_{0.85}As$ sample exceeds the nominal critical thickness of 20 nm.[10, 11, 12] The defects are attributed to (111) stacking faults and dislocations. Analysis of the TEM also indicates that in the case of the $In_{0.30}Ga_{0.70}As$ and $In_{0.15}Ga_{0.85}As$ samples the (111) stacking faults in the epitaxial layers extend to the $HfO_2/In_xGa_{1-x}As$ interface.

### 3.4. Room Temperature Electrical Analysis

The room temperature CV multi-frequency responses (20 Hz to 1MHz) for the $In_xGa_{1-x}As$ devices are shown in Figures 3.2 (a-d). These results are for samples which received no three-stage passivation treatment or anneal. Over the gate bias range of 0V to +4V, corresponding to what is expected to be the nominal accumulation region for *n*-type devices, it is apparent that very significant frequency
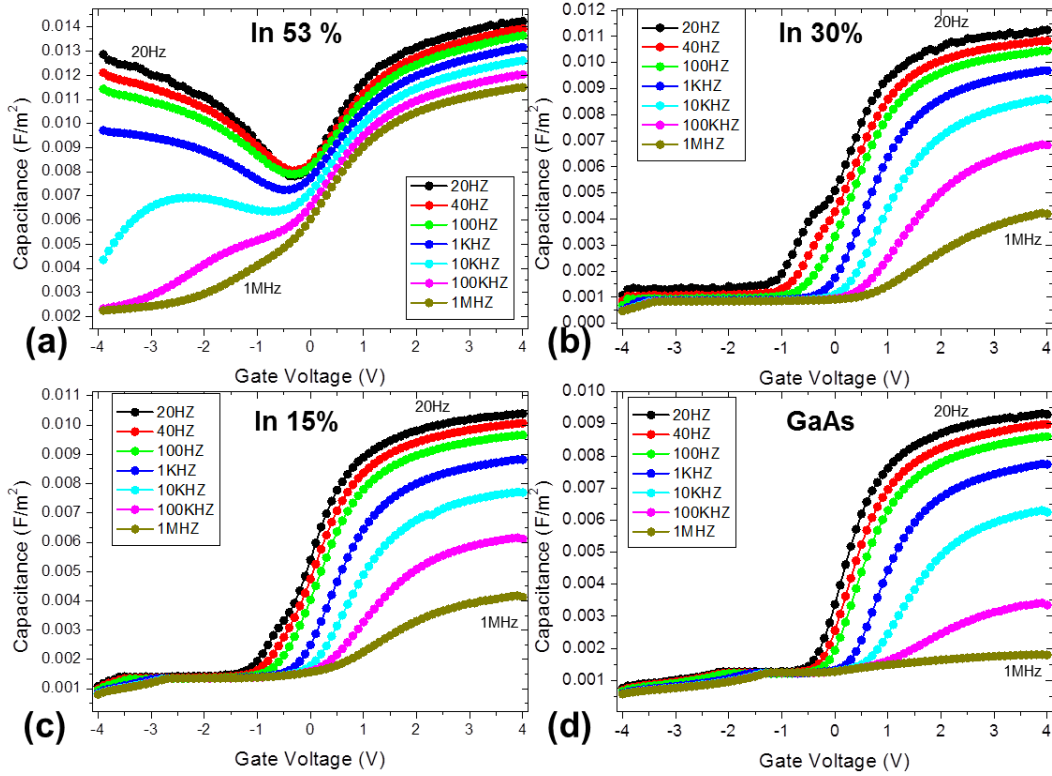
Figure 3.2 Multi-frequency (20 Hz to 1 MHz) C-V responses measured at room temperature (295K) for: (a) Pd/HfO$_2$/In$_{0.53}$Ga$_{0.47}$As/InP, (b) Pd/HfO$_2$/In$_{0.30}$Ga$_{0.70}$As/GaAs, (c) Pd/HfO$_2$/In$_{0.15}$Ga$_{0.85}$As/GaAs and (d) Pd/HfO$_2$/GaAs MOS.

dispersion of capacitance is observed for these In$_{0.30}$Ga$_{0.70}$As, In$_{0.15}$Ga$_{0.85}$As, and GaAs MOS samples. Similar behaviour has been reported extensively in the literature for GaAs MOS samples and in general represents one of the primary difficulties associated with the use of GaAs semiconductor layers in devices. [2, 13] In Figure 3.2 (a) it is noticeable that the capacitance dispersion at positive gate bias for the highest In content, In$_{0.53}$Ga$_{0.47}$As device, is markedly reduced in comparison with the lower In % devices in Figure 3.2 (b)-(d). Figure 3.3 compares the average frequency dispersion per decade (100 Hz to 1 MHz) at a gate bias of 4 V to illustrate this point. The average percentage capacitance dispersion per decade of frequency at a gate voltage (V$_{gate}$) = 4 V is ∼ 31 %, 19 %, and 20 %, for GaAs, In$_{0.15}$Ga$_{0.85}$As, and In$_{0.30}$Ga$_{0.70}$As respectively. This is reduced to ∼ 4 % for In$_{0.53}$Ga$_{0.47}$As devices. It
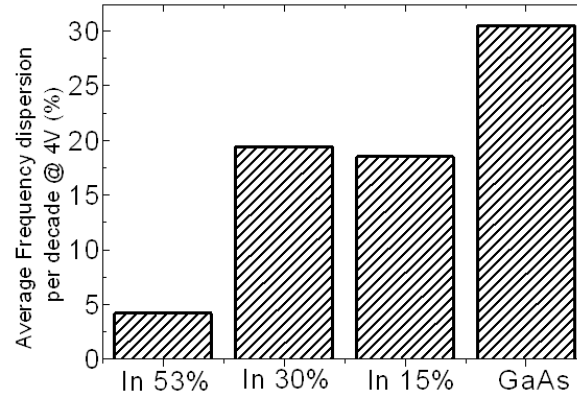
Figure 3.3 Average capacitance dispersion per decade of ac signal frequency (100Hz to 1MHz) for HfO$_2$/In$_x$Ga$_{1-x}$As MOS devices

should be noted again that the In$_{0.30}$Ga$_{0.70}$As epitaxial layer (0.0475μm) is well beyond the critical thickness (0.012 μm) contributing to a higher number of dislocations in this epitaxial layer. The Pd/HfO$_2$/$n$-In$_x$Ga$_{1-x}$As MOS structures were measured before and after the back metal contact formation. One important point is that the CV response over frequency was not modified by the back metal contact formation, ruling out the contribution of series resistance to the observed frequency dependence of the capacitance at positive gate voltage. Also it is noted that the three-stage surface passivation did not affect the trends observed for the frequency dispersion.

### 3.5.  Variable Temperature Electrical Analysis

#### 3.5.1.  Variable Temperature CV: -50$^o$C to 75$^o$C

Having examined the multi-frequency CV responses as a function of varying frequency at room temperature, another avenue to explore the effect of D$_{it}$ on the

electrical characteristics is to vary the measurement temperature while fixing the frequency. As a first step in examining the temperature dependence of the CV response the $In_xGa_{1-x}As$ samples were measured in the conventional Cascade probe station microchamber, with the lowest possible measurement temperature in this set-up being ~ -50$^o$C. Figures 3.4 (a-d) present CV responses at fixed a.c. signal frequency (10 kHz) with varying measurement temperatures (-50$^o$C to 75$^o$C) for the $In_xGa_{1-x}As$ devices.
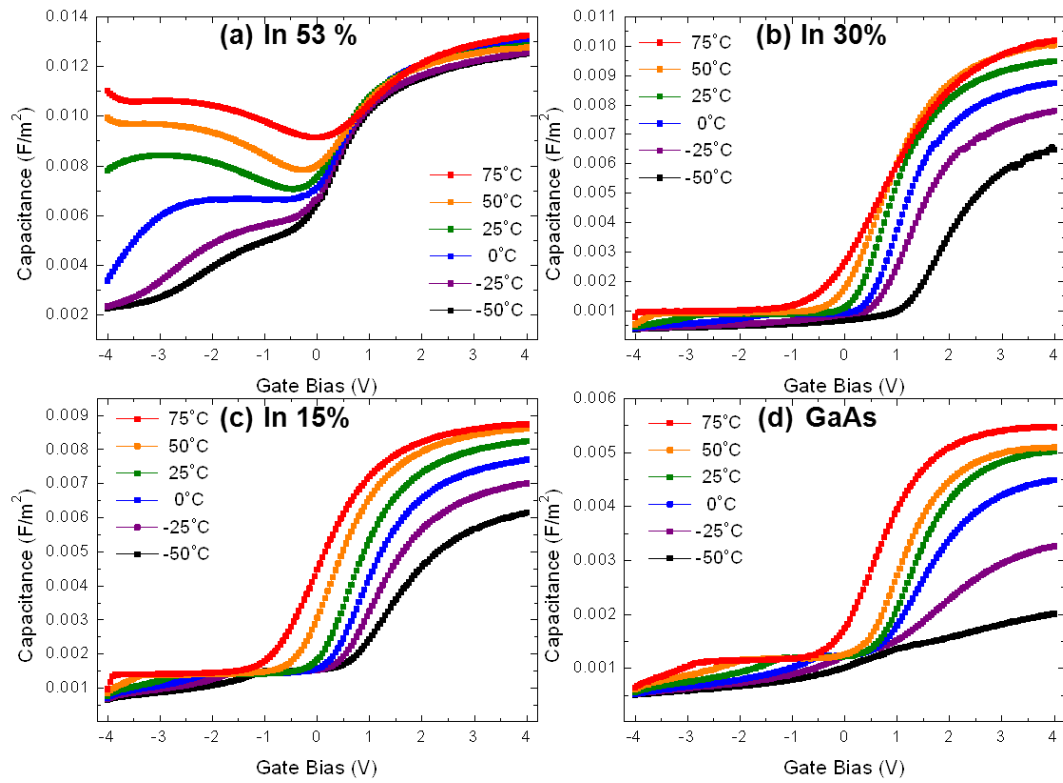


Figure 3.4 10 kHz CV response with varying temperature (-50$^o$C to 75$^o$C) of (a) Pd/9.5nm ALD $HfO_2$/$n$-$In_{0.53}Ga_{0.47}As$/InP, (b) Pd/9.2nm ALD $HfO_2$/$n$-$In_{0.30}Ga_{0.70}As$, (c) Pd/14.0nm ALD $HfO_2$/$n$-$In_{0.15}Ga_{0.85}As$ , and (d) Pd/11.4nm ALD $HfO_2$/$n$-GaAs. The average percentage capacitance dispersion (-50$^o$C to 75$^o$C) per 25$^o$C step of the temperature at $V_{gate}$ = 4 V is: 1.7% ($In_{0.53}Ga_{0.47}As$); 8.5% ($In_{0.30}Ga_{0.70}As$); 6.9% ($In_{0.15}Ga_{0.85}As$); 16.7% (GaAs). The leakage current densities for unpassivated devices at $V_{gate}$ = 3V are: $4.0 \times 10^{-7}$ A/cm$^2$ ($In_{0.53}Ga_{0.47}As$); $6.6 \times 10^{-7}$ A/cm$^2$ ($In_{0.30}Ga_{0.70}As$); $6.2 \times 10^{-7}$ A/cm$^2$ ($In_{0.15}Ga_{0.85}As$); $9.0 \times 10^{-7}$ A/cm$^2$ (GaAs).

The CVs display characteristics analogous to those observed with varying frequency at fixed temperature in Figure 3.2 (a-d). There is a pronounced increase in the dispersion of accumulation capacitance (0 to 4V) for the $In_{0.30}Ga_{0.70}As$, $In_{0.15}Ga_{0.85}As$, and GaAs samples. This is reduced considerably for the highest indium content, $In_{0.53}Ga_{0.470}As$ case. The average percentage capacitance dispersion (-50$^o$C to 75$^o$C) per 25$^o$C step of the temperature at $V_{gate}$ = 4 V is: 1.7% ($In_{0.53}Ga_{0.47}As$); 8.5% ($In_{0.30}Ga_{0.70}As$); 6.9% ($In_{0.15}Ga_{0.85}As$); 16.7% (GaAs). Again it is noticeable that the $In_{0.30}Ga_{0.70}As$ sample very slightly falls outside the trend of decreasing dispersion with increasing In content. As stated earlier it is possible that as it exceeds the critical thickness the stacking faults observed in the TEM in Figure 3.1 may contribute an additional defect source. It is important to point out however that structural defects in the $In_{0.30}Ga_{0.70}As$ epitaxial layer extending to the interface cannot be the sole contributor to interface defects. In fact, the GaAs sample, which exhibited excellent epitaxial structure with no evidence of defects in the TEM analysis displays the highest dispersion in accumulation with both temperature and frequency by quite some margin.

### 3.5.2. Variable Temperature CV: 77 K to 295 K

This temperature dependence over the range -50$^o$C to 75$^o$C indicated the potential value in extending the analysis by cooling the samples down to 77K in a cryogenic probe station. These measurements were carried out during a research visit to the University of Texas at Dallas. The multi-frequency CV responses (1 kHz to 1 MHz) at 295K and 77K for the 53% In, 30% In, 15%In, and GaAs MOS structures are shown in Figures 3.5 (a-d) respectively. These 295K results were also recorded in the cryogenic probe station prior to cooling in order to eliminate any contributing factors other than temperature reduction in comparing the CVs.
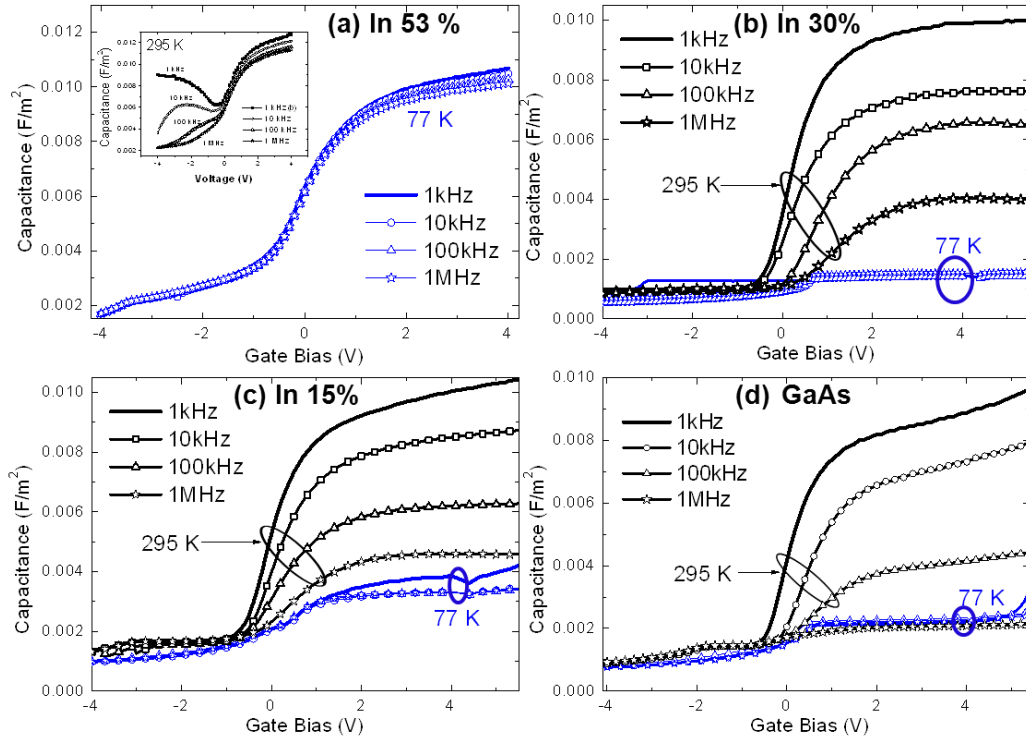
Figure 3.5 Multi-frequency (1 kHz to 1 MHz) C-V responses measured at room temperature (295K, black curves) and liquid nitrogen (77K, blue curves) for: (a) $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$: inset is the 295K data, (b) $Pd/HfO_2/In_{0.30}Ga_{0.70}As/GaAs$, (c) $Pd/HfO_2/In_{0.15}Ga_{0.85}As/GaAs$ and (d) $Pd/HfO_2/GaAs$ MOS.

For the $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ device in Figure 3.5 (a), there is no significant difference in the capacitance measured in the accumulation region (4V) at 77K and 295K, indicating that the devices are most likely in accumulation and that it is possible to move the Fermi level ($E_f$) at the $In_{0.53}Ga_{0.47}As/HfO_2$ interface to the conduction band edge ($E_c$). In addition, the minimum measured capacitance (-4V) at both 77K and 295K is close to the expected theoretical minimum capacitance, ~ 0.002 $F/m^2$, for the $4x10^{17}cm^{-3}$ $n$ type doping level in the $In_{0.53}Ga_{0.47}As$ layer, and an oxide capacitance of 0.011 $F/m^2$. This is another indicator of free Fermi level movement at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface with changes in applied gate bias.

However, for the case of the 30% In, 15% In, and GaAs MOS devices, the curves in Figure 3.5 (b-d) show that a very different CV response is measured at 77K compared to 295K. At 77K the capacitance practically becomes independent of the ac

measurement frequency and is observed to settle at an approximately constant value over the gate bias range examined. This behaviour is consistent with the filling of an interface defect with the slowly varying DC gate bias and provides confirmation that the frequency dependent increase of capacitance at 295K is due to an interface trap capacitance response. The almost constant capacitance at 77K implies that the Fermi Level at the $HfO_2/In_xGa_{1-x}As$ (x: 0, 0.15, 0.30) interface is pinned at a fixed energy, and all additional gate charge is compensated by charging on the $HfO_2/In_xGa_{1-x}As$ interface defects, preventing the formation of an electron surface accumulation layer.

The observation that we can achieve accumulation for $In_{0.53}Ga_{0.47}As$, but not for $In_{0.30}Ga_{0.70}As$, $In_{0.15}Ga_{0.85}As$, and GaAs, suggests the presence of interface defects which move from energies aligned within the energy gap to energy levels in the conduction band as the energy gap of the semiconductor is changed from GaAs (~ 1.42 eV) to $In_{0.53}Ga_{0.47}As$ (~ 0.75 eV). There is some other evidence in the literature to support this argument. Theeten *et al.* observed a similar effect where a defect response, which is dominant in the case of lower In content (< 0.35) devices, becomes insignificant for higher In content devices.[14]

Internal photoemission (IPE) measurements were performed on the $HfO_2/In_xGa_{1-x}As$ samples, with the IPE samples being cleaved directly from the same wafers used for fabrication of the MOS devices. IPE measurements were carried out by a collaborator, Prof. Valeri Afanasiev of K. U. Leuven. The IPE results indicate that the increase in the energy gap moving from $In_{0.53}Ga_{0.47}As$ (0.75eV) to GaAs (1.42eV) occurs due to a decrease in the electron affinity.[15] The values of the (energy gap, and electron affinity) are; $In_{0.53}Ga_{0.47}As$ (0.75 eV, 4.5 eV), $In_{0.30}Ga_{0.70}As$ (1.01 eV, 4.31 eV), $In_{0.15}Ga_{0.85}As$ (1.21eV, 4.19 eV), GaAs (1.43 eV, 4.07 eV).[16, 17] The IPE analysis in combination with the CV results indicate that the defect states responsible for the observed frequency dispersion at positive gate bias for GaAs and $In_xGa_{1-x}As$ (x=0.15, 0.30) devices are located at an energy in the range 4.07 to 4.5 eV from the vacuum level. This is summarized the schematic in Figure 3.6.
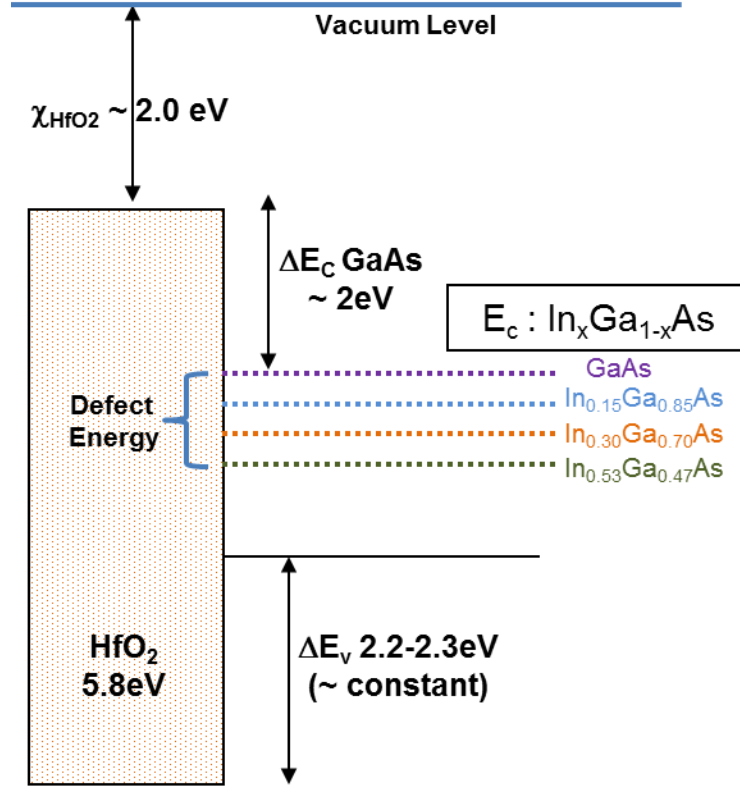
Figure 3.6 Schematic of position of $E_c$ relative to the vacuum level for varying indium content devices, and the likely energy range for the interface defect responsible for the observed dispersion of accumulation capacitance for lower In content (x: 0, 0.15. 0.30) $In_xGa_{1-x}As$ devices.

Therefore for the case of $In_{0.53}Ga_{0.47}As$ devices this defect enters the conduction band, but still has the potential to have a detrimental effect on device performance. The defect energy with respect to the $In_{0.53}Ga_{0.47}As$ valence band permits inversion mode $In_{0.53}Ga_{0.47}As$ MOSFET operation. However, the defect density, now in the conduction band, is comparable to the inversion charge density. When the Fermi level reaches the defect energy level it will be pinned, and any additional gate charge will be compensated by charging of the interface defect level over the voltage range where the defect is occupied (> 4 volts from the results in Figures 3.5 (b) - (d)). Consequently there will be a rapid decrease in transconductance with gate bias, with an apparent decrease in the inversion layer mobility. Literature reports have observed such behavior for $In_{0.53}Ga_{0.47}As$ MOSFETS.[18, 19]

The charge in the defect level for the $In_xGa_{1-x}As$ (x: 0, 0.15, 0.30) devices at 77K, $\Delta Q_{it}$, can be estimated from the simple relationship where $\Delta Q_{it} = \Delta V_g$ x $C_{ox}$, $\Delta V_g$ being the gate bias range over which the capacitance remains constant at 77K, and $C_{ox}$ being the oxide capacitance. Therefore, one can determine a lower limit to the interface defect concentration for the $In_xGa_{1-x}As$ (x: 0, 0.15, 0.30) devices. This calculation yields minimum interface state densities of $2.5 \times 10^{13}$ $cm^{-2}$ of acceptor like defects at the $HfO_2/In_xGa_{1-x}As$ interface (x: 0, 0.15, 0.30). Over the bias range examined at 77K, surface accumulation was not achieved, thus rendering this a minimum $D_{it}$ value. While an upturn in the CV response was observed at higher gate bias, this was attributable to a detrimental increase in gate leakage current. This density of interface defects, $2.5 \times 10^{13}$ $cm^{-2}$, would prevent inversion mode MOSFET behavior for $In_xGa_{1-x}As$ channel devices with an In% below 53%, and the observations in this study are consistent with work by Sonnet *et al.* [20] where drain currents for $Al_2O_3/In_{0.2}Ga_{0.8}As$ MOSFETs were three orders of magnitude lower than $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSFETs, fabricated using an identical process.

### 3.6. $D_{it}$ Analysis of $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ devices

While accumulation can be achieved for the $In_{0.53}Ga_{0.47}As$ stack, the dispersion observed in the CV as a function of both temperature and frequency, for $V_{gate}$ in the range -1 V to -4 V, is characteristic of interface defects with a peak density at a specific energy in the $In_{0.53}Ga_{0.47}As$ bandgap (as discussed in Chapter 2). Figures 3.7 (a) and (b) show room temperature CV multi-frequency responses for unpassivated, and post $325^{o}C$ forming gas anneal, $Pd/HfO_2/n\text{-}In_{0.53}Ga_{0.47}As/InP$ devices respectively. The FGA results in a noticeable reduction in the frequency dispersion both at $V_{gate}$=4 V and also in the transition region from depletion to accumulation at $V_{gate} \sim$ 0V to 1V. The CV dispersion for $V_{gate}$ in the range -1V to -4V, which is characteristic of interface defects, is also visibly reduced following $325^{o}C$ FGA.
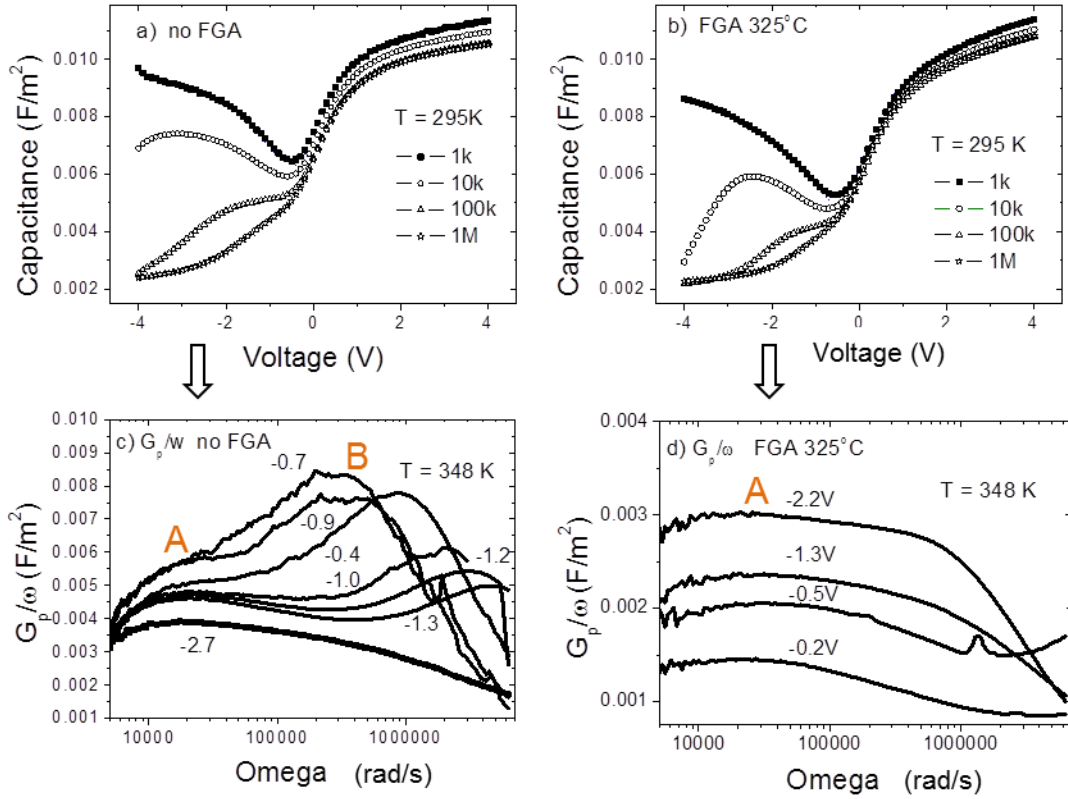
FIG. 3.7 $G_p/\omega$ versus $\omega$ ($\omega = 2\pi$ x frequency) at 75°C for selected and representative gate voltage bias points (indicated), for (a) unpassivated, and (b) three stage ex-situ passivated, Pd/10.3nm ALD HfO$_2$/*n*-In$_{0.53}$Ga$_{0.47}$As/InP. IL thickness for the passivated In$_{0.53}$Ga$_{0.47}$As device is 1.3nm. A slight reduction in the peak $D_{it}$ of defect response (A), and removal of defect response (B), have also been observed for a three-stage passivated device.

There is also possibly an additional benefit during the FGA of employing the Pd as a gate metal. Pd is known to react with hydrogen, and is used in some applications for $H_2$ detection. Therefore it may be possible that there is a catalytic effect of using the Pd gate in terms of cracking $H_2$ during the forming gas anneal to increase the efficiency of the anneal step.

The CV response from -1V to -4 V is not representative of true inversion at the HfO$_2$/In$_{0.53}$Ga$_{0.47}$As interface. As discussed in Chapter 2, a genuine inversion CV for an MOS capacitor would result in a constant capacitance as a function of V$_{gate}$, where the magnitude of this constant capacitance region increases with increasing

temperature or decreasing measurement frequency up to a maximum value set by $C_{ox}$.[21,22] Similar frequency dependent CV profiles have previously been reported irrespective of the dielectric layer, passivation approach, and $In_{0.53}Ga_{0.47}As$ growth method, suggesting that these interface states originate from the $In_{0.53}Ga_{0.47}As$ surface.[3-5]

In quantifying the interface state defect density contributions to the CV and GV responses, the approach used is the conductance technique as developed for $Si/SiO_2$ systems, and it is applied here to the $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ devices.[8, 22, 23] The technique involves measuring the capacitance and conductance at a constant $V_{gate}$ while applying a logarithmic frequency sweep from 50Hz to 1MHz. The measurements are carried out at temperatures of -50ºC, 25ºC, and 75ºC, in order to obtain interface state responses over a wider portion of the semiconductor energy gap. The equivalent parallel conductance ($G_p/\omega$) is calculated and plotted against angular frequency ($\omega$) for each bias point (100mV steps) in a gate voltage range encompassing the entire defect response as estimated from CV and GV measurements.[22] The analysis inherently assumes the $HfO_2/In_{0.53}Ga_{0.47}As$ surface is in depletion where only majority carriers interact with the interface traps, and an accurate estimate of $D_{it}$ can be extracted. If the $HfO_2/In_{0.53}Ga_{0.47}As$ surface is in weak inversion, the analysis may overestimate the $D_{it}$ value.[24] Series resistance corrections were estimated for all devices and found to be negligible.[22]

Figures 3.7 (c) and (d) show estimates of $G_p/\omega$ versus $\omega$ curves for an unpassivated and post 325ºC forming gas anneal $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ structure, respectively. The measurement temperature is 75ºC for all devices, as in the case of these samples clear $G_p/\omega$ peaks were not distinguishable at -50ºC and 25ºC. The plot in Figure 3.7 (c) shows two maximum peak profiles at low and high angular frequencies, and at different gate voltages within depletion, which may possibly be characteristic of two defects with distinct energy levels. For ease of discussion here the defect responses at lower and higher angular frequency will be termed (A) and (B), respectively, as indicated on the Figure. A peak $D_{it}$ of $1.7 \times 10^{13}$ $cm^{-2}$ $eV^{-1}$ is calculated for defect response (A) and $1.5 \times 10^{13}$ $cm^{-2}$ $eV^{-1}$ for defect response (B). Figure 3.7 (d) shows $G_p/\omega$ versus $\omega$ curves for the post-FGA device. No peak for (B)

is evident while for (A) the $D_{it}$ is estimated to be 1.0 x $10^{13}$ cm$^{-2}$ eV$^{-1}$, representing an approximately 40% $D_{it}$ reduction for (A) compared to the unpassivated sample. Similarly broad peak profiles have been reported by Mui *et al.* for $Si_3N_4/In_{0.53}Ga_{0.47}As$ interfaces.[23] There is slight reduction in $D_{it}$ at lower angular frequency for (A) post forming gas anneal, while it significantly reduces the contribution of (B) to the extent where it is below detectable limits in the conductance analysis. This effect of the FGA suggests that the defect response at higher angular frequency, (B), may be related to a dangling bond orbital of Ga, As, or In. However, precise atomic identification of the defects is beyond the scope of this work, and remains a challenging topic in the field of high-k systems on III-V semiconductors. Other characterization methods such as electron spin resonance (ESR), which have proved highly successful for Si based systems, eg. in detection of $P_b$ dangling bond defects, could be explored in an effort to garner more information regarding the physical origin of interface states for $In_{0.53}Ga_{0.47}As$.

### 3.7.    Conclusions

In summary, it is found that the large temperature and frequency dispersion in CV responses at positive gate bias in devices using *n*-type GaAs and low In content (x= 0.30, 0.15) $In_xGa_{1-x}As$ epitaxial layers is significantly reduced using high In content (x=0.53) epitaxial layers, suggesting that it is only possible to achieve true accumulation for the $In_{0.53}Ga_{0.47}As$ devices using the surface preparations and ALD $HfO_2$ layers examined in this work. However, the CV responses at negative gate bias still indicate a significant contribution from defect states at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface. An estimation of $D_{it}$ using the conductance technique indicates that densities for the $HfO_2/In_{0.53}Ga_{0.47}As$ devices examined in this work (~ 1.0 x $10^{13}$ cm$^{-2}$ eV$^{-1}$ to 1.7 x $10^{13}$ cm$^{-2}$ eV$^{-1}$) remain too high for practical device applications, but it has been shown that a three-stage $In_{0.53}Ga_{0.47}As$ surface passivation and post-metallization FGA at 325$^o$C can provide a significant reduction in interface state defect densities.

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# Chapter 4

## 4. A systematic study of In$_{0.53}$Ga$_{0.47}$As surface passivation using (NH$_4$)$_2$S

### 4.1. Introduction

In order to address the high interface state density (D$_{it}$) which is typically observed and detrimental to the performance of high-$k$/III-V devices, various approaches have been attempted in the passivation of the high-$k$/III-V interface in an attempt to reduce D$_{it}$.[1,2,3,4,5,6,7] One of the more common ex-situ passivation techniques involves the use of sulphur based chemicals such as ammonium sulphide (NH$_4$)$_2$S.[8,9,10,11,12] Aqueous (NH$_4$)$_2$S is widely used due to its' effectiveness at removing native oxides, and at improving the electrical characteristics of devices fabricated on (NH$_4$)$_2$S treated surfaces.[5,6] In addition, passivation in (NH$_4$)$_2$S solution is a relatively quick, cost-effective, and straight-forward process. However, there is little discussion in the literature regarding the optimization of the passivation procedure. Despite it being a simple process, there are a number of important parameters which can have a decisive bearing on the efficacy of the passivation, principal among these being: the surface pre-treatment, if any, prior to immersion in the (NH$_4$)$_2$S solution; the passivation time in the (NH$_4$)$_2$S solution; the concentration of the (NH$_4$)$_2$S solution; and the temperature of the (NH$_4$)$_2$S solution.

An extensive chemical and physical study, using X-ray photoelectron spectroscopy (XPS) and atomic force microscopy (AFM), by Brennan *et al.* investigated various aqueous ammonium sulphide passivation conditions.[13] The results of that work established that an initial degrease followed by immersion for 20 minutes in a 10% (NH$_4$)$_2$S solution at room temperature, was the most effective in terms of suppression of native oxide formation and in minimizing surface roughening effects. Given the positive results from that chemical and physical analysis, the principal aim of the work described in this chapter is to investigate the electrical

characteristics of MOS devices to understand the effects of varying the $(NH_4)_2S$ concentration in the passivation of *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ surfaces prior to atomic layer deposition (ALD) of $Al_2O_3$. A secondary objective of this study is to utilize the electrical results from the MOS device exhibiting the best electrical characteristics, to perform a comparison of the extracted $D_{it}$ across the $In_{0.53}Ga_{0.47}As$ energy gap at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface using two different methods, the temperature modified High-Low frequency CV method and the more traditional approximation to the Conductance method.

## 4.2.  Experimental Details

The $In_{0.53}Ga_{0.47}As$ epitaxial layers used in this work were either (1) ~2μm *n*-type $In_{0.53}Ga_{0.47}As$ (S at ~$4x10^{17}cm^{-3}$) grown by MOVPE on heavily (S at ~$2x10^{18}$ $cm^{-3}$) *n*-doped InP(100) wafers, or (2) ~2μm *p*-type $In_{0.53}Ga_{0.47}As$ (Zn at ~$4x10^{17}cm^{-3}$) grown by MOVPE on heavily *p*-doped (Zn at ~$2x10^{18}$ $cm^{-3}$) InP(100) wafers. Identical epitaxial layers and substrates were used previously in the chemical and physical study by Brennan *et al*.13 Prior to immersion in aqueous $(NH_4)_2S$ solutions, all $In_{0.53}Ga_{0.47}As$ surfaces were initially degreased by sequentially rinsing for 1 minute each in acetone, methanol, and isopropanol. $(NH_4)_2S$ concentrations of 22%, 10%, 5%, and 1% in deionised $H_2O$ were used, and the $In_{0.53}Ga_{0.47}As$ surfaces were subjected to the dilute $(NH_4)_2S$ for 20 minutes, with the solution at room temperature (~ 295K).

One of the conclusions of the physical study performed by Brennan *et al*.,13 was that increasing the temperature of the $(NH_4)_2S$ solution significantly increased the $In_{0.53}Ga_{0.47}As$ surface roughness. This is illustrated in Figure 4.1 (a-c) where the root mean square (RMS) roughness is seen to rise from 0.20 nm at room temperature, to 0.33 nm at $40^{o}C$ and $60^{o}C$. As it is known that surface roughening is detrimental to device electrical properties in terms of carrier mobility, it was decided to compare the $(NH_4)_2S$ concentration while maintaining the solution at room temperature.
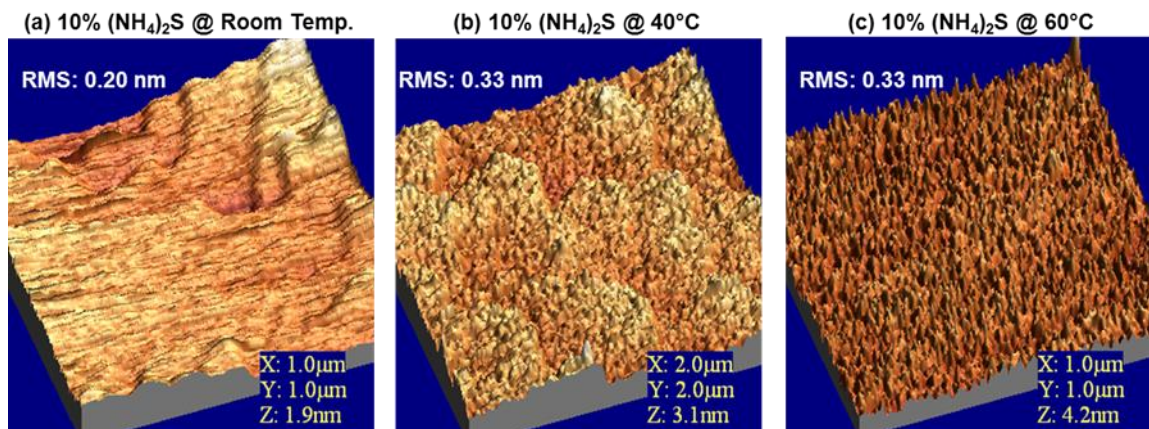
Figure 4.1 Atomic Force Microscopy (AFM) images of 10% (NH4)2S treated $In_{0.53}Ga_{0.47}As$ surfaces with the varying solution temperatures (a) Room temperature, (b) $40^{o}C$, and (c) $60^{o}C$. The AFM was performed by Dr. Barry Brennan (formerly of Dublin City University and the University of Texas at Dallas).

Samples were introduced to the ALD chamber load lock (base pressure of less than $2 \times 10^{-8}$ mbar) within ~ 7 minutes after removal from the aqueous $(NH_4)_2S$ solution, unless otherwise stated. This air exposure was kept as short as possible in an effort to minimise both native oxide re-growth and ambient contamination prior to $Al_2O_3$ growth (nominal thickness 8 nm) by ALD using alternating pulses of TMA $(Al(CH_3)_3)$ and $H_2O$. Gate contacts ~ 100 nm thick were formed by e-beam evaporation of Ni (60nm), and Au (40nm), through a shadow mask. For comparative purposes across all samples, the electrical tests were performed on capacitors of nominal 100 μm diameter, and in an attempt to minimize variation due to any differences in the shadow masks used for metal deposition, the actual dimensions of all test devices were measured using an optical microscope. Multiple sites were examined in all cases to ensure the results are representative of device behaviour. It is also noted that larger and smaller device areas were measured on all samples and the capacitance scaled as expected with area. Back metal contacts of Ti/Au (for *p*-type devices) and Au/Ge/Au/Ni/Au (for *n*-type devices) were deposited, followed by a 30 second rapid thermal anneal (RTA) at 623 K in $N_2$. The back metal contact formation was carried out to minimise any contribution of series resistance to the electrical

results. The capacitance-voltage (CV) and conductance-voltage (GV) measurements were recorded using a HP4284A LCR meter. The measurements at room temperature were performed on-wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry air, dark environment (dew point ≤203K). Conventional transmission electron microscopy (TEM) samples were prepared using focused ion beam (FIB) thinning procedures in an FEI 200 Workstation and examined at 200kV in a JEOL2000FX.[14] Monochromated X-ray photoelectron spectroscopy (XPS) was carried out using an Al Kα (1486.7 eV) X-ray source with a line-width of 0.25 eV and an Omicron 125 mm seven channel hemispherical analyzer with a pass energy of 15 eV and seven Channeltron detection system described elsewhere.[15] Core level photoemission spectra were taken of the As $2p_{3/2}$, Ga $2p_{3/2}$, In $3d_{5/2}$, C $1s$, O $1s$, S $2p$, As $3d$, Ga $3d$ and In $4d$ regions after loading to ultra-high vacuum (UHV) and prior to both $Al_2O_3$ and metal deposition in order to determine the chemical composition of the initial interfacial region.

### 4.3.    Structural Analysis

TEM micrographs for *n*-type and *p*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ devices are shown in Figures 4.2 (a) and (b) respectively. These particular samples had received the 10% $(NH_4)_2S$ passivation prior to ALD deposition. The TEM results show that the actual physical thicknesses of the $Al_2O_3$ layers are close to the nominal value of 8 nm, and the ALD oxide layers exhibit good thickness uniformity over the area examined. The oxide layers also appear amorphous without any evidence of crystallite formation. In addition it is noticeable that there is no visible roughening of the $Al_2O_3$/ $In_{0.53}Ga_{0.47}As$ interfaces from the 10% $(NH_4)_2S$ $In_{0.53}Ga_{0.47}As$ surface treatment. Roughening effects have been observed when higher concentrations (~ 22%), and temperatures (~333K), of $(NH_4)_2S$ have been used, and in which case the $(NH_4)_2S$ may have partially etched the $In_{0.53}Ga_{0.47}As$ surface.[13, 16] This is relevant to metal-oxide-semiconductor field effect transistor (MOSFET) device transport properties as
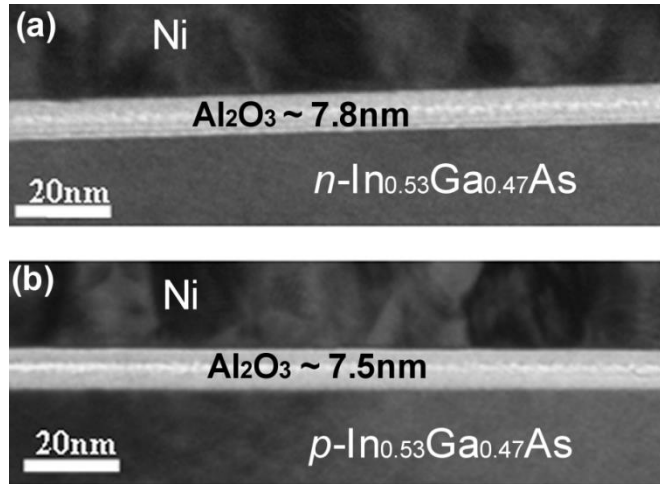
Figure 4.2. Cross-sectional TEM micrographs of (a) 10% $(NH_4)_2S$ treated, Au/Ni/ 7.8nm $Al_2O_3$/*n*-$In_{0.53}Ga_{0.47}As$/InP, and (b) 10% $(NH_4)_2S$ treated, Au/Ni/ 7.5nm $Al_2O_3$/*p*-$In_{0.53}Ga_{0.47}As$/InP device structures. This TEM was performed by Dr. Simon Newcomb of Glebe Scientific Ltd.

it is crucial to have as smooth an interface as possible because roughness at the oxide-semiconductor interface can result in surface scattering effects leading to reduced mobility.[17] It is noted that there appears to be a band of lighter image contrast running through the centre of the $Al_2O_3$ layer in both samples. In addition, this band was not observed in TEM micrographs taken from an area of the *n*-type sample with no gate metal (not shown), which may suggest that mechanical stress from the gate metal could be a contributing factor. However, the authors of this work have observed similar bands running through $Al_2O_3$ layers which were deposited in three independent ALD reactors. A detailed analysis of this effect is beyond the scope of the current work, and further physical characterization would be required to precisely identify the physical origin of this observation.

## 4.4. Electrical Analysis: CV and GV characteristics

The C-V curves at room temperature (295K) with ac signal frequencies from 200 Hz to 100 kHz for the 22%, 10%, 5%, and 1% $(NH_4)_2S$ passivated $n$-type $In_{0.53}Ga_{0.47}As$ devices are shown in Figures 4.3 (a), (b), (c), and (d) respectively. With regard to the 22%, 5%, and 1% devices, the frequency dispersion, with a broad peak response observed for $V_{gate}$ in the range of -0.25 V to -2 V, is typical of that commonly observed in the literature for $n$-type $In_{0.53}Ga_{0.47}As$[2, 5, 7, 18, 19, 20] As mentioned in Chapter 2, for the case of interface defects having a peak density at a specific energy in the semiconductor bandgap, the capacitance will move through a peak and then reduce with increasing bias (as discussed in Chapter 2). Additionally, the peak capacitance will occur at a bias closer to the accumulation region with increasing ac signal frequency.[21] Such behaviour has been observed for Si based devices where the CV is affected by unpassivated Pb centers.[21] Clearly, from Figure 4.3, the CV profiles are consistent with that expected for a defect with a specific energy in the $In_{0.53}Ga_{0.47}As$ bandgap. The conductance data (not shown) also exhibits peaks moving towards accumulation with increasing frequency, reflecting the capacitance behaviour.

It can also be stated that this is not representative of true inversion at the $Al_2O_3/n$-$In_{0.53}Ga_{0.47}As$ interface.[18] Inversion at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface would result in a constant capacitance as a function of $V_{gate}$, where the magnitude of this constant capacitance region increases with increasing temperature or decreasing measurement frequency up to a maximum value set by the oxide capacitance ($C_{ox}$) as described in Chapter 2.[22] This has been observed in numerous works for MOS devices incorporating Ge and Si as a semiconductor.[22, 23] For arguments sake, were it the case that the $Al_2O_3/In_{0.53}Ga_{0.47}As$ samples in the current study were inverted, but excessive gate leakage resulted in a situation where the devices could not sustain the inversion charge, then this would manifest in the CV curve as an abrupt collapse in the capacitance in inversion, and would occur at a bias independent of ac signal frequency. Clearly this is also not the case here as evident from the peak responses in Figure 4.3.

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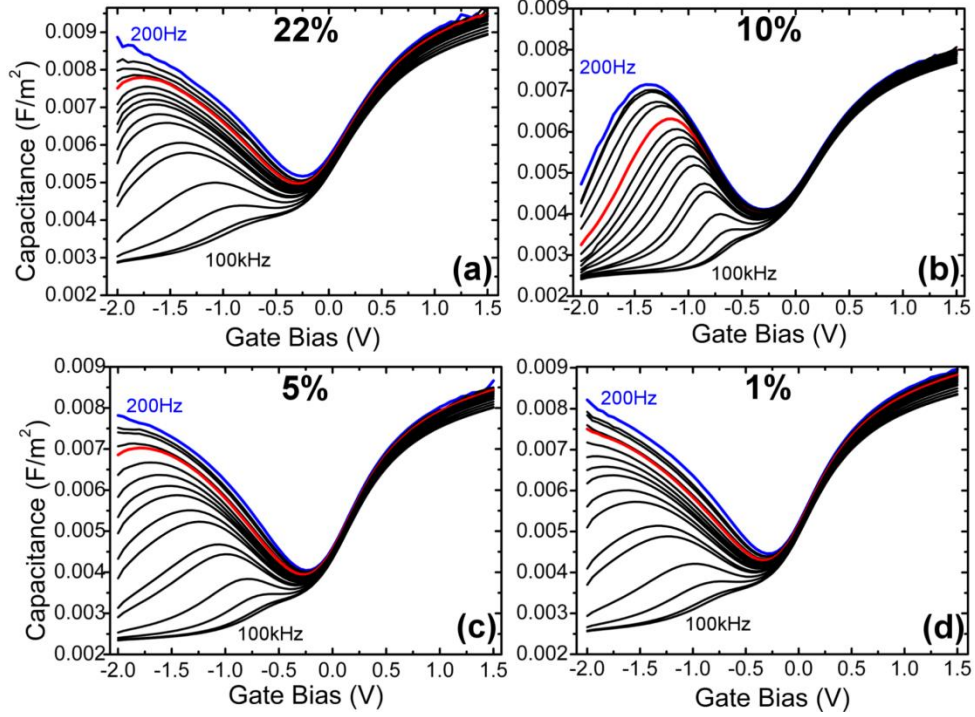
Figure 4.3. Room temperature CV frequency variation (200 Hz to 100 kHz) of (a) 22%, (b) 10%, (c) 5%, and (d) 1%, $(NH_4)_2S$ treated, Au/Ni/ ~8nm $Al_2O_3$/$n$-$In_{0.53}Ga_{0.47}As$/InP devices. All samples were introduced to the ALD load lock as quickly as possible (< 7 minutes) after removal from $(NH_4)_2S$ solution, in order to minimise ambient exposure. Actual diameters of the capacitors were: 118 μm, 106 μm, 106 μm, 106 μm, for the 22%, 10%, 5%, and 1% samples, respectively. 1 kHz curves have been highlighted in red to illustrate that a more accurate representation of the interface defect response is obtained by measuring down to 200 Hz.

A similar form of the C-V response observed in Figures 4.3 (a), (c), and (d), has been reported for different $n$-$In_{0.53}Ga_{0.47}As$ surface preparations, different high-$k$ oxide layers, different high-$k$ deposition methods, and for samples with and without interlayer (IL) oxides. [2, 5, 7, 18, 19, 20] This indicates that the dominant interface defect originates from the $In_{0.53}Ga_{0.47}As$ surface, as opposed to the interfacial layer or high-$k$ oxide. However, for the 10% $n$-type device in Figure 4.3 (b), the CV profile is noticeably improved. There is a reduced response for the interface state related capacitance ($C_{it}$) at negative gate bias in terms of the peak magnitude and width, and it is significant that even at 200Hz, the CV goes through a peak and then decreases again as the gate bias approaches -2V. This is in contrast to the higher magnitude and broader profiles evident for the other three samples as seen in Figures 4.3 (a), (c), and

(d). This suggests a reduction in the interface state density for the 10% $(NH_4)_2S$ surface treatment. It is also necessary here to stress the importance of measuring down to very low frequencies (200Hz) in order to capture as much of the interface defect related response as possible. This allows for a more accurate determination of the interface state density as will be discussed later. It appears to be a common practice in much of the literature on this topic to only measure the CV down to 1 kHz. While this may give some useful information, and provide indications of device performance, it will also result in an underestimation of the extracted magnitude of the interface state defect density. In Figures 4.3 (a-d), the 1 kHz CV curves have been highlighted in red to illustrate that a more accurate representation of the interface defect response is obtained by measuring down to 200Hz (blue curves). It should be noted that although all devices experienced a 30 second, 623 K RTA in $N_2$, for back contact formation, there has been no attempt as yet to anneal the samples in forming gas, an approach which has been shown to reduce interface defect concentrations on *n*-type $In_{0.53}Ga_{0.47}As$ MOS capacitor devices.[18, 24, 25] Therefore, potential exists to further improve the CV response of the 10% device.

Another means to gauge the efficacy of the passivation treatment on the *n*-type $In_{0.53}Ga_{0.47}As$ devices is to compare the deviation of the measured accumulation capacitance from the expected theoretical capacitance. It has been reported for *n*-type $In_{0.53}Ga_{0.47}As$ that the theoretical CV response is asymmetrical in shape, with a reduction in accumulation capacitance expected on *n*-type due to both the fact that the density of states in the $In_{0.53}Ga_{0.47}As$ conduction band ($1.7x10^{17}$ $cm^{-3}$) is over one order of magnitude lower compared to the $In_{0.53}Ga_{0.47}As$ valence band ($2.6x10^{18}$ $cm^{-3}$), and also due to charge quantization effects.[12, 26, 27] Brammertz *et al*,[28] have reported that the inclusion of a large interface state distribution in the $In_{0.53}Ga_{0.47}As$ conduction band leads to an increase in the modeled theoretical accumulation capacitance, due to the capacitance contribution from these interface states. This is in agreement with CV responses typically measured on *p*-type and *n*-type $In_{0.53}Ga_{0.47}As$ MOS structures which do not exhibit the asymmetry between the maximum accumulation capacitances. With regard to the samples in this work the theoretical capacitance has been calculated using a one dimensional self-consistent Poisson-Schrödinger CV

simulation.[29] This yields simulated theoretical values of accumulation capacitance (at $V_{gate}$=1.5V) in the range 0.0065 to 0.007 $F/m^2$ for an ~8 nm thick $Al_2O_3$ film with dielectric constant values in the range 8 to 9. The simulated accumulation capacitance of 0.007 $F/m^2$ corresponds to a capacitance equivalent thickness ($C_{et}$) of 4.9 nm (assuming a dielectric constant for $SiO_2$=3.9). Based on the physical thickness of 7.8 nm for the $Al_2O_3$ and assuming dielectric constants for $Al_2O_3$=9 and for $SiO_2$=3.9, yields an equivalent oxide thickness ($E_{ot}$) of ~ 3.4 nm, which is 1.5 nm less than the simulated $C_{et}$. This can be accounted for by an $E_{ot}$ correction which has been reported to be in the range of 1.1 nm to 1.5 nm for devices on $In_{0.53}Ga_{0.47}As$.[27]

It can be seen in the CV responses in Figure 4.3 that the actual measured accumulation capacitance at $V_{gate}$=1.5V exceeds the simulated theoretical capacitance of 0.007 $F/m^2$ in all cases. The presence of interface states having energies aligned with the $In_{0.53}Ga_{0.47}As$ conduction band is the most likely explanation for the measured capacitance exceeding the theoretical capacitance for $Al_2O_3$/*n*-$In_{0.53}Ga_{0.47}As$ structures.[26-28] The difference between the measured and theoretical accumulation capacitance values, $\Delta C$ (in $F/m^2$), is 0.0025, 0.0015, and 0.0020, for the 22%, 5%, and 1% passivated devices respectively. This is reduced to 0.0009 for the 10% device and therefore the smallest deviation from the theoretical capacitance occurs for this sample. This provides evidence that for the 10% passivated device there is a reduction in the density of interface defects degenerate with the conduction band. The presence of such defects is technologically relevant for surface inversion mode *n*-channel $In_{0.53}Ga_{0.47}As$ MOSFETs, as beyond the threshold voltage, any additional charge applied to the gate will be partially compensated by charging of the interface defect level in the $In_{0.53}Ga_{0.47}As$ conduction band. The consequence will be a decrease in transconductance with gate voltage, and an apparent decrease in the inversion layer mobility. Both of these effects are observed experimentally in $In_{0.53}Ga_{0.47}As$ surface inversion mode *n*-channel MOSFETs.[30]
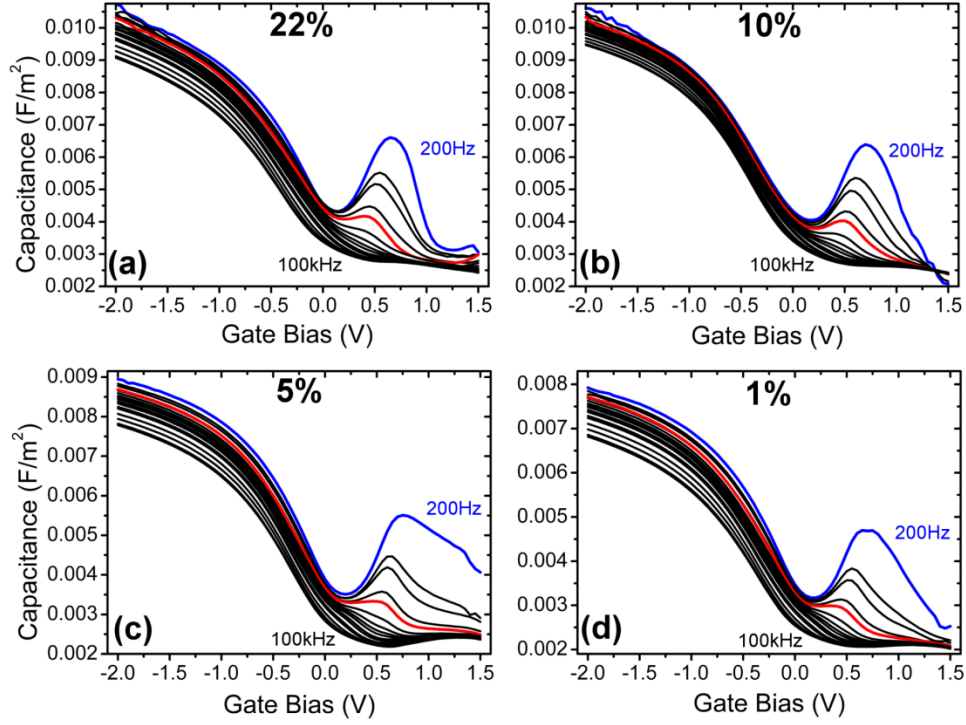
Figure 4.4. Room temperature CV frequency variation (200 Hz to 100 kHz) of (a) 22%, (b) 10%, (c) 5%, and (d) 1%, $(NH_4)_2S$ treated, Au/Ni/ ~8nm $Al_2O_3$/$p$-$In_{0.53}Ga_{0.47}As$/InP devices. All samples were introduced to the ALD chamber load lock as quickly as possible ($<$ 7 minutes) after removal from $(NH_4)_2S$ solution, in order to minimise ambient exposure. Actual diameters of the capacitors tested were: 111 $\mu$m, 113 $\mu$m, 110 $\mu$m, 105 $\mu$m, for the 22%, 10%, 5%, and 1% samples, respectively. The 1 kHz curves have been highlighted in red to illustrate that a more accurate representation of the interface defect response is obtained by measuring down to 200Hz.

The C-V response at room temperature (295K) with ac signal frequencies from 200 Hz to 100 kHz for the 22%, 10%, 5%, and 1% $(NH_4)_2S$ passivated $p$-type $In_{0.53}Ga_{0.47}As$ devices are shown in Figures 4.4 (a), (b), (c), and (d) respectively. The CV response at positive gate bias in this case is mainly attributable to interface state defects, not surface inversion where the capacitance becomes independent of the applied gate bias.[31] There does not appear to be a significant difference between the various aqueous $(NH_4)_2S$ concentrations in terms of their impact in reducing the interface defect response observed on all devices at $V_{gate}$ ~ 0.25 V to 1.5 V. The clear improvement for the 10% treatment in reducing the defect response on $n$-type devices is not as noticeable in the $p$-type case. However, it is apparent in comparing the CV

curves shown in Figure 4.4 that over the whole bias range investigated ($V_{gate}$ -2 to 1.5 V) the 10% treated *p*-type device clearly exhibits the best characteristics in terms of having both the lowest frequency dispersion and the steepest transition from depletion to accumulation. It is particularly important in the case of these *p*-type devices to measure down to very low frequencies (200Hz) in order to capture as much of the interface defect related response as possible. This is necessary in order to obtain a more accurate determination of the extracted interface state density as will be discussed later. In Figures 4.4 (a-d), the 1 kHz curves have been highlighted in red to illustrate that a significantly better representation of the interface defect response is obtained by measuring down to 200Hz (blue curves). It is also the case that the hysteresis measured around the flatband capacitance, $C_{fb}$ at 100 kHz on *p*-type devices is approximately 15% higher for the other $(NH_4)_2S$ concentrations compared to the 10% passivated *p*-type device, which has a hysteresis of ~ 300 mV, as shown in Figure 4.5. The hysteresis for all *n*-type devices is practically constant at ~ 80 mV for the different $(NH_4)_2S$ concentrations. Clockwise hysteresis was observed on *n*-type
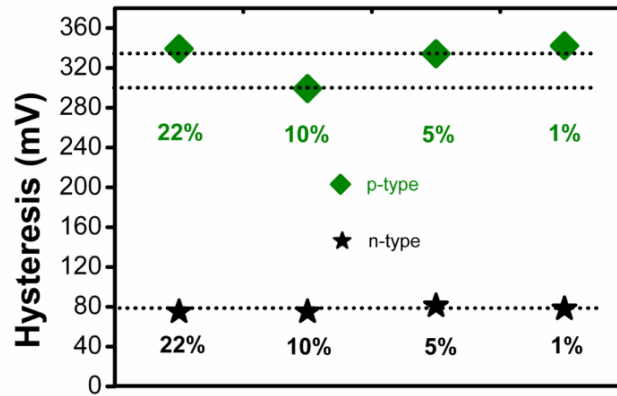


Figure 4.5 Hysteresis measured around $C_{fb}$ at 100 kHz for all the $(NH_4)_2S$ passivated *n*-type and *p*-type samples examined in this study. The green diamond symbols the *p*-type devices and the star symbols represent *n*-type devices. The dotted lines are guides for comparative purposes. The hysteresis measurements were performed by sweeping at 100 kHz from negative to positive gate bias for *n*-type devices (-2.0V to 1.5V), and from positive to negative gate bias for *p*-type devices (1.5V to -2.0V). There was no hold time in accumulation, and two consecutive sweeps were performed, with hysteresis values obtained from the second sweep.

samples while anti-clockwise hysteresis was observed on *p*-type samples. Note that the devices only experienced a 633 K, 30s RTA in $N_2$ during metallisation, and that no specific effort has been made to perform high temperature RTA as is common practice to reduce hysteresis levels.

As described in the experimental section, the time between removal of the $In_{0.53}Ga_{0.47}As$ sample from the aqueous $(NH_4)_2S$ solution and loading into the ALD chamber was minimized (typically under 7 minutes). Therefore the samples saw as little exposure to ambient air and contaminants as was possible within the experimental set-up. This was the case for all devices whose results are presented in Figures 4.3 and 4.4. In order to investigate the effect of increased ambient exposure time, additional *n*-type and *p*-type samples were processed where the time between the removal of the $In_{0.53}Ga_{0.47}As$ samples from a 10% $(NH_4)_2S$ solution to loading into the ALD chamber was extended to ∼ 30 minutes. Figures 4.6 (a) and (b) show the C-V response at room temperature (295K) with ac signal frequencies from 200 Hz to 100 kHz for the 10% $(NH_4)_2S$ passivated *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ devices with 30 minute ambient exposure. In comparing the *n*-type CV response in Figure 4.5(a) of the sample with 30 minutes ambient exposure, with that in Figure 4.3(b) of the sample with 7 minutes ambient exposure, it is immediately apparent that there is a significant increase in the CV frequency dispersion and in the defect related response at negative gate bias for the device subjected to longer ambient exposure. The difference between the measured and theoretical accumulation capacitance values, $\Delta C$ (in $F/m^2$), is 0.0020 for the 30 minute exposure device, compared to just 0.0009 for the 7 minute exposure device, which, as discussed previously, is suggestive of an increase in defects degenerate with the $In_{0.53}Ga_{0.47}As$ conduction band upon longer ambient exposure. In the case of the *p*-type MOS devices, a comparison of Figure 4.6(b) and Figure 4.4(b) also shows a clear increase in frequency dispersion over the entire bias range examined for the longer ambient exposed sample. It is thus clear that extended ambient exposure post-passivation and prior to ALD deposition causes a significant degradation in device electrical properties on both *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$.
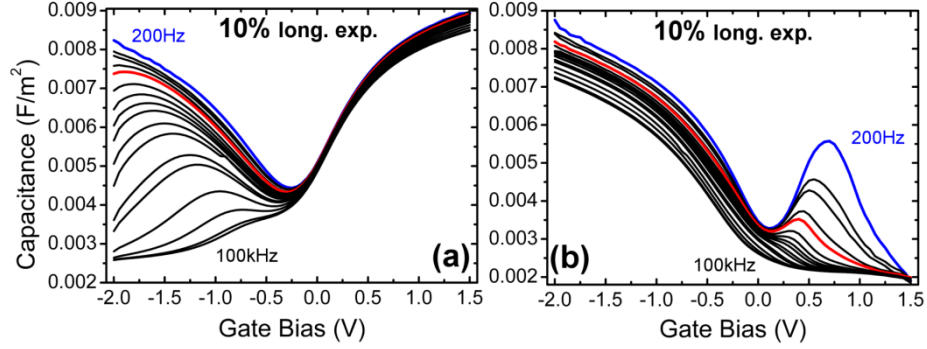
Figure 4.6. Room temperature CV frequency variation (200 Hz to 100 kHz) of (a) 10% $(NH_4)_2S$ treated Au/Ni/Al$_2$O$_3$/*n*-In$_{0.53}$Ga$_{0.47}$As/InP, and (b) 10% $(NH_4)_2S$ treated Au/Ni/Al$_2$O$_3$/*p*-In$_{0.53}$Ga$_{0.47}$As/InP. In both these cases, the time between removal of the InGaAs sample from the 10% $(NH_4)_2S$ solution to loading to the ALD load lock was increased to ~ 30 minutes. Actual diameters of the capacitors tested were: 114 μm, and 106 μm, for the *n*-type and *p*-type samples, respectively. The 1 kHz curves are in red.

## 4.5. XPS analysis

Prior to ALD deposition, in-situ XPS was also performed on the 10% passivated *n*-type samples after 7 minute and 30 minute exposure times to atmosphere. The As 2*p* core level spectra of the 7 and 30 minute exposed *n*-In$_{0.53}$Ga$_{0.47}$As samples are presented in Figures 4.7(a) and (b) respectively. Peak fits were carried out using AAnalyzer software,[29,32] so that all peaks could be fitted consecutively to provide the highest level of conformality between the spectra, using previously determined fitting parameters.[13, 33] The XPS analysis was performed by a collaborator, Dr. Barry Brennan, formerly of UT Dallas, and DCU.

Both samples show the presence of As$_2$O$_3$, As$_2$O$_5$, elemental arsenic (identified as As-As), lower coordinated oxidation states labeled 2+ and 1+, tentatively ascribed to AsO and As$_2$O respectively, as well as a peak corresponding to As surface states (dimers and possibly dangling bonds). The XPS results, as expected, show an increase in the total oxide levels for the longer exposed sample, with the most significant being that of the As$_2$O peak. Given that the As$_2$O state has been seen to form preferentially at the interface between the oxide and the substrate,[33] this could
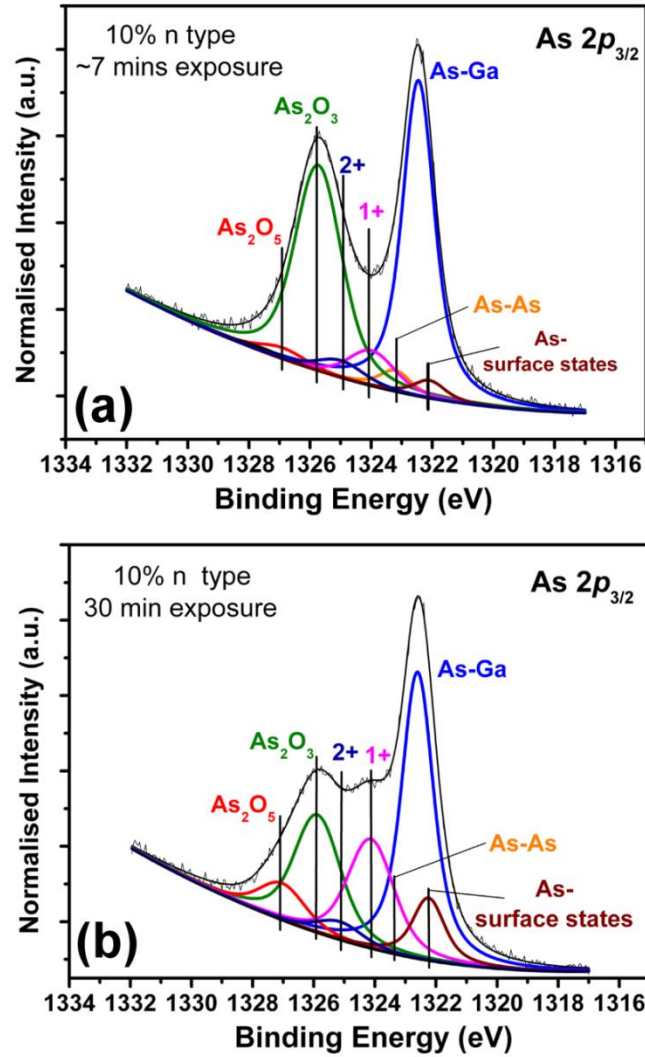
Figure 4.7. The As 2*p* core level x-ray photoelectron spectra of the (a) 7 minute and (b) 30 minute ambient exposed 10% $(NH_4)_2S$ *n*-$In_{0.53}Ga_{0.47}As$ samples. The in-situ XPS was performed prior to ALD deposition. The XPS was performed by Dr. Barry Brennan (formerly of DCU and UT Dallas).

be evidence of the growth mechanism of the oxide, with $As_2O$ forming initially, which then over time converts to form the other oxidation states, consistent with the growth of the $As_2O_5$ peak.

It is also observed from the XPS spectra that there is marked increase in the As surface state related spectral feature for the sample exposed for 30 minutes as compared to the sample exposed for 7 minutes. This is potentially significant as a recent study by Robertson[34] identified As dimers as a possible source of interface defects at the oxide/III-V interface as detected previously using in-situ XPS studies

by Milojevic *et al.* [35] These again could be formed as a result of the oxide growth, with the formation of the $As_2O$ causing a disruption of the interface.[36] In the case of the *n*-type XPS samples analysed here, the corresponding electrical characteristics after ALD and gate MOS device formation are seen in Figures 4.3(b) for the 7 minute exposure sample and 4.6(a) for the 30 minute exposure sample. As discussed earlier, there is a noticeable increase in the interface defect CV response at negative gate bias for the longer exposed device. It is possible that the increase in As surface states, as observed by XPS, could be a contributory factor to this. It must be pointed out that correlation of XPS and electrical results is difficult and while these results may provide a suggestion as to the origin of some interface defects responsible for the CV response, a definitive statement cannot be made as to the real significance of the role of As surface states. The presence of Ga and In surface states are also much more difficult to identify with XPS due to a smaller binding energy separation between the peaks, as well as reduced surface sensitivity due to the lower binding energies involved. As stated previously it is the case that physical identification of interface defects at the oxide/III-V interface remains one of the most challenging topics in this field.

## 4.6. $D_{it}$ extraction using High-Low CV and Conductance Techniques

It has been seen thus far that in terms of overall device electrical performance the 10% $(NH_4)_2S$ passivation is superior on both *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ to that of the other $(NH_4)_2S$ concentrations (1%, 5%, 22%) examined. This is in agreement with the results of the chemical and physical investigations performed by Brennan *et al.*[13] One possible explanation for this is that the lower $(NH_4)_2S$ concentrations (1%, 5%) provide insufficient protection to the $In_{0.53}Ga_{0.47}As$ surface to prevent significant re-oxidation during the 7 minutes ambient exposure, while the much higher 22% concentration leads to increased surface roughness and consequently a degradation in device performance. It is possible that there is a transition point at a $(NH_4)_2S$ concentration of ~10%, where the passivation is effective in suppressing significant

re-oxidation without introducing the detrimental effects of higher $In_{0.53}Ga_{0.47}As$ surface roughness. It has also been established at this point that minimizing the ambient exposure time after removal from the $(NH_4)_2S$ solution prior to ALD is critical to device performance. Given that they exhibited the most promising electrical properties within this sample set, a detailed examination of the interface state density and profiles is presented for the *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ devices which had received the 10% $(NH_4)_2S$ treatment with minimal exposure post passivation. To this end, characterization of the interface state density was performed using two approaches: a temperature-modified version of the High-Low Capacitance Voltage technique; and an approximation to the more traditional Conductance Method. This provides a useful comparison of these two methods to characterize $D_{it}$ for the oxide/$In_{0.53}Ga_{0.47}As$ system. Moreover, if the peak position and magnitude of the $D_{it}$ obtained with the two methods is comparable, this will provide a higher level of confidence in terms of the $D_{it}$ values obtained, which is important for the high-*k*/$In_{0.53}Ga_{0.47}As$ system, where the validity of the conventional C-V and G-V approaches remains an issue of discussion. This analysis will focus on the characterization of mid-gap interface defects, and does not encapsulate defects degenerate with the $In_{0.53}Ga_{0.47}As$ conduction band discussed earlier for *n*-type $In_{0.53}Ga_{0.47}As$ devices.

The first method used to estimate $D_{it}$ is a temperature-modified version of the "Combined High-Low frequency CV method", as discussed in Nicollian and Brews.[37] At low frequency, the interface traps have time to respond to the slowly changing ac signal and therefore add a capacitance to the measured low frequency CV curve, $C_{LF}$. In this work $C_{LF}$ was taken at a frequency of 40Hz and at room temperature (~ 295K). In this regard it is worth emphasizing again the importance of the earlier point about measuring to as low a frequency as possible in order to maximize the interface state response. By contrast, at high frequencies interface defect states cannot respond in any significant way to the ac signal and therefore they contribute little or no capacitance to the high frequency CV measurement, $C_{HF}$. In this work, a slight modification to the High-Low frequency CV method is performed in that a high

frequency curve at a reduced temperature is chosen where the interface defect response is minimized further, and a more accurate $D_{it}$ can therefore be extracted. Thus the $C_{HF}$ is taken at 1 MHz and a temperature of 220 K in this work. Further discussion of this method can be found in Chapter 2 of this thesis. As stated by Nicollian and Brews, one of the advantages of using this method is that no assumptions regarding material properties are required, and $D_{it}$ is estimated simply and directly from measured CV curves without the need for simulation.[37] One caveat for employing this method, which is particularly important for narrow band gap materials such as $In_{0.53}Ga_{0.47}As$, is that it will work most effectively where $C_{LF}$ is chosen for a sample where the capacitance associated with the interface state contribution goes through a peak within the gate bias range examined. This is the case for the samples used in this study with the 10% $(NH_4)_2S$ passivation, as can be seen for the 200 Hz curves in Figure 4.3(b) and Figure 4.4(b).

The second method used here to estimate $D_{it}$ is the more commonly used approximation to the Conductance method.[37, 38] As described in Chapter 2, the equivalent parallel conductance ($G_p/\omega$) is estimated from the measured conductance ($G_m$), and measured capacitance ($C_m$) against voltage sweep (using equation [2.3]).[37, 38] One issue in general for $In_{0.53}Ga_{0.47}As$ devices is which value to use for $C_{ox}$ in this characterization. Clearly in the case of these samples a lower capacitance in accumulation is recorded for the *n*-type sample compared to the *p*-type sample. At the time this analysis was performed, a $C_{ox}$ value ~ 0.0108 F/m$^2$ was used based on using the $Al_2O_3$ thickness determined by TEM and assuming an $Al_2O_3$ dielectric constant of k=9, and this calculated $C_{ox}$ as opposed to the measured accumulation capacitance is used in the determination of interface state density. It was decided for the sake of comparison to use this $C_{ox}$ for analysis of both the *n*-type samples and the *p*-type samples. The equivalent parallel conductance, $G_p$, was converted to peak interface state density using the approximation with the relevant equations outlined in Chapter 2.

The $D_{it}$ profiles versus gate bias are shown for 10% passivated devices on *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ in Figures 4.8 (a) and 4.8 (b) respectively. Firstly with regard to Figure 4.8 (a) it is obvious that there is good agreement between the $D_{it}$ estimated

from the temperature modified High-Low method and the approximation to the Conductance Method. The magnitude of the $D_{it}$ is higher in the case of the conductance-based technique, while the position and profile of the peaks are similar. In the case of the *p*-type devices in Figure 4.8 (b), there is again close agreement in terms of the peak profile while the magnitude is also a little higher for the conductance-based technique. This provides strong evidence that both of these methods are valid routes to extracting $D_{it}$ for structures incorporating a high-k oxide layer on $In_{0.53}Ga_{0.47}As$, provided appropriate caution is used in their application. The fact that both methods employed here make minimal assumptions regarding material properties (only assumption being k=9 for $Al_2O_3$ to calculate $C_{ox}$) and the profiles are
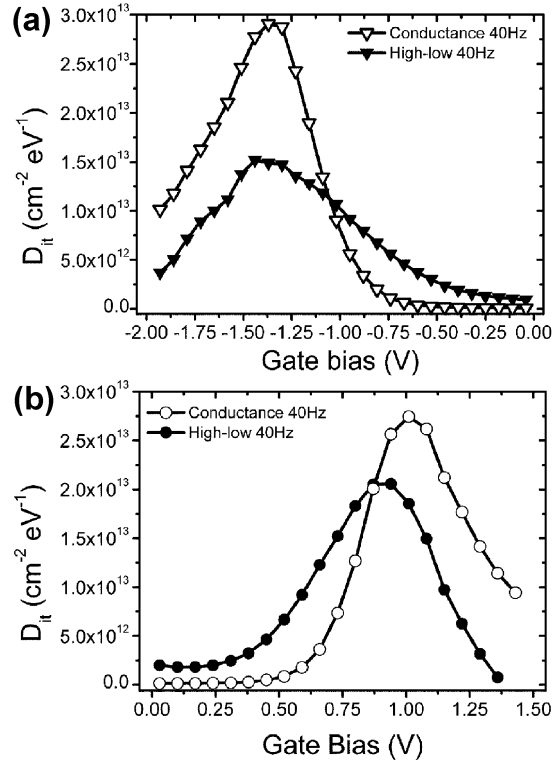


Figure 4.8 $D_{it}$ profiles versus gate bias extracted from the High-Low frequency CV method, and the Conductance method, for 10% $(NH_4)_2S$ passivated devices on (a) *n*-type and (b) *p*-type $In_{0.53}Ga_{0.47}As$ devices. It is seen that there is good agreement between the Conductance and High-Low methods in determining the peak profile and magnitude.

simply extracted from actual electrical measurements gives further confidence that the profiles presented are representative of the device behaviour. It is also a significant result that the peak magnitude and position of the extracted $D_{it}$ using the Conductance Method, which utilizes both measured capacitance and extracted parallel conductance data, yields very similar results to the $D_{it}$ extracted using the High-Low frequency CV method, which uses only measured capacitance data. This provides evidence to support that the extraction of $D_{it}$ using the Conductance Method is valid for high-k on $In_{0.53}Ga_{0.47}As$.

Given that $D_{it}$ profiles versus gate bias have thus far been obtained using two independent approaches, the High-Low frequency CV method and the Conductance method, it follows that a natural extension of this analysis is obtain the $D_{it}$ profile versus the $In_{0.53}Ga_{0.47}As$ energy gap. Recent studies in the literature employed alternative methods to those used in the present work in order to determine $D_{it}$ versus energy profiles for high-k/$In_{0.53}Ga_{0.47}As$ system. Brammertz *et al.*[12] used an admittance spectroscopy technique, while Ali *et al.*[39] employed an equivalent circuit model. In the case of Ali *et al.* the peak $D_{it}$ was estimated at an energy of approximately Ev+0.4 eV, while in both works the reported peak $D_{it}$ magnitudes were in the range $7x10^{12}$ $cm^{-2}$ to $5x10^{13}$ $cm^{-2}$. In the case of the samples in the present work, if we consider that at high frequency (1 MHz) and low temperature (~ 220 K) that the interface state contribution is negligible, then it follows that the measured capacitance is comprised of the semiconductor capacitance, $C_s$, in series with the oxide capacitance, $C_{ox}$. Therefore it is possible to calculate the semiconductor depletion width and hence the semiconductor potential. This in turn allows the calculation of a corresponding energy position for the $D_{it}$ profiles plotted versus gate bias in Figures 4.8(a) and (b).[37] Using the procedure described above the $D_{it}$ profiles versus $In_{0.53}Ga_{0.47}As$ bandgap energy are plotted in Figures 4.9 (a) and 4.9 (b). It is noted that the method used to translate the $D_{it}$ profiles from gate bias to an energy position in the bandgap, is sensitive to the doping concentration. It has been reported that in estimating the energy position for defects even on Si-based devices that the
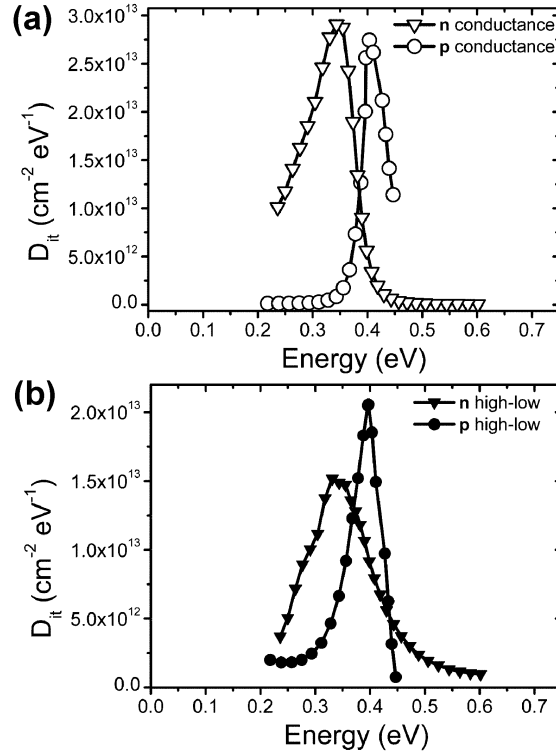
Figure 4.9. Interface state density profiles for 10% $(NH_4)_2S$ passivated $n$-type and $p$-type devices extracted using (a) the conductance method, and (b) the high-low method, and plotted versus $In_{0.53}Ga_{0.47}As$ bandgap energy. The energy is plotted with reference to the $In_{0.53}Ga_{0.47}As$ valence band edge.

error in the peak position can be of the order of $\pm$ 0.05eV.[40] Therefore some caution must be exercised in quoting peak energy positions for the $D_{it}$ response. Table 1 summarizes the energy positions of the peak $D_{it}$ with respect to the valence band edge, and the integrated $D_{it}$ values were obtained by integrating over the range $E_v +$ ~0.2 eV to $E_v +$ ~0.65 eV for $n$-type and $p$-type devices. It is seen in comparing Figures 4.9 (a) and (b) that there is good agreement between the Conductance method and High-Low frequency CV method in terms of the extracted peak profiles and magnitudes. This may be expected given their similarity with gate bias as seen in Figure 4.8. The Conductance method and High-Low method yield identical values for the peak $D_{it}$ energy position over $n$-type (Ev+0.34 eV), and over $p$-type (Ev+0.40 eV). The analysis gives an indication of the $D_{it}$ for these particular samples over $In_{0.53}Ga_{0.47}As$ bandgap from $E_v +$ ~0.2 eV to $E_v +$ ~0.65 eV with integrated $D_{it}$ values ranging from $1.6 \times 10^{12}$ to $3.4 \times 10^{12}$ $cm^{-2}$.

Table 1. Summary of the integrated $D_{it}$ values (italics) obtained by integrating over the range $E_v + \sim 0.2$ eV to $E_v + \sim 0.65$ eV, and also the energy positions of peak $D_{it}$ with respect to the valence band edge, for *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ devices.

| | Integrated $D_{it}$ ($cm^{-2}$) | | Defect Energy (eV) | |
|---|---|---|---|---|
| | *n-type* | *p-type* | n-type | p-type |
| **High-low** | *2.4x10^{12}* | *1.6x10^{12}* | Ev+0.34 | Ev+0.40 |
| **Conductance** | *3.4x10^{12}* | *1.6x10^{12}* | Ev+0.34 | Ev+0.40 |

It is worth mentioning that a third method was used in order to estimate $D_{it}$ for the 10% $(NH_4)_2S$ devices. This is a charge separation and quantification technique developed by Hurley *et al.*, and is described in detail in those publications.[21, 41] Using this method the $D_{it}$ was estimated at $2.9x10^{12}$ $cm^{-2}$, which is within the range obtained using the High-Low and Conductance techniques. Therefore this gives an additional degree of confidence in the extracted values given that three independent techniques yield very similar integrated $D_{it}$ [$cm^{-2}$] values for these devices.

Finally, some examples of work by other research groups provide supporting evidence for the conclusions of the passivation study described in this chapter. Ye *et al.* referenced this work as the motivation for investigating the effect of $(NH_4)_2S$ concentration in the fabrication of buried channel 3-dimensional $In_{0.52}Ga_{0.48}As$ MOSFET devices.[42] They compared a 20%, 10%, and 5% $(NH_4)_2S$ solution concentration. The results of that independent study also concluded that the MOSFET devices treated with a 10% $(NH_4)_2S$ passivation displayed superior interface properties and device behavior with improved subthreshold swing and drain induced barrier lowering.[42] More recently Dai *et al.* used the 10% $(NH_4)_2S$ passivation technique described in this chapter in the fabrication of their InGaAs FINFETs with integration of III-V layers on Si.[43] These also provide real examples of the value of fundamental work looking at III-V interfaces via characterization of MOS devices, which are relatively simple structures, in that the findings are relevant and can be

applied to far more complicated device structures,[42] and incorporated in more extensive processing flows.[43]

## 4.7. Conclusions

In this investigation into the effectiveness of varying ammonium sulphide $(NH_4)_2S$ concentrations (from 1% to 22%) in the passivation of *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$, multi-frequency capacitance-voltage results indicated that the lowest frequency dispersion over the bias range examined occurs for *n*-type and *p*-type devices treated in 10% $(NH_4)_2S$ solution. It has also been shown that there is a deleterious effect on device behaviour for increased ambient exposure time after removal from 10% $(NH_4)_2S$ solution and that XPS analysis has detected changes in the composition of the re-grown oxide on this timescale. Estimations of interface state density, $D_{it}$, extracted from an approximation to the Conductance Method, and independently from the temperature-modified High-Low frequency CV method, show very good agreement both in terms of magnitude and characteristic peak profile for the optimum 10% $(NH_4)_2S$ passivated $In_{0.53}Ga_{0.47}As$ devices. This indicates that the Conductance Method can be applied to devices incorporating high-k oxides on $In_{0.53}Ga_{0.47}As$. The results suggest that these *n*-type and *p*-type devices have an integrated $D_{it}$ of ~ $2.5x10^{12}$ cm$^{-2}$ ($\pm1x10^{12}$ cm$^{-2}$), with the peak density value occurring at approximately 0.37eV ($\pm$0.03 eV) from the valence band edge

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# Chapter 5

## 5. The $Al_2O_3/In_{0.53}Ga_{0.47}As$ system: Interface state reduction, surface inversion, and analysis of the minority carrier response

### 5.1. Introduction

To date, few studies in the literature have demonstrated true minority carrier behaviour in the capacitance voltage (CV) response of MOS capacitors on either *n*-type or *p*-type $In_{0.53}Ga_{0.47}As$. A true minority carrier response (as shown in Chapter 2), would be achieved when the interface state density is reduced sufficiently to allow the Fermi level to be moved throughout the energy gap. To achieve genuine surface inversion has been one of the main challenges of high-k/III-V research over the last 40 years.

In the case of *n*-type $In_{0.53}Ga_{0.47}As$, a CV response at negative gate bias consistent with mid-gap interface states is typically observed, regardless of the gate oxide or passivation method employed.[1, 2, 3, 4, 5, 6, 7] In the case of *p*-type $In_{0.53}Ga_{0.47}As$, at positive gate bias CV characteristics consistent with a mid-gap interface state response have been observed.[8, 9, 10, 11] Recently Trinh *et al.*[12, 13] and Lin *et al.*[7] presented CV responses consistent with true minority carrier behaviour for *n*-$In_{0.53}Ga_{0.47}As$ and *p*-$In_{0.53}Ga_{0.47}As$ respectively. In this chapter we report on a study of the minority carrier response of both *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor (MOS) devices formed using an optimized 10% ammonium sulfide ($(NH_4)_2S$) treatment.[11, 14] $D_{it}$ is sufficiently reduced such that a clear minority carrier response is observed for both *n*-type and *p*-type devices following this optimized $(NH_4)_2S$ passivation. The temperature dependent CV and GV responses are analyzed using an Arrhenius relationship, allowing an extraction of activation energies in order to discriminate the mechanisms responsible for the minority carrier response, be it generation-recombination through mid-gap defects or diffusion from the

semiconductor bulk. The analysis performed on these $n$-In$_{0.53}$Ga$_{0.47}$As and $p$-In$_{0.53}$Ga$_{0.47}$As devices is based on the procedure described by Nicollian and Brews for SiO$_2$/Si devices,[15, 16] who in turn developed their work based on the theory derived by Hofstein and Warfield.[17]

In order to provide further evidence for whether the In$_{0.53}$Ga$_{0.47}$As surface is truly inverted, MOS capacitors were fabricated on $n$- and $p$-In$_{0.53}$Ga$_{0.47}$As with semiconductor doping concentrations ranging over two orders of magnitude from ~$1\times10^{16}$cm$^{-3}$ to ~$2\times10^{18}$cm$^{-3}$. This was in order to examine if the minimum capacitance scaled correctly with doping, following an approach reported by Callegari $et$ $al$.[18] Utilizing different doping concentrations the measured minimum capacitance (C$_{min\text{-}meas}$) at high frequency can be compared with the theoretical minimum capacitance (C$_{min\text{-}theor}$) calculated by assuming the semiconductor surface is inverted.

## 5.2.    Experimental Details

### 5.2.1.  Samples for analysis of Minority Carrier Response

The In$_{0.53}$Ga$_{0.47}$As epitaxial layers used in this work were either, (1) ~2μm $n$-type In$_{0.53}$Ga$_{0.47}$As (S at ~$4\times10^{17}$cm$^{-3}$) grown by metalorganic-vapour-phase-epitaxy (MOVPE) on $n$-doped (S at ~$2\times10^{18}$ cm$^{-3}$) InP(100) wafers, or (2) ~2μm $p$-type In$_{0.53}$Ga$_{0.47}$As (Zn at ~$4\times10^{17}$cm$^{-3}$) also grown by MOVPE on $p$-doped (Zn at ~$2\times10^{18}$ cm$^{-3}$) InP(100) wafers. These wafers were supplied by IQE Wales, who performed the MOVPE growth according to specifications we requested. The actual doping concentrations of the epitaxial layers were measured on sacrificial test pieces by the supplier IQE, and the specifications varied slightly from the nominal and were found to be $4.4\times10^{17}$cm$^{-3}$ for the $n$-In$_{0.53}$Ga$_{0.47}$As and $3.3\times10^{17}$cm$^{-3}$ for the $p$-In$_{0.53}$Ga$_{0.47}$As. In$_{0.53}$Ga$_{0.47}$As surfaces were initially rinsed for 1 minute each in acetone, methanol, and isopropanol. (NH$_4$)$_2$S concentrations of 10% in deionised H$_2$O were used (20 minutes, ~ 295K). These optimized passivation parameters were determined from

previous physical and electrical studies.[11, 14] The $Al_2O_3$ layers were grown by atomic layer deposition (ALD) at 300$^o$C (Cambridge NanoTech, Fiji F200LLC), using alternating pulses of TMA ($Al(CH_3)_3$) and $H_2O$. TEM confirmed the thickness was close to the nominal 8nm.

From the results presented in Chapter 4, it was evident that there was a marked improvement in the CV response when the transfer time from the $(NH_4)_2S$ passivation to the ALD chamber was reduced from 30 minutes to 7 minutes. This provided the motivation to assess if this transfer time could be further reduced, and if the resulting interface state density could be further reduced to the point where surface inversion could be achieved in the $In_{0.53}Ga_{0.47}As$ MOS structure. The time taken to rinse the samples in DI water, blow dry with nitrogen and transfer to the ALD chamber could be reduced to 3 minutes, and this was the time used in the experiments presented in this chapter of the thesis.

Finally, gate contacts ~ 160 nm thick were formed by e-beam evaporation of Ni (70nm), and Au (90nm), using a lift-off process. In the case where forming gas annealing was performed it was carried out post-metallization in a tube furnace at 275$^o$C for 30 minutes in a 5% $H_2$:95% $N_2$ ambient. This anneal condition was deliberately selected based on previous experience of FGA on $HfO_2/In_{0.53}Ga_{0.47}As$ stacks (those detailed in Chapter 3) which saw a deterioration in device characteristics at temperatures higher than 325$^o$C. It was hoped that the more conservative 275$^o$C, 30 minute, FGA would allow an assessment of any improvement in device characteristics while avoiding the complication of a significant increase in leakage current, which was also a factor in choosing the furnace anneal as opposed to an RTA. Electrical measurements were recorded using an Agilent E4980A, and were performed on-wafer in a microchamber probe station (Cascade, Summit 12971B) in a dry air, dark environment (dew point ≤203K). It is noted that lower gate leakage current densities were recorded (not shown) on samples which received the optimum passivation compared to samples which did not receive the passivation step but were otherwise identical in structure.

### 5.2.2. Samples for variable doping experiment

For the purposes of the variable doping experiment, Tyndall's in-house MOVPE growth facility was used. For the *p*-type samples, using *p*-doped (Zn at ~2x10$^{18}$ cm$^{-3}$) InP(100) as a starting substrate, ~2μm *p*-type In$_{0.53}$Ga$_{0.47}$As layers were grown by MOVPE with the following dopant (Zn) concentrations (cm$^{-3}$): 1.4x10$^{16}$, 3.3x10$^{16}$, 1.8x10$^{17}$, 2.7x10$^{17}$, and 2.0x10$^{18}$. Using *n*-doped (S at ~2x10$^{18}$ cm$^{-3}$) InP(100) as a starting substrate, ~2μm *n*-type In$_{0.53}$Ga$_{0.47}$As layers were grown by MOVPE with the following dopant (Si) concentrations(cm$^{-3}$): 7.8x10$^{15}$, 3.0x10$^{16}$, 2.0x10$^{17}$, 6.0x10$^{17}$, and 2.0x10$^{18}$. These doping concentrations were determined by Electrochemical Capacitance-Voltage (ECV) Profiling, by Dr, Kevin Thomas, who also performed the MOVPE growths. In$_{0.53}$Ga$_{0.47}$As surfaces were initially rinsed for 1 minute each in acetone, methanol, and isopropanol. (NH$_4$)$_2$S concentrations of 10% in deionised H$_2$O were used (20 minutes, ~ 295K). Samples were loaded to the ALD reactor within ~ 3 minutes after removal from the (NH$_4$)$_2$S solution. The Al$_2$O$_3$ layers were grown by atomic layer deposition (ALD) at 300$^{\circ}$C (Cambridge NanoTech, Fiji F200LLC), using alternating pulses of TMA (Al(CH$_3$)$_3$) and H$_2$O. TEM indicated an Al$_2$O$_3$ thickness of ~ 7nm for the growth run on *p*-type samples and a thickness of ~ 5nm for the growth run on *n*-type samples. Finally, gate contacts ~ 160 nm thick were formed by e-beam evaporation of Ni (70nm), and Au (90nm), using a lift-off process.

## 5.3. Simulated CV and GV responses

Before examining the experimental data it is useful to examine the simulated responses of capacitance and conductance with voltage to illustrate the expected behavior for *n* and *p*-type In$_{0.53}$Ga$_{0.47}$As. Figure 5.1 illustrates these responses obtained using a Synopsys Sentaurus Device Simulator.[19, 20] The parameters input to the simulation mirrored those of the experimental MOS devices in terms of the semiconductor doping and oxide capacitance. Zero D$_{it}$ was assumed in this case. In

terms of the CV a clear plateau corresponding to the inversion response is seen for both *n*-type and *p*-type In$_{0.53}$Ga$_{0.47}$As, Figure 5.1 (a) and (b). Such a plateau in the CV has been experimentally observed previously for inverted MOS devices incorporating Ge and Si as semiconductor layers.[15, 16] The frequency scaled conductance, G/ω, curves are plotted over a narrower bias range to focus on the inversion region, and again a characteristic plateau region is observed with gate biases approaching strong inversion, Figure 5.1 (c) and (d). Also notable is that the conductance divided by the angular frequency increases to a maximum value in strong inversion and then begins to decrease again (open symbols in the G/ω plot indicate frequencies where conductance is decreasing). This is consistent with inversion behavior observed in the work of Nicollian and Brews for SiO$_2$/*n*-Si MOS devices and with the simulations



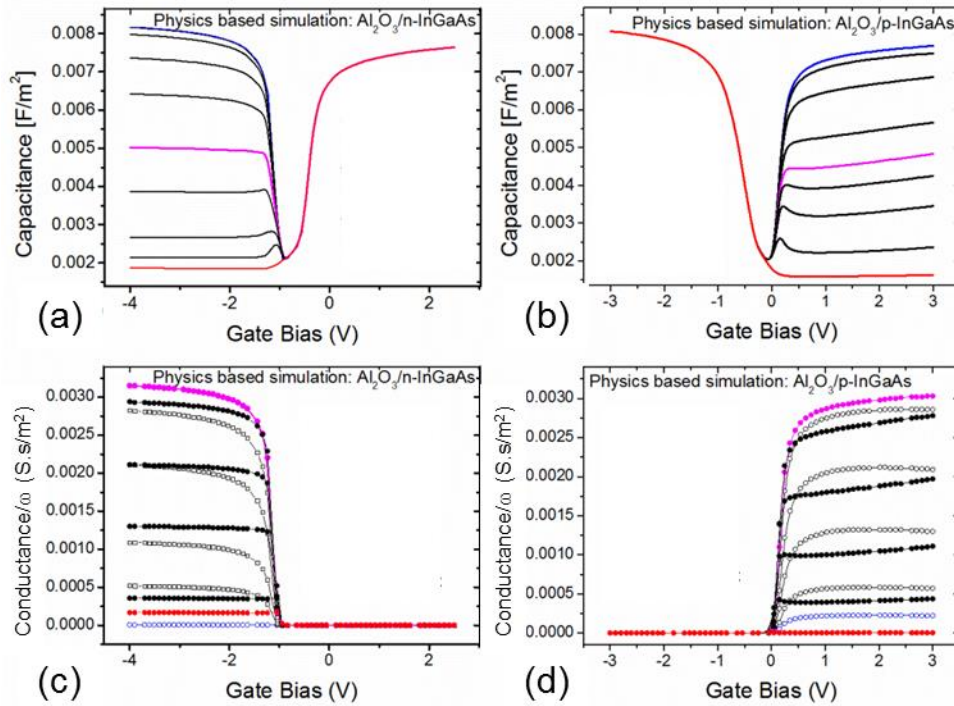Figure 5.1. Simulated multifrequency Capacitance Voltage responses (100 Hz to 1 MHz, 295K) for (a) *n*-type and (b) *p*-type In$_{0.53}$Ga$_{0.47}$As. The corresponding frequency scaled conductance versus voltage plots are plotted in (c) and (d) for *n*-In$_{0.53}$Ga$_{0.47}$As and *p*-In$_{0.53}$Ga$_{0.47}$As respectively These simulations were provided by Dr. Rafael Rios of Intel Components Research.

presented in Chapter 2 for Si. They define the frequency for which the measured conductance ($G_m/\omega$) in inversion is a maximum as the transition frequency.[15]. This is also the frequency at which the capacitance in strong inversion is mid-way between the capacitance measured at high and low frequency.[15] This behavior is observed in the simulated responses in Figure 5.1, and the CV and GV at the transition frequencies are the magenta curves in the plots. In Figure 5.1 one also observes a slight asymmetry in the maximum capacitance in accumulation for the *p*-type and *n*-type. The capacitance is expected to be lower in this case due to a lower density of states in the $In_{0.53}Ga_{0.47}As$ conduction band.

### 5.4.    Measured CV and GV response

The multi-frequency CV and GV curves measured on the experimental samples at room temperature (295 K) with ac signal frequencies from 20 Hz to 1 MHz for the *n*-type and *p*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$ devices are shown in Fig. 5.2.[21] Firstly, for the *n*-type device, as the gate bias is swept to more negative voltages, the CV is seen to rise and then plateau in the bias range of ~ -1.5 to -4V. This is consistent with a minority carrier response and is in marked contrast to the frequency dispersion typically observed in the literature for *n*-type $In_{0.53}Ga_{0.47}As$,[1-7] where broad peaks associated with an interface state response are observed in the CV at negative gate bias. A distortion in the CV in the transition to inversion is observed at intermediate and higher frequencies, seen in Figure 5.2 in the bias range around -0.6 $V_{gate}$ to -1 $V_{gate.}$ This is attributed to a mid-gap interface defect response, (a corresponding peak is evident in conductance curves), whereas at lower frequency it is not distinguishable due to the inversion response becoming dominant. However the CV is seen to pass through this interface defect feature and then rise to a plateau over the remaining bias range, indicating that the mid-gap $D_{it}$ is sufficiently low following the optimized 10% $(NH_4)_2S$ (~ 3 minute ALD transfer time) to allow movement of the Fermi level through the mid-gap interface defect for these samples within the bias range applied.
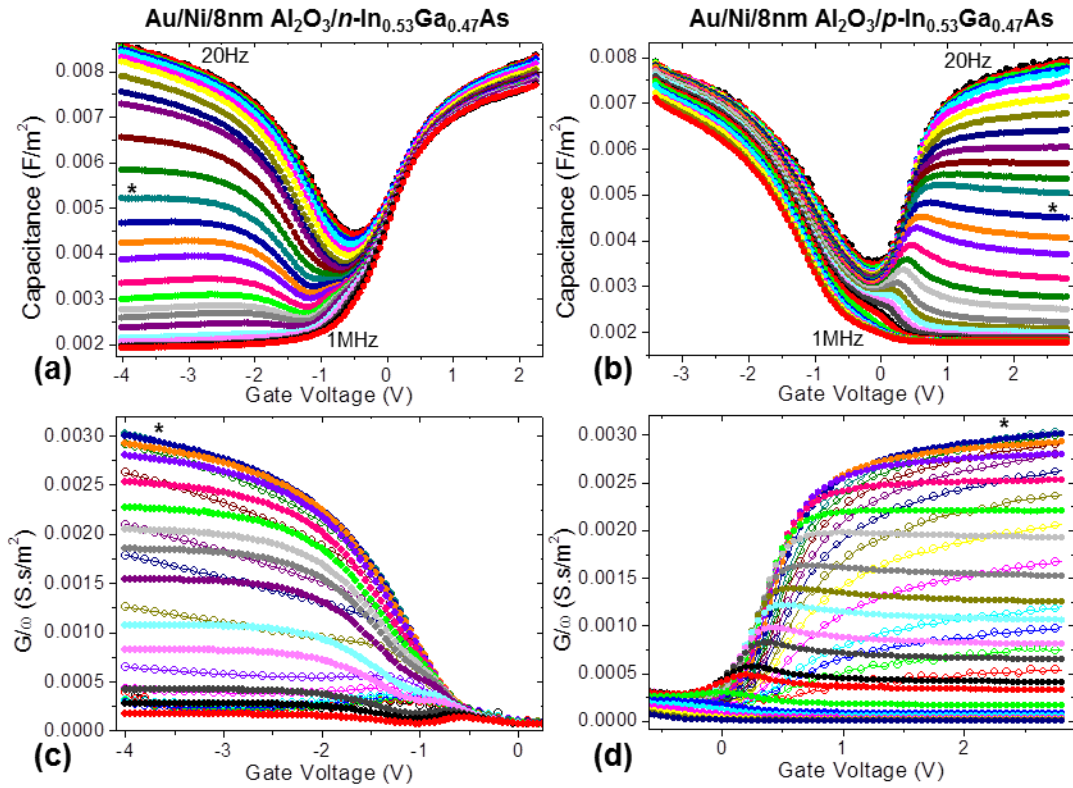
Figure 5.2. Multi-frequency CV (20 Hz to 1 MHz, 295K) for (a) *n*-type and (b) *p*-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As/InP devices (optimum 10% (NH$_4$)$_2$S treatment, ~ 3 minute ALD transfer, 8 nm Al$_2$O$_3$). The dispersion in accumulation is relatively low over both the *n*-type and *p*-type compared to that typically observed for high-*k*/In$_{0.53}$Ga$_{0.47}$As devices, particularly given that the measurement is over an extended frequency range of 20 Hz to 1 MHz. The theoretical C$_{min}$ is ~ 0.00196 F/m$^2$ and 0.00177 F/m$^2$ for the *n*-type and *p*-type devices respectively, calculated using the actual *n*-type and *p*-type In$_{0.53}$Ga$_{0.47}$As dopings of ~4.4x10$^{17}$cm$^{-3}$.and 3.3x10$^{17}$cm$^{-3}$ respectively. The frequency scaled conductance, G/ω, can also be expressed in units of F/m$^2$. The *p*-In$_{0.53}$Ga$_{0.47}$As device received a 275$^{\circ}$C forming gas anneal (5% H$_2$:95% N$_2$, 30 mins). Leakage current densities are low (< 6x10$^{-7}$ A/cm$^2$) over the entire bias range examined for both *n*- and *p*-type samples.

In the case of the *p*-type device in Fig. 5.2 (b), the CV is also observed to plateau with increasing positive gate bias, indicative of a minority carrier response. At intermediate frequencies, in the gate bias range of 0V to 1V, a small hump is evident on entering the plateau region. It is noted that this hump is also observed in the simulations, where zero D$_{it}$ contribution was assumed. The effect of FGA on the

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transition into the inversion region for $p$-type samples is addressed in a later section. The measured minimum capacitance at 1 MHz (red curves in Fig. 5.2) for these $n$-type and $p$-type devices both reach the theoretical minimum capacitance, which is a strong indication that the Fermi level has been swept to the opposite band edge in both cases.

A greater dispersion of capacitance is observed in the transition to accumulation for the $p$-type samples than for the $n$-type. This is in line with most literature observations that there is a higher $D_{it}$ density closer to the valence band edge than towards the conduction band edge for $In_{0.53}Ga_{0.47}As$. However this dispersion for the $p$-type sample in Figure 5.2 is still lower than that observed in most reports in the literature, and it is also noted that the frequency range here is 20Hz to 1MHz, again being a wider frequency range than that typically reported, where in a few cases 100Hz, and more frequently 1kHz, are the lowest frequencies examined.

The frequency scaled conductance for the $n$ and $p$-type devices is shown in the lower plots on Figure 5.2, and the bias range is focused on the inversion region. It is evident that the conductance also displays the plateau regions characteristic of inversion. A notable feature of the $G/\omega$ responses measured on the experimental samples, also predicted by simulations, is that $G/\omega$ exhibits a peak in inversion, with the peak occurring at the transition frequency.[15, 22] For the $In_{0.53}Ga_{0.47}As$ devices in this study $G_m/\omega$ is also at a maximum value at the transition frequencies of ~25 kHz ($n$-type) and ~600 Hz ($p$-type). These are indicated with an asterisk in Figure 5.2, where the $G/\omega$ curves for frequencies after this peak value are plotted with open symbols. It is significant that the CV and GV behaviour in inversion is consistent with what is expected from the simulations in Figure 5.1 and Si simulations in Chapter 2, and consistent with what is observed by Nicollian and Brews for an inverted $SiO_2/n$-Si surface[15, 16]: a plateau region is observed in both the capacitance and conductance, and the peak $G_m/\omega$ occurs at the transition frequency, with the mid-capacitance value in inversion also occurring at $\omega_m$. As part of the simulations performed, a fitting exercise was conducted to correlate the measured transition frequencies to a minority carrier generation lifetime, $\tau_g$. This yielded $\tau_g$ values of

11ps for the *n*-type device and of 930ps for the *p*-type device, reflecting the difference in measured transition frequencies for the two devices.

Further support that this represents inversion of the $In_{0.53}Ga_{0.47}As$ surface exists in correlating the results with work done by Dr. Vladimir Djara, who developed a process for III-V MOSFETs at Tyndall.[23, 24] In that study, MOS capacitors were produced in parallel on the same wafers with the MOSFETs so that they saw identical processing conditions to the FETs. This is illustrated in Figure 5.3, which shows (a) the MOS device in this work, ie. the plot as Figure 5.2 (b), and a comparison
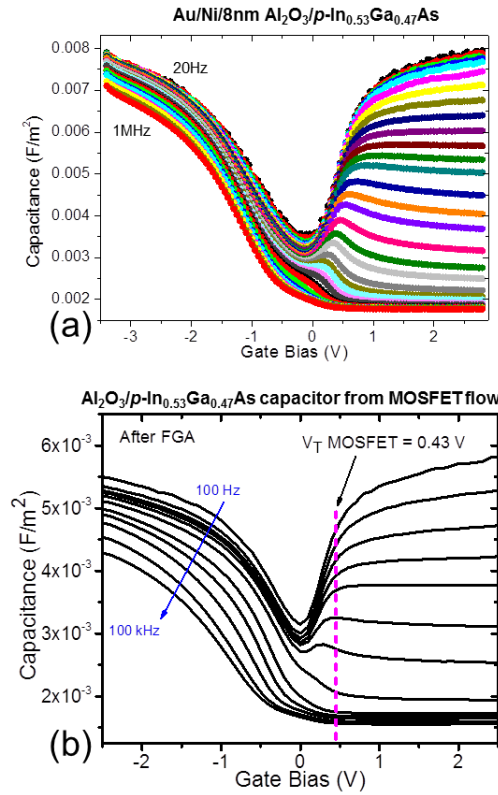


Figure 5.3 (a) Multi-frequency CV (20 Hz to 1 MHz, 295K) for a *p*-type Au/Ni/$Al_2O_3$/$In_{0.53}Ga_{0.47}As$/InP device in this work, (ie. same plot as Figure 5.2 (b)), and (b) Multi-frequency CV (from 100 Hz to 100 kHz) for an $Al_2O_3$(10 nm)/*p*−$In_{0.53}Ga_{0.47}As$/InP MOS capacitor from the full surface channel $In_{0.53}Ga_{0.47}As$ MOSFET process developed by Dr. Vladimir Djara at Tyndall.[23, 24] The threshold voltage of the neighboring MOSFET is 0.43 V. The CV response for a gate bias > 0.43 V is the CV response for the $Al_2O_3$/*p*−$In_{0.53}Ga_{0.47}As$ interface in inversion.

with 5.3 (b) which is a MOS capacitor from the process flow in the MOSFET study.[24, 25, 26] In that case the threshold voltage ($V_T$) of the neighbouring MOSFET was 0.43 V and is indicated on Figure 5.3 (b) by the magenta dotted line. This corresponds to the regime of strong inversion for the MOSFET device, therefore the CV responses at a gate bias > 0.43 V in Figure 5.3 (b) represent the CV for an inverted $Al_2O_3$/$p$-$In_{0.53}Ga_{0.47}As$ surface. The similarity with the CV in Figure 5.3(a) is further evidence that the multi-frequency CV for the MOS device in this work is representative of inversion for the $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ devices. This also provides a nice example of how MOSFET behavior can complement our understanding of the MOS results, and vice versa. In the same vein, it is worth noting that the 10% $(NH_4)_2S$ passivation and FGA parameters developed in the work described in this thesis were incorporated into the MOSFET process flow, which again shows the relevance of work on MOS structures in that it can be extended to benefit more complex systems.

Figures 5.4 (a) and (b) show $G_p/\omega$ versus $\omega$ curves for these $n$-type and $p$-type samples respectively, obtained using the Full Conductance Method.[15, 27] For this measurement the gate bias was fixed and the capacitance and conductance were recorded as the ac signal frequency was swept from ~ 100 Hz to 1MHz. Previous work indicated that a $D_{it}$ peak existed near mid-gap for similar $In_{0.53}Ga_{0.47}As$ device structures.[11] A comparable energy level was therefore chosen in order to estimate the midgap $D_{it}$ for the samples in the current work. In the case of the $n$-type devices the peak $D_{it}$ at ~ $E_v$ + 0.4eV is ~ $9x10^{11}$ $cm^{-2}$ $eV^{-1}$, while for the $p$-type device the peak $D_{it}$ at ~ $E_v$+0.4eV is ~ $6x10^{11}$ $cm^{-2}$ $eV^{-1}$, derived using the $G_p/\omega$ curve peaks and profiles. It is important to stress that this is primarily useful here only as a qualitative estimation of the $D_{it}$. The minority carrier response observed for these devices renders application of conventional $D_{it}$ extraction techniques such as the Conductance Method problematic, and makes it very difficult to accurately quantify $D_{it}$.[28] One point of note is that it transpires that the gate bias corresponding to the mid-gap profile plotted in Figure 5.4 (a) is -0.6V, which aligns with the gate bias where the defect related distortion is observed in the CV in Figure 5.2.
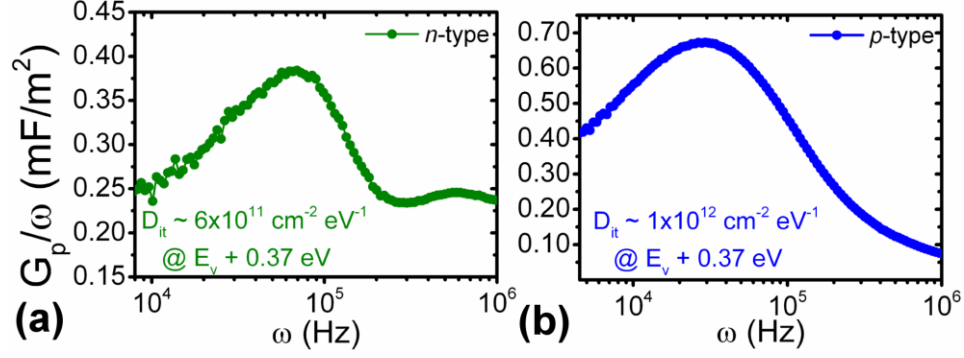
Figure 5.4. $G_p/\omega$ versus $\omega$ curves (at $V_{gate} \sim$ -0.6 V, equivalent to $\sim E_v +$ 0.4eV) for (a) *n*-type and (b) *p*-type, Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As devices. $D_{it}$ was extracted from $G_p/\omega$ versus $\omega$ profiles using the Conductance Method[15]; $f_D(\sigma_s) \sim$ 0.37.

## 5.5. Sources of Minority Carrier Response

There are three possible sources of minority carriers[15]: (1) Diffusion of minority carriers from the semiconductor bulk; (2) Generation and recombination of minority carriers through mid-gap defects in the depletion region; (3) supply of minority carriers from an external source beyond the gate eg. peripheral charge induced by device processing steps. It is necessary to eliminate the possibility of the inversion response arising as a result of (3), in order to perform analysis with regard to (1) and (2).

### 5.5.1. Peripheral Inversion

During the development of high-*k* processes on semiconductor surfaces it is possible to have a metal gate patterned on the high-*k* oxide surface with no additional passivation, leaving the oxide regions outside the gate area exposed to ambient conditions as well as processing steps such as reactive ion etching, rapid thermal processing, and forming gas annealing. These processing steps have the potential to induce charge within the oxide, or leave residual charge on oxide surfaces, in particular where the oxide is exposed during such a processing step. If this oxide

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charge results in depletion of the semiconductor surface and the density of the residual charge is higher than the semiconductor charge associated with the maximum depletion width ($\sim 8 \times 10^{10}$ cm$^{-2}$ for $1 \times 10^{15}$ cm$^{-3}$ doping concentration), then peripheral inversion will be present outside the area defined by the gate electrode.[29]

Capacitance-voltage measurements performed at multiple frequencies and on varying capacitor areas on both *n*-type and *p*-type devices can be used to determine if such peripheral inversion is responsible for the low frequency behaviour, as the low frequency behaviour provided through peripheral inversion would exhibit specific CV behaviour in the following ways:

(i) For a given device area, the inversion response will reduce with increasing ac measurement frequency.

(ii) At a given ac signal frequency the inversion response will be reduced as the device area increases, due to the increasing diffusion distance from the periphery to the centre of the gate electrode.

(iii) The low frequency inversion like behaviour will be observed for either *n* or *p* doped semiconductor substrates, and not for both, as a given oxide charge will only invert the oxide/semiconductor surface for one dopant type.

While the observations described in (i) will be observed for minority carriers supplied either from under the gate area (by generation/recombination or diffusion from the quasi-neutral bulk), or via a peripheral inversion charge, the observations described in (ii) and (iii) are not consistent with minority carrier supply from the depletion region under the gate electrode. The supply of minority carriers by generation/recombination in the depletion region or by diffusion from the quasi-neutral bulk, should not exhibit a dependence on the electrode area, and should also be present for both *n* and *p* type semiconductor substrates.

A more extensive discussion of peripheral inversion and illustrative examples of this behavior for Si and GaAs based devices is included in Appendix 2 and in the associated publication.[29] However, for the In$_{0.53}$Ga$_{0.47}$As samples under investigation in the current study, it was critical to eliminate the possibility of an a.c. inversion

response due to peripheral charge effects. In Figure 5.5 the multi-frequency CV responses for Au/Ni/Al$_2$O$_3$/$n$-In$_{0.53}$Ga$_{0.47}$As are displayed as a function of increasing capacitor area, (a) 30x30µm, (b) 70x70µm, and (c) 200x200µm. This represents an approximately 50-fold increase in area, and it is clear that near identical CV frequency dependence is observed regardless of the device dimensions. In addition the minority carrier response is also observed over $p$-type In$_{0.53}$Ga$_{0.47}$As, and similarly there is no area dependence of the $p$-type multi-frequency CVs. This rules out any contribution of peripheral or external charge effects, thus leaving diffusion of minority carriers from the semiconductor bulk, and generation and recombination of minority carriers through mid-gap defects in the depletion region above as the remaining sources for the minority carrier response.
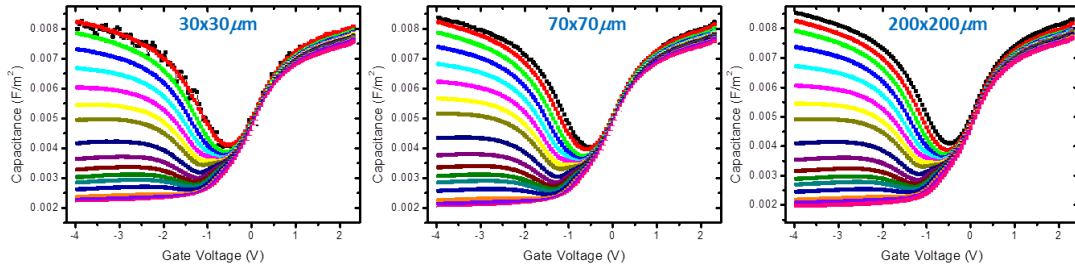


Figure 5.5 The C-V multi-frequency response at room temperature (295 K) of $n$-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As devices for capacitor squares with dimensions of (a) 30x30 µm, (b) 70x70 µm, and (c) 200x200 µm respectively. Identical frequency dependent behavior is observed for a 50-fold increase in device area. Similarly, no area dependence was observed in the minority carrier response for $p$-type devices. Therefore peripheral inversion effects are not present for the In$_{0.53}$Ga$_{0.47}$As sample set under examination. The ac signal frequencies range from 100 Hz to 1 MHz in all cases. Identical frequencies were measured on all areas, so the colours in each plot correlate to the same frequency in the case of this figure.

## 5.6. Temperature Response

In order to investigate further the origin of the minority carrier response, the CV and GV as a function of variable temperature were analyzed. This is following the approach used by Nicollian and Brews,[15] who based their work on the theory derived by Hofstein and Warfield.[17] The measurements were carried out in a microchamber probe station (Cascade, Summit 12971B), with the lowest temperature possible using this set-up being -50$^o$C. The 30 kHz CV and GV responses as a function of temperature (T) for the $n$-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As device are plotted in the right column of Figure 5.6. For the sake of comparison the left column of Figure 5.6 shows the results obtained by Nicollian and Brews for a SiO$_2$/$n$-Si device.[15] The CV for the $n$- In$_{0.53}$Ga$_{0.47}$As device in Figure 5.6 exhibits a similar behaviour to the multi-frequency plots in Fig. 5.2 (a). The capacitance goes through a small peak associated with a mid-gap interface state response ~ -0.6 V$_{gate}$ before rising to a plateau over the remaining bias range. The conductance mirrors this behaviour, exhibiting a peak due to interface states in the gate bias range ~ -0.4 V to -0.8 V before rising and plateauing over the gate bias range -1.5 V to -4 V. Furthermore, this is the same characteristic behavior as the CV and GV temperature dependence for the SiO$_2$/$n$-Si MOSCAP in inversion in Figure 5.6 (a).[15] The conductance response of the minority carriers in inversion for an MOS capacitor exhibits a specific temperature dependent behaviour, where at a fixed ac signal frequency, the conductance increases to a maximum value and then subsequently decreases with any further increase in temperature.[15] This characteristic is observed for the $n$-In$_{0.53}$Ga$_{0.47}$As device in Figure 5.6, over the bias range -1.5 V to -4 V V$_{gate}$, where open symbols are used to highlight the decrease in conductance for temperatures in excess of 20$^o$C. Also, the peak conductance occurs at the temperature where the capacitance in inversion is mid-way between the maximum and minimum recorded values. This is analogous to the multi-frequency behavior, described earlier, see Figure 5.2, where the conductance in inversion peaks at the transition frequency, that also being the frequency of the mid-capacitance.
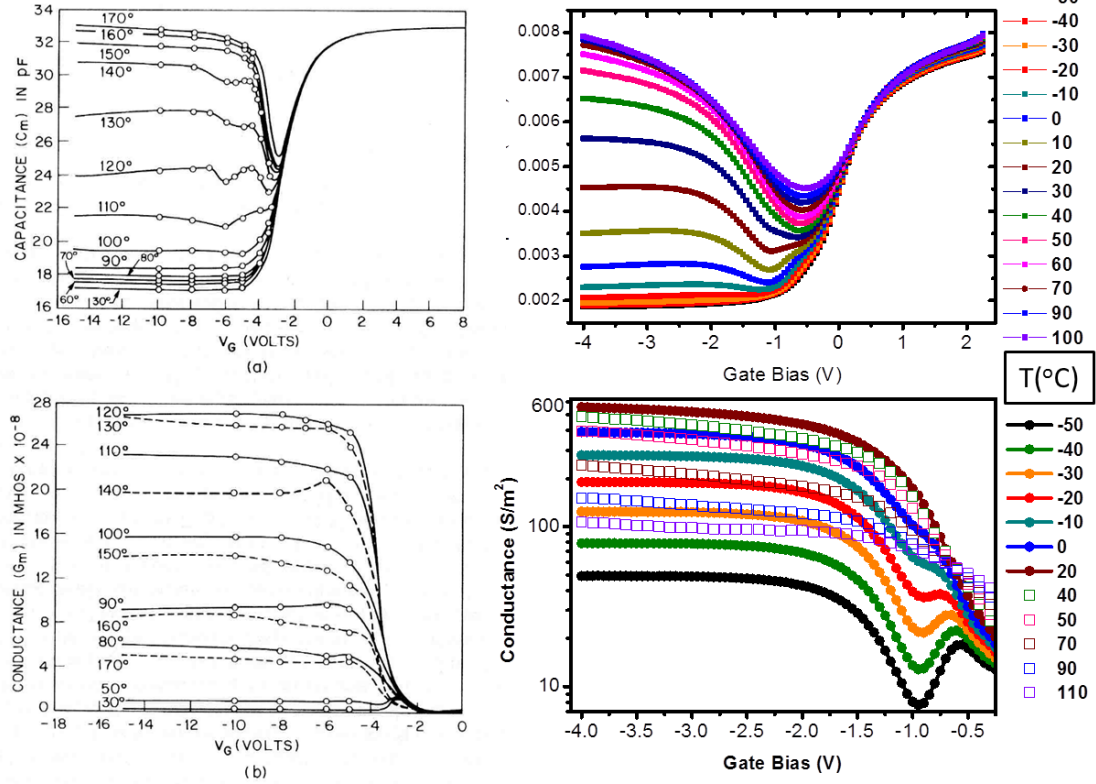
Figure 5.6 Left Column: 6 kHz CV and GV versus temperature (30$^{o}$C to 170$^{o}$C), for a SiO$_2$/$n$-Si device as published by Nicollian and Brews. [15] The peak conductance occurs around 120$^{o}$C, decreasing with further temperature increases. 120$^{o}$C is also the temperature where the mid-capacitance in inversion is recorded. Right Column: 30 kHz CV and GV responses as a function of temperature (T) (-50$^{o}$C to 110$^{o}$C), for an $n$-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As device (optimum 10% (NH$_4$)$_2$S treatment, ~ 3 minute ALD transfer). Open symbols are used in the GV to highlight the decrease in G$_m$ for T > 20$^{o}$C.[21]

The 10 kHz CV and GV responses as a function of temperature (T) for the optimized 10% (NH$_4$)$_2$S passivated (~ 3 minute ALD transfer) $p$-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As device, are plotted in Figure 5.7. The same characteristic behavior is seen in inversion as for the $n$-type samples, and in this case the conductance peaks at a temperature of ~90$^{o}$C.
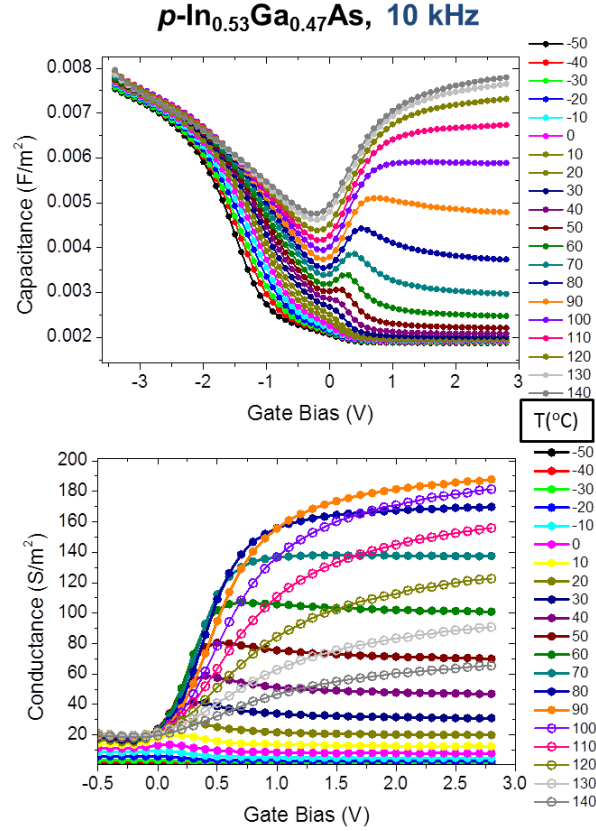
Figure 5.7 10 kHz CV and GV responses as a function of temperature (T) (-50$^{\circ}$C to 110$^{\circ}$C), for a *p*-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As device (optimum 10% (NH$_4$)$_2$S treatment, ~ 3 minute ALD transfer). Open symbols are used in the GV to highlight the decrease in G$_m$ for T > 90$^{\circ}$C.

## 5.7.    Arrhenius Extraction of Activation Energies

It is possible to differentiate between the mechanisms responsible for the minority carrier response over a given temperature range. The activation energy ($E_A$) of the minority carrier response will be approximately half the bandgap energy ($E_G$) for a generation recombination process through mid-gap traps, and will be equal to $E_G$ for a diffusion controlled regime of minority carriers from the substrate. It is expected that generation-recombination through mid-gap traps in the depletion region will dominate at lower temperature, while diffusion from the bulk will become dominant at higher temperature. By calculating the parallel inversion conductance ($G_I$),

extracted from the measured conductance ($G_m$) and capacitance ($C_m$) in inversion using Equation [5.1], and plotting versus 1/T, the activation energies can be obtained from the resulting Arrhenius plot.[15, 16, 21, 22, 28] $G_m$ and $C_m$ in this case are taken at a $V_{gate}$ of -4V for the *n*-type device and at a $V_{gate}$ of 2.8V for the *p*-type device. In the equation below, $\omega$ is the angular frequency, $\tau_o = C_{ox}/G_m$ and $\tau_m = C_m/G_m$, $C_{ox}$ being the oxide capacitance.[15]

$$G_I = \frac{\omega^2 C_{ox} \tau_o (1 + \omega^2 \tau_m^2)}{\omega^2 \tau_o^2 + [\omega^2 \tau_m (\tau_o - \tau_m) - 1]^2} \quad \text{EQ [5.1]}$$

The Arrhenius plots for the *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ devices examined in this work are shown in Figures 5.9 (a) and (b) respectively.[21] Again, for the sake of comparison, the results from Nicollian and Brews are plotted in Figure 5.8 for a $SiO_2$/*n*-Si device. In Figure 5.9 (a) and (b) there is a clear change in the slope of $G_I$ versus 1/T for both the *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ devices. For the *n*-$In_{0.53}Ga_{0.47}As$ device, at lower temperature an $E_A$ of approximately 0.31eV is obtained from curve *(a)*, which is close to half the bandgap (~0.37eV) for $In_{0.53}Ga_{0.47}As$, indicating a generation-recombination regime. At higher temperatures an $E_A$ lower than $E_G$ is obtained from curve *(b)*. However this discrepancy can be removed following a correction procedure.[15, 16] This subtracts the contribution of depletion layer generation and recombination at higher temperature, and is performed by subtracting the extrapolated values of curve *(a)* from curve *(b)*, yielding curve *(c)* in Figure 5.9(a). This now yields an $E_A$ of 0.67eV, which is close to the $E_G$ of $In_{0.53}Ga_{0.47}As$ (~ 0.74eV), indicating a transition to a diffusion controlled minority carrier response. A discrepancy of ~ 0.07eV is not unreasonable given that a similar deviation of $E_A$ from $E_G$ is observed for the $SiO_2$/*n*-Si MOS device.[15, 16] For the *p*-type device, at lower temperature curve *(d)* yields an $E_A$ of 0.37eV, approximately equal to $E_G/2$, indicating a generation-recombination regime. At higher temperature curve *(f)* is obtained following the correction procedure described earlier.
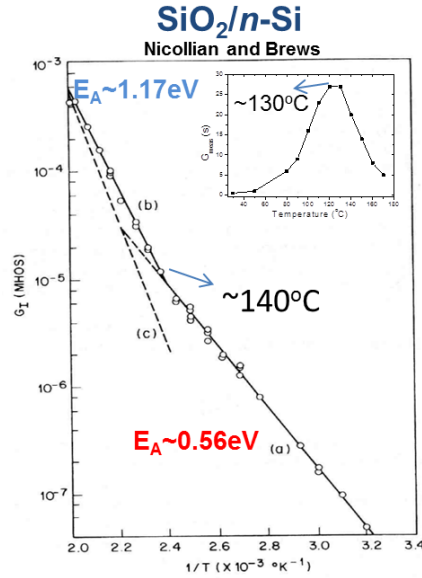
Figure 5.8 Arrhenius plots of the inversion parallel conductance ($G_I$), plotted versus 1/T for a $SiO_2$/*n*-Si device as published by Niccolian and Brews in MOS Physics and Technology.[15]
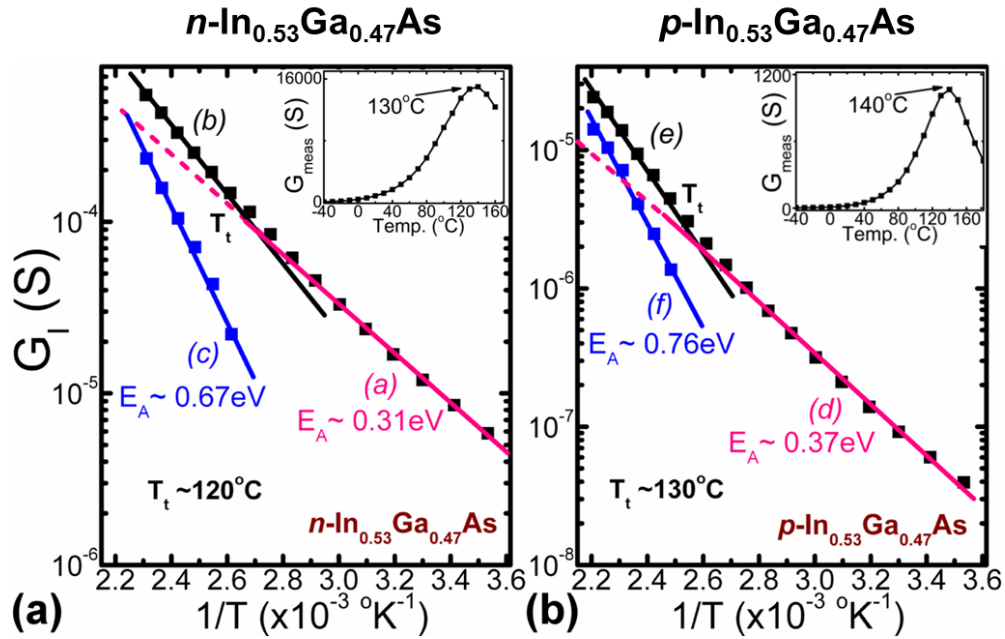


Figure 5.9 Arrhenius plots of the inversion parallel conductance ($G_I$), plotted versus 1/T for (a) *n*-type and (b) *p*-type Au/Ni/$Al_2O_3$/$In_{0.53}Ga_{0.47}$As devices. $T_t$ is the transition temperature. $G_I$ was extracted at 1 MHz for the *n*-type and 60 kHz for the *p*-type device respectively. The insets plot the measured conductance ($G_m$) in inversion versus T, showing that at a given frequency the temperature where $G_m$ peaks is approximately equal to $T_t$.[21]

This yields an $E_A$ of 0.76 eV, very close to $E_G$, indicating a transition to a diffusion regime. The temperature where the regime changes from generation-recombination to diffusion is labelled as the transition temperature ($T_t$). In the analysis performed for a SiO$_2$/Si device this $T_t$ corresponds closely with the temperature where the maximum $G_m$ occurs,[15] which is also observed for these In$_{0.53}$Ga$_{0.47}$As devices, see Fig 5.9 insets.

## 5.8. Variable Doping Experiment: Motivation

For an MOS device in strong inversion the depletion layer width reaches a maximum value.[30] The equation governing the maximum depletion width is given in Equation [5.2] below where: $\varepsilon_0$ is the permittivity of free space; $\varepsilon_s$ is the semiconductor permittivity; $k$ is Boltzmann's constant; $n_i$ is the intrinsic semiconductor carrier concentration; $N_D$ is the semiconductor doping concentration.[31]

$$x_{d\_max} = \sqrt{\frac{4\varepsilon_0\varepsilon_S kT \ln\left(N_D/n_i\right)}{q^2 N_D}} \qquad \text{[EQ. 5.2]}$$

From this equation, as the semiconductor doping level is increased the maximum depletion width is reduced, which in turn is reflected in an increase in the minimum depletion capacitance ($C_D$) of the semiconductor as given by Equation [5.3]:

$$C_D = \frac{\varepsilon_0\varepsilon_S}{x_{d\_max}} \qquad \text{[EQ. 5.3]}$$

The theoretical minimum capacitance of a gate stack is then given by the series combination of the semiconductor capacitance and the oxide capacitance:

$$C_{min-theor} = \frac{C_{ox}C_D}{C_{ox}+C_D} \qquad \text{[EQ. 5.4]}$$

It is thus expected that for an inverted surface, the minumum measured gate stack capacitance will increase as a function of doping concentration. This approach was used by Callegari and co-workers in 1989 to investigate improvements in the CV characteristics of plasma deposited Ga oxide films on GaAs substrates.[32] As discussed

earlier GaAs substrates present serious problems due to their typically high defect densities. The authors used two different GaAs doping concentrations, $\sim 2 \times 10^{17} cm^{-3}$ and $\sim 2 \times 10^{18} cm^{-3}$, and compared the high-frequency CV repsonses. As shown in Figure 5.10 below this demonstrated good agreement between the measured and theoretical minumum capacitances over this doping range, indicating free Fermi level movement over the bias range examined.
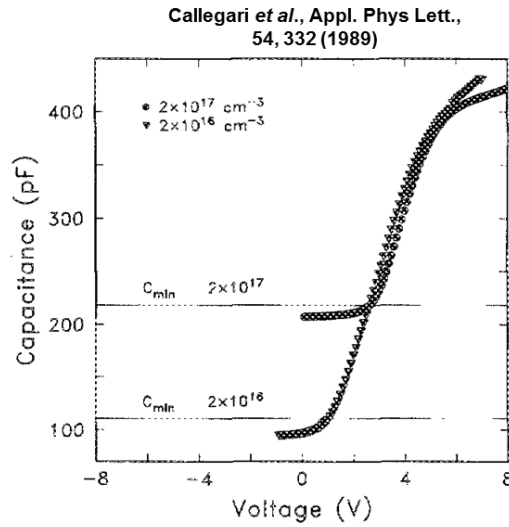


Figure 5.10 CV curves @1 MHz of MOS devices with plasma deposited Ga oxide films on GaAs substrates with differing doping concentrations, $2 \times 10^{16} cm^{-3}$ and $2 \times 10^{17} cm^{-3}$, as published by Callegari et al. [32]

We adapted this approach to investigate $n$ and $p$-$In_{0.53}Ga_{0.47}As$ MOS devices where the range in the semiconductor doping concentration was extended even further to over two orders of magnitude, from $\sim 1 \times 10^{16} cm^{-3}$ to $2 \times 10^{18} cm^{-3}$. This provides another manner in which to investigate inversion behavior in $In_{0.53}Ga_{0.47}As$ MOS devices. Comparing the measured minimum capacitance with the theoretical capacitance calculated assuming the surface is inverted, it is possible to examine if the device minimum capacitance scales correctly with semiconductor doping.

## 5.9.    $C_{min}$ as a function of $In_{0.53}Ga_{0.47}As$ doping concentration
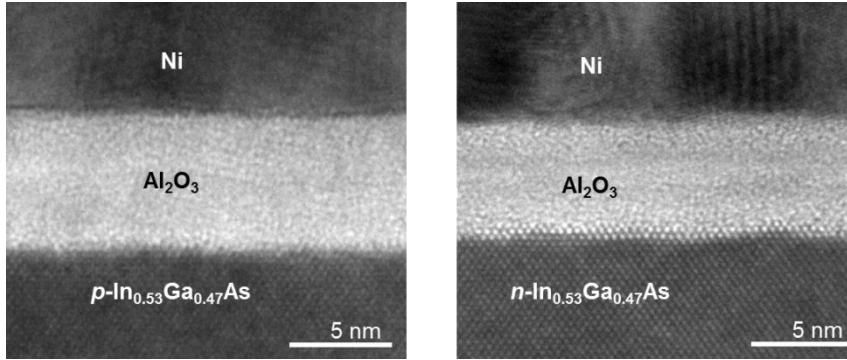


Figure 5.11. Cross-sectional TEM micrographs of Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As/InP, devices. The TEM indicates that the Al$_2$O$_3$ layer thicknesses are approximately 7nm and 5nm in the case of the *p* and *n*-type samples respectively. The TEM imaging and sample preparation was performed by Dr. Patrick Carolan of Tyndall National Institute.

The TEM images in Figure 5.11 above show the gate stack for one each of the *p*-type and *n*-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As/InP doping series samples (with doping concentrations of $2.7x10^{17}$ cm$^{-3}$ and $6.0x10^{17}$ cm$^{-3}$ respectively). Thus the Al$_2$O$_3$ layer thicknesses are ~7nm in the case of the *p*-type samples and closer to ~ 5nm in the case of the *n*-type samples.

Figure 5.12 exhibits the 1MHz CV responses for the *p*-type In$_{0.53}$Ga$_{0.47}$As MOS devices with dopant (Zn) concentrations of (cm$^{-3}$): $1.4x10^{16}$, $3.3x10^{16}$, $1.8x10^{17}$, $2.7x10^{17}$, and $2.0x10^{18}$. [33] The 1 MHz CV curves were chosen in order to minimize any contribution of interface states to the measured capacitance in inversion. The open symbols represent the theoretical minimum capacitance, $C_{min-theor}$, for each doping concentration and calculated using a $C_{ox}$ value in this case of 0.0075 F/m$^2$, taken from the measured capacitance at low frequency (20Hz). It is clear from the figure that there is excellent agreement between the measured and theoretical capacitance values. This is particularly notable considering that the change in doping concentration is over two orders of magnitude. When plotting the measured (@ 1.75 V$_{gate}$) capacitance versus the theoretical value, Figure 5.13 demonstrates that there is close to a linear relationship.
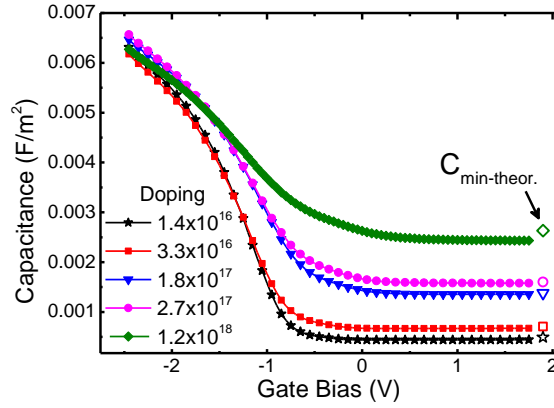
Figure 5.12 1MHz CV responses for the Au/Ni/ 7nm $Al_2O_3$/$p$-$In_{0.53}Ga_{0.47}As$ MOS devices with dopant (Zn) concentrations of ($cm^{-3}$): $1.4x10^{16}$, $3.3x10^{16}$, $1.8x10^{17}$, $2.7x10^{17}$, and $1.2x10^{18}$. The theoretical values were estimated using a $C_{ox}$ value of 0.0075 $F/m^2$.
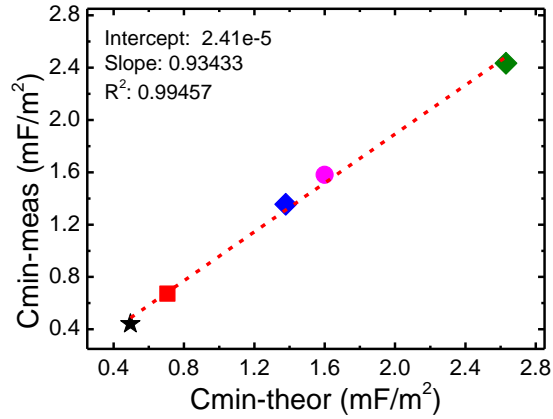


Figure 5.13 Plot of measured versus theoretical minimum capacitance for the different $p$-type doping concentrations. The measured values are those at a gate bias of 1.75 V in Figure 5.12. The symbols corresponding to each doping concentration are the same as those in Figure 5.12.

Figure 5.14 exhibits the 1MHz CV responses for the $n$-type $In_{0.53}Ga_{0.47}As$ MOS devices with the following epitaxial layer dopant (Si) concentrations ($cm^{-3}$): $7.8x10^{15}$, $3.0x10^{16}$, $2.0x10^{17}$, $6.0x10^{17}$, and $2.0x10^{18}$. As in the case of the $p$-type samples, there is excellent agreement between the measured and theoretical capacitance values. Again, open symbols represent the theoretical minimum capacitance, $C_{min-theor}$, for

each doping concentration and calculated using a $C_{ox}$ value in this case of 0.0093 $F/m^2$, taken from the measured capacitance at low frequency (20Hz).
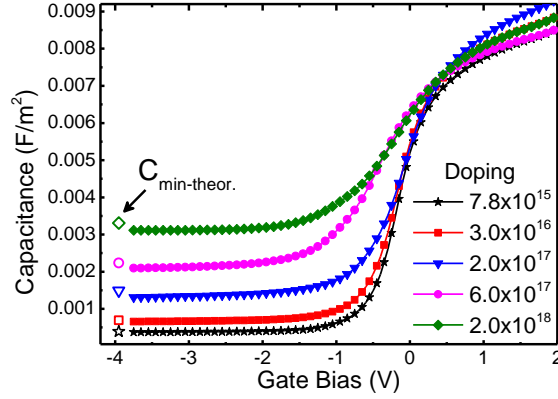


Figure 5.14 1MHz CV responses for the Au/Ni/5 nm $Al_2O_3$/$n$-$In_{0.53}Ga_{0.47}As$ MOS devices with dopant (Si) concentrations($cm^{-3}$): $7.8x10^{15}$, $3.0x10^{16}$, $2.0x10^{17}$, $6.0x10^{17}$, and $2.0x10^{18}$. The theoretical values were estimated using a $C_{ox}$ value of 0.0093 $F/m^2$.
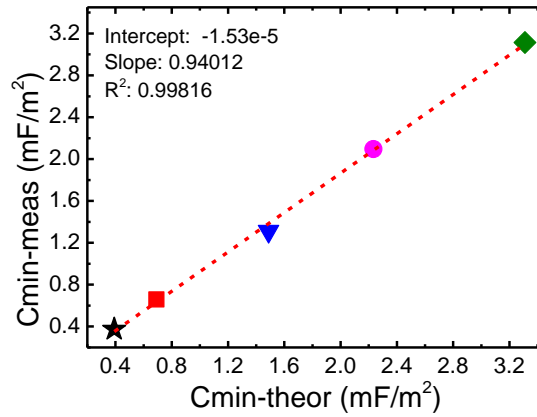


Figure 5.15 Plot of measured versus theoretical minimum capacitance for the different $n$-type doping concentrations. The measured values are those at a gate bias of -3.75 V in Figure 5.14. The symbols corresponding to each doping concentration are the same as those in Figure 5.14.

## 5.10.  Variation in $\omega_m$ with In$_{0.53}$Ga$_{0.47}$As doping concentration

Multi-frequency CV and GV responses (20 Hz to 1 MHz) were also recorded on all samples. The full responses are plotted in Appendix 3, section 10.1. In summary, these exhibited the characteristic signatures of inversion behavior as discussed in the previous chapter. One observation of note over both *n* and *p*-type is that the transition frequency at which G/$\omega$ peaks in inversion increases as the semiconductor doping concentration in increased. The transition frequency is inversely proportional to the minority carrier generation lifetime, which therefore reduces with doping concentration.

Figure 5.16 shows the change in transition frequency with doping for (a) *p*-type and (b) *n*-type devices. It is clear that the transition frequency increases significantly with doping in both cases. The results also indicate that at any given doping concentration the transition frequency for the *n*-type samples is generally one order of magnitude higher than the corresponding *p*-type samples. At the time of
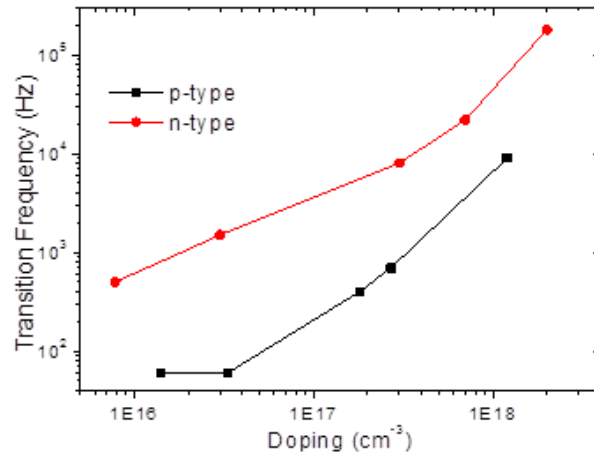


Figure 5.16 Increase in transition frequency as a function of In$_{0.53}$Ga$_{0.47}$As doping concentration for (a) p-type, and (b) n-type MOS devices. This corresponds to a decrease in the minority carrier generation lifetime with increasing doping.

writing simulations to fit minority carrier generation lifetimes to these transition frequencies are being undertaken. To further illustrate this behaviour, 1 kHz CV curves on the *p*-type doping samples are plotted in Figure 5.17. It is clear from the increasing capacitance observed in the inversion region that at a given frequency it is easier to invert the surface for higher epitaxial doping levels; in effect there is a greater supply of minority carriers. This may be expected as increasing the doping concentration introduces more impurities in the $In_{0.53}Ga_{0.47}As$ epitaxial layer, thus generating more bulk defects for supply of minority carriers. It is noted that the same behavior seen in Figure 5.17 is observed over *n*-type for a given frequency (not shown).
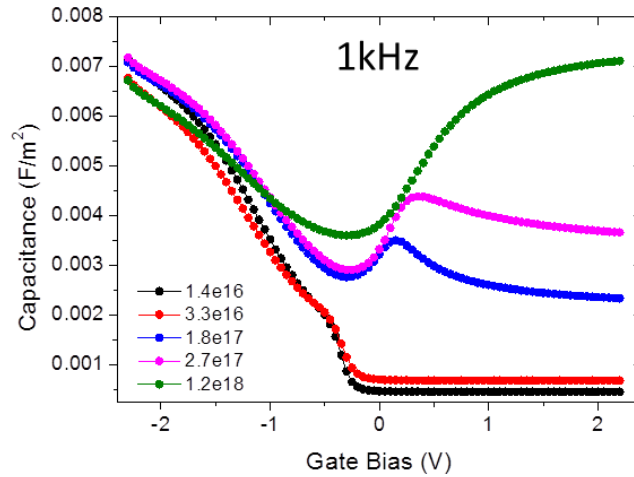


Figure 5.17 Comparison of 1kHz CV profiles as a function of *p*- $In_{0.53}Ga_{0.47}As$ doping concentration.

## 5.11. Conclusions

In summary, a clear minority carrier response was observed for both *n*-type and *p*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS devices following an optimized $(NH_4)_2S$ treatment with minimal ambient exposure pre-ALD. An extraction of activation energies for the minority carrier response indicated a transition from a generation-recombination regime to a diffusion controlled response, for both *n*-type and *p*-type

devices. These observations are consistent with a $D_{it}$ which is sufficiently reduced for these *n*-type and *p*-type devices to permit the Fermi level to be swept across the $In_{0.53}Ga_{0.47}As$ band gap. Also, for MOS capacitors fabricated on *n* and *p*-$In_{0.53}Ga_{0.47}As$ with semiconductor doping concentrations ranging over two orders of magnitude from ~$1x10^{16}cm^{-3}$ to ~$2x10^{18}cm^{-3}$ it was clearly observed that the measured $C_{min}$ increases as doping concentration increases, and that the measured $C_{min}$ is in very good agreement with the theoretical value, providing further confirmation for an inverted $In_{0.53}Ga_{0.47}As$ surface.

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# Chapter 6

## 6. Experimental method for extraction of $C_{ox}$ for $In_{0.53}Ga_{0.47}As$ MOS capacitors, and the effect of FGA on minority carrier response

### 6.1. Introduction

In Chapter 5, results were demonstrated consistent with a reduction in $D_{it}$ sufficient to allow inversion of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ surface and the observation of a minority carrier response over both $n$ and $p$-$In_{0.53}Ga_{0.47}As$.[1] To extend this analysis, this chapter describes a methodology where the capacitance and conductance in strong inversion can be used to estimate $C_{ox}$. Given $C_{ox}$ is an important parameter, eg. in common $D_{it}$ extraction methods, a reliable method to provide an accurate $C_{ox}$ is highly desirable, particularly for high-$k$/III-V systems. Experimental observations indicate there is a unique relationship between the capacitance and conductance in strong inversion, facilitating an experimental avenue to determine $C_{ox}$. This is also analysed using physics based simulations. By utilizing an equivalent circuit model a mathematical derivation to extract an expression for this relationship is performed.

Also, MOS capacitors were fabricated on $n$ and $p$-$In_{0.53}Ga_{0.47}As$ with varying $Al_2O_3$ thickness, 4nm, 8nm, and 12nm. It is beneficial both to assess if the minority carrier response is altered by annealing and whether it can be observed for a reduced $E_{ot}$. In addition the effect of varying $t_{ox}$, and of post-metallization forming gas annealing, on the minority carrier generation lifetime is examined.

## 6.2. Experimental Details

### 6.2.1. Samples for determination of $C_{ox}$

The results pertaining to the determination of $C_{ox}$ are based on the samples as described in section 5.2.1, the details are repeated here for completeness.

The $In_{0.53}Ga_{0.47}As$ epitaxial layers used in this work were either (1) ~ 2μm $n$-type $In_{0.53}Ga_{0.47}As$ (S at ~ $4x10^{17}cm^{-3}$) grown by metalorganic-vapour-phase-epitaxy (MOVPE) on $n$-doped (S at ~ $2x10^{18}$ $cm^{-3}$) InP(100) wafers, or (2) ~ 2μm $p$-type $In_{0.53}Ga_{0.47}As$ (Zn at ~ $4x10^{17}cm^{-3}$) grown by MOVPE on $p$-doped (Zn at ~ $2x10^{18}$ $cm^{-3}$) InP(100) wafers. The actual doping concentrations of the epitaxial layers were measured on sacrificial test pieces by the supplier IQE, and the specifications varied slightly from the nominal and were found to be $4.4x10^{17}cm^{-3}$ for the $n$-$In_{0.53}Ga_{0.47}As$ and $3.3x10^{17}cm^{-3}$ for the $p$-$In_{0.53}Ga_{0.47}As$. All $In_{0.53}Ga_{0.47}As$ surfaces were initially rinsed for 1 minute each in acetone, methanol, and isopropanol. $(NH_4)_2S$ concentrations of 10% in deionised $H_2O$ were used (20 minutes, ~ 295K). The $Al_2O_3$ layers were grown by atomic layer deposition (ALD) at $300^oC$ (Cambridge NanoTech, Fiji F200LLC), using alternating pulses of TMA ($Al(CH_3)_3$) and $H_2O$. TEM confirmed the thickness was close to the nominal 8nm. The time taken to rinse the samples in DI water, blow dry with nitrogen and transfer to the ALD chamber was 3 minutes. Finally, gate contacts ~ 160 nm thick were formed by e-beam evaporation of Ni (70nm), and Au (90nm), using a lift-off process. In the case where forming gas annealing was performed it was carried out post-metallization in a tube furnace at $275^oC$ for 30 minutes in a 5%-$H_2$:95%-$N_2$ ambient. Electrical measurements were recorded using an Agilent E4980A, and were performed on-wafer in a microchamber probe station (Cascade, Summit 12971B) in a dry air, dark environment (dew point $\leq$203K). It is noted that lower gate leakage current densities were recorded (not shown) on samples which received the optimum passivation compared to samples which did not receive the passivation step but were otherwise identical in structure.

### 6.2.2. Samples with variable $Al_2O_3$ thickness

The samples for the variable thickness experiment underwent nominally identical processing to those above, using the same IQE $In_{0.53}Ga_{0.47}As$ wafers. However in this case the ALD thickness was varied, with 4nm, 8nm, and 12nm $Al_2O_3$ layers. These were separate 8nm growth runs to those mentioned to date.

## 6.3. Experimental Observation: $G/\omega$ and $-\omega dC/d\omega$ relationship in inversion

As described extensively in the previous chapter, results consistent with inversion behaviour were observed for $n$ and $p$-$In_{0.53}Ga_{0.47}As$ MOS devices with an $Al_2O_3$ dielectric, and having been subjected to an optimized $(NH_4)_2S$ passivation procedure.[1, 2, 3] In the course of performing the CV and GV measurements plotted in Figure 5.2, it became noticeable that the maximum rate of change in capacitance in strong inversion appeared to be around the frequency where $G/\omega$ peaks, ie. around the transition frequency, $\omega_m$. Therefore, on observing this, the frequencies for the measurements were chosen with the spacing of the frequency steps being altered and reduced around $\omega_m$. It was then decided to compare the derivative of the measured capacitance with respect to frequency in inversion, and compare this to the corresponding $G/\omega$ values, in order to determine if any relationship existed with regard to this behaviour.

For this analysis the measured capacitance ($C_m$) and frequency scaled conductance ($G/\omega$) in strong inversion was used, utilizing the data shown in Figure 5.2, at a gate bias of -4V for the $n$-type device and 2.8V for the $p$-type device. Figure 6.1 (a) and (b) present a comparison of $G/\omega$ versus $\omega$, and the derivative of the natural log of $C_m$ with respect to $\omega$, ie. ($-dC/dLn(\omega)$), for $n$-type and $p$-type $In_{0.53}Ga_{0.47}As$ devices respectively. For ease of reference, the term "$-dC/dLn(\omega)$" is mathematically

equivalent to -ωdC/dω and will be referred to as such going forwards. It is immediately apparent that the curves exhibit very similar profiles across the entire frequency range examined, while it is noticeable that the full-width-half-maximum (FWHM) of the G/ω plots is slightly wider in both cases than that of the −ωdC/dω plots. More significantly, the peak values of G/ω and -ωdC/dω are equal in magnitude. Additionally, the angular frequency at which these peak values coincide is the transition frequency, $\omega_m$, which as mentioned earlier is ~ 25 kHz for this $n$-type device and ~ 600 Hz for this $p$-type device.



Figure 6.1 $G_m/\omega$ and -ωdC/dω plotted as a function of the angular frequency (ω) in strong inversion for (a) Au/Ni/8nm $Al_2O_3/n$-$In_{0.53}Ga_{0.47}As$ device, and (b) Au/Ni/8nm $Al_2O_3/p$-$In_{0.53}Ga_{0.47}As$. The values of $C_m$ and G/ω were taken at a gate bias of -4V for $n$-$In_{0.53}Ga_{0.47}As$ devices and at a gate bias of 2.8 V for $p$-$In_{0.53}Ga_{0.47}As$ devices , utilizing the multi-frequency data plotted in Figure 5.2.

## 6.4. Simulations: G/$\omega$ and $-\omega$dC/d$\omega$ relationship in inversion

The relationship observed experimentally between G/$\omega$ and $-\omega$dC/d$\omega$ was next investigated using physics based simulations.[4,5] The simulation parameters reflected the $Al_2O_3$ thickness, and the $In_{0.53}Ga_{0.47}As$ doping concentrations of the experimental samples. In addition, the simulations assumed zero contribution from interface states, fixed charges, or border traps.

Figures 6.2 (a) and (b) show a comparison of the simulated G/$\omega$ and $-\omega$dC/d$\omega$ in strong inversion versus $\omega$, for *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ respectively. It is striking that the plots arising from the simulation data exhibit near identical behavior to that observed in Figure 6.1 for the experimental MOS devices. Again both G/$\omega$ and $-\omega$dC/d$\omega$ share an identical peak magnitude, occurring at $\omega_m$, and the FWHM of the G/$\omega$ curves are slightly wider. It is noted that the minority carrier generation lifetimes used in the simulation were adjusted to mirror the transition frequencies of the experimental devices. Changing the minority carrier generation lifetime in the simulation will shift the $\omega_m$ peak, but not alter its magnitude.
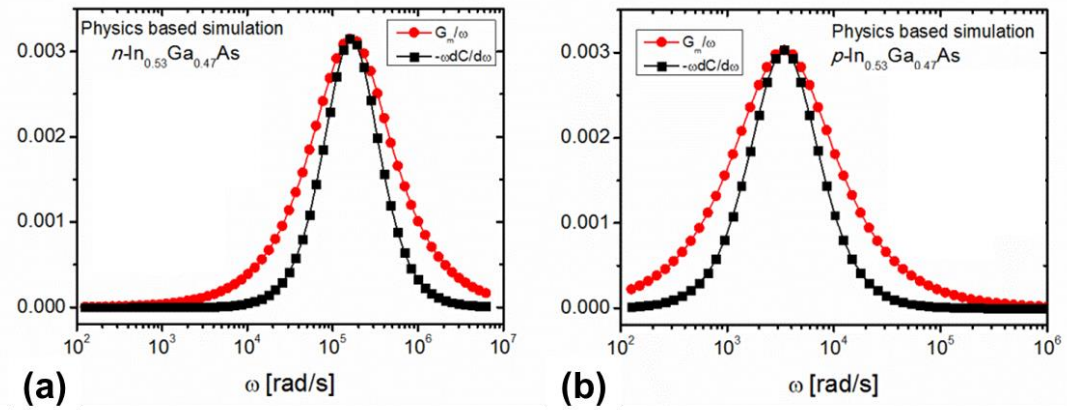


Figure 6.2 Simulated $G_m/\omega$ and $-\omega$dC/d$\omega$ plotted as a function of the angular frequency ($\omega$), for the case of strong inversion. The minority carrier generation lifetime ($\tau_g$) used for the simulations was chosen to mirror the transition frequencies of the experimental devices. The simulations were performed by Dr. Rafael Rios of Intel using a Synopsys Sentaurus Device Simulator.

To further illustrate the similarity in the experimental and simulated responses, Figure 6.3 overlays the G/ω versus ω plots from Figures 6.1 and 6.2. Over the entire frequency range (20 Hz to 1 MHz) examined there is almost no deviation in the profiles of the curves. One important point to highlight in this regard is that the simulations assumed zero interface state and border trap response. The fact that the plots from the experimental and simulated data are so similar indicates that neither interface states nor border traps are making a significant contribution to the behavior of the experimental MOS devices in strong inversion. This is significant also in that it is further proof that the minority carrier response observed is dominated in this case by generation and recombination through traps in the depletion region with energies near mid-gap, and confirmation that interface states do not play a role, as stated by Nicollian and Brews.[2]
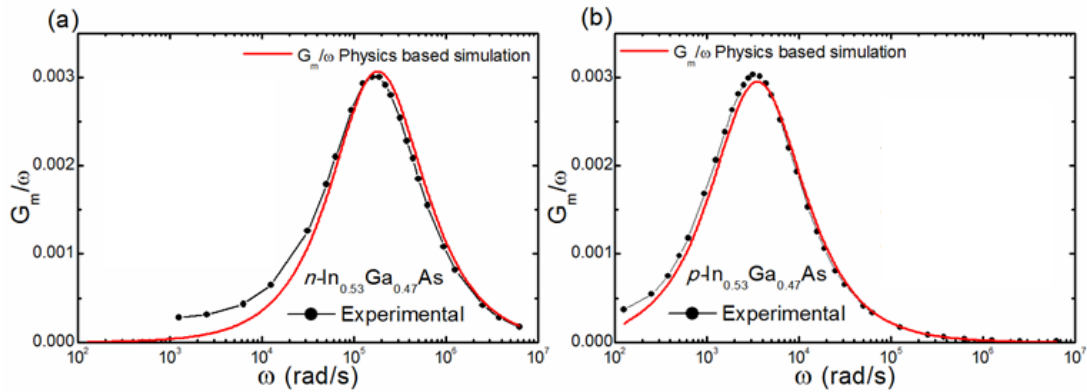


Figure 6.3 Measured (black circles) and simulated $G_m/\omega$ (solid line) plotted as a function of the angular frequency ($\omega$), for (a) $n$-In$_{0.53}$Ga$_{0.47}$As and (b) $p$-In$_{0.53}$Ga$_{0.47}$As. This overlays the experimental and simulated G/ω versus ω data from Figures 6.1 and 6.2. It is evident that there is near identical behavior in both cases over the frequency range examined, ~ 20 Hz to 1 MHz. The simulations assumed zero contribution of interface states or border traps. [4, 5] This is significant as the similarity in behavior confirms that the minority carrier response observed in the experimental samples is dominated in this case by generation and recombination through bulk traps, and confirmation that interface states do not play a role. Very good agreement is also obtained for the simulated and measured values of -ωdC/dω (not shown).

### 6.5.    Experimental Observation: G/ω and dC/dT relationship in inversion

In analyzing the inversion response of the $In_{0.53}Ga_{0.47}As$ devices in Chapter 4, in addition to multi-frequency CV and GV measurements at room temperature, electrical characteristics were examined as a function of varying temperature while keeping the frequency fixed (see Figures 5.6 and 5.7). It is possible therefore to utilize $C_m$ and G/ω measured versus temperature in strong inversion to plot the rate of change of capacitance with temperature (dC/dT) versus the change in G/ω with temperature (T).  Figure 6.4 plots dC/dT and G/ω versus T, for the *n*-type device (30 kHz) and the *p*-type device (10 kHz). It is observed in both Figures 6.4 (a) and (b) that the peak value of G/ω versus temperature is the same as that of G/ω versus frequency (Figure 6.1). It is also immediately apparent that the maximum rate of change of capacitance occurs at the same temperature as the peak G/ω. Therefore the capacitance and conductance behavior at fixed frequency with varying temperature is analogous to that observed at fixed temperature with varying frequency (Figure 6.1). However, clearly in this case dC/dT and G/ω do not share the same peak magnitude. The ratio of the peak of G/ω to dC/dT is ~28 for both the *n*-type and *p*-type devices. Further analysis of this relationship has not been attempted at the time of writing, these results being included for illustrative purposes.
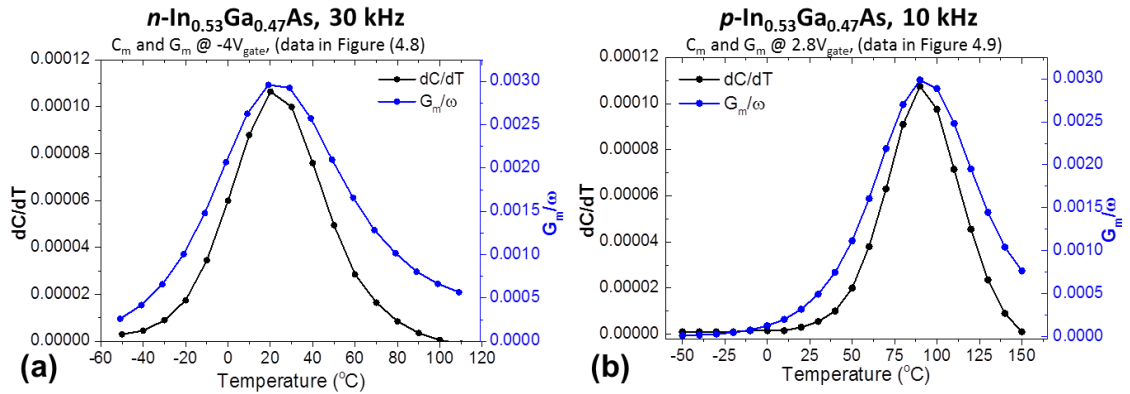


Figure 6.4 $G_m$/ω and dC/dT plotted versus measurement temperature in strong inversion for (a) Au/Ni/8nm $Al_2O_3$/*n*-$In_{0.53}Ga_{0.47}As$/*n*-InP devices, and (b) Au/Ni/8nm $Al_2O_3$/*p*-$In_{0.53}Ga_{0.47}As$/*p*-InP . The values of $C_m$ and G/ω were taken at a gate bias of -4V for *n*-$In_{0.53}Ga_{0.47}As$ devices, and at a gate bias of 2.8 V for *p*-$In_{0.53}Ga_{0.47}As$ devices, utilizing the data plotted in Figures 5.6 and 5.7.

### 6.6. Mathematical Derivation of G/ω and −ωdC/dω

The experimental and simulated results indicating the equality in peak magnitude and frequency for G/ω and −ωdC/dω suggests that this may be a fundamental relationship which is generally true for all MOS systems in inversion. This raised the possibility that one could utilize the equivalent circuit model of an MOS device in inversion to mathematically derive an expression for this relationship. The mathematical derivation was performed by Liam Floyd and Scott Monaghan of Tyndall National Institute and at the time of writing of this thesis a manuscript based on this is in press.[5] The main features of the mathematical analysis are summarized in this section.

The equivalent circuit in Figure 6.5 was suggested by Nicollian and Brews to represent an MOS system in strong inversion. The function $G_{gr}(\omega)$ is used to represent a frequency dependent conductance associated with the supply of minority carriers to the inversion layer via generation and recombination. Using this circuit model the capacitance and frequency scaled conductance are represented mathematically by the expressions in Equation [6.1] and [6.2] respectively. Therefore manipulation of these equations can be used to attempt to derive an expression for G/ω and −ωdC/dω.
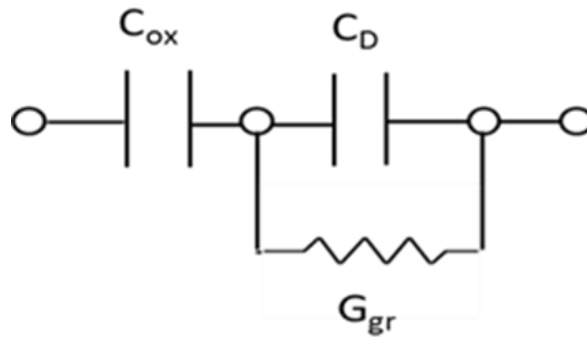


Figure 6.5 Schematic of equivalent circuit model for a MOS capacitor in strong inversion as proposed by Niccollian and Brews.[2] $G_{gr}$ models the conductance related to the supply of minority carriers while $C_D$ represents the maximum depletion capacitance.

$$C = C_{ox}\left[1 - \frac{\omega^2 C_{ox}(C_{ox} + C_D)}{(G_{gr}(\omega))^2 + \omega^2(C_{ox} + C_D)^2}\right] \quad \text{EQ. [6.1]}$$

$$G/\omega = G_{gr}(\omega)\frac{\omega C_{ox}^2}{(G_{gr}(\omega))^2 + \omega^2(C_{ox} + C_D)^2} \quad \text{EQ. [6.2]}$$

These equations were used to generate curves for C and G/ω in order to compare them to those obtained using physics based simulations. The results (not shown) were in excellent agreement across the frequency range, thus confirming that this circuit model gives an accurate representation of the MOS system in strong inversion.

It is shown that regardless of the dependence of $G_{gr}(\omega)$,[5] G/ω will peak at $\omega_m$, with this maximum magnitude given by:

$$[G/\omega]_{max} = \frac{C_{ox}^2}{2(C_{ox} + C_D)} \quad \text{EQ. [6.3]}$$

It is also shown that provided the derivatives of $G_{gr}(\omega)$ are zero at $\omega_m$,[5] then $-\omega dC/d\omega$ will also exhibit a maximum at $\omega_m$, the maximum magnitude given by:

$$[-\omega dC/d\omega]_{max} = \frac{C_{ox}^2}{2(C_{ox} + C_D)} \quad \text{EQ. [6.4]}$$

Therefore, the mathematical analysis provides equivalent formulae for the peak magnitude of G/ω and $-\omega dC/d\omega$ in inversion (given some assumptions regarding $G_{gr}(\omega)$ in Appendix 3). Significantly, it has now been demonstrated that the experimental data, physics based simulations, and mathematical derivation from the equivalent circuit, all exhibit agreement in the relationship that $-\omega dC/d\omega$ has the same peak magnitude as G/ω, occurring at $\omega_m$. Taken together, this provides very strong evidence that this relationship is true in general for MOS systems, and not

restricted to the samples under investigation in this work. Provided the semiconductor doping concentration is known, $C_D$ can be accurately calculated. Therefore, given the mathematical expressions for $(G/\omega)_{max}$ and $(-\omega dC/d\omega)_{max}$, a more accurate value for $C_{ox}$ can now be determined using the measured capacitance and conductance in strong inversion. Therefore given the simplicity of the relationship, this is a new and straightforward technique to calculate $C_{ox}$ for an MOS system. This analysis is predicted to be particularly beneficial in cases where it is difficult to extract $C_{ox}$ estimates from the capacitance in strong accumulation, such as in the event of gate leakage issues or high frequency dispersion of accumulation capacitance.

In the case of these samples, using the measured doping concentrations to calculate $C_D$, and using the measured $G/\omega$ or $-\omega dC/d\omega$ values in strong inversion, values of $C_{ox}$ of 0.0079 F/m$^2$ and 0.0078 F/m$^2$ are estimated for the *n*-type and *p*-type devices respectively. It is noted that this provides a good estimation of $C_{ox}$ if one looks at the multi-frequency CV plots in Figure 5.2 (a) and (b). It is also noted that 0.008 F/m$^2$ was used for $C_{ox}$ for the Arrhenius analysis of the minority carrier mechanisms in the previous chapter, and the values calculated here using the mathematical relationship provide confidence that this was a suitable $C_{ox}$ to use in that regard.

## 6.7.    G/ω and C$_{ox}$ relationship as a function of semiconductor doping

The doping series samples mentioned in Chapter 5 can also be utilized with regard to the relationship discussed here in Chapter 6 where in strong inversion the maximum value of $G/\omega$ at $\omega_m$ was found to be equal to $C_{ox}^2/2(C_{ox}+C_D)$. For a given $C_{ox}$, the semiconductor depletion capacitance will increase with the doping concentration. Therefore it would be expected using this relationship that the value of $G/\omega$ would decrease as the doping concentration increases. Figure 6.6 plots the expected theoretical values of $G/\omega$ versus doping, for various values of $C_{ox}$. The measured $G/\omega$ values are plotted as open symbols, with the dashed blue lines representing an

approximate fitting to those points in each case. It is seen that the experimental values follow the trend of the theoretical values quite closely. In Figure 6.14 (a) it is obvious that the curve calculated using $C_{ox}$ of 0.0075 F/m$^2$ is extremely
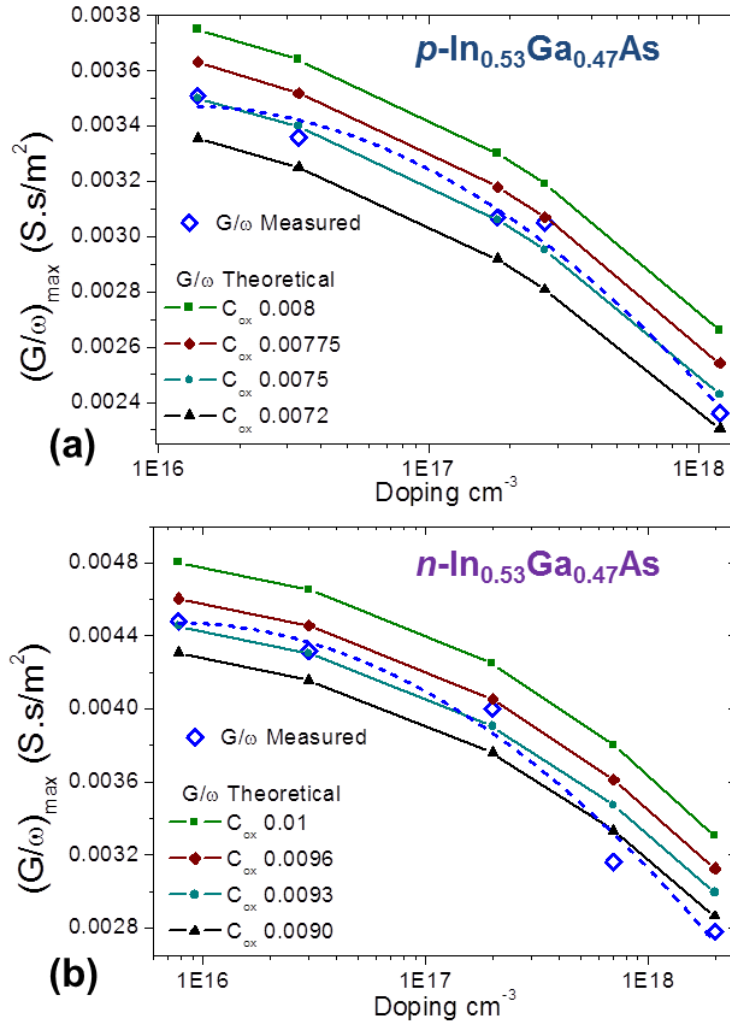


Figure 6.6 Peak G/ω in inversion as a function of doping concentration. A variety of $C_{ox}$ values were used to compute theoretical G/ω values according to Equation 6.3. It is noted that in the earlier analysis (Section 5.9) to compute the theoretical minimum capacitances, a $C_{ox}$ of 0.0075 F/m$^2$ and 0.0093 F/m$^2$ was used for $p$-type and $n$-type samples respectively. The corresponding curves for these $C_{ox}$ values compared to the experimental points in Figure 6.6 show these to be reasonable $C_{ox}$ estimates for that analysis. The frequency scaled conductance, G/ω, can also be expressed in units of F/m$^2$.

close to the fitted curve for the experimental $G/\omega$ data. In the case of the *n*-type devices the 0.0093 $F/m^2$ for $C_{ox}$ provides a good approximation over most of the doping range, although some deviation is observed in the experimental data for the two highest doping concentrations. These observations are important also in validating the calculations of the theoretical minimum capacitances described earlier in Section 5.9, where the $C_{ox}$ values used were 0.0075 $F/m^2$ and 0.093 $F/m^2$ for *p*-type and *n*-type samples respectively.

## 6.8.    Inversion Response with varying $Al_2O_3$ thickness

Devices were also fabricated with nominal $Al_2O_3$ thicknesses of 4nm, 8nm, and 12nm. (note that the 8nm samples in this set are from a different fabrication run and not the same 8nm samples discussed to date, as explained in the experimental section). These samples all received the optimized 10% $(NH_4)_2S$ passivation procedure. The actual thicknesses from TEM are 3.6nm, 8nm, and 12nm, and plotted in Figure 6.7.
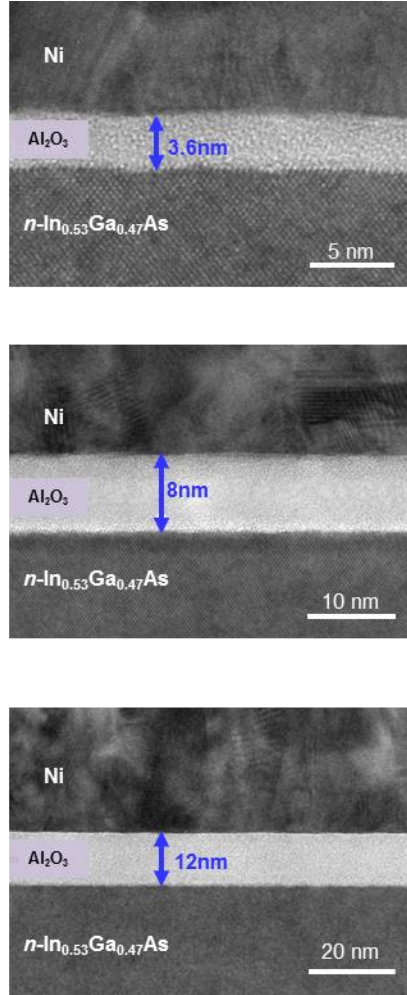
Figure 6.7. Cross-sectional TEM micrographs of Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As/InP, devices. The TEM indicates that the Al$_2$O$_3$ layer thicknesses are close to the nominal 4nm, 8nm, and 12 nm values. The TEM imaging and sample preparation was performed by Dr. Patrick Carolan of Tyndall National Institute.

In Figure 6.8 the multi-frequency CV are plotted pre- and post-FGA for *n*-In$_{0.53}$Ga$_{0.47}$As devices with varying Al$_2$O$_3$ thickness (the corresponding G/ω plots can be seen in Appendix 3, Section 10.2) These exhibit signature features consistent with those of an inversion response as discussed extensively in Chapter 5. In the few reports in the literature to date which indicate an inversion response for In$_{0.53}$Ga$_{0.47}$As MOS structures, only a single oxide thickness has been examined, and the effects of annealing on the inversion response has not been discussed. Obviously in the interests

of scaling it is of more relevance to investigate lower oxide thickness samples for reduced $E_{ot}$. The benefit in looking at slightly thicker samples is that leakage current factors are of little significance so fundamental device behavior can be examined. It is important therefore that the optimum passivation allows observation of the inversion behavior in these thin 3.6 nm $Al_2O_3$ films, even after forming gas anneal. Note that these were not pushed too far into accumulation in order not to stress the devices. It was mentioned earlier for pre-FGA $n$-$In_{0.53}Ga_{0.47}As$ devices, that at intermediate frequencies a distortion is observed in the transition to inversion, which was attributed to an interface defect response. Further evidence to support this exists in the CV responses for the $n$-$In_{0.53}Ga_{0.47}As$ varying thickness series pre-anneal. This distortion is seen for all three oxide thicknesses, but the peak is noticeable over a wider bias range as the $Al_2O_3$ thickness is increased. Using the simple relationship Q=CV, which can be re-written as $Q=(\varepsilon_0.\varepsilon_r/t_{ox}).\Delta V$, it is clear that for a given charge associated with an interface defect, a larger $\Delta V$ term is required to maintain



Figure 6.8. Multi-frequency CV responses of $n$-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As/InP$, devices, with $Al_2O_3$ thicknesses of 4nm, 8nm, and 12nm. The plots in the top row represent CVs for the devices pre-anneal, and the plots in the bottom row are the CVs post-FGA (275$^o$C, 30 mins). Note that some frequencies have been omitted from each plot for clarity. Also, given that it was necessary to measure different intermediate frequencies owing to a change in transition frequency (discussed in a subsequent section) the colour of the curves for each sample do not correspond to the same frequency.

the equality with increasing oxide thickness, consistent with what is observed. In the case of the $n$-type devices the profiles of the CV curves post-FGA are modified from the pre-anneal samples. A reduction in the mid-gap $D_{it}$ is noticeable in that the defect related distortion around mid-gap is less evident post-FGA. It is also noticeable that the profiles now exhibit a hump in the transition to strong inversion, which is very similar to the CV behavior observed on the $p$-type samples.

In Figure 6.9 the multi-frequency CV are plotted pre and post-FGA for $p$-$In_{0.53}Ga_{0.47}As$ devices with varying $Al_2O_3$ thickness (the corresponding $G/\omega$ plots can be seen in Appendix 3, Section 10.2). Again the $p$-$In_{0.53}Ga_{0.47}As$ devices exhibit behavior consistent with inversion of the $In_{0.53}Ga_{0.47}As$ surface for all oxide thicknesses. In examining the CVs in Figure 6.9 it is evident that for the $p$-type devices post-FGA, the transition into inversion is steeper, (lower stretch-out, reflected also in the conductance response, Appendix 3), indicating a reduction in $D_{it}$ moving from mid-gap towards the conduction band edge. Also, if one considers the "V" shape in the low frequency CV curves (transition from accumulation to depletion to inversion) then this is clearly steeper on both sides with a lower capacitance measured at the lowest frequency for the post-FGA samples. This is indicative of a reduced $C_{it}$ contribution from interface states over a wide energy range. It is acknowledged that the discussion in this section on the reduction in $D_{it}$ post-FGA for $n$-type and $p$-type devices is somewhat qualitative. To address this, at the time of writing, analysis is being undertaken to quantitatively evaluate the reduction in $D_{it}$ post-FGA, and also to examine any influence of thickness on the $D_{it}$. This will be based on the Conductance Method, using measurements of the conductance response at fixed bias points and sweeping the a.c signal frequency.
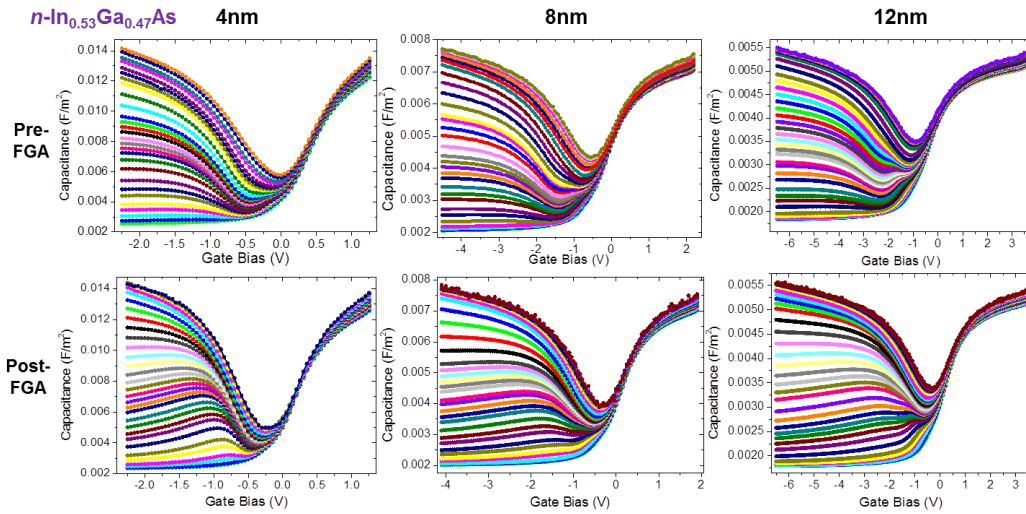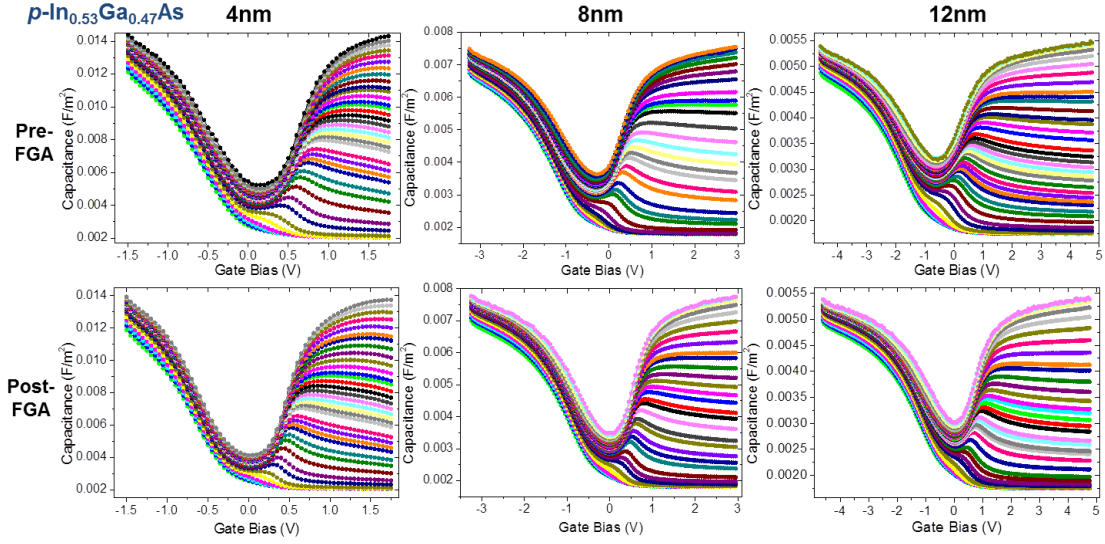
Figure 6.9 Multi-frequency CV responses of *p*-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As/InP, devices, with Al$_2$O$_3$ thicknesses of 4nm, 8nm, and 12nm. The plots in the top row represent CVs for the devices pre-anneal, and the plots in the bottom row are the CVs post-FGA (275$^{\circ}$C, 30 mins). Note that some frequencies have been omitted from each plot for clarity. Also, given that it was necessary to measure different intermediate frequencies were selected owing to a change in transition frequency(discussed in a subsequent section) the colour of the curves for each sample do not correspond to the same frequency.

## 6.9.   Fixed Oxide Charge: Effect of FGA and varying Al$_2$O$_3$ thickness

It is worth briefly mentioning that a shift in the CVs associated with a change in the fixed charge in the Al$_2$O$_3$ oxide layer is observed. To this end the 1MHz CV curves measured before and after FGA are plotted in Figure 6.10. The red curves correspond to the post-FGA responses. For the 4nm Al$_2$O$_3$ samples on both *n*-In$_{0.53}$Ga$_{0.47}$As and *p*-In$_{0.53}$Ga$_{0.47}$As, the pre-FGA curves are positively shifted compared to the post-FGA curves, indicating the removal of negative fixed charge during the anneal. For the two thicker Al$_2$O$_3$ layers, 8nm and 12nm on both *n*-In$_{0.53}$Ga$_{0.47}$As and *p*-In$_{0.53}$Ga$_{0.47}$As, different behavior is observed. In these cases the pre-FGA curves are negatively shifted compared to the post-FGA curves. This implies the removal of fixed positive charge during the anneal of the thicker Al$_2$O$_3$
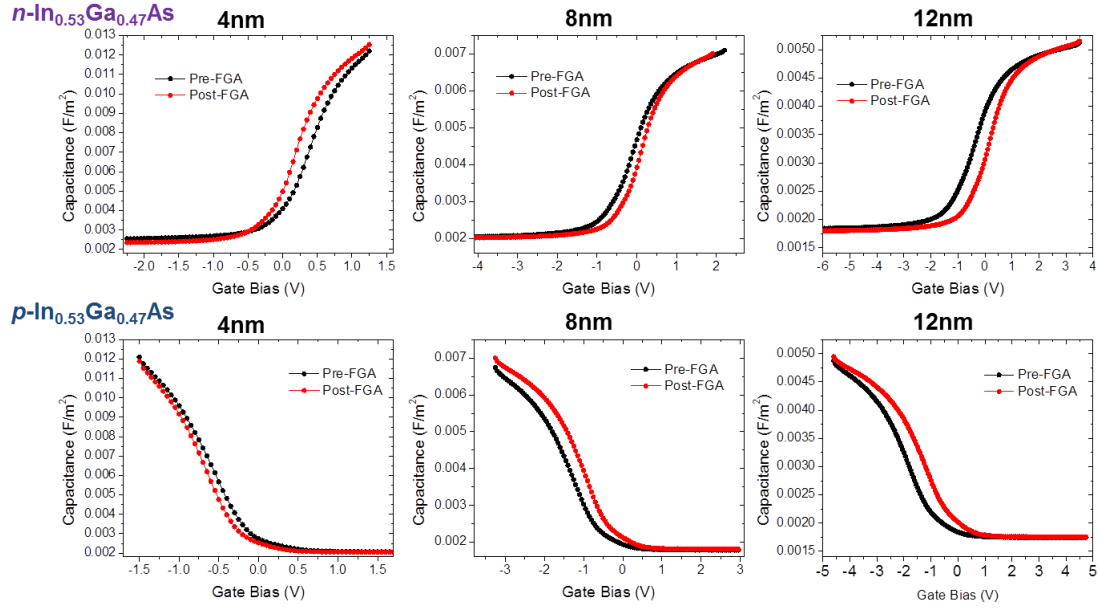
Figure 6.10 1MHz CV responses of *n*-type and *p*-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As/InP, devices, with Al$_2$O$_3$ thicknesses of 4nm, 8nm, and 12nm. The black curves are for the devices pre-anneal, and the red plots are the CVs post-FGA (275$^o$C, 30 mins).

films. Some previous reports have indicated the presence of negative fixed charges in proximity to the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface, and positive fixed charges distributed throughout the Al$_2$O$_3$, both of which were reduced through forming gas annealing. [6, 7, 8] This is entirely consistent with the results presented in Figure 6.10 for this work where for the 4nm films the negative fixed charge is dominant, and for thicker films the positive fixed charge dominates, with the FGA treatment leading to a reduction of the fixed charge components in both cases. Additionally, it would be useful to examine the effect of the FGA on the measured hysteresis in these devices.

## 6.10. G/ω and −ωdC/dω relationship with varying t$_{ox}$

These thickness series samples also serve a purpose in discussion of the relationship derived earlier in Chapter 6 where in strong inversion the maximum value of both G/ω and -ωdC/dω at ω$_m$ was found to be equal to C$_{ox}^2$/2(C$_{ox}$+C$_D$), C$_{ox}$ being the oxide capacitance per unit area and C$_D$ is the semiconductor depletion capacitance in

inversion. For the variable doping series samples in Section 6.7 earlier, there was a situation where $G/\omega$ changes as a result of the changing $C_D$ for a given $C_{ox}$. Conversely for these thickness series samples, $C_{ox}$ is varying but the doping and therefore $C_D$, is fixed. Therefore one would expect that as $C_{ox}$ is increased, the maximum value of $G/\omega$ and $-\omega dC/d\omega$, as predicted by the equality, would increase also. To this end Figures 6.11 and 6.12 show the $G/\omega$ and $-\omega dC/d\omega$ curves for all $Al_2O_3$ thicknesses, both pre-and post FGA, on $n$-type and $p$-type $In_{0.53}Ga_{0.47}As$ respectively. It is clear that the behavior described earlier in Section 6.3 is again evident, ie. $G/\omega$ and $-\omega dC/d\omega$ have the same peak magnitude, occurring at the transition frequency $\omega_m$, and the $G/\omega$ curves have a wider FWHM. Notably the peak magnitudes increase from the 12nm sample which obviously has the lowest $C_{ox}$, to the 4nm sample.
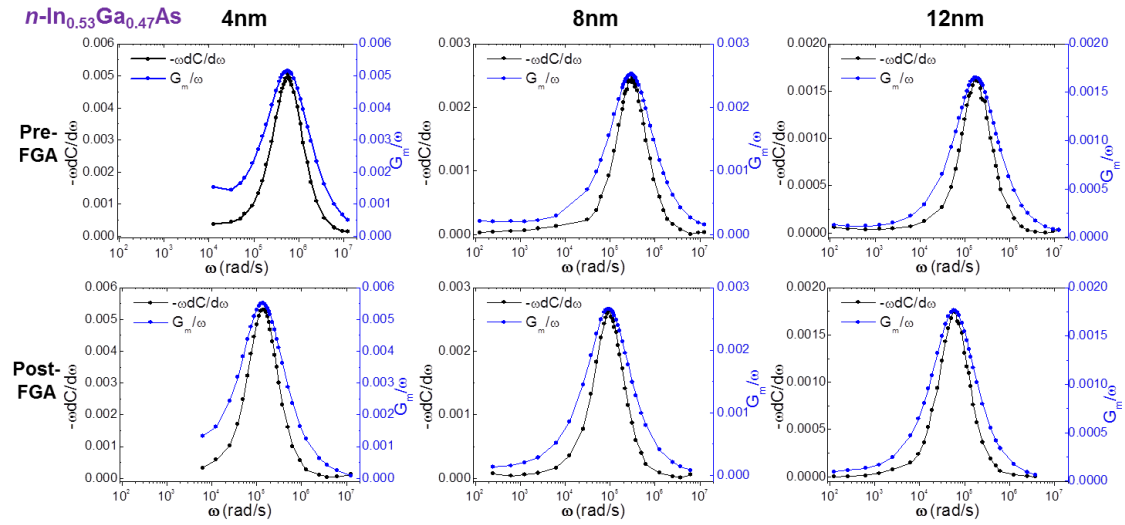


Figure 6.11 $G_m/\omega$ and $-\omega dC/d\omega$ plotted versus $\omega$ (rad/s) in strong inversion for Au/Ni/8nm $Al_2O_3$/$n$-$In_{0.53}Ga_{0.47}As$/$n$-InP devices, pre- and post-FGA. The values of $C_m$ and $G/\omega$ were taken in strong inversion using the CV data plotted in Figure 6.8 and corresponding GV data, Appendix 10.2.
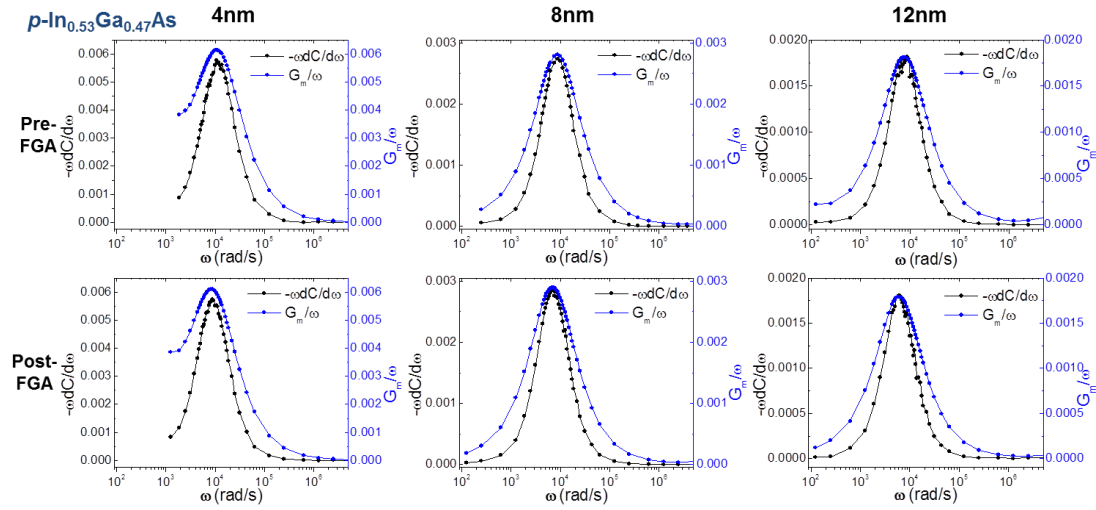
Figure 6.12 $G_m/\omega$ and $-\omega dC/d\omega$ plotted versus $\omega$ (rad/s) in strong inversion for Au/Ni/Al$_2$O$_3$/$p$-In$_{0.53}$Ga$_{0.47}$As/$n$-InP devices, pre- and post-FGA. The values of $C_m$ and $G/\omega$ were taken in strong inversion using the CV data plotted in Figure 6.9 and corresponding GV data, Appendix 10.2.

One can take this a little further and perform an exercise to show the usefulness of the expression derived for $G/\omega$ and $-\omega dC/d\omega$ in strong inversion as a means to estimate $C_{ox}$ for experimental samples. To this end one can compare the following for this thickness series: (i) the $C_{ox}$ as measured experimentally at low frequency; (ii) the value of $C_{ox}$ required to satisfy the equality where the peak $G/\omega$ and $-\omega dC/d\omega$ at $\omega_m$ was found to be equivalent to $C_{ox}^2/2(C_{ox}+C_D)$; and (iii) the $C_{ox}$ value as estimated theoretically using the Al$_2$O$_3$ thickness and a $k$-value for Al$_2$O$_3$, a common approach in many literature reports. For the sake of clarity only the post-FGA results are used. Therefore: for (i) the $C_{ox}$ as recorded at low frequency for the post-FGA samples in Figures 6.8 and 6.9 is used; for (ii) the $C_{ox}$ is fit to the peak $G/\omega$ values as seen in Figures 6.11 and 6.12 using the equality $(G/\omega)_{max}=C_{ox}^2/2(C_{ox}+C_D)$; and for (iii) $C_{ox}$ is determined theoretically using the TEM Al$_2$O$_3$ thickness, and a $k$-value in the range of 7 to 9 for Al$_2$O$_3$, which is a common range reported in literature. Figure 6.13 shows a comparison of (i), (ii) and (iii) for the post-FGA $n$-In$_{0.53}$Ga$_{0.47}$As and $p$-In$_{0.53}$Ga$_{0.47}$As devices.

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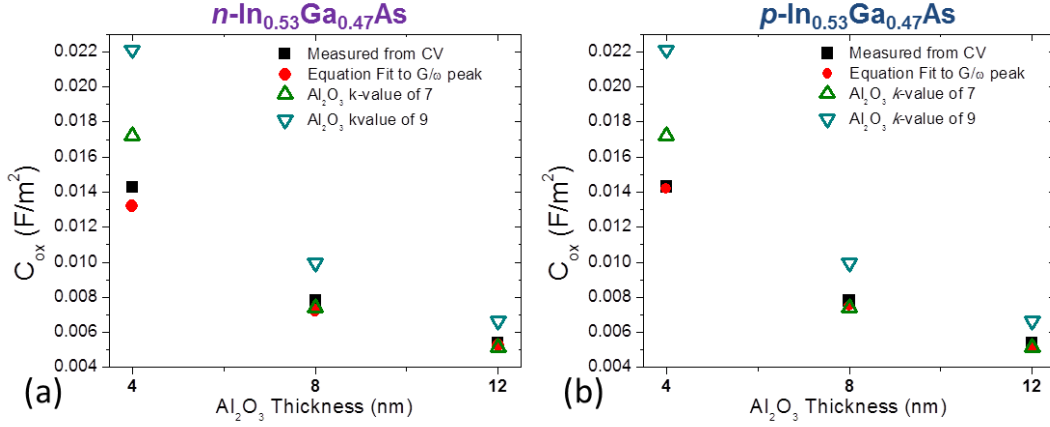
Figure 6.13 Comparison of $C_{ox}$ as determined by three methods (i) from low-frequency CV, (ii) by fitting to $(G/\omega)_{max}$ in inversion, and (iii) assuming an $Al_2O_3$ $k$-value range. This is for post-FGA $n$-type and $p$-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As/InP, devices, with Al$_2$O$_3$ thicknesses of 4nm, 8nm, and 12nm. Note the TEM thicknesses of 3.6nm, 8nm, and 12 nm were used in conjunction with the $k$-values, the use of the 4nm label is for ease of reference.

It is apparent in Figure 6.13 (a) and (b) that the measured $C_{ox}$ at low frequency is in excellent agreement with that predicted by the $(G/\omega)_{max}=C_{ox}^2/2(C_{ox}+C_D)$ relationship derived earlier. This is observed over the entire thickness range. By contrast, it is clear that problems arise when one estimates $C_{ox}$ from a $k$-value for Al$_2$O$_3$, even when the actual oxide thickness is known (from TEM). Even though it appears that 7 is a more realistic Al$_2$O$_3$ $k$-value in the case of the samples in this study, while this provides a $C_{ox}$ estimate in good agreement with the measured $C_{ox}$ at higher oxide thicknesses, a much more significant divergence occurs at lower $E_{ot}$, as seen for the 4nm sample points in Figure 6.13. This is very significant in that lower $E_{ot}$ devices are obviously more relevant from a scaling perspective. Such a strong divergence is not observed when comparing the measured $C_{ox}$ with that predicted by the relationship derived relating the peak values of $G/\omega$ and $-\omega dC/d\omega$ in inversion to $C_{ox}$. This provides a strong practical example that this relationship serves as an extremely useful tool to estimate $C_{ox}$ for experimental devices, and is particularly relevant as one reduces $E_{ot}$.

## 6.11. Influence of $t_{ox}$ and FGA on minority carrier generation lifetime

One feature which was evident from the measurements performed on these samples was there was a reduction in the transition frequency both with increasing $Al_2O_3$ thickness and with forming gas annealing. This is noticeable in the shift in the plots in Figures 6.11 and 6.12. It is illustrated more clearly in Figure 6.14, where the transition frequency (in Hz) is plotted for (a) *n*-type and (b) *p*-type samples. It is very noticeable that there is a dramatic reduction in $\omega_m$ for the *n*-$In_{0.53}Ga_{0.47}As$ devices post-FGA, a factor of about three times for each thickness. The reduction is also evident for *p*-type samples post FGA but is more subtle, although clearly the transition frequency is significantly lower in any case in general for the *p*-type samples both pre- and post-anneal. One also notices that the transition frequency reduces with $Al_2O_3$ thickness on both substrate types.

The corresponding minority carrier generation lifetimes, $\tau_g$, being inversely proportional to $\omega_m$, were obtained from simulation fittings and are plotted in Figures 6.14 (c) and (d). Therefore the effect of reducing $t_{ox}$, and of FGA, is to increase $\tau_g$. This is indicative of passivation of some of the bulk traps in the depletion region responsible for the observed minority carrier responses, also consistent with post-FGA results in recent MOSFET work by Djara *et al.*[9] Given the effect of FGA it is clear that hydrogen plays a large role in this defect reduction, and may also provide a clue as to why $\tau_g$ increases with thickness. Obviously the growth time for the 12nm sample will be longer than that for 4nm sample, therefore any H species present in the ALD chamber from the precursors have the potential to act as a passivant. Additionally, given the samples sit in a heated environment for ALD growth ($300^o$C), the thicker samples will be exposed to this temperature for longer so there may be a mild annealing effect also on these bulk defects responsible for the minority carrier response.
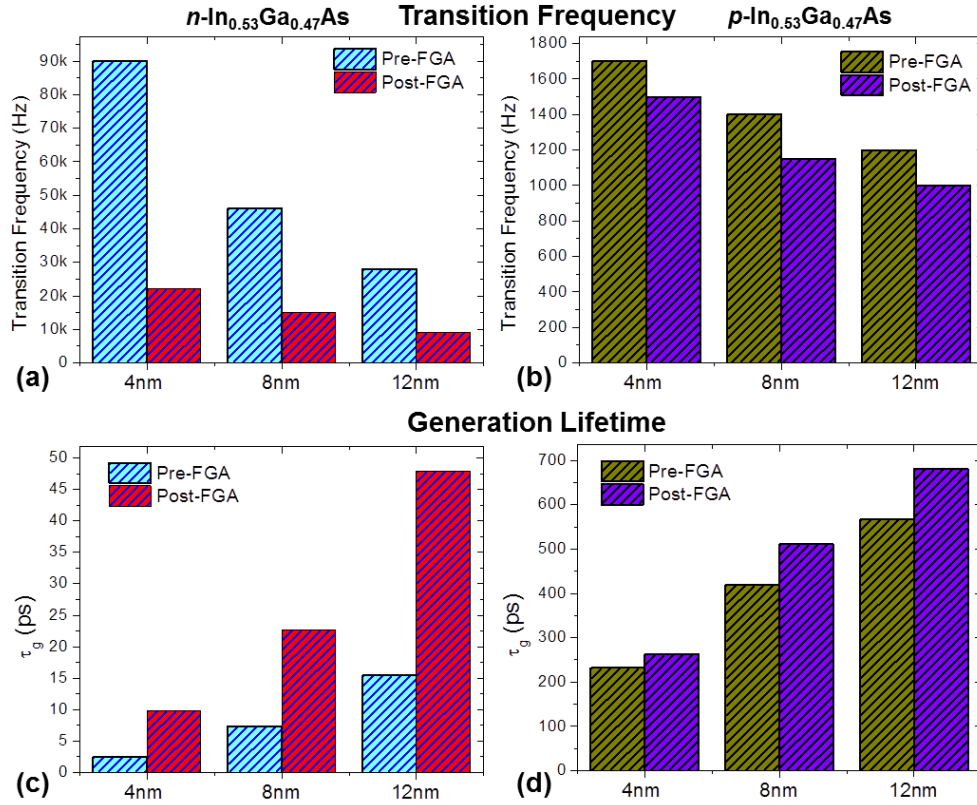
Figure 6.14 Transition Frequencies (Hz) both pre- and post-FGA (275°C, 30 minutes) for (a) *n*-type and (b) *p*-type In$_{0.53}$Ga$_{0.47}$As MOS devices with varying Al$_2$O$_3$ thicknesses. The values were obtained from the multi-frequency CV and G/ω plots. The plots in (c) and (d) are the minority carrier generation lifetimes, τ$_g$, extracted by simulation corresponding to the measured transition frequencies above.

## 6.12. Conclusions

A methodology was developed to provide an experimental route to estimate the value of oxide capacitance, C$_{ox}$, from analysis of the inversion capacitance and conductance of an MOS stack. It was observed experimentally that in strong inversion the magnitude of G/ω and −ωdC/dω are equal. This result is also shown to hold for physics based simulations of G/ω and −ωdC/dω. Using an equivalent circuit model a mathematical derivation of G/ω and −ωdC/dω led to a value of C$_{ox}^2$/(C$_{ox}$+C$_D$) being extracted for (G/ω)$_{max}$ and (−ωdC/dω)$_{max}$, where C$_D$ is the semiconductor depletion

capacitance. This provides an experimental avenue for more accurate determination of $C_{ox}$ for MOS devices. Also, a 275$^o$C forming gas anneal was found to reduce minority carrier response generation lifetimes for $n$ and $p$-In$_{0.53}$Ga$_{0.47}$As devices with a range of Al$_2$O$_3$ thicknesses.

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[3] A. Goetzberger, E. H. Nicollian, *Bell System Technical Journal*, **46**, p 513, (1967).

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[6] P. K. Hurley, E. O'Connor, V. Djara, S. Monaghan, I. M. Povey, R. D. Long, B. Sheehan, J. Lin, P. C. McIntyre, B. Brennan, R. M. Wallace, M. E. Pemble, and K. Cherkaoui, *IEEE Tran. Dev. Mats. Rel.*, **13**, p429, (2013).

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[8] R. D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre, and P. K. Hurley, *J. Electrochem. Soc.*, **158**, G103–G107, (2011).

[9] V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, E. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, *IEEE Tran. Elec. Dev.*, **59**, 1084, (2012).

# Chapter 7

## 7. Summary and Suggestions for Future Work

### 7.1. Summary of work presented in thesis

The primary aim of this thesis was to examine MOS systems incorporating high-$k$ dielectrics on III-V semiconductors, which is a materials system of current interest for future CMOS applications. This was achieved through electrical characterization of MOS devices in order to examine the influence of the semiconductor substrate, to perform optimization of surface passivation techniques, and to differentiate between device electrical behaviour associated with interface state defects or that attributable to true accumulation or inversion of free carriers at the semiconductor surface.

The structural and electrical properties of $HfO_2$ films on GaAs and $In_xGa_{1-x}As$ substrates for x: 0, 0.15, 0.30, and 0.53, were investigated. The large capacitance dispersion with frequency and temperature observed at positive gate bias in devices using $n$-type GaAs and low In content (x = 0.30, 0.15) $In_xGa_{1-x}As$ epitaxial layers was significantly reduced using high In content (x = 0.53) epitaxial layers. This result indicates that when using ALD to form the high-$k$ oxide layers, it is only possible to achieve true accumulation for the $In_{0.53}Ga_{0.47}As$ devices in this study. Comparison of the CV characteristics at 295K and cooled to 77K indicates that the interface defect density is > $2.5\times10^{13}$ cm$^{-2}$, with an energy level $\geq 0.75$ eV above the valence band in the $HfO_2/In_xGa_{1-x}As$ system, where the defect energy with respect to the valence band does not change with the composition of the $In_xGa_{1-x}As$. In the case of the 53% indium concentration $HfO_2/In_xGa_{1-x}As$ MOS structures, this defect is aligned with the $In_{0.53}Ga_{0.47}As$ conduction band energy, and as a consequence, genuine surface accumulation can be achieved in this case. However, electrically active interface defects are still detected in the CV response of $HfO_2/In_{0.53}Ga_{0.47}As$ structures at a

negative gate bias. A post-gate metallization 325$^{\circ}$C forming gas anneal was found to reduce $D_{it}$ at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface.

In varying ammonium sulphide $(NH_4)_2S$ concentrations (from 1% to 22%) in the passivation of *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$, multi-frequency CV results indicated that the lowest frequency dispersion over the bias range examined occurred for devices treated in 10% $(NH_4)_2S$ solution. It has also been shown that there is a deleterious effect on device behaviour for increased ambient exposure time after removal from 10% $(NH_4)_2S$ solution and that XPS analysis detected changes in the composition of the re-grown oxide on this timescale. Estimations of interface state density, $D_{it}$, extracted using the Conductance Method, and the High-Low method, show very good agreement both in terms of magnitude and characteristic peak profile for the optimum 10% $(NH_4)_2S$ passivated $In_{0.53}Ga_{0.47}As$ devices. The results suggest that these *n*-type and *p*-type devices have an integrated $D_{it}$ of $\sim 2.5x10^{12}$ cm$^{-2}$ ($\pm 1x10^{12}$ cm$^{-2}$), with the peak density approximately 0.37eV ($\pm 0.03$ eV) from the valence band edge.

Following an optimized 10% $(NH_4)_2S$ treatment with minimal ambient exposure pre-ALD, a clear minority carrier response was observed for both *n*-type and *p*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS devices. CV and GV characterization as a function of varying frequency, and varying temperature, indicated that the devices exhibited characteristics consistent with inversion of the $In_{0.53}Ga_{0.47}As$ surface. Having eliminated any contribution from peripheral charge effects, the mechanisms for the minority carrier response were determined using Arrhenius plots to extract activation energies for the minority carrier response. This indicated a transition from a generation-recombination regime at lower temperature to a diffusion controlled response at elevated temperatures, for both *n*-type and *p*-type devices. Additionally, MOS capacitors were fabricated on *n* and *p*-$In_{0.53}Ga_{0.47}As$ with semiconductor doping concentrations ranging over two orders of magnitude from $\sim 1x10^{16}$cm$^{-3}$ to $\sim 2x10^{18}$cm$^{-3}$. It was clearly observed for both *n* and *p*-$In_{0.53}Ga_{0.47}As$ devices that the measured $C_{min}$ increases as doping concentration increases, and that the measured $C_{min}$ is in very good agreement with the theoretical value calculated by assuming an inverted surface. These observations are consistent with a $D_{it}$ which is sufficiently

reduced for these *n*-type and *p*-type devices to permit the Fermi level to be swept across the $In_{0.53}Ga_{0.47}As$ band gap at the $Al_2O_3/$ $In_{0.53}Ga_{0.47}As$ interface.

It was observed both experimentally, and supported by simulations, that in strong inversion the peak magnitudes of $G/\omega$ and $-\omega dC/d\omega$ are equal, with the peaks being coincident at the transition frequency, $\omega_m$. Therefore this offers an experimental route to estimate the value of oxide capacitance, $C_{ox}$, from analysis of the inversion capacitance and conductance of an MOS stack. Using an equivalent circuit model mathematical derivations yielded a value of $C_{ox}^2/2(C_{ox}+C_D)$ being extracted for $(G/\omega)_{max}$ and $(-\omega dC/d\omega)_{max}$, where $C_D$ is the semiconductor depletion capacitance. This provides a straightforward method for more accurate determination of $C_{ox}$ for MOS devices. MOS capacitors were fabricated on *n* and *p*-$In_{0.53}Ga_{0.47}As$ with varying $Al_2O_3$ thickness (4nm, 8nm, and 12 nm). The variation in $C_{ox}$ for these devices was used to illustrate the application of the relationship mentioned above, and is shown to be particularly beneficial as $t_{ox}$ is reduced. Additionally, an increase in minority carrier generation lifetime was observed with an increase in $t_{ox}$, and also with post metallization forming gas annealing. This is indicative of an improvement in device quality owing to passivation of bulk $In_{0.53}Ga_{0.47}As$ defects which are responsible for the minority carrier response observed in the generation recombination regime.

Taking the work described in Chapters 5 and 6 in this thesis as a whole, we can summarize the requirements to unambiguously identify inversion not only for MOS gate stacks incorporating III-V materials, but for MOS systems in general:

1) The capacitance and conductance plateau with increasing gate bias in the inversion region.
2) The frequency scaled conductance peaks at the transition frequency, $\omega_m$, this also being the frequency of the mid-capacitance in strong inversion.
3) Analogous behavior is observed with varying temperature and fixed frequency.

4) Arrhenius extractions yield an activation energy of $E_g/2$ for generation and recombination through defects in the depletion region, changing to $E_g$ as diffusion from the bulk becomes dominant at higher temperature.

5) Supply of minority carriers from an external source, peripheral inversion, must be eliminated through multi-frequency CV characterization with varying device area over *n* and *p*-type substrates.

6) The minimum capacitance measured at high-frequency in inversion should scale as a function of the semiconductor doping concentration, and be in agreement with the theoretical minimum capacitance calculated assuming the surface is inverted.

7) $G/\omega$ and $-\omega dC/d\omega$ have equal peak magnitudes, occurring at $\omega_m$, in strong inversion.

8) Based on mathematical derivations from an equivalent circuit model, the peak magnitude of $G/\omega$ and $-\omega dC/d\omega$ approaches $C_{ox}^2/2(C_{ox}+C_D)$.

It is noted that the work described here on MOS capacitors has proved relevant to fabrication of more complicated FET device structures incorporating III-V materials. The optimized 10% $(NH_4)_2S$ surface passivation, and the forming gas annealing parameters, developed in the course of this MOS work, were incorporated into the processing of conventional and junctionless III-V planar MOSFETs and FINFETs developed by Dr. Vladimir Djara at Tyndall National Institute.[1] Furthermore, the optimized 10% $(NH_4)_2S$ passivation procedure has been adopted by other research groups for use in applications such as buried channel planar and 3-dimensional InGaAs MOSFETs,[2] and also in the process flow of FINFETs incorporating integration of InGaAs channels on Si.[3]

## 7.2. Suggestions for future work

One possible route forward which could yield valuable information would be to attempt to correlate the electrical behavior of the MOS devices examined with more detailed analysis of structural properties at the interface. For example, samples could

be generated with a deliberately high $D_{it}$, and then compared to samples processed using the methodology whereby it is know that $D_{it}$ is reduced sufficiently to observe a minority carrier response. A technique such as XPS or EELS may then be useful in analyzing any differences in the composition of oxide species at the interface which may go some way to explaining the improvement observed in the electrical behaviour. As mentioned already, correlation of structural properties with electrical characteristics, and specific atomic identification of the interface defects responsible, is an area which is still under-explored in the literature in general. This could also be related to first principles simulations to paint a more complete picture of what is occurring at the critical interface of high-$k$ oxides on III-V semiconductors. These first principles simulations could be used to determine the defect energies and charge transitions associated with a range of defects which are fundamental to the interface, such as dangling bonds, dimers and anti-sites associated with the As, In and Ga elements, and these defects levels and charge transitions could be related to what is measured experimentally. If successful this approach could provide insight into the atomic nature of the interface states which are detected in the CV and GV measurements of the high-$k$/ $In_{0.53}Ga_{0.47}As$ MOS structures.

Another possible avenue for further progress would be to examine the influence of the InGaAs epitaxial growth conditions on device behavior. The growth conditions for $n$-type and $p$-type InGaAs are slightly different in terms of temperature, and obviously thermal budget can be critical in terms of the electrical properties of ensuing devices. The results in Chapters 5 and 6 indicate that the $D_{it}$ moving towards the valence band in $n$-type devices can be reduced sufficiently to observe a minority carrier response, while some dispersion associated with defects is still observed in what would be the corresponding energy range over $p$-type samples. Indeed in much of the literature very significant dispersion is typically reported towards the valence band edge for $p$-type devices. Therefore it may be a useful exercise to examine the influence of changing the parameters for MOVPE growth of the $p$-type devices and subsequently to assess how this alters the surface reconstruction of the InGaAs and the resulting $D_{it}$ profile. This could provide further insight into the asymmetry in the $D_{it}$ profile over $n$-type and $p$-type InGaAs devices.

Finally, it would be of interest to explore further the ambient exposure during the transfer from the optimized 10% $(NH_4)_2S$ solution to the atomic layer deposition chamber. It could be a valuable extension of the studies in this thesis to perform the optimized 10% $(NH_4)_2S$ in a nitrogen filled glove box, and be able to transfer the sample in a vacuum container to an ALD system which could load the sample from the vacuum vessel. While this would be quite difficult to achieve practically, it would allow a range of important experiments. One experiment would be to have no ambient exposure between the optimized 10% $(NH_4)_2S$ surface passivation and the oxide ALD growth, and assess how much additional improvement can be achieved when compared to the 3 minutes transfer time in air, which was the minimum time air exposure in this thesis. This would also allow the sample to be exposed to controlled environments between the optimized 10% $(NH_4)_2S$ surface passivation and the ALD, such as $O_2$ and $CO_2$, and with and without light exposure. Based on these experiments it may be possible to determine what is causing the generation of interface states during ambient exposure.

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[2] J. J. Gu, A. T. Neal, and P. D. Ye, *Appl. Phys. Lett.,***99**, 152113 (2011).

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# Appendix 1

## 8. Publications, Conference Presentations, Awards.

### 8.1. Publications directly linked to work presented in Thesis

E. O'Connor, K. Cherkaoui, S. Monaghan, D. O'Connell, I. Povey, P. Casey, S.B. Newcomb, Y.Y. Gomeniuk, G. Provenzano, F. Crupi, G. Hughes, P. Hurley, *J. of Appl. Phys.*, 111, 12 , 124104, (2012).

E. O'Connor, S. Monaghan, K. Cherkaoui, I. Povey, P. Hurley, *Appl. Phys. Lett.*, 99, 21, 212901, (2011).

E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S.B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M.E. Pemble, R.M. Wallace, P.K. Hurley, *J of Appl. Phys.*, 109, 2, 24101, (2011).

E. O'Connor, B. Brennan, R. Contreras, M. Milojevic, K. Cherkaoui, S. Monaghan, S.B. Newcomb, M.E. Pemble, G. Hughes, R.M. Wallace, P.K. Hurley, *ECS Trans.*, 28, 1, 231, (2011).

P.K. Hurley, E. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, J. MacHale, A.J. Quinn, G. Brammertz, M. Heyns, S.B. Newcomb, V. V. Afanas'ev, A. M. Sonnet, R. V. Galatage, M. N. Jivani, E. M. Vogel, R. M. Wallace, M. E. Pemble, *ECS Trans.*, 25, 6, 113 (2009).

E. O'Connor, S. Monaghan, R. Long, A. O'Mahony, I. Povey, K. Cherkaoui, M. Pemble, G. Brammertz, M. Heyns, S.B. Newcomb, V.V. Afanas'Ev, P.K. Hurley, *Appl. Phys. Lett.*, 94, 10, 102902 (2009).

## 8.2. Conference Presentations

### 8.2.1. Oral Presentations:

(1) É. O'Connor *et al.*, **2013 MRS Spring Meeting**, April 1-5, 2013, San Francisco, California.

"*The characteristic features of capacitance and conductance for surface inversion in $In_{0.53}Ga_{0.47}As$ MOS capacitors*".

(2) É. O'Connor *et al.*, **2011 MRS Spring Meeting**, April 25 - 29, 2011, San Francisco, California.

"*Improved CV response for $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS Capacitors using optimized $(NH_4)_2S$ treatment*".

(3) É. O'Connor *et al.*, **219th ECS Meeting**, May 1 - May 6, 2011, Montreal, Canada.

"*Improved capacitance-voltage characteristics of MOS capacitors on GaAs incorporating a PECVD deposited $Si_3N_4$ dielectric layer*".

(4) É. O'Connor *et al.*, **16th WODIM**, June 28 – June 30, 2010, Bratislava, Slovakia.

"C*apacitance-voltage characteristics of MOS capacitors on GaAs incorporating a PECVD deposited Si$_3$N$_4$ dielectric layer*".

*(5)* É. O'Connor *et al.*, **217th ECS Meeting**, April 25-30, 2010, Vancouver, Canada.

*"(NH$_4$)$_2$S passivation of high-k/In$_{0.53}$Ga$_{0.47}$As surfaces: A systematic study of (NH$_4$)$_2$S concentration"*.

### 8.2.2. Poster Presentations:

(1) É. O'Connor *et al*., **18$^{th}$ WODIM**, June 9-11, 2014, Kinsale, Ireland.

*"Minority carrier response of n-type and p-type In$_{0.53}$Ga$_{0.47}$As MOS capacitors with varying Al$_2$O$_3$ thickness and In$_{0.53}$Ga$_{0.47}$As doping concentration"*

(2) É. O'Connor *et al*., **Intel ERIC**, October 13-15, 2011, Leixlip, Ireland.

*"Analysis of the minority carrier response of n-type and p-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOS capacitors following optimized (NH$_4$)$_2$S treatment"*

(3) É. O'Connor *et al*., **Intel ERIC**, October 12-14, 2010, Leixlip, Ireland.

*"(NH$_4$)$_2$S passivation of high-k/In$_{0.53}$Ga$_{0.47}$As surfaces: A systematic study of (NH$_4$)$_2$S concentration"*

(4) É. O'Connor *et al.*, **39th IEEE SISC**, December 11-13, 2008, San Diego, CA *"Temperature dependent capacitance-voltage and conductance-voltage characterisation of the HfO₂ / In$_x$Ga$_{1-x}$As interface: The influence of In% concentration and low temperature forming gas annealing"*

## 8.3.  Awards

2013: Marie Curie Intra-European Fellowship

É. O'Connor was granted a two-year Marie Curie Intra-European Fellowship grant for a proposal submitted in conjunction with IBM Research in Zurich, to commence in January 2015.

2010: BOC Gases PhD Bursary Award.

The BOC gases award is granted annually to one PhD student in Tyndall based on the quality of their research and journal publications. There were around 100 PhD students in Tyndall in 2010.

2008: Tyndall Annual Best Paper Award.

Tyndall National Institute awarded an annual best paper prize which was open to both researchers and students. This was awarded for the following publication:

É. O'Connor, *et al.*, Applied Physics Letters, **92**, 022902 (2008). *"In-situ H$_2$S passivation of In$_{0.53}$Ga$_{0.47}$As/InP metal-oxide-semiconductor capacitors with atomic-layer deposited HfO$_2$ gate dielectric"*

## 8.4.    Full List of Publications

This list is accurate as per Google Scholar, September 2014.

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# Appendix 2

## 9. Appendix 2: Peripheral Inversion in MOS devices

During the development of high-$k$ processes on semiconductor surfaces it is possible to have a metal gate patterned on the high-$k$ oxide surface with no additional passivation, leaving the oxide regions outside the gate area exposed to ambient conditions as well as processing steps such as reactive ion etching, rapid thermal processing, and forming gas annealing. These processing steps have the potential to induce charge within the oxide, or leave residual charge on oxide surfaces, in particular where the oxide is exposed during such a processing step. If this oxide charge results in depletion of the semiconductor surface and the density of the residual charge is higher than the semiconductor charge associated with the maximum depletion width (~ $8x10^{10}$ cm$^{-2}$ for $1x10^{15}$ cm$^{-3}$ doping concentration), then peripheral inversion will be present outside the area defined by the gate electrode.[1,2]

As an illustrative example of this behavior for a Si-based MOS device, the CV response at room temperature (295K) with ac signal frequencies from 2 kHz to 1 MHz for the NiSi/MgO/$p$-Si devices are shown in Figures 9.1 (a), (b), and (c) for capacitor squares with dimensions of 30x30 μm, 60x60 μm, and 90x90 μm respectively. The multi-frequency CV responses for the corresponding $n$-type devices are shown as insets to Figures 9.1 (a-c). Firstly, in analyzing the CV response in Figure 9.1 (a) for the smallest device area (30x30 μm), what appears to be a low frequency response is observed in the gate bias range of ~ -0.5 V to 4 V, at the lowest measured frequency of 2 kHz. However, the capacitance in this bias range still remains high for the 1 MHz curve, which is not expected for typical minority carrier lifetimes in silicon. In the case of a low frequency CV response due to the generation and recombination of minority carriers in the depletion region of the silicon, low
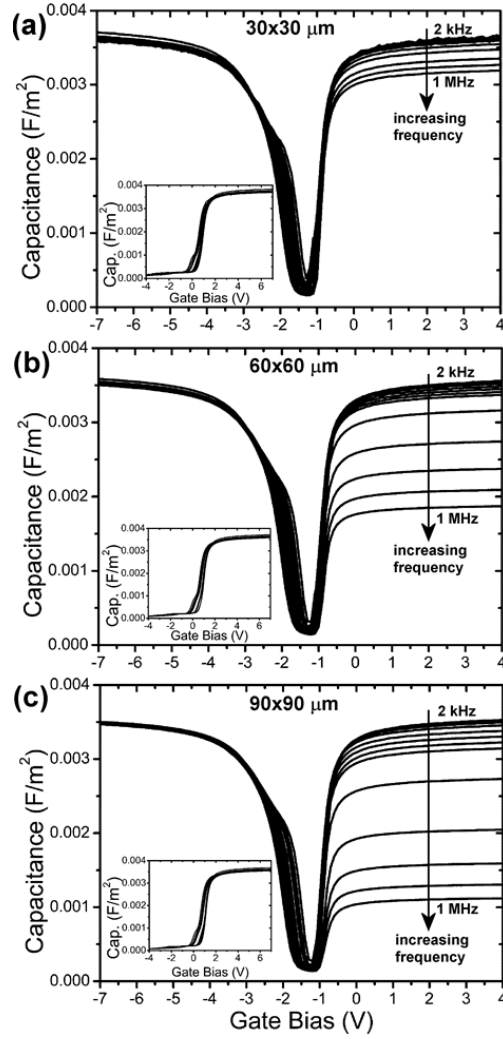
Figure 9.1 The C-V multi-frequency response at room temperature (295 K) of the NiSi/MgO/$p$-Si devices for capacitor squares with dimensions of (a) 30x30 μm, (b) 60x60 μm, and (c) 90x90 μm respectively. The multi-frequency CV responses for the corresponding $n$-type devices are shown as insets. The ac signal frequencies range from 2 kHz to 1 MHz in all cases.

frequency CV characteristics are not typically recorded at frequencies above 100 Hz. In the work of Goetzberger and Nicollian,[3] for a $SiO_2$/$n$-Si device measured at room temperature, a frequency as low as 10 Hz was required to observe the full inversion response, and the transition frequency was 70 Hz.

A possible explanation for this effect is shown in Figure 9.2, which shows plan and cross sectional views of MOS capacitors with different gate areas, where
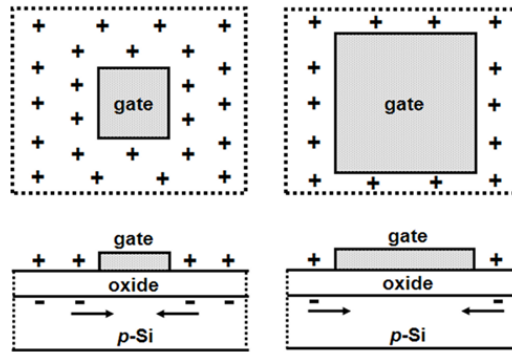
Figure 9.2 Schematic to illustrate a possible mechanism for peripheral inversion effects for *p*-type MOS devices. A plan view looking down on the gate area is shown for a smaller device (on the left) and a device where the perimeter-length is doubled (on the right). Beneath these, corresponding cross-sectional schematics illustrate the MOS device structure in each case.

charge exists on the oxide surface, (or within the oxide), in the region outside the area defined by the gate electrode area. If this oxide surface charge is of the same type as the semiconductor doping it will induce a corresponding charge of the opposite sign in the semiconductor at the oxide/semiconductor interface, and will give rise to an inversion region in the peripheral area outside the area defined by the gate oxide ("peripheral inversion"), if the oxide charge density [cm$^{-2}$] is larger than the product of the doping concentration in the semiconductor and the maximum depletion width. The resulting peripheral inversion layer is a source of minority carriers, which can be supplied to the area under the gate electrode once the oxide/semiconductor interface under the gate electrode is inverted by the applied gate voltage. Capacitance-voltage measurements performed at multiple frequencies and on varying capacitor areas on both *n*-type and *p*-type devices can be used to determine if such peripheral inversion is responsible for the low frequency behaviour, as the low frequency behaviour provided through peripheral inversion would exhibit specific CV behaviour in the following ways:

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(1) For a given device area the inversion response will reduce with increasing ac measurement frequency.

(2) At a given ac signal frequency the inversion response will be reduced as the device area increases, due to the increasing diffusion distance from the periphery to the centre of the gate electrode.

(3) The low frequency inversion like behaviour will be observed for either $n$ or $p$ doped semiconductor substrates, and not for both, as a given oxide charge will only invert the oxide/semiconductor surface for one dopant type.

While the observations described in (1) will be observed for minority carriers supplied either from under the gate area (by generation/recombination or diffusion from the quasi-neutral bulk), or via a peripheral inversion charge, the observations described in (2) and (3) are not consistent with minority carrier supply from the depletion region under the gate electrode. The supply of minority carriers by generation/recombination in the depletion region or by diffusion from the quasi-neutral bulk, should not exhibit a dependence on the electrode area, and should also be present for both $n$ and $p$ type semiconductor substrates.

The CV responses in Figures 9.1 (b) and (c) are consistent with the presence of a peripheral inversion region, as the low frequency inversion-like behaviour in the region -0.5V to 4V is observed to decrease as the area is increased for the 60x60 µm device in Figure 9.1 (b) and the 90x90 µm device in Figure 8.1 (c). We can determine that the charge on the surface or in the bulk of the oxide is positive in this case, which induces negative charge in the substrate, leading to an inversion response for the $p$-type devices. The results for the same NiSi/MgO gate stack over $n$ type Si are shown as insets in Figures 9.1 (a-c). For the $n$ type silicon no inversion behavior is observed, as the positive oxide charge will result in accumulation of the semiconductor surface in this case. This is again consistent with the source of the minority carriers originating from the periphery of the device.

The CV response at room temperature (295K) for NiSi/MgO/$p$-Si devices with varying capacitor dimensions from 30x30 $\mu$m to 100x100 $\mu$m, are shown in

Figures 9.3 (a), (b), and (c), for fixed ac signal measurement frequencies of 10kHz, 100 kHz, and 1 MHz respectively. The corresponding CV responses for *n*-type Si devices are plotted as insets. For the *p*-type devices at low frequency (10 kHz) in Figure 9.3 (a) the peripheral inversion charge has time to respond to the ac signal and contribute to the measured capacitance, even for the largest device area (100x100 *μ*m). However at 100 kHz in Figure 9.3 (b) there is a more rapid drop-off in the
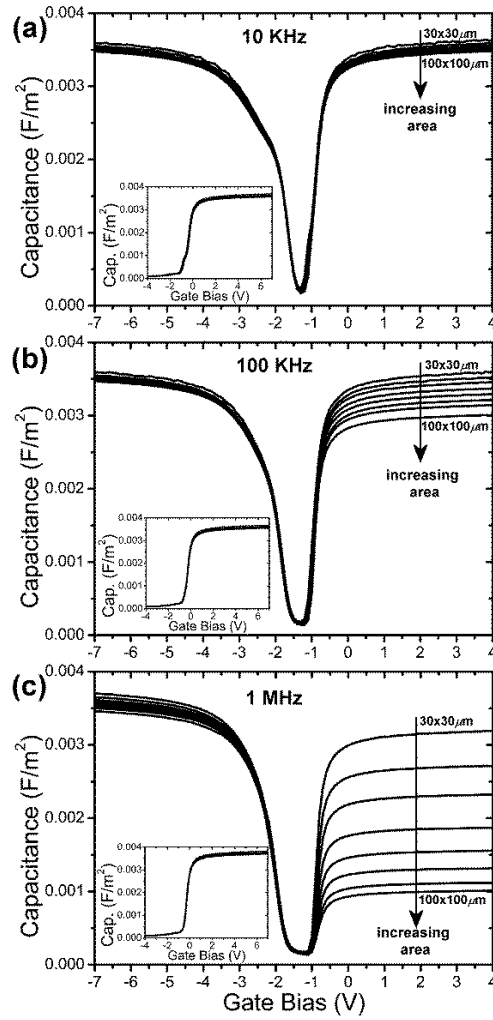


Figure 9.3 The C-V response at room temperature (295K) for NiSi/MgO/*p*-Si MOS devices with capacitor squares having varying dimensions from 30x30 μm to 100x100 μm, are shown for fixed ac signal measurement frequencies of (a) 10kHz, (b) 100 kHz, and (c) 1 MHz. The corresponding *n*-type Si device CV responses are plotted as insets. MOS capacitor side lengths are 30, 40, 50, 60, 70, 80, 90, 100 *μ*m.

peripheral inversion response as the device area increases. This is more pronounced again for the 1 MHz curves plotted in Figure 9.3 (c). It is noted that for the *n*-type devices plotted in the insets to Figures 8.3 (a-c), no low frequency CV behaviour is observed for any ac signal frequency from 2kHz to 1MHz for the three device areas. It has been also been shown that such behaviour is not unique to a particular device structure or set of processing conditions. While for these MgO/Si devices the periperhal inversion effect is observed over *p*-type, it has also been observed over *n*-type Si devices with a GdSiO$_x$ dielectric, and further details and plots can be found in the full publication on this work.[1]

It is however important to state that this phenomenon is not restricted to Si substrates. To illustrate this, results are now presented showing evidence of peripheral inversion effects for an MOS system on a III-V semiconductor, GaAs. The C-V response at room temperature (295K) for Au/Ni/Al$_2$O$_3$/*n*-GaAs(111B) devices with varying capacitor dimensions from 30x30 μm to 90x90 μm, are shown in Figure 9.4 for a fixed ac signal measurement frequency of 200 Hz. The corresponding CV responses for *p*-type GaAs(111B) devices are plotted as the inset to Figure 8. Under normal measurement conditions it should not be possible to observe a minority carrier response on GaAs. As discussed by Passlack *et al.,*[4] low-intensity light illumination is required to generate sufficient minority carriers to observe inversion in C–V measurements on GaAs, as the GaAs energy gap (1.42eV) results in a reduction of the thermal generation/recombination rate. In this work, the measurements presented in Figure 9.4 were obtained at room temperature, on-wafer, in a light-tight probe station in a dry air environment. Most importantly, as the measurements were performed in the dark this rules out any contribution of generation of minority carriers through light illumination. It is clear that the minority carrier response in Figure 9.4 is area dependent, and it is only observed on one substrate polarity (see Fig. 9.4 inset), indicating a peripheral inversion effect is responsible for inducing the minority carrier response. This work has also been recently cited by Byun *et al* who used this methodology to identify peripheral inversion effects in their HfO$_2$/GaAs devices.[5]
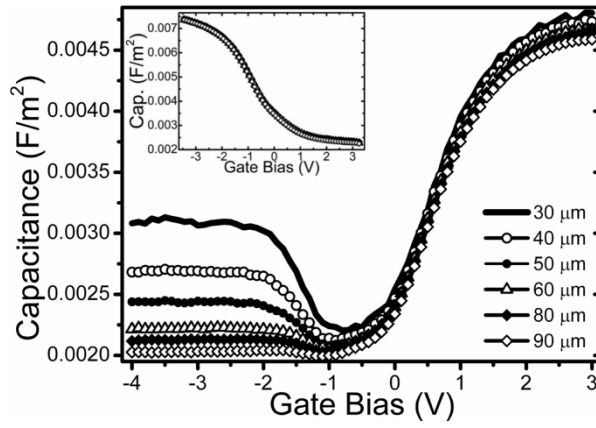
Figure 9.4: The C-V response at room temperature (295K) for Au/Ni/Al$_2$O$_3$/$n$-GaAs(111B) devices with varying capacitor diameters from 30x30 μm to 90x90 μm, are shown for a fixed ac signal measurement frequency of 200 Hz. The corresponding $p$-type GaAs(111B) device CV responses are plotted as an inset. The square MOS capacitors have side lengths of 30, 40, 50, 60, 80, 90 $\mu$m.

[1] E O'Connor, K. Cherkaoui, S. Monaghan, D. O'Connell, I. Povey, P. Casey, S. B. Newcomb, Y. Y. Gomeniuk, G. Provenzano, F. Crupi, G. Hughes, P. K. Hurley, *J. Appl. Phys.*, **111**, 124104 (2012).

[2] E. Nicollian, J. Brews, *MOS Physics and Technology* Wiley, New York, (1982).

[3] A. Goetzberger, E. H. Nicollian, Bell System Technical Journal, **46**, p 513, (1967).

[4] M. Passlack, M. Hong, J. P. Mannaerts, R. L. Opila, S. N. G. Chu, N. Moriya, F. Ren,  and J. R. Kwo, *IEEE Trans. Elec. Dev.*,  **44** (2) 214 (1997).

[5] Y. C. Byun, S. Choi, Y. An, P. C. McIntyre,  and  H. Kim *ACS Appl. Mater. Interfaces*,  **6,**  p 10482, (2014).

# Appendix 3

## 10. Appendix 3 – Supplementary Results

### 10.1. CV and G/ω plots for variable doping experiment samples

The plots below represent the CV and G/ω versus gate bias plots for the Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As devices with varying doping. The discussion of device behaviour with varying semiconductor doping can be found in Section 5.8 of the main thesis.
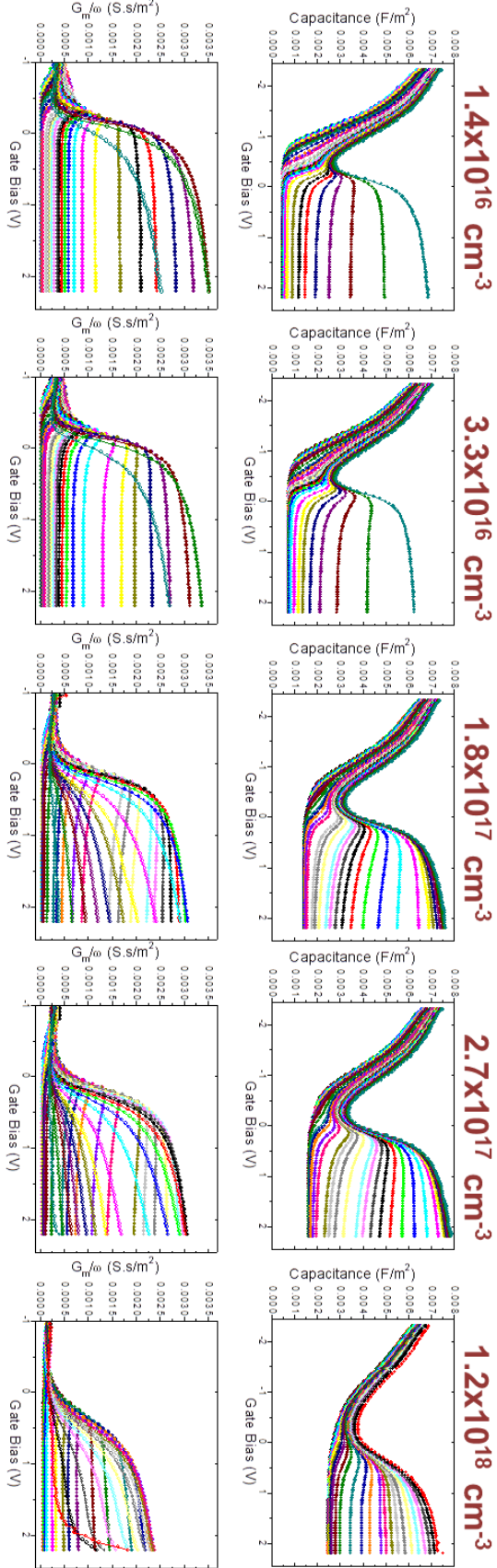
Multifrequency CV (top row) and G/ω (bottom row) responses for Ni/Au/7nm $Al_2O_3$/$p$-$In_{0.53}Ga_{0.47}$As devices where the doping concentration is varied from $1.4 \times 10^{16} cm^{-3}$ to $1.2 \times 10^{18} cm^{-3}$. The y-axis scales are kept the same for all plots to graphically highlight both the increase in $C_{min}$ and reduction in G/ω as doping is increased.
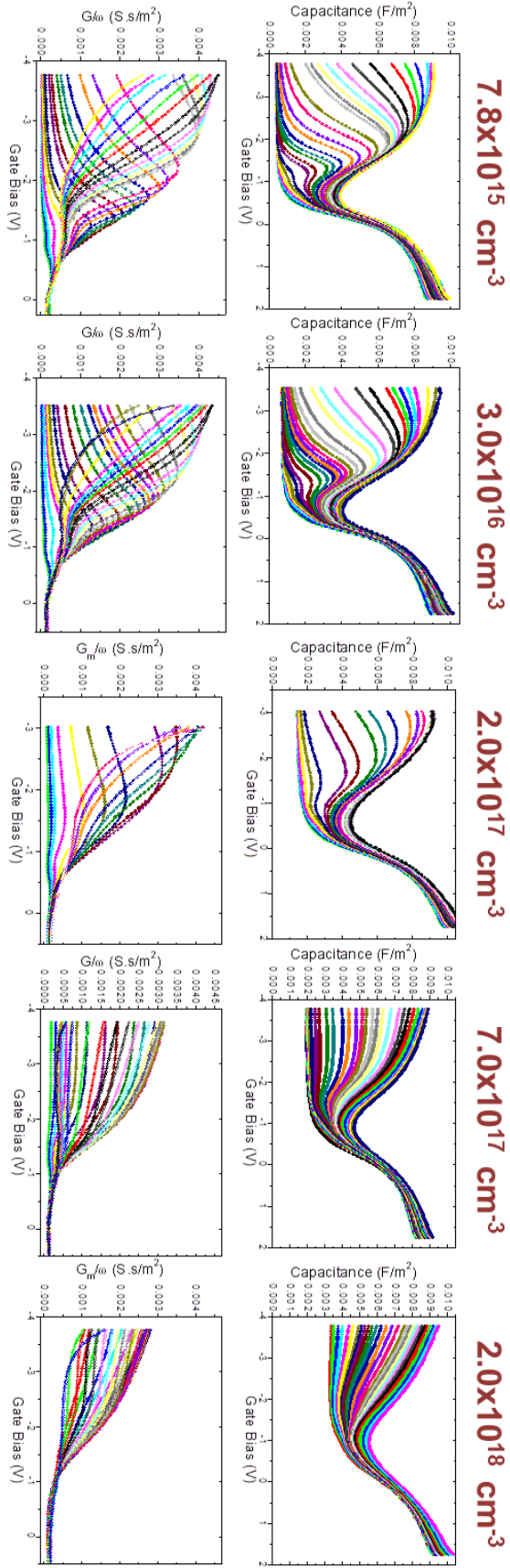
Multifrequency CV (top row) and G/ω (bottom row) responses for Ni/Au/5nm Al$_2$O$_3$/$n$-In$_{0.53}$Ga$_{0.47}$As devices where the doping concentration is varied from 7.8x10$^{15}$cm$^{-3}$ to 2.0x10$^{18}$cm$^{-3}$. The y-axis scales are kept the same for all plots to graphically highlight both the increase in C$_{min}$ and reduction in peak G/ω as doping is increased.

## 10.2. G/ω plots for variable Al$_2$O$_3$ thickness samples

The plots below represent the G/ω versus gate bias plots for the Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As devices with varying Al$_2$O$_3$ thickness. The CVs and relevant discussion can be found in Section 6.8 of the main thesis.
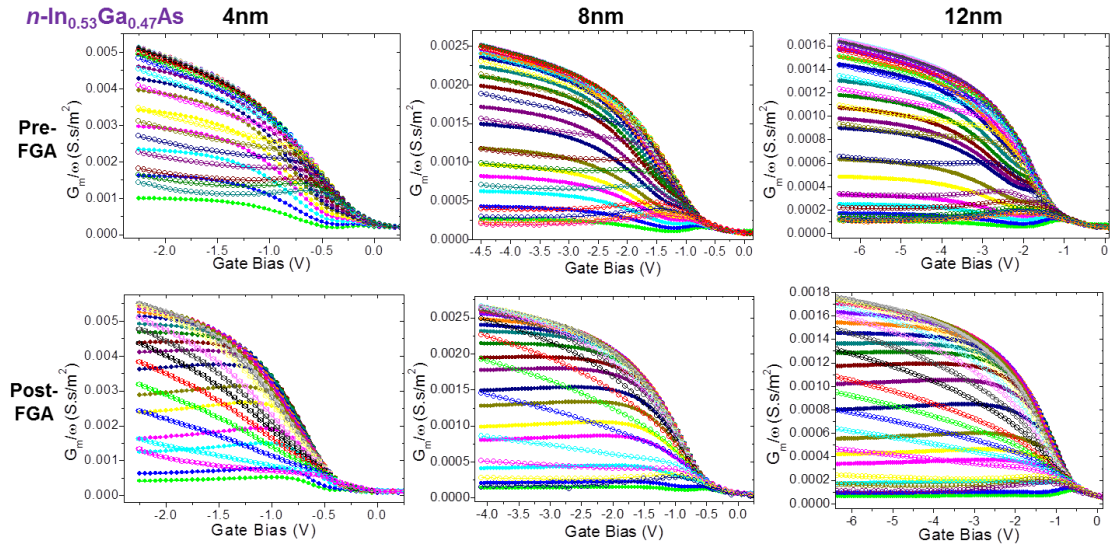


Figure 10.3. Multi-frequency G/ω responses of *n*-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As/InP, devices, with Al$_2$O$_3$ thicknesses of 4nm, 8nm, and 12nm. The plots in the top row represent G/ω curves for the devices pre-anneal, and the plots in the bottom row are the G/ω curves post-FGA (275$^o$C, 30 mins). Note that some frequencies have been omitted from each plot for clarity. Also, given that it was necessary to measure different intermediate frequencies owing to a change in transition frequency (discussed in the main thesis in Chapter 6) the colour of the curves for each sample do not correspond to the same frequency. The frequency scaled conductance, G/w, can also be expressed in units of F/m$^2$.
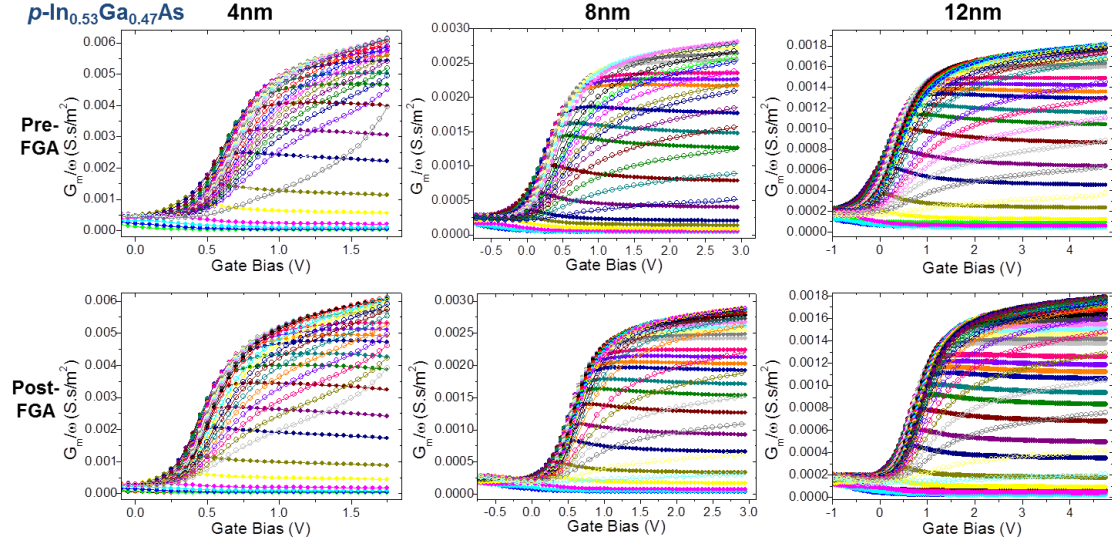
Figure 10.4. Multi-frequency G/ω responses of *p*-type Au/Ni/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As/InP, devices, with Al$_2$O$_3$ thicknesses of 4nm, 8nm, and 12nm. The plots in the top row represent G/ω curves for the devices pre-anneal, and the plots in the bottom row are the G/ω curves post-FGA (275$^{\circ}$C, 30 mins). Note that some frequencies have been omitted from each plot for clarity. Also, given that it was necessary to measure different intermediate frequencies owing to a change in transition frequency(discussed in the main thesis in Chapter 6) the colour of the curves for each sample do not correspond to the same frequency. The frequency scaled conductance, G/ω, can also be expressed in units of F/m$^2$.

# Appendix 4

## 11. Appendix 4 – Supplementary Information

### 11.1. Mathematical derivation of the terms G/ω,-ωdC/dω

This mathematical analysis was performed by Liam Floyd and Scott Monaghan from Tyndall, and is reproduced here with permission.

We have observed experimentally that the graphs of $f_1(w) = \frac{G(w)}{w}$ and $f_2(w) = \frac{-w\, dC(w)}{dw}$ both have the same local maximum value at the same value of ω. They also both exhibit a very clear graphical symmetry when plotted against the logarithm of ω. In this appendix we examine the properties that the unknown function $G_{gr}(\omega)$ must satisfy if these observations are to hold true.

In the main body of the paper we defined $\omega_m$ ("m" for Mid) to be the frequency at which the monotone decreasing capacitance $C(\omega)$ is midway between its low frequency limit ($C_{ox}$) and its high frequency limit $C_D.C_{ox}/(C_D+C_{ox})$, i.e.

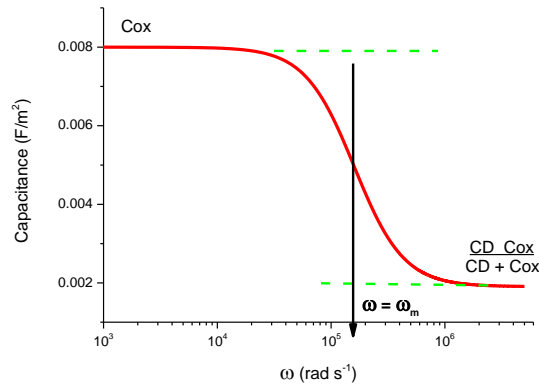$$C(w_m) = \frac{1}{2} C_{ox}\left(1 + \frac{C_D}{C_D + C_{ox}}\right)$$



Fig. 1 Definition of $\omega_m$

Since $C(w) = C_{ox}(1 - \frac{C_{ox}(C_D+C_{ox})w^2}{G_{gr}(w)^2+(C_D+C_{ox})^2w^2})$

We must have $\quad C_{ox}\left(1 - \frac{C_{ox}(C_D+C_{ox})w_m^2}{G_{gr}(w_m)^2+(C_D+C_{ox})^2w_m^2}\right) = \frac{1}{2}C_{ox}(1 + \frac{C_D}{C_D+C_{ox}})$

Solving this quadratic for $G_{gr}(\omega_m)$ we see that the unknown function $G_{gr}(\omega)$ must satisfy $G_{gr}(\omega_m) = \omega_m(C_D+C_{ox})$.

Since $f_1(\omega) = (C_{ox}^2 G_{gr}(\omega) \omega)/(G_{gr}(\omega)^2+(C_D+C_{ox})^2 \omega^2)$

we see that $f_1'(\omega_m) = 0$ (we need to use $G_{gr}(\omega_m) = \omega_m(C_D+C_{ox})$ for this, otherwise $G_{gr}(w)$ may be arbitrary).

Differentiating once again gives $f_1''(\omega_m) < 0$ and thus $f_1(\omega)$ has a local maximum at $\omega=\omega_m$ & by direct evaluation the value of this local maximum is

$f_1(\omega_m) = C_{ox}^2/ (2(C_D+C_{ox}))$

A further calculation shows that

$$\left(1 - \frac{G_{gr}'(w_m)}{C_D + C_{ox}}\right)f_1(w_m) = f_2(w_m)$$

So our two graphs will cross at $\omega=\omega_m$ (or at least touch ) only if $G_{gr}'(w_m) = 0$ , hence this is a requirement on $G_{gr}(w)$. While it cannot be demonstrated based on higher order derivatives that $f_2(\omega)$ has a local maxima at $\omega_m$, it is possible to demonstrate that $f_2(\omega)$ has a local maxima be using the symmetry which is evident in the experimental and simulated function $f_1(\omega)$ and $f_2(\omega)$.

It is easily shown that a function $f(\omega)$ that exhibits graphical symmetry about $\omega = \omega_m$ in a plot of $f(\omega)$ against $Log(\omega)$ necessarily has the mathematical symmetry that $f(\omega)=f(\omega_m^2/\omega)$. Since $f_1(\omega) = G(\omega)/\omega$ exhibits graphical symmetry about $\omega=\omega_m$ when plotted against $Log(\omega)$, we must have $f_1(\omega)= f_1(\omega_m^2/\omega)$.

A short calculation shows that this can only happen if $G_{gr}(\omega)$ has the mathematical symmetry

$$G_{gr}(w_m^2/w) = \frac{(C_D + C_{ox})^2 w_m^2}{G_{gr}(w)} \qquad \otimes$$

We can note that setting $\omega=\omega_m$ in the above relationship returns our earlier expression that $G_{gr}(w_m) = w_m(C_D + C_{ox})$.

Differentiating $\otimes$ across w.r.t $\omega$ and setting $\omega=\omega_m$ immediately gives us the requirement that $G_{gr}''(w_m) = 0$. Physically to ensure that $G_{gr}(w)$ has derivatives of all orders at $\omega = \omega_m$ we expect that all derivatives of $G_{gr}(w)$ be zero at $\omega=\omega_m$. Hence $G_{gr}(w)$ , though not constant, does not have a Taylor expansion about $\omega=\omega_m$ and belongs to a large family of so called "flat functions". When $G_{gr}(\omega)$

has all derivatives  equal to zero at $\omega = \omega_m$  and $G_{gr}(\omega)$ has the required symmetry that  $G_{gr}(\omega_m{}^2/\omega)=$ $(C_D+C_{ox})^2$ $\omega_m{}^2/G_{gr}(\omega)$, then $f_1$ & $f_2$ will exhibit graphical symmetry when plotted against Log($\omega$) and will also have the same local maxima at $\omega=\omega_m$ as required.

The required mathematical symmetry in $G_{gr}(w)$ also finds an application in accurately determining the value of $C_{ox}$.

From the circuit equations for $G(\omega)$ & $C(\omega)$ it follows that :

$G_{gr}(\omega)= G(\omega)$ $(C_{ox}+C_D)/(C_{ox}-C(\omega))$

If we have experimentally measured values for $G(\omega)$ and $C(\omega)$ and have estimated the values of the constants $C_D$ and $C_{ox}$, we can then plot out a graph of $G_{gr}(\omega)$ against $\omega$. Call this graph "$G_{gr}$ measured", this graph is sensitive to the value of $C_{ox}$ chosen.

But we now also know that $G_{gr}(\omega)$ has the mathematical symmetry that

$G_{gr}(\omega_m{}^2/\omega) = (C_D+C_{ox})^2$ $\omega_m{}^2$ $/G_{gr}(\omega)$

where $\omega_m$ can be read from our graph of $G(\omega)/\omega$ (we know that it is the frequency at which the graph of $f_1(\omega)$ has a maximum).

Consequently the symmetry of $G_{gr}(\omega)$ produces a second "companion" graph of "$G_{gr}$ measured", which we might call "$G_{gr}$ from symmetry".  From the earlier arguments these two graphs should be co-incident over a range of w and be flat at $\omega=\omega_m$ with the value of $G_{gr}$ being $\omega_m(C_D+C_{ox})$ at $\omega=\omega_m$. By varying $C_{ox}$ over an appropriate narrow range and plotting out the measured and companion graphs these requirements can be achieved and an accurate value for $C_{ox}$ obtained. This technique has been used in the main body of the thesis.

For the special case of $G_{gr}(\omega)$ having  a constant value the results in this appendix can be obtained using the Kramers-Kronig relations.

For a linear causal time-invariant system which in the frequency domain is represented by  $r(\omega)= g(\omega)$ $i(\omega)$ ( $i(\omega)$ being the input and $r(\omega)$ being the output response). Then the real and imaginary parts of the measured quantity $g(\omega)= g_R(\omega)+ i\, g_I(\omega)$ are related by :

$$g_R(w) = -\frac{2}{\pi}\mathcal{P}\int_0^\infty \frac{x\, g_{I(x)}}{x^2 - w^2}dx$$

$$g_I(w) = \frac{2\,w}{\pi}\mathcal{P}\int_0^\infty \frac{g_{R(x)}}{x^2 - w^2}dx$$

Whether or not these relationships will hold for our equivalent circuit depends on the form of $G_{gr}(\omega)$. If $G_{gr}(\omega)$ is a constant  and taking  $g_R(w) = \frac{G(w)}{w^2}$  & $g_I(w) = \frac{C(w)-C_{ox}}{w}$

then they will hold.

So for example this gives:

$$\frac{G(w)}{w^2} = \frac{-2}{\pi} \mathcal{P} \int_0^\infty \left(\frac{x}{x^2 - w^2}\right)\left(\frac{C(x) - C_{ox}}{x}\right) dx$$

And since $\mathcal{P} \int_0^\infty \frac{1}{x^2 - w^2} dx = 0$ we again get that our $f_1(\omega)$ and $f_2(\omega)$ graphs will cross when

$$-w \frac{dC(w)}{dw} = \frac{G(w)}{w} = \frac{-2\,w}{\pi} \mathcal{P} \int_0^\infty \frac{C(x)}{x^2 - w^2} dx$$

i.e.  $\frac{dC(w)}{dw} = \frac{2}{\pi}\mathcal{P} \int_0^\infty \frac{C(x)}{x^2 - w^2} dx$

(a condition on $C(\omega)$ alone).

This leads to our graphs crossing at $\omega = G_{gr}/(C_D + C_{ox})$ i.e. at $\omega = \omega m$ as before.

We also have $\frac{C(w) - C_{ox}}{w} = \frac{2\,w}{\pi}\mathcal{P} \int_0^\infty \frac{G(x)}{x^2(x^2 - w^2)} dx$

So that $C(w) - C_{ox} = \frac{2w^2}{\pi}\mathcal{P} \int_0^\infty \frac{1}{x^2}\frac{G(x)}{(x^2 - w^2)} dx$.

Differentiating across w.r.t. $\omega$ and calculating $w\frac{dC(w)}{dw}$ quickly gives

$$f_1(w) - f_2(w) = \frac{w\,w_m\,C_{ox}^2\,(w - w_m)^2}{(C_D + C_{ox})(w^2 + w_m^2)^2}$$

This explicitly shows the relationship between our two graphs $f_1(\omega)$ and $f_2(\omega)$ for a constant $G_{gr}$. Also note that $f_1(\omega) = f_2(\omega)$ for $\omega = \omega_m$

For non-constant $G_{gr}$'s the Kramers-Kronig relations generally will not hold.