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Data transmission at 1300 nm using optical interposer comprising hybrid integrated silicon waveguide and dilute nitride electroabsorption modulator

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Abstract: High speed back-to-back transmission of NRZ data at 12.5 Gbit/s was achieved over a repeaterless optical network without the use of forward error correction or optical clock recovery using a hybrid integrated silicon photonics optical interconnect. The interconnect comprises an electroabsorption modulator based on dilute nitride multiple quantum well material on GaAs substrate optically coupled to large core silicon waveguide using passive alignment and flip-chip bonding.

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1. Introduction

Demand for bandwidth intensive data and video streaming services is increasing, calling for continuous development and deployment of new optical interconnect technology in data centres [1]. To this end, the use of large core silicon (Si) waveguide technology, i.e. rib-waveguides [2], and active III-V photonic devices has gained popularity for hybrid integration. The main advantages associated with using 3 µm or 12 µm thick silicon-on-insulator (SOI) waveguides are related to their insensitivity to polarization, dimensional variations, surface roughness, reduced nonlinearity, and the excellent mode match with I/O connectors and III-V active waveguides. On the other hand, thick Si waveguides cannot be used to provide fast enough modulation in Si. Therefore, this platform requires the integration of either directly modulated lasers or electroabsorption modulators (EAM) [3]. For example, this heterogeneous platform has been used recently to demonstrate a 400 Gbps transceiver based on the hybrid integration of directly modulated vertical-cavity surface emitting lasers (VCSEL) and photodiode arrays operating at 1300 nm [4]. On the other hand, the deployment of active modulation with EAM has been largely limited to the 1.5 µm window and InP technology.

Here we demonstrate an optical interconnect platform consisting of hybrid integrated thick Si waveguide technology and EAMs based on dilute nitride multiple quantum well (MQW) materials on a GaAs substrate, i.e. GaInNAs/GaAs. The transmission module was designed for short distance data communications links, and incorporated EAMs with large core SOI waveguides. Dilute nitride QWs are known to provide excellent absorption properties at 1300 nm [5], thus potentially enabling the fabrication of ultracompact EAMs with high modulation

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speeds. Moreover, these materials have an advantage over InGaAsP, or AlInGaAs alloys grown on InP due to a very large conduction band offset [6], leading to high temperature performance with potential for un-cooled operation [7]. These features are very important in particular for increasing the integration density and mitigating the need for active cooling at high data rates. Furthermore, the GaInNAs/GaAs platform has recently been used to demonstrate monolithic integration of 1.3 μm laser diodes on Ge substrate, opening a very promising approach for full-scale monolithic integration with Si/SiGe technology [8].

Ultimately, from the large-scale fabrication point of view, GaAs technology is compatible with microelectronics fabrication and also benefits from the availability of larger substrates at lower cost (i.e. 6" for GaAs compared to 4" for InP). In addition, GaAs is a harder substrate than InP and is based on a more mature technology, which is ideally suited for larger scale manufacturing [3].

This paper presents results on recent work towards the development of a hybrid integrated transmitter comprising a VCSEL, large core SOI waveguides and an EAM. This paper focuses on the large core SOI waveguide and the EAM, with work on the VCSEL development having been reported elsewhere [9]. Details are presented on the development of an epitaxial structure for an EAM based on dilute nitride quantum wells. The recipe for processing the high speed EAM is given. The integration of fabricated EAM in Si interposer is described. DC and RF characterisation results show that the EAM was successfully fabricated and operates in agreement with how it was designed. Results from data transmission experiments show that the EAM integrated on Si interposer can be used to successfully transmit data at 10 Gbps and 12.5 Gbps with bit error rate (BER) below the 1×10^{-3} limit for forward error correction (FEC).

The structure of the paper is as follows: section 2 describes the design of the epitaxial material for the EAM; section 3 describes the design of the fabricated EAM; section 3.1 describes the hybrid integration of the fabricated EAM with the wide-waveguide SOI interposer; section 4 describes the DC characterisation of the EAM and finally section 5 describes the characterisation of the dynamic performance of the fabricated module in back-to-back (BtB) communication format at data rates of 10 Gbps and 12.5 Gbps.

Table 1. Epitaxy design for dilute nitride based electroabsorption modulator.

Material	**Thick** (*nm*)	**Doping** (cm^{-3})
p-GaAs	200	1×10^{19}
p-AlGaAs	1000	4×10^{17} - 4×10^{18}
GaAs	103	
GaAsN Barrier	10	
InGaAsN QWs	7	
GaAsN Barrier	10	
GaAs	103	
n-AlGaAs	700	3×10^{17}
n-GaAs	600	4×10^{18}
GaAs Substr.		

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2. Epitaxy design

The heterostructure design required modelling the bandgap of dilute nitride material alloys. This was done using a combination of 8-band $\mathbf{k} \cdot \mathbf{p}$ theory [10], which accounts for strain-induced bandgap changes in a quantum well structure, and the band anti-crossing (BAC) model which describes the variation in bandgap energy of the dilute nitride materials GaN_xAs_{1-x} [11] and $Ga_{1-y}In_yN_xAs_{1-x}$ [12], these models are known to be accurate when describing alloys containing up to 5% Nitrogen [13]. The band edge emission wavelength for $Ga_{0.7}In_{0.3}N_{0.02}As_{0.98}$ and $Ga_{0.7}In_{0.3}As$ quantum wells in bulk GaAs were simulated for different quantum well widths, and the results were compared with known measured values of the photoluminescent emission from the same materials [14]. The data, shown in Fig. 1 shows that there is good agreement between the values predicted by our bandgap model and the known measured values.

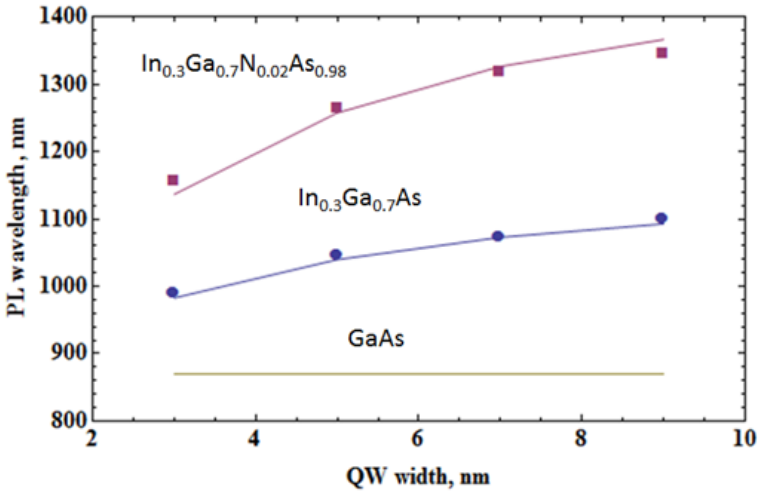


Fig. 1. Measured (dots) and simulated (solid lines) PL emission wavelength of single quantum wells versus quantum well width for $In_{0.3}Ga_{0.7}N_{0.02}As_{0.98}$, $In_{0.3}Ga_{0.7}As$ and GaAs. Measured data is taken from [14]. Good agreement between our model and the known measured data is observed.

Models for the electron and heavy hole effective masses in $Ga_{1-y}In_yN_xAs_{1-x}$ quantum wells were derived from [15] with the appropriate band parameters being taken from [16]. In the limit $y \to 0$, $x \to 1$ electron and heavy hole effective masses predicted by our $Ga_{1-y}In_yN_xAs_{1-x}$ model match that of the known electron and heavy hole effective masses in GaAs. A similar match is observed for InAs in the limit $y \to 1$, $x \to 1$ [17].

Extensive modelling of the quantum confined Stark effect (QCSE) for the quantum wells (QW) based on acceptable dilute nitride alloys was completed to provide a design appropriate for EAM operation near 1.3 µm [18]. The finalised epitaxy design is shown in Table 1.

The band structure of the design in Table 1 was approximated using a 1D Poisson solver known as SimWindows [19]. Results from simulations show that the valence band offset at the GaAs-QW interface is $\Delta E_v = 0.06$ eV, while the conduction band offset is $\Delta E_c = 0.26$ eV for our chosen InGaAsN alloy. The high value of conduction band offset ratio of $Q_c = 0.81$ in our structure is consistent with more advanced theoretical calculations [6] and agrees with reported measured values of the conduction band offset ratio for similar InGaAsN alloys [14]. Moreover, the layers are arranged in a manner that minimises photo-generated hole pile-up at the GaAs-QW interface [20].

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3. EAM design and fabrication

Wafers of the material in Table 1, from which the EAM was fabricated, were grown by molecular beam epitaxy [21]. The high speed EAM processing was completed using six lithography steps. The first step was to provide electrical isolation between the EAM and the adjacent transparent region. This was done by defining 300 nm of Si_3N_4 as a hard mark prior to using an Inductively Coupled Plasma (ICP) based BCl_3/Ar etch to remove the highly doped p-contact layers. After removing the remaining hard mask, a further 700 nm of Si_3N_4 was deposited and defined as a hard mask for the waveguide and large area contact pedestals. Again a BCl_3/Ar ICP etch was used to define a deep waveguide, as this etch went through the quantum wells into the n-doped contact region ($\approx 2.7\,\mu m$). After cleaning the surface, a silicon dioxide layer was deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) to passivate the side walls to minimise dark current.

The next two steps were used to deposit the contact metals. This was done for the p-metal by first using PMGI-SF5 and S1828 photoresist to form an undercut for lift off. The silicon dioxide on the surface of the ridge waveguide and pedestals was etched away using a dry etch and then after a surface clean, the p-metal was evaporated onto the wafer. An identical process was then used to evaporate n-metal onto the lower n-layers. The metals were then annealed to minimise the contact resistance, see [21] for details.

The next step was used to isolate the contact pillars from the remainder of the device. A thick photoresist SPR 220-4.5 was used as a mask for a 3 µm deep ICP BCl_3/Ar etch that went through the n-contact layers; well into the undoped GaAs wafer.

The final steps were used to define the high speed metal contacts. This began with depositing thick BCB, which was first planarized using reflow and then defined using photoresist as a mask to only remain over the ridges and where the BCB was required to support the contact metal. Thus, no BCB remained over the large pedestals. The BCB was then etched back until the ridges were exposed. The contact metal was then evaporated connecting the contact pedestals with the p-metal on the devices. Finally, the wafer was thinned and diced into the final set of devices and bars as shown in Fig. 2.

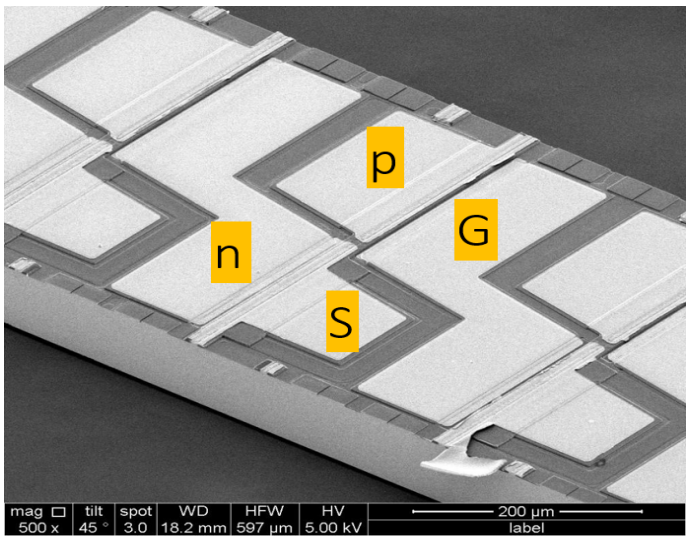


Fig. 2. SEM image of fabricated high speed EAM array with RF contacts for arranged in SG configuration. Also shown is the electrically isolated SOA section with DC contacts.

The EAMs were designed to be both high speed as well as compatible with flip-chip bonding.

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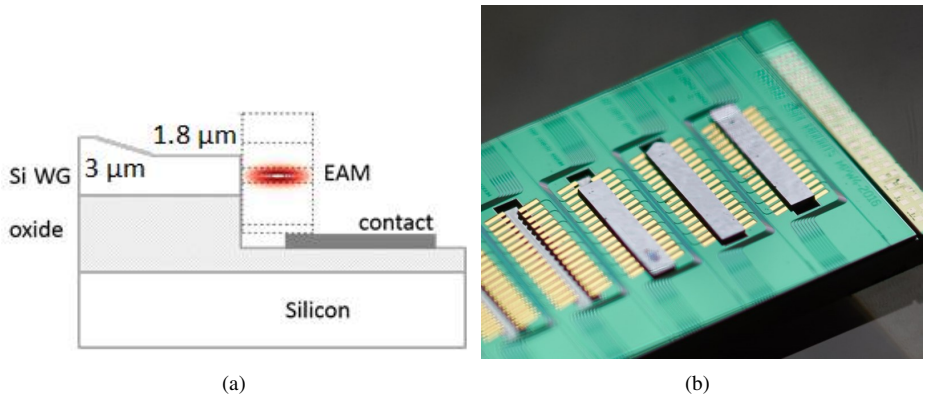
To accommodate both requirements, isolated pedestal high speed contacts were used [20]. For these contacts, the metal is placed on the top of the semiconductor material, where a robust metal contact can be made. Then, the large area contact is electrically isolated from the device by etching through the epitaxial layers into the undoped layers of the semiconductor wafer.

The length of the EAMs needed only be 200 µm for the required extinction ratio. However, this was too short for cleaving and handling. As a result, additional 200 µm sections were added adjacent to the EAMs, which would be operated to transparency using a small forward bias. These sections could also be operated as low gain semiconductor optical amplifiers (SOA) using a larger bias. A scanning electron microscopy (SEM) image of the completed EAM bar is shown in Fig. 2.

3.1. Incorporation of EAM bar into Si interposer

A Si interposer was designed to provide the full functionality of a multi channel high speed optical transmitter. This included a VCSEL array, reported in [9], EAM array and optical mode adapters to provide coupling between all components as well as to an output single mode fibre array.

The EAM waveguide was designed to align its optical mode with the mode of the large core Si waveguide after flip chip bonding [3]. Thus, the thickness of the EAM epitaxy and the total metal thickness on the host silicon platform as well as on the EAM were chosen to minimise coupling losses, see Fig. 3(a) for EAM-SOI coupling schematic.



(a) (b)

Fig. 3. a) Schematic illustrating optical coupling between silicon waveguide and EAM b) EAM flip chip bonded onto silicon interposer.

The large core Si waveguide was 1.8 µm thick, on top of a 3 µm oxide layer, which sits on the host Si substrate. The Si waveguides were 6 µm wide, thus, the EAM waveguide ridge width was increased to 6 µm to minimise mode mismatch. Simulations of the coupling efficiency between the Si optical mode and the EAM optical mode show that Si-EAM coupling was maximised when the EAM ridge width was 6 µm, with this EAM ridge width it was determined that the lateral alignment tolerance for the flip-chip bonding process was 0.7 µm. The lateral alignment needed to tolerate some misalignment due to the flip chip bonding based passive alignment of the EAM bar.

The epitaxial layers of the EAM and the contact metal thickness was designed to ensure that Si-EAM coupling was maximized along the vertical direction, thus providing a solution for vertical alignment. The final EAM bars were then flip chip bonded into the silicon interposer, as seen in Fig. 3(b).

A consequence of increasing the EAM ridge width to improve optical coupling and ease

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alignment tolerances during flip-chip bonding of EAMs on Si interposer was to increase the capacitance of the EAMs which negatively impacts their performance. The details of the measured EAM capacitances are discussed in section 4.

4. Characterisation of EAM

After cleaving the EAM bars, they were tested for DC and RF performance on a high speed photonics probe station designed to accommodate bare bars. Figure 4 shows the set up used to perform characterisation of the EAMs. The device temperature was controlled and stabilized by placing the device on a Peltier cell driven by a thermoelectric cooler (TEC) controller and monitoring the chip temperature through a thermistor. The EAM and SOA sections of the chip were biased separately using Keithley 2602 two channel sourcemeter. Light of known wavelength λ and power P_{in} was coupled to the EAM section using lensed optical fibre. Light exiting the device was captured using lensed optical fibre and coupled to an optical power meter (PM).

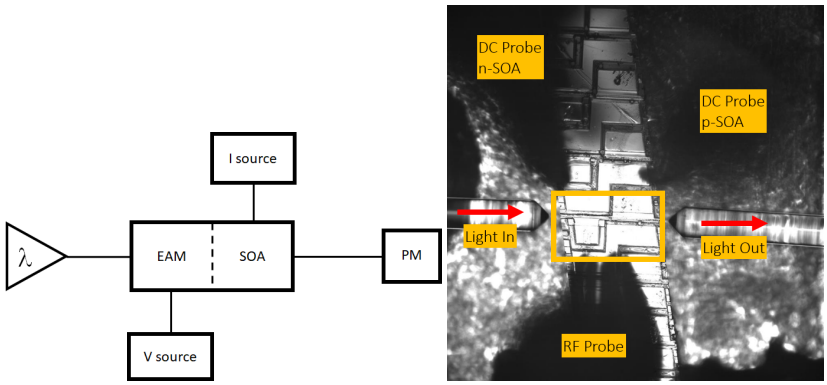


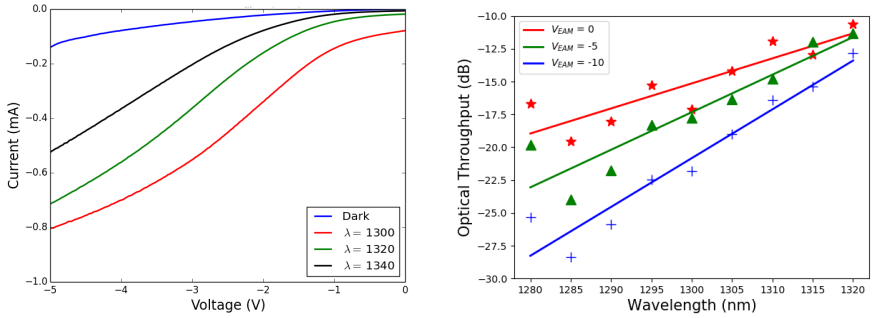
Fig. 4. a) Schematic of set up used to characterise fabricated EAMs. b) Microscope image of device under test. Device is 400 µm long.

To confirm absorption based on the QCSE, the EAM QWs were illuminated with light at different wavelengths and optical power of $P_{in} = 9$ dBm. Light from the laser was coupled to the EAM using a lensed fibre, see Fig. 4(b). Once coupling was optimised the photocurrent generated in the QWs was measured as the reverse bias across the EAM was increased. Figure 5(a) shows the measured photocurrent for a typical fabricated EAM. At reverse bias of -3 V and $\lambda = 1300$ nm the generated photocurrent of 0.7 mA is much greater than the observed dark current of 0.1 mA. The generated photocurrent also decreases as the wavelength increases. This confirms that QCSE is taking place inside the QWs since the absorption is decreasing as you move away from the material bandedge.

The optical transmission through the EAM was measured as a function of input wavelength and reverse bias while the SOA section was held at 0 mA. Data in Fig. 5(b) shows that optical throughput at $\lambda = 1300$ nm can be substantially altered by applying a reverse bias. The data in Fig. 5(b) provides further evidence for strong QCSE taking place inside EAM. Figure 5(b) shows that the EAM should be operated at wavelengths around 1300 nm, where there is extinction ratio (ER) of 7.5 dB for applied reverse bias of 10 V. The observed 10 dB optical insertion loss seen in Fig. 5(b) is due to sub-optimal coupling between the lensed fibre and the EAM during chip level tests of the EAM array, see Fig. 4(b). It was not possible to improve fibre-EAM coupling efficiency during the chip level test because the EAM waveguides were tilted at an angle of 10° relative to the facet. The EAM waveguide was tilted to ensure reduced optical reflections when

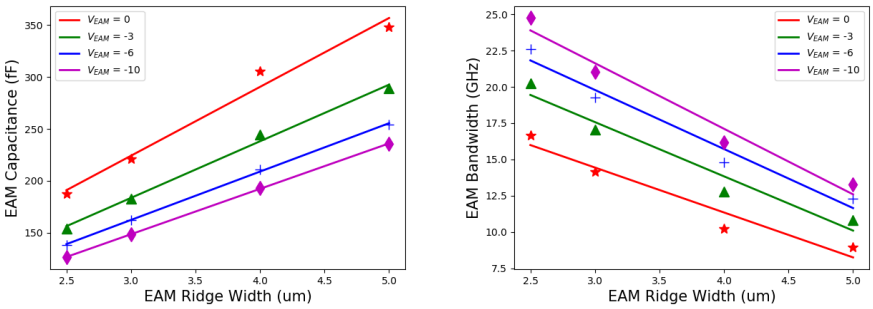
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the EAM array was hybrid integrated on the SOI interposer.



(a) (b)

Fig. 5. a) Measured photocurrent generated in the EAM epitaxial structure while QWs were illuminated by light with different wavelengths. b) Optical power transmitted through EAM at different EAM reverse bias. ER of 7.5 dB possible at 1300 nm at -10 V.



(a) (b)

Fig. 6. a) EAM capacitance as a function of waveguide width for 200 µm long EAMs. b) EAM bandwidth estimated from the measured EAM capacitance.

The equivalent circuit of the EAMs was extracted from S_{11} reflection measurements made on the devices using a vector network analyser (VNA). The pedestal bond pads were found to have a capacitance of 38 fF, while the EAMs were found to have length dependent capacitances as high as 400 fF. A series of test bars were also characterised that included EAMs with widths varying from 2 µm to 5 µm. The results, shown in Fig. 6(a), demonstrate that the EAM capacitance is significantly reduced by narrowing the waveguide width.

Assuming that the 3dB bandwidth of the EAM is given by $f_{3dB} = (2\pi RC)^{-1}$, where R is the device impedance and C its capacitance, the data in Fig. 6(a) shows that a factor of 2 reduction in ridge width would give a factor of 2 enhancement in 3dB bandwidth. The dependence of EAM bandwidth on EAM ridge width is confirmed by calculations made using the measured EAM capacitance data. In Fig. 6(b) it can be seen that bandwidth is doubled when ridge-width is halved. From the data in Fig. 6(b) it can be estimated that the bandwidth of the EAM in the fabricated transmission module, which has EAMs of ridge-width 6 µm to maximise optical coupling, is 7.3 GHz when a reverse bias of -4.5 V is applied to the EAM.

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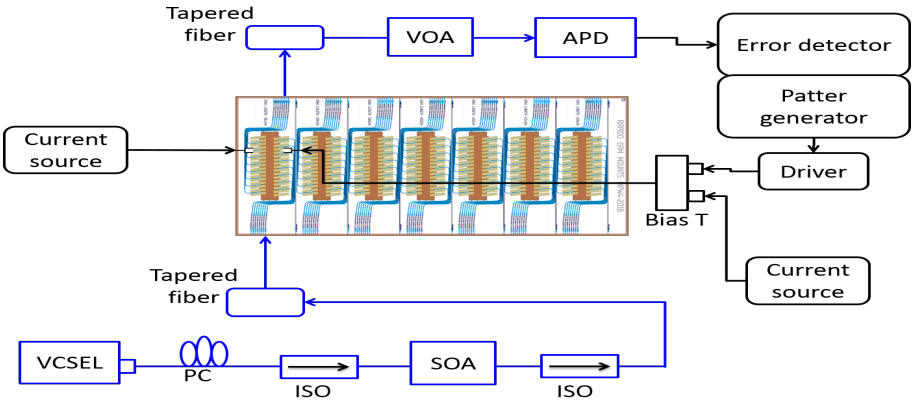


Fig. 7. Experimental configuration of high speed transmission testing, with EAM bar flip chip mounted inside Si interposer.

5. Dynamic performance of packaged device

Dynamic performance of the EAM was characterised by modulating it with NRZ signal and a PRBS sequence of length $2^{31} - 1$, and measuring bit error rate (BER) of transmitted data back-to-back (BtB) at data rate of 10 Gbps. It was also possible to demonstrate BtB data transmission at 12.5 Gbps. In the transmission experiment EAM temperature was maintained at 28 $^{\circ}C$, current in SOA section was 30 mA, EAM section was reverse biased to −4.5 V. Optical input power to the EAM during this measurement was supplied by VCSEL operating at $\lambda = 1311$ nm with $P_{VCSEL} = -38$ dBm. Optical power from VCSEL was amplified to 6.5 dBm and coupled into Si interposer device which contained the EAM.

The set-up used to perform BER characterisation is shown in Fig. 7. It is a repeaterless system configuration, as there is no source of optical amplification after transmission through the EAM. Data was generated using pulse-pattern generator (PPG) and an RF amplifier with peak-to-peak voltage set to $V_{pp} = 7.5$ V in order to exploit the EAM dynamic ER of 5 dB. The RF signal was fed to the EAM section using a bias-tee, enabling DC biasing and RF modulation simultaneously.

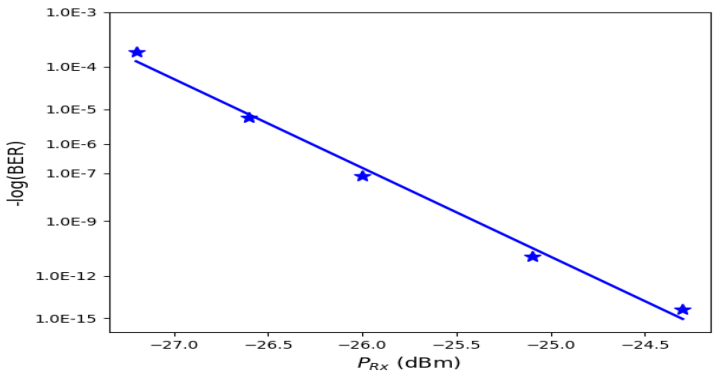
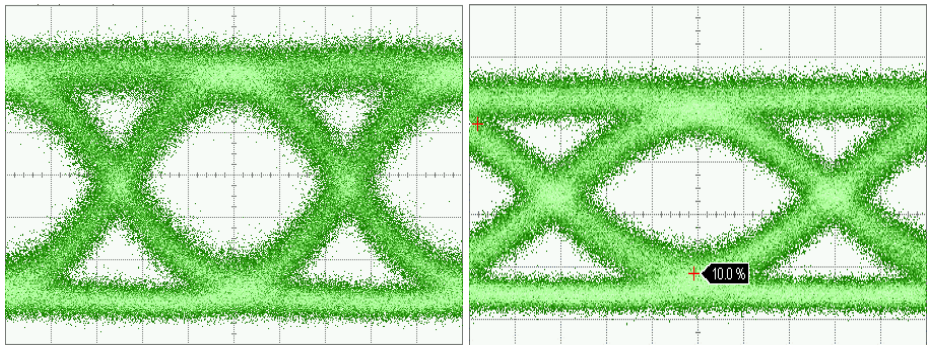


Fig. 8. Measured BER of the hybrid integrated EAM. Data rate is 10 Gbps. Input power to EAM is 6.5 dBm. PRBS length is 10^{31}. Vpp across EAM is 7.5 V.

The transmitted optical signal was connected to in-line power monitor with integrated variable optical attenuator (VOA) which enabled the power at the receiver (P_{Rx}) to be recorded; The

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signal was connected to an avalanche photodetector (APD). Power at the receiver is limited by available transmitter power, since the link is non-amplified. BER was measured using error detector (ED). No clock recovery was used, and both the sampling oscilloscope and ED were triggered by the same clock used by the PPG from the RF Synthesiser.



(a) 10 Gbps BtB eye diagram. Time scale is 20 ps/div, volt scale is 14 mV/div.

(b) 12.5 Gbps BtB eye diagram. Time scale is 13.1 ps/div, volt scale is 18.9 mV/div.

Fig. 9. BtB eye diagrams showing transmitted NRZ data with PRBS length $2^{31} - 1$

Initially the data rate was set at 10 Gbps. The BER against received power (P_{Rx}) is shown in Fig. 8. In BtB format BER = 5×10^{-15} for $P_{Rx} = -24.3$ dBm. Receiver sensitivity at BER = 1×10^{-9} level is approximately -25.5 dBm. BER measurement shows that the EAM integrated on the Si interposer is capable of transmitting data with BER below the FEC limit. The BtB eye diagram is shown in Fig. 9(a). At 10 Gbps the eye amplitude is 78.6 mV, and the signal to noise ratio (SNR) is 9.18 dB.

The experiment was repeated with a data rate of 12.5 Gbps. Figure. 9(b) shows the 12.5 Gbps eye diagram generated by the system. At 12.5 Gbps the eye amplitude is 61.6 mV, and the SNR is 6.03 dB. When the transmitted data was connected to the error detector it was found that the minimum achievable BER was 9×10^{-4} for $P_{Rx} = -22$ dBm which is below the FEC limit for data transmission.

6. Conclusion

Details were presented on the development of an epitaxial structure for an EAM based on dilute nitride quantum wells grown on GaAs substrate. The recipe for processing the high speed EAM was given. The integration of fabricated EAM in Si interposer was described. Dilute nitride EAMs grown on GaAs substrates were passively aligned to Si photonics transmission module using flip chip bonding. Measurements of photocurrent in the EAM structure and optical transmission through the fabricated EAM show that QCSE is taking place inside the MQW structure of the device and that ER = 7.5 dB is possible around the design wavelength of 1300 nm. RF characterisation data shows that the devices were limited in speed due to the parasitic capacitance of the large waveguide width EAMs. The bandwidth of the devices can be scaled up to much higher data rates by narrowing the waveguides of the EAMs. Results from data BtB transmission experiments with the EAM integrated on Si interposer show that the device can be used to successfully transmit data at 10 Gbps and 12.5 Gbps with BER below the 1×10^{-3} limit for FEC. The results obtained as part of this work indicate the potential for future development of the dilute nitride-on-GaAs Si photonics platform for optical interconnect technology.

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