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An investigation of capacitance-voltage hysteresis in metal/high-k/$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors

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An investigation of capacitance-voltage hysteresis in metal/high-*k*/$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors

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In this work, we present the results of an investigation into charge trapping in metal/high-*k*/$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors (MOS capacitors), which is analysed using the hysteresis exhibited in the capacitance-voltage (C-V) response. The availability of both *n* and *p* doped $In_{0.53}Ga_{0.47}As$ epitaxial layers allows the investigation of both hole and electron trapping in the bulk of HfO_2 and Al_2O_3 films formed using atomic layer deposition (ALD). The HfO_2/$In_{0.53}Ga_{0.47}As$ and Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS capacitors exhibit an almost reversible trapping behaviour, where the density of trapped charge is of a similar level to high-*k*/$In_{0.53}Ga_{0.47}As$ interface state density, for both electrons and holes in the HfO_2 and Al_2O_3 films. The experimental results demonstrate that the magnitude of the C-V hysteresis increases significantly for samples which have a native oxide layer present between the $In_{0.53}Ga_{0.47}As$ surface and the high-*k* oxide, suggesting that the charge trapping responsible for the C-V hysteresis is taking place primarily in the interfacial oxide transition layer between the $In_{0.53}Ga_{0.47}As$ and the ALD deposited oxide. Analysis of samples with a range of oxide thickness values also demonstrates that the magnitude of the C-V hysteresis window increases linearly with the increasing oxide thickness, and the corresponding trapped charge density is not a function of the oxide thickness, providing further evidence that the charge trapping is predominantly localised as a line charge and taking place primarily in the interfacial oxide transition layer located between the $In_{0.53}Ga_{0.47}As$ and the high-*k* oxide. © *2013 AIP Publishing LLC*.
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I. INTRODUCTION

As the minimum feature size of silicon based Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) reaches the limits of dimensional scaling, there is a concerted research effort directed towards the use of alternative high mobility channel materials (e.g., Ge and III-V materials) and high dielectric constant (high-*k*) gate oxides in future MOSFETs.[1–6] The motivation for using high mobility channel materials and high-*k* gate oxides is for lower leakage, lower power consumption, and higher speed of operation for minimum channel lengths below 22 nm. However, there are a range of challenges associated with the integration of high mobility compound semiconductor channels into a MOSFET process, which include the integration of the high mobility materials onto a large area silicon platform, forming high-*k* gate oxide layers on the III-V substrate, and finding a suitable *p* channel device when using III-V materials for both the *p* and *n* channel MOSFET. Due to the combination of a high electron mobility (~14 000 cm^2/V s at low doping levels), suitable energy gap (~0.75 eV) and the fact that it can be grown lattice matched in InP, there has been a considerable focus of research attention on InGaAs with a 53% In concentration (i.e., $In_{0.53}Ga_{0.47}As$). The electrically active interface defects between the high-*k* gate oxide and the $In_{0.53}Ga_{0.47}As$ surface,[7–16] and fixed charges within the high-*k* oxide,[15–17] have been studied in some detail in the literature. Charge trapping states can also be located in the transition region between the high-*k* oxide and $In_{0.53}Ga_{0.47}As$ surface and are often referred to a "slow states" or "border traps". These trapping sites have been examined based on the dispersion they cause in the capacitance with ac signal frequency for $In_{0.53}Ga_{0.47}$ As MOS structures biased in accumulation.[18–21] However, this dispersion can also include fast interface states aligned with energy levels in the $In_{0.53}Ga_{0.47}As$ conduction band.[9,10,22] In addition to causing frequency dispersion in the measured capacitance, charge trapping sites located in the oxide can be manifest as hysteresis in the C-V response. The issue of C-V hysteresis in the $In_{0.53}Ga_{0.47}As$ MOS system has received only a limited amount of research attention to date.[23,24] The issue of C-V hysteresis is important from a technological perspective as it represents a physical process that results in device instability, and in addition, the level of charge trapping can be comparable to, or greater than, the effect of interface states for the $In_{0.53}Ga_{0.47}As$ MOS system.[23] From a scientific perspective, the study of C-V hysteresis is of interest as it presents a method to analyse and quantify the density of charge trapping states in high-*k* oxides on III-V surfaces.

The principal aim of this work is to investigate C-V hysteresis in the high-*k*/$In_{0.53}Ga_{0.47}As$ MOS system for different metal gate electrodes and varying experimental bias conditions in order to quantify the level of electron and hole trapping, and to gain a more complete understanding of the primary location of the charge trapping sites. The experimental results also provide insight into the approach that is required to reduce the density of charge trapping sites

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responsible for the C-V hysteresis in the $In_{0.53}Ga_{0.47}As$ MOS system.

II. EXPERIMENTAL DETAILS

The samples used in this work were heavily *n*-doped (S at $\sim 2 \times 10^{18}$ cm^{-3}) and heavily *p*-doped (Zn at $\sim 2 \times 10^{18}$ cm^{-3}) InP(100) substrates with 2 μm *n*-type (S at $\sim 4 \times 10^{17}$ cm^{-3}) and *p*-type (Zn at $\sim 4 \times 10^{17}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ epitaxial layers, respectively, grown by metal organic vapour phase epitaxy (MOVPE). The $In_{0.53}Ga_{0.47}As$ surfaces were initially degreased by sequentially rinsing for 1 min each in acetone, methanol, and isopropanol. Before the high-*k* oxide deposition, the samples were immersed in $(NH_4)_2S$ solutions (10% in deionized H_2O) for 20 min at room temperature ($\sim$295 K). The 10% $(NH_4)_2S$ passivation approach for 20 min and room temperature was found to be the optimum to suppress the formation of $In_{0.53}Ga_{0.47}As$ native oxides and to reduce the high-*k*/$In_{0.53}Ga_{0.47}As$ interface state density as reported in Ref. 25. Samples were then introduced to the atomic layer deposition (ALD) chamber load lock (base pressure of less than 2×10^{-5} mbar) after the removal from the 10% $(NH_4)_2S$ surface passivation solution. The transfer time from the aqueous $(NH_4)_2S$ solution to the ALD chamber was kept to a minimum in order to minimise the formation of $In_{0.53}Ga_{0.47}As$ native oxides due to air exposure.

Either HfO_2 or Al_2O_3 were deposited on the $In_{0.53}Ga_{0.47}As$ by ALD. The HfO_2 dielectric has a nominal thickness of 5 nm by ALD using $Hf[N(CH_3)C_2H_5]_4$ (TEMAH) and H_2O as precursors at 250 °C. The Al_2O_3 dielectric has a nominal thickness of 8 nm and was deposited by ALD at 300 °C using trimethylaluminum (TMA) $Al(CH_3)_3$ and H_2O. For the Al_2O_3 thickness series results presented in this work, the Al_2O_3 dielectric with nominal thicknesses of 5, 10, 15, 20 nm were deposited by ALD at 250 °C using the same aluminium precursor and H_2O. In this work, we examined samples with several metal gates representing low and high work functions, which included Al, Pt, Pd, and Ni/Au. Gate contacts were formed by electron beam evaporation and a lift-off process. Pt (115 nm) and Al (115 nm) were used as the two metal gates for HfO_2 (5 nm) samples, Al (160 nm) and Ni(70 nm)/Au(90 nm) were the two gates for Al_2O_3 (8 nm) samples, and Pd (160 nm) was the metal gate for the Al_2O_3 thickness series(5–20 nm). The full sample details are provided in Table I.

The C-V hysteresis measurements were recorded using a Cascade Microtech probe station (model Submmit 12971B) and an Agilent CV-enabled B1500A semiconductor device analyser. All the C-V hysteresis measurements were carried out at a high frequency of 1MHz and at room temperature (295 K) in order to minimise the contribution of high-*k*/$In_{0.53}Ga_{0.47}As$ interface states to the overall capacitance. Under these conditions, the primary effect of the interface states is to stretch out the measured high frequency C-V along the gate voltage axis.[26,27] All the reported C-V hysteresis responses were measured starting from inversion and sweeping towards the accumulation region, and subsequently sweeping back towards inversion. There was no hold time in accumulation. The terms "inversion" and "accumulation" used here are for simplicity of expression to represent the nominal regions of the C-V characteristic. To confirm surface inversion would require more analysis, but this is beyond the scope and intention of this work. The MOS capacitors under investigation were all driven beyond the flatband condition and towards accumulation region which allows charge to be accumulated at the $In_{0.53}Ga_{0.47}As$ surface. The C-V hysteresis (i.e., the gate voltage difference between the double-directional sweeps) is estimated at either the flat-band capacitance (C_{fb}) or half the maximum capacitance in accumulation ($C_{max}/2$). The level of charge trapping is quantified using the following equation:

$$Q_{trapped} = \frac{C_{ox} \times \Delta V}{q} (\mathrm{cm}^{-2}), \quad (1)$$

where $Q_{trapped}$ is the population of trapped charge in cm^{-2}, ΔV is the C-V hysteresis in V, C_{ox} is the oxide capacitance in F/cm^2 (proportional to the oxide *k*-value and inversely proportional to the oxide thickness), and *q* is the elementary charge in C. The value of $Q_{trapped}$ in Eq. (1) represents the equivalent charge density at the oxide/$In_{0.53}Ga_{0.47}As$ interface. Multiple sites with different capacitor areas were examined to ensure the C-V hysteresis results are representative of the sample behaviour. The effect of different oxide electric fields due to small variations in oxide thickness has been neglected. The C_{ox} values are based on oxide thickness values obtained from high-resolution cross-sectional transmission electron microscopy (HR-TEM), taking into account any interfacial oxide layers formed in the MOS structure. The following dielectric constant values were adopted, HfO_2 (21),[28] Al_2O_3 (8.6),[23] and the native oxide of $In_{0.53}Ga_{0.47}As$ (9).[29,30]

III. RESULTS AND DISCUSSIONS

Twenty C-V hysteresis sweeps for *n*-type and *p*-type Pt/HfO_2(5 nm)/$In_{0.53}Ga_{0.47}As$ MOS capacitors are shown in Figures 1(a) and 1(b), respectively. The flat-band voltage (V_{fb}) difference estimated from the first C-V hysteresis

TABLE I. Sample details.

Sample	Gate (thickness)	Oxide (thickness)	ALD precursors	ALD temperatures
HfO_2/(n and p)$In_{0.53}Ga_{0.47}As$ sample series	Pt (115 nm) Al (115 nm)	HfO_2 (5 nm) HfO_2 (5 nm)	TEMAH and H_2O	250 °C 250 °C
Al_2O_3/(n and p)$In_{0.53}Ga_{0.47}As$ sample series	Ni/Au(70 nm/90nm) Al (160 nm)	Al_2O_3(8 nm) Al_2O_3(8 nm)	TMA and H_2O	300 °C 300 °C
Al_2O_3/(n and p)$In_{0.53}Ga_{0.47}As$ oxide thickness series	Pd (160 nm)	Al_2O_3 (5, 10, 15, 20 nm)	TMA and H_2O	250 °C

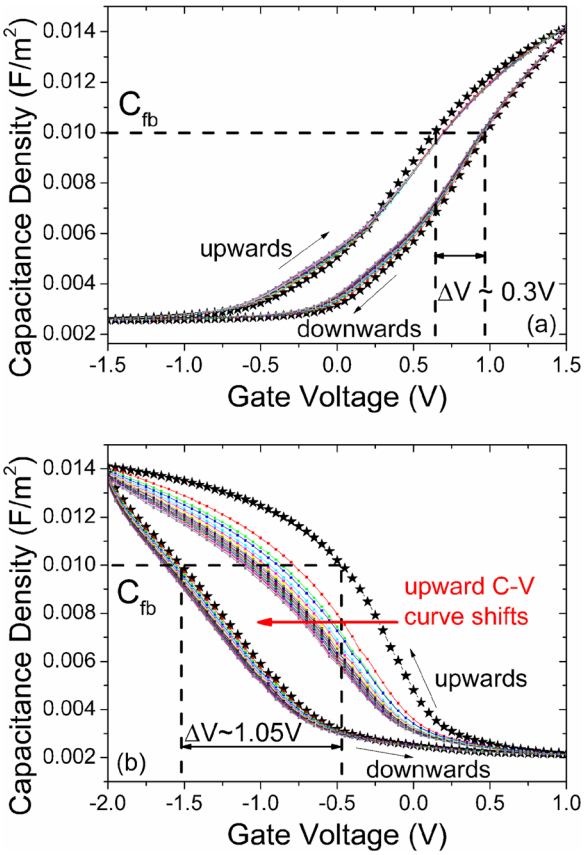


FIG. 1. Twenty C-V hysteresis responses at 1 MHz and 295 K for (a) Pt/HfO_2(5 nm)/*n*-$In_{0.53}Ga_{0.47}As$/*n*-InP and (b) Pt/HfO_2(5 nm)/*p*-$In_{0.53}Ga_{0.47}As$/*p*-InP MOS capacitors. A progressive gate voltage shift occurring with subsequent C-V sweeps is evident in the upward sweep direction in (b). Note: the curve with black star symbols is the 1st C-V hysteresis sweep.

sweep, which is shown in black stars in Figure 1, corresponds to an electron trapping level of 4.7×10^{12} cm^{-2} for the *n*-type sample, and a hole trapping level of 1.6×10^{13} cm^{-2} for the *p*-type sample, assuming all the charge trapping is taking place at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface. The validity of this assumption will be explored later in the paper. The density calculations are based on an oxide capacitance value $C_{ox} = 2.5 \times 10^{-6}$ F/cm^2 taking into consideration the $HfO_2/In_{0.53}Ga_{0.47}As$ interface oxide thickness observed in the TEM micrographs which will be presented and discussed later. Both the electron and hole trapping levels are comparable to the estimated interface state density (D_{it}) using the approach described in Ref. 15, highlighting the importance of electron and hole trapping in the high-*k*/$In_{0.53}Ga_{0.47}As$ MOS system. Considering first the *n*-type $In_{0.53}Ga_{0.47}As$ sample in Figure 1(a), the repeated C-V hysteresis sweeps are almost overlapping the 1st C-V hysteresis in the upward sweep direction, where the MOS capacitor is measured from inversion to accumulation, indicating that the majority of charge trapping is a reversible process (or a temporary trapping behaviour). In the *p*-type $In_{0.53}Ga_{0.47}As$ sample (Figure 1(b)), there is a significant shift in V_{fb} between the 1st and 2nd C-V hysteresis sweeps, but subsequent sweeps show the same behaviour as the *n*-type sample, where the majority of the charge trapping is a reversible process. There is only a small non-reversible component referred to here as permanent charge trapping, which is manifested as a progressive shift in V_{fb} in the inversion to accumulation sweeps of the C-V responses, which is a positive V_{fb} shift for the *n*-type sample and a negative V_{fb} shift for the *p*-type sample. From Figure 1, it is clear that the progressive V_{fb} shift is more significant in the *p*-type sample, implying a larger portion of permanently trapped charges in the *p*-type sample compared to that in the *n*-type sample.

Figure 2 illustrates the effect of the maximum bias in accumulation on the level of C-V hysteresis. For these measurements, the same starting DC bias point in inversion is used, with an increasing maximum DC bias point in accumulation (V_{max}) for the Pt/HfO_2(5 nm)/*n*-$In_{0.53}Ga_{0.47}As$ (Figure 2(a)) and Pt/HfO_2(5 nm)/*p*-$In_{0.53}Ga_{0.47}As$ (Figure 2(b)) MOS capacitors. As shown in the insets of the figures, the C-V hysteresis window increases linearly with V_{max}. The C-V hysteresis is also found to increase with V_{max} for the Al_2O_3(8 nm)/$In_{0.53}Ga_{0.47}As$ MOS structures, but the level of increase is less than observed for the HfO_2 structures (results not shown). It has recently been demonstrated that SiO_2 doped HfO_2 (Ref. 31) and $ZrHfO_2$ thin films on silicon[32] exhibit a ferroelectric behaviour. The C-V results in Figures 2(a) and 2(b) obtained for the undoped HfO_2 are not consistent with a ferroelectric response, suggesting electron and hole trapping as the source of the C-V hysteresis. The origin of the linear increase of the C-V hysteresis window with the V_{max} is the subject of further studies.

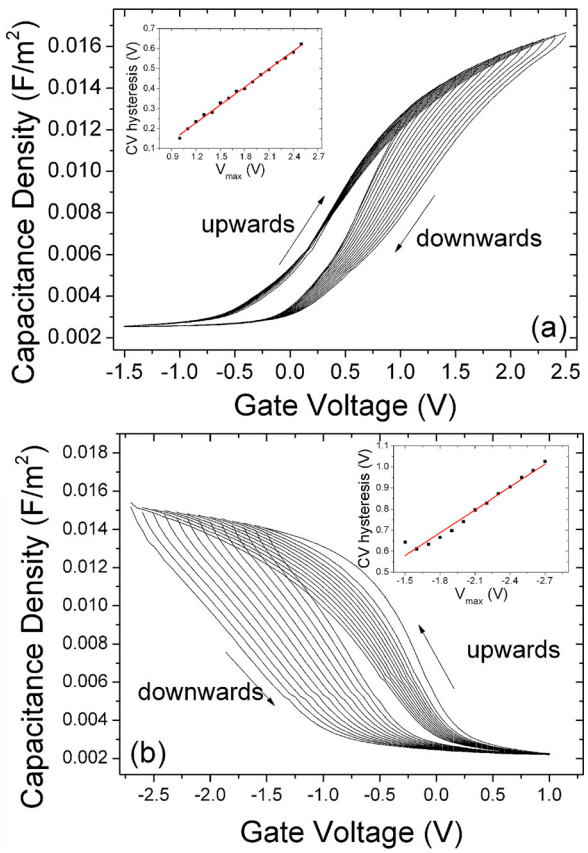


FIG. 2. C-V hysteresis at 1 MHz and 295 K for (a) Pt/HfO_2(5 nm)/*n*-$In_{0.53}Ga_{0.47}As$ and (b) Pt/HfO_2(5 nm)/*p*-$In_{0.53}Ga_{0.47}As$ MOS capacitors using the same start DC bias in inversion and increasing DC bias (V_{max}) in accumulation. Inset is the C-V hysteresis as a function of V_{max}.

From Figure 2, which has a range of maximum bias values in accumulation, it is possible to compare the level of charge trapping in the *n*- and *p*-type $In_{0.53}Ga_{0.47}As$ samples at the same maximum electric field across the oxide (i.e., the same $|V_{max}\text{-}V_{fb}|$). It is important to have the same $|V_{max}\text{-}V_{fb}|$ for the two samples so that same amount of majority carriers are accumulated at the $In_{0.53}Ga_{0.47}As$ surface which makes the comparison valid. For example, if $|V_{max}\text{-}V_{fb}|$ is taken as 1.4 V, the trapped charge density is 7.3×10^{12} cm^{-2} for the *n*-$In_{0.53}Ga_{0.47}As$ sample and 1.3×10^{13} cm^{-2} for the *p*-$In_{0.53}Ga_{0.47}As$ MOS sample. This indicates that there is a significantly lower level of charge trapping in the case of the *n*-type $In_{0.53}Ga_{0.47}As$ MOS capacitor than in the case of *p*-$In_{0.53}Ga_{0.47}As$. There are a range of possible factors which can contribute to the higher level of temporary charge trapping (i.e., C-V hysteresis) and permanent charge trapping in the *p*-$In_{0.53}Ga_{0.47}As$ MOS structures, which are illustrated schematically by the energy band diagrams shown in Figures 3(a) and 3(b) for the *n*-type and *p*-type samples, respectively. The possible reasons for a higher level of charge trapping in the *p*-type sample compared to the *n*-type sample are: (i) a higher density of border traps with energy levels aligned with the $In_{0.53}Ga_{0.47}As$ valance band edge than that aligned with the conduction band edge, (ii) the barrier height ΔE_v for the trapped holes to be removed from the border traps is larger than the barrier height ΔE_c for the trapped electrons.[33]

The study of the C-V hysteresis also included an examination of the impact of the metal gate based on low (i.e., aluminium) and high (i.e., platinum) work function metals, as detailed in Table I. Figure 4 shows the C-V hysteresis for the Pt/HfO_2(5 nm)/*n*-$In_{0.53}Ga_{0.47}As$ and Al/HfO_2(5 nm)/*n*-$In_{0.53}Ga_{0.47}As$ MOS capacitors. The Al gate sample is driven into strong accumulation as the measured capacitance is plateauing at 1.5 V, and the value of $|V_{max}\text{-}V_{fb}|$ is higher for the Al gate samples than the Pt gate sample. Under this condition, the C-V responses exhibit three features of importance. First, the maximum capacitance in accumulation for the Al gate sample is almost half of that obtained for the Pt gate sample. Second, the level of charge trapping determined from the C-V hysteresis at the flat-band capacitance for the Al gate sample, of $\sim 6.8 \times 10^{11}$ cm^{-2}, is significantly lower when

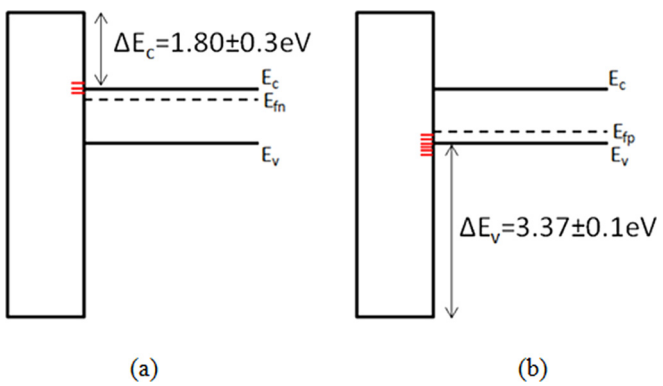


FIG. 3. Band diagrams for (a) HfO_2/*n*-$In_{0.53}Ga_{0.47}As$ and (b) HfO_2/*p*-$In_{0.53}Ga_{0.47}As$ structures.[33] The energy levels shown in red are the border trap energy levels which are aligned with the conduction band edge (E_c) for the *n*-type sample and aligned with the valance band edge (E_v) for the *p*-type sample.

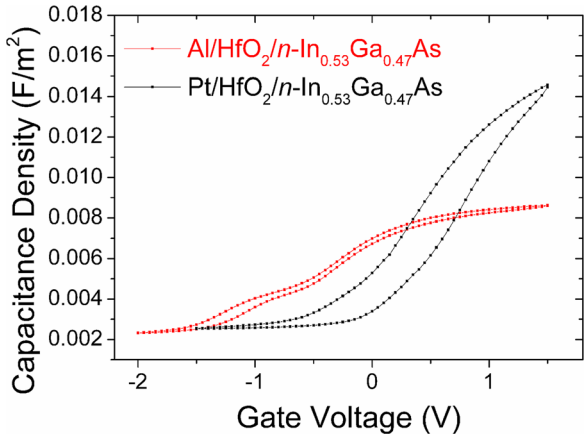


FIG. 4. C-V hysteresis at 1 MHz and 295 K for Pt/HfO_2(5 nm)/*n*-$In_{0.53}Ga_{0.47}As$ and Al/HfO_2(5 nm)/*n*-$In_{0.53}Ga_{0.47}As$ MOS capacitors. There is a significant reduction in the maximum capacitance for the Al gate sample in accumulation and a considerable reduction in $Q_{trapped}$ (C-V hysteresis) in comparison to the Pt gate sample.

compared to $\sim 4.7 \times 10^{12}$ cm^{-2} for the Pt gate sample. In addition, the reduced charge trapping for the Al gate sample occurs even with a higher value of $|V_{max}\text{-}V_{fb}|$. Finally, the samples exhibit a low level of frequency dispersion (<3.5%/decade) in the region corresponding to nominal accumulation ($V_g > 1.0$ V) (not shown). In addition, the capacitance in this bias region does not significantly change when reducing the temperature to −50 °C (not shown). These results suggest the samples exhibit genuine surface accumulation.[11]

Further insight into the differences between the Al and Pt gate HfO_2(5 nm)/*n*-$In_{0.53}Ga_{0.47}As$ MOS C-V responses can be obtained from the microstructure of the samples as indicated by TEM images for both samples, as shown in Figures 5(a)–5(d). The Pt gate sample exhibits an interface oxide of ~1 nm between HfO_2 and the $In_{0.53}Ga_{0.47}As$. Previous analysis has indicated that this layer is the native oxide of $In_{0.53}Ga_{0.47}As$ and predominantly comprised of a Ga oxide.[12] In Figure 4, the maximum capacitance of the Pt gate sample at +1.5 V is ~0.0146 F/m^2. The oxide capacitance associated with 5 nm of HfO_2 ($k = 21$) is $C_{ox} = 0.037$ F/m^2. Even if the Pt gate HfO_2/*n*-$In_{0.53}Ga_{0.47}As$ MOS sample is driven further into accumulation, it is clear that the experimental capacitance will not acquire the C_{ox} value associated with a 5 nm HfO_2 layer alone. This observation also points to a formation of interface oxide with a much lower *k*-value that is responsible for the reduction in C_{ox}. As observed from Figures 5(a) and 5(b), this interface oxide layer is present both in the areas under the Pt gate and in the areas outside the Pt gate. The same interfacial oxide is present for the Al gate sample in the area outside the Al gate (see Figure 5(d)). However, the TEM for the Al gate sample taken in the region where the Al gate is present shows that the electron-beam evaporated Al gate results in marked changes in the micro-structure of the HfO_2/$In_{0.53}Ga_{0.47}As$ gate stack. First, a layer of Al_2O_3 of ~5 nm in thickness is formed between the Al gate and HfO_2, adding an extra capacitance in series with the total capacitance of the MOS capacitor and thus reducing the maximum capacitance for the

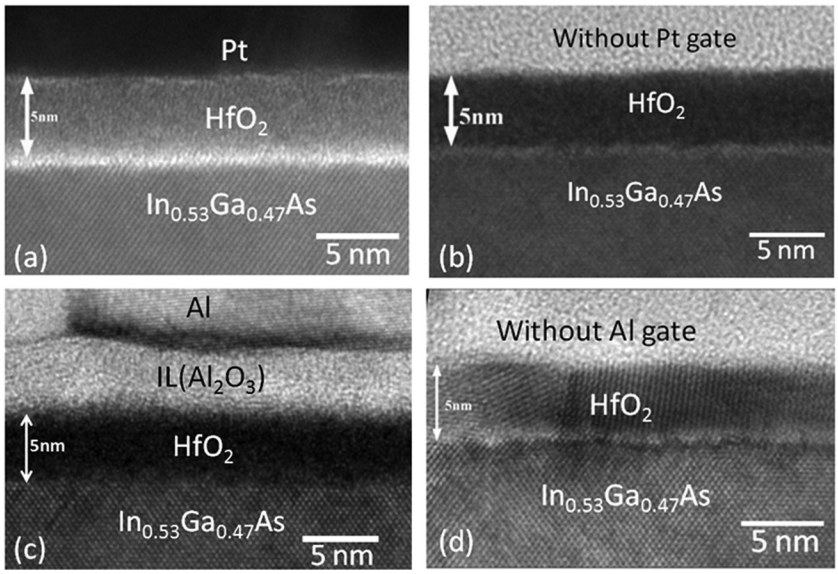


FIG. 5. TEM micrographs for Pt/HfO_2 (5 nm)/*n*-$In_{0.53}Ga_{0.47}As$ MOS capacitor in the area (a) under the Pt gate and (b) outside the Pt gate, and for Al/HfO_2 (5 nm)/*n*-$In_{0.53}Ga_{0.47}As$ MOS capacitor in the area (c) under the Al gate and (d) outside the Al gate. Note in (c) the thick interface layer (IL) formed between Al and HfO_2 and the removal of the HfO_2/$In_{0.53}Ga_{0.47}As$ interface oxide.

Al gate sample, as observed in Figure 4. It is noted that a similar Al/HfO_2 interface layer was also observed in Al/HfO_2/Ge MOS structures, as reported in Ref. 34. Second, the presence of the Al gate "scavenges" the $In_{0.53}Ga_{0.47}As$ interfacial oxide layer and the HfO_2/$In_{0.53}Ga_{0.47}As$ interface oxide is almost gone in the region under the Al gate. This scavenging effect is similar to the effect reported for HfO_2 on silicon MOS structures with a Ti gate,[35] but it is noted that for the samples presented in this work (Figure 5(c)) the scavenging on the interface oxide layer has occurred during a room temperature Al deposition without any subsequent thermal annealing. The removal of the native oxide interface layer also has a marked effect on the level of charge trapping, which is estimated from C-V hysteresis at the flat-band capacitance, and is approximately an order of magnitude lower for the Al gate sample than the Pt gate sample even though the Al gate sample is driven further into accumulation. This observation provides strong evidence that the charge trapping responsible for the observed C-V hysteresis is taking place predominantly at the interfacial transition layer between the high-*k* oxide and $In_{0.53}Ga_{0.47}As$, which can contain native oxides of Ga, In, and As substrate elements.[12]

Figure 6 illustrates the C-V hysteresis for Al_2O_3 (8 nm)/*n*-$In_{0.53}Ga_{0.47}As$ MOS capacitors using either Ni/Au or Al as metal gates. Due to the reported "self-cleaning" effect of the ALD process to form the Al_2O_3, removal of the interfacial oxide between the Al_2O_3 and $In_{0.53}Ga_{0.47}As$ is possible, with improved electrical performance as a result.[30,36–39] The charge trapping level estimated for Al_2O_3 (8 nm)/*n*-$In_{0.53}Ga_{0.47}As$ MOS capacitors with no Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface layer, using either high (Ni/Au) or low (Al) work function gates is of a level which is around one order of magnitude lower than the typical interface state density in high-*k*/$In_{0.53}Ga_{0.47}As$ MOS system. Table II summaries the charge trapping levels calculated from the C-V hysteresis at flat-band capacitance in Figures 4 and 6 for the case of samples with and without a native oxide interface transition layer between the high-*k* oxide and the $In_{0.53}Ga_{0.47}As$. This provides further evidence that the charge trapping phenomenon originates from the high-*k*/$In_{0.53}Ga_{0.47}As$ interfacial transition layer, indicating that engineering of the interface transition region is the key to reducing C-V hysteresis in metal/high-*k*/$In_{0.53}Ga_{0.47}As$ MOS systems. In addition, the maximum capacitance for Al/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS capacitors is slightly lower than the Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS capacitors. This is possibly due to the formation of a thin, self-limiting interface layer of Al_2O_3 formed between the Al gate and Al_2O_3, which is similar to what is observed in Al/HfO_2/*n*-$In_{0.53}Ga_{0.47}As$ MOS structure with a formation of Al_2O_3 between Al and HfO_2. The Al/Al_2O_3 interface layer increases the nominal high-*k* oxide thickness and thus reduces the oxide capacitance, further reducing the total measured capacitance in accumulation (C_{max}). As in the case of the C-V in Figure 4, the dependence of the capacitance on temperature and ac signal frequency at

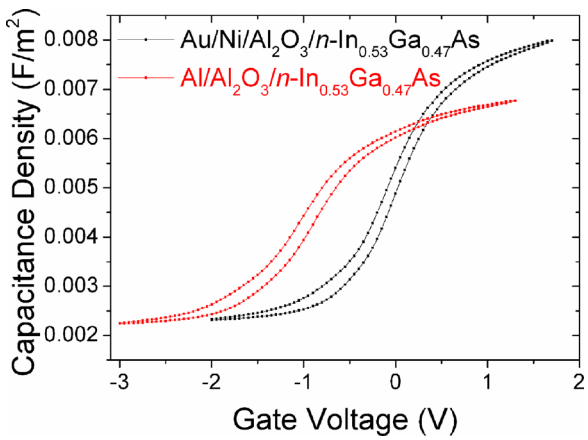


FIG. 6. C-V hysteresis at 1 MHz and 295 K for Au/Ni/Al_2O_3(8 nm)/*n*-$In_{0.53}Ga_{0.47}As$ and Al/Al_2O_3(8 nm)/*n*-$In_{0.53}Ga_{0.47}As$ MOS capacitors measured under the same electric field across the Al_2O_3. The charge trapping level of these two samples is relatively low, and comparable to the Al/HfO_2/*n*-$In_{0.53}Ga_{0.47}As$ sample where the interlayer oxide is scavenged by the Al gate. The difference between the two C_{max} values indicates an Al_2O_3 oxide thickness difference of no more than ~1.7 nm, probably a result of a reactive Al/Al_2O_3 interface compared to a non-reactive Ni/Al_2O_3 interface.

TABLE II. Summary of charge trapping for the C-V hysteresis shown in Figures 4 and 6.

Sample	$Q_{trapped}$	High-k/$In_{0.53}Ga_{0.47}As$ interfacial oxide layer	Comments
Pt/HfO_2/n-$In_{0.53}Ga_{0.47}As$	4.7×10^{12} cm^{-2}	Yes	~1 nm of HfO_2/$In_{0.53}Ga_{0.47}As$ IL
Al/HfO_2/n-$In_{0.53}Ga_{0.47}As$	6.8×10^{11} cm^{-2}	No	Al scavenges the oxygen from the $In_{0.53}Ga_{0.47}As$ surface
Al/Al_2O_3/n-$In_{0.53}Ga_{0.47}As$	8.9×10^{11} cm^{-2}	No	"Self-cleaning process" of ALD of Al_2O_3 removes the $In_{0.53}Ga_{0.47}As$ IL
Au/Ni/Al_2O_3/n-$In_{0.53}Ga_{0.47}As$	5.9×10^{11} cm^{-2}	No	"Self-cleaning process" of ALD of Al_2O_3 removes the $In_{0.53}Ga_{0.47}As$ IL

$V_g > 0V$ (not shown) indicates that genuine surface accumulation has been achieved.

To further examine the physical location and distribution of the trapped charge, C-V hysteresis was measured as a function of oxide thickness series for (a) n-type and (b) p-type Pd/Al_2O_3(5–20 nm)/$In_{0.53}Ga_{0.47}As$ MOS capacitors.[23] The use of a thickness series is useful in this respect, as for a trapped charge located in a plane within the oxide or at the oxide/semiconductor interface, the C-V hysteresis ΔV increases linearly with increasing oxide thickness. This linear relation can be expressed by the following equation:

$$\Delta V = \frac{qQ_{trapped} \times t_{ox}}{\varepsilon_0 k}, \quad (2)$$

where t_{ox} is the oxide thickness, ε_0 is the vacuum permittivity, and κ is the relative permittivity of the oxide. If the charge is distributed throughout the oxide, then ΔV is proportional to the square of the oxide thickness.[40]

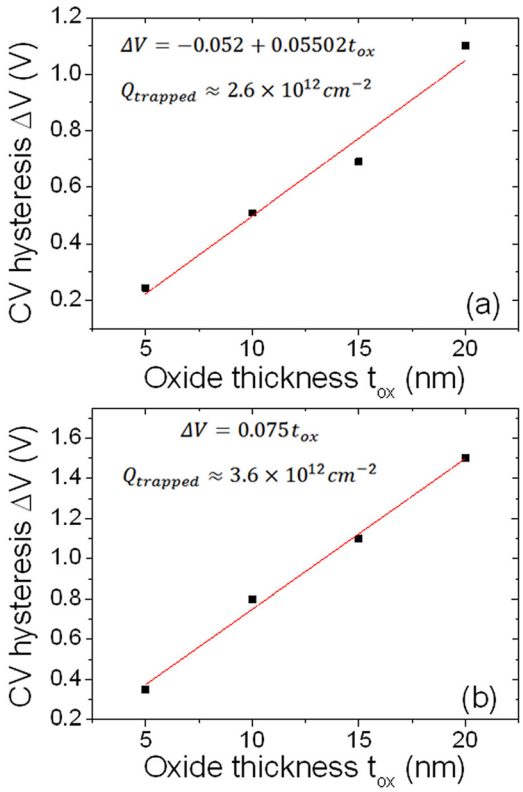


FIG. 7. C-V hysteresis at 1 MHz and 295 K as a function of oxide thickness (5, 10, 15, 20 nm) for (a) Pd/Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ and (b) Pd/Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ MOS capacitors. The maximum electric field across the oxide, as determined by the maximum voltage in accumulation, is kept at the same value for all thicknesses for both n-type and p-type sample.

The C-V hysteresis ΔV versus oxide thickness characteristics are shown in Figure 7 for (a) n-type, and (b) p-type, where ΔV is the estimated at $C_{max}/2$, and both plots clearly demonstrate a linear dependence of ΔV on the oxide thickness, supporting the earlier independent indications that the vast majority of the charge trapping occurs in a plane near the oxide/semiconductor interface and is not distributed through the oxide. The gradient of the plot of ΔV versus the oxide thickness is proportional to the trapped charge and yields values of 2.6×10^{12} cm^{-2} for the n-$In_{0.53}Ga_{0.47}As$ and 3.6×10^{12} cm^{-2} for the p-$In_{0.53}Ga_{0.47}As$ MOS structures.

IV. CONCLUSIONS

In this work, charge trapping behaviour in metal/high-k/$In_{0.53}Ga_{0.47}As$/InP MOS structures with either HfO_2 (5 nm) or Al_2O_3 (5 nm to 20 nm) ALD deposited high-k oxides was studied using C-V hysteresis measurements in combination with TEM microscopy analysis. The samples studied employed both high work function metal gates (Pt, Pd, Ni/Au) and a low work function metal gate (Al). The high-k/$In_{0.53}Ga_{0.47}As$ MOS system exhibits both electron and hole trapping, which is predominantly a reversible process. The temporary charge trapping levels, that can be as high as 10^{13} cm^{-2}, were recorded from the C-V hysteresis which is of the same magnitude as, or even greater than, the high-k/$In_{0.53}Ga_{0.47}As$ interface state density, indicating the importance of C-V hysteresis in the high-k/$In_{0.53}Ga_{0.47}As$ MOS system. C-V hysteresis is found to increase linearly with the increasing bias in accumulation, and the p-type $In_{0.53}Ga_{0.47}As$ MOS samples exhibit a larger C-V hysteresis and permanent charge trapping than their n-type $In_{0.53}Ga_{0.47}As$ counterparts.

Based on TEM analysis, it is observed that the use of an Al gate in HfO_2/$In_{0.53}Ga_{0.47}As$ samples results in the formation of an Al_2O_3 layer at the top Al/high-k oxide interface which reduces the maximum capacitance in accumulation. In addition, the top Al metal layer reduces the thickness of the native oxide transition layer present between the HfO_2 and the $In_{0.53}Ga_{0.47}As$ surface. The removal of the native oxide transition layer for the Al gate samples results in a marked reduction in the level of charge trapping and C-V hysteresis when compared to a Pt gate HfO_2/$In_{0.53}Ga_{0.47}As$ sample with ~1 nm of HfO_2/$In_{0.53}Ga_{0.47}As$ interface oxide, indicating that the charge trapping takes place mainly at the interfacial transition layer between the high-k oxide and $In_{0.53}Ga_{0.47}As$. In addition, Al/Al_2O_3/$In_{0.53}Ga_{0.47}As$ and Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS capacitors, which have no detectable interface oxide due to the reported "self-cleaning" effect of Al_2O_3 by ALD, have a relatively low level of charge

trapping. The C-V hysteresis voltage window (ΔV) increases linearly with the increasing high-k oxide thickness, with the corresponding trapped charge being independent of the oxide thickness, providing further evidence that the trapped charge is predominantly localised as a line charge (in units in cm^{-2}) at or near the high-k/$In_{0.53}Ga_{0.47}As$ interface. The results presented in this work identify the understanding and engineering of a native oxide interfacial transition layer between the high-k oxide and the $In_{0.53}Ga_{0.47}As$ surface, as central to reducing C-V hysteresis in the high-k/$In_{0.53}Ga_{0.47}As$ MOS systems.

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