

Title	Two-dimensional transition metal dichalcogenides as next generation semiconductor materials
Authors	Coleman, Emma M.
Publication date	2023
Original Citation	Coleman, E. M. 2023. Two-dimensional transition metal dichalcogenides as next generation semiconductor materials. PhD Thesis, University College Cork.
Type of publication	Doctoral thesis
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Download date	2026-09-23 00:05:27
Item downloaded from	https://hdl.handle.net/10468/15420

Two-Dimensional Transition Metal Dichalcogenides as Next Generation Semiconductor Materials

PhD Thesis

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UNIVERSITY COLLEGE CORK

FACULTY OF SCIENCE

DEPARTMENT OF CHEMISTRY

**Thesis submitted for the degree of
Doctor of Philosophy**

23 May 2023

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Abbreviations

2D 2 Dimensional

2P 2 Point Hall Measurement

3D 3 Dimensional

4P 4 Point Hall Measurement

AC Alternating Current

AFM Atomic Force Microscopy

Al_2O_3 Aluminium Dioxide

ALD Atomic Layer Deposition

Au Gold

CTL Circular Transmission Line Measurement

CV Capacitance – Voltage

CVD Chemical Vapour Deposition

DIBL Drain Induced Barrier Lowering

DC Direct Current

e^- Electron

eV Electron Volt

D_{it} Interface Defects

FET Field Effect Transistor

G_m Transconductance

I_{ds} Drain - Source Current

IV Current – Voltage

MOS Metal Oxide Semiconductor

MoSe_2 Molybdenum Diselenide

MoS_2 Molybdenum Disulfide

MoCO_2 Molybdenum Hexacarbonyl

MOSFET Metal Oxide Semiconductor Field Effect Transistor

n Electron Doping

p Hole Doping

Nb Niobium

R_c Contact Resistance

R_q Root Mean Square Average of Height Deviation

R_{sh} Sheet Resistance

SEM Scanning Electron Microscopy

SiO₂ Silicon Dioxide

SNR Signal to Noise Ratio

TCAD Technology Computer Aided Design (Software)

TEM Transmission Electron Microscopy

TLM Transmission Line Measurement

TMD Transition Metal Dichalcogenides

V_{ds} Drain - Source Voltage

V_{gs} Gate - Source Voltage

WSe₂ Tungsten Diselenide

WS₂ Tungsten Disulfide

μ Mobility

List of Publications

Publications Directly Related to the Thesis:

Chapter 2

Investigating interface states and oxide traps in the MoS₂/oxide/Si system

E Coleman, G Mirabelli, P Bolshakov, P Zhao, E Caruso, F Gity, S Monaghan, K Cherkaoui, V Balestra, RM Wallace, CD Young, R Duffy, PK Hurley
Solid-State Electronics (2021).

Chapter 3

Large-area growth of MoS₂ at temperatures compatible with integrating back-end-of-line functionality

J Lin, S Monaghan, N Sakhuja, F Gity, R Kumar Jha, E Coleman, J Connolly, C P Cullen, L Walsh, T Mannarino, M Schmidt, B Sheehan, G Duesberg, N McEvoy, N Bhat, PK Hurley, I Povey, S Bhattacharjee,
2D Materials (2020).

Chapter 4

Scrutinising pre- and post- device fabrication properties of atomic layer deposition WS₂ thin-films

E Coleman, F Gity, R Duffy, S Monaghan, B Sheehan, G Mirabelli, S Balasubramanyam, A A. Bol, PK Hurley
Applied Physics Letters (2023).

Chapter 5

Synthesis of large area crystalline MoS₂ by sputter deposition and pulsed laser annealing

E Di Russo, A Tonon, A Mischianti, F Sgarbossa, E Coleman, F Gity, L Panarella, B Sheehan, V Lebedev, D De Salvador, R Duffy, E Napolitani.
ACS Applied Electronic Materials (2023)

Publications Not Directly Related to the Thesis:

Structural and electrical characterisation of PtS from H₂S-converted Pt

S Monaghan, E Coleman, L Ansari, J Lin, A Buttner, P Coleman, J Connolly, I Povey, B Kelleher, C O Coileain, N McEvoy, PK Hurley, F Gity, Applied Materials Today (2021).

Atomic Layer Deposition of Large-Area Polycrystalline Transition Metal Dichalcogenides from 100 °C through Control of Plasma Chemistry

M Mattinen, F Gity, E Coleman, J F A Vonk, M Verheijen, R Duffy, W M M Kessels, A A. Bol Solid-State Electronics (2021).

Conferences: Oral and Poster Presentations

Large Area Growth of MoS₂ by Chemical Vapour Deposition

AiMES ECS Conference, Cancun, Mexico, October 2018.

An investigation of carrier mobility in MoS₂ grown by chemical vapour deposition in a 300mm reactor

MRS Conference, Phoenix, USA, April 2019.

Activation Energy Extractions in Low Thermal Budget CVD MoS₂ by a 300mm Reactor

IEEE SISC, San Diego, USA, December 2019.

Investigating interface states and oxide traps in the MoS₂/oxide/Si system

INFOS, Online, June/July 2021.

Dedicated to my Grandad

I, Emma Coleman, certify that this thesis is my own work and I have not obtained a degree in this university or elsewhere on the basis of the work submitted in this thesis.

Emma Coleman

Acknowledgements

I would first like to thank my supervisors Prof. Paul Hurley, Dr Karim Cherkaoui and Prof. Colm O'Dwyer. Paul, never has there been a kinder, more supportive and understanding supervisor. A lot has happened over the last few years, both inside and outside of the PhD. Life wasn't always easy and I was so very fortunate to have had you as my supervisor. The joy and enthusiasm you bring to the workplace is something I admire and I will try my best to do the same throughout my career. I would also like to extend a huge thank you to Dr. Karim Cherkaoui. The probe station would not have been the same (or worked) without you. Your guidance and assistance in the lab was invaluable and I really appreciated it. . . especially when you had to help over facetime back in 2020! And to Prof. Colm O'Dwyer, you were a big influence when it came to deciding to do a PhD when I was in undergrad. You made research enjoyable and exciting and I want to thank you for those first positive experiences in the lab.

I would like to thank my Viva examiners Dr. Michael Nolan and Dr. Toby Hallam. To Dr. Ray Duffy, Dr. Farzan Gity and Dr. Scott Monaghan, your guidance, help and encouragement throughout the last few years has meant so much to me. Thank you all for being such kind and motivating mentors. I was so lucky to be a part of your group. And thank you to my other fantastic Tyndall colleagues, past and present, including Dr. Jun Lin (Sally), Dr. Brendan Sheehan, Dr Gioele Mirabelli, Dr. Carlos Marquez, Dr. Shubhadeep Bhattacharjee, Dr Joice Ponraj, Dr. Justina Anulika Ugwah and Dr. Mack Johnson. I would also like to extend my thanks to colleagues from outside of Tyndall including Prof. Ageeth Bol, Dr. Miika Mattinen, Dr. Nikolay Petkov, Dr. Vasily Lebedev Dr. Enrico Di Russo and Dr. Enrico Napolitani.

To the amazing, lifelong friends I made throughout my time in Tyndall. To Anya, my partner in crime, thank you for always being there (both literally and figuratively) and for the many amazing adventures we had along the way. To Ian, thank you for the constant laughs, evening chats and free counseling sessions. I will miss the random sweets found in my headphones. To my Tyndall family Louise, Ruaidhri, Creamy, Dillane, Rory, Anna, Eoin and Meysam, I probably should say that the research was my favourite part of the PhD, but if I am honest, my favourite part was squishing on to one table at lunch and belly laughing with all of you.

To my gorgeous friends outside of Tyndall. Eimear, from supporting me through those awkward teen years to supporting me through this PhD, you have always been my rock. To Emma and Niamh, we have all come a long way from Ovens N.S and I wouldn't be where I am today without ye. To Alison, Caoimhe and Amy, thank you for your endless love, support and friendship. To my chemistry crew Eimear, Niall, Eadaoin, Trevor and Alex, thank you for always making time in 319 so enjoyable. Thank you to James for sending top tier memes, those chuckles were very much appreciated. Thanks to my Bendemeer family Ayisha, Caolan, Sinead, Dillane and Fran (the cat). I was so lucky to have such an amazing, and slightly unhinged, group of friends to come home to every evening after work. And to the extension of that family, thank you to Russell, Nicole and Dave, you were basically our adoptive housemates and it wouldn't have been the same without you. I would also like to thank both my Belvedere hockey team

and Phantom Tags tag rugby team. Sport has always been such an important part of my life and some of the tougher days during the PhD were made so much better when I was out on the pitch with all of you.

To Jen Lefforge, Liam Munn, Adam Hattan, Gary C, Rachel Maksy, Cecilia Blomdahl, Caleb Marshall, Karen Bee, Beatrice MacCabe, Rosemary MacCabe, Bo Burnham, Billie Eilish and Phoebe Bridgers, thank you for keeping me entertained throughout these last few years. Your youtube channels, podcasts and music have gotten me through countless sessions of graph plotting, poster making and thesis writing.

Thank you Kay and Orla, without the two of you I wouldn't be the person I am today. I am proud to have finished the PhD and show the two of you what has been accomplished.

Thank you to Papa, Nana, Brendan, Mary and Granny. How lucky I am to have such a beautiful family. You have supported me throughout all stages of my life and I am forever grateful for your love and encouragement... and I know Grandad is beaming down with pride. To Mary and the boys next door, thank you for always cheering me on. To my new relatives Anne, Kevin, Emily and Tom, thank you for welcoming me into your family and making me feel so accepted. Now I have 2 homes!

On that note, I would like to thank my best friend and partner, Killian. Hands down, the best thing to come out of this PhD is meeting you. You have gotten me through the good days, the not so good days, you make me laugh everyday and as an added bonus, thank you for being a physics genius and helping me with science/coding queries!

Finally, to my Mom, Dad and sister Julie. I won the lottery when it came to family. Thank you seems too small a phrase to convey what I want to say to you. Your support all through the years has meant the world to me. Our Coleman clan is something I will always be so grateful for and thank you for being the most amazing family anyone could ask for. And to the best dog Mo, thanks for all the cuddles.

Abstract

In recent years 2D materials, and more specifically transition metal dichalcogenides (TMD) MoS_2 and WS_2 have been investigated in the field of semiconductors as they exhibit energy gaps which span from semi-metals through to wide band gap semiconductors. Due to their thickness on an atomic scale, their properties differ from that of their bulk counterpart. The tunability of TMD bandgaps between the monolayers and bulk allows for a broader range of physical, electronic and optical properties and can be applied to a variety of applications including sensors, photodetectors, flexible devices, optoelectronics, electronic (logic and memory) devices and green energy. This thesis focuses on the possible use of TMDs for the 3D back end of line (BEOL) integration of logic and memory and it investigates some of these challenges to help bridge the gap in the knowledge to strive for the reality of 3D BEOL.

One of the approaches examined in this thesis is the mechanical exfoliation of TMD crystals. The interface properties of WS_2 or MoS_2 and insulating oxides is investigated with fabricated inverted MOSCAP (metal oxide semiconductor capacitor) structures, where a heavily doped silicon substrate is used as the back gate. With a variety of different devices, the impact of boundary defects is discussed along with a proposed bulk defect effects.

Another important line of work is the improvement of TMD growth. Chemical vapour deposition (CVD) is a popular TMD growth process. Though high quality TMDs have been produced by CVD, there is a lack of knowledge about how to grow at lower temperature, in order to stay within the thermal budget of 3D BEOL. We investigate CVD grown MoS_2 at temperatures lower than 550°C and perform Hall data on transistors which provides positive mobility values and carrier concentrations.

The significance of this work also shows findings in the nanoelectronic operation of atomic layer deposition (ALD) WS₂. Insight is gained from Hall effect analysis and temperature dependent electronic studies, which are lacking in literature. Typically, for WS₂ thin-films, the mobility values reported to date have been field effect mobility values extracted from transistor characteristics. More specifically, data includes the similarity of contact and sheet resistance temperature dependence in the WS₂ device, indicating that both are dominated by the WS₂ hole concentration temperature dependence. Moreover, rarely reported change in the TMD material, such as sheet resistance, due to device fabrication, is attributed to the chemicals and thermal treatments required to form the electronic devices.

Finally, the aim of investigating laser annealed MoS₂ was to show an in-depth investigation into synthesizing crystalline MoS₂ layers on wafer scale area, where MoS₂ films deposited on Si and Si/SiO₂ surfaces are explored. This method shows that within the correct parameter range, the process can produce crystalline MoS₂ films with small domains size of around 3.5 nm, from an initially amorphous MoS₂ film. Field effect transistors formed in laser annealed MoS₂ show limited I_{ds} variation with V_{gs} consistent with the small domain size.

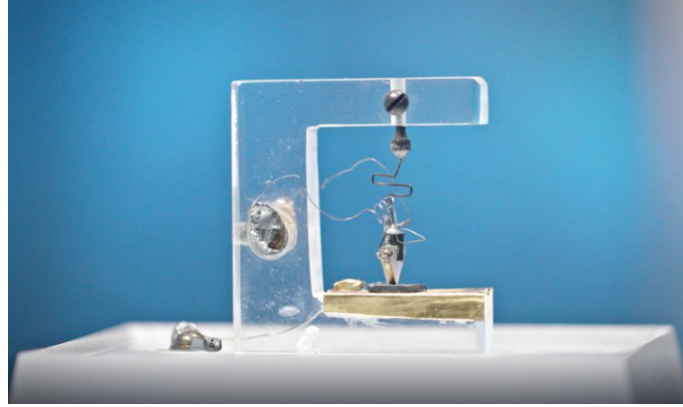
Chapter 1

Introduction

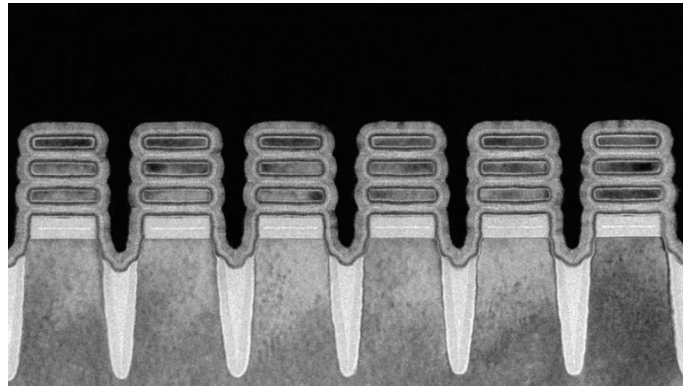
1.1 Historical Background of Semiconductors

In 1930, Julius E. Lilienfeld filed his patent with the title 'Method and Apparatus For Controlling Electric Currents' which is the birthplace of our modern day field effect transistor [1]. Unfortunately for Lilienfeld, he was slightly ahead of his time. It was not until December 1947 when John Bardeen and Walter Brattain invented the first working transistor in Bell Labs, New Jersey [2]. Note, this was a bipolar transistor and not a MOSFET as Lilienfeld has proposed. William (Bill) Shockley, the head of this research group, also majorly contributed to this work, including being the first person to consider minority carrier injection into the semiconductor [3]. The 3 men were awarded the 1956 Nobel Prize in Physics "for their researches on semiconductors and their discovery of the transistor effect".

The foundation of semiconductor scaling has been built around Moore's Law. In 1965 Gordon Moore predicted that every 2 years, the number of transistors on a circuit would double [4]. The first transistor was approximately 40 mm in size as seen in Figure 1.1 (a).[5] About 2 decades after the discovery of the transistor, Dawon Kahng published his schematic of a Metal Oxide Field Effect Transistor (MOSFET) structure.[6]. In 1974, Dennard et al introduced his MOSFET scaling theory, showing that when the transistors got smaller, the power consumption per transistor goes down.[7] With the introduction of MOS structures in the 1970's, Very Large Scale Integration (VLSI) became accepted on an industrial scale. Due to their high speeds with lower voltage and lower power consumption, MOS structures became a fundamental building block in complex integrated circuits [8]. In 2021, IBM announced their 2nm technology node - Figure 1.1 (b) - fitting approximately 50 billion transistors into the area of a fingernail.[9] However, with such vigorous down-scaling over the last 70 years, dimensional limits of Si challenge the continuation of Moore's law.[10, 11]



(a)



(b)

Figure 1.1: (a) The first transistor invented by John Bardeen and Walter Brattain in 1947. [5] (b) IBM's Row of 2 nm nanosheet devices as seen using transmission electron microscopy. [9]

1.2 Short channel MOSFET effects

Some of the biggest limitations of Si MOSFETs come from scaling and short channel effects. MOSFETs exhibit short scale effects when at a source-drain voltage of zero, the depletion layer width of the source and drain regions sum to the channel length [8].

If we take the general model for the behaviour of current in a MOSFET as

$$I_{ds} = \mu_n C_{ox} \frac{W}{L} [(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}] \quad (1.1)$$

where μ_n is the mobility of carriers, C_{ox} is the oxide capacitance, W is the channel width and L the channel length, V_{gs} is the gate-source voltage, V_{ds} is the drain-source

voltage and V_{th} is the threshold voltage. We can show the relationship between mobility, electron drift velocity (v_n) and electric field (E) at some distance x by

$$v_n = \mu_n E(x) \quad (1.2)$$

For short channel MOSFETs, the decrease in L causes an increase in the electrical field along $E(x)$. When the critical value of the electric field, E_c , is reached, constant V_{ds} can be represented as

$$V_{ds,sat} = L \times E_c = L \frac{v_{sat}}{\mu_n} \quad (1.3)$$

With this, at saturated current we combine equation 1.1 with equation 1.3 to get

$$I_{ds,sat} = v_{sat} C_{ox} W \left[(V_{gs} - V_{th}) - \frac{V_{ds,sat}}{2} \right] \quad (1.4)$$

Here, velocity saturation occurs where the drain current is linearly dependent on $(V_{gs} - V_{th})$ and W and not V_{ds} [12, 13]. This impacts the scalability and speed of devices.

Short channels also induce Drain Induced Barrier Lowering (DIBL), caused by a field penetration from the drain depletion region moving closer to the source depletion and leading to a shifted threshold voltage [14, 15]. The effect of DIBL in a MOSFET is visually represented in Figure 1.2. [15], where the surface potential is plotted against the channel length. Curve A shows a long-channel MOSFET where the potential peak is kept constant over most of the channel length. Poisson's equation can be used to calculate the height of this peak. Curve B shows the shortening of the channel length, where the potential peak is now just one curve and its height is lower than that of the long channel peak (Curve A). Curve C shows the further implications

of shortening the channel length, where the drain voltage is increased, the potential height is further decreased and with an increase in channel current.[15] As the size of transistors continues to drastically decrease in modern technology, the physical and economic challenges of optical lithography increases [16]. Diffraction effects limits the minimum dimensions of UV exposure. This has led to a need for advanced lithography methods including extreme UV lithography, ion beam lithography [16, 17], short-wavelength lithography and electron beam lithography [16, 18]. The cost of these techniques, performance proficiency and accuracy play key roles in the choice of lithography and are still a huge area of question for large scale integrated circuit production [16].

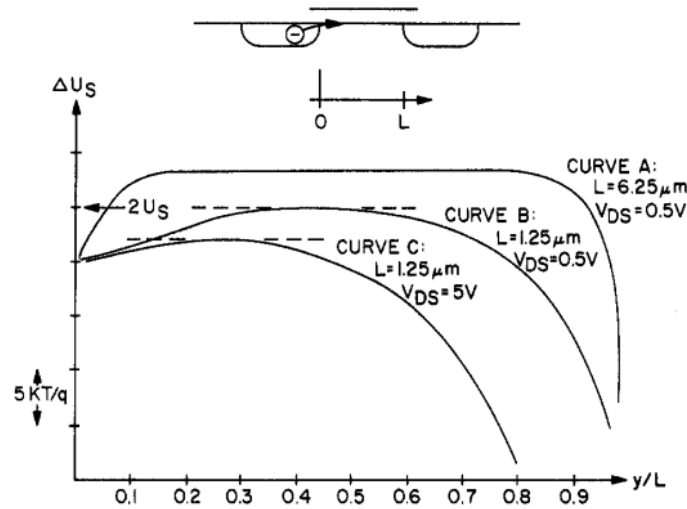


Figure 1.2: Schematic representation of Drain Induced Barrier Lowering. [15]

Another short channel challenge is the relationship between V_t (threshold voltage) and I_{off} (off current). For a transistor to turn on, V_{ds} must be greater than V_t , otherwise the current drops off exponentially. There is a minimum subthreshold slope at room temperature of 60mV/dec [19]. This is further explained with the help of Figure 1.3 [20]. Curve 1 conveys a traditional bulk MOSFET where V_t (threshold voltage) cannot be decreased without the increase of I_{off} , causing an increase in power consumption. 3 orders of magnitude of leakage current can occur from a shift of just 200 mV in

V_t . At the moment there are 2 solutions; (a) If the subthreshold slope is steeper, this allows for a V_t at a fixed I_{off} (curve 2) or (b) keep the same V_t and have a much lower I_{off} (curve 3). Curve 4 shows the 'ideal' solution and is currently being investigated with a sub 60 mV/dec subthreshold swing. In Curve 4, the voltage V_{DD} could not be used in the other examples 1-3 because V_{DD} is in the sub threshold region, below the value of their V_t [20].

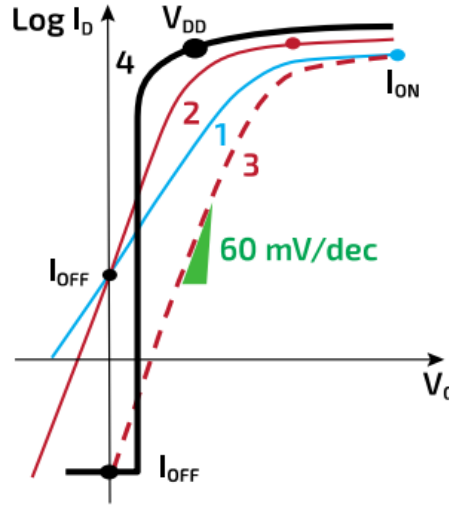


Figure 1.3: Schematic of sharp-switching transistor. Curve 1 - Bulk Si MOSFET degraded subthreshold. Curve 2 - MOSFET with slope of 60 mV/decade (room temp) and a low threshold voltage. Curve 3 - MOSFET with slope of 60 mV/decade (room temp) and reduced I_{off} . Curve 4 - 'Ideal' sharp switching MOSFET device [20].

1.3 Transition Metal Dichalcogenides

So what is the next step for MOSFETs? This thesis is focused on (1) finding materials which can scale further than silicon and (2) the investigation into 3D integration. One of modern science's most serendipitous moments came in 2004, with the discovery of monolayered graphitic films by Prof. Novoselov and Prof. Geim [21]. During one of their casual 'Friday afternoon' sessions they found that the repeated mechanical exfoliation of graphite, with merely some sticky tape, could get the material down to a few monolayers of carbon while still maintaining its stability and strength [21]. The

success of graphene stems from the fact that for such an easy and cheap fabrication, it has excellent electronic properties [22]. Some of these include its impenetrability to gases [23], high room temperature electron mobility [24], intrinsic strength [25], ability to survive high electric currents [26] and a high thermal conductivity [27]. However, one of the main problems with graphene is the zero width bandgap. Effects from this include the channels not switching off making them unfit for complex logic circuits [28]. This is where 2D TMDs (Transition Metal Dichalcogenides) have become a key topic in this field of research.

Transition metal dichalcogenides are broadly represented as MX_2 where M is the metal and X is the chalcogen (group 16 of periodic table) [29]. The layers of TMDs are held by weak Van der Waals forces while the interatomic bonds of each layer are covalent. The structures consist of a metal layer sandwiched between 2 chalcogen layers [29–31], as seen in Figure 1.4. The properties of bulk TMDs are varied from semi metals (NbS_2 and VSe_2) right through to wide gap semiconductors. This body of work focuses on the semiconductors such as MoS_2 and WS_2 .

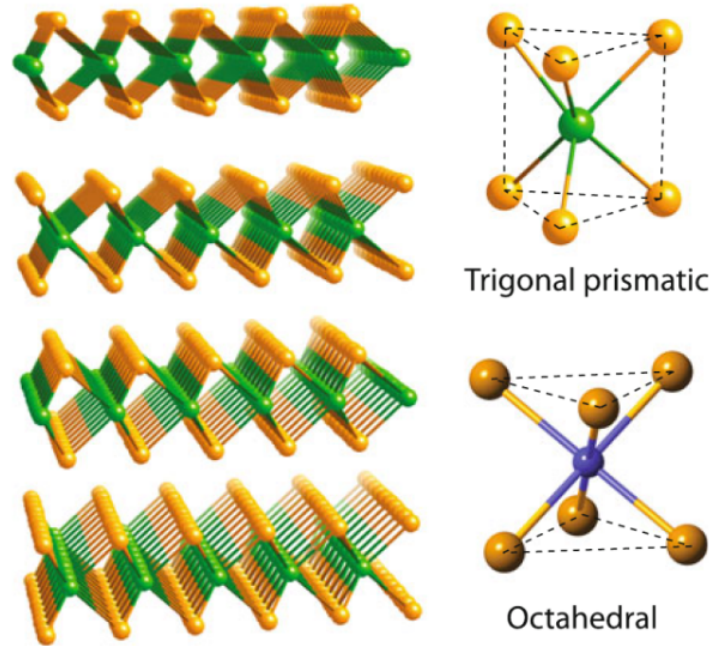


Figure 1.4: On the left is a 3-dimensional representation of a classic TMD structure. The metal is in green and the chalcogen in orange. To the right are 2 different orientations of the metal species that can be found - on the top is trigonal prismatic and on the bottom is octahedral [29].

TMDs, such as MoS_2 and WS_2 , have become one of the focal points for research into next generation semiconductor materials thanks to the magnitude of their bandgaps. Due to their thickness on an atomic scale, their properties differ from that of their bulk counterpart [32]. For monolayer MoS_2 and WS_2 the *direct* bandgaps are approximately 1.9 eV and 2 eV respectively. Contrastingly, for bulk MoS_2 and WS_2 the *indirect* bandgaps are approximately 1.2 eV and 1.3 eV respectively [33, 34]. Figure 1.5 depicts the band structures for bulk and monolayer (a) MoS_2 and (b) WS_2 . With this direct bandgap, an interband tunnel FET can be made which consumes less power than traditional transistors [35, 36]. Also, the tunability of TMD bandgaps between the monolayers and bulk allows for a broader range of physical, electronic and optical properties and can be applied to a variety of applications [37, 38].

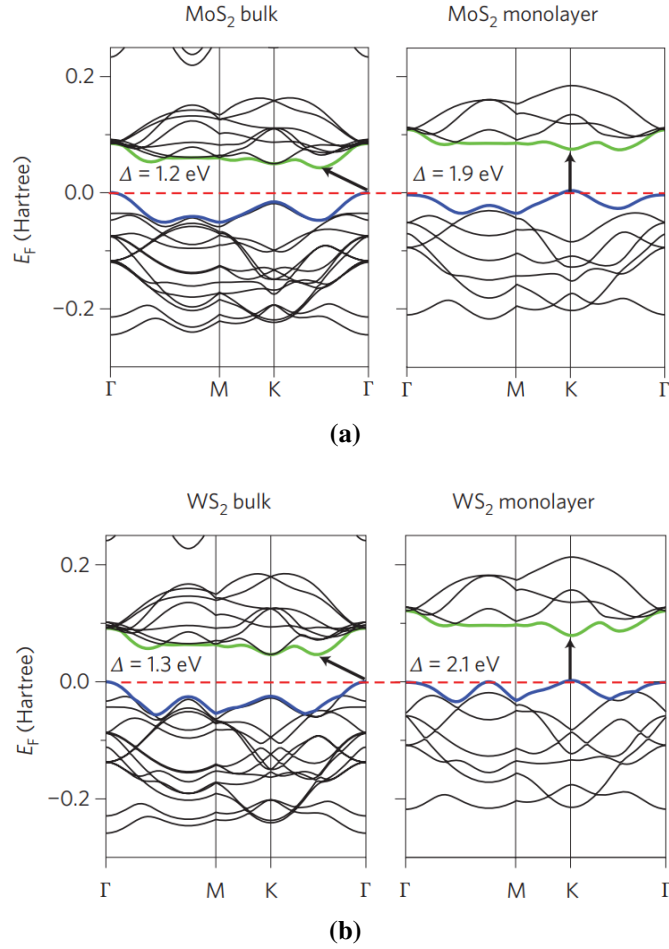


Figure 1.5: Band structures calculated from first-principles density functional theory (DFT) for bulk and monolayer MoS₂ (a) and WS₂ (b). The horizontal dashed lines indicate the Fermi level. The arrows indicate the fundamental bandgap (direct or indirect). The top of the valence band (blue) and bottom of the conduction band (green) are highlighted [34].

The possible applications of TMDs are extensive. They include sensors, photodetectors, flexible devices [39], optoelectronics [40], electronic (logic and memory) devices and green energy.[41] As discussed earlier, industry is hitting the dimensional limits of transistors, all the while trying to reduce both device sizes and energy consumption. It is here where TMDs are bringing possible answers in the form of logic and memory in back end of line (BEOL) [42]. BEOL is the section in an integrated circuit where the individual components of the circuit are interconnected.[43] If active devices can be incorporated into the BEOL this will decrease latency, decrease power consumption, and increase the form factor. These 2D materials also offer more ideal surfaces due to

their large anisotropy [44]. Figure 1.6 shows a theoretical schematic of the 3D BEOL integration of memory and logic. Here, layers of logic combine with memory technology.[42] The fabrication process consists of low temperature growth and integrated layers stacked in a three dimensional chip.[45]. These thin devices could allow short, high-density interlevel paths, connecting logic and memory in an interated circuit.[42]

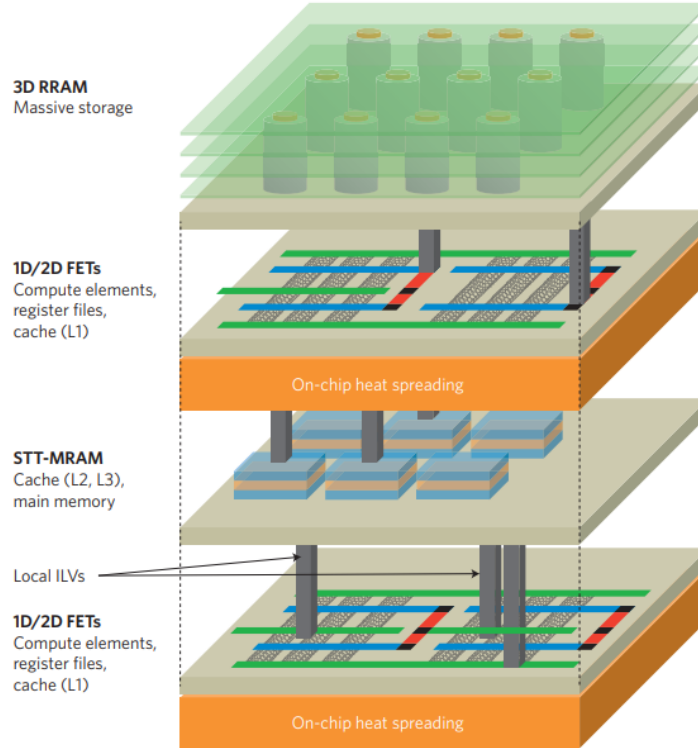


Figure 1.6: Monolithic 3D integration of memory interleaved with logic computation layers. ILV, interlevel via; FET, field-effect transistor [42, 45].

1.4 Growth Processes of MoS_2 and WS_2

There are numerous ways in which TMDs such as MoS_2 and WS_2 can be fabricated into devices. The first is of course mechanical exfoliation of natural TMD crystals. However, popular methods like chemical vapour deposition (CVD) and atomic layer deposition (ALD) have gained a lot of interest in terms of highly controlled wafer growth of MoS_2 and WS_2 . This thesis investigates both processes, and more specifically, looks at CVD grown MoS_2 and ALD grown MoS_2 . For CVD MoS_2 , conditions

for growth vary greatly including choice of precursors, growth temperature, pressure and duration of process. Yu et al grew uniform monolayer and bilayer MoS₂ films at 800 °C using MoCl₅ as a precursor and found their process to be self-limiting.[46] A common set of precursors is MoO₃ and sulfur vapour. Groups including Lee et al and Chen et al used these to grow MoS₂ films at 650 °C which produced n-type transistors with an Ion/Ioff current ratio of $\approx 10^4$ and $\approx 10^5$ respectively.[47, 48] Bergeron et al grew at 800 °C and found an Ion/Ioff current ratio greater than 10^4 with field effect mobility of 0.4 - 4.1 $cm^2 V^{-1} s^{-1}$. At 680 °C, Zheng et al obtained transistors with a field effect mobility of 0.2 and 0.05 $cm^2 V^{-1} s^{-1}$ with an Ion/Ioff ratio of 10^6 and 6×10^3 .[49].

However, one of the major obstacles for large area CVD growth is the low thermal budget for 3D BEOL. In order to successfully create 3D integrated circuits, the temperature at which the top tier layers are deposited/grown cannot exceed the thermal budget.[50] In order to successfully create 3D integrated circuits, the temperature and time at which the materials are made cannot be above the thermal budget which degrades the underlying transistors. The first negative impact is typically on the source and drain silicide contacts in the p and n channel MOSFETs. [50] The permissible thermal budget for above CMOS will depend on the particulars of the process, but a representative example is shown below. Based on the work of Fenouillet-Beranger et al, no degradation of the underlying CMOS performance was detected up to 550 °C for 2 hours and 500 °C for 5 hours.[50, 51] Figure 1.7 suggests that 550 °C for 2 hours should be acceptable, and is used as the upper limit for the thermal budget for the CVD MoS₂ growth. The use of Mo(CO)₆ and H₂S as precursors also allows for lower temperature growth.[52] Mun et al utilised these precursors and grew monolayer MoS₂ with a maximum Ion/Ioff ratio of 10^5 and a mobility of 0.15 $cm^2 V^{-1} s^{-1}$ at a temperature of 350 °C. At 400 °C, Kim et al produced monolayer transistors with a mobility of 0.47 $cm^2 V^{-1} s^{-1}$ and Ion/Ioff ratio of 5.4×10^4 .

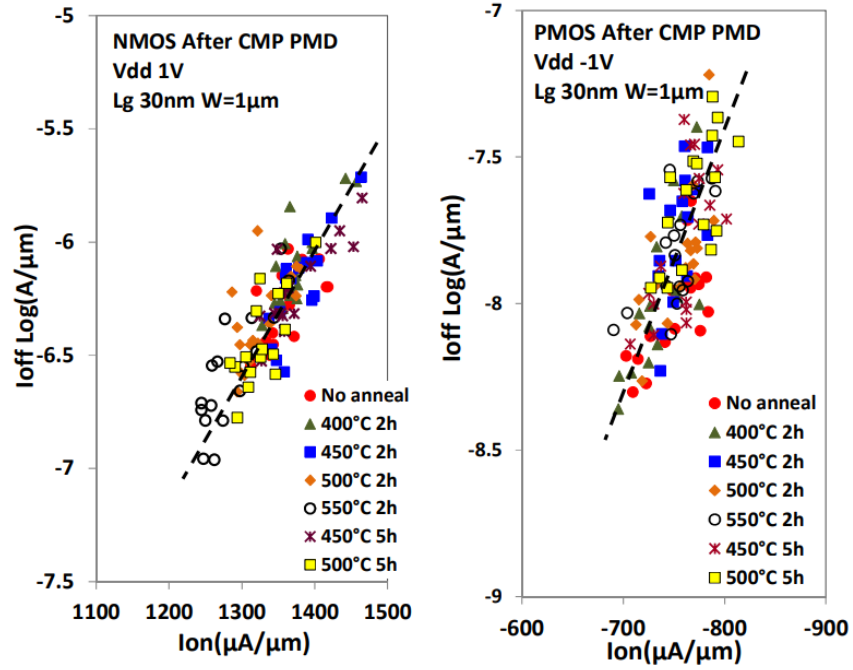


Figure 1.7: NMOS and PMOS I_{on}/I_{off} of bottom transistor versus thermal anneals [51].

WS₂ large area deposition has been explored by chemical vapour deposition (CVD) [53–56] and by sulfurisation of WO_x [57, 58]. Notably, ALD chemistry studies of WS₂ synthesis have been undertaken by Groven et al [59, 60] and demonstrated 3 nm thin-films in FETs. Furthermore, Balasubramanyam et al. produced area-selective ALD WS₂ films in the nanometre range [61], while Kim et al. studied ALD WS₂ as a catalyst for water splitting [62]. Dorow et al [63] (shown in Fig. 1.8) and Lin et al [64] fabricated FETs using CVD films and both showed benchmarking of the latest WS₂ thin-films FETs and is shown in Schram et al. compared ALD and CVD WS₂ FETs with low-temperature device integration flows, and highlighted substrate adhesion issues [65]. Recently, Yang et al [66] produced impressive ALD WS₂ FET I_{on}/I_{off} ratios of 10^5 , as well as Nb-doping in ALD deposited WS₂ films [67].

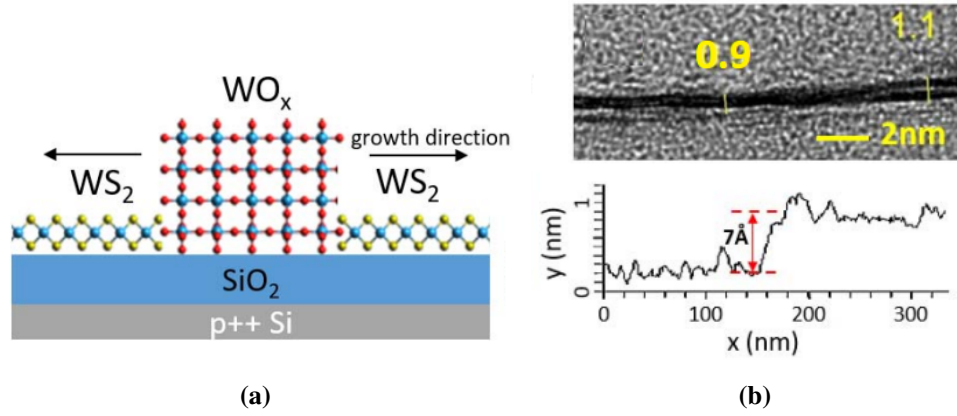


Figure 1.8: (a) Schematic diagram of WS₂ high temperature growth in S- based gas from WO_x seed [63]. (b) Cross sectional TEM and AFM step height plot of grown WS₂ [63].

Modifying the properties of Transition Metal Dichalcogenide (TMD) materials is a research area which has emerged in recent years [68–71]. Short time laser processing has adjusted TMDs by doping [72], phase transformation [73–75], localised patterning [76, 77], thinning or etching [78–80] and site-specific modification.[81, 82] However, with its positive possibilities comes its challenges. Laser conditions can vary considerably depending on a number of parameters - wavelength, repetition, laser source and pulse duration. As well as the laser conditions, results can fluctuate due to substrate type, what TMD is being tested, processing aims and the ultimate application required. Since 2015, there have been a handful of studies done on laser annealing of 2D materials in general. It begins with synthetic MoS₂ flakes [83–85] and has now followed into the trend of thin films [86, 87], with many concentrating on MoS₂ formed by sputter deposition [88]. Investigations of MoS₂ and other TMDs laser processed on different high-k dielectrics have taken place [74, 89, 90]. Studies also include a host of substrates including Polydimethylsiloxane (PDMS) [91, 92], boron-nitride (BN) [93, 94], and more commonly, SiO₂ on Si [95, 96] and glass [79, 97]. When it comes to laser annealing, the choice of substrate can greatly affect the process, due to the irradiation reflection or absorbance of the laser. When beginning a study, this can lead to a lot of 'fine-tuning' to perfect and optimise the procedure. When looking specifically at MoS₂, the popular approach is the use of the Raman 532

nm wavelength laser source [98–101]. However, when looking at other TMDs, the wavelengths span across a large range of 248-1048 nm [102, 103]. Laser sources also vary and include Nd:YAG [104], KrF excimer UV [105], Ti:sapphire [93] and Ar ion [106].

1.5 Challenges with TMDs

With all of these promising applications, there are quite a number of challenges to overcome in order to reach such potential. Some of these obstacles, as shown in Figure 1.9, include the previously mentioned thermal budget for BEOL [50], large area growth [107, 108], stable approaches to doping [109], understanding and controlling defects/grain boundaries [110], investigating the properties of oxide/TMD interfaces and achieving required values of specific contact resistivity [111]. It is noted that these challenges are relevant to the integration of TMDs as high performance logic devices as well as their application as logic and memory elements in the back-end-of-line (BEOL).

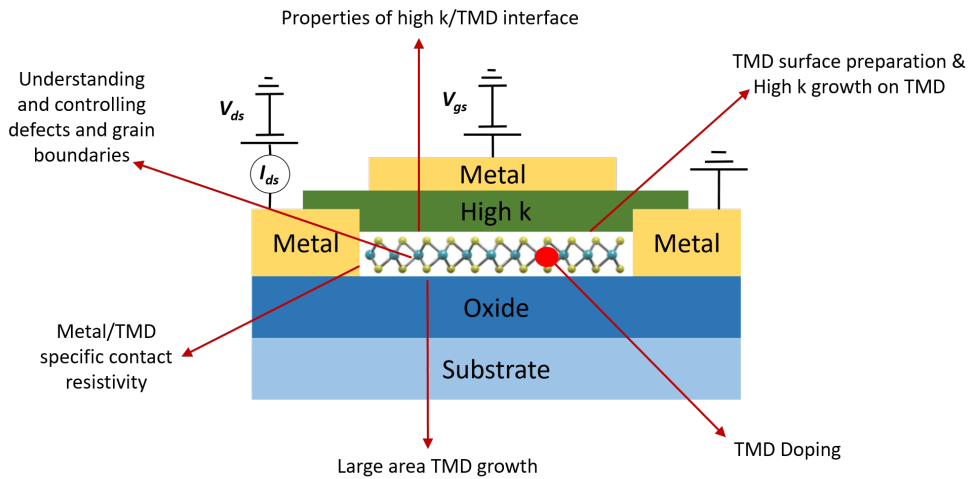


Figure 1.9: Challenges related to next generation TMD MOSFETs.

As mentioned above, defects in TMDs like MoS₂ and WS₂ can cause challenges

when it comes to the electrical behaviour of device. Work by Lin et al divide these 2D crystals into sub-groups which include zero-dimensional and one-dimensional defects.[112] Zero-dimensional defects include vacancies and adatoms. Santosh et al calculated formation energies of numerous defects and found that the most energetically favourable point defects were at sulfur vacancies and adatoms.[112, 113] Substitutional doping can also occur, for example the incorporation of oxygen into the lattice structure, possibly stemming from precursors or ambient conditions.[114, 115] One-dimensional defects include grain boundaries [110, 112], line vacancies [112, 116, 117] and the passivation of edges/vacancies.[118, 119] Figure 1.10 visually depicts a variety of possible defects in 2D TMD materials.[120] Outside effects can cause the formation of defects. When put through various different fabrication/characterisation procedures like electron beam imaging [34], chemical etching stimulation [113], vacancies generated during mechanical or chemical exfoliation [113], ballistic displacement of atoms (e.g. sputtering) and chemical etching [113].

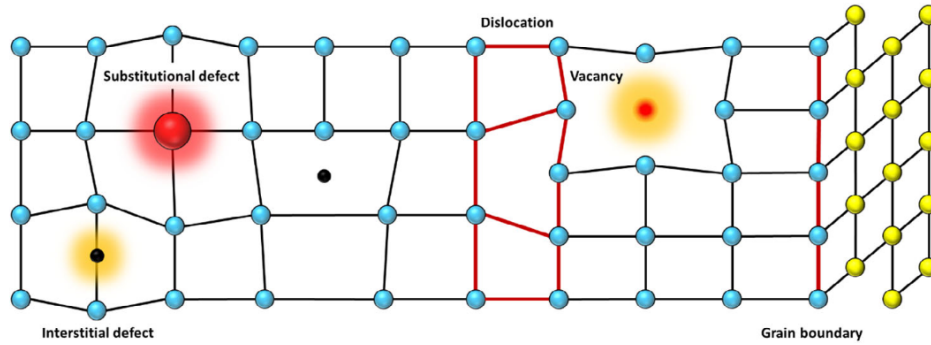


Figure 1.10: Variety of defects that can be found in 2D TMDs [120].

1.6 Thesis Outline

Chapter 2 discusses the theory of experimental methods utilised in this thesis. The parameters and setup of all processes are also reviewed.

Chapter 3 focuses on the mechanical exfoliation of natural MoS₂ and WS₂ crystals onto various substrates. The aim of this study is to extend the study of back gated

metal/MoS₂/oxide/Si MOS structures, where the MoS₂ or WS₂ layer is thicker than the maximum depletion width. The results cover a range of processes, combining experimental data and physics-based AC simulations. The results and analysis indicates that while close to ideal properties can be achieved, there is evidence of defects in the MoS₂ or WS₂ close to the TMD/oxide interface.

Chapter 4 investigates MoS₂ grown by chemical vapour deposition (CVD). One of the major obstacles of large area growth of 2D materials above existing integrated circuits is the low thermal budget for 3D BEOL. We explore the growth of MoS₂ by an industry compatible CVD process in the range 350 °C to 550 °C with times ranging from 30 minutes to 2.5 hours, with the aim of assessing the structural and electronic properties of the films.

Chapter 5 studies the structural and electrical behaviour of WS₂ grown by atomic layer deposition. We report Hall analysis of the WS₂ films as well as an examination of the temperature dependence of the bulk WS₂ resistivity and specific contact resistivity based on electrical Circular Transfer Length Method structures.

Finally, chapter 6 show an in-depth investigation into synthesizing crystalline MoS₂ layers on wafer scale area. Amorphous MoS₂ films were deposited on Si and Si/SiO₂ surfaces, and subsequently exposed to pulsed laser irradiation using a 248 nm KF laser as a route to MoS₂ crystallisation achieved in an irradiation time scale of 22 ns with varied amounts of laser pulses.

Chapter 2

Methods

2.1 Mechanical Exfoliation of Crystals

The first experimental chapter investigates mechanically exfoliated TMD crystals. The MoS₂ and WS₂ crystals were bought from HQ Graphene and varied in types of doping. The following procedure was executed to transfer the crystals on each substrate. Small strips of tape were cut and then pressed onto the crystal. When the flake of MoS₂/WS₂ was on the tape, the tape was then folded over itself 5 - 6 times to create thinner flakes. Once complete, the tape with thinned down MoS₂/WS₂ was pressed face down onto the substrate. The substrates were $\approx 1 \times 1 \text{ cm}^2$. After a number of seconds of pressing with the thumb, the tape was peeled back and left behind on the substrate were MoS₂/WS₂ flakes. There were usually a number of flakes on the substrate. The challenge was finding the flake best suited for the fabrication of an inverted MOSCAP structure. Only one flake could be used and once chosen, the sample could not be reused or reprocessed. With the use of an optical microscope and a profilometer, a flake was chosen for each sample. Figure 2.1 shows the mechanical exfoliation procedure. Note, the metal patterning is also seen in the figure, and this will be discussed later. There were certain criteria that needed to be met when choosing what flake to pattern. The lateral area of the flake had to be at least $\approx 60 \times 60 \text{ }\mu\text{m}$ so that the smallest metal contact ($40 \times 40 \text{ }\mu\text{m}$) would fully cover the TMD flake. Not only that, the thickness of the flakes needed to be $\geq 200 \text{ nm}$ to exceed the maximum depletion width of MoS₂. [121, 122] Finally, the surface of the flake had to be flat. This was to ensure the best possible adhesion to the metal contacts. I carried out these exfoliations.

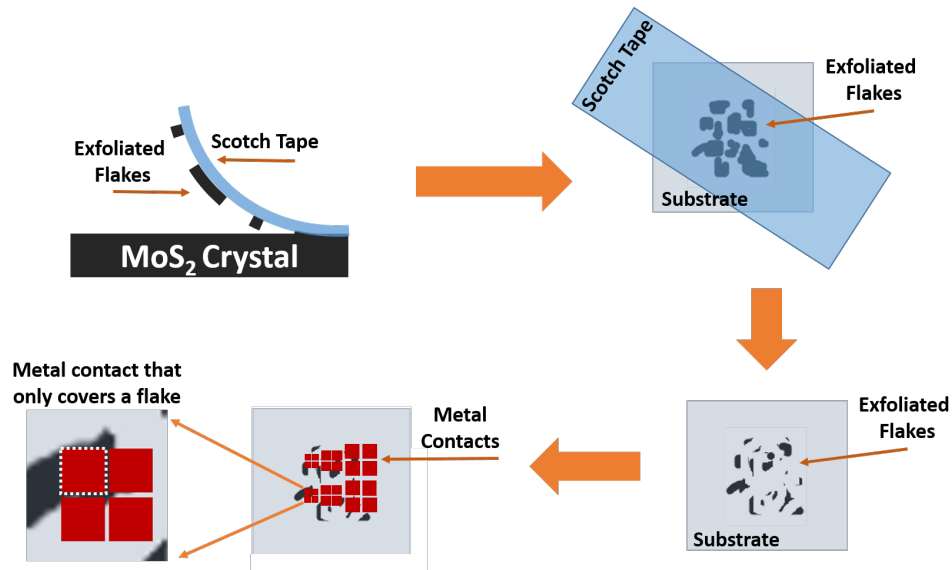


Figure 2.1: Schematic diagram of mechanical exfoliation process using scotch tap. Flakes are transferred on a substrate. The 'best' flake was then chosen and covered with the metal contact based on optical inspection and surface profilometer measurements.

2.2 Chemical Vapour Deposition

Chemical vapour deposition (CVD) is a deposition process that has been in use for more than 150 years.[123–125] Though the term 'CVD' was not officially coined until 1960 by John Blocher, this type of process was applied in many areas of industry well before that.[126] In fact, the process was first seen in 1852, when German scientist Robert Bunsen observed that in volcanic gases containing hydrogen chloride, iron oxide condenses as crystals. [127] In its most simple form, CVD is the deposition of solid materials using gaseous precursors in a vacuum system. Today, CVD is mainly used to form thin-films onto wafers in the semiconductor industry,[128–130] however it can also be applied to the production of high quality bulk materials and powders. [126] Focusing on general thin-film CVD, the following steps are applied. First, active reactants in a gaseous state are brought into the reaction chamber. Intermediate gaseous species are then formed, where the temperature is kept below the dissociation limit of the intermediate phase. This ensures diffusion of the species across the boundary layer of the substrate. Adsorption occurs on the heated substrate and both the deposit and

by-product species are formed. The deposits form the growth of the thin film and the un-reacted gaseous by-products (as well as un-reacted precursors) are taken out of the deposition chamber.[131] Figure 2.2 depicts this process.

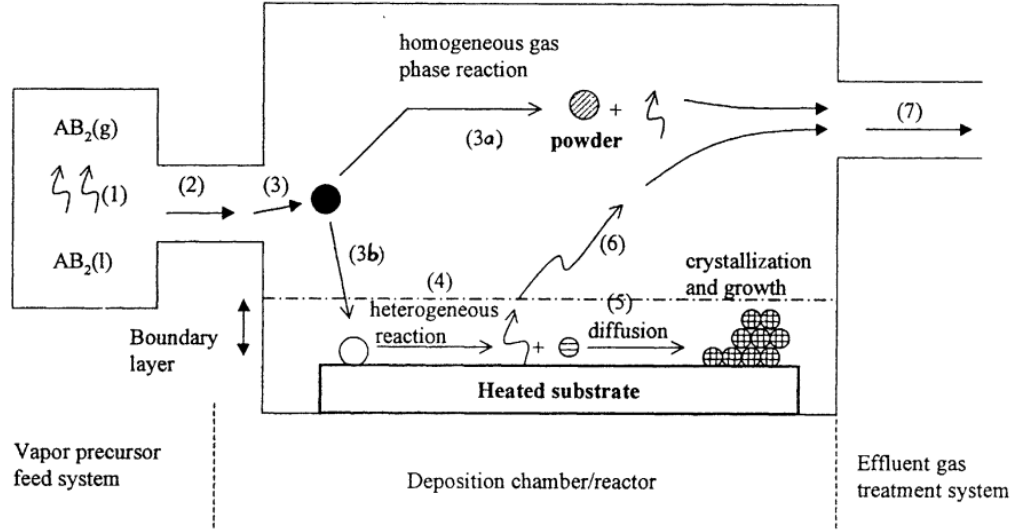


Figure 2.2: Schematic diagram of generalised CVD process.[131]

Regarding the work in this thesis, chapter 4 investigates CVD grown MoS₂ on various substrates. A commercial 300 mm ALD (atomic layer deposition) reactor with a shower head was used for the CVD of MoS₂. ALD will be discussed in more detail later in this chapter. The precursors were Mo(CO)₆ (99.99%, Versum Materials) and 1% H₂S (99.999%) in Ar (Air Products). The reactor temperature was varied between 350 °C and 550 °C and the chamber pressure maintained at $\approx$ 2.2 Torr by an N₂ carrier flow of 150 standard cubic centimeters per minute(sccm). Precursor flux of the Mo source was determined by the source temperature (28 °C – 50 °C) and the H₂S flow was set at 10 sccm or 20 sccm of the 1% gas mix. A variety of substrates were used - SiO₂ (85 nm) on Si (p++), c-plane sapphire, glass, and amorphous alumina (a-Al₂O₃, $\approx$ 30 nm grown by ALD) on c-plane sapphire and on glass. These were all done at the highest temperature of 550 °C and the growth time was $\approx$ 2.5 hours for all nominally 10 nm MoS₂ thicknesses. For lower temperature growth (350 °C and 450 °C) the precursor flow was altered by doubling H₂S flow or reducing the Mo(CO)₆

flux by lowering the Mo(CO)_6 ampule temperature. The objective was to increase the sulfur/molybdenum ratio in order to minimise sulfur vacancies in lower temperature grown films. With sulfur vacancies, the molybdenum is exposed and open to chemical reactions.[132] For the reduced Mo(CO)_6 flow condition the growth time changed to ≈ 6 hours. It is noted that the growth times and temperatures are below the maximum thermal budget for above CMOS growth as discussed previously. These samples were grown in Tyndall and the CVD process was performed by Dr. Ian Povey.

2.3 Atomic Layer Deposition

Atomic layer deposition (ALD) is a subsection of CVD. The process was first developed by Russian scientists Aleskovskii and Kol'tsov in the 1950-60's.[133] The difference between them is that CVD reactions are all performed in one reaction, while in ALD, the gaseous precursors react separately with the substrate in a self-limiting process. Each gaseous reactant is sequentially pulsed into the vacuum chamber where a 'half-reaction' takes place with the substrate. Each cycle forms one monolayer of synthesised material. Once both reactions occur, the chamber is purged with an inert gas which removes any unreacted reactants or reaction by-products. This series of steps are repeated until the required thickness of material is formed.[134] Figure 2.3 shows a depiction of an ALD cycle. The advantage of ALD over general CVD is the ability to deposit reactants atomic layer by atomic layer, allowing the formation of films with a thickness control at the atomic level and films which exhibit conformity to the underlying substrate.

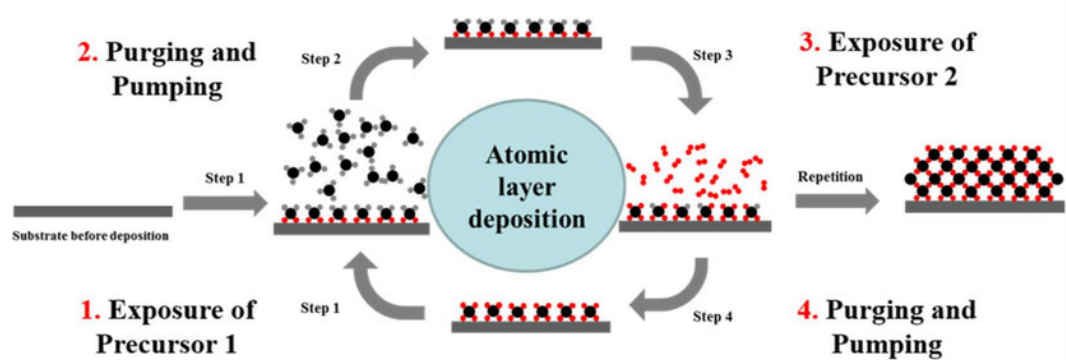


Figure 2.3: Schematic diagram of an ALD cycle.[135]

Chapter 5 of this thesis contains plasma enhanced ALD (PEALD) grown 2D WS_2 . These samples were grown by collaborators in TU Eindhoven.[136–138] An 'ABC' cycle was adopted. Step 'A' consisted of pulsing bis(tert-butylimido)-bis(dimethylamido)-tungsten precursor ($\text{W}-(\text{NMe}_2)_2(\text{NtBu})_2$) followed by step 'B', which pulsed the chamber with H_2S plasma precursor. Finally, step 'C' was performed. Here, a H_2 plasma was exposed onto the material in the chamber (15 mTorr) for 50 seconds at 500 W. Ar purges occurred between all steps.[138]

2.4 Sputter Deposition & Laser Annealing

Sputtering is a form of physical vapour deposition. There is a target layer made of the desired material. An inert gas is pumped into the chamber where an electric field is present between the target and substrate. The target is bombarded with atoms, causing the displacement of atoms and ions are formed in the plasma. They are transported on the substrate and a thin film begins to form, as seen in figure 2.4. [139–142]

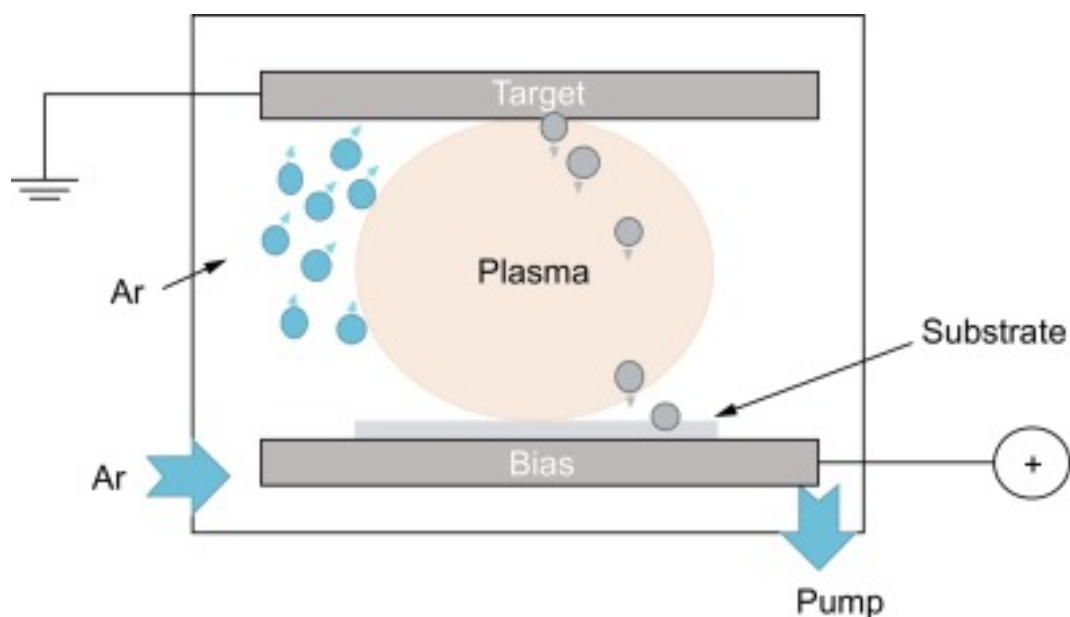


Figure 2.4: Schematic diagram of Sputter Deposition cycle.[139]

Chapter 6 looks at sputtered MoS₂ on Si substrates. These were made by collaborators in the University of Padova. MoS₂ films were grown on a SiO₂ on Si substrate which was supplied from Ossila. The $725 \pm 25 \mu\text{m}$ wafer was a p-type, B-doped Czochralski wafer with a resistivity of $< 0.001 \Omega/\text{m}$ followed by a thick, thermally grown, $90 \pm 4.5 \text{ nm}$ SiO₂ layer. Before sputtering, the SiO₂ on Si substrate was dipped in acetone for 10 minutes, dried with a N₂ jet and then cleaned in a UV/ozone cleaner for another 10 minutes. The nominal thickness of MoS₂ after the 3 minute deposition process was found using a KLA Tencor P17 stylus profilometer and found to be $(8 \pm 1.5) \text{ nm}$. This correlated with results from RBS, where the thickness was calculated to be approximately $(7.4 \pm 0.2) \text{ nm}$.

Immediately after MoS₂ sputtering, laser annealing took place using a Coherent COMPex 201 KrF excimer laser. The atmosphere was flushed with N₂ at 10 L/min over the whole sample. A homogeneous laser beam was pulsed at 1 Hz for the duration of 22 ns, where the laser spot size was $5 \times 5 \text{ mm}^2$. This was generated by a micro-lens laser beam homogenizer [143], with spatial energy density variations $< 2\%$

with a pulse accuracy and repeatability of $\approx 1\%$. For sputtering, the same process was used for both Si and SiO₂-on-Si substrates.

2.5 Device Fabrication

Throughout this thesis, a variety of metal-oxide-semiconductor (MOS) capacitors and field effect transistors (FET) were fabricated based on the grown or exfoliated TMD materials.. All devices were fabricated in Tyndall. Though device designs differed between chapters, the general fabrication processes were similar. All structures were patterned using Ni(5 nm)/Au(160 nm) metallisation through a lithography and lift-off process. A MA6 Mask Aligner was used as the photolithography setup. The samples were spin resisted with a PMGI bake on a hot plate at 180 C for 5 minutes. Note, for the exfoliated flakes in chapter 2, flakes were irregular in size, and the areas on the metal mask are squares. As a consequence, there were regions where the MoS₂/WS₂ were larger than the metal contacts and vice versa. This led to difficulties in interpretation of the electrical data, as the MoS₂/WS₂ and the gate metal areas are not equal. To overcome these issues, for selected samples the MoS₂/WS₂ was etched using the Ni/Au as a hard mask. For samples that were etched, the gas used was SF₆ (5 sccm)/Ar (45 sccm) for 30 seconds at 100 W and 6 mT [144]. Some samples were investigated without any etching process. It must also be noted, there were a number of flakes that did not survive the patterning process. Figure 2.5 shows the general cross sectional image of the MOSCAP device design.

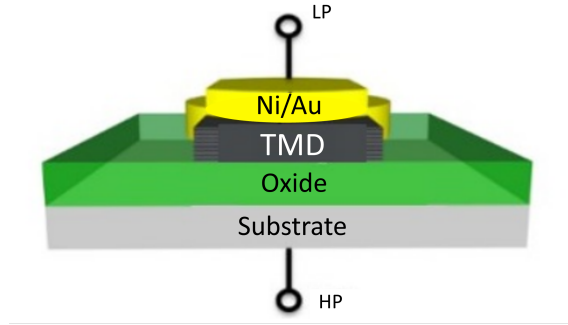
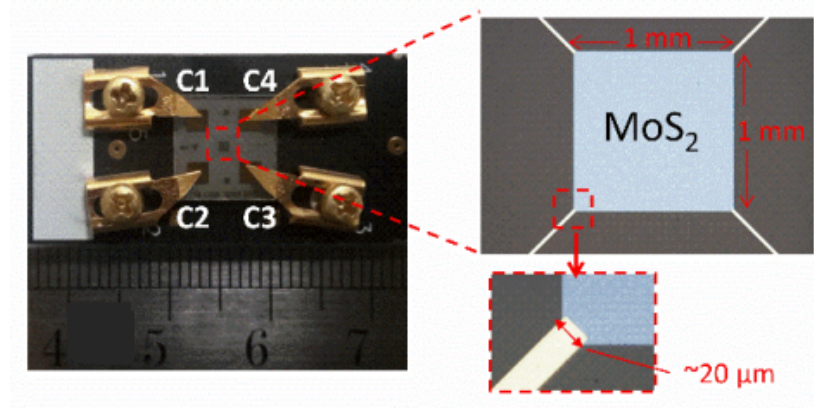
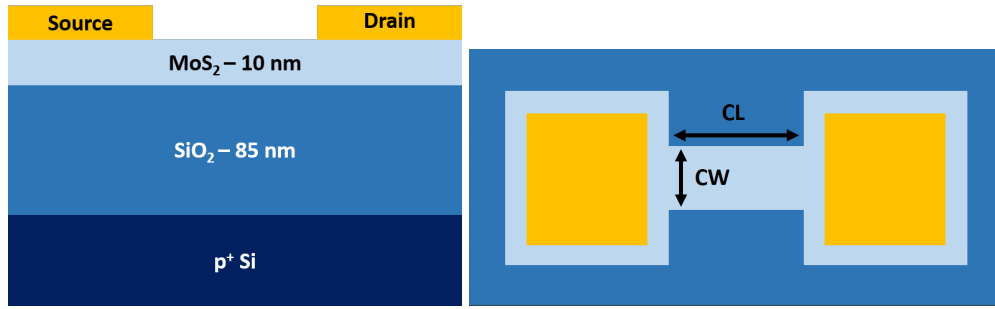


Figure 2.5: Cross sectional diagram of the MOSCAP device design. The bottom 2 layers represents the substrate material. The light grey is the p^{++} Si and green is the oxide layer of either Al_2O_3 and SiO_2 . Darker grey is MoS_2 or WS_2 . Yellow is the Ni/Au metal contact.

In chapter 4, for the 1 mm x 1 mm Van der Pauw (VdP) Hall devices, a SF_6 -based inductively coupled plasma (ICP) etch was used on the MoS_2 and metallised with Ni/Au tracks and pads and the design is seen in figure 2.6 (a). The same ICP etch process was used for the back-gated FET devices in chapter 4 and 6, as well as the same Ni/Au material for source and drain contacts. Figures 2.6 (b) and (c) depict the design. Dark blue is the substrate, blue is the oxide, light blue is MoS_2 and finally the orange shows each source and drain metal contacts. Figure 2.6 (c) shows a plan view of the back-gated transistor. Channel lengths were varied systematically throughout the mask. They ranged between $4\ \mu\text{m}$ and $60\ \mu\text{m}$. Channel widths were also varied within a similar range of $15\ \mu\text{m}$ to $50\ \mu\text{m}$. All masks were designed by Dr. Farzan Gity in Tyndall.



(a)



(b)

(c)

Figure 2.6: (a) Patterned 1 cm x 1 cm MoS₂ film on sapphire or *a* - Al₂O₃/sapphire with Ni/Au metal contacts. The zoomed-in inset shows the metal tracks going towards each of the 4 contact pads which forms a VdP structure. These measurements were done at room temperature. (b) Side-view of back gated transistors. This specific sample include 10 nm MoS₂, 85 nm SiO₂ and p⁺ Si but the design is the same throughout all samples. (c) Top view of back-gated transistors

Chapter 5 used a Circular Transmission Line Measurement (CTLM) setup. For general TLM structures, a 2 terminal setup with 3 or more contacts, can be used to extract both contact resistance and specific contact resistance. These parameter can be calculated using the relationship of the resistance and gap lengths between the contacts.[145] However, to combat possible current crowding, and to minimize processing steps, a circular TLM structure can be used. [146] In order to extract the total resistance, a correction must be used on the raw current-voltage measurements. This calculation is

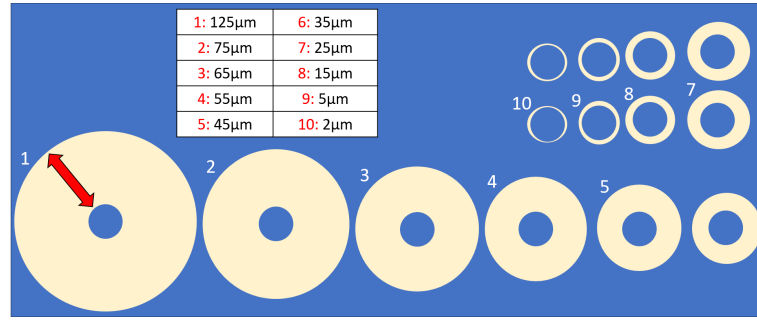
$$R_T = \frac{R_{sh}}{2\pi L} (d + 2L_T)C \quad (2.1)$$

where R_T is the total resistance, R_{sh} is the sheet resistance, L is the radius of the inner

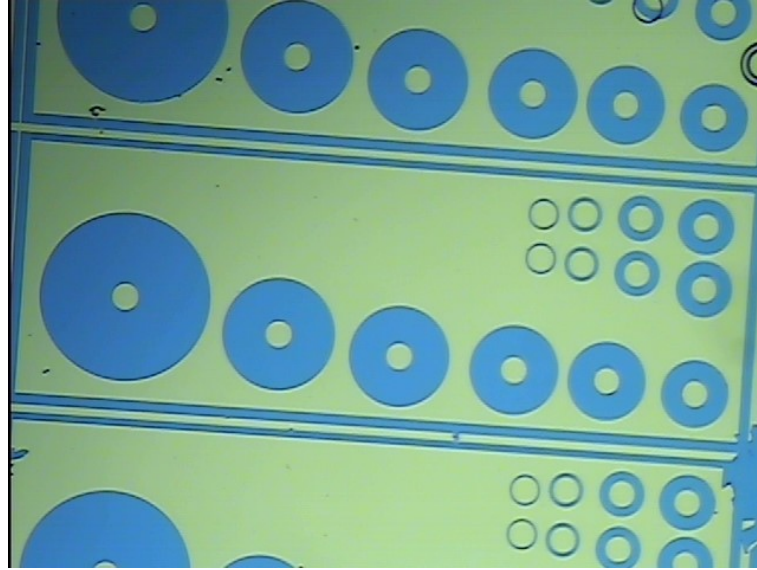
contact (stays constant at 25 μm), d is the changing gap width and C is the correction factor. The correction factor is given as

$$R_T = \frac{L}{d} \ln\left(1 + \frac{d}{L}\right) \quad (2.2)$$

The correction factor assumes that $L \gg d$. In our CTLM design, though this is true for some contacts, as seen in Figure 2.7 (a), it is not the case for others. A separate correlation test was done for the contacts with the larger d values and a straight line was found, therefore it was accepted that the assumption is valid for our results. Figure 2.7 (b) shows an optical image of the structures. The CTLM structures were fabricated by Dr. Farzan Gity and the analysis was done by me.



(a)



(b)

Figure 2.7: (a) Schematic diagram of CTLM structure. The radius (d) of the metal contact (red arrow) are labelled 1 to 10 as seen in the table. The inner radius (I) can be seen in blue in the middle of each circle. (b) Optical image of the CTLM structures on WS₂

2.6 Electrical Characterization using a Probe Station

For all current-voltage (IV) and capacitance-voltage (CV), test were done using a Cascade Mircotech probe station (model Submit 12971B) with an Attoguard Microchamber and -55°C to +100°C Shielded Chuck. Two semiconductor device analysers were connected - either an Agilent 4156A or an Agilent B1500A. Currents down to femtoamps can be detected. The largest range of voltages went between 0 V to +100 V and 0 V to -100 V. Before any measurements, a number of calibration tests were performed to ensure no leakage points and other sources of errors were present. This included

testing the cables, probe tips, probe tip holders, chuck and analysers. Once tested, IV and CV measurements could be performed. Chapter 3 includes many CV measurements. Both DC and AC voltage was used. It must be noted that this equipment does not directly measure capacitance. Instead, it measures impedance (ohms) and the phase angle (rads) and uses this information to calculate the capacitance. Figure 2.8 shows the relationship between these parameters. R is resistance, z is impedance, θ is phase angle, ω is angular frequency and C is capacitance. These measurements were carried out by myself, Dr. Gioele Mirabelli and Kimberley Intonti in Tyndall. Chapter 4, 5 and 6 also includes electrical measurements, all of which were carried out by me.

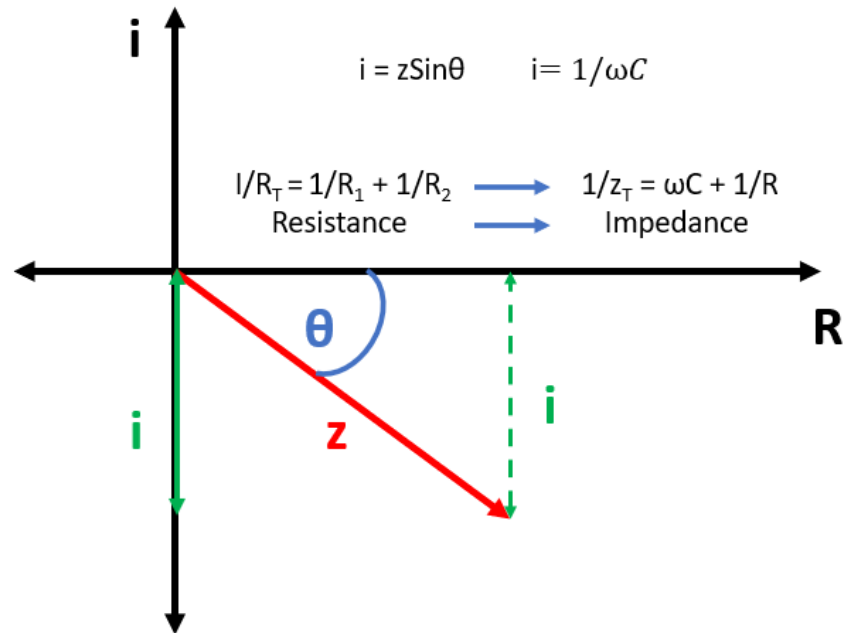


Figure 2.8: Relationship between impedance, phase angle, resistance and capacitance from probe station measurements.

2.7 Hall Effect

The Hall effect was first established by American scientist Edwin Hall in 1879.[147] The Hall effect results from the force on an electron when travelling in a magnetic field.[148] It is the combination of the flow of current through a conductive material in a magnetic field, thus creating a measurable potential difference.[149, 150] Figure

2.9 depicts this phenomenon. Hall measurements can help uncover various important information about conductive materials, including the dominant carrier type, the mobility and the carrier concentration.[149, 151]

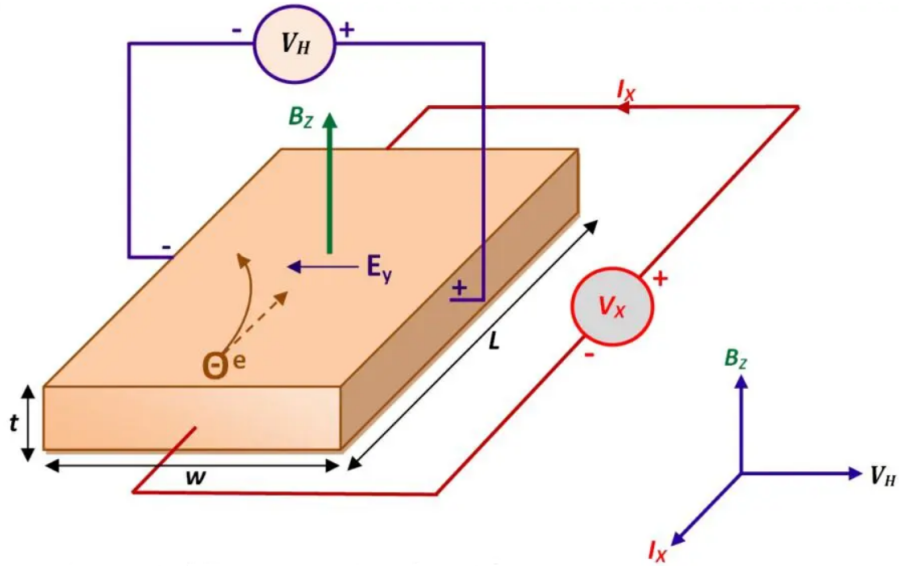


Figure 2.9: Schematic diagram showing the Hall effect. [149]

The Hall-effect, 4-point and 2-point resistance (Hall/4P/2P) measurements were performed in a LakeShore Model 8404 DC/AC Hall-Effect Measurement System fitted with a high resistance unit (up to 200 G Ω in DC mode). The Hall system uses all combined optimum methods available to calibrate and remove error components.[151, 152] Also, an InAs sample on the 2 and 4 point geometry was first tested to ensure system calibration prior to experimental testing. Sheet resistivity was measured from the 4P resistivity tests, where current reversal was performed to remove the thermal-electric voltage. The electromagnet can provide DC (up to ± 1.7 T) or AC (≈ 1.28 T RMS at a frequency of 50 mHz and ≈ 1.24 T RMS at 100 mHz) magnetic fields. Room temperature DC Hall-effect measurements (at the maximum of ± 1.7 T) gave the carrier type and sheet carrier concentration. Indium foil was put onto the gold probes and MoS₂ film to reduce contact resistance for the DC Hall/4P/2P measurements. All Hall measurements were performed by Scott Monaghan and I.

2.8 Raman Spectroscopy

Indian scientist, Raman, won the Nobel Prize in 1930 for the first observation of the inelastic scattering (Raman scattering) of light in organic liquids.[153] Raman spectroscopy is an analytical technique where a laser illuminates a material and the Raman scattered light is used to identify and interpret the compound.[154] When a monochromatic light hits a material, depending on the molecular structure, certain vibrations occur due to the increase in energy. The electrons absorb the light energy and are promoted to a higher state. In most cases, the energy is released and the electron return to the original state. This is known as elastic or Rayleigh scattering. However, if the electron returns to a different energy state, this is known as inelastic or Raman scattering. Due to this difference, the reflected light has a different wavelength to the incident beam, which can be used to identify the compound. If the electron returns to a lower energy state, it is called anti-stokes Raman and to a higher energy state, it is called Stokes Raman. This is visually depicted in figure 2.10 (a). MoS₂ and WS₂ share the same type of visible vibration modes, the out of plane $A_1(g)$ mode and in plane $E_2(g)$ mode, shown in figure 2.10 (b).

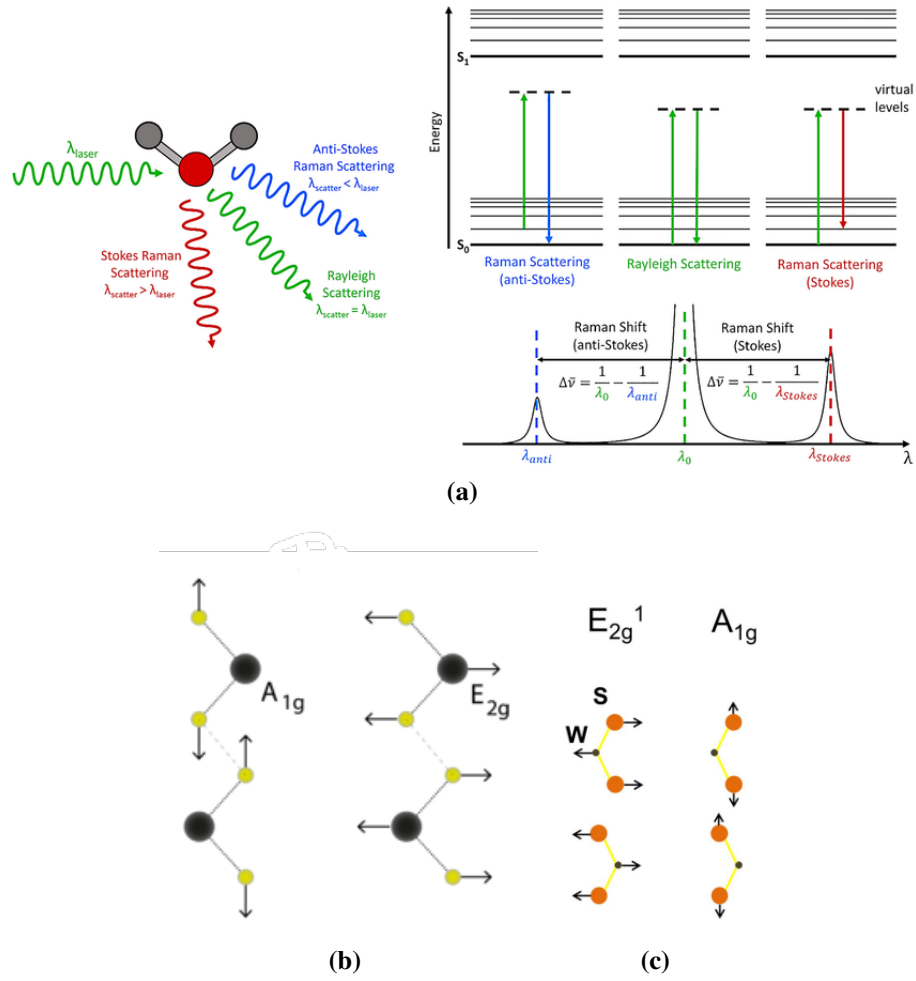


Figure 2.10: (a) Raman scattering and Rayleigh Scattering. [155] (b) Vibration modes of MoS_2 . [156] (c) Vibration modes of WS_2 . [157]

Raman spectroscopy was used in a number of chapters. In Chapter 4, two different separate Raman setups were used. One in Tyndall (myself), a Renishaw RAMAN inVia (Modu-514 nm laser) with a laser spot size was $\approx 5 \mu\text{m}$. The other was in Trinity College Dublin, on a WITec Alpha 300R with a 532 nm excitation laser. These measurements were performed in Trinity College Dublin. It will be specified in each chapter which system was used for a particular sample. Chapter 5 includes results from the Tyndall setup. Finally in chapter 6, Raman was also performed on 2 setups. A Thermo Fisher DXR2 confocal Raman microscope equipped with a 532 nm laser focused on a $1.1 \mu\text{m}$ diameter spot was used before device fabrication in the University of Padova. Post device fabrication, the measurements were performed by me on the

Tyndall Raman spectrometer. Wavenumbers below 200 cm^{-1} could not be tested.

2.9 Atomic Force Microscopy

Atomic force microscopy (AFM) is a type of scanning probe microscopy where a force-sensing cantilever is excited at a fixed frequency and the amplitude of oscillations can be used to define a sample's topography.[158] The introduction of the scanning tunnelling microscope by Binnig, Rohrer, Gerber, and Weibel in 1982 [159] revolutionised the world of microscopy. It was now possible to see a real image of materials at an atomic scale.[160] There are 3 main concepts involved with AFM - piezoelectric transducers, force transducers and feedback control.[161] The piezoelectric transducer oscillates the tip along the sample surface, the force transducer senses the forces between the cantilever tip and surface, then finally the feedback control takes that measured force and feeds that signal back to the piezoelectric transducer, keeping a constant force between the tip and sample.[161] Figure 2.11 shows a simplified version of what an AFM setup looks like.

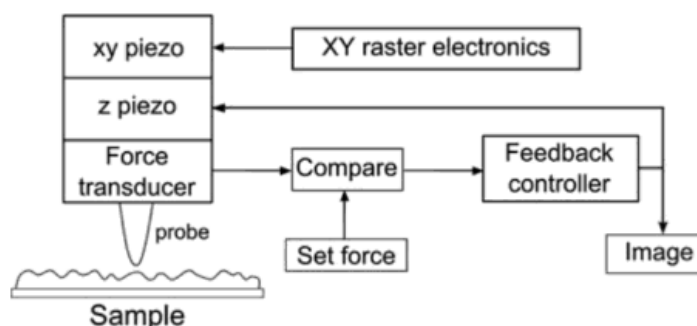


Figure 2.11: Schematic diagram of AFM setup.[161]

There are different ways in which an AFM instrument can be used. There are various static and dynamic modes, the choice depending on the material being investigated. For ALD grown WS_2 AFM data was acquired both pre and post metal processing using a Bruker Dimension Icon. Peak force tapping scanning with SCANASYST-AIR AFM probes was performed. These tests were performed in Tyndall by Gioelle Mirabelli

and I. For the laser annealed MoS₂ samples, a Veeco AutoProbe CP-II AFM was used, operating in non-contact mode using the PPP-NCHR probes supplied by Nanosensor. This was done in the University of Padova.

2.10 Transmission Electron Microscopy

Transmission electron microscopy is an analytical technique that can be used to understand crystalline structure, morphology and elemental information of materials.[162] In TEM, a high energy electron beam interacts with a thinned piece of a sample.[163] The reason an electron beam is used is because compared to light, the wavelength of the electrons is much smaller and hence can achieve much finer resolutions.[164] Figure 2.12 depicts the process, where an electron beam is emitted and condensed towards the specimen.[165] They interact and the resulting diffraction information and image is recorded. In order for the electrons to pass through the sample, a very thin 'lamella' of the sample must be made.

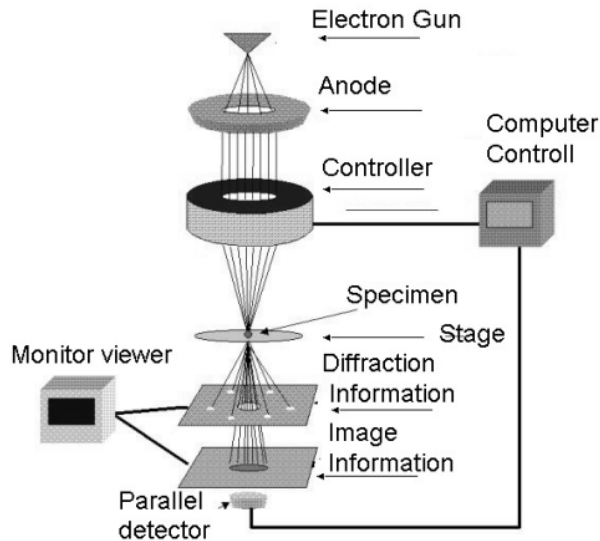


Figure 2.12: Schematic diagram of TEM setup.[165]

TEM results are discussed a number of times throughout this thesis. Excluding chapter 6, all TEM results used the same prep and execution performed by Dr.Farzan Gity in

Tyndall. Cross-sectional transmission electron microscopy samples were made using a dual beam focused ion beam FEI Helios Nano Lab 600i. 50 nm of carbon and 300 nm of platinum were deposited by e-beam evaporation, followed by deposition of a 2 μm carbon layer. This layer was used for sample protection before the milling process. The lamella was made to be less than 200 nm in thickness (final thinning at 93 pA 30 kV, final polish 2 kV 28 pA). Samples suitable for plan view TEM were formed by transferring MoS_2 from the substrate onto a TEM grid using 2 M sodium hydroxide solution. The floating MoS_2 film was then 'fished out' and put onto the TEM grid. TEM analysis was performed using a JEOL JEM-2100 at 200 kV in bright field mode. For chapter 6, energy dispersive x-ray (EDX) was also performed using this system. In chapter 6, TEM measurements were performed in the University of Limerick. A dual beam focused ion beam (FIB) FEI Helios NanoLab 600i was used to prepare lamellae. A 50/300 nm thick C/Pt stack was deposited followed by a 3 μ thick C layer with ion beam induced deposition. 30 kV Ga^+ ions was used to thin the lamellae. TEM was performed on a JEOL 2100 TEM operated at 200 kV and equipped with double tilt-holder and an energy dispersion X-ray (EDX) detector for chemical analysis.

2.11 Rutherford Backscattering Spectroscopy

Rutherford backscattering spectroscopy (RBS) is the analytical technique used to identify the distribution of elements in the surface region of a sample. [166] Named after New Zealand's Ernst Rutherford, RBS was first used for material analysis by Rubin et al in 1957. [167] For RBS, a sample is bombarded with ions and the charged particles displaced by the ions are recorded using a detector. [166, 168] In terms of applying this process to thin film characterisation, it provides quantification of the elements present in a thin film as well as their concentrations per unit area. Figure 2.13 depicts a basic schematic diagram of this phenomenon.[169]

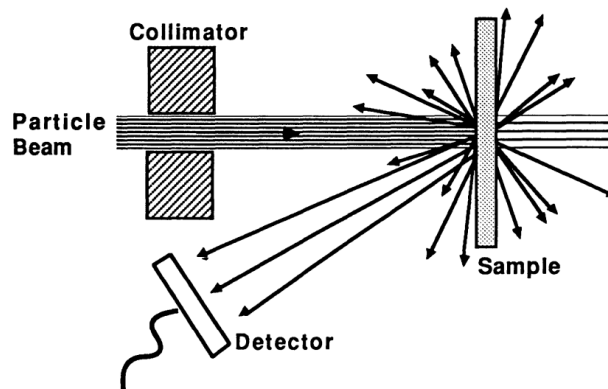


Figure 2.13: Schematic diagram of RBS.

RBS measurements were carried out to estimate the structural variation of S and Mo occurring in the samples grown on SiO_2 . A 2.0 MeV 4He^+ beam generated by the AN2000 accelerator at INFN-Laboratori Nazionali di Legnaro was used for RBS testing. The scattering angle was set to 160° . The sample was carefully moved in accordance with the low divergence beam using a high-resolution vacuum goniometer with an angular resolution of 0.01° . The RBS measurements were performed in the University of Padova.

2.12 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is an analytical technique that targets a sample with a monochromatic x-ray and measures the resulting kinetic energy of the displaced photoelectrons, depicted in Figure 2.14.[170] These values determine what elements are present and their chemical bonding/oxidation states. [170] For the usual x-ray energy used in XPS, the depth of penetration is several microns.[171]

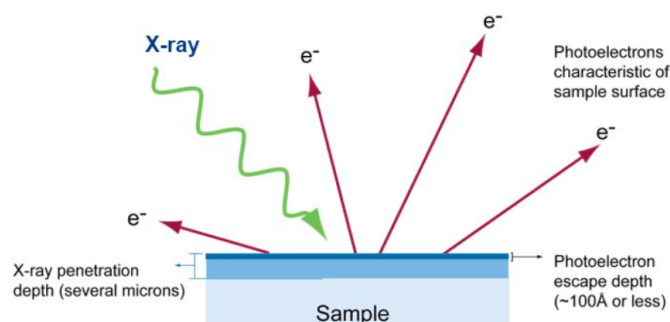


Figure 2.14: Schematic diagram of XPS.

X-ray photoelectron spectroscopy (XPS) spectra were recorded under ultra-high vacuum conditions ($< 10^{-8}$ mbar) using a VG Scientific ESCA^{lab} MkII system using Al K α x-rays and an analyser pass energy of 20 eV. Corelevel spectra were fitted with CasaXPS software using Gaussian-Lorentzian line shapes, after subtraction of a Shirley background and charge correction to the C 1s at 284.8 eV. Confirmatory spectra were gathered using monochromated Al K α x-rays from an Omicron XM1000 MkII x-ray source and an Omicron EA125 energy analyser. An Omicron CN10 electron flood gun was used for charge compensation.

Chapter 3

Investigating Interface States and Oxide Traps in Mechanically Exfoliated MoS₂/Oxide/Si and WS₂/Oxide/Si Systems

3.1 Introduction

In recent years 2D materials have featured prominently in research, as they exhibit energy gaps which span from semi-metals through to wide band gap semiconductors with potential applications including sensors, electronics, and flexible display technologies [172, 173]. In the area of insulating gate electronic devices, the 2D structure of the semiconductor has the potential to result in near ideal semiconductor/oxide interface properties [174], which is one of the main factors motivating research into MOSFET and tunnel FET devices based on 2D semiconductors. The application of multi-frequency capacitance and conductance measurements to investigate electrically active defects in MoS₂/oxide structures is a research area which has emerged in recent years [175–179], covering back-gated MoS₂ capacitors [175] and top-gated [176–179] MoS₂ MOSFETs. Our aim is to extend the study of back gated metal/MoS₂/oxide/Si MOS structures, where the MoS₂ or WS₂ layer is thicker than the maximum depletion width. The results from separate processes, combining experimental data and physics-based AC simulations, all indicate that while close to ideal properties can be achieved, there is evidence of defects in the MoS₂ or WS₂ close to the TMD/oxide interface.

The study also investigates WS₂ flakes. The transition metal dichalcogenide WS₂ has been actively researched for many years, in some cases through fundamental precursor chemistry or synthesis material studies [180–183] or with a specific application area in mind such as lubricants, [184–187] batteries, [188, 189] photovoltaics, [190] sensors, [191] opto-electronics, [192] or catalysis [62]. In relation to nanoelectronic applications, WS₂ is of particular interest due to its semiconductor nature and indirect bandgap, in the order of 1.3-1.4 eV in bulk form [193–196]. The possibility of fabricating field-effect-transistors (FETs), and complementary-metal-oxide-semiconductor (CMOS) circuits has stimulated research into this exciting TMD material.

The approach used in this study to examine the interface properties of WS₂ or MoS₂ and insulating oxides is the use of an inverted MOSCAP (metal oxide semiconductor capacitor) structure, where a heavily doped silicon substrate is used as the back gate. The silicon has an oxide on the surface, onto which the WS₂ or MoS₂ is transferred by mechanical exfoliation. The top surface of the WS₂ or MoS₂ is metallised, resulting in an inverted MOSCAP structure. The inverted MOSCAP structures are examined through current-voltage characterization and multi-frequency capacitance-voltage and conductance-voltage characteristics to examine the electronic properties of the WS₂/oxide and MoS₂/oxide interfaces.

3.2 MoS₂ and WS₂ crystals

Assuming that CVD will eventually produce high quality crystalline films, the resulting characteristics of the TMD/oxide/substrate interfaces must be investigated. As an ideal large scale CVD process has yet to be found, the next highest quality TMD materials available come in the form of crystals. They are either grown by high temperature chemical vapour transport [197] or found naturally in nature. This study utilises natural MoS₂ and WS₂ crystals bought from HQ Graphene. Figure 3.1 (a) shows 2H MoS₂, provided by HQ Graphene. MoS₂ has a monolayer band gap of ≈ 1.8 eV, an indirect bulk band gap of ≈ 1.2 eV and a charge carrier density of $\approx 10^{15} \text{ cm}^{-3}$ at room temperature [198]. Both n-type and p-type crystals were available. Figure 3.1 (b) shows 2H WS₂, provided by HQ Graphene. It has an indirect bandgap of ≈ 1.3 eV and a charge carrier density of $\approx 10^{14} \text{ cm}^{-3}$ at room temperature [199]. The free carrier density values calculated in this chapter were higher than the values of 10^{15} cm^{-3} and 10^{14} cm^{-3} quoted by the manufacturers, which will be discussed later in this chapter. These crystals were then mechanically exfoliated onto various substrates.

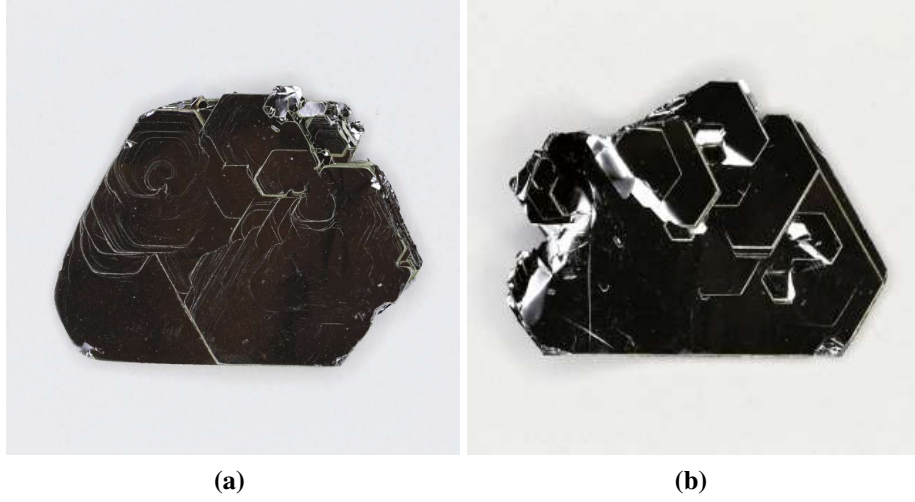


Figure 3.1: (a) Natural MoS₂ crystal from HQ Graphene. [198] (b) Natural WS₂ crystal from HQ Graphene [199].

3.3 Experimental Case Studies & Results

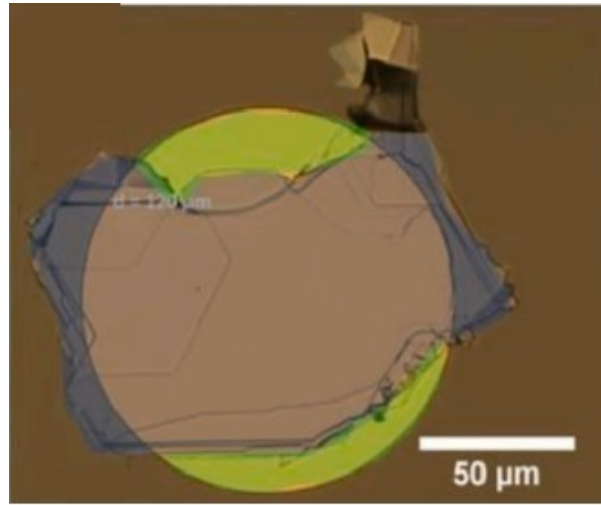
The Experimental procedures are discussed in the methodology chapter. The results in this chapter span across 5 separate devices, each one differing in substrate, TMD and etching process. Figure 3.2 displays the 5 samples tested. The first case study investigates AuNi/MoS₂/Al₂O₃/p⁺Si. Note, this sample was made by Gioele Mirabelli, a then PhD student in Tyndall. UT Dallas were collaborators with this sample and were responsible for the AC simulations. The MoS₂ flake was not etched. The rest of the samples were exfoliated and fabricated by Farzan Gity and I. Electrical tests were done by Kimberley Intonti and I. The second case study sample investigates AuNi/MoS₂/SiO₂/p⁺Si where the MoS₂ was not etched. The third investigates AuNi/MoS₂/Al₂O₃/p⁺Si where the MoS₂ was not etched. The fourth investigates AuNi/MoS₂/Al₂O₃/p⁺Si where the MoS₂ was etched. The area of the flake equals that of the metal contact. Finally, the fifth case study investigates AuNi/WS₂/Al₂O₃/p⁺Si where the WS₂ was etched.

Metal Contact	TMD	Oxide	Substrate
<u>AuNi</u>	MoS ₂	Al ₂ O ₃	p ⁺ Si
<u>AuNi</u>	MoS ₂	SiO ₂	p ⁺ Si
<u>AuNi</u>	MoS ₂	Al ₂ O ₃	p ⁺ Si
<u>AuNi</u>	MoS ₂	Al ₂ O ₃	p ⁺ Si
<u>AuNi</u>	WS ₂	Al ₂ O ₃	p ⁺ Si

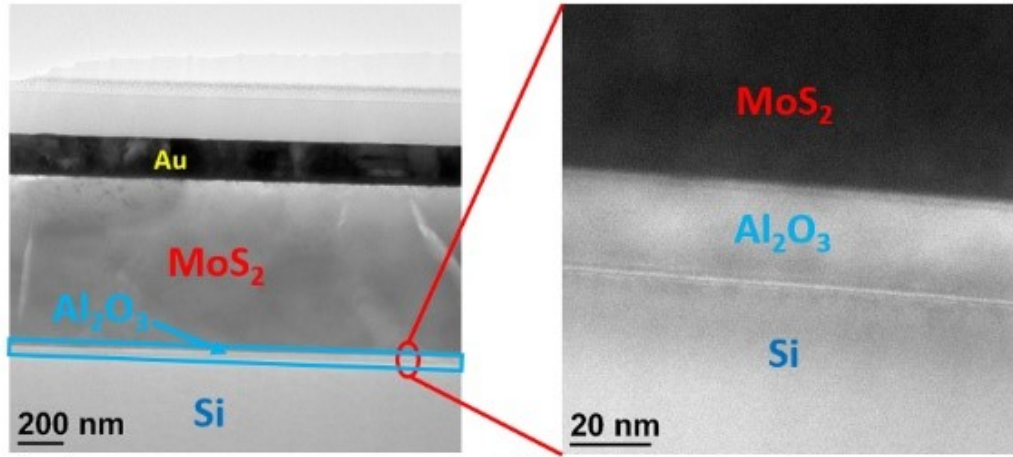
Figure 3.2: Table of each sample investigated.

3.3.1 Case Study 1: AuNi/MoS₂/Al₂O₃/p⁺Si

Figure 3.3 (a) shows an optical image of an inverted AuNi/MoS₂/Al₂O₃/p⁺Si MOS capacitor. The structure was formed based on mechanical exfoliation of highly crystalline MoS₂ and subsequent transfer to the Al₂O₃ (23 nm)/p⁺Si substrate. Contrary to what one may immediately think when looking at this image, the circular metal contact is on top of the flake, not below. Figure 3.3 (b) shows a TEM image of the AuNi/MoS₂/Al₂O₃/p⁺Si structure with a close up of the interfaces between MoS₂/Al₂O₃ and Al₂O₃/p⁺Si. The Ni (5 nm)/Au (160 nm) metal contact was aligned with the 728 nm MoS₂ flake by optical inspection, with no subsequent processing prior to electrical measurements.



(a)



(b)

Figure 3.3: (a) Optical picture of the device showing the metal in contact with (green) the Si/Al₂O₃ substrate and (blue) the MoS₂. (b) Cross sectional TEM of the structure, with a zoomed in image of the MoS₂/Al₂O₃/Si region.

A multi-frequency CV measurement was conducted on the AuNi/MoS₂/Al₂O₃/*p*⁺Si structure. The voltage was applied to the silicon substrate and the gate contact was grounded, ie the device was back-gated. The voltage range was performed between -9 V to +5 V. The response is shown in Figure 3.4. The behaviour of the CV response in the depletion region shows negligible which suggests a very low density of electrically active interface defects (D_{it}). The CV response is shifted along the gate axis towards negative voltage, indicating the presence of fixed oxide charges in the oxide or at

the oxide/MoS₂ interface. The negative shift in the CV response yields a net fixed oxide charge density of $8.3 \times 10^{12} \text{ cm}^{-2}$ (+ve), assuming all the fixed oxide charge is located at the MoS₂/Al₂O₃ interface. The fixed oxide charge density is determined based on the shift of the flat band voltage from the ideal value. This positive charge is typically observed for ALD grown Al₂O₃ prior to H₂/N₂ annealing, and the density value obtained is consistent with other ALD grown films with a thickness around 24 nm [200].

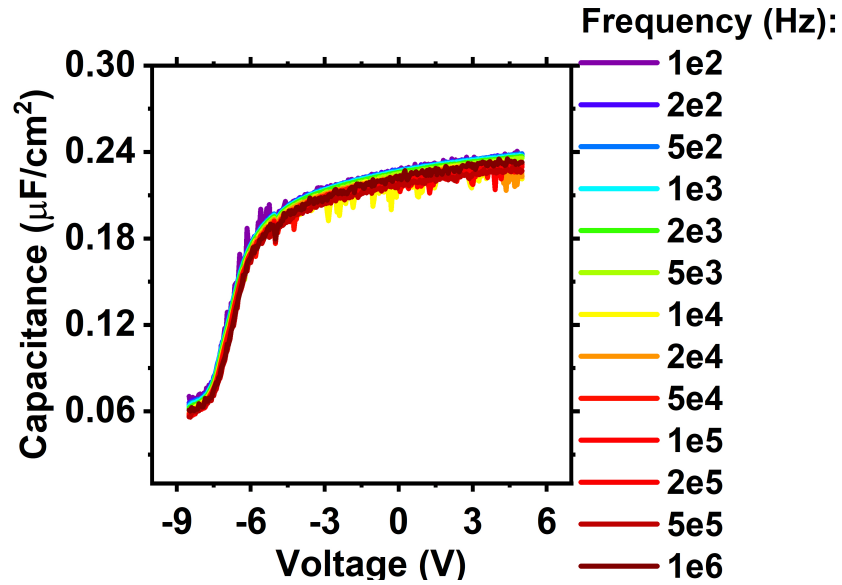
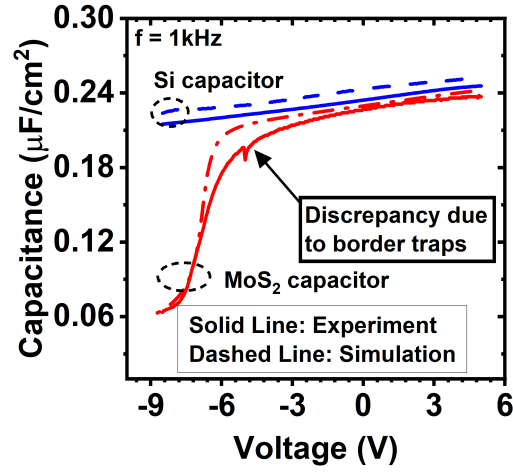


Figure 3.4: Experimental multi-frequency CV response of the NiAu/MoS₂/Al₂O₃/p⁺Si. CV was recorded at room temperature

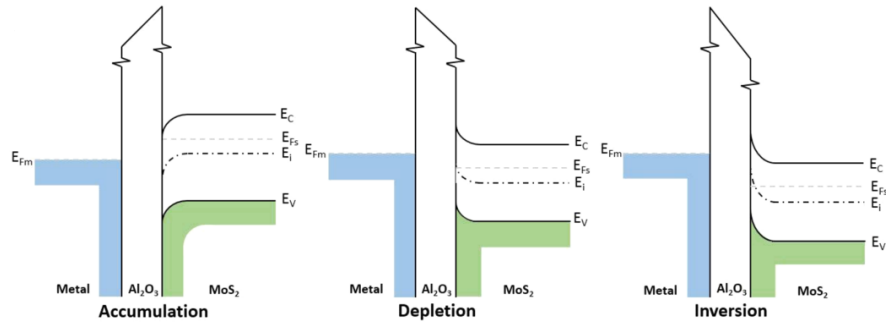
Along with the experimental data, physics-based AC simulations of the CV response based on TCAD software (Sentaurus Device Manual: L-2016.03-SP2) were also investigated. Figure 3.5 (a) shows the 1 kHz CV response for the case of the reference AuNi/Al₂O₃/p⁺Si structure (blue) and the 1 kHz CV plot of the AuNi/MoS₂/Al₂O₃/p⁺Si structure (red). The dashed lines are physics-based AC simulations of the CV response and solid lines are the experimental results. The availability of the reference structure, with no MoS₂, allows a determination of the doping concentration in the p⁺ silicon, which can subsequently be used in the simulation of the full AuNi/MoS₂/Al₂O₃/p⁺Si structure. From the reference structure

(AuNi/Al₂O₃/p⁺Si), a boron doping concentration in the Si of $3 \times 10^{19} \text{ cm}^{-3}$ is obtained, consistent with the p⁺ wafer resistivity range of 1×10^{-2} to $2 \times 10^{-3} \text{ }\Omega\text{cm}$. For these simulations of the reference structure, the Al₂O₃ thickness is 23 nm (from TEM), with a dielectric constant of 6.5.

The MoS₂ parameters used in the simulations were: energy gap = 1.20 eV, electron affinity = 4.5 eV, electron effective mass = 0.57, hole effective mass = 0.8. The carrier density versus Fermi energy was taken from [201]. Fitting of the simulated CV response to the experimental response yielded an n-type doping concentration in the MoS₂ of $1.75 \times 10^{17} \text{ cm}^{-3}$. The effective fixed positive charge in the Al₂O₃, had an equivalent value of $8.3 \times 10^{12} \text{ cm}^{-2}$ (+ve) located at the MoS₂/Al₂O₃ interface. It is noted that while the MoS₂ crystal used for the mechanical exfoliation was not intentionally doped, Hall analysis performed on the starting bulk crystal [151] yielded an n-type semiconductor with a doping concentration of $\approx 10^{17} \text{ cm}^{-3}$ consistent with the value extracted from fitting the experimental CV response. The presence of interface states was excluded from simulations. From Figure 3.5 (a), one can see close correlation between the simulated and experimental slopes. However there is an unexpected feature at -5 V with the exfoliated flake. Caruso et al. investigated the possible effects of oxide defects as border traps in a InGaAs MOS system.[202] There, a 'hump' feature was also present and when they included the presence of oxide traps in the simulated CV curve, it matched that of the experimental CV slopes. Since our samples are mechanically exfoliated MoS₂ crystals, as well as being stored in air, it would not be surprising if some border traps exist in the form of oxide traps. This feature is in the region where the Fermi level at the surface of the oxide reaches the MoS₂ conduction band edge. This depletion region can be visualised in terms of a band diagram in Figure 3.5 (b), along with the regions of accumulation and inversion.[178] We propose that our feature is likely due to oxide defects (border traps) in the Al₂O₃ layer. [202, 203]



(a)



(b)

Figure 3.5: (a) 1 kHz CV responses of NiAu/MoS₂/Al₂O₃/p⁺Si structure and the reference AuNi/MoS₂/Al₂O₃/p⁺Si structure. The dashed lines are the physics based AC simulations of the structure and solid lines are the experimental results. (b) Schematic band diagrams of accumulation, depletion and inversion regions for a n-type MoS₂ and Al₂O₃ MOS system.[178]

3.3.2 Case Study 2: AuNi/MoS₂/SiO₂/p⁺Si

Further studies were performed to understand the electrical behaviour of exfoliated MoS₂ on heavily doped SiO₂ (10 nm)/p⁺Si. The process began with a synthetic MoS₂ crystal, provided from HQ Graphene as seen in Figure 3.6. The scratches seen on the contacts are from probing tests. These flakes were not etched. Again, the voltage was applied to Si substrate, creating a back-gated device.

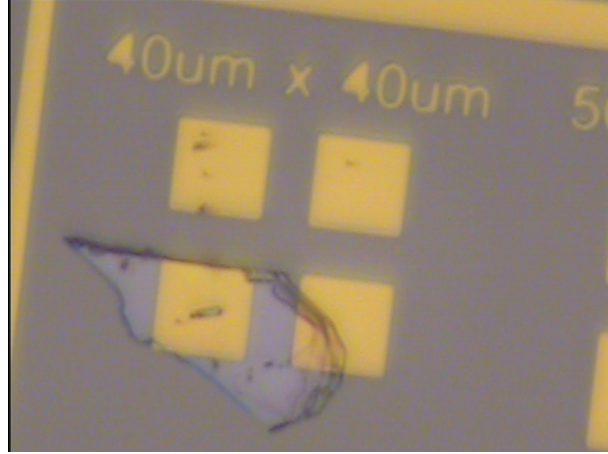


Figure 3.6: 40 μm x 40 μm capacitor (Ni5 nm/Au 160 nm) patterned onto a mechanically exfoliated MoS_2 flake on SiO_2 (10 nm)/ $p^+\text{Si}$. Note, the image was taken after some probing tests hence the scratch seen on the contacts.

The multi frequency CV as shown in Figure 3.7 (a), highlights a possible effect when the dimensions of the flake exceed the dimensions of the metal contact. Multi-frequency CV double sweeps in the range of 1 kHz to 1 MHz were performed between -3 V and $+3\text{ V}$. In this case, the CV responses are double sweep hysteresis curves with no hold time in the accumulation region ($+3\text{ V}$) of the SiO_2/Si and the $\text{MoS}_2/\text{SiO}_2$ interfaces. The expected maximum capacitance, based on the metal contact area of the $40\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$ square, is $5.52 \times 10^{-12}\text{ F}$ and is shown as a dashed line in Figure 3.7 (b). However, as seen in the CV plot, at low frequencies, the experimental maximum oxide capacitance is much higher. It is theorised that the entire flake is also involved in the CV sweep. This was investigated using the following set of calculations. First, the C_{ox} per unit area was determined with the equation below

$$C_{ox} = \frac{\epsilon_0 \epsilon_{\text{SiO}_2}}{t_{ox}} \quad (3.1)$$

Where C_{ox} is the oxide capacitance per unit area. ϵ_0 is vacuum permittivity ($8.85 \times 10^{-12}\text{ F m}^{-1}$), ϵ_{SiO_2} is the permittivity of SiO_2 (3.9) and t_{ox} ($1 \times 10^{-9}\text{ m}$) is the oxide thickness. This gave a C_{ox} per unit area of $3.45 \times 10^{-3}\text{ F m}^{-2}$. The metal contact was $1.6 \times 10^{-9}\text{ m}^2$. In total, the area of the flake was found to be ≈ 2.5 the size of a single

40 μm x 40 μm metal contact site, which gives an area of $\approx 4 \times 10^{-9} \text{ m}^2$ for the flake. This area was multiplied by the C_{ox} per unit area to give a maximum oxide capacitance of $1.38 \times 10^{-11} \text{ F}$. At AC signal frequencies from 1 kHz to approximately 100 kHz it is proposed that rather than just the metal contact, the electrons can follow the AC signal throughout the entire MoS_2 flake. Therefore, the maximum capacitance is defined by the area of the flake as opposed of the metal contact area. Based on an estimated flake area of $4 \times 10^{-9} \text{ m}^2$, the expected maximum capacitance value is $1.38 \times 10^{-11} \text{ F}$ and the experimental data showed the maximum capacitance to be $1.46 \times 10^{-11} \text{ F}$. These values are in much better agreement and therefore it is proposed that both the metal contact and flake are involved in the CV sweep.

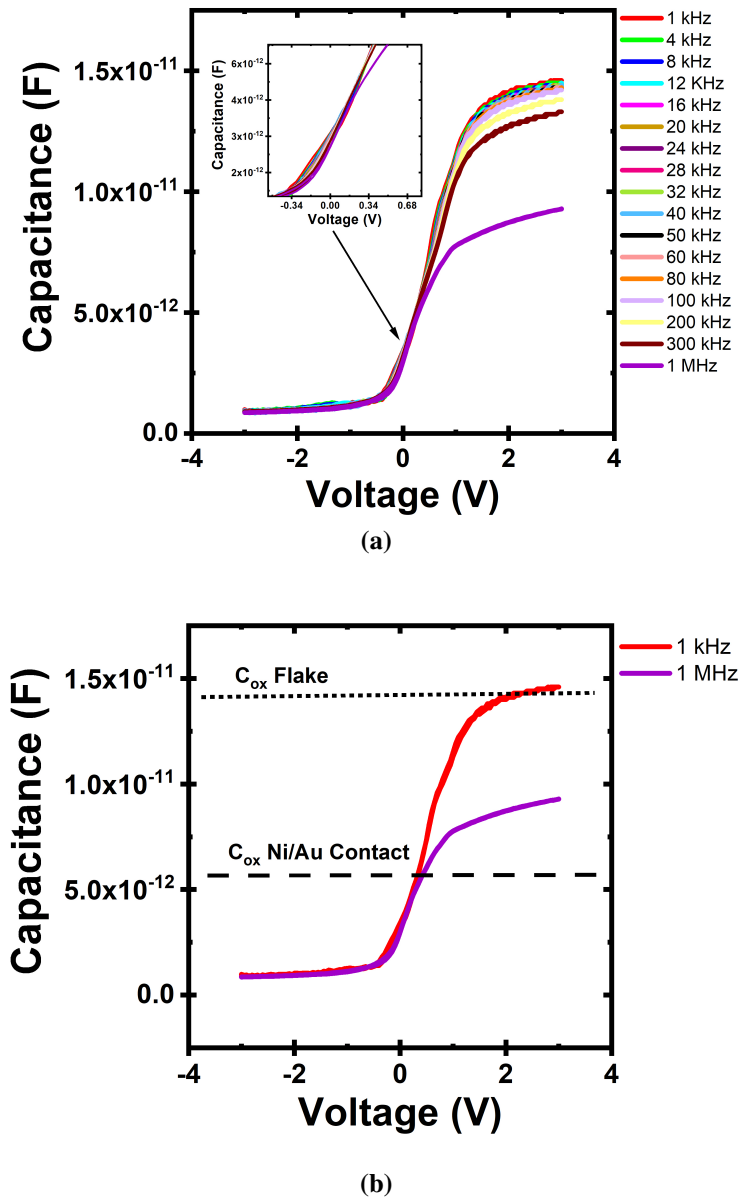


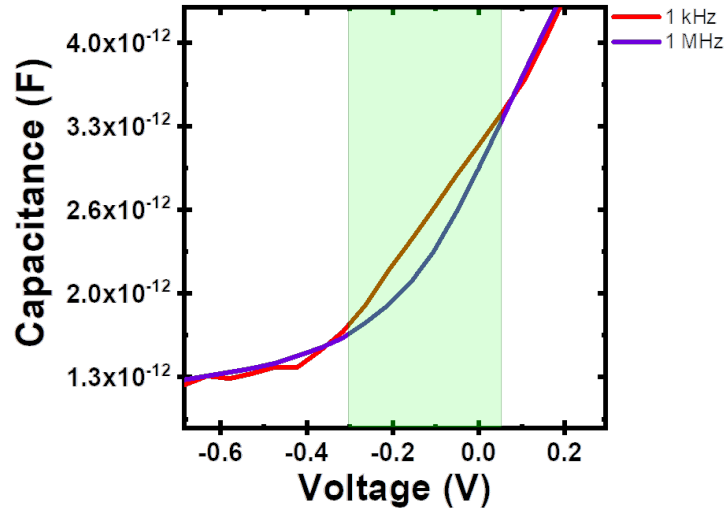
Figure 3.7: (a) Experimental multi-frequency CV response of NiAu/MoS₂/Al₂O₃/p⁺Si. CV was recorded at room temperature. The inset shows the negligible hysteresis in the depletion region. (b) The CV response at 1 kHz and 1 MHz with the expected maximum capacitance shown as a dotted line for the cases where the area is defined by the Ni/Au contact and where the area is defined by the MoS₂ flake.

The results show a frequency dependence between 1 kHz and 1 MHz. Negligible hysteresis during each double sweep was found, as highlighted in the inset in Figure 3.7 (a). Looking closely at the plot, the presence of slight frequency dispersion between the lowest and highest frequencies can be seen. Using the High - Low CV technique

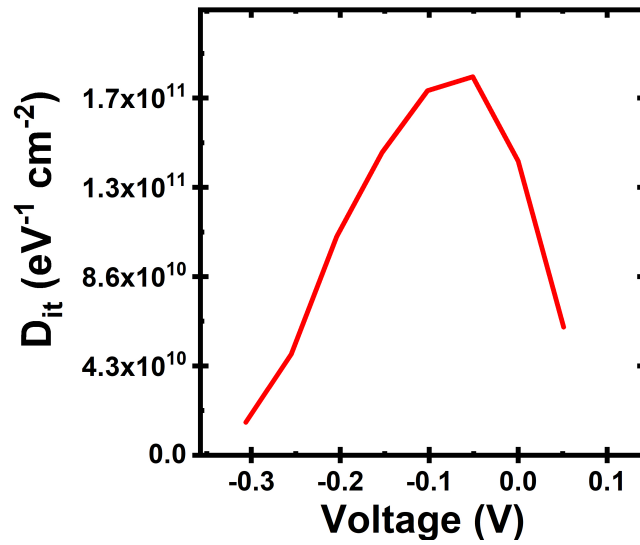
[204], the density of interface states within the highlighted area in figure 3.8 (a) was calculated. The High - Low equation was used to calculate the density of interface states.

$$D_{it} = \left(\frac{1}{q}\right) \left(\frac{C_{ox}C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{ox}C_{HF}}{C_{ox} - C_{HF}} \right) \quad (3.2)$$

where D_{it} is the density of interface states, q is the charge of an electron, C_{ox} is the maximum oxide capacitance of the Au/Ni metal contact area, C_{LF} is the capacitance of the lowest frequency (1 kHz) and C_{HF} is the capacitance of the highest frequency (1 MHz). The forward sweep (-3 V to +3 V) of the double CV sweep was used to investigate this phenomenon. Figure 3.8 (b) shows the D_{it} within the area of frequency dispersion. This data shows that there are two factors influencing the AuNi/MoS₂/oxide CV interface behaviour. These factors are area of the flake and the presence of defect states at the interface causing frequency dispersion as seen in Figure 3.8 (b). It must be noted that this is a potential source of error. This equation requires the capacitance to be normalised as a function of area. With this sample, we know that the charge is distributed past that of the metal contact and throughout the rest of the MoS₂ flake. Therefore, we cannot definitely state that the area at the lowest and highest frequencies are the same. However, when the carrier density at the surface is low, ie in depletion, the area effect is small. This is because the density of electrons in the conduction band is low. When looking at Figure 3.7 (b) the curves diverge with frequency when the capacitance is larger than the nominal oxide capacitance. For this reason, though the D_{it} value may not be exactly correct, it gives an approximation.



(a)



(b)

Figure 3.8: (a) Zoom in of the -3 V to +3 V section of the double sweep CV plot for both 1 kHz and 1 MHz. The area highlighted in green shows the area of frequency dispersion and these voltage and capacitance values were used in the High - Low CV calculations between -0.3 V and +0.1 V. (b) The density of interface states between the highest and lowest frequency as a function of voltage.

3.3.3 Case Study 3: AuNi/MoS₂/Al₂O₃/p⁺Si

The same exfoliation and device patterning process were performed with n-type MoS₂ on 20 nm Al₂O₃ on p⁺Si. Again, the area of the metal contacts were 40 μm x 40 μm as seen in Figure 3.9.

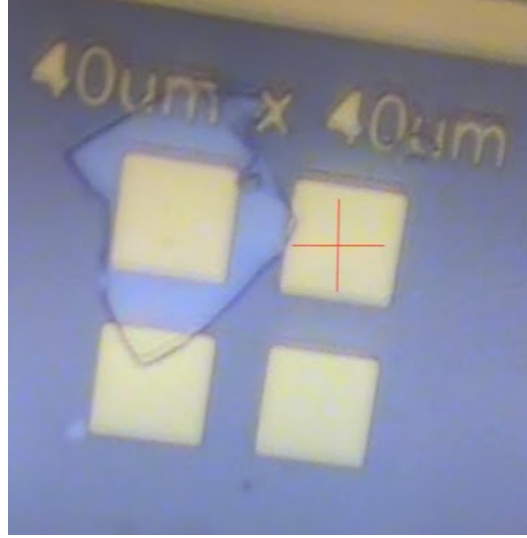


Figure 3.9: $40\ \mu\text{m} \times 40\ \mu\text{m}$ capacitors (Ni5 nm/Au 160 nm) patterned onto a mechanically exfoliated MoS_2 flakes on Al_2O_3 (20 nm)/ $p^+\text{Si}$.

The same process was repeated with exfoliated MoS_2 on Al_2O_3 , with the C_{ox} calculation. The oxide had a permittivity of 8 and thickness of 20×10^{-9} nm. However, the behaviour did not mirror that from exfoliated MoS_2 on SiO_2 as discussed directly above. A further investigation was needed to understand the difference in behaviour. The area instead covers one $40\ \mu\text{m} \times 40\ \mu\text{m}$ Au/Ni contact as seen in Figure 3.9. The theoretical C_{ox} was calculated to be approximately 1.53×10^{-11} F from a flake size of ≈ 2.5 sites. A double multi-frequency CV sweep was performed between -4.5 V and +3 V, shown in Figure 3.10. As seen in the inset, again, there was negligible hysteresis in the depletion region. A small hump can be seen at ≈ -3.5 V for all frequencies. This feature is even more present in the next Case Study (Figure 3.13). Takenaka et al also observe this hump-like feature with their exfoliated MoS_2 CV plots.[175] They attribute these characteristics to interface trap responses, which is what we theorise is also the case here. Though we do not see hysteresis, since the crystal was mechanically exfoliated, it makes sense that some defect traps are present at the interface.

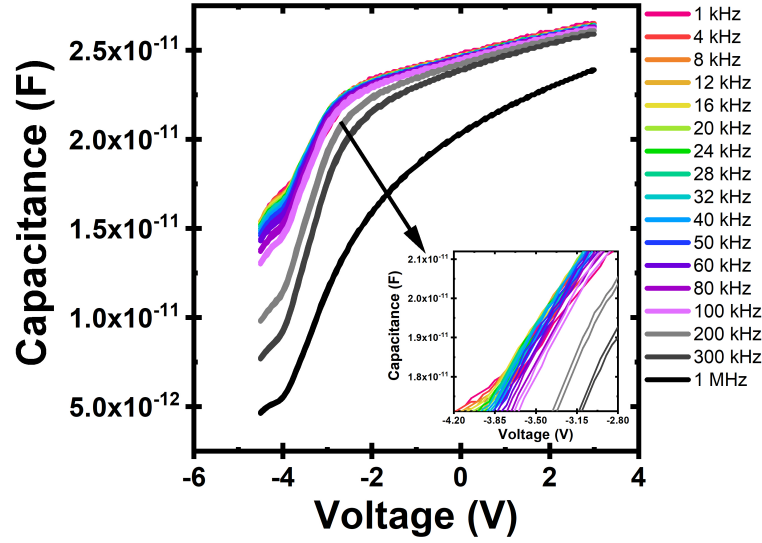
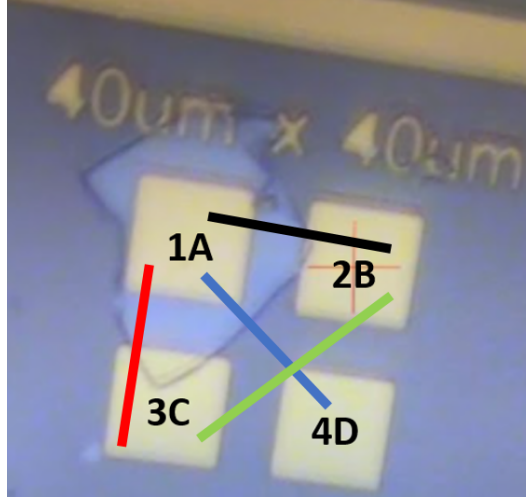
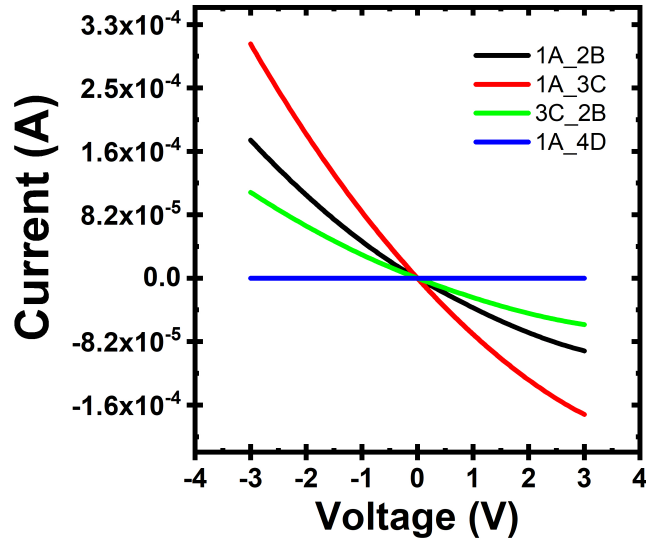


Figure 3.10: Experimental multi-frequency CV response of the NiAu/MoS₂/Al₂O₃/p⁺Si. CV was recorded at room temperature. The inset shows the negligible hysteresis in the depletion region.

In the previous sample, it was only the area of the flake that was involved in the increase of the effective area at low AC signal frequencies. However, here, the value seemed to give a value of maximum capacitance based on a larger area. It is proposed that with this sample, if a piece of the flake was touching a metal contact, that entire contact was also involved in the CV response. To investigate this behaviour, a series of simple IV tests were done. Four IV tests took place with probe tips placed between contacts 1A - 2B (black), 1A - 3C (red), 2B - 3C (green) and 1A - 4D (blue) as seen in Figure 3.11 (a). It is clear from Figure 3.11 (b) that metal contacts 2B and 3C are electrically connected. The effective area calculation was changed accordingly to include to the area of the flake plus the 3 metal contacts (≈ 4.5 sites). The result gives a value of 2.55×10^{-11} F. Now, comparing the experimental max C_{ox} of 2.65×10^{-11} F and the updated theoretical value, this shows that the entire metal contacts were activated, even if the flake was only partially covering the contact. This behaviour is opposite to the behaviour seen in Case Study 2, where only the flake and fully covered metal contact are electrically active. We theorise that the adhesion of the flake onto each contact affects whether that contact will be involved in the CV sweep.



(a)



(b)

Figure 3.11: (a) Top view optical image of the AuNi/MoS₂/Al₂O₃/p⁺Si structure where the Ni(5 nm)/Au(160 nm) contacts. Black, red, green and blue lines represent the individual IV tests done between the contacts. (b) IV behaviour of the 4 paths between contacts.

3.3.4 Case Study 4: Etched AuNi/MoS₂/Al₂O₃/p⁺Si

The mechanical exfoliation of AuNi/MoS₂/Al₂O₃/p⁺Si matched those previously mentioned. However, in this case study, the Ni(5 nm)/Au(160 nm) metal was used as a hard mask during reactive ion etching of the MoS₂ (the MoS₂ flake averaging ≈ 350 nm in height) on doped Al₂O₃ (20 nm)/p⁺Si. This approach allows a well-defined area of MoS₂ in the capacitor structure. An image of the initial flake outline is still

visible, due to the height difference (MoS_2 and Al_2O_3) during the etch process.

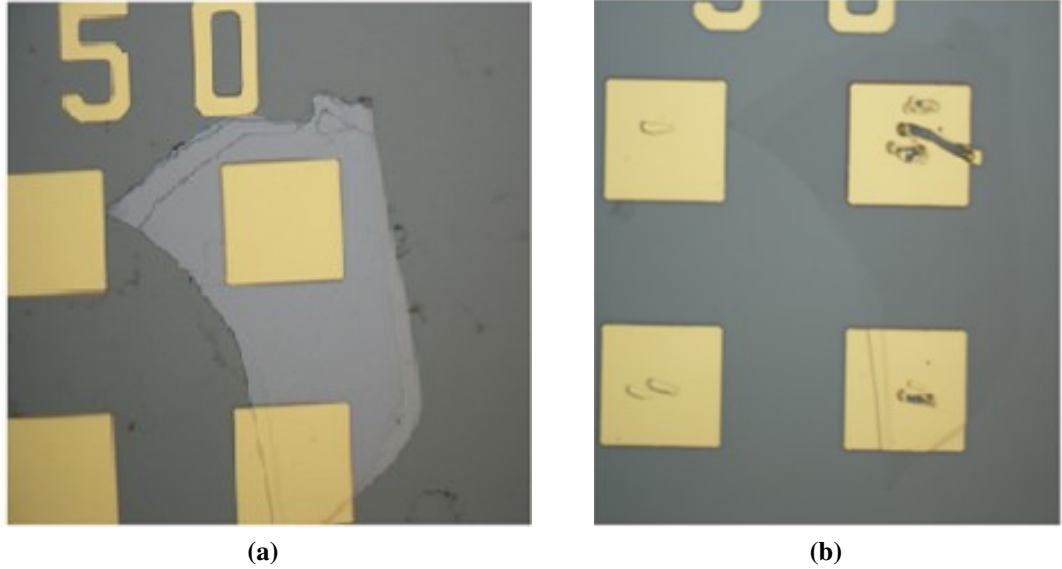


Figure 3.12: (a) Top view optical image of the $\text{AuNi}/\text{MoS}_2/\text{Al}_2\text{O}_3/p^+\text{Si}$ structure where the $\text{Ni}(5\text{ nm})/\text{Au}(160\text{ nm})$ contacts and the MoS_2 flake are both visible, (b) the same structure after reactive ion etching of the MoS_2 layer using the Ni/Au as a hard mask. Note that an impression remains of the original flake position due to the height differences during the reactive ion etching. The marks on the Ni/Au pads are probing marks.

Following the etching process, Figure 3.13 demonstrates another close agreement between the theoretical maximum C_{ox} of $7.75 \times 10^{-12}\text{ F}$ and the experimental values. Between -2 V and -3 V some frequency dispersion is noted. Hysteresis is also present during the double sweep, suggesting charges are getting trapped at the semiconductor/oxide interface. We propose that the emergence of hysteresis in this etched sample, as opposed to the previous non etched sample, could be due to the exposed edges of the flake post etching. The same may be true for the etched WS_2 sample below. Future work into the impact of perimeter/area capacitors would help uncovering the effects of etching on hysteresis.

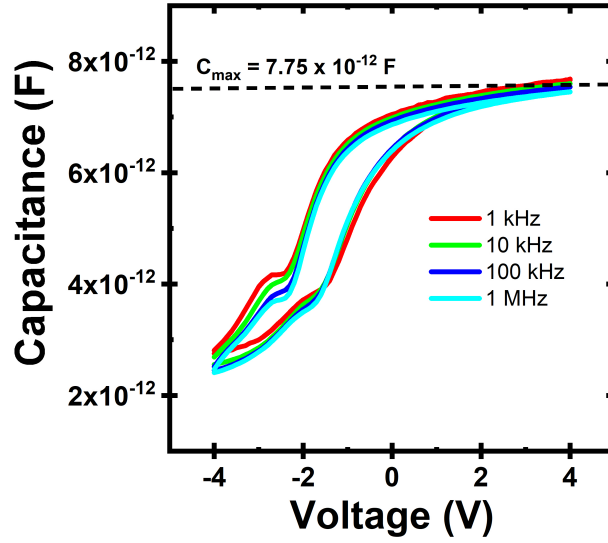


Figure 3.13: Experimental multi-frequency CV response of the AuNi/MoS₂/Al₂O₃/p⁺Si. CV was recorded at room temperature and the double sweeps were performed from -4 V to +4 V back to -4 V. The CV in forward bias demonstrates some CV dispersion at the hump-like feature between ≈ -2 V to -3 V. Hysteresis is also present during the double sweep.

3.3.5 Case Study 5: Etched AuNi/WS₂/Al₂O₃/p⁺Si

For the final case study, there is a change in TMD. The experimental process was almost identical to that used for the MoS₂ samples with the only difference being the use of a bulk WS₂ crystal. The WS₂ flake thickness was measured to be 460 nm. The sample was then etched after metal deposition, using the metal as a hard-mask. This ensured a definite area of WS₂. (ie. 40 μ m x 40 μ m) Figure 3.14 shows the flake both pre AuNi metal patterning (a) and post AuNi metal patterning (b) on 20 nm Al₂O₃ on p⁺Si.

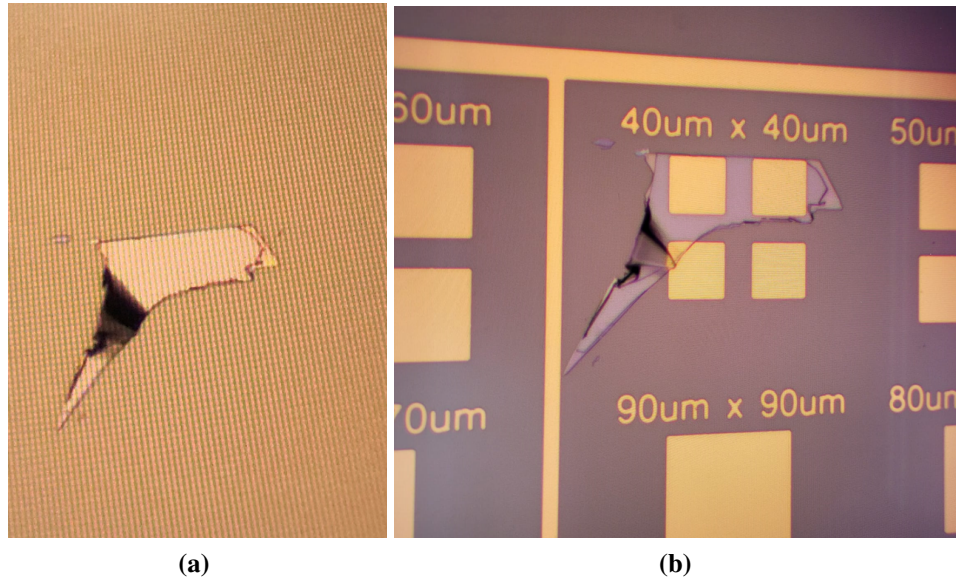
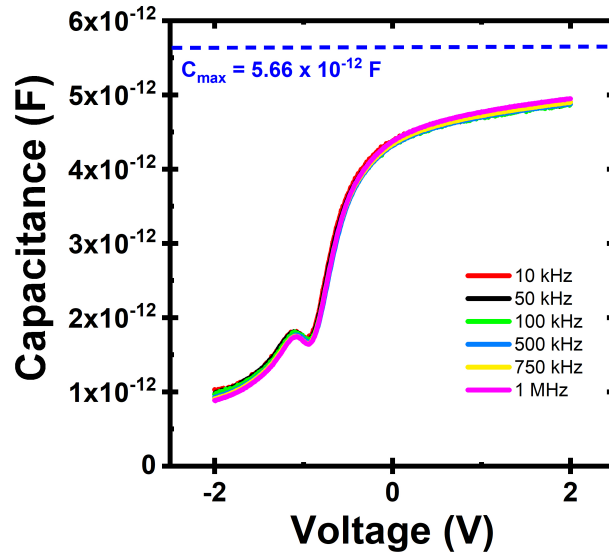
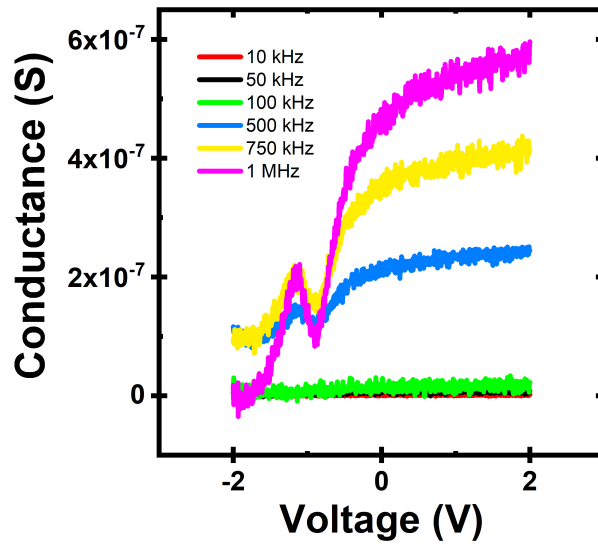


Figure 3.14: (a) 460 nm thick WS₂ flake pre patterning and (b) WS₂ flake post patterning of AuNi metal patterning on 20 nm Al₂O₃ on *p*⁺Si. The site on the top right of the flake was probed. Note, the sample was then etched to the size of the 40 μm x 40 μm metal contact.

The maximum oxide capacitance was calculated using the same equation as the other case studies. The maximum oxide capacitance for this 40 μm x 40 μm flake was 5.66×10^{-12} F. The first set of CV measurements on the etched WS₂ flake were performed with the following frequencies - 10 kHz, 50 kHz, 100 kHz, 500 kHz, 750 kHz and 1 MHz. It was a single sweep with a bias range of -2V to +2V, where the voltage was applied through the Si substrate. The maximum C_{ox} value for this WS₂ capacitor is shown as a dotted line in Figure 3.15 (a). From the experimental data, shown in Figure 3.15 (a), it was clear CV response remains insensitive to frequency in almost all regions of the response. The GV response was also recorded, as depicted in Figure 3.15 (b).



(a)

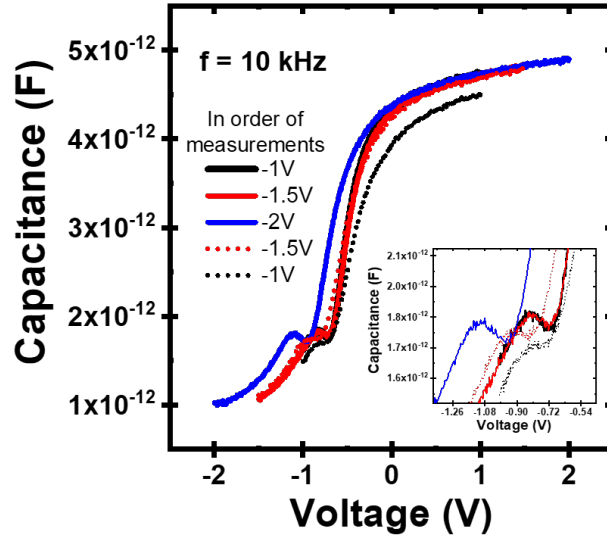


(b)

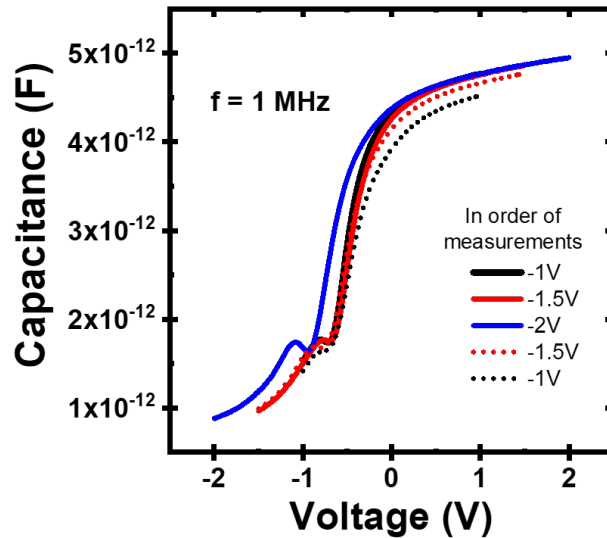
Figure 3.15: (a) CV response of WS₂ flake on Al₂O₃/p⁺Si with AuNi contacts. The maximum C_{ox} is also shown at 5.17×10^{-12} . (b) GV response of WS₂ flake on Al₂O₃/p⁺Si with AuNi contacts.

Further investigations then took place to understand the performance of this MOSCAP device. Single sweep CV tests were performed between different bias windows. The same frequency range was used as above. However, in order to see the behaviour more clearly, only the lowest (10 kHz - Figure 3.16 (a)) and highest (1 MHz - Figure 3.16 (b)) are shown. The sequence of voltage ranges were -1 V to +1V, -1.5 V to +1.5V, -2

V to +2V and then reversed back to -1.5 V to +1.5V and finally -1 V to +1V. An inset in Figure 3.16 (a) for 10 kHz shows a magnified look at the peak seen in the depletion region. The GV sweep at 1 MHz is also shown in Figure 3.17. As the voltage is increased, the sweep is shifted to the left.



(a)



(b)

Figure 3.16: (a) Single sweep 10 kHz CV response of WS₂ flake on Al₂O₃/p⁺Si with AuNi contacts, measured at between -1 V to +1V, -1.5 V to +1.5V, -2 V to +2V and then reversed back to -1.5 V to +1.5V and finally -1 V to +1V. (b) Single sweep 1 MHz CV response of WS₂ flake on Al₂O₃/p⁺Si with AuNi contacts, measured at between -1 V to +1V, -1.5 V to +1.5V, -2 V to +2V and then reversed back to -1.5 V to +1.5V and finally -1 V to +1V.

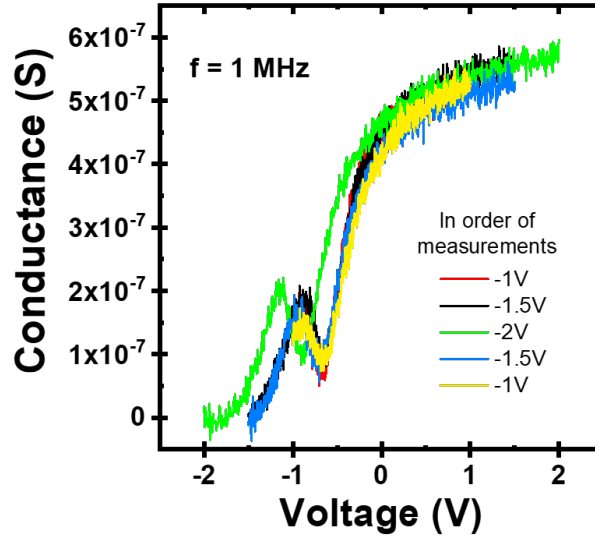


Figure 3.17: Single sweep 1 MHz GV response of WS₂ flake on Al₂O₃/p⁺Si with AuNi contacts, measured at between -1 V to +1V, -1.5 V to +1.5V, -2 V to +2V and then reversed back to -1.5 V to +1.5V and finally -1 V to +1V.

The possibility of hysteresis was then investigated. A double sweep was performed at -1 V to +1V back to -1 V. This process was repeated at -1.5 V and -2 V, depicted in Figure 3.18 (a). Then, the same tests were repeated but in reverse order, as seen in Figure 3.18 (b). Note, the plots may seem like they are 2 single sweeps in different directions but they are in fact from the same double sweep. The full and dotted lines are there to make it easier to understand position of the negative to positive/positive to negative part of the curve. The black arrow to the left of each plot sequence shows the order of voltage range testing. It was found that as the voltage bias increased, hysteresis also increased. The CV shows a net increase in positive charge as the start bias moves to a more negative value. This could be electron emission from a donor like state. When the defect is occupied by an electron, the defect is neutral and when the electron is emitted, it is negative and hence we propose this could be electron de-trapping by the applied negative back gate voltage.

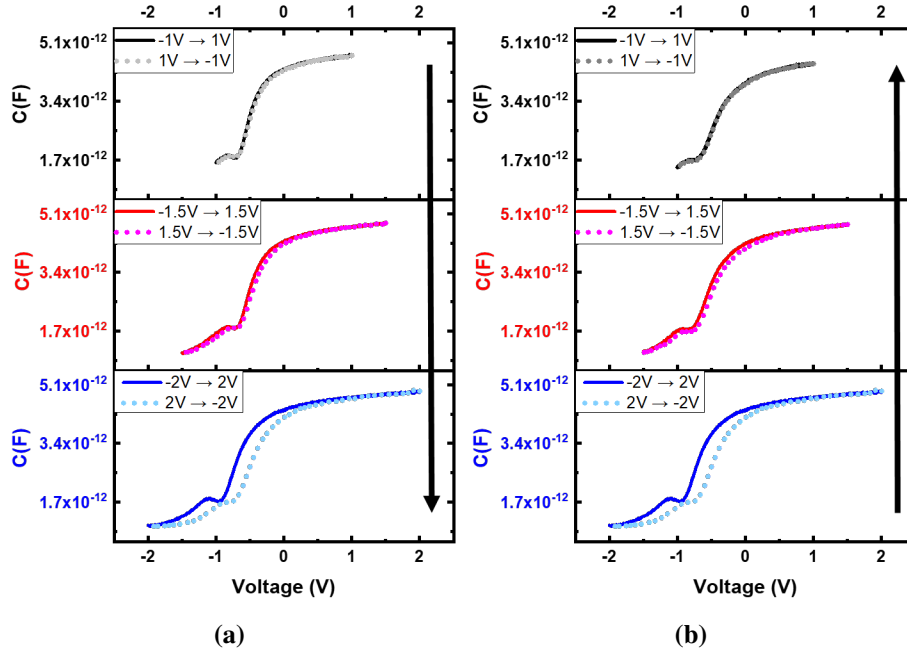


Figure 3.18: (a) Double sweep 10 kHz CV response of WS₂ flake on Al₂O₃/p⁺Si with AuNi contacts, starting at -1 V to +1V to -1 V and repeated at 1.5 V and 2 V, investigating change in hysteresis as voltage range increases. (b) The same was done as described in (a) but in reverse order, starting at -2 V to +2 V to -2V and repeated at 1.5 V and 1 V ranges.

The number of defect changes per cm^2 was calculated. The equations used was the following,

$$\Delta q = C \Delta V \quad (3.3)$$

where Δq is the change in charge during hysteresis, C is the capacitance where the largest hysteresis is measured and ΔV is the corresponding voltage shift. When this was found, Δq was divided by the flake and contact area of $40 \mu m \times 40 \mu m$. Finally, this values was divided by the charge of an electron which gave the number of defect charges per area for each bias range. The results are presented in Figure 3.19. The plot indicates an increase of the trapped charge as a function of the maximum voltage in accumulation during the CV sweep.

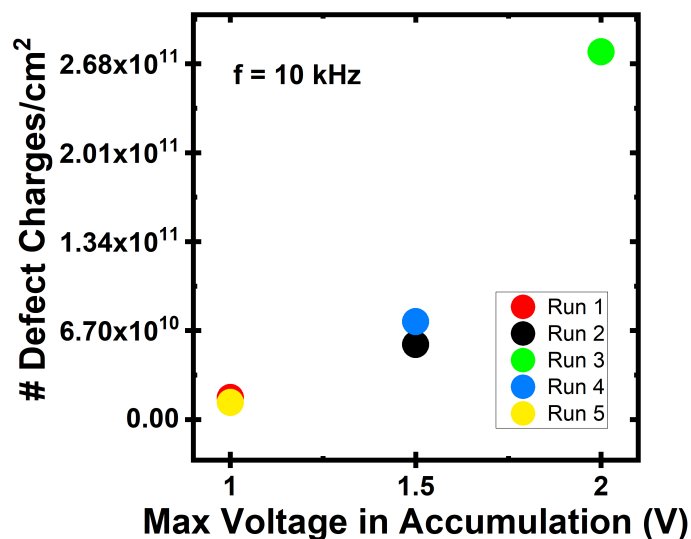


Figure 3.19: The number of WS₂ defect charges as a function of the maximum voltage in accumulation. Runs 1 and 5 were between -1 V to +1V, Runs 2 and 4 were between -1.5 V and +1.5 V and Run 5 from -2 V to +2V.

A check was also done to see if the starting voltage sign had an effect. A series of double sweeps were performed at 10 kHz. A double sweep starting at a positive voltage was performed, followed by a double sweep starting at a negative voltage. This was done for 1 V/-1 V, 1.5 V/-1.5 V and 2 V/-2 V, shown in Figure 3.20 (a), (b) and (c) respectively. No significant changes in the CV curves were found.

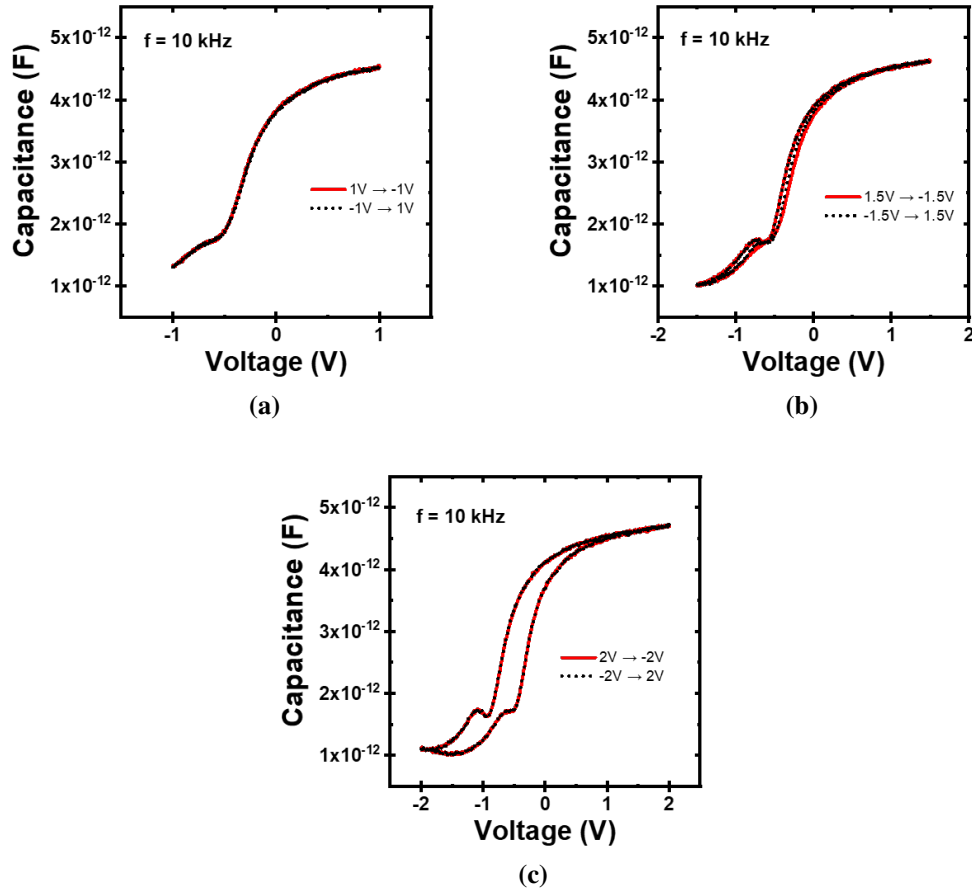


Figure 3.20: (a) Double sweep 10 kHz CV response of WS₂ flake on Al₂O₃/p⁺Si with AuNi contacts, starting at -1 V to +1 V to -1 V (dotted black line) and repeated starting from +1 V to -1 V to +1 V (full red line), investigating change in hysteresis as voltage range increases. (b) Double sweep 10 kHz CV response starting at -1.5 V to +1.5 V to -1.5 V (dotted black line) and repeated starting from +1.5 V to -1.5 V to +1.5 V (full red line), investigating change in hysteresis as voltage range increases. (c) Double sweep 10 kHz CV response starting at -2 V to +2 V to -2 V (dotted black line) and repeated starting from +2 V to -2 V to +2 V (full red line), investigating change in hysteresis as voltage range increases.

Throughout the CV measurements, a hump feature is present in the negative bias range and is not frequency dependent. A similar feature was found in some MoS₂ samples, however, in this case, the feature shows a distinct decrease in capacitance before it increases again towards accumulation. (Figure 3.15) We know that from the hysteresis, there are indeed traps, and the density of trapped charges increases with an increase in bias. However, the absence of frequency dispersion was puzzling and further investigations were performed to find the cause of this feature between ≈ -1.24 V and -0.94 V, highlighted in Figure 3.21.

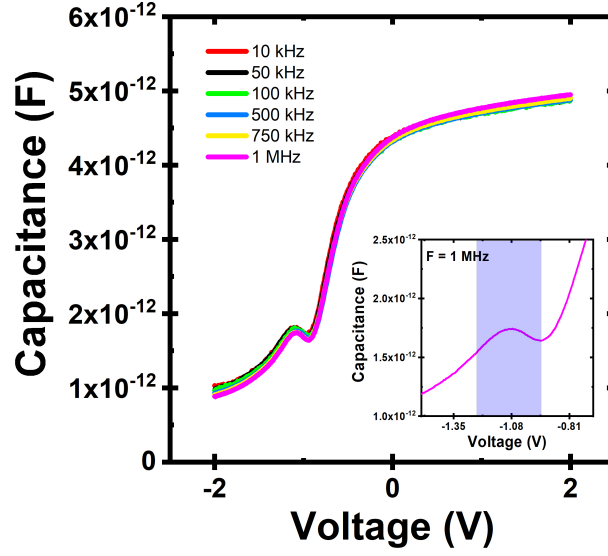


Figure 3.21: CV of the forward sweep from -2 V to +2 V at all frequencies, with the inset highlighting the hump feature found between ≈ -1.24 V and -0.94 V at 1 MHz.

Further calculations were made investigating the depletion region of the forward bias sweep. The region chosen was from -2 V to -0.5 V. First, the change in depletion width was calculated using the following equation,

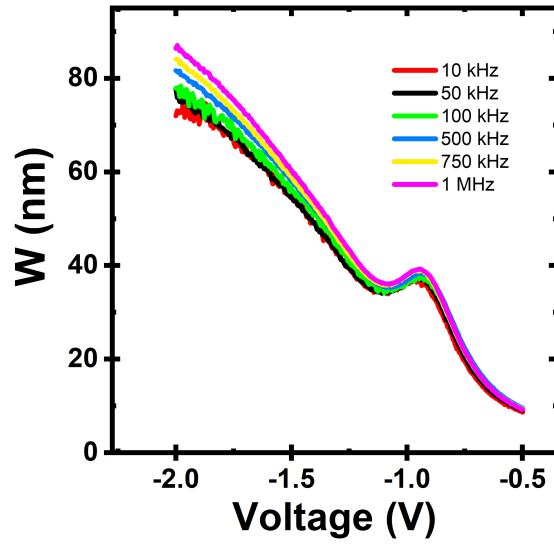
$$W = \epsilon_0 \epsilon_{WS_2} A \left(\frac{1}{C_{measured}} - \frac{1}{C_{max}} \right) \quad (3.4)$$

where W is the depletion width, ϵ_0 is the permittivity of free space ($8.85 \times 10^{-12} \text{ Fm}^{-1}$), ϵ_{WS_2} is the relative permittivity of bulk WS_2 (6.4 [205]), A is the area of the flake ($40 \mu\text{m} \times 40 \mu\text{m}$), $C_{measured}$ is the measured experimental oxide capacitance and C_{max} is the true maximum oxide capacitance ($5.66 \times 10^{-12} \text{ F}$). The plot is shown in Figure 3.22 (a). The surface potential for this depletion region was then found using the following equation

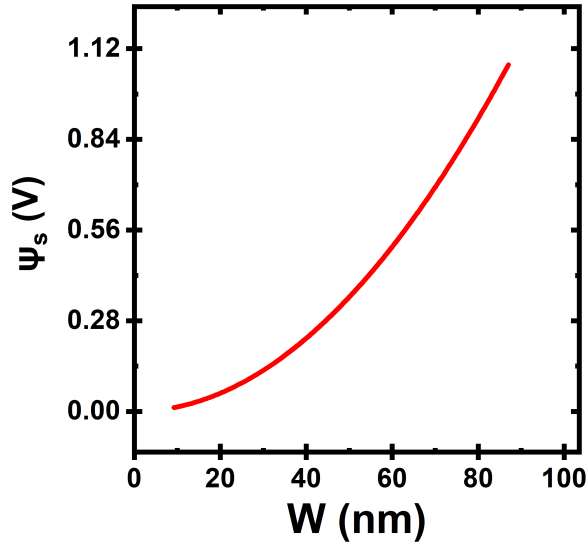
$$\psi_s = \frac{qNW^2}{2\epsilon_0 \epsilon_{WS_2}} \quad (3.5)$$

where ψ_s is the surface potential, q is the charge of an electron ($1.602 \times 10^{-19} \text{ C}$), N

is the doping concentration (10^{23} m^{-3}), W is the depletion width, ϵ_0 is the permittivity of free space ($8.85 \times 10^{-12} \text{ Fm}^{-1}$) and ϵ_{WS_2} is the relative permittivity of bulk WS_2 (6.4 [205]). The results are conveyed in Figure 3.22 (b). Figure 3.22 (a) shows that as the voltage bias increase, the depletion width decreases. This indicates that upward band bending is present where the WS_2 Fermi is shifted to lower energies. This is also represented by the surface potential in (b).



(a)



(b)

Figure 3.22: (a) The region of depletion width as a function of voltage for all frequencies. (b) Surface potential (ψ_s) as a function of the depletion width at 1 MHz.

Next, the density of interface states was investigated. The High-Low CV technique [204] was performed. Note, the same equation was used for the MoS₂ etched flake in case study 4.

$$D_{it} = \left(\frac{1}{q}\right) \left(\frac{C_{ox}C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{ox}C_{HF}}{C_{ox} - C_{HF}} \right) \quad (3.6)$$

Where D_{it} is the density of interface states, q is the charge of an electron, C_{ox} is the maximum oxide capacitance of the Au/Ni metal contact area, C_{LF} is the capacitance of the lowest frequency (1 kHz) and C_{HF} is the capacitance of the highest frequency (1 MHz). The density of interface states as a function of voltage in the depletion region is shown in Figure 3.23. With this data, the amount of charges needed to shift this hump like feature was calculated to be $2.4 \times 10^{10} \text{ cm}^{-2}$ by converting the voltage values to eV and integrating the area of the feature.

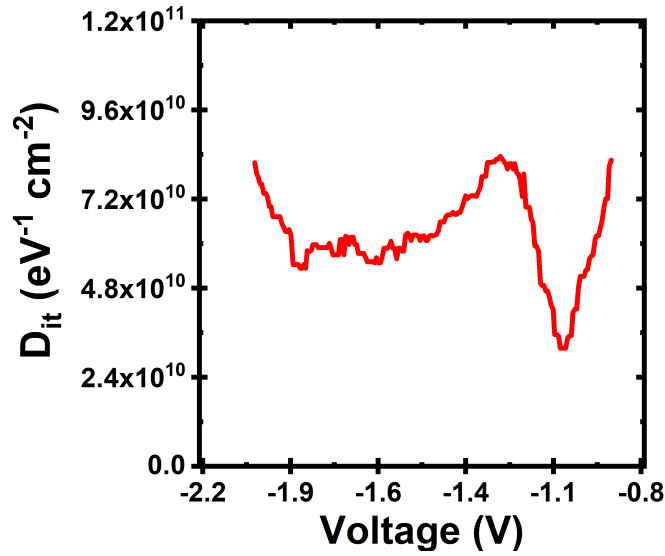


Figure 3.23: Density of interface states as a function of voltage in the depletion region at 1 MHz. Note this data has been smoothed using Origin.

This value can be compared to the density of interface states which would be required to generate a feature in the CV with a width of 0.3 V (see Figure 3.21 (inset)). This value, N_{it} , is given by

$$N_{it} = \frac{C_{ox}\Delta V}{q} \quad (3.7)$$

where N_{it} is the number of interface states per unit area, C_{ox} is the maximum oxide capacitance per unit area ($3.54 \times 10^{-3} \text{ F m}^{-2}$), ΔV is the voltage range of the feature (0.3 V) and q is the charge of an electron ($1.602 \times 10^{-19} \text{ C}$). The value was found to be $6.6 \times 10^{11} \text{ cm}^{-2}$. This value is approximately one order of magnitude larger than that of the density of interface states, which means there must be another factor influencing this feature. The bulk of this semiconductor material has been repeatedly exfoliated by the use of tape. We theorise that this exfoliation does not only affect the interface of the WS_2 , but also a few nanometers into the bulk. This could explain the hump like feature. When a positive bias is pushed through the material, towards accumulation, the defects are being filled both at the interface and the bulk. This causes a CV semi-flat region and could account for the additional charge needed to generate the 0.3 V feature evident experimentally.

3.4 Conclusion

Both MoS_2 and WS_2 were mechanically exfoliated and patterned into back gated MOSCAP devices. Firstly, in MoS_2 , the importance of flake adhesion to the metal contact was highlighted. One of the non etched flakes showed that the frequency dispersion exceeded the area of the metal contact and travelled throughout the whole flake. Another showed that when a flake touches other metal contacts (but are not fully covered) and the adhesion is strong enough, the entire contact becomes involved in frequency dispersion. Hump-like features found in multiple samples and the presence of hysteresis in some double sweeps show the proposed effects of defect charge traps at the oxide/semiconductor interface. A WS_2 back gated MOSCAP device was also investigated. This uncovered very interesting results suggesting not only the presence of interface trap states but also the possibility of charges trapping into the bulk of the

semiconductor, giving more insight to the behaviour of the TMD/oxide beyond the interface. D_{it} values calculated in this study were lower than other reports and to the best of my knowledge, we are the first to propose charge trapping in the bulk semiconductor.[175, 179, 206, 207] This is certainly going to be a focus for future work. Since the area must be certain, more etched MoS₂ and WS₂ samples must be made to further investigate this hypothesis. Though the results varied throughout some samples, these results demonstrate that interface state density values below the detection limit of $\approx 1 \times 10^{10} \text{ cm}^{-2}$ [208] can be achieved between crystalline MoS₂ on amorphous Al₂O₃ or SiO₂ and WS₂ on Al₂O₃, supporting one of the main motivations for using 2D semiconductors in MOSFETs and Tunnel FETs.

Chapter 4

**The structural and electronic
properties of MoS₂ grown on SiO₂ by
chemical vapour deposition between
350 °C and 550 °C**

4.1 Introduction

There has been extensive research into CVD grown MoS₂ with various applications in mind, including gas sensing [209–212], biosensors [213, 214], phototransistors [215, 216] and electrocatalysis [217, 218]. These have helped make important developments in the field of large area MoS₂ CVD processes. However, there is still a lack of knowledge around device performance on low temperature CVD grown MoS₂. This formed the motivation for our study. Our study utilizes a commercial tool and includes extensive electrical characterization and Hall analysis.

One of the major obstacles of large area growth of 2D materials above existing integrated circuits is the low thermal budget for 3D BEOL. In order to successfully create 3D integrated circuits, the temperature and time at which the materials are made cannot be above the thermal budget which degrades the underlying transistors. The first negative impact is typically on the source and drain silicide contacts in the p and n channel MOSFETs. [50] The permissible thermal budget for above CMOS will depend on the particulars of the process, but a representative example is shown below. Based on the work of Fenouillet-Beranger et al, no degradation of the underlying CMOS performance was detected up to 550 °C for 2 hours and 500 °C for 5 hours. [50, 51] Based on these studies, we explored the growth of MoS₂ by an industry compatible CVD process in the range 350 °C to 550 °C with times ranging from 30 minutes to 2 and a half hours, with the aim of assessing the structural and electronic properties of the films.

4.2 Results and Discussion

4.2.1 Structural and chemical analysis

Experimental methods and parameters are discussed in the methodology chapter. The effects of changing the growth temperature of $\approx 10\text{nm}$ MoS₂ on SiO₂/ is first discussed. 350 °C, 450 °C and 550 °C were chosen and MoS₂ was uniformly grown in the 300 mm diameter chamber. Figure 4.1 (a) shows each sample becoming lighter in blue colour as the temperature decreases. Work by Ardahe et al also observe a change in colour due to varying growth temperatures.[219]

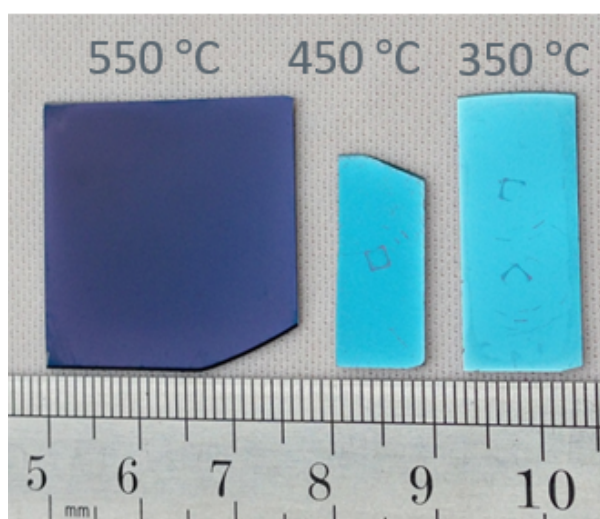


Figure 4.1: CVD-grown MoS₂ on SiO₂/Si substrates at 350/450/550 °C. These small coupons are placed throughout the chamber, demonstrating that uniform and continuous film deposition is achievable across a 300 mm diameter. It must be noted that comparing to literature, the darker blue colour from 550 °C shows 10 nm while the lighter blue colours from 450 °C and 350 °C indicates fewer layers of MoS₂. The little darker square outlines are remnants of IR testing.

Following on from this, a new series of investigations took place, looking at the impact of changing growth times. Using 550 °C as the baseline temperature (at 10 sccm 1 % H₂S) the following time periods were chosen, resulting in varying thicknesses - 2.5 hours: 10 nm, 1.25 hours: 5 nm, 0.75 hours: 3 nm, 0.3 hours: 1.2 nm. Figure 4.2 shows the varied thickness series on (a) SiO₂ (b) sapphire and (c) glass. As the growth time increases, so does the thickness and hence affecting the colour of each

sample.[220] The 10 nm of MoS₂ grown over 2.5 hours was confirmed using high resolution TEM, with the assumption of linear growth.

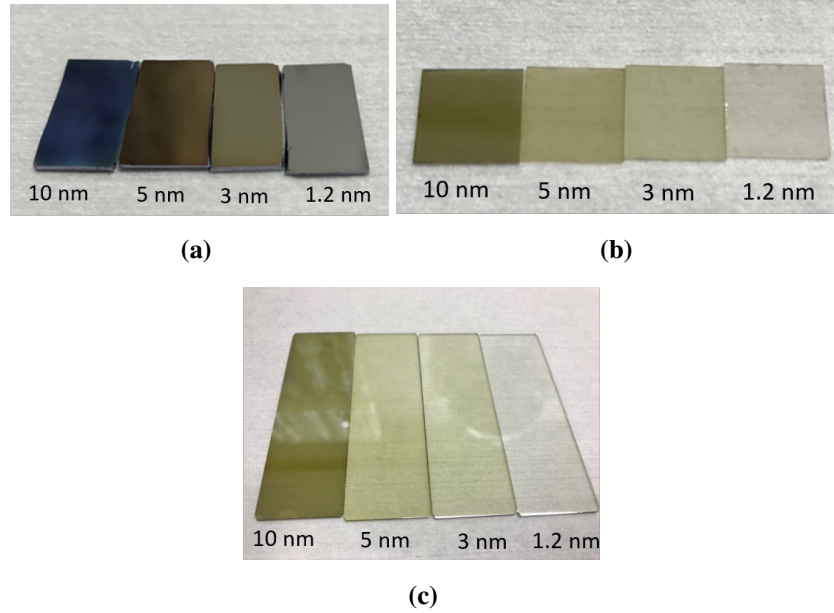


Figure 4.2: CVD grown MoS₂ on (a) SiO₂ (b) sapphire (c) glass. Each series has 4 different thicknesses - 10, 5, 3 and 1.2 nm and as seen in all images, the colour lightens with decreasing thickness. 550 °C at 10 sccm 1 % H₂S where the 2.5 hours gives 10 nm, 1.25 hours gives 5 nm, 0.75 hours gives 3 nm and 0.3 hours gives 1.2 nm.

The next investigation series focused on the impact of the substrate on the growth of MoS₂. MoS₂ was grown at 550 °C on SiO₂, sapphire and a-Al₂O₃ /sapphire. Using HR-TEM, Figure 4.3 (a) – (c) confirms that polycrystalline and layered MoS₂ was formed continuously and uniformly on the substrates. However, all 3 substrates gave varied results. SiO₂ (Figure 4.3 (a)) gives the thickest and most ordered layering of MoS₂ at 9 – 10 nm. Figure 4.3 (b) shows that the thickness of MoS₂ was only slightly affected by the sapphire substrate (5–6 nm) but fin like structures, perpendicular to the plane were formed. Finally, Figure 4.3 (c) conveys the smallest thickness of 4 -5 nm on a-Al₂O₃ /sapphire, but more ordered than on sapphire. These out of plane fins are also observed in Vila et al. and they contribute these features to a *MoO_x* partial pressure gradient.[221] Since one of our precursors is Mo(CO)₆, we propose that this could be an effect present in our samples too.

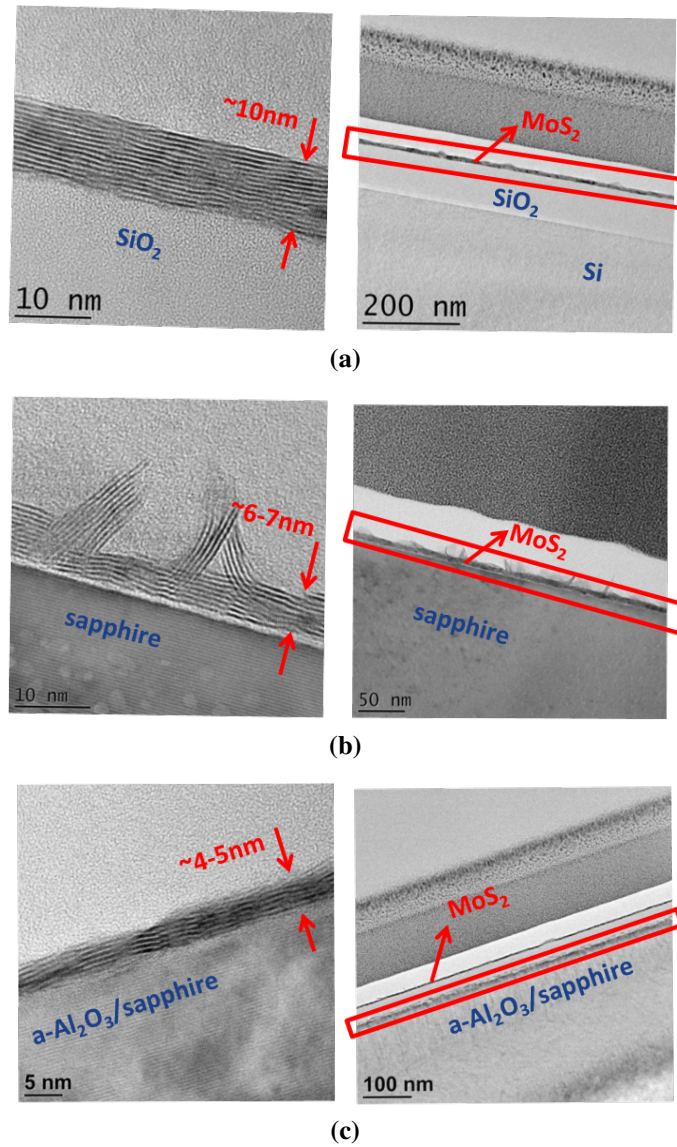


Figure 4.3: HR-XTEM micrographs show layered and polycrystalline MoS₂ (550 °C, 10 sccm 1 H₂S, 2.5 hours) on (a) SiO₂/Si, (c) sapphire and (e) *a* – Al₂O₃/sapphire. MoS₂ on SiO₂/Si gave the most uniform layers. MoS₂ on sapphire gave fin like structures, perpendicular to the plane. MoS₂ on *a* – Al₂O₃/sapphire gave moderately ordered layers but less layers than that on SiO₂/Si. Zoomed-out HR-XTEM micrographs of the MoS₂ (b) SiO₂/Si, (d) sapphire and (f) *a* – Al₂O₃/sapphire.

A plan-view TEM of MoS₂ on SiO₂ was also obtained, along with a fast Fourier transfer. Figure 4.4 (a) shows a 30 x 30 nm real plan-view TEM image of MoS₂ on SiO₂. From this image alone, not much information can be deduced. However, Figure 4.4 (b) shows the same image but put in reciprocal space which conveys details about the material's diffraction behaviour. This electron diffraction pattern shows 6 groups,

with each group containing 3 - 4 dots, representing the reciprocal lattice vector. Let us compare this to Figure 4.4 (c), an inverted plan view TEM of polycrystalline MoS₂ over a much larger area. Here the dominant [100] and [110] orientations of MoS₂ can be seen as full rings. In theory, the shape of the outlines should be hexagonal, like the shape of MoS₂ domains, however, since this is polycrystalline and there are many different orientations on top of each other. A circular shape was observed. Going back to (b), the 6 groups of 3/4 dots can be used to estimate the grain size. The area of 30 x 30 nm, taking 3 dots the domain size would be 17 nm and for 4 dots, 15 nm. This ties in nicely with results from HR-TEM and later when discussing Hall and electrical data. In order to stay within the thermal budget for BEOL, the growth temperature must be kept as low as possible for as short possible. However, the results show that the highest temperature of 550 °C gives the most ordered layers of MoS₂ but at the cost of needing a shorter growth time - leading to smaller grain sizes. Finally, if the diffraction image in Figure 4.4(b) is filtered such that all data points within the 6 groups of 3 / 4 dots are removed, and the resulting image is passed through inverse Fourier Transform, the short range order in the image, and the hexagonal nature of the MoS₂ is evident (see in Figure 4.4 (d)). If looked at closely, you can see a kaleidoscope image of multiple orientations of hexagonal shapes, which represents the different orientations in the various layers of MoS₂ crystal.

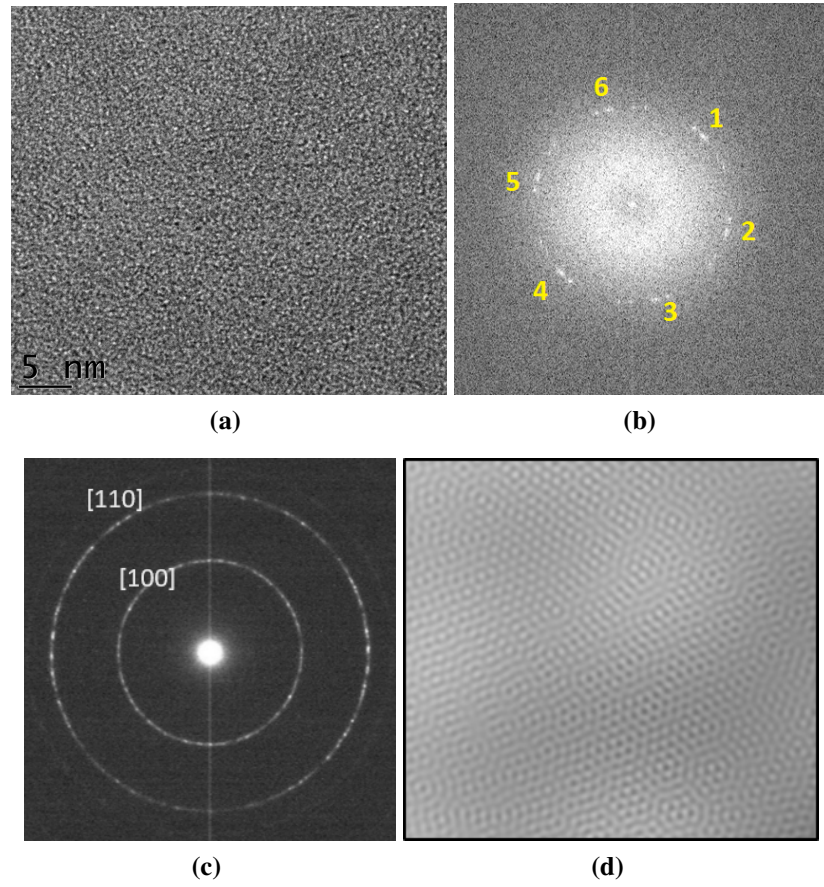


Figure 4.4: (a) 30 x 30 nm real image of CVD grown MoS₂ on SiO₂ (b) Fourier Transform of (a) showing the electron diffraction pattern of the 30 x 30 nm real image of CVD grown MoS₂ on SiO₂. (c) Large area electron diffraction pattern confirms the formation of polycrystalline MoS₂, where the dominant orientations, [100] and [110], are indicated. (d) Inverse Fourier Transform of filtered image (b) produces a clear image of the hexagonal crystal structure

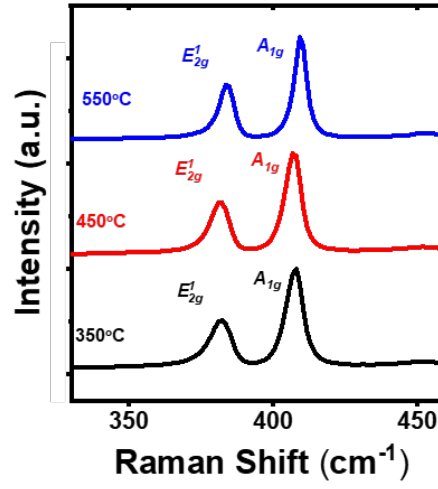
4.3 Raman Analysis of CVD Grown MoS₂

Previously, in Figure 4.1, the impact of growth temperature can be seen by eye with a change of colour. Acquiring a more in depth understanding of this was achieved with the help of Raman spectroscopy. Figure 4.5 (a) shows the Raman spectra of all 3 temperature. For MoS₂ Raman data, there are 2 visible vibration modes that can be detected with the Reinshaw spectrometer. These modes are E_{2g}^1 and A_{1g} . For bulk MoS₂, the E_{2g}^1 is an in-plane vibration mode observed at approximately 383 cm^{-1} . The A_{1g} is an out-of-plane vibration mode, observed at approximately 408 cm^{-1} . [222] A shift to the right is present going from lower to higher temperature as

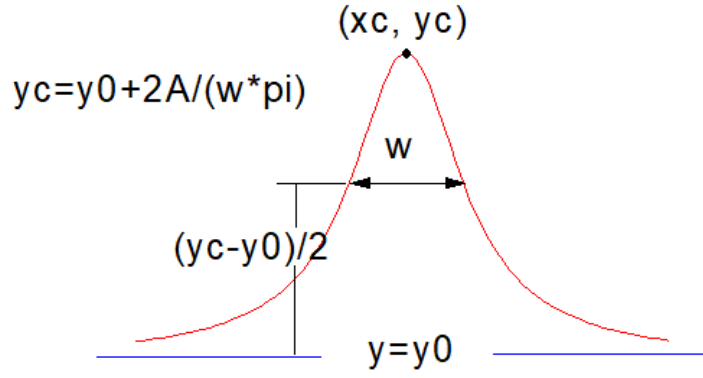
seen in Fig 4.5. When comparing these results to literature, this shift can be attributed to an increase in crystalline order. In addition to this, OriginPro was used to plot a Lorentzian FWHM (full width half maximum) fitting of the E_{2g}^1 and A_{1g} peaks of MoS_2 for each growth temperature. The equation from OriginPro is defined below -

$$y = y_0 + \frac{2A}{\pi} \left(\frac{4}{4(x - x_c)^2 + w^2} \right) \quad (4.1)$$

where y_0 is the offset, x_c the centre of the peak, w is the FWHM and A is the area of the peak. A schematic of the equation is shown in Figure 4.5 (b), also taken from OriginPro. Since the The FWHM increases as the growth temperature decreases providing evidence that disorder increases as the growth temperature reduces.[223] Results are shown in table 3.1.



(a)



(b)

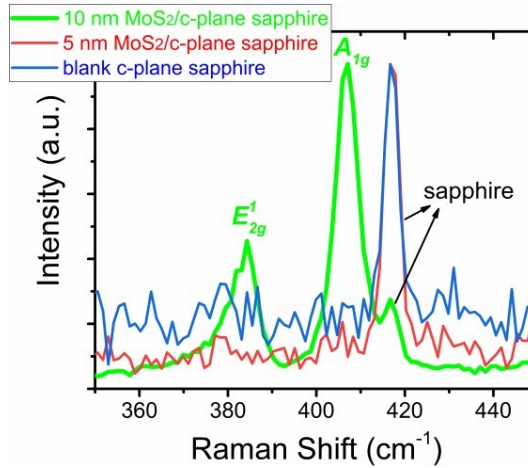
Figure 4.5: (a) Raman spectra comparison of all 3 temperature growth procedures; 350 °C (bottom, black line), 450 °C (middle, red line) and 550 °C (top, blue line) on SiO₂/Si substrate. The presence of both E'_{2g} and A_{1g} MoS₂ peaks were found in all growth processes. (b) Schematic diagram conveying each element in the equation for Lorentzian FWHM fitting from OriginPro, where y_0 is the offset, x_c the centre of the peak, w is the FWHM and A is the area of the peak.

Table 4.1: A Lorentzian fitting of the FWHM values for the E'_{2g} and A_{1g} from Figure 4.5 (b). The FWHM decreases as the growth temperature increases, providing evidence that disorder decreases as the growth temperature is increased.

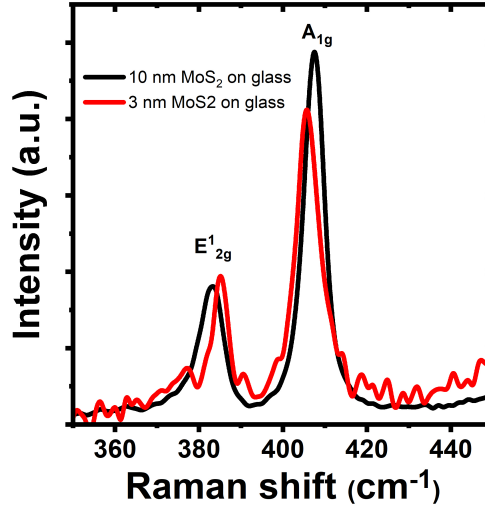
Growth Temperature	FWHM of E'_{2g} (cm^{-1})	FWHM of A_{1g} (cm^{-1})
350 °C	9.01	6.76
450 °C	7.51	6.33
550 °C	5.54	4.81

Following on from the set of samples grown at separate temperatures, an extensive Raman analysis was done on MoS₂ grown with different thicknesses and also MoS₂

grown on 5 different substrates. First, the thickness series is discussed. Nominally 10nm, 3nm and 1.2nm MoS₂ films were grown on glass in different deposition experiments under the same growth condition (550°C, 10 sccm 1% H₂S, 2.2 Torr) for different process times. It must be mentioned that a thickness series on sapphire was also investigated but substantial back-scattering noise and the prominent sapphire Raman peak at $\approx 416 - 418 \text{ cm}^{-1}$ as seen in Figure 4.6 (a), made it too difficult to analyse MoS₂ peaks at lower thicknesses. To combat the combination of noise from the glass substrate series, and the low intensity Raman peaks on the 1.2 nm film, the two Raman mode peaks are statistically estimated for this MoS₂ film from the large set of microscale mapping data over the three macroscale separated sites. The peak values for this thin film are not determined solely from the spectra in figure 4.6 (b) but from the statistical analysis shown later in figure 4.8 (b). The same procedure was performed for the MoS₂ on 5 separate substrates.



(a)



(b)

Figure 4.6: (a) Raman spectra of nominally 10 nm MoS₂ on c-plane sapphire, nominally 5 nm MoS₂ on c-plane sapphire, and blank c-plane sapphire. The Raman mode on the 5 nm MoS₂ is lost due to the large Raman signal from c-plane sapphire. (b) Plot showing the E'_{2g} and A_{1g} intensity peaks of 10 nm and 3 nm CVD grown MoS₂ on glass at 550 °C.

To illustrate that a uniform MoS₂ had been grown by CVD, microscale statistical spatial mapping by Raman spectroscopy was performed. For the spatial mapping by Raman spectroscopy, 66 measurements were performed over an area of 15 μm x 15 μm , on three macroscale separated sites, for each sample. For each mapping, the baseline was subtracted and set to zero. Then, for a mapping image, an intensity range was set. The A_{1g} peak was chosen to represent the maps since it is the most well defined peak of the two Raman modes. The colour on the images varies from black

to red which corresponds to lowest to highest intensity (see Figure 4.8 (a) and Figure 4.11 (a)). Hence, the higher the intensity at the set Raman shift, the brighter the red colour. Samples were tested on the same day to ensure the same calibration of the Raman system was used. Due to the difference in thicknesses, in order to get visible results for each sample, the laser power and integration times varied for each set.

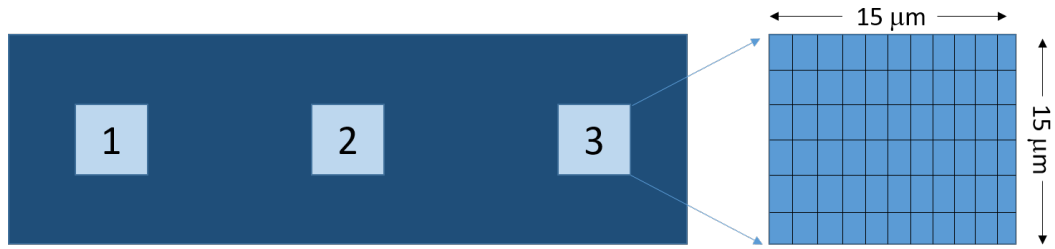


Figure 4.7: Micro vs macro Raman diagram. On the left are the three $15\ \mu\text{m} \times 15\ \mu\text{m}$ macroscale sites on the MoS_2 sample. On the right is a zoomed in image of a macroscale site, divided into 66 microscale sites. A Raman measurement was done on each microscale site in order to get an average Raman peak for each macroscale site.

For the nominally 10 nm and 3 nm on glass, it can clearly be seen that MoS_2 is present throughout all sites, with only slight changes. For the nominally 1.2 nm on glass, the colour is a darker red. One of the challenges with this set was that the A_{1g} peak was not as well defined, therefore, picking one Raman shift was more difficult. For noisier spectra, ie 1.2nm sample, the baseline was subtracted in order to obtain a viable intensity reading. The set intensity ranges can be seen in Table 4.2. The uniformity of the MoS_2 , indicated by the macroscale separated sites that underwent microscale mapping, is excellent, with very similar Raman spectra obtained from the extensive number of statistical spectra per site, and across three macroscale separated sites. The very dark red colour on the thinnest MoS_2 of 1.2 nm thickness in Figure 4.8 (a) is attributed to the very weak A_{1g} mode. The E_{2g}^1 and A_{1g} modes on the 1.2 nm MoS_2 , although weak, are still visible and statistically detectable from the large set of Raman mapping data. Hence, in order to define the 1.2 nm Raman peaks more accurately, a statistical analysis is performed from the large set of Raman mapping data and the two Raman peaks are estimated on this MoS_2 thin film (see Figure 4.8 (b)) and the caption

containing the mean values of the two Raman peaks, which also includes the standard deviation values). These results indicate that MoS₂ was formed uniformly over the entire sample.

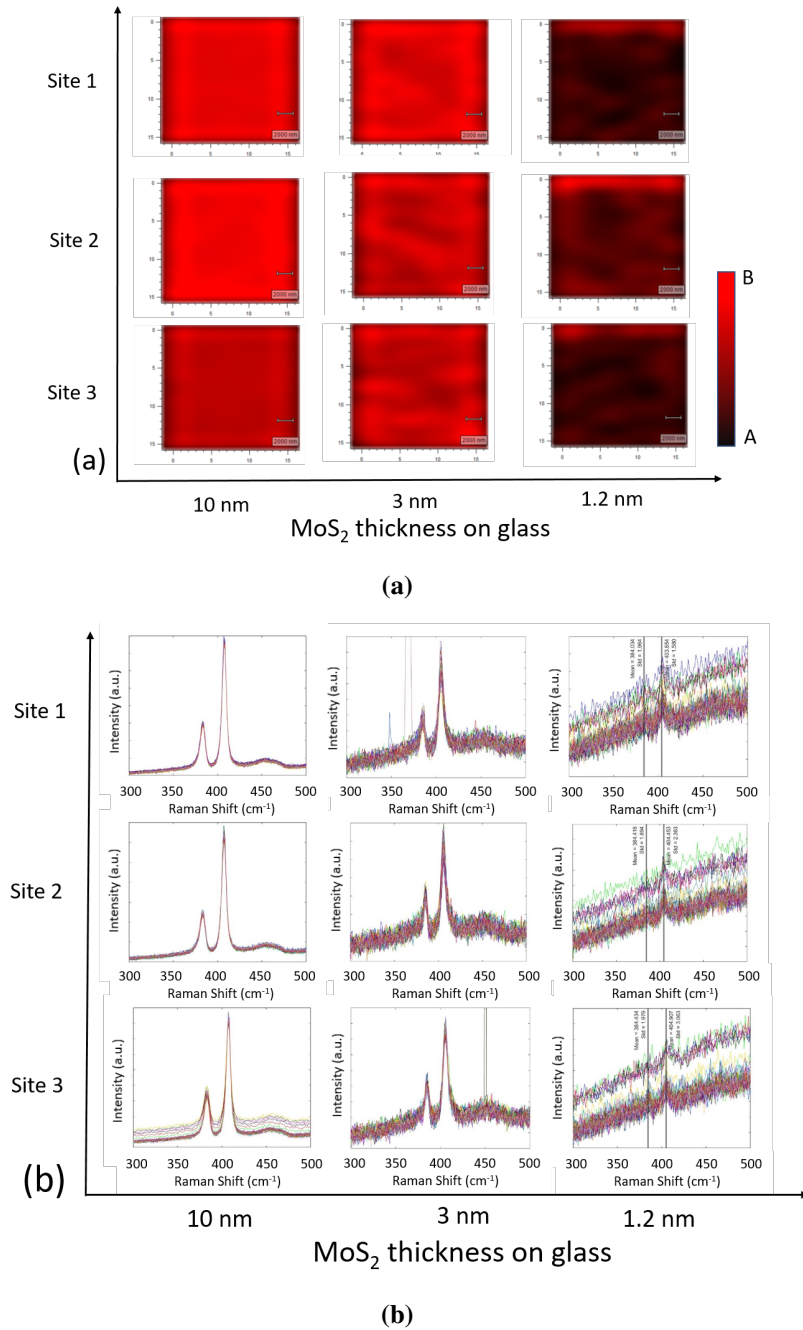


Figure 4.8: (a) Raman maps for 3 separate sites of A_{1g} Raman peak for MoS₂ for each of the thicknesses on glass. (b) Statistical analysis of individual MoS₂ Raman spectra including both E_{2g}^1 and A_{1g} modes.

Table 4.2: Table outlining the A_{1g} intensity peak for each of the thicknesses, 10 nm, 3 nm, and 1.2 nm, of CVD grown MoS_2 on glass at 550 °C. It also gives the intensity ranges used for each sample. To ensure that uniform growth was achieved, mapping was done across 15 μm x 15 μm area on 3 different spots. The intensity values in the table are representative of that data, since individual measurements were also performed. The intensity ranges differ for each sample for various reasons - substrate choice, MoS_2 thickness and MoS_2 crystallinity. They were then normalised for the mapping images (Figure 4.8 (a)) so each sample could be compared.

MoS₂ on Glass	Intensity Peak (cm^{-1})	Intensity Range (a.u.)
10nm	407.1	0 – 7996
3nm	405.9	0 - 760
1.2nm	404.5	1100 – 1600

Raman spectra of nominally 10 nm, 3 nm, 1.2 nm MoS_2 on glass and blank glass substrate is shown in figure 4.9. For each thickness, 3 spectra taken from each site are shown. For thinner MoS_2 , the glass substrate mode interference's increases. The positions of the E_{2g}^1 and A_{1g} modes are assigned for each thickness are statistically obtained from each of the 3×66 Raman microscale mapping at the three macroscale separated sites. The separation ($\Delta\omega$) between the E_{2g}^1 mode and A_{1g} mode are estimated to be: 24.0 cm^{-1} for the nominally 10 nm MoS_2 ($\approx$ 15 monolayers), 20.4 cm^{-1} for the 3 nm MoS_2 ($\approx$ 5 monolayers), and 20.0 cm^{-1} for the 1.2 nm MoS_2 ($\approx$ 2 monolayers). Comparing these results from our low thermal budget polycrystalline grown MoS_2 , a similar trend is observed of decreasing $\Delta\omega$ with reducing nominal film thickness, confirming the reducing thickness sequence of the grown films.

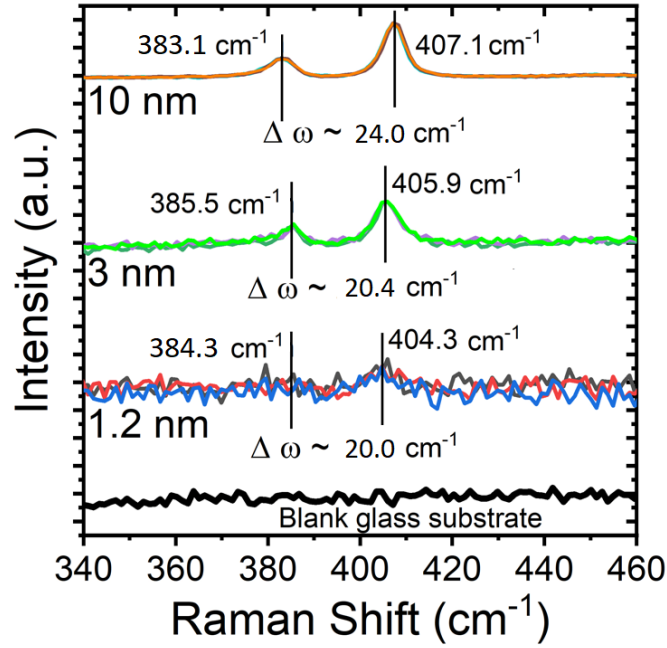


Figure 4.9: Raman spectra of nominally 10 nm, 3 nm, 1.2 nm MoS₂ on glass and blank glass substrate. For each thickness, 3 spectra taken from each site are shown. For thinner MoS₂, the glass substrate mode interference's increases. The positions of the E_{2g}^1 and A_{1g} modes are assigned for each thickness are statistically obtained from each of the 3×66 Raman microscale mapping at the three macroscale separated sites (note: they are not extracted solely from the plots shown here). The separation $\Delta\omega$ between the 2 Raman modes are displayed, showing a decrease in value with decreases MoS₂ thickness.

Next, a series of 10 nm MoS₂ on 5 different substrates was investigated. The five substrates were glass, a-Al₂O₃/glass, c-plane sapphire, a-Al₂O₃/sapphire and SiO₂/Si. The growth process used was 550 °C, 10 sccm 1 % H₂S for 2.5 hours. First, a simple Raman measurement was performed to ensure the presence of MoS₂ as well as comparing the spectra on each substrate, shown in Figure 4.10. (Note, the measurements done in Figure 4.10, were performed on a separate Raman tool in CRANN, Trinity College Dublin.) The $\Delta\omega$ was then estimated for each sample. The results show $\approx 24.0 \text{ cm}^{-1}$ on glass, $\approx 24.0 \text{ cm}^{-1}$ on a-Al₂O₃/glass, $\approx 22.8 \text{ cm}^{-1}$ on c-plane sapphire, $\approx 22.8 \text{ cm}^{-1}$ on a-Al₂O₃/sapphire, and $\approx 22.8 \text{ cm}^{-1}$ on SiO₂/Si. From previous HR-TEM images, it is proven that 10 nm MoS₂ was grown on SiO₂/Si as seen in Figure 4.3 (a).

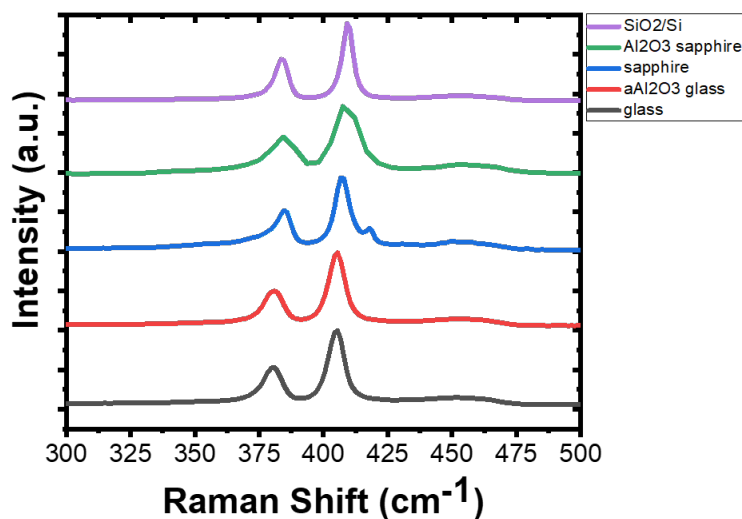


Figure 4.10: Stacked and normalised Raman of 10nm MoS₂ grown on 5 different substrates. (550 °C, 10 sccm 1 % H₂S for 2.5 hours) The results show $\approx 24.0 \text{ cm}^{-1}$ on glass (black), $\approx 24.0 \text{ cm}^{-1}$ on a-Al₂O₃/glass (red), $\approx 22.8 \text{ cm}^{-1}$ on c-plane sapphire (blue), $\approx 22.8 \text{ cm}^{-1}$ on a-Al₂O₃/sapphire (green), and $\approx 22.8 \text{ cm}^{-1}$ on SiO₂/Si (purple).

The same Raman mapping technique was done on the 5 different 10 nm MoS₂ samples. Figure 4.11 (a) shows the maps of 3 separate sites from each sample. As seen by the uniformity of the red, it is clear that at 10 nm, on all 5 substrates, the growth process was consistent throughout the whole area of the substrate. Figure 4.11 (b) shows representative Raman spectra for each macroscale site. Again, we see the uniformity of the spectra. It must be noted that the sapphire peak interferes with the A_{1g} peak, which can be seen on the spectra for both c - plane sapphire and a - Al₂O₃/sapphire. The intensity ranges for each substrate is displayed in Table 4.3.

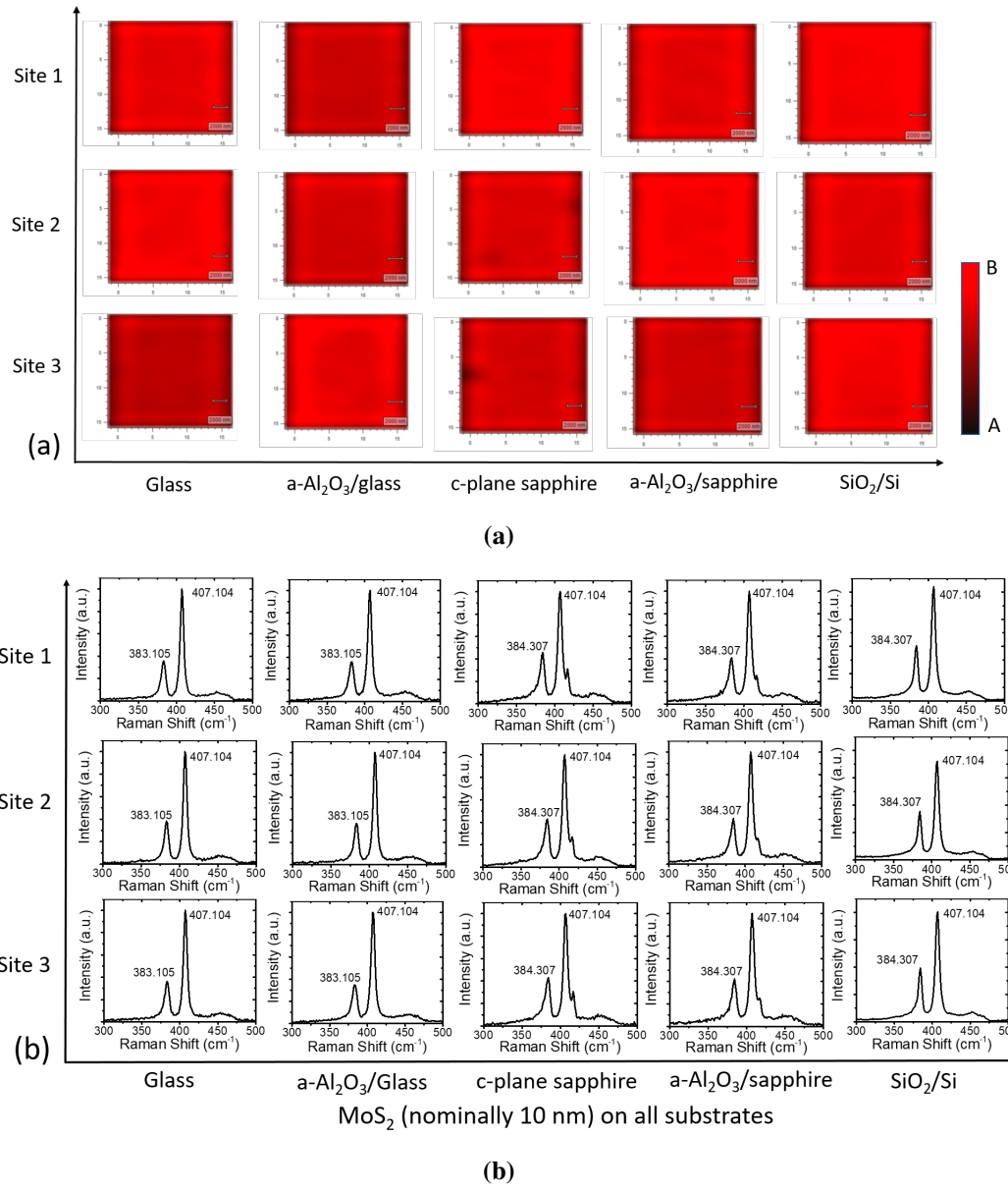


Figure 4.11: (a) Raman maps for 3 separate sites of A_{1g} Raman peak for MoS₂. (b) Individual MoS₂ Raman spectra including both E_{2g}¹ and A_{1g} modes.

Table 4.3: Table outlining the A_{1g} intensity peak for each of the 10 nm CVD grown MoS_2 on glass, $\alpha\text{-Al}_2\text{O}_3/\text{Glass}$, Sapphire, $\alpha\text{-Al}_2\text{O}_3/\text{Sapphire}$ and SiO_2 . It also gives the intensity ranges used for each sample. To ensure that uniform growth was achieved, mapping was done across $15 \times 15 \mu\text{m}$ area on 3 different spots. The intensity values in the table are representative of that data, since individual measurements were also performed. The intensity ranges differ for each sample for various reasons - substrate choice, MoS_2 thickness and MoS_2 crystallinity. They were then normalised for the mapping images (Figure 4.11 (a)) so each sample could be compared.

10nm MoS_2	Intensity Peak (cm^{-1})	Intensity Range (a.u.)
Glass	407.1	0 – 7996
$\alpha\text{-Al}_2\text{O}_3/\text{Glass}$	407.2	0 - 6328
Sapphire	407.1	0 – 3540
$\alpha\text{-Al}_2\text{O}_3/\text{Sapphire}$	407.2	0 – 4900
SiO_2	407	0 – 11450

A full width half maximum study was also carried out to help understand the crystal quality of MoS_2 on each substrate as seen in figure 4.12 (a) - (e). Defects on both the surface and bulk of a material can contribute to the broadening of Raman peaks. [224] The lower the FWHM value, the narrower the Raman peak is, which corresponds to a higher crystalline structure. As seen in Table 4.4, glass gave the lowest value at 5.6. The broadest FWHM value was on $\alpha\text{-Al}_2\text{O}_3/\text{sapphire}$. It must be noted that the FWHM values found on both sapphire substrate have been slightly distorted due to the presence of the sapphire Raman peak at $\approx 414 \text{ cm}^{-1}$. [225] Despite this, combining Raman mapping results with FWHM, it concludes that the growth process gave very similar polycrystalline MoS_2 on each substrate.

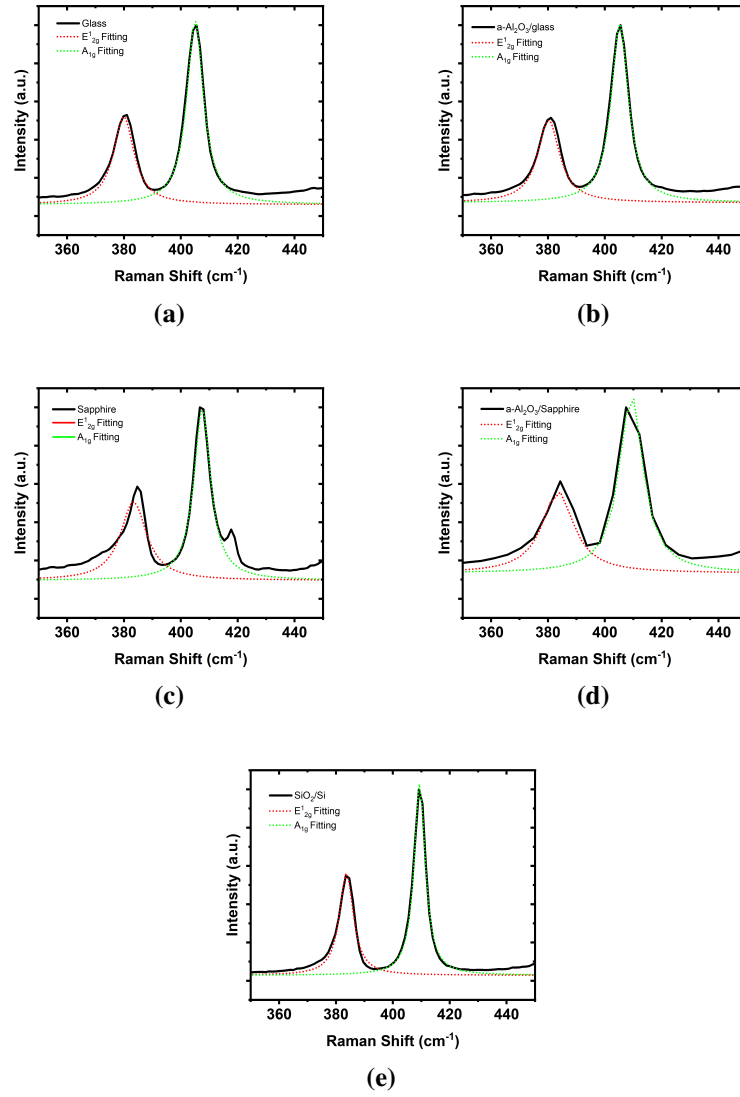


Figure 4.12: Lorentzian fit of E_{2g}^1 and A_{1g} peaks for each of the 10 nm CVD grown MoS_2 on (a) glass (b) $\text{a-Al}_2\text{O}_3/\text{Glass}$ (c) Sapphire (d) $\text{a-Al}_2\text{O}_3/\text{Sapphire}$ (e) SiO_2

Table 4.4: Table outlining the E_{2g}^1 and A_{1g} peaks for each of the 10 nm CVD grown MoS₂ on glass, a-Al₂O₃/Glass, Sapphire, a-Al₂O₃/Sapphire and SiO₂. The smaller the FWHM, the sharper the peak, which in turn corresponds to a more ordered crystalline material. The lowest FWHM value came from SiO₂. The highest came from a-Al₂O₃/Glass.

10nm MoS ₂ Substrate	E_{2g}^1 FWHM (cm^{-1})	A_{1g} FWHM (cm^{-1})
Glass	7.2	6.5
a-Al ₂ O ₃ /Glass	9.3	7.4
Sapphire	7.2	7.3
a-Al ₂ O ₃ /Sapphire	13.4	10.0
SiO ₂	5.9	4.8

4.4 Hall Analysis

Room temperature Hall/4P/2P analysis was performed on a number of MoS₂ samples on sapphire and *a* – Al₂O₃/*sapphire* (both patterned and non-patterned) using a high resistance unit. A 1 cm x 1 cm Van der Pauw structure, as shown in Figure 4.13 (a), was used for each test, [226] with corresponding Ohmic behaviour for MoS₂ grown at 550 °C on sapphire, shown in Figure 4.13 (b). Excellent Ohmic behaviour was found for all MoS₂ samples. Figure 4.13 (c) conveys patterned 1 cm x 1 cm MoS₂ film on sapphire or *a* – Al₂O₃/*sapphire* with Ni/Au metal contacts. The zoomed-in inset shows the metal tracks going towards each of the 4 contact pads which forms a VdP structure. These measurements were done at room temperature. It must be noted that the resistance values are quite high (GΩ range) both with and without contact resistance. All Hall-effect measurements were obtained from a DC magnetic field (± 1.7 T) with hold times of up to 420 s. These long hold times before each measurement ensures stability in the current through the MoS₂ thin film before the the voltages are measured in Hall/4P. Up to 500 counts were performed during each test to ensure reliable signal-to-noise ratios. ($\approx 11:1$ for Hall effect and $\approx 374:1$ for 4P

resistance/resistivity.)

Please be aware that the Hall results for MoS₂ on SiO₂ (85 nm)/Si(p++) substrates are excluded from this work since Hall/resistance results can be affected, or even dominated, by the underlying p-type Si substrate. Though Ohmic, the resistance of the MoS₂ is high at the GΩ range and the Hall system can apply a maximum voltage of ±100 V to achieve a maximum set current (1 pA to 0.1 A range). Consequently, significant leakage through the 85 nm SiO₂ to the underlying Si substrate can be observed. Even at lower voltages, stress induced leakage currents in SiO₂ can still contribute, or dominate, the Hall analysis. [227, 228] To avoid untrustworthy data, all the Hall/4P/2P results focuses on MoS₂ grown on sapphire or *a* – Al₂O₃/*sapphire* substrates.

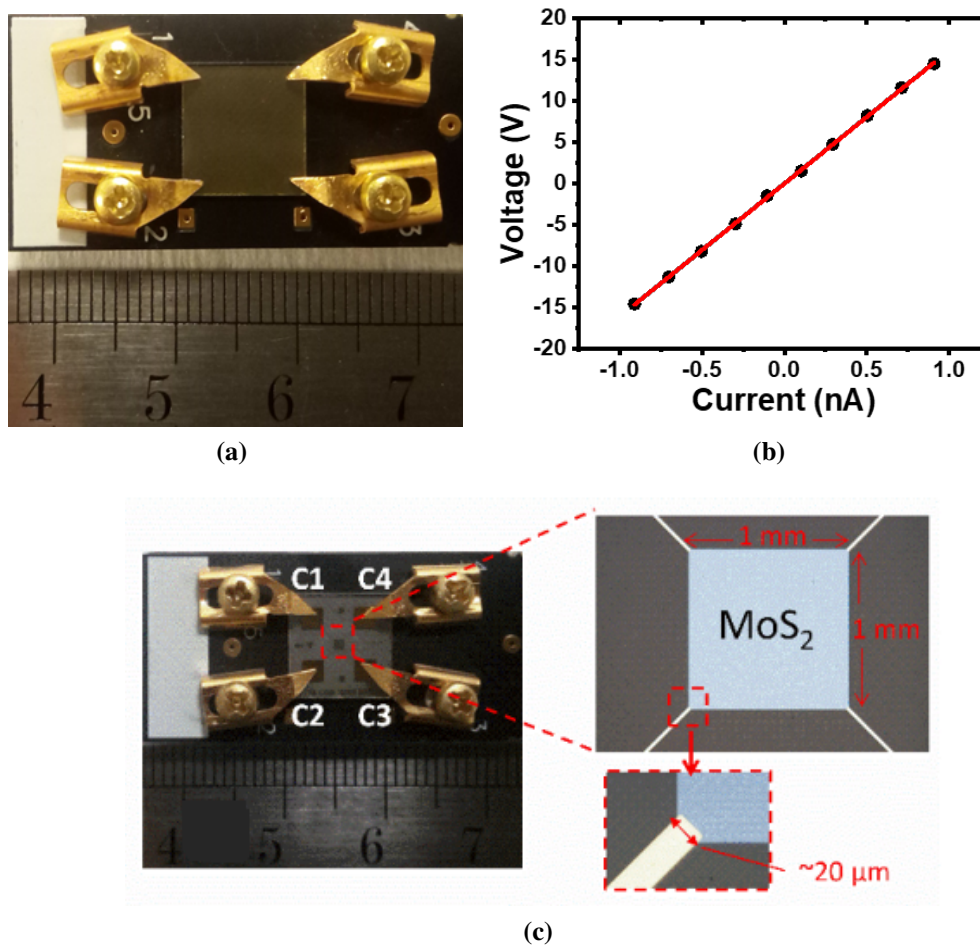


Figure 4.13: (a) non-patterned 1 cm x 1 cm MoS₂ film on sapphire or *a*-Al₂O₃/sapphire contacted for room temperature Hall effect/4-point (Hall/4P) resistance in a Van der Pauw (VdP) set up.(b) Perfect Ohmic behaviour of MoS₂ on sapphire from Hall/4P system. The 2-point (2P) resistance was then extracted from the slope. (c) Patterned 1 cm x 1 cm MoS₂ film on sapphire or *a*-Al₂O₃/sapphire with Ni/Au metal contacts. The zoomed-in inset shows the metal tracks going towards each of the 4 contact pads which forms a VdP structure. These measurements were done at room temperature.

Figure 4.14 displays the summary of Hall/4P/2P results for MoS₂ from several growth processes, substrates, and also patterned/non-patterned. A high resistivity range of (1.4– 3.3 kΩ cm) was found for all MoS₂ samples. Both unpatterned 550 °C MoS₂ films were n-type with low carrier concentrations on the order of 10¹⁴ cm⁻³. The electron mobility values were between 3.3 - 16 cm²/Vs. For lower growth temperatures of 350 °C and 450 °C, the carrier concentrations were in the order of 10¹⁵ cm⁻³. Though 450 °C gave n-type, 350 °C gives p-type. N-type behaviour has

been attributed to sulfur vacancy densities [229] while p-type behaviour has been connected to the oxidation of sulfur vacancies. [230] This oxidation can lead to an increase in $\text{MoS}_x\text{O}_{3-x}$ which gradually transforms n-type MoS_2 to p-type MoS_2 .

Defects in the CVD grown MoS_2 contribute to the low carrier concentrations where there are states in the MoS_2 energy gap. [110] These energy levels in the MoS_2 band gap can trap free carriers from any unintentional doping in the MoS_2 . As a reference, this phenomenon shares similarities with the early works on polycrystalline silicon, where grain boundaries defects needed to be saturated to get controllable semiconductor or pseudo-metallic behaviour. [231, 232] Gradually switching from n-type to p-type MoS_2 is observed by repetitions of electromagnetic or electrical testing. In addition to this, it is also observed that p-type behaviour is present after VdP patterning, with a comparable carrier concentration to that of non-patterned MoS_2 . Due to the low carrier concentration, only a small movement of the Fermi level can switch the type of MoS_2 . In this work, a possible movement of the Fermi level is attributed to the resist coating and removal during the patterning process.

<i>Growth Temp/ Substrate</i>	ρ_s ($\text{G}\Omega/\text{sq.}$)	ρ_s ($\text{k}\Omega\text{-cm}$)	<i>Carrier type</i>	n_s (cm^{-2})	n (cm^{-3})	μ (cm^2/Vs)
550°C Sapphire	3.561	2.315	n	1.05×10^8	1.62×10^{14}	16.72
550°C a- Al_2O_3 / Sapphire	5.768	2.596	n	3.28×10^8	7.29×10^{14}	3.30
450°C a- Al_2O_3 / Sapphire	2.351	1.411	n	1.09×10^9	1.82×10^{15}	2.44
350°C a- Al_2O_3 / Sapphire	3.483	2.961	p	3.69×10^9	4.34×10^{15}	0.49
550°C Sapphire (Patterned)	4.433	2.438	p	2.84×10^8	5.16×10^{14}	4.96
550°C a- Al_2O_3 / Sapphire (Patterned)	7.356	3.310	p	3.58×10^8	7.96×10^{14}	2.37

Figure 4.14: (a) Table containing Hall data from 3 MoS_2 samples on 2 different substrates, including the temperature at which each sample was grown. The results include resistivity, carrier type, carrier concentration and mobility.

For repeated electrical measurements, as mentioned previously, oxidation of the MoS_2

can cause switching from n-type to p-type. [230, 233] This coincides with XPS data recorded on MoS₂ on *a* – Al₂O₃/*sapphire* as seen in Figure 4.15 where MoS₂ is formed with the presence of Mo-based trioxides. This is further corroborated with activation energies in Figure 4.17, which will be discussed in more detail below.

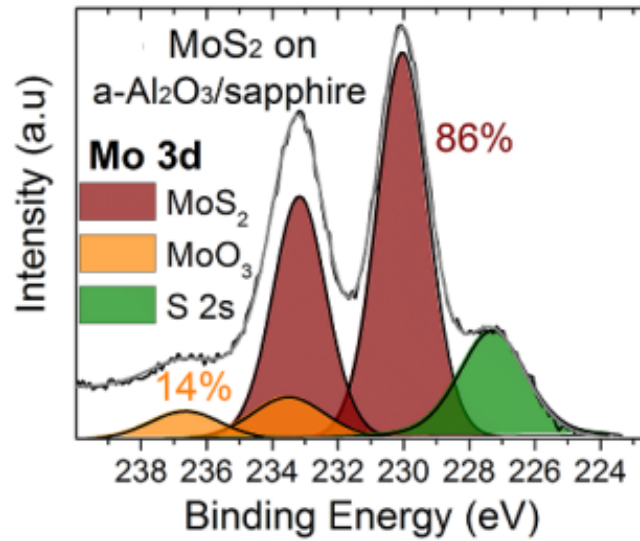


Figure 4.15: XPS of nominally 10 nm MoS₂ on *a* – Al₂O₃/*sapphire*, confirming that MoS₂ is formed with the presence of Mo-based trioxides.

Temperature dependent current-voltage (IV) measurements were also performed on patterned MoS₂ on *a* – Al₂O₃/*sapphire* (550 °C for 2.5 hours) using the Cascade Semiautomatic Prober MicroChamber. The metal contacts followed the same structure as that shown in Figure 4.13 (c). Since there were a number of different pathways, 3 separate routes were chosen, which are detailed on the bottom right of each plot. First, a baseline temperature of +25 °C was performed. Then, the system was brought down to -50 °C and tested. The temperature was systematically increased by 25 °C up until +100 °C. Finally, the sample was brought back to +25 °C. As seen in Figure 4.16 (a), (c) and (e) excellent Ohmic behaviour was obtained. Figure 4.16 (b), (d) and (f) shows that there is a slight change in resistance after the temperature dependent tests. However, this change is negligible and was not considered a problem for further investigations.

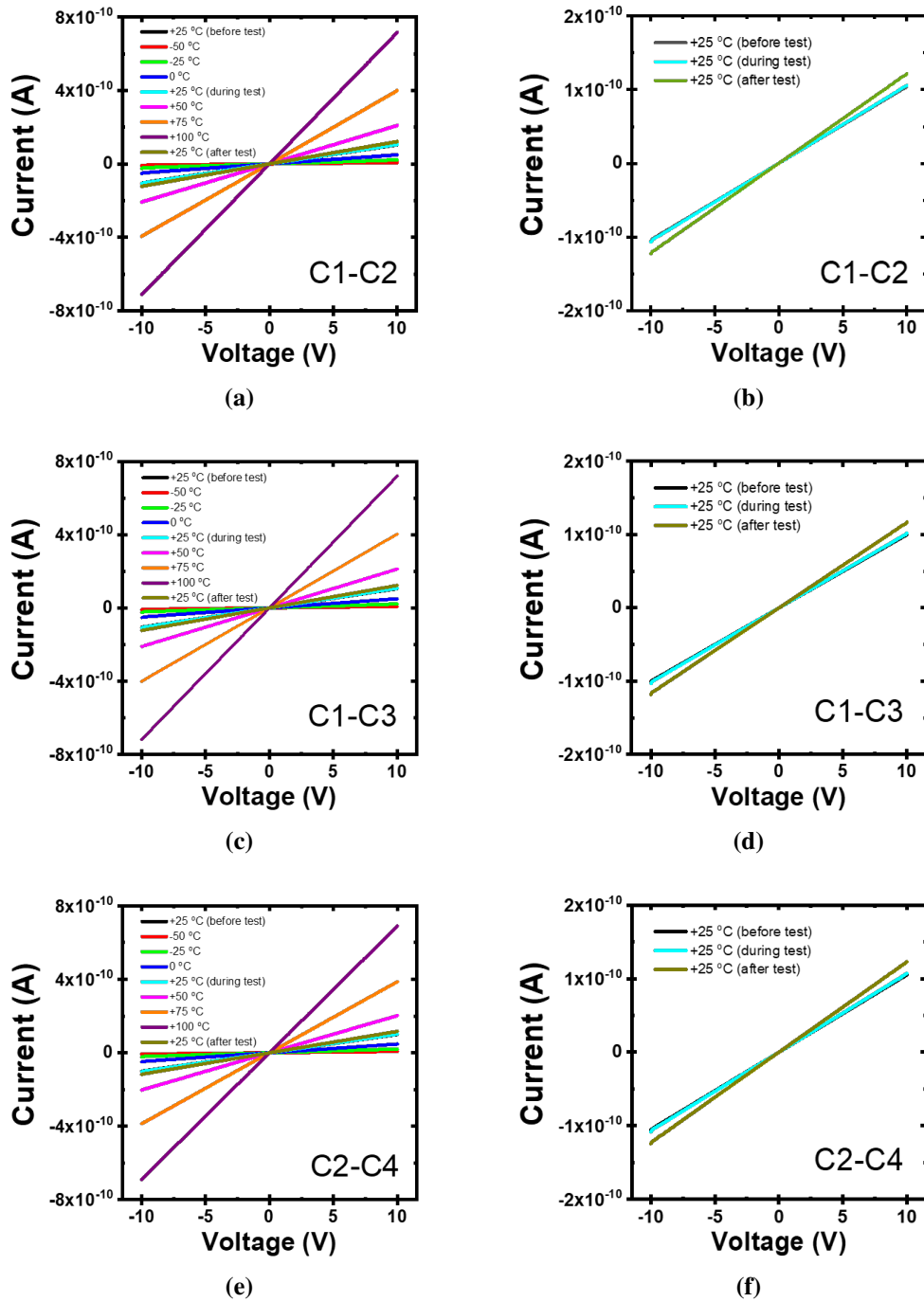


Figure 4.16: Temperature dependent current-voltage (IV) characteristics of CVD grown MoS_2 at 550°C for 2.5 hours done on the Cascade Semiautomatic Prober MicroChamber. (a), (c) and (e) present the IV characteristics of 3 different sites on the same sample (bottom right of each graph). The temperature range was between -25°C up to $+100^\circ\text{C}$. To investigate the effect of temperature on the material, the sites were first tested at $+25^\circ\text{C}$, at $+25^\circ$ during the temperature increase and finally at $+25^\circ\text{C}$ after the last test at $+100^\circ\text{C}$. (b), (d) and (f) represent the data.

As discussed with Figure 4.15, XPS showed the presence of oxidation of MoS_2 . Further investigations also point to the oxidation of MoS_2 . From the IV data, (Figure 4.16)

the activation energy at 2.5V, 5V, 7.5V and 10V for the same 3 sites were extracted, shown in Figure 4.17. The range of activation energies was between 0.214 eV - 0.216 eV. These results are consistent with the reported data by Neal et al where they attributed their activation energy of 0.214 eV to the oxidation of MoS₂ from exposure to air. [230] Our samples were stored in air and therefore is highly likely that our activation energy values are from the same phenomenon.

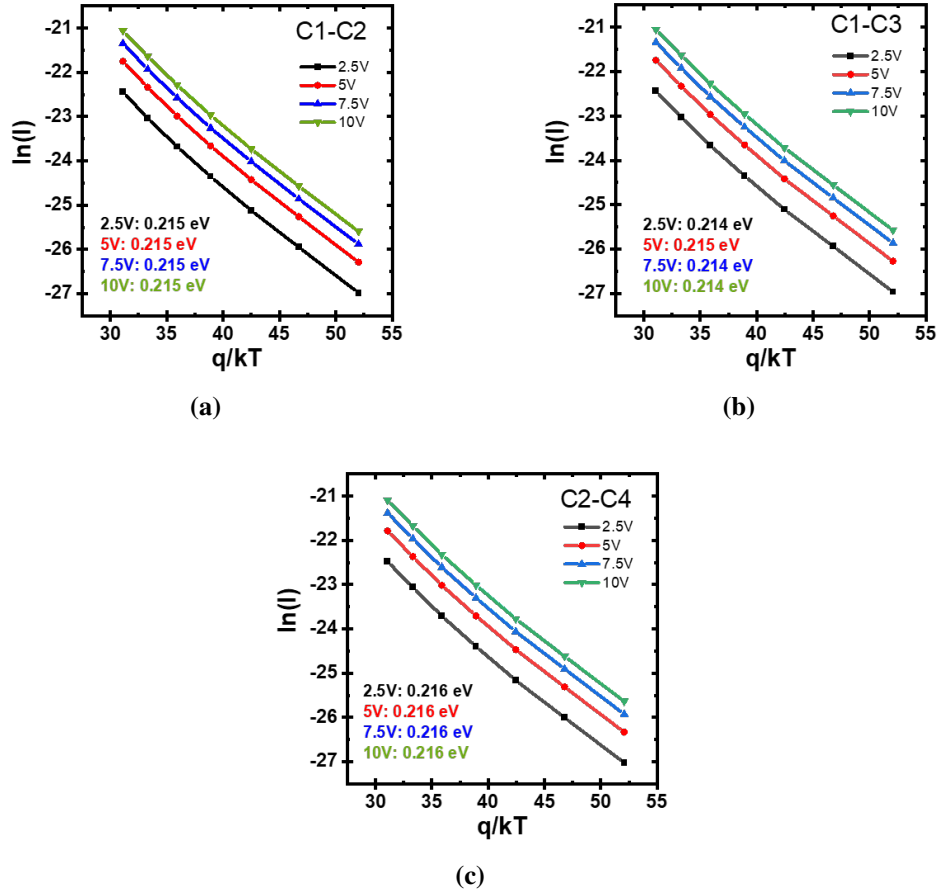
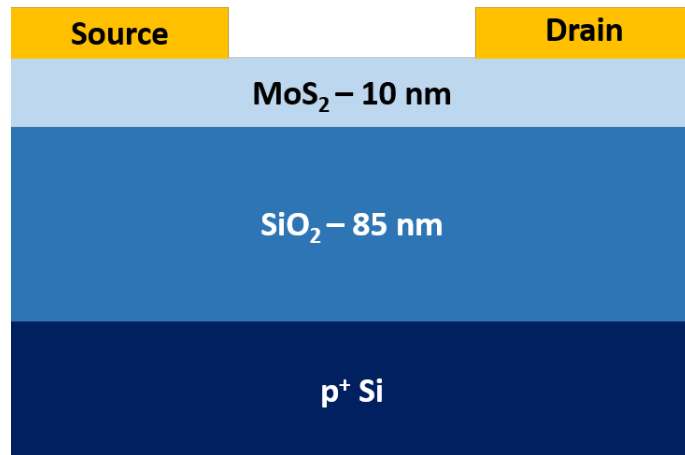


Figure 4.17: Activation energy extracted at 2.5V, 5V, 7.5V and 10V for 3 separate sites.. The individual sites are denoted in the top right corner. The activation energies were consistently between 0.214 - 0.216 eV. Each activation energy for each voltage is seen at the bottom left of each plot.

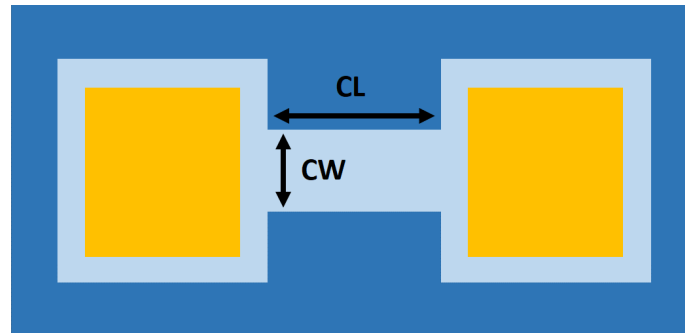
4.5 Back-Gated Transistors

The back-gated junctionless transistors were, as discussed earlier, Ni/Au contacts fabricated on ≈ 10 nm MoS₂ on 85 nm SiO₂/Si (p^+). These were used to investigate

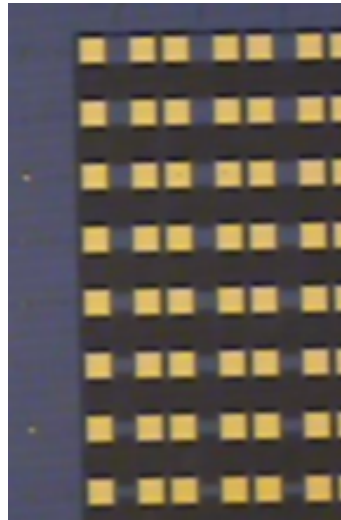
field-effect modulation of the lateral conduction. Figure 4.18 (a) and (b) shows 2 schematic diagrams of the transistor set-up. Figure 4.18 (a) shows a cross sectional schematic of the back-gated transistor. Dark blue is the Si (p^+) substrate, blue is the 85 nm SiO₂ oxide, light blue is ≈ 10 nm MoS₂ and finally the orange shows each source and drain metal contact. Figure 4.18 (b) shows a plan view of the back-gated transistor. The colours follow the same representation as in Figure 4.18 (a). The channel width (CW) and channel length (CL) are also shown here. CLs were varied systematically throughout the mask used when fabricating the devices. They ranged between 4 μm and 60 μm . CWs were also varied within a similar range of 15 μm to 50 μm .



(a)



(b)



(c)

Figure 4.18: Schematic diagrams of the transistor set-up. (a) Side view of the back gated transistor. Dark blue is the p^+ Si substrate, blue is the 85 nm SiO_2 oxide, light blue is 10 nm MoS_2 and finally the orange shows each source and drain metal contacts. (b) Top view of back gated transistor. The colours follow the same representation as in (a). The channel width (CW) and channel length (CL) are also shown. (c) Real image of FET devices.

Both output and transfer characteristics were investigated. Figure 4.19 and 4.20 present

these findings from a transistor with a CL of 10 μm and a CW of 25 μm . First, Figure 4.19 shows the output behaviour where I_{ds} is the drain-source current and V_{ds} is the drain voltage. The back-gate voltage, V_g , was swept through a series of voltage values, beginning with -33 V to +33 V, as seen on the bottom right of the plot. As observed on the graph, the results gave an I_{ds} of $\approx 1 \times 10^{-9}$ A at V_{ds} of 2 V. This compliments the previous results found in Hall. Hall data gave a carrier concentration of $1 \times 10^{14} \text{ cm}^{-3}$ and a mobility of $10 \text{ cm}^2/\text{Vs}$. At flat band potential, there is no depletion layer at the junction hence stopping band bending of the valence/conduction bands.[234]. Here, at flat band, the following equation is used

$$I_{ds} = qn\mu \left(\frac{V_{ds}}{L} \right) (Wt) \quad (4.2)$$

where I_{ds} is drain-source current, V_d is drain voltage, q is electronic charge, n is carrier concentration, μ is mobility, L is channel length, W is channel width and t is thickness. Using the values found from Hall and implementing the same channel dimensions as used for the FET measurement (CL of 10 μm and a CW of 25 μm), this equation predicts that at a V_{ds} equal to 2 V, the corresponding I_{ds} gives 1×10^{-9} A. This is an important finding as it shows consistency between both Hall analysis and probe analysis data.

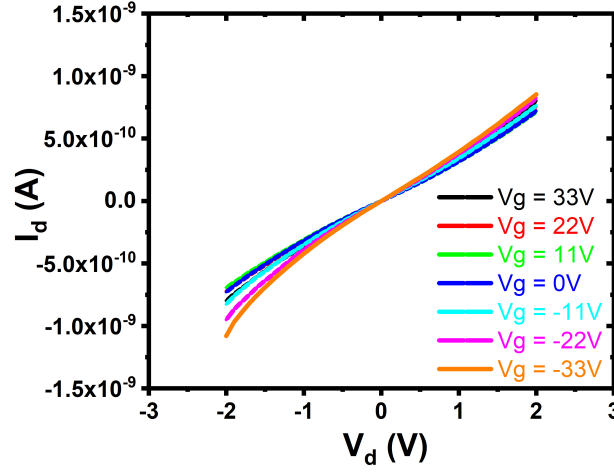


Figure 4.19: Back gated ≈ 10 nm MoS₂ on SiO₂ showing Room temperature output characteristics at varied V_{gs} .

Next, the transfer characteristics are discussed, as seen in Figure 4.20. Here, V_g was varied between -35 V and +35 V. The inset shows the data in log form, and as seen, there is negligible modulation. Comparing these results with physical traits found in previous tests, the lack of variation of I_{ds} is most likely attributed to the large density of charge trapping defects within the MoS₂ energy gap. [110] Additional charge on the back gate is compensated by trapped charge in the MoS₂ energy gap. This restricts the movement of the Fermi level in the MoS₂ when voltage is varied on the back gate. This behaviour is similar to amorphous or polysilicon thin film transistors without reduction/passivation of defects within the energy gap.[231, 235] The charge trapping density can be calculated using the data from Figure 4.20. If the Fermi level motion in MoS₂ is pinned by the gap state defects in MoS₂ then the effective density of gap states should be enough to pin the Fermi level at the MoS₂/oxide interface over the applied gate voltage range of ± 35 V. This is the maximum voltage range used as seen in Figure 4.20. To calculate the amount of charge trapping needed to restrict Fermi level movement, the following equation is used

$$Q_t \geq C_{ox} \frac{\Delta V}{q} \quad (4.3)$$

Where Q_t is charge trapping, C_{ox} is oxide capacitance, δV is change in voltage and q is elementary electronic charge. For a positive back-gate voltage, an oxide capacitance of (85 nm SiO_2) of $4.06 \times 10^{-8} \text{ F/cm}^2$ and a δV of 35 V, the density of trapped charges needed to stop movement in the Fermi level (of MoS_2) is estimated to be $\approx 1 \times 10^{13} \text{ cm}^{-2}$. When the small grain size for this material is considered ($\approx 10 \text{ nm}$), this corresponds to a trap charge volume of $\geq 1 \times 10^{19} \text{ cm}^{-3}$.

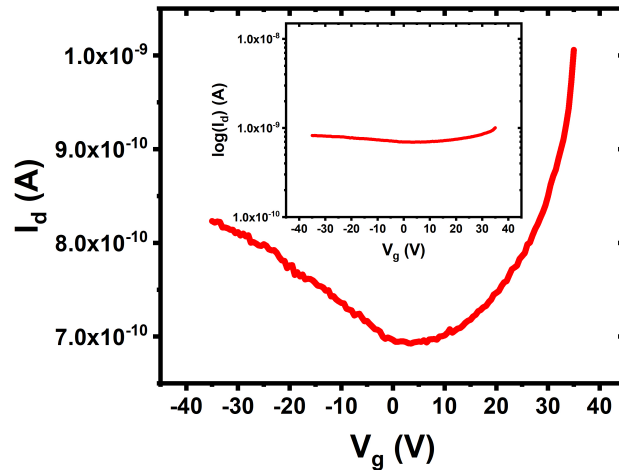


Figure 4.20: Back gated $\approx 10 \text{ nm}$ MoS_2 on SiO_2 showing Room temperature transfer characteristics at $V_{ds} = 2 \text{ V}$ and swept between a $V_g \pm 35 \text{ V}$. Negligible field modulation is observed, most likely attributed to a high density of carrier-trapping defects and grain boundaries.

4.6 Conclusion

Rapid and repeatable growth of MoS_2 on glass, sapphire, $\text{a-Al}_2\text{O}_3/\text{sapphire}$, and SiO_2/Si is achieved by CVD growth at temperatures of 350°C , 450°C and 550°C . These depositions were performed in an industry friendly 300 mm ALD reactor and stays at and below the thermal budget for BEOL integration. Many structural and chemical tests were performed to confirm polycrystalline MoS_2 . Extensive Raman analysis was conducted, which further proved the successful growth of uniform 10nm MoS_2 . Hall/4P/2P analysis, which is rarely found in literature, indicates high resistivity ($\approx 1.4 - 3.3 \text{ k}\Omega \text{ cm}$), low carrier concentrations ($10^{13} - 10^{14} \text{ cm}^{-3}$) and Hall mobilities of $\approx 0.5 - 17 \text{ cm}^2/\text{Vs}$. Our mobility values of devices, grown at temperatures of 550

°C - 350 °C, are the highest compared to other studies done on CVD grown MoS₂. [46–48, 236–239] Independent measurements on FET devices, corroborated with Hall data. This work has helped the research into emerging materials and devices for 3D heterogeneous integration.

Chapter 5

Physical and electronic properties of WS₂ grown by an atomic layer deposition process

5.1 Introduction

The transition metal dichalcogenide WS_2 has been actively researched for many years, in some cases through fundamental precursor chemistry or synthesis material studies [180–183] or with a specific application area in mind such as lubricants [184–187], batteries [188, 189], photovoltaics [190], sensors [191], opto-electronics [192], or catalysis [62]. In relation to nanoelectronic applications, WS_2 is of particular interest due to its semiconductor nature and indirect bandgap, 1.3 eV - 1.4 eV in bulk form [193–196]. The possibility of fabricating field-effect-transistors (FETs), and complementary-metal-oxide-semiconductor (CMOS) circuits has stimulated research into this exciting TMD material. While work on mechanically exfoliated flakes of 2D materials generates valuable insight into the physical and electronic properties of these material systems, [240–242] it is generally accepted that large area synthesis is required to take the research to the next stage [243–245]. Atomic layer deposition (ALD) is CMOS compatible, and enables precision deposition of large area novel materials on the nanometer thickness scale [246, 247], a compositional control, conformity to 3D surfaces and at relatively low processing temperatures.

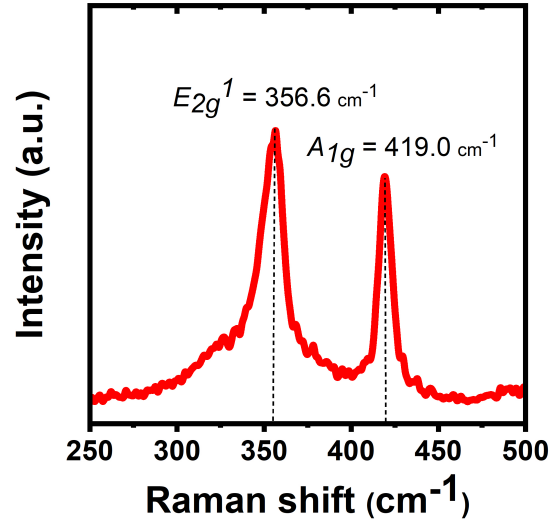
For most practical nanoelectronics applications, large-area high-quality thin-films will be required, and this is our focus here. In terms of electronic demonstration of ALD WS_2 FETs, the number of studies are few. Dorow et al [63] and Lin et al [64] fabricated FETs using CVD films and both showed benchmarking of the latest WS_2 thin-films FETs. Schram et al. compared ALD and CVD WS_2 FETs with low-temperature device integration flows, and highlighted substrate adhesion issues [65]. Recently, Yang et al [66] produced impressive ALD WS_2 FET I_{on}/I_{off} ratios of 10^5 , as well as Nb-doping in ALD deposited WS_2 films [67]. With that in mind, we investigate the structural and electrical behaviour of ALD grown WS_2 . We report Hall analysis of the WS_2 films as well as an examination of the temperature dependency

of the bulk WS₂ resistivity and specific contact resistivity based on electrical Circular Transfer Length Method (CTLTM) structures.

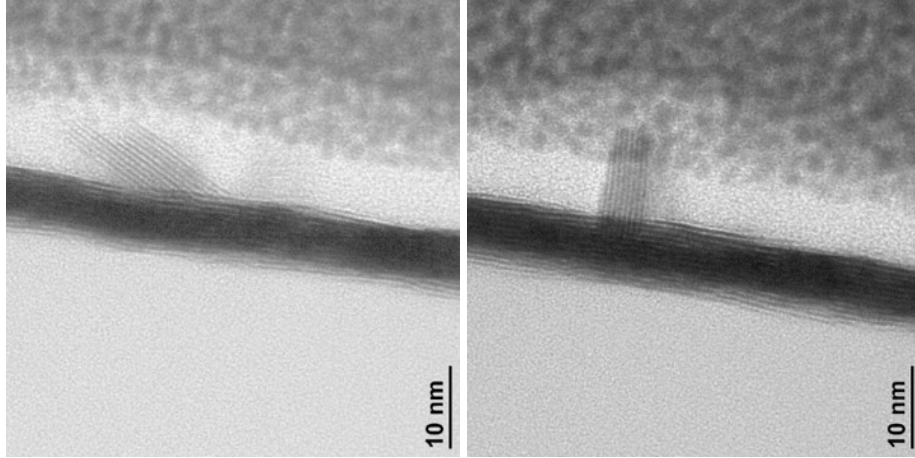
5.2 Results and Discussion

5.2.1 Physical Characterisation

Experimental procedures are discussed in the methodology chapter. For WS₂, the Raman spectra includes 2 Brillouin zone first order modes - E_{2g}¹ and A_{1g}. At $\lambda_{exc} = 514$ nm, the E_{2g}¹ peak is found at 356.6 cm^{-1} and A_{1g} at 419.0 cm^{-1} . These results, as seen in figure 5.1 (a) agree with those found in literature [248]. Cross section TEM images of the WS₂ films are shown in Figure 5.1 (b), (c). The cross sectional analysis reveals the WS₂, where the layered structure is primarily parallel to the SiO₂ surface. The average thickness of the WS₂ film is 8 nm, corresponding to 13 monolayers of WS₂, with an interlayer spacing of 0.62 nm. The cross sectional TEM analysis also indicates some out of plane features, which can be at an angle to (a) or perpendicular (b) to the WS₂ film. These features are consistent with the observations in [44], and the height of the perpendicular feature is around 10 nm above the planar WS₂ surface.



(a)



(b)

(c)

Figure 5.1: (a) Raman shift data of WS₂ showing the presence of characteristic WS₂ peaks - E_{2g}^1 and A_{1g} . (b) Cross sectional TEM image of WS₂ on SiO₂. (c) Cross sectional TEM image of WS₂ on SiO₂ taken from a different site.

Figure 5.2 (a) shows a 10 μm x 10 μm AFM scan before CTLM device processing. The pre-processed RMS (root mean square) gave a value of approximately 1.3 nm while a post-process AFM scan gave a value of 3.8 nm. We propose that this increase in surface roughness is linked with surface degradation due to ambient organic contaminants [249–251]. The vertical features have already been investigated by Balasubramanyam et al and they adjusted the growth process to reduce the formation of vertical nanostructures using a H₂ plasma [136]. These fins survived the device process and Figure

5.2 (b) shows a graph representing 4 line profiles within the 10 μm by 10 μm scan. The 3 nm scale bar shows the general surface roughness while we theorize the peaks above to be the fins. A statistical analysis on the number of peaks per 2 μm was performed. Over 20 scans, the average number of peaks was 4.25. If we compare this to work done by Balasubramanyam et al we find a close correlation between the two [136]. The profile lines were taken at different orientations and directions. The width of the fins cannot be picked up on these particular line scans, just the height. This is due to the width and length of the fins being around 5 nm and 25 nm and the step size of the AFM line scan is 25 nm while the scan covers 2 μm with a 25 nm step size. As a consequence, whatever the orientation of the fin to the line scan, the height is the only parameter affecting them. Figure 5.1 (b) and (c) show that some fins grow at an angle while others grow directly vertical.

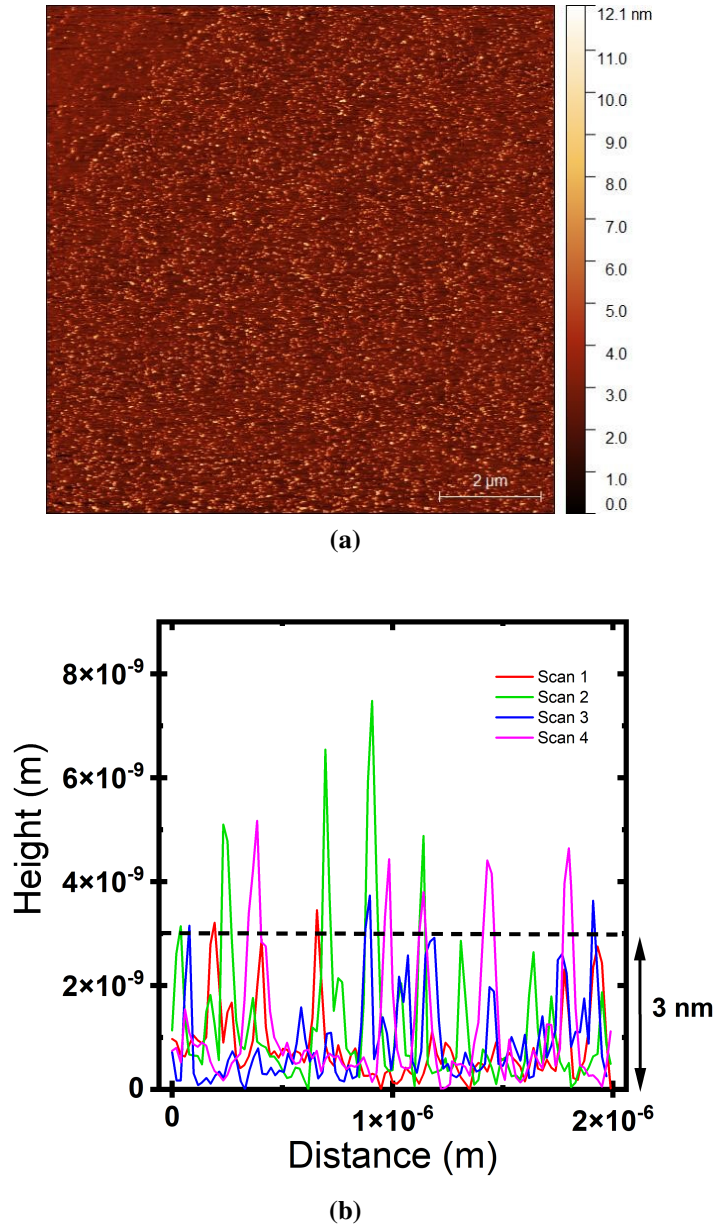


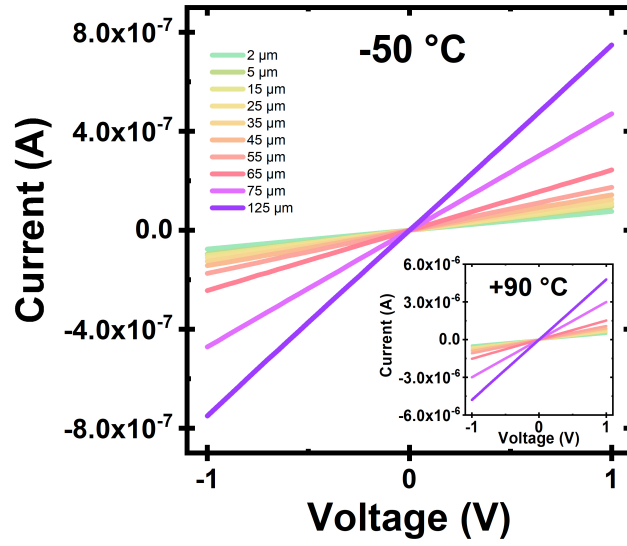
Figure 5.2: (a) 10 μm x 10 μm AFM image of WS₂ pre device processing. (b) Line profiles from (a) across a length of 2 μm.

5.2.2 Electrical Characterisation

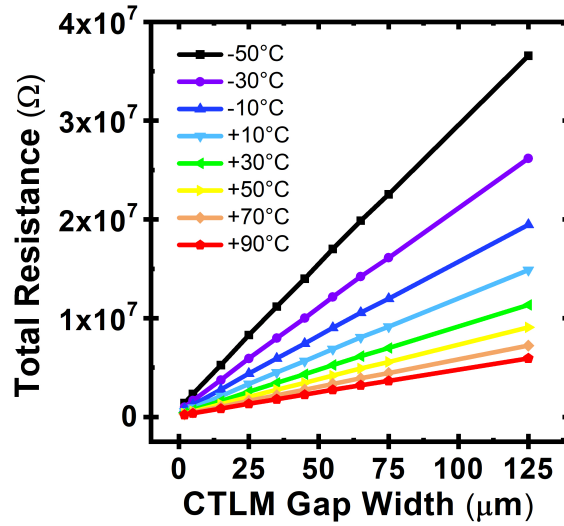
In this work we analysed the Hall effect mobility of the WS₂ films prior to any device fabrication. 2-point (2P) resistance, 4-point (4P) resistivity and DC/AC Hall-effect analysis was carried out on a cm^2 sample at room temperature. It was only possible to obtain results from 2P, 4P and DC Hall measurements (AC Hall failed due to a low signal to noise ratio). 2P Ohmic average resistance shows 1.6

$\times 10^7 \Omega$. Results show a 4P average resistance of $5.5 \times 10^5 \Omega$, with a 4P sheet resistance of $2.4 \times 10^6 \Omega/\text{sq}$ and 4P resistivity of $2.0 \Omega \text{ cm}$. The DC Hall results can only be described as weakly indicative since the SNR is only 3.8:1. The same can be said on a number of other parameters extracted from the DC Hall results which indicate p-type WS_2 with a mobility of $\approx 23.2 \text{ cm V}^{-1} \text{ s}^{-1}$ and carrier concentration of $1.31 \times 10^{17} \text{ cm}^{-3}$. While our DC Hall results had a SNR of 3.8:1 it is noted that Balif et al [252] also observed p-type behaviour in thin film WS_2 (100 nm to 200 nm) with Hall mobility of $10 \text{ cm V}^{-1} \text{ s}^{-1}$. In this work the WS_2 was formed by reactive rf sputtering of a Sulphur rich WS_{3-4} film, which was subsequently annealed for 1 h under argon flow at 850°C or 950°C . 4P resistivity measurements gave a signal to noise ratio (SNR) of 370:1 at room temperature (21°C).

We can also compare the Hall values to the temperature dependent electrical measurements. The inner diameter was $25 \mu\text{m}$, and the separation values available were between $2 \mu\text{m}$ and $125 \mu\text{m}$. CTLM structures on WS_2 were tested electrically between 50°C and $+90^\circ\text{C}$. At each temperature, the sample shows Ohmic behaviour, as seen in Figure 5.3 (a). The total resistance versus separation is derived using standard methods by applying a geometrical correction factor [253] and is represented in Figure 5.3 (b). From this total resistance, a number of parameters can be extracted. The sheet resistance (R_{sh}) at room temperature is calculated at $1.58 \times 10^7 \Omega/\text{square}$. Transfer length gives $1.73 \times 10^{-4} \text{ cm}$, a specific contact resistivity of $0.46 \Omega \text{ cm}^{-2}$ and contact resistance (R_c) of $1.71 \times 10^5 \Omega$.



(a)



(b)

Figure 5.3: (a) Electrical data from the CTLM devices. Representative current versus voltage taken on each site at $-50\text{ }^{\circ}\text{C}$ for different gap spacing's in the CTLM structure. Inset shows data at $+90\text{ }^{\circ}\text{C}$. (b) Total resistance for each gap spacing at various temperatures, after applying the usual CTLM geometrical correction factor

Table 1 compares 4P and CTLM results at room temperature. The R_{sh} value obtained from the CTLM structures is approximately 5 times larger than on the unprocessed WS_2 film. We attribute this to the impact of the processing required to form the CTLM structures, which involves the deposition of resist, UV exposure, metal deposition and a lift off process. It is noted that from the Hall analysis of the film, the hole carrier

concentration is $1.31 \times 10^{17} \text{ cm}^{-3}$. For a film thickness of 8.6 nm this corresponds to a total sheet charge of $1.54 \times 10^{11} \text{ cm}^{-2}$. It is expected that the exposed WS_2 surface will have a surface charge, and any change in this surface charge density during the CTLM processing will change the associated R_{sh} of the WS_2 . Any slight change to the surface, in this case metal patterning, will impact the R_{sh} . Structures will change when connecting this consideration with the AFM data showing a change in surface roughness following device processing. It is not surprising that there is a difference in R_{sh} values obtained from the Hall analysis and the CTLM data. It must be noted that the sample was halved - one for Hall and the other for electrical characterisation.

Property	Units	4P	CTLM
Resistivity	$\Omega \text{ cm}$	2.0	12.9
R_{sh}	Ωsq	2.38×10^6	1.58×10^7
R_c	Ω	1.58×10^7	1.71×10^5

Table 1. Resistive properties of WS_2 from 4 point probe and CTLM electrical probe data.

The temperature dependence of the WS_2 resistivity and specific contact resistivity of R_{sh} and R_c are shown in Figure 5.4 (a) and (b) respectively. In general, the bulk E_a is equal to the sum of the activation energy values of the carrier mobility and the carrier concentration. This can be explained using the following equation where σ is conductivity, q is the charge of electron, n is carrier concentration and μ is mobility -

$$\sigma = q.n.\mu \quad (5.1)$$

Then, we look at Eq. (5.2) and (5.3) for the activation energy of both carrier concentration (n) and mobility (μ) using the Arrhenius Equation. k_1 and k_2 are the preexponential factors, E_a and E_b the activation energies, k the Boltzmann constant and T the temperature.

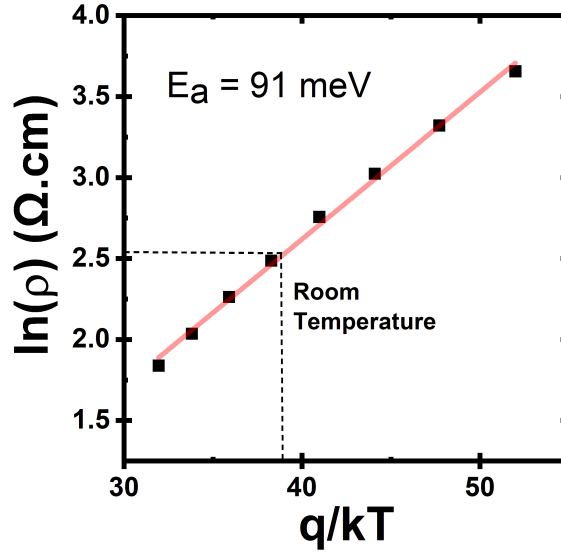
$$n(T) = k_1 \exp \frac{-q(E_a)}{kT} \quad (5.2)$$

$$\mu(T) = k_2 \exp \frac{-q(E_b)}{kT} \quad (5.3)$$

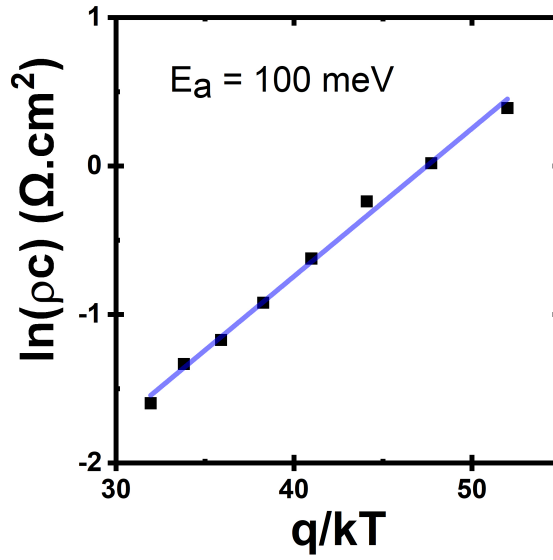
Finally, subbing (5.2) and (5.3) back into (5.1) but instead of conductivity, we present it in terms of resistivity ρ .

$$\rho = \frac{1}{q.k_1.k_2 \exp \frac{-q(E_a+E_b)}{kT}} \quad (5.4)$$

It can be concluded that the activation energy of the total reaction is the sum of the activation energy of the carrier concentration and activation energy of the mobility. For specific contact resistivity, the activation energy is determined to primarily be the doping concentration in the WS₂, which determines the barrier height and tunneling distance. For the bulk WS₂ resistivity, the activation energy can be influenced by both mobility and carrier concentration. The activation energy of specific contact resistivity (100 meV) and resistivity (91meV) are close in value. With both having nearly equal gradients, this suggests little temperature dependence of carrier mobility in the WS₂, which is consistent with the surface roughness observed in the TEM and AFM analysis. For this reason, we propose that carrier concentration dominates the activation energy for both parameters.



(a)



(b)

Figure 5.4: (a) Activation energy of sheet resistivity with corresponding resistivity value at room temperature which calculates to be 9 Ω cm (b) Activation energy of specific contact resistivity

5.3 Conclusion

In summary, our work demonstrates that plasma ALD deposited 8.6nm WS₂ exhibits a p type behavior where the unintentional doping concentration of $1.31 \times 10^{17} \text{ cm}^{-3}$ and an indicative hole mobility of $23.2 \text{ cm V}^{-1} \text{ s}^{-1}$. Analysis of the temperature

dependence of the bulk WS₂ resistivity and the specific contacts resistivity between the WS₂ and the Ni(20 nm)/Au(200 nm) contacts exhibit similar activation energy values of 91 meV and 100 meV, consistent with both activation energy values being controlled by the temperature dependence of the hole concentration. This work adds to the little literature available of mobility and resistivity values of ALD grown WS₂.

Chapter 6

Investigating the impact of Laser Annealing on the structural and electronic properties of MoS₂ thin films

6.1 Introduction

Modifying the properties of Transition Metal Dichalcogenide (TMD) materials is a research area which has emerged in recent years [68–71]. Short time laser processing has adjusted TMDs by doping [72], phase transformation [73–75], localised patterning [76, 77], thinning or etching [78–80] and site-specific modification [81, 82]. However, with its positive possibilities comes its challenges. Laser conditions can vary considerably depending on a number of parameters - wavelength, repetition, laser source and pulse duration. As well as the laser conditions, results can fluctuate due to substrate type, what TMD is being tested, processing aims and the ultimate application required.

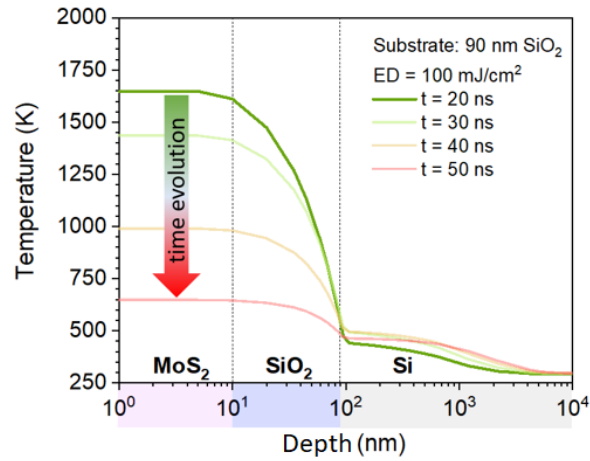
The aim of this research activity was to show an in-depth investigation into synthesizing crystalline MoS₂ layers on wafer scale area, where MoS₂ films deposited on Si and Si/SiO₂ surfaces are explored. The role of a SiO₂ on Si substrate and 248 nm KF laser is shown. This method shows that within the correct parameter range, the process can produce crystalline MoS₂ films with small domains size of around 3.5 nm, from an initially amorphous MoS₂ film. Field effect transistors formed in laser annealed MoS₂ show limited I_{ds} variation with V_{gs} consistent with the small domain size.

6.2 Results & Discussion Pre Device Fabrication

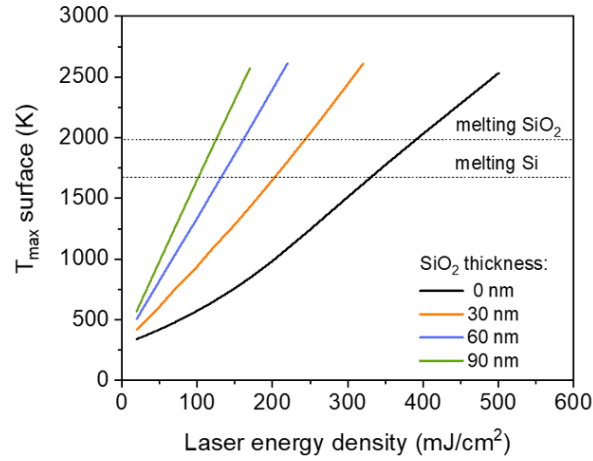
6.2.1 LIMP Software Calculations

All experimental results are discussed in the methodology chapter. With the help of LIMP software [254] (Harvard University), heat flow calculations were performed [255, 256]. Despite the model not giving a prediction for the amorphous to crystalline phase transformation of MoS₂, important details were uncovered about the thermal budget. The progression of temperature strongly depends various parameters - laser

energy density, number of pulses, substrate choice and substrate thickness. Figure 6.1 (a) displays the time-evolution of temperature throughout the depth of the sample. The SiO₂ acts as a buffer for the heat dissipation between the MoS₂ and Si substrate, which enables the ability to laser anneal at higher temperatures. The Si substrate always remained below 500 K. Calculations were done by varying the energy density from 20 to 500 mJ cm⁻² for substrates with a SiO₂ layer thicknesses 0, 30, 60 or 90 nm as seen in Figure 6.1 (b). It shows that substrate damage can occur if the energy density is too high, causing a fatal temperature increase and degrading the MoS₂ film. The calculations suggested that melting of the Si substrate can happen with anything over 325 mJ cm⁻². To limit the potential of melting, a 90 nm SiO₂ substrate was chosen with a laser energy densities between 100 - 150 mJ cm⁻². Due to the temperature of the Si substrate staying well below the BEOL temperature limit [257], this laser annealing process shows promise for Si CMOS technology.



(a)



(b)

Figure 6.1: (a) Time-evolution of temperature following a laser pulse as it begins at the top MoS₂ and down through the SiO₂-on-Si substrate. (b) Maximum surface temperature T_{max} as a function of laser density of energy and SiO₂ film thickness.

6.3 Physical Characterisation prior to FET Fabrication

6.3.1 Raman Analysis

A number of physical characterisation tests were performed on these samples. Figure 6.2 (a) shows the Raman spectra of MoS₂ for an energy density of 1000 mJ cm^{-2} and the number of pulses varying between 1 - 8. A single pulse gives a weak signal but from

2 pulses upwards, there is a steady improvement of peak intensities. A broadening of the E_{2g}^1 peak is seen as the number of pulses increase. This may be a consequence of crystalline defect formation as these defects give rise to disorder-activated vibration modes at 358 and 377 cm^{-1} [258]. Following this, the laser annealing process was further diversified, alternating both laser energy density and amount of pulses. This is represented in Figure 6.2 (b) as a function of A_g^1 peak height. The blue in the colour bar represents the lowest height values of the A_g^1 peak (less ordered MoS₂) while the red represents the highest A_g^1 peak values (more ordered MoS₂). Raman signals were recorded at 100 mJ cm^{-2} with 2-8 pulses. With the most intense peak found at 8 pulses, one would assume that this laser annealing process gives the optimum MoS₂ quality. However, when further physical characteristic investigations were performed, namely RBS and TEM measurements, this assumption was refuted, showing the importance of implementing a large scale characteristic study on these samples.

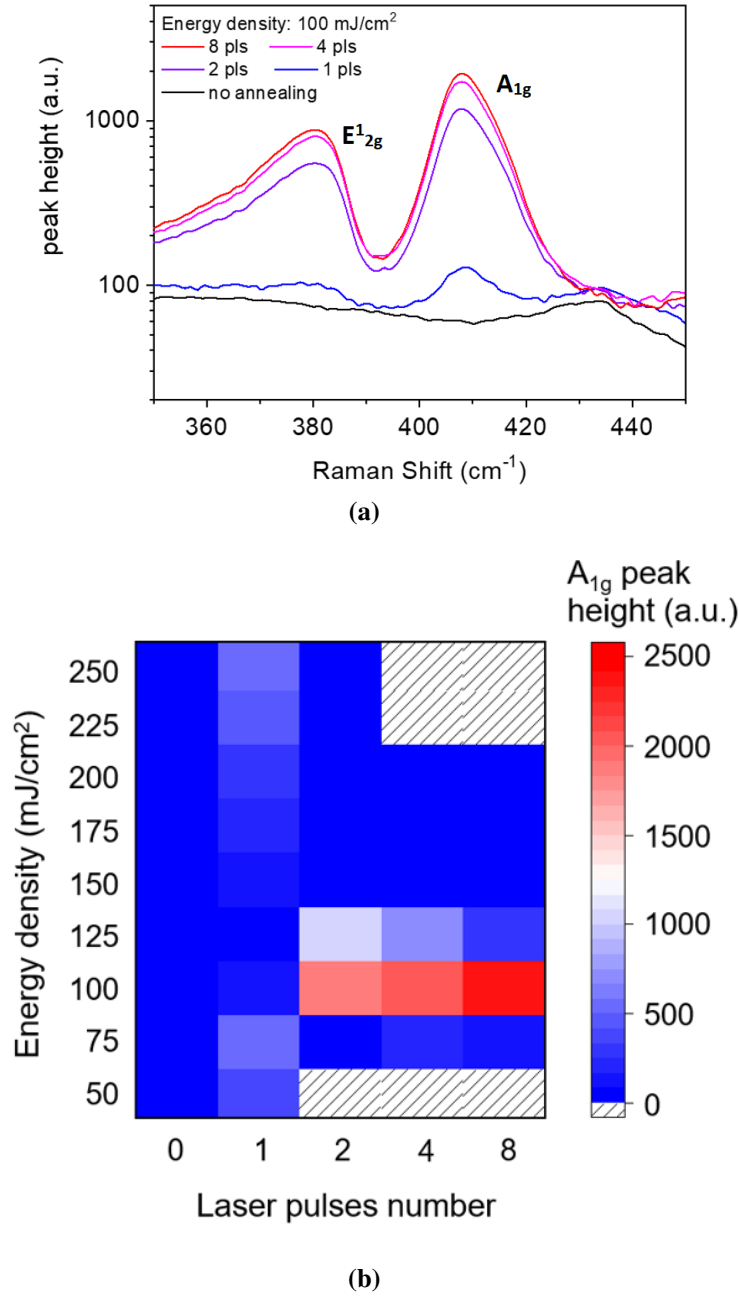


Figure 6.2: (a) MoS₂ grown Raman spectra on SiO₂-on-Si substrates with laser energy of 100 mJ cm⁻² (b) height of the A_{1g} peak with respect to the Raman spectra. The laser conditions vary in number of pulses and laser energy density. All the samples were processed under N₂ flux.

6.3.2 RBS Analysis

RBS measurements were carried out to estimate the structural variation of S and Mo occurring in the samples grown on SiO₂. RBS provides quantification of the elements present in the thin film as well as their concentrations per unit area. The results can be

seen in Figure 6.3 where the S/Mo dose ratios measured are presented as a function of the laser energy density and the number of laser pulses. Keep in mind, the optimum RBS S/Mo ratio for the stoichiometric composition of MoS₂ is 2:1. For all amorphous MoS₂ with no laser annealing, the S/Mo dose ratio equaled 2.1. As laser annealing is introduced, this ratio begins to change. Regardless of energy density, after a single laser pulse, the S areal dose significantly decreased to a S/Mo ratio of about 1.0 - 1.2. This decrease of dose ratios continued with an increase in pulses. When the energy density was increased from 100 mJ cm⁻² to 200 mJ cm⁻², the ratio of S/Mo also deteriorated. At a glance, these values seem to completely contradict the results gathered from the Raman spectra. There, the higher the number of pulses, the better the quality of MoS₂ Raman peaks. However, here, RBS tells us the opposite - the higher the number of pulses, the worse the S/Mo ratio gets. In order to make sense of this seemingly conflicting data, TEM and EDX was performed.

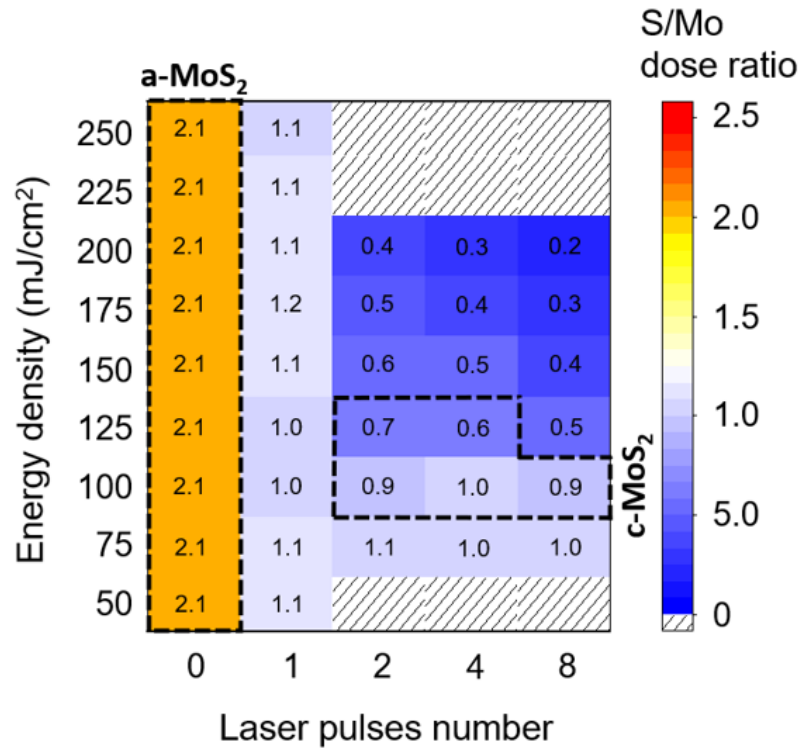


Figure 6.3: RBS results showing S/Mo dose ratios measured as a function of the laser energy density and the number of laser pulses.

6.3.3 TEM & EDX Images

Transmission electron microscopy (TEM) and energy dispersion X-ray (EDX) images were performed to understand the physical structure of these samples and helped to identify the reasoning for the discrepancies between Raman and RBS data. Cross sectional TEM images were taken of MoS₂ with 4 pulses at 100 mJ cm⁻². As seen in Figure 6.4, some dome-like defects were found. They measure to be $\approx 50 - 60$ nm in width. These protrusions can also be related to the AFM images, which are discussed later. Using EDX-compositional analysis, it was found that these hemispherical defects are clusters of Mo, S and O - also Figure 6.4. The energy density of 100 mJ cm⁻² causes a maximum surface temperature of 1650 K for 20 ns - ie 1 laser pulse length. Though this is well below the melting point of MoS₂ of 2375° C, sublimation of MoS₂ can begin at around 1000° C [259]. Here, we theorise that the effects of sublimation forms clusters of dome defects. When comparing these results to the RBS ratios of 1:1 for S/Mo, sublimation formation of MoS may be due to the loss of S through the formation of SO and SO₂. Even in N₂ ambient, there can still be traces of moisture. In addition, O could have been adsorbed onto the MoS₂ before laser annealing. It must also be noted that many of the measurements had to be performed in air (where instruments were placed in labs), which of course opens up the samples to possible oxidation of S. With a number of potential causes of oxidation, it is no surprise that some clusters also included O. (ie. MSO)

Though the RBS and TEM/EDX seem to relate, the Raman results still asks the question - why does the Raman spectra improve with increasing pulses? The answer, we believe is in the detail of what exactly Raman and RBS test. The Raman collects data from the poly crystalline MoS₂, but does not include the amorphous region. Though the Mo:S ratio is very low, the Raman can still pick up poly MoS₂ regions. The layers do not need to be continuous to be detected by Raman. They do need to have a contin-

uous percolation path for electrical measurements above the noise floor.

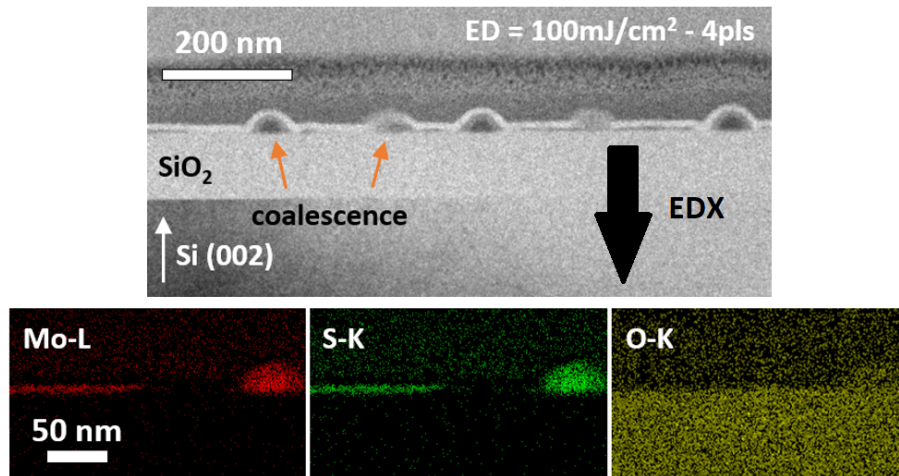


Figure 6.4: TEM and EDX of MoS₂ made with an laser energy density of 100 mJ cm^{-2} . Dome-like protrusions can be seen in the TEM, measuring at $\approx 50\text{-}60 \text{ nm}$. The EDX shows the presence of Mo, S and O in these defects.

Figure 6.5 (a) - (c) shows high resolution TEM images of various MoS₂ polycrystalline layers with a (002) dominant orientation. This coincided with XRD results, which will be discussed further on. The samples with an ED of 100 mJ cm^{-2} , with 1 pulse or 4 pulses of laser annealing, gave the most ordered results of MoS₂. However, they are not perfectly continuous layers, with many gaps and uneven surfacing. A single pulse at 150 mJ cm^{-2} showed some layers but the quality of crystallinity was poor, in keeping with other experimental results.

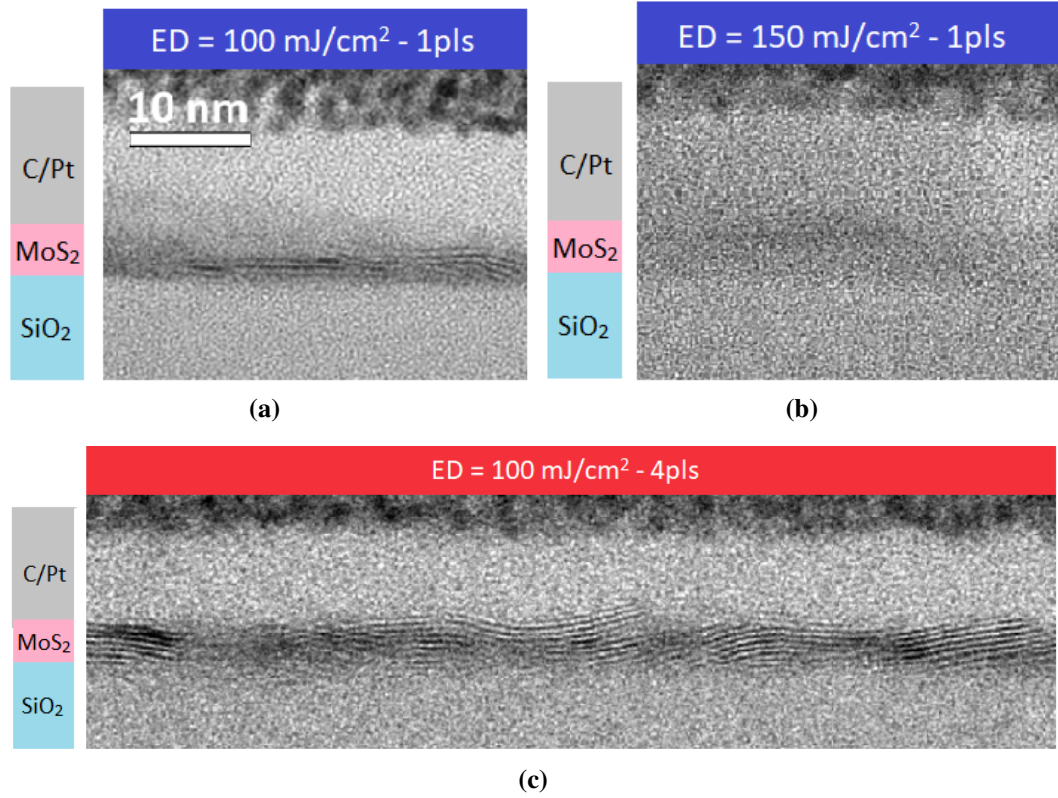


Figure 6.5: HR-TEM of 3 separate samples post laser annealing. (a) 1 pulse at 100 mJ cm^{-2} shows layered but unordered MoS₂. (b) 1 pulse at 150 mJ cm^{-2} shows very little evidence of MoS₂. (c) 4 pulses at 100 mJ cm^{-2} shows layered but unordered MoS₂.

6.3.4 AFM Analysis

AFM was performed to image the sample's micro-structure morphology post laser annealing. As seen in Figure 6.6 (a), large, low-density coalescence formations ($\approx 100 \text{ nm}$) appear on samples grown at an energy density of 75 cm^{-1} . As the energy density increased (in stages) up to 200 cm^{-1} the AFM showed a decrease in the lateral size of defects to $\approx 50 \text{ nm}$. These lateral sizes are comparable with the size of defects documented in TEM. As the ED increased, the surface roughness decreased from $\approx 13.7 \text{ nm}$ to $\approx 4.5 \text{ nm}$, which in turn shows the decrease in coalescence height. Other studies on CVD grown MoS₂ on SiO₂ have also found similar out-of-plane features [260, 261]. Figure 6.6 (b) shows the AFM results of the 3 laser conditions that were chosen for FET fabrication.

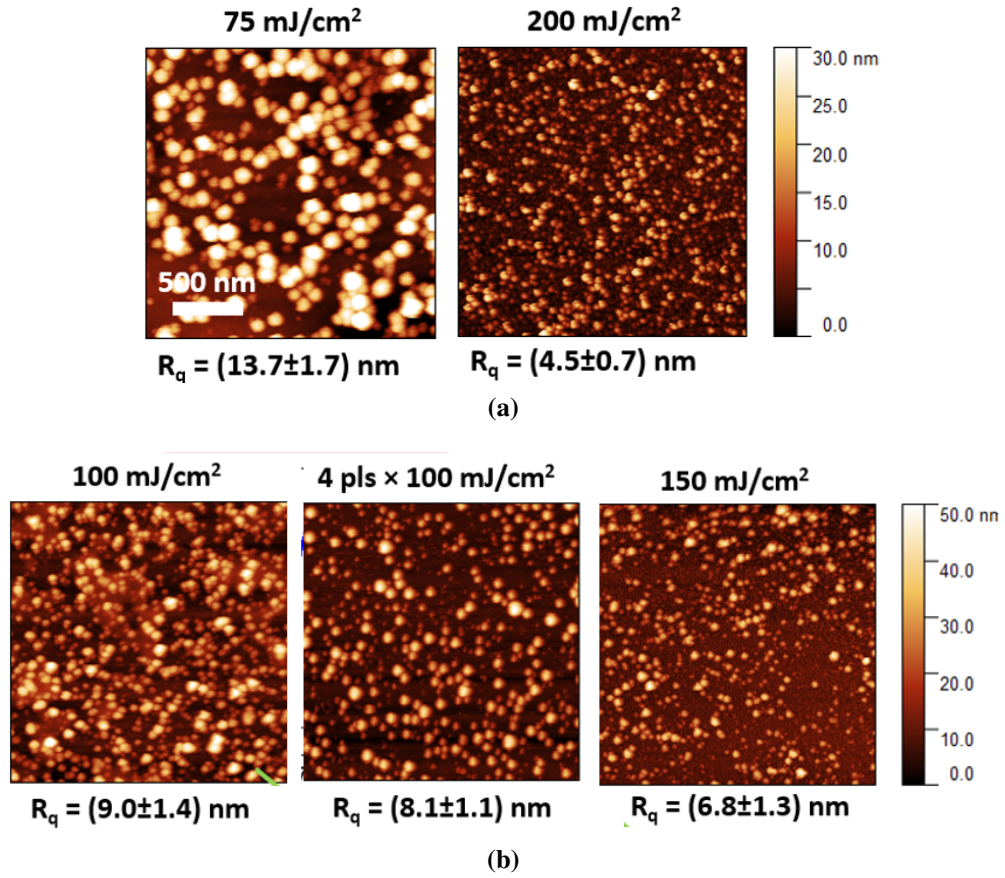


Figure 6.6: (a) AFM of 2 different processes - 75 and 200 mJ cm⁻² with 1 pulse of laser annealing. Surface roughness is provided below each image. The white circles seen in the 75 mJ cm⁻² process are the dome like defects found in TEM. (b) AFM and subsequent surface roughness of the 3 conditions (100 and 150 mJ cm⁻² with 1 pulse and 100 mJ cm⁻² with 4 pulses) used as the base for the fabrication of FET devices.

6.3.5 XRD Analysis

X-ray diffraction was performed on MoS₂/SiO₂/Si samples exposed to 100 mJ/cm² (with 1, 2, 4 and 8 laser annealing pulses) on a Philips PANalytical X'Pert PRO diffractometer. Figure 6.7 (a) depicts a schematic of planar (002) and perpendicular (020) growth patterns that can occur during the growth process. Figure 6.7 (b) displays the data collected on each sample. It shows that for this 2H-MoS₂, the only XRD peak found is the perpendicular (002) phase where the diffraction angle (2θ) = 14.125°. Similar to the Raman results, as the amount of laser pulses increases, so does the XRD peak height. It shows that the poly-crystalline MoS₂ does improve with higher pulse numbers but, referring back to RBS, the overall quality of the film does not. In fact,

it worsens, with some of the MoS₂ coalescing into dome-like structures. A FWHM calculation was also evaluated on the (002) XRD peaks and gave about 2.3°. The following Scherrer equation was then used to uncover the ordered crystalline domain size

$$\tau = \frac{K\lambda}{\beta \cos \theta} \quad (6.1)$$

where τ is the mean domain size, K is the shape factor, λ is the X-ray wavelength (1.54 Å), β is the FWHM (2.3°) and θ is the Bragg angle. This gave a domain size of ≈ 3.5 nm. This is an important finding when understanding the electrical behaviour of these samples. Note, a broad peak can be seen for every sample at $2\theta = 23^\circ$ and it is associated with the 90 nm thick SiO₂ film on the Si substrate.

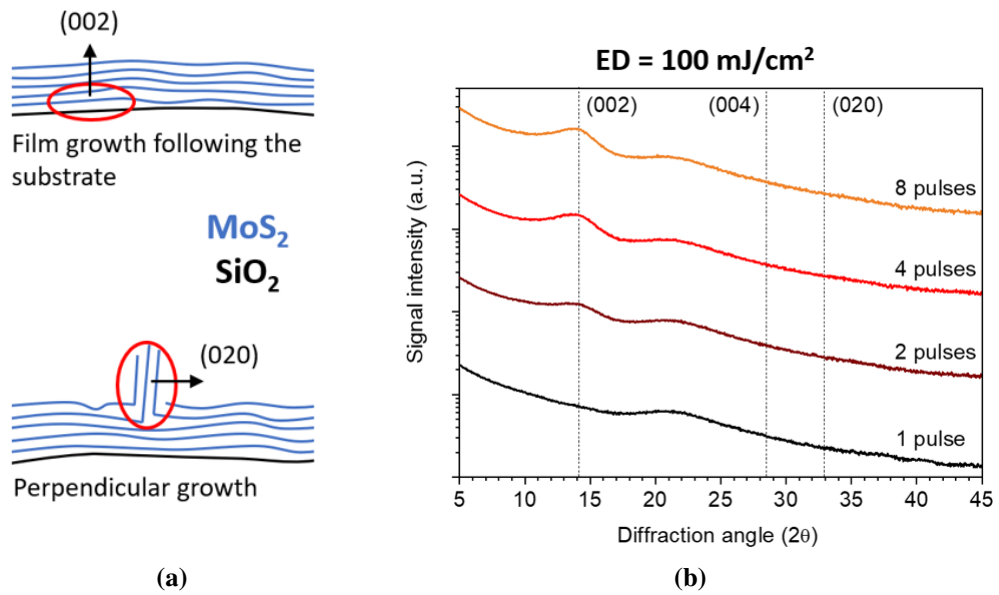


Figure 6.7: (a) Schematic diagram of XRD peak of both planar and perpendicular growth features of MoS₂ on SiO₂. (b) XRD peaks for MoS₂ with 1, 2, 4 and 8 laser pulses at an energy density of 100 mJ cm⁻². Only planar (002) MoS₂ phase was present. A second broad and weak XRD peak was observed at 23° and is associated with the 90 nm SiO₂ substrate.

6.4 FET Fabrication

After various physical tests were performed to understand the many different laser anneal methods, 3 processes were chosen and used for further patterned FET examinations. These processes were (1) 1 laser pulse with an energy value of 100 mJ cm^{-2} , (2) 4 pulses of 100 mJ cm^{-2} and finally (3) 1 pulse of 150 mJ cm^{-2} . For every process there were 2 separate samples (hence 6 in total) and each looked like that showed in Figure 6.8 (a). It must be noted that the aim of these electrical tests were not done to find high performance FET devices but rather be a part of the wider evaluation of the material. Along with AFM, XTEM, EDX, RBS and Raman, the FET testing was used to gain insight into this laser annealing process and understand the 'why' behind each sample's behaviour. The results of this study will be applied to future fabrication projects of such materials, providing an in depth understanding of the materials and help improving future fabrication processes. Figure 6.8 (a) shows a cross-sectional schematic diagram of a device and (b) displays a top-view schematic diagram.

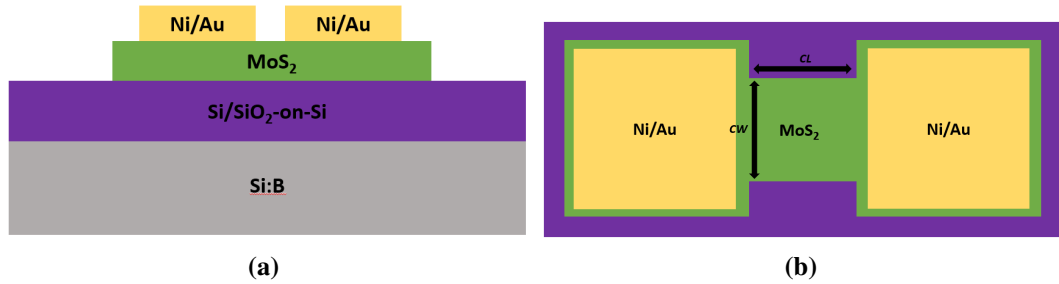


Figure 6.8: (a) Cross-sectional schematic diagram of a FET device (b) Top-view schematic diagram of a FET device.

6.5 Results Post Device Fabrication

6.5.1 TEM & EDX - laser annealing of 1 pulse at 100 mJ cm^{-2}

Cross sectional TEM revealed important information about all 3 processes. Figure 6.9 shows the top-view schematic diagram of a device, with red boxes outlining the areas

used when making TEM lamellae.

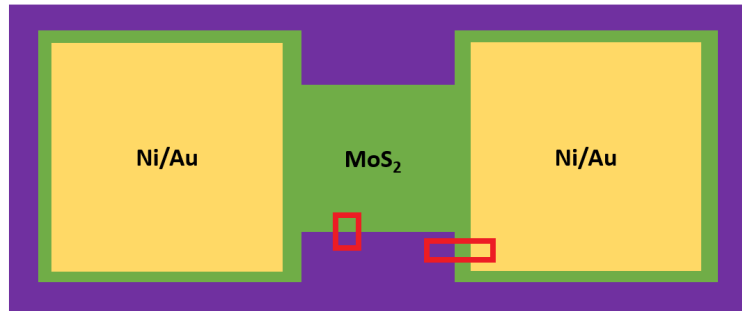


Figure 6.9: Area on devices used to make TEM lamellae. Some only included the MoS₂ and substrate while others included the metal contact, MoS₂ and substrate.

For 1 pulse at 100 mJ cm^{-2} , the thin-films of $\approx 6\text{-}8$ layers were found to be mostly homogeneous (left) with some broken sections in the film as seen in Figure 6.10 (a). Figure 6.10 (b) shows deformities within the thin film and the darker region in the SiO₂ layer could be some S that has melted into the substrate. Figure 6.10 (c) zooms in on the thin film and conveys a polycrystalline structure. Figure 6.10 (d) shows that at the contact edge, the MoS₂ is gently curved. This effect can be related to lithography and the presence of a metal contact, and has been seen in other studies [111, 262]. This could potentially cause localised parasitic resistance and interfere with device performance. EDX was also executed as seen in Figure 6.11 and Mo and S looking homogeneous overall. It also showed the presence of the gold contact as seen in blue.

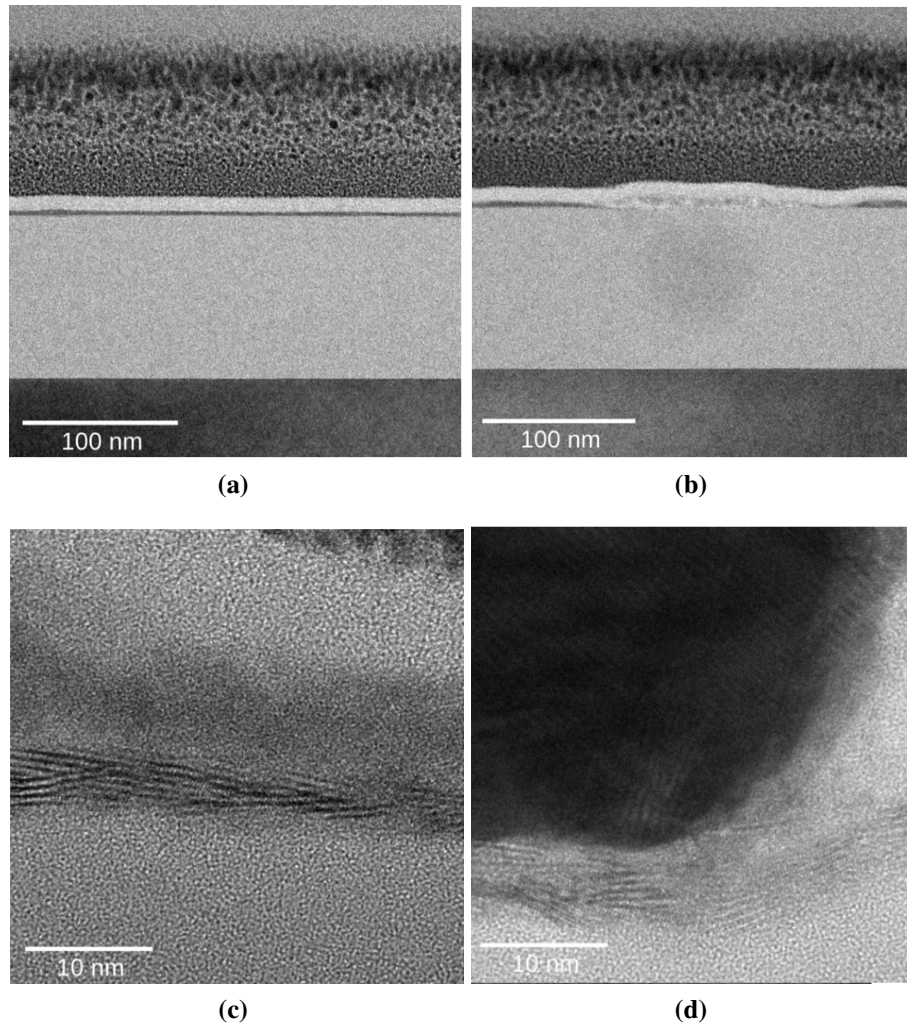


Figure 6.10: TEM images of 1 pulse at 100 mJ cm^{-2} . (a) Homogeneous layers of MoS₂ on SiO₂-on-Si. (b) Broken layers of MoS₂ on SiO₂-on-Si, with possible diffusion of S and/or Mo into the underlying SiO₂ (c) Zoomed in image of MoS₂ layers. (d) Image taken at the edge of the metal contact.

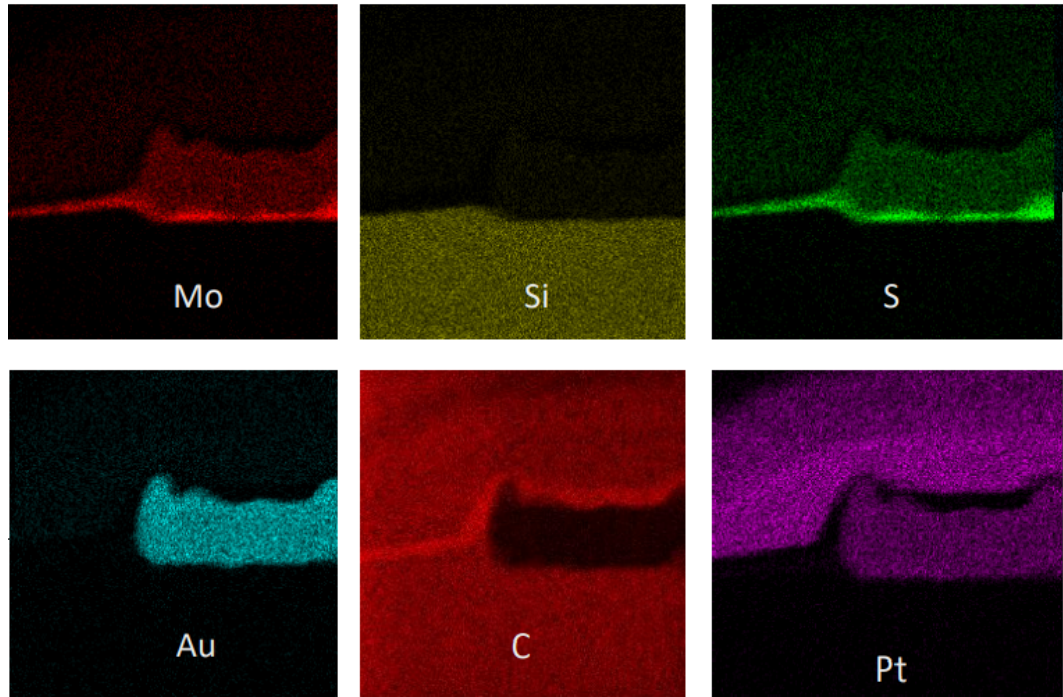


Figure 6.11: EDX images of Mo, Si, S, Au, C and Pt of 1 pulse at 100 mJ cm^{-2} taken at the edge of the metal contact.

6.5.2 TEM & EDX - laser annealing of 4 pulses at 100 mJ cm^{-2}

Next, the process with 4 pulses of 100 mJ cm^{-2} was explored. Cross-section bright-field TEM images revealed approximately 6-7 layers (15-20 nm). Though there were areas of layered MoS_2 , clusters of $\approx 100 \text{ nm}$ width and $\approx 25 \text{ nm}$ height also had formed on the surface, shown in Figure 6.12 (a) and (b). Figure 6.12 (c) shows a zoomed in high definition TEM images of the material. EDX images in Figure 6.13 also shows these defects.

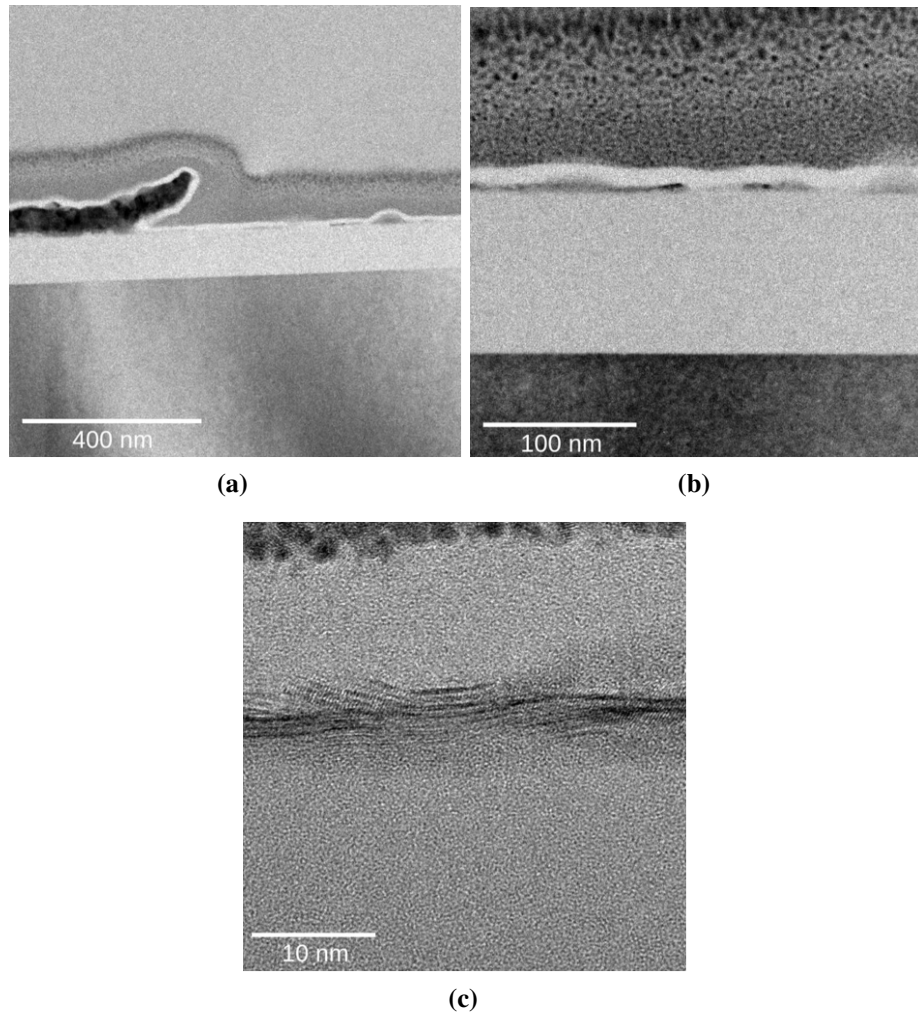


Figure 6.12: TEM images of 4 pulses at 100 mJ cm^{-2} . (a) MoS₂ on SiO₂-on-Si at the edge of a metal contact. (b) Broken layers of MoS₂ on SiO₂-on-Si. (c) Zoomed in image of MoS₂ layers

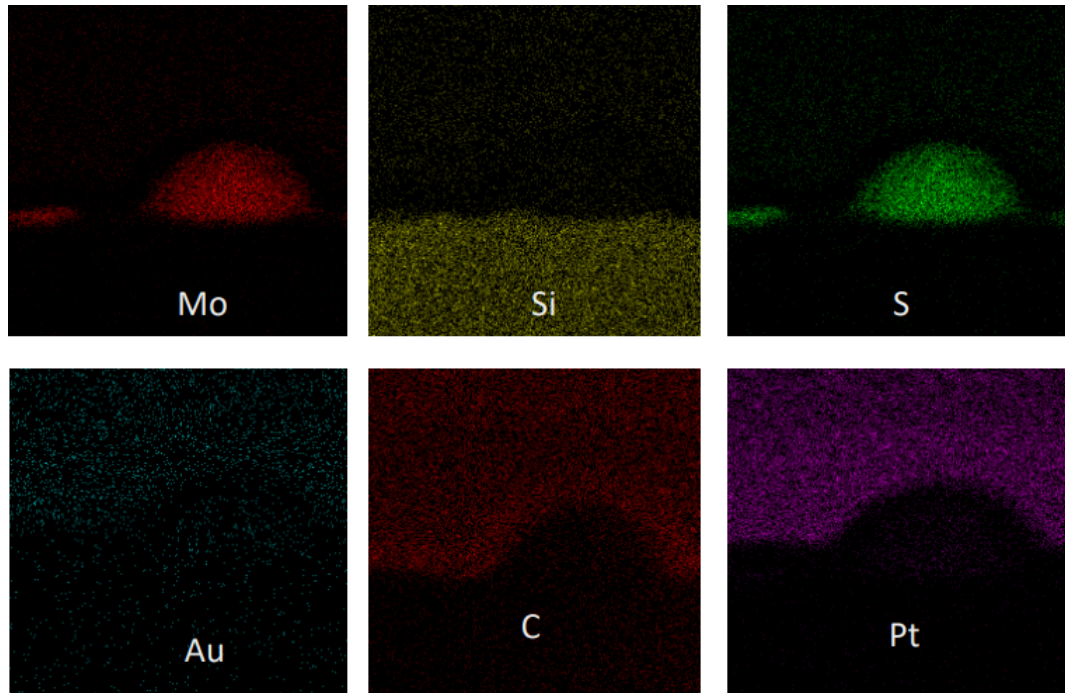


Figure 6.13: EDX images of Mo, Si, S, Au, C and Pt of 4 pulses at 100 mJ cm^{-2} taken at the edge of the metal contact.

6.5.3 TEM & EDX - laser annealing of 1 pulse at 150 mJ cm^{-2}

Finally, the last process is shown - 1 pulse at 150 mJ cm^{-2} . Both TEM and EDX reveal poor quality MoS_2 . Figure 6.14 (a) shows large protrusions on the surface, more than that of the previous process. EDX in Figure 6.15 reveals that the sample did not seem to not survive metal lift-off, also shown in Figure 6.14 (b). This was proved further when no working devices were found on this sample.

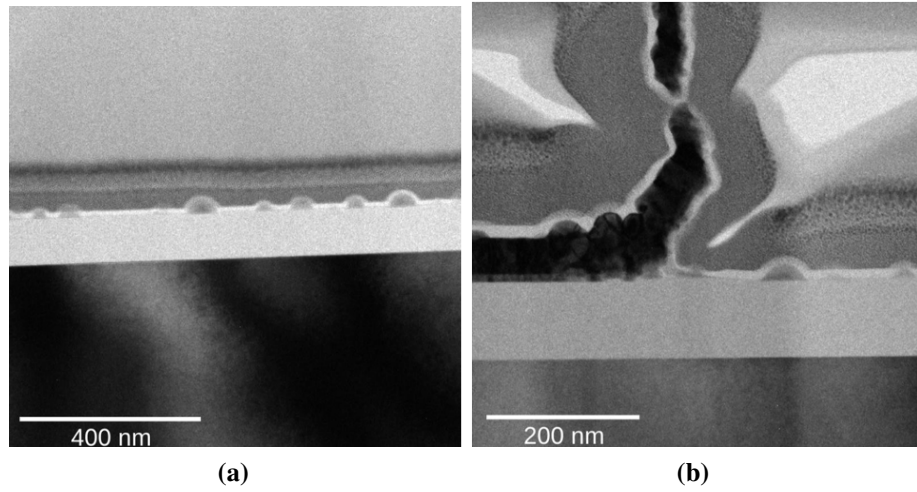


Figure 6.14: TEM images of 1 pulse at 150 mJ cm^{-2} . (a) Dome-like MoS_2 features on SiO_2 -on-Si (b) Morphed metal contact, along with dome MoS_2 feature on substrate.

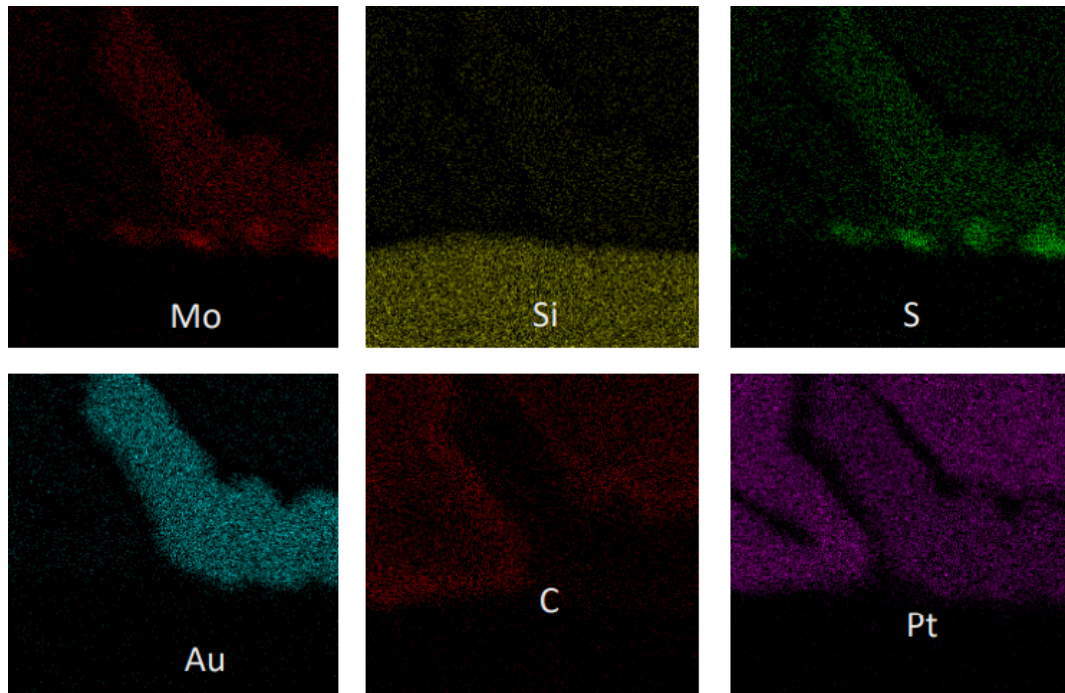
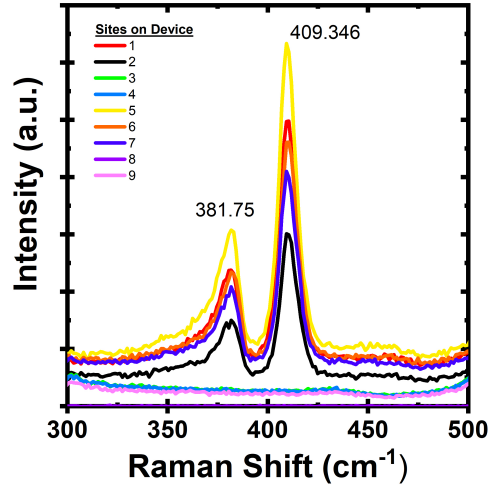


Figure 6.15: EDX images of Mo, Si, S, Au, C and Pt of 1 pulse at 150 mJ cm^{-2} taken at the edge of the metal contact.

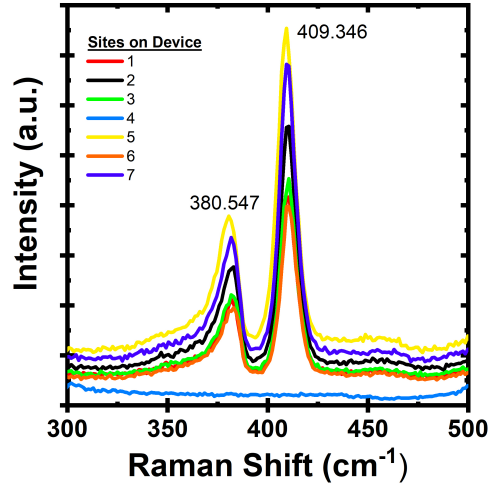
6.6 Electrical Characterisation Post FET Fabrication

6.6.1 Locating Working Devices

Following on from TEM and EDX, a representative electrical study of the laser annealed samples was carried out. The batch of samples were split up into 3 groups. Sample 10 and 11 were 1 pulse at 100 mJ cm^{-2} . Sample 12 and 13 were 4 pulses at 100 mJ cm^{-2} . Finally sample 14 and 15 were 1 pulse at 150 mJ cm^{-2} . Working devices were only found on samples 10, 11 and 12. Prior to the investigation into the electrical behaviour of these devices, Raman spectroscopy was performed as seen in Figure 6.16. These Raman measurements were performed on a separate system to previous Raman tests – Renishaw RAMAN inVia (Modu-514 nm laser with a spot size of $\approx 1.5 \mu\text{m}$ at 50x magnification). On each sample, a number of tests were done at different sites around 1 device - the MoS_2 throughout the gate and the MoS_2 around the metal contacts. MoS_2 peaks at 381 cm^{-1} (E_{2g}) and 409 cm^{-1} (A_{1g}) were present in samples 10 - 13. The delta shift between the modes are consistent with that of other multi layer MoS_2 [263]. In both samples the intensity of the modes vary throughout the device and at some sites, no peaks are found. It concludes that the MoS_2 is not homogeneous throughout the laser annealed areas. This aligns with the presence of coalescence defects seen in TEM and EDX. Samples from 150 mJ cm^{-2} had very weak/no MoS_2 . No electrical activity was found on these samples.



(a)



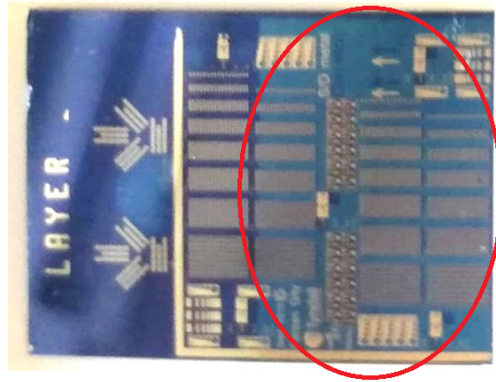
(b)

Figure 6.16: (a) Raman Shift of MoS₂ deposited on SiO₂/Si with a laser anneal of 1 pulse at 100 mJ cm⁻² post FET fabrication. (b) Raman Shift of MoS₂ deposited on SiO₂/Si with a laser anneal of 4 pulses at 100 mJ cm⁻² post FET fabrication.

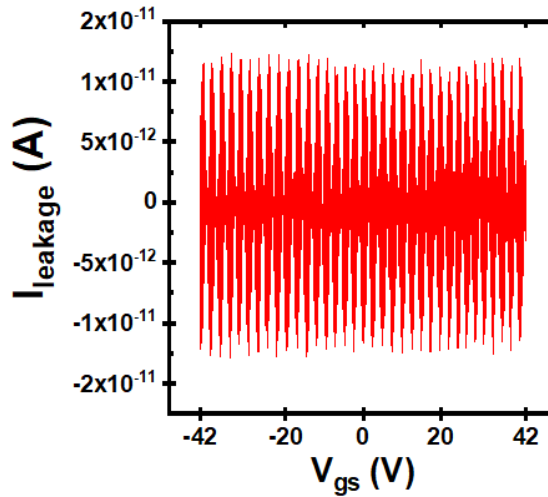
6.6.2 Transfer Characteristics

It was first necessary to locate possible working devices on each sample. A systematic analysis was done throughout the areas where the samples had been laser annealed and is circled in red in Figure 6.17 (a). As mentioned previously, the 1 pulse at 150 mJ cm⁻² was also investigated, but aligning with the physical characterisation tests, no working devices were found. The rest of this chapter focuses on the electrical tests

of 1 pulse and 4 pulse 100 mJ cm^{-2} laser annealed samples. Channel length (L) and width (W) are specified within each individual figures. The back-gate voltage range was from -42 V to +42 V. Also, no significant gate leakage current was measured suggesting that laser processing did not affect SiO_2 layer for functioning devices. This is shown in Figure 6.17 (b).



(a)



(b)

Figure 6.17: (a) Area of laser annealing circled in red. This was the same area for all samples. (b) Gate leakage check on FET device.

Figures 5.18 (1 pulse) and 5.19 (4 pulses) show FET transfer characteristics demonstrated by V_{gs} of range -42 V to +42 V. V_{ds} was altered between 5 V, 10 V and 15 V. A small modulation of the drain current with the back gate voltage was recorded,

where current flows in both negative and positive gate voltage direction. There seemingly is p-type saturation at a high negative gate bias. These plots display FET transfer characteristics of devices with the same layout dimensions within each plot for 1 pulse and 4 pulses. This, along with the Raman spectra, conveys some device-to-device variation, most likely due to local variations of MoS₂ thickness across a large channel surface area.

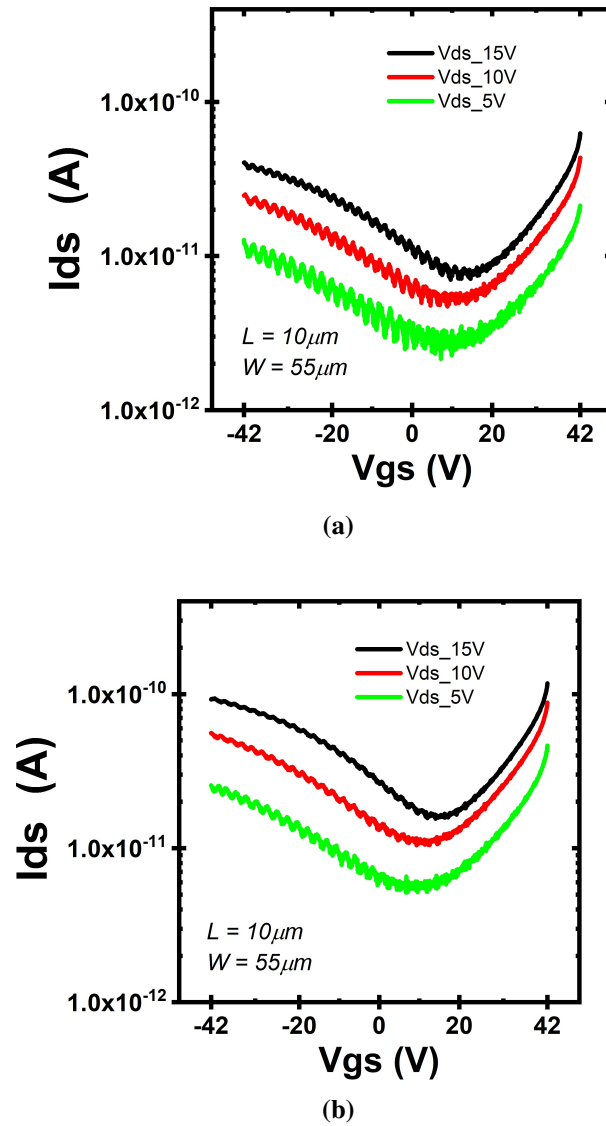


Figure 6.18: 10nm MoS₂ deposited on SiO₂/Si with a laser anneal of 1 pulse at 100 mJ/cm² (a) I_{ds} vs V_{gs} of device series with channel length 10 μm , channel width 55 μm with changing V_{ds} . (b) I_{ds} vs V_{gs} of device series with channel length 10 μm , channel width 55 μm with changing V_{ds} .

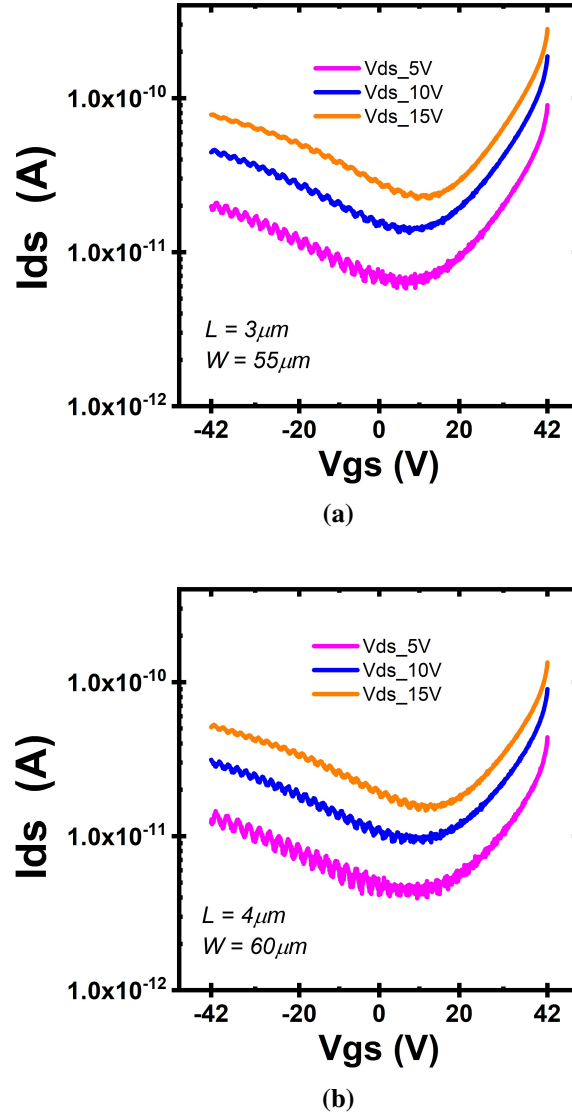
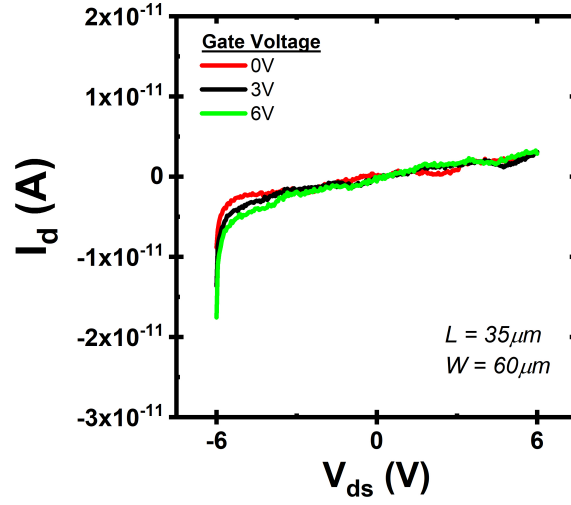


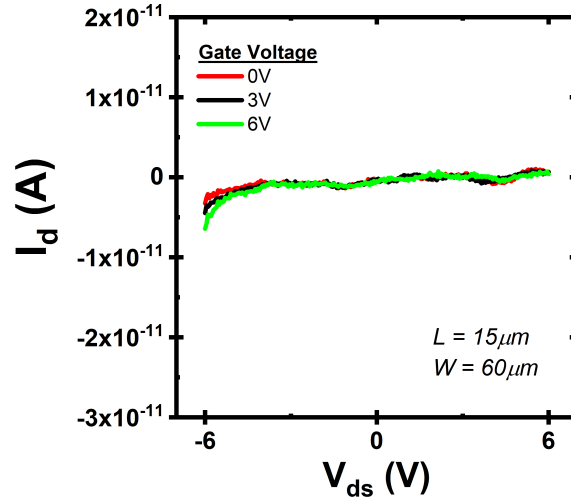
Figure 6.19: 10nm MoS₂ deposited on SiO₂/Si with a laser anneal of 4 pulses at 100 mJ/cm² (a) I_{ds} vs V_{gs} of device series with channel length 3 μm , channel width 55 μm with changing V_{ds} . (b) I_{ds} vs V_{gs} of device series with channel length 4 μm , channel width 60 μm with changing V_{ds} .

6.6.3 Output Characteristics - Investigating the influence of channel resistance and contact resistance.

Figures 5.20 (1 pulse) and 5.21 (4 pulses) plot representative output characteristics for the 4 pulses laser anneal case. The output characteristics were then plotted in accordance with device theory to see whether contact or channel resistance dominates the current characteristics [264].

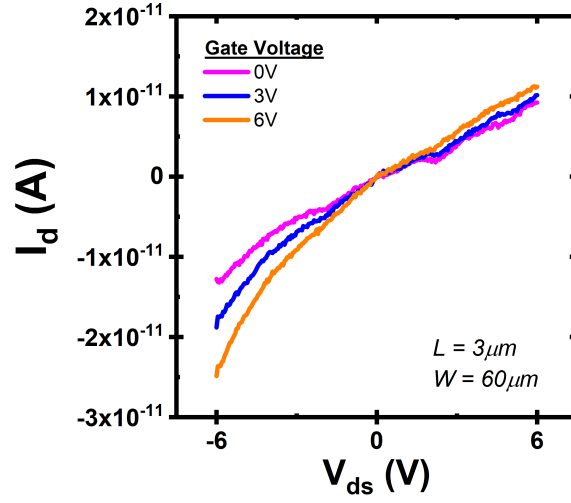


(a)

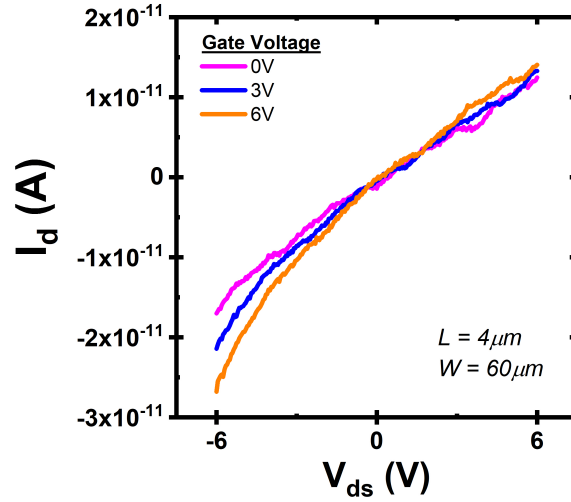


(b)

Figure 6.20: 10nm MoS₂ deposited on SiO₂/Si with a laser anneal of 1 pulse at 100 mJ/cm² (a) I_{ds} vs V_{gs} of device series with channel length 35 μm , channel width 60 μm . (b) I_{ds} vs V_{gs} of device series with channel length 15 μm , channel width 60 μm .



(a)



(b)

Figure 6.21: 10nm MoS₂ deposited on SiO₂/Si with a laser anneal of 4 pulses at 100 mJ/cm² (a) I_{ds} vs V_{gs} of device series with channel length 3 μm , channel width 60 μm . (b) I_{ds} vs V_{gs} of device series with channel length 4 μm , channel width 60 μm .

Two different equations were manipulated to try and further this understanding. First, Richardson-Schottky emission was investigated, followed by Fowler-Nordheim tunnelling. In the case of a small Schottky barrier is present hence thermionic emission dominating the transport, $\ln(I_{ds}/V_{ds}^2)$ versus $\ln(1/V_{ds})$ is expected to give a linear trend with a negative slope. For Fowler-Nordheim tunnelling, if the barrier is high and wide enough, linear behaviour is expected with $\ln(I_{ds})$ versus $\sqrt{V_{ds}}(V^{0.5})$. However, both produced inconclusive results and a definitive dominant resistance could not be found.

This is an area of investigation that will be addressed in future work.

6.7 Conclusion

In conclusion, uniform 2H-MoS₂ was successfully grown by sputtering deposition of stoichiometric MoS₂ followed by nanosecond UV laser annealing. The 90 nm SiO₂ on Si film increases the temperature in the MoS₂ and results in regions of 2H MoS₂ at a laser energy density of 100 mJ cm⁻², with a single pulse of 22 ns duration. Raman, AFM, RBS, TEM, EDX and LIMP software were used to build a systematic investigation into the detailed characteristics of these laser annealed samples under various conditions. The film was found to be discontinuous after the laser pulse - with S:Mo ratio values dropping to the range 1.2 to 1. This is speculated to be a result of sublimation. Finally 2 laser annealing conditions survived FET fabrication and gave some working devices, though at very low currents. This work sets a stepping stone to growing 2D materials on SiO₂/Si using a cost-effective methodology at lower temperatures and could enable further refinement in order to fabricate devices targeting optoelectronic and nanoelectronics.

Chapter 7

Conclusion and Future Outlooks

2D TMD materials have shown significant potential for their role in next generation semiconductors. Both MoS₂ and WS₂ have provided promising results in this area. However, there is certainly more work to be done to improve the performance of these materials.

High quality natural MoS₂ and WS₂ crystals exfoliated onto substrates work on a small scale, but replicating this process on a bigger industrial scale still proves to be an obstacle. Another challenge is understanding the behaviour at the metal/TMD and oxide/TMD interfaces, since there is quite a lot of variability between samples when dealing with exfoliated flakes. Though our results varied throughout some samples, we did demonstrate that interface state density values below the detection limit can be achieved between crystalline MoS₂ on amorphous Al₂O₃ or SiO₂ and WS₂ on Al₂O₃, supporting one of the main motivations for using 2D semiconductors in MOSFETs and Tunnel FETs. For future work, we believe one of the major ways to better understand these behaviours lies with TCAD simulations. With the aid of such simulations, complex calculations and predictions could be made about these interfaces as well investigating our interesting results suggesting not only the presence of interface trap states but also the possibility of charges trapping and de-trapping effect into the bulk of the 2D semiconductor.

Another hurdle is creating the optimal growth process of TMD materials. Creating high quality structures within the BEOL thermal budget still stands as one of the biggest challenges in this field. Our research produced uniform MoS₂ grown by chemical vapour deposition within the 550 C budget, with rapid and repeatable growth on glass, sapphire, a-Al₂O₃/sapphire, and SiO₂/Si. This process was also accomplished in an industry compatible 300 mm ALD reactor. Extensive Raman, Hall and electrical analysis were performed and gave valuable insight into the emergence of

TMDs for 3D heterogeneous integration. However, our materials did prove to be quite resistive with lower values of mobility and carrier concentrations than obtained in high temperature grown crystals. This was most likely caused by the small grain size which results in a high density of defect states located within the MoS₂ energy gap. The studies indicated that while a reasonable carrier mobility can be achieved through low temperature growth (1 to 17 $cm^2 V^{-1}s^{-1}$), the ability to modulate the drain to source current in a MOSFET structure is limited due defect states in the MoS₂ energy gap. It is clear more variety and testing in growth parameters must be investigated to improve the quality of CVD grown MoS₂ and implement them on an industrial scale.

For our ALD grown WS₂, new findings in the nanoelectronic operation of TMD thin-film devices were found and can help close the gaps in the knowledge. Hall effect and temperature dependent electronic findings are rare in literature. We find that these plasma ALD deposited 8 nm WS₂ thin-films exhibit a p-type behavior with the unintentional active doping concentration of $1.31 \times 10^{17} cm^{-3}$. Analysis of the temperature dependence of the WS₂ resistivity and the specific contact resistivity between the WS₂ and the Ni/Au contacts, indicates similar activation energy values of 91 meV and 100 meV. This data predicts that both activation energy values are being controlled by the temperature dependence of the hole concentration. Looking forward, repeating such experiments and understanding trends will help with processes and performances of 2D materials. It would also be worth using CTLM structures with different dimensions. More specifically, dimensions where the difference between the inner metal contact circle and outer WS₂ circle are much larger. This would bring the data closer to the ideal ratios when applying the correction factor for resistivity.

Our final study successfully grew uniform 2H-MoS₂ by sputtering deposition of stoichiometric MoS₂ followed by nanosecond UV laser annealing. The 90 nm SiO₂-

on-Si substrate obtained crystalline MoS₂ at an laser energy density of 100 mJ cm⁻². Raman, AFM, RBS, TEM, EDX and LIMP software were used to build a systematic investigation into the detailed characteristics of these laser annealed samples under various conditions. We observed the formation of dome-like structures and theorize that this stems from the sublimation of MoS₂ during the laser annealing step. One of the suggested future actions would be to cap the samples with a thin Al₂O₃ layer during the laser annealing.. This would protect the MoS₂ from overexposure and possibly stop the sublimation of MoS₂ and in turn, the formation of the unwanted dome-like structures. With these findings, more work can be done that could possibly lead the way to cost effective BEOL processes in optoelectronic and nanoelectronics.

There is a lot more to understand about these 2D materials regarding next generation semiconductors. Many questions are yet to be answered. Yet, with every study, we are a step closer to finding new age technology that could change the face of electronics.

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