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Junctionless multigate field-effect transistor

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This paper describes a metal-oxide-semiconductor (MOS) transistor concept in which there are no junctions. The channel doping is equal in concentration and type to the source and drain extension doping. The proposed device is a thin and narrow multigate field-effect transistor, which can be fully depleted and turned off by the gate. Since this device has no junctions, it has simpler fabrication process, less variability, and better electrical properties than classical MOS devices with source and drain *PN* junctions. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3079411]

Research in multigate silicon-on-insulator metal-oxide-semiconductor field-effect transistors (MOSFETs) for deep submicron complementary MOS applications is currently being carried out by many semiconductor companies, as these devices hold the promise for pushing the limits of silicon integration beyond the limits of classical planar technologies.[1] In a multigate field-effect transistor (MuGFET) the gate electrode is wrapped around a silicon wire, called "finger" or "fin," forming a gate structure that delivers optimal control of the channel potential. The excellent gate-to-channel coupling combined with the use of a small wire section allows one to fully deplete the channel region even if it is heavily doped and, therefore, to turn the device off.

In very short-channel devices ($L=10$ nm or less) the formation of ultrasharp source and drain junctions imposes orders of magnitude of variation in doping concentration over a distance of a few nanometers. Such concentration gradients impose drastic conditions on doping techniques and thermal budget. The devices proposed here are fabricated without the need for forming junctions. Since the channel doping concentration and type are the same as in the source and drain extensions, there is no doping concentration gradient and therefore no impurity diffusion during thermal processing steps. This relaxes the thermal budget by a great deal.

Thin-film accumulation-mode double-gate devices have been shown to have better short-channel properties [drain-induced barrier lowering (DIBL) and subthreshold slope degradation] than conventional inversion-mode (IM) devices.[1] It has been shown that the use of accumulation-mode devices (a family of device to which the proposed device belongs) improves contact resistance and reduces the sensitivity to gate overlap/underlap issues.[2] It has also been shown that accumulation-mode devices are less sensitive to doping fluctuation effects than classical IM devices.[3] Accumulation-mode MuGFETs have been shown to be less sensitive to negative bias thermal instability than IM devices and to have less variation in drain current with doping concentration.[4]

A junctionless transistor is basically an accumulation-mode device in which the channel doping concentration is equal to that on the source and drain. Simulations show that these junctionless devices have better short-channel electrical characteristics than conventional IM devices. The electrical characteristics of both conventional (N^+-P-N^+) and junctionless (N^+-N^+-N^+) devices were simulated using the Atlas 3-D device simulator.[5] Abrupt source and drain junctions are used for the conventional transistors. Table I shows the parameters used in device simulation, and Fig. 1 shows the general structure of a trigate MuGFET. The cross section of the device is 5×5 nm^2. The feasibility of accumulation-mode devices with such a small cross section was demonstrated in the past.[6] Because of the N-type doping of the channel, a N-channel junctionless device requires a gate material with a high work function such as P^+ polycrystalline silicon or platinum in order to achieve a suitable V_{th} value. It is, however, clear that the use of a metal as gate material is preferable for gate resistance reduction purposes. It is also to be noted that the junctionless device lends itself to the use of a gate-last process, which facilitates the use of a metal gate. A midgap gate material is used for the classical IM device. If the cross section of the channel is small enough, the gate can deplete the heavily doped channel entirely, which turns the transistor off. The subthreshold characteristics of junctionless MuGFETs with different gate lengths (5–20 nm) at low drain voltage are shown in Fig. 2. The subthreshold slope of shortest junctionless device ($L=5$ nm) is below 80 mV/decade. This shows the potential of junctionless transistor for extremely short-channel applications. It is important to note that the off current is determined solely by the electrostatic control of the gate and not by the leakage current of a reverse-biased diode. This renders the device less sensitive to contamination, which reduces carrier lifetime and to temperature, as shown in Ref. 1, for accumulation-mode double-gate transistors; it also enables one to minimize leakage current if a low-bandgap semiconductor such as germanium is used. It is important for the cross section of the junctionless device to be sufficiently small in order to be able to fully

TABLE I. MuGFET device parameters.

	Conventional	Junctionless
Channel doping	2×10^{15} cm^{-3} (P-type)	8×10^{19} cm^{-3} (N-type)
Gate oxide thickness	2 nm	2 nm
Gate work function	4.6 eV	5.5 eV
T_{si}	5 nm	5 nm
W_{fin}	5 nm	5 nm
L_{gate}	5–30 nm	10–30 nm

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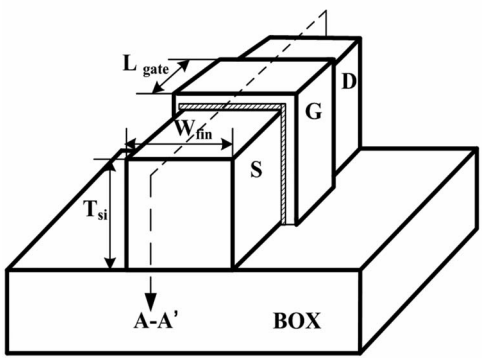


FIG. 1. MuGFET device schematic view.

deplete the channel of carriers and turn the device off. The higher the channel doping concentration, the smaller the cross section needs to be. One may suggest further analysis of the device to parameter variations such as fin width and height and doping concentration.[7]

For the IM devices we used a lightly doped channel in order to avoid premature inversion at the corners.[3] The simulated IM devices have a source/drain and source/gate overlap of 1 nm, which means that effective channel length of the device is 8 nm when the physical gate length is 10 nm. The simulated results for DIBL and threshold voltage versus physical gate length for both junctionless MuGFETs and IM MuGFETs are plotted in Fig. 3. The DIBL is defined as the difference in threshold voltage when the drain voltage is increased from 0.05 to 1.0 V [DIBL=$V_{th}(V_{DS}=0.05\ V)-V_{th}(V_{DS}=1\ V)$]. The junctionless MuGFETs has better short-channel characteristics than the IM device. In the accumulation-mode device, the effective gate length, defined

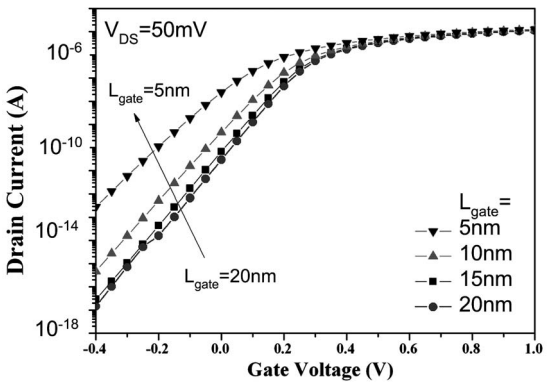


FIG. 2. Subthreshold characteristics of junctionless devices with $T_{si}=W_{si}=5$ nm at $V_{DS}=50$ mV for different gate length values.

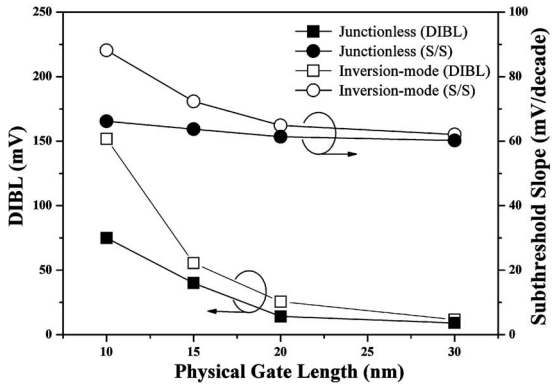


FIG. 3. DIBL and subthreshold slope at $V_{DS}=50$ mV in junctionless and IM devices with $T_{si}=W_{si}=5$ nm.

as the distance between the source and drain junctions, is 2 nm shorter than the printed gate length ($L_{eff}=L_{gate}-2$ nm). In the junctionless device, we arbitrarily define the effective length as being equal to the printed gate length ($L_{eff}=L_{gate}$). It is worth noting that the longer effective gate length of the junctionless device is not the reason for its better short-channel characteristics since, for instance, a junctionless transistor with $L_{gate}=L_{eff}=10$ nm has a lower subthreshold slope than an IM device with $L_{gate}=15$ nm and thus $L_{eff}=13$ nm.

In conclusion, we propose a type of MOSFET in which there are no *PN* junctions and where the doping concentration in the channel is sensibly equal to that in the source and drain. The device exhibits excellent turn-off and short-channel characteristics based on our simulations.

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