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# Miniaturization of Wireless Sensor Network Nodes

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***Abstract*— Wireless sensor network (WSN) node, typically equipped with a radio transceiver, a small microcontroller and a battery, is different from traditional embedded systems because of its requirement of random deployment, small size and low power consumption. Based on these reasons, miniaturization of the WSN nodes becomes increasingly crucial in embedded system design for numerous applications, such as bio-medical monitoring and body network. In this paper, several technologies of different packaging levels to achieve miniaturization and integration are presented, including flip chip packaging of transceiver and micro-controller bare dies, embedded capacitance and epoxy based three dimensional integration technologies. Comparison of the proposed technologies with the original traditional PCB WSN mote is provided. The current experiments and measurements are also presented to show the benefits brought by these technologies not only in shrinking of the mote size, but also some improvements in electrical performance such as reduction of parasitic passives. It is possible to utilizing several different miniaturization technologies for future miniaturized WSN nodes design. Comparison of these technologies in WSN application is provided as conclusion of this paper .**

## I. Introduction

Because of the wide use of wireless sensor network in medical, environmental and monitoring applications in recent years, there is a strong need to integrate more functionality and miniaturize the wireless sensor network node. This paper presents three different levels of miniaturization technologies developed in Tyndall National Institute.

The content of this paper is organized as:

1. Interconnect and chip:

The smallest type of the chip, bare die, is utilized with the well developed flip chip interconnect. The idea of this method for miniaturization is replacing interconnect and chip of WSN node with smaller technology.

2. Substrate material:

Substrate provides the support structure, ground and power planes for the mote. Moreover, a novel functionality of substrate is developed. The concept of the embedded capacitance makes full use of the ground and power planes to form a built-in decoupling capacitance layer. By doing so, lots of discrete decoupling capacitors can be removed and thus miniaturization purpose is achieved.

3. 3D packaging:

A low parasitic 3D packaging technology that is capable of embedding electronic die of various thicknesses in extremely thick (up to 0.5mm) build-up layers is presented. This approach uses the quick processing and low shrinkage properties of the Cyracure epoxy and permits the patterning of very thick layers. By embedding the micro-controller and the RF die to build up the mote layers, miniaturization and 3D integration of the wireless sensor node is achievable.

## II. Interconnect and Chip: Bare Die Flip Chip Packaging

### A. The benefits

Based on the design of the Tyndall 25mm wireless sensor node [1], a credit card shape flat mote with flip chip bare die, shown in Figure 1 is developed with the same circuit connection. This mote utilizes the ADF7020 ISM band transceiver from Analog devices and MSP430 micro-controller from Texas Instruments. Both chips are of high performance and low power consumption, which are essential for wireless sensor applications. The availability of bare die of both chips from the manufactures is also a reason to use these two chips.

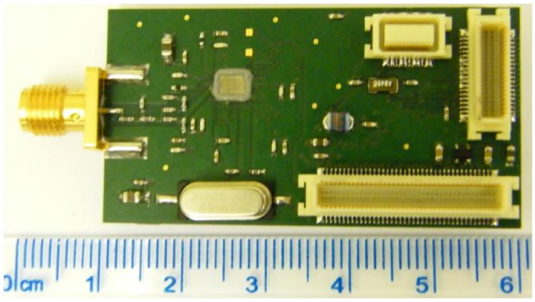



Fig. 1. The credit card shape mote with flip chip of bare die.

The ADF7020 bare die is the un-packaged chip directly from Analog Devices. The usage of the die is a great improvement not only in the area of the chip (smaller size), which is shown in Figure 2, but also in the RF performance. It is well known that the parasitic (especially the inductance) is very critical to the high frequency circuit. The flip chip of bare die eliminates the wire bonding of the traditional packaging, equivalent to tens of nH parasitic inductance.

The basic RF system is formed with only ADF7020 setup components and 14pin connectors to the ADI evaluation board or some other programming board. The ADF7020 is controlled by MSP430 micro-controller. These two chips occupy 40% of the whole PCB space. Table I shows that the use of bare die could lead to a reduction of chip space of 90%, which means around 35% of the PCB space can be saved.

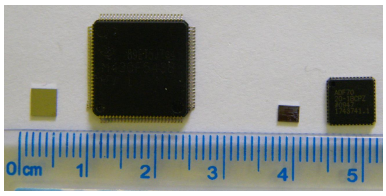



Fig. 2. Size comparison: Bare die vs. QFN package
Left: MSP430F5438 $\mu$C; Right: ADF7020 radio chip

TABLE I
BARE DIE VS. QFN PACKAGE

| Chip | Die dimension | QFN dimension | Rate of area |
|---|---|---|---|
| ADF7020 | 3.09mm×2.4mm | 6.75mm×7.00mm | 15.7% |
| MSP430 | 4.05mm×3.85mm | 14.20mm×14.20mm | 7.7% |

The mote can be used as a separate wireless transmission node, and it is compatible with other Tyndall sensor layers as well. The credit shape makes it easy to bring and the die usage guarantees its high performance.

### B. PCB Layout design for flip chip and die mounting

The layout of the bare die is very challenging because the minimum gap and track is as narrow as 50$\mu$m, compared with around 1mm for traditional PCB design. The minimum size of the through holes is 0.2mm. As shown below in Figure 3, the routing of the die is carefully designed to meet the gap requirement and to minimize the track length.

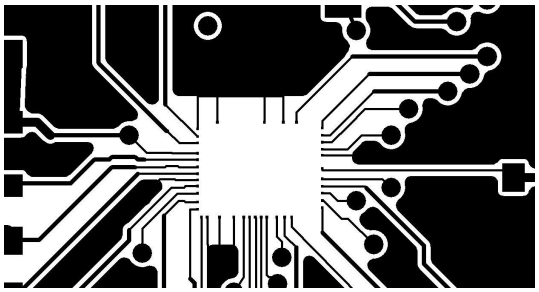


Fig. 3. The layout design for the bare die flip chip, with a minimum gap and track width of 50$\mu$m

There are also some issues to be considered during the die mounting procedure.

Firstly, note that the thickness of the solder mask is not negligible with the height of the pad and thus the solder mask will bring extra stress to the die to be mounted. In the area of the die, solder mask is removed to avoid this situation.

Secondly, two different temperature solders are used: a solder with melt temperature of 280 degree is used to mount the die only, and another tin solder with lower melt temperature (230 degree) is applied to mount the other components. By doing so, the following soldering will not bring damage to the die which is mounted already.

Thirdly, the mounted chip is underfilled using an electrically-insulating adhesive to enhance the interconnect. With the help of the adhesive, the die will stay at the proper interconnect pads even if the second soldering causes remelt of the 280 degree solder.

TABLE II
METALIZATION OF THE WIRE-BONDING INTERCONNECT.

| | Metalization | Area | Hieght |
|---|---|---|---|
| A | 98.5%Al, 1% Si, 0.5% Cu | 75$\mu$m×75$\mu$m | 10$\mu$m |
| B | 98.5%Al, 1% Si, 0.5% Cu | 200$\mu$m×200$\mu$m | 10$\mu$m |

TABLE III
METALIZATION OF THE FLIP CHIP INTERCONNECT.

| | Metalization | Area | Hieght |
|---|---|---|---|
| C | Electroless Ni/ Au | 75$\mu$m×75$\mu$m | 10$\mu$m |
| D | 98.5%Al, 1% Si, 0.5% Cu | 75$\mu$m×75$\mu$m | 10$\mu$m |

### C. Interconnect analysis of wire-bonding and flip-chip

It is necessary to validate the flip-chip interconnect could bring positive change to the whole system as the RF circuit is critical to the interconnect parasitics. The parasitics of the wire-bonding and flip-chip interconnection are modeled and extracted by Ansoft Q3D Extractor simulation.

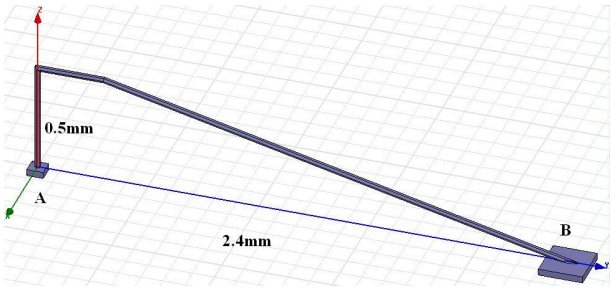



Fig. 4. 3D structure of wire-bonding.

Figure 4 shows the geometry of the wire-bonding interconnection inside the QFN packaging. The structure "A" is the pad of the die, while "B" is the pad of the quad flat nonlead (QFN) package. The metal used for the wire-bonding is gold, with a height of 0.5mm and length of 2.4mm, which is the average length of all the wire-bondings. The metal composition, area and height of the pads A and B are listed in Table II.

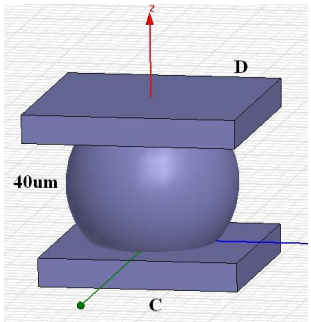



Fig. 5. 3D structure of flip-chip.

The purpose of wire-bonding simulation is to have a comparison with the result of flip-chip. Since the convert method

TABLE IV
PARASITIC PARAMETERS OF THE EQUIVALENT CIRCUIT.

| | R1wire | L1wire | Cwire | L2wire | R2wire |
|---|---|---|---|---|---|
| Wire bonding | 0.057Ω | 1.28nH | 35.8fF | 1.28nH | 0.057Ω |
| Flip chip | 0.001Ω | 8.33pH | 5.9fF | 8.33pH | 0.001Ω |

is to be investigated, the differences between wire-bonding and flip-chip, no matter in interconnect parasitic or in PCB layout, are essential to predict the system performance.

Figure 5 shows the geometry of the flip-chip interconnection[2]. The solder ball, conducting the die and the board, is made of gold, with a height of 40$\mu$m. The structure "D" is the pad of the die, while "C" is the pad of the PCB board for flip chip. The metal composition, area and height of the pads C and D are listed in Table III.

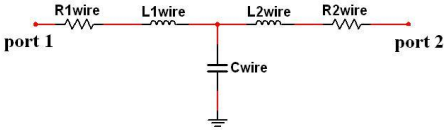



Fig. 6. The equivalent circuit for both interconnect technologies.

The parasitic parameters are extracted by simulation and the equivalent circuits of the wire-bonding and flip-chip are expressed by the same form of circuit shown in Figure 6. However, the values of the components, shown in Table IV, differ between two simulation results.

It is clear that the flip-chip technology has very low parasitic property. The equivalent circuit is presented by a sub-circuit in PSpice or Ansoft Designer.

Based on the previous discussion, we could get the conclusion that the flip chip technology has great advantage against wire bonding, not only in size but also in interconnect parasitics.

## III. SUBSTRATE MATERIAL MINIATURIZATION: EMBEDDED CAPACITANCE

### A. *Principle of the embedded capacitance*

Usually there are lots of decoupling capacitors in the wireless sensor network nodes, which becomes a limit factor of integration and optimization of the motes. The embedded capacitance demonstrator uses the advanced dielectric technology to remove all the decoupling capacitors.

Figure 7 shows the principle of the embedded capacitance technology. It is obvious that the upper image with two copper layers and one dielectric layer in the middle form a basic capacitance. The model can be carried out for the multi-layer PCB as we use the ground and power layers as the two copper layers, and put some high dielectric material between them. This implementation is presented by the lower image of Figure 7.

The capacitance C, available from an embedded capacitance material is given by the equation for a parallel plate

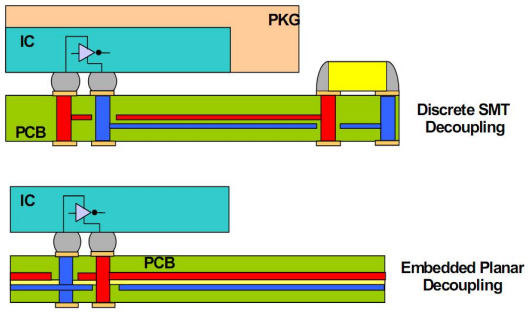



Fig. 7. The embedded capacitance principle

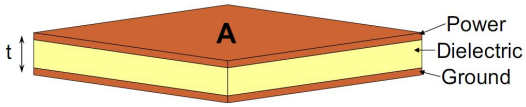



Fig. 8. Planar capacitance for the ECM material

capacitor:

$$C = \frac{\varepsilon_o \varepsilon_r A}{t}$$

where $\varepsilon_o$ is permittivity of free space, $\varepsilon_r$ relative dielectric constant, A is area and t is dielectric thickness.

C is rather low for the FR4 dielectric usually used for PCB fabrication because of the low dielectric constant of FR4 (4.35) and the thickness of the FR4 (several hundreds of $\mu$m). According to the above formula, choosing higher relative dielectric constant material and decreasing the dielectric thickness lead to a larger capacitance. The technology adopted in this paper is 14$\mu$m thick C-Ply material, whose dielectric constant is as high as 16. The capacitance/area can reach $1.25\mathrm{nF/cm^2}$.

Based on the fact that the mote is size of around 3cm×3cm, the capacitance of the embedded capacitance material is: 3cm×3cm×$1.25\mathrm{nF/cm^2}$=11.25nF. 11.25nF is far less than the recommended value for decoupling capacitor from the datasheet[3], which is 100nF for discrete capacitance. However, the embedded capacitance has very low parasitic inductance, which is key limitation for decoupling capacitance to increase its resonance frequency. Research [4] showed the embedded capacitance material of low value can provide sufficient decoupling of times of discrete capacitance.

Not only reduction of size, the benefits of the ECM also include:

- Improves power integrity by reducing power bus noise and PCB impedance
- Reduces EMI by decreasing resonance that causes EMI
- Can improve signal integrity via improvements in power integrity and EMI
- Dissipates heat much better than 2 mil FR-4 due to high thermal conductivity and low thermal impedance
- Increases usable board area by allowing for the removal of many, if not all, capacitors equal to or below 0.1 $\mu$F and their associated solder joints and vias

• Less sensitive to electrostatic discharge (ESD) than 2 mil FR-4
• Allows for delivery of required charge even with small, split planes unlike 2 mil FR-4.

### B. Design and results

The capacitance formed by the ground, power and dielectric layers can be the same function of decoupling if calculated with good parameters. By doing so, all the surface mount decoupling capacitors can be replaced by the embedded capacitance.

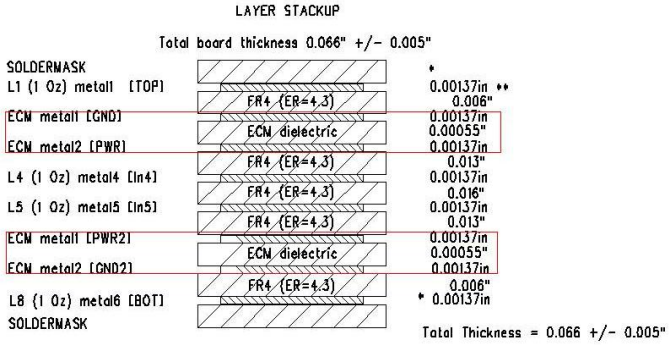



Fig. 9. The ECM design stack-up: two ECM layers

The high dielectric constant material (DK=16), with a thickness of 14$\mu$m, was inserted between the power and ground planes during the fabrication. To increase the total capacitance of the ECM materials, two layers of the ECM, shown as Figure /refECMlayer.JPG were used so that the parallel connection can double the capacitance and decrease the parasitics. To achieve even larger capacitance, more layers of the ECM materials can be used or the area of the ECM planes should be increased. Besides layer stack-up, no special change of the circuit connection or PCB layout is required, which means that if in some cases the ECM material could not provide enough decoupling capacitance, it is still easy to mount one discrete decoupling capacitor at the exact location designed previously. This relationship provides kind of flexibility of design and fabrication specification.

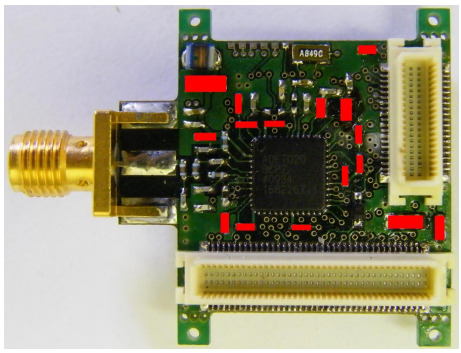


Fig. 10. The node's layout with the decoupling capacitors marked in red

Figure 10 shows the decoupling capacitors removed by the embedded capacitance. Obviously a large percentage of the circuit components are replaced and thus around 30% of PCB layout space is saved. Table V gives the details of the comparison of embedded and discrete capacitance.

TABLE V
DISCRETE CAPACITANCE VS. EMBEDDED CAPACITANCE

| Discrete Capacitance Removed | Embedded Capacitance | Ratio of Removed to Embedded | %of Total Discrete Caps Removed |
|---|---|---|---|
| 4×100nF 4×10nF | 11.25nF | 39 | 75% |

## IV. VERTICAL INTERCONNECT: EXPOY BASED 3D TECHNOLOGY

### A. Methods

The process [5] involves patterning of extremely thick layers of photoresist to achieve top to bottom side interconnect for relatively thick die. It is possible to provide a batch fabricated low parasitic packaging technology that does not require specially thinned die and can accommodate components of various heights.

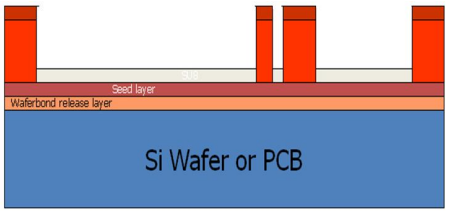



Fig. 11. The temporary substrate

This method fabricates the build up layers on a temporary substrate (on 100 4" P-type wafer in this case), which is shown in Figure 11. Prior to placing the die, the temporary substrate is provided with a "release" layer and an electrically conductive seed layer. The release layer, over the Si wafer, is formed by spin coating a wafer bonding material such as Wafer-bond HT-250 in a thickness of approximately 15$\mu$m. The next step is forming a conductive seed layer typically by either evaporation or sputtering of an adhesion layer comprising titanium (Ti) (20nm thick) and a conductive layer comprising Cu (200nm thick). The Ti acts as a seed layer for good adhesion of the Cu conduction layer to the substrate and the Cu conduction layer ensures electrical contact for plating purposes. Then a Cu layer (50$\mu$m) and a black nickel layer (5$\mu$m) are formed with the help of the photoresist SU-8. After these operations, the structure presented in Figure 11 is constructed.

Then soldering of the die is performed using a tool such as a flip chip bonder. Following this the photo-imageable resin is dispensed onto the substrate thus embedding the die. The composition of the epoxy resists is described in [6].

Lithography is used to create vias to the die/seed layer and to define the individual packages. The epoxy is exposed to UV light using a mask so that the epoxy is not cured in areas

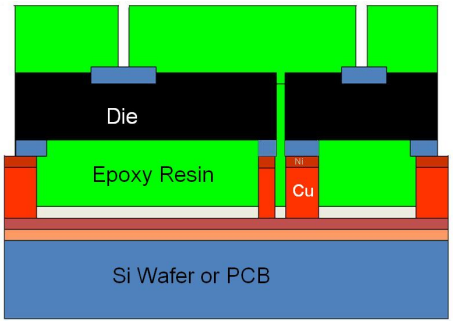



Fig. 12. The formation of the via using resin.

in which it is required to have vias. A development process using typical solvents such as EC solvent in an ultrasonic bath is carried out in order to open the vias. Horizontal tracks on top of the resin are produced using a conventional photoresist. Figure 12 shows this structure, with die in black color and resin in green.

Electroless deposition is used to provide a seed layer in the vias/tracks so as to permit electroplating of the interconnect. An electrically conductive material (Cu in this case) with a thickness of 30$\mu$m, is deposited in the pattern by electroplating techniques. Electrical interconnects (tracks) between the dies and the rest of the module are created. If multi-layer die stacking is required, this could be done easily by repeating the previous precedures. Then encapsulation is performed by depositing a thick layer of SU-8 for protection purpose. After releasing the packaged die the seed layer is removed using etching. Following this soler ball is applied for chip-board interconnect, which is also shown in Figure 13.

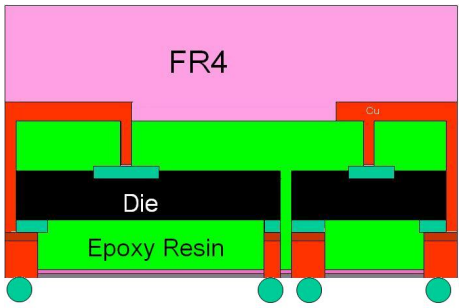



Fig. 13. Package for chip-board interconnect

During fabrication, novel thick photoresist process is developed. Some modified commercial materials (Cyracure Resin [6]) are used. Patterning of thick layers is achievable with the help of this material.

### B. Results

Cyracure products used in the proposed method are liquid epoxy without solvent, with the UV cure acting as a fast and effective means of curing. This approach uses the quick processing and low shrinkage properties of the epoxy and hence permits the patterning of very thick layers.

TABLE VI
VIA DIMENSION SPECIFICATION

| Vertical Via's | | | Horizontal interconnect | |
|---|---|---|---|---|
| Max via length | Min Via length | Min via spacing | Min width | Min spacing |
| 500$\mu$m | 200$\mu$m | 200$\mu$m | 50$\mu$m | 50$\mu$m |

The specification of the via in vertical and horizontal directions is presented in table VI. It is evident that the chip to chip connection length is reduced from several cm for ordinary PCB to about hundreds of $\mu$m in this 3D technology.

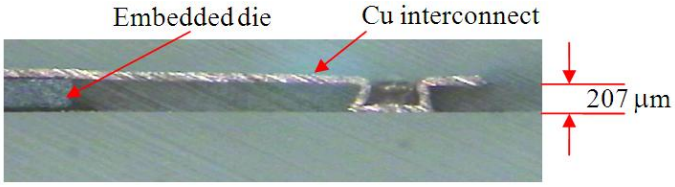



Fig. 14. Cross section of embedded die showing top side interconnect

After all the processes, the final structure of one build up layer can be seen in Figure 14. It is clear that the die is embedded by the epoxy resin and Cu is plated successfully as the conducting material.

### C. Electrical property

The length of the interconnect is no longer an issue as the wire interconnect has been dispensed with. Thus this leads to a low parasitic conductive interconnect for the die. Q3D Modelling is used to estimate parasitics of interconnect.

For stacked packaging: L_parasitic= 0.68 nH.

For side by side packaging: L_parasitic= 1.22 nH.

Compared with several nH as the parasitic inductance of the discrete components, the above values show the low parasitic property of the proposed technology.

## V. CONCLUSIONS

Three different levels of integration and miniaturization technologies are presented. Each has its own advantage and limitation.

1. Bare die flip chip: the design of PCB and mounting of bare die require special care because of the size of pad and track being small for standard PCB fabrication. However, the PCB can be made without any extra process, which leads to fast and cheap development of the PCB substrate. Mounting is rather reliable as well. The only problem would be the availability of bare die.

2. Embedded capacitance: not too much modification in PCB design is required. The embedded capacitance material can only be fabricated by some certain companies. The performance of the replace decoupling capacitance is not so straightforward; modeling and simulation of the mote stackup is needed. The extra procedure of the embedded capacitance material brings more cost of develop and fabrication time.

TABLE VII

PARASITIC PARAMETERS OF THE EQUIVALENT CIRCUIT.

| Packaging Technologies | Standard FR4 | Flip Chip | Embedded Capacitance Materials | Epoxy Based 3D Packaging (N: layer NO.) |
|---|---|---|---|---|
| Size | 100% | 70% | 75% | 1/N |
| Fabrication | Very easy | Easy | Medium | Difficult |
| Cost | Low | Medium | Medium | High |
| Develop time | Short | Short | Medium | Long |
| Modeling | Easy | Easy | Medium | Difficult |
| Applications | Wide | Bare Die Required | Decoupling only | Wide |

3. Epoxy based 3D technology: very difficult to implement the 200$\mu$m epoxy structure. The cost of develop this novel packaging technology is expensive and requires a long time. The benefits of the 3D packaging is also obvious: high density packaging, flexibility, interconnect improvement and miniaturization of the motes.

Finally Table 14 gives some summaries of the several packaging technologies we have discussed in WSN node applications.

In the future, it is possible to combine these three technologies into one mote.

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