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TiN/ZrO₂/Ti/Al Metal–Insulator–Metal Capacitors With Subnanometer CET Using ALD-Deposited ZrO₂ for DRAM Applications

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5 *Abstract*—We provide the first report of the structural and 6 electrical properties of TiN/ZrO₂/Ti/Al metal-insulator-metal ca-7 pacitor structures, where the ZrO₂ thin film (7–8 nm) is de-8 posited by ALD using the new zirconium precursor ZrD-04, also 9 known as Bis(methylcyclopentadienyl) methoxymethyl. Measured 10 capacitance-voltage (C–V) and current-voltage (I–V) charac-11 teristics are reported for premetallization rapid thermal annealing 12 (RTP) in N₂ for 60 s at 400 °C, 500 °C, or 600 °C. For the RTP at 13 400 °C, we find very low leakage current densities on the order of 14 nanoamperes per square centimeter at a gate voltage of 1 V and 15 low capacitance equivalent thickness values of ~0.9 nm at a gate 16 voltage of 0 V. The dielectric constant of ZrO₂ is 31 ± 2 after RTP 17 treatment at 400 °C.

18 *Index Terms*—ALD, capacitor, dynamic random access mem-19 ory (DRAM), effective dielectric constant, gate oxide, high-*k*, 20 metal–insulator–metal (MIM), ZrD-04, ZrO₂.

I. INTRODUCTION

21

22 T HE METAL-INSULATOR-METAL (MIM) capacitor for 23 dynamic random access memory (DRAM) and for other 24 analog and radio-frequency applications is attracting great in-25 terest in recent times [1]–[3] and must be aggressively scaled 26 to meet the expectations of the semiconductor roadmap [4]. 27 This demands the replacement of SiO₂ with a high dielectric 28 constant (k) oxide that will provide a capacitance equivalent 29 thickness (CET¹) for the dielectric in the low subnanometer

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¹The CET rule gives the same capacitance for a physically thicker high-k oxide layer, where CET = $3.9\varepsilon_0 A/C_{\mathrm{high}-k}$. CET and the equivalent oxide thickness (EOT = $3.9t_{\mathrm{high}-k}/k_{\mathrm{high}-k}$) are approximately equal for MIM devices; hence, we can use this to get an effective value for $k_{\mathrm{high}-k}(k_{\mathrm{eff}})$. Hence, $k = k_{\mathrm{high}-k} \sim k_{\mathrm{eff}}$.

regime and a leakage current density of less than 1 fA/cell, 30 equivalent to approximately $1 \times 10^{-8} - 1 \times 10^{-7}$ A/cm². 31

Replacing SiO₂ (k = 3.9) with ZrO₂($k \sim 20-40$) is consid- 32 ered by the authors as an investigative step toward introducing 33 favored Hf/Zr-based crystalline ternary oxides (k > 40) that 34 will further reduce the CET value in line with current expec- 35 tations [4]. Although DRAM MIM capacitor dielectrics with 36 a CET of ~0.9 nm are currently being implemented by the 37 semiconductor industry, the high-k values and the very low 38 leakage current densities reported here presently allow a margin 39 of opportunity for the ALD method to further reduce the phys- 40 ical thickness of the oxide and improve on the ~0.9-nm CET 41 while still maintaining acceptable leakage current densities [4]. 42

II. SAMPLE DETAILS AND TECHNIQUE 43

The substrate is n-type silicon with n+ type As surface 44 doping $(\sim 5 \times 10^{19} \text{ cm}^{-3})$ of Si(100). This surface is exposed 45 pre-MIM processing and forms a heavily As-doped SiO₂ layer, 46 on which a layer of TiN metal (~10 nm) is formed by 47 metal-organic chemical vapor deposition. An \sim 7–8-nm thick 48 ZrO₂ film is deposited by ALD in an ASM Pulsar 2000, hot 49 wall cross-flow reactor, at a reaction temperature of 275 °C, 50 using Bis(methylcyclopentadienyl) methoxymethyl zirconium 51 (SAFC Hitech, ZrD-04, see [5]) and ozone as precursors. Crys- 52 tallization to the preferred tetragonal ZrO₂ symmetry would 53 maximize the dielectric constant and minimize the CET; hence, 54 premetallization rapid thermal annealing (RTP) treatments are 55 employed to investigate the optimum temperature for increas- 56 ing the k-value without significantly increasing the leakage 57 current density. RTP is carried out for 60 s in N_2 (1000-mbar 58 pressure) either at 400 °C, 500 °C, or 600 °C, using the Jipelec 59 JetFirst 150 system. As-deposited samples (no RTP processing) 60 are retained for comparative measurements. DRAM test MIM 61 planar capacitors of various areas are formed from the as- 62 deposited and RTP-treated samples using photolithography and 63 a lift-off process for gate metallization. Device areas range from 64 400 to 160 000 μ m². The metal gate consists of 10 nm Ti and 65 200 nm Al, both deposited ex situ by e-beam. Ti, Al, and TiN 66 are the preferred metals because they meet the basic industrial 67 standards, such as acceptable work functions, good adhesion, 68 low cost, good step coverage, high temperature stability, and 69 low resistivity.

Capacitance voltage (C-V) and capacitor quality factor volt- 71 age (Q-V) measurements were performed at 25 °C using 72

0.040

0.035

0.030

0.025

0.020

0.015

0.010

0.005

0.000

-0.005

Capacitance (F/m²)

C-V

-1.2

1 kHz Q-V

-0.8

-0.4



0.0

Gate Voltage (V)

0.4

1 kHz C-V

100

90

60

50

40

30

20 Q-V-

10

0

1.2

0.8

g 80

Factor 70

Capacitor Quality

73 an HP4284A Precision LCR Meter. Current-voltage (I-V)74 measurements were performed with an HP4156A Precision 75 Semiconductor Parameter Analyzer. I-V measurements were 76 recorded at 25 °C, 50 °C, 75 °C, and 100 °C. All measurements 77 were performed on-wafer in a microchamber probe station 78 (Cascade Microtech, model Summit 12971B) in a dry-air en-79 vironment (dew point ~ -70 °C).

80 **III. MEASUREMENTS AND RESULTS**

Before using results from multifrequency C-V responses, 81 82 it is necessary to establish the effects of series resistance at 83 different frequencies. An established method is to compare the 84 series capacitance–voltage (C_s-V) response with the parallel 85 capacitance-voltage (C_p-V) response. If the C-V responses 86 differ in low leakage current density devices, then this is due to 87 series resistance effects.

Fig. 1 shows the C-V and Q-V responses for a low leakage 88 89 device of area 160 000 μm^2 having undergone an RTP of 90 400 °C. The 1 kHz responses are almost identical, whereas 91 the 10, 100, and 1 MHz responses are affected by series 92 resistance. In addition, Q values are good for the 1 kHz 93 responses (\sim 30) but reduce rapidly as the frequency is in-94 creased. Transmission electron microscopy (TEM) energy dis-95 persive X-ray spectroscopy shows a 10–20 nm SiO_2 layer 96 between the Si substrate and the TiN layer, which has a 97 high As doping. The thickness of this interlayer does not 98 increase with RTP treatment; however, its presence gives a 99 substrate resistivity/higher resistivity film underneath the TiN 100 layer and is the likely cause of the series resistance ef-101 fects for frequencies > 1 kHz. Hence, information extracted 102 from C-V responses is confined to the 1 kHz measure-103 ments, which are sufficient for electrical characterization. 104 Other higher frequency C-V data are ignored. The ob-105 served C-V frequency dispersion for frequencies greater than



Fig. 2. Gate leakage current (J-V) plots for 40 000 μ m² area devices with an RTP of 400 °C. Measurement temperatures (T_m) are 25 °C, 50 °C, 75 °C, and 100 °C. At 25 °C, J is approximately 1×10^{-9} A/cm² at 1 V. The dominant conduction mechanism for all positive gate voltages up to 1 V is SE, and the dominant conduction mechanisms for negative gate voltages at $T_m = 25$ °C are PF emissions in the range of -0.8 to -1 V, and SE in the range of 0 to -0.8 V. It can be seen that PF becomes increasingly dominant over SE in the range of 0 to -0.8 V as T_m increases, consistent with the lower work function of Ti compared with TiN. (Inset) SE's linear relationship of J/T^2 versus $10^3/T$ ($V_g = 1$ V), with an activation energy of ~0.4 eV and a TiN/ZrO₂ barrier height of \sim 1.4 eV.

1 kHz is more pronounced for devices with larger areas 106 $(\sim 0.005 \text{ F/m}^2 \text{ range} \rightarrow \sim 0.03 \text{ F/m}^2 \text{ range})$ and is also more 107 pronounced for devices processed with higher RTP tempera- 108 tures (~0.013 F/m² range \rightarrow ~0.025 F/m² range). In addition, 109 the Q-V responses show reductions in Q by at least an order 110 of magnitude for devices with larger areas and for devices 111 processed with higher RTP temperatures. It is noted, however, 112 that leakage current densities for all devices remain low on the 113 order of nanoamperes per square centimeter and scale with the 114 device area; hence, the leakage current is not a contributing 115 factor to the observed frequency dispersion. 116

Leakage current densities (J-V) at 1 V for all devices 117 (except RTP at 600 °C) are low at $\sim 1-2 \times 10^{-9}$ A/cm² for a 118 measurement temperature (T_m) of 25 °C. This would indicate 119 that C contamination is low [6]. The J-V of devices with an 120 RTP of 600 °C increases to \sim 3 \times 10⁻⁸ A/cm² (T_m = 25 °C) for 121 all device areas. Fig. 2 shows J-V plots for a 40 000 μ m² area 122 device with an RTP of 400 °C. The conduction mechanisms at 123 $V_q = 1$ V and -1 V are Schottky (SE) and Poole–Frenkel (PF) 124 emissions, respectively (see Fig. 2 inset for SE details). 125

Fig. 3 shows X-ray diffraction (XRD) data for as-deposited 126 and RTP-treated devices. The inset also shows a TEM mi- 127 crograph of a post-RTP of 600 °C device. Considering these 128 data with the k values shown in Fig. 4, there seems to be 129 cubic/tetragonal crystallites contained within an amorphous 130 structure. As the RTP temperature increases, the k value in- 131 creases, possibly due to a cubic-to-tetragonal phase change 132 due to contaminants, such as F becoming less influential on 133 the crystalline phase [6]. The high leakage at the 600 °C 134 RTP is likely due to the higher k polycrystalline structure 135 forming grain boundaries [7] and, possibly, Ti diffusion into 136 the oxide via the TiO interlayer formation at the TiN/ZrO2 137 interface [8]. Interlayer roughness can also increase with the 138 RTP temperature, as seen from TEM, where ZrO_2 will follow 139 the crystallization grains of TiN and Ti metals. However, this 140



Fig. 3. XRD data conducted at room temperature for the as-deposited and post 900 °C RTP devices $(2\Theta = 29^{\circ}-65^{\circ})$ and at ~400 °C, ~500 °C, and ~600 °C *in situ* for the equivalent RTP devices $(2\Theta = 25^{\circ}-37^{\circ})$. The dominant response at ~30° shows a significant cubic and/or tetragonal crystalline contribution which does not change significantly with RTP processing. (Inset) TEM micrograph of a post-RTP of 600 °C device.



Fig. 4. CET values extracted from 1 kHz C-V responses at $V_g = 0$ V, plotted against leakage current densities at $V_g = 1$ V. The calculated dielectric constants are also shown. (Star) As-deposited devices. (Square) Four-hundred-degree-Celsius RTP devices. (Circle) Five-hundred-degree-Celsius RTP devices. (Triangle) Six-hundred-degree-Celsius RTP devices. The physical thickness of ZrO₂ remains unchanged for all devices at 7–8 nm.

141 does not affect the device performance at or below an RTP of 142 500 $^{\circ}$ C [7].

143 Fig. 4 shows CET values extracted from 1 kHz C-V re-144 sponses at $V_g = 0$ V, plotted against leakage current densities at 145 $V_g = 1$ V. The estimated k-value ranges for ZrO₂ are included, 146 indicating an increase in k with RTP processing (22.5 ± 1.5 → 147 32 ± 5) and an associated reduction in CET with RTP process-148 ing (~0.3 nm). However, the leakage current density increases 149 (> 1 × 10¹) following the 600 °C RTP processing. These re-150 sults compare well with a recent study [6], apart from the lower leakage observed here for all devices except those with the 151 600 °C RTP processing.

MIM capacitors (TiN/ZrO₂/Ti/Al), having the oxide formed 154 by ALD with the new ZrD-04 precursor, are investigated for the 155 first time. C-V frequency dispersion (> 1 kHz) is observed, 156 which is more pronounced for devices with larger areas and 157 with higher RTP temperatures. Q-V responses reduce by at 158 least an order of magnitude with increasing frequency. The 159 leakage current densities at 1 V for all devices (except 600 °C 160 RTP) are on the order of nanoamperes per square centimeter. 161 Devices with an RTP of 600 °C show an unacceptable increase 162 in the leakage current density by at least an order of magni- 163 tude. CET and k values are extracted using the 1 kHz C-V 164 responses and TEM micrographs. There is an increase in k with 165 RTP processing $(22.5 \pm 1.5 \rightarrow 32 \pm 5)$, with an associated re- 166 duction in CET with RTP processing (~0.3 nm) toward the 167 subnanometer regime. The best CET-leakage values for post- 168 RTP (400 °C-500 °C) are ~0.9 nm and ~ 1×10^{-9} A/cm², 169 respectively. As the leakage current density values obtained at 170 1 V are below the target of $1 \times 10^{-8} - 1 \times 10^{-7}$ A/cm², there 171 remains scope for further reduction in CET with ZrO2 MIM 172 structures formed by ALD with the new ZrD-04 precursor. 173

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