University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

Characterization of germanium/silicon p–n junction fabricated by low temperature direct wafer bonding and layer exfoliation

Farzan Gity, Ki Yeol Byun' , Ko-Hsin Lee, Karim Cherkaoui, John M. Hayes, Alan P. Morrison, Cindy Colinge, and Brian Corbett

Citation: Appl. Phys. Lett. **100**, 092102 (2012); doi: 10.1063/1.3688174
View online: http://dx.doi.org/10.1063/1.3688174
View Table of Contents: http://aip.scitation.org/toc/apl/100/9
Published by the American Institute of Physics

Characterization of germanium/silicon *p–n* junction fabricated by low temperature direct wafer bonding and layer exfoliation

Farzan Gity,[1,2] Ki Yeol Byun,[1,a)] Ko-Hsin Lee,[1] Karim Cherkaoui,[1] John M. Hayes,[1] Alan P. Morrison,[1,2] Cindy Colinge,[1] and Brian Corbett[1]
[1]*Tyndall National Institute, Lee Maltings, Dyke Parade, Cork, Ireland*
[2]*Department of Electrical and Electronics Engineering, University College Cork, Cork, Ireland*

(Received 19 October 2011; accepted 2 February 2012; published online 27 February 2012)

The current transport across a p-Ge/n-Si diode structure obtained by direct wafer bonding and layer exfoliation is analysed. A low temperature anneal at 400 °C for 30 min was used to improve the forward characteristics of the diode with the on/off ratio at −1 V being >8000. Post anneal, the transport mechanism has a strong tunnelling component. This fabrication technique using a low thermal budget (T ≤ 400 °C) is an attractive option for heterogeneous integration. © *2012 American Institute of Physics*. [doi:10.1063/1.3688174]

Germanium (Ge) due to its compatibility with silicon (Si) processing is recognized as the best candidate for expanding the range of functions on complementary metal oxide semiconductor (CMOS)-based devices and circuits.[1,2] Monolithic integration by the deposition of high-quality single crystalline Ge layer onto Si is impeded by the lattice mismatch of about 4% leading to a high density of threading dislocations in the Ge epitaxial layer and requires high temperature post-growth annealing cycles.[3] An alternative approach which avoids the epitaxial relationship and could be done with low thermal budget is direct wafer bonding followed by removal of all but a thin layer of the material being transferred. The technique (Smart Cut™ (Ref. 4)) typically uses hydrogen implantation to form a sub-surface damaged layer which permits the separation (called exfoliation) of the top part of a wafer from its substrate after bonding. This technique does not require controlled wafer thinning as required with bulk wafer bonding.

To date, Si-on-insulator (SOI),[5] strained SOI,[6] Ge-on-insulator (GeOI),[7] and SiGe-on-insulator (SGOI)[8] substrates as well as Si n–p junctions[9] have been fabricated using this technique. More recently, Si/Ge junctions were fabricated by nanomembrane bonding where the junction is dominated by Fowler–Nordheim tunnelling leakage current.[10] In this letter, we perform a proof of concept of p-Ge/n-Si integration by using wafer bonding and layer exfoliation with a low thermal budget followed by the fabrication, characterisation, and analysis of the electrical transport across the interfacial oxide which is present between the p-Ge and n-Si regions.

To realise the Ge/Si diodes, a protective 100 nm thick layer of plasma enhanced chemical vapour deposition silicon dioxide was deposited on a p-Ge (gallium doped, resistivity = 0.05 Ω cm) substrate. The Ge substrate was then implanted at room temperature with H_2^+ ions at a dose of 5×10^{16} cm^{-2} and energy of 180 keV without active chuck cooling to create a defective blistered region below the surface. Following the implant, the oxide layer was removed in a dilute hydrofluoric acid solution. An n^+-Si (phosphorous doped, resistivity = 0.001 Ω cm) host wafer and the p-Ge donor wafer were cleaned in a dilute ammonium hydroxide–hydrofluoric acid–DI water using standard cleaning 1 (SC1) solution with ozone for the Si wafer and without ozone for the hydrogen-implanted Ge wafer.[11] The wafers were then loaded in an Applied Microengineering Limited (AML) AW04 aligner bonder chamber which was pumped down to 10^{-5} mbar and exposed for 10 min to oxygen free radicals generated by a remote plasma ring at 100 W. The chamber pressure during remote plasma exposure was 1 mbar. The wafers were then bonded under a force of 1 kN applied for 5 min at a chamber pressure of 10^{-5} mbar. The wafers were annealed *in situ* at 100 °C for 1 h with an applied force of 500 N followed by an *ex situ* annealing at 130 °C for 24 h in order to enhance the bond strength and induce hydrogen platelet nucleation. The higher the annealing temperature, the higher the bond strength; however, it is desirable that the splitting temperature is low enough to avoid stress problems associated with the difference in the thermal expansion coefficients. The layer exfoliation was triggered by a short time (5 min) anneal at 300 °C by increasing the pressure inside the blisters. The ramp-up rate was set to 0.5 °C/min in all annealing steps. Since hydrogen can diffuse out from the surface during the bonding process, the low temperature bonding step produces a more concentrated hydrogen profile at the peak implantation region due to the low diffusion coefficient of hydrogen in Ge at low temperatures.[12] After layer exfoliation a thin Ge film, which is 680 nm thick, remained bonded to the Si wafer. It has been shown for the same implant conditions that there is an approximately 150 nm thick "damage-free" region in the transferred Ge film located at the Ge bonded interface.[13]

The electrical transport across the p-Ge/n^+-Si junction was measured on fabricated mesa diodes (Fig. 1). Ohmic contacts were made using Ti/Au (25/250 nm) deposited by e-beam evaporation. The circular mesa structures ranging in diameter from 100 μm to 500 μm were formed by SF_6/C_4F_8 reactive ion etching through the junction to a depth of 2.5 μm. No passivation layers were used on the mesa sidewall. After the initial measurements, an annealing step was carried out for 30 min at 400 °C in H_2/N_2 (0.05/0.95) atmosphere in order to improve the performance of the devices. The entire fabrication process is done with temperature

a)Author to whom correspondence should be addressed. Electronic mail: eafslag@yahoo.co.kr.

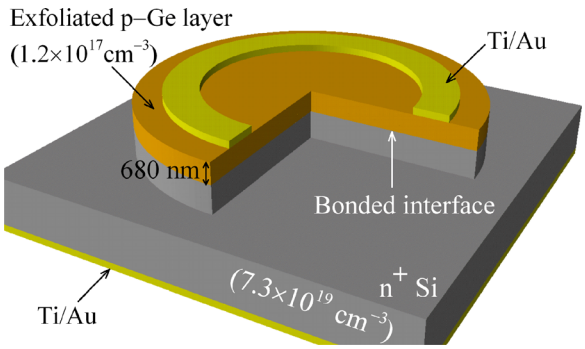

FIG. 1. (Color online) Schematic illustration of the Ge/Si diode made by hydrogen implantation and layer transfer technique. The diode diameter ranges from 100 μm to 500 μm.

$\leq$400 °C and is compatible with the backend processing of CMOS microelectronics.

Fig. 2(a) shows the log current versus voltage (*I–V*) characteristic of a 100 μm-diameter device with the inset showing the characteristics on a linear scale. The *I–V* curve exhibits rectifying behaviour before the anneal, but the forward bias current is limited. After the annealing step a superior *I–V* characteristic is obtained with an on/off current ratio of >50 000 and >8000 at −0.5 V and −1 V, respectively. The annealing step has improved the ideality factor of the forward current of the diodes from 5.48 to 2.28. The forward resistance also shows a reduction from 245 Ω to 15 Ω, both of which are indications of the improvement in the diode

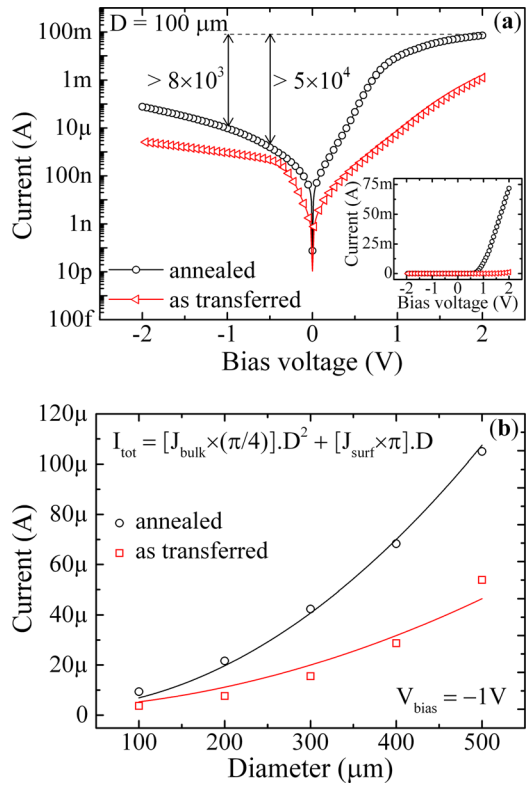

FIG. 2. (Color online) (a) *I–V* characteristic of a 100 μm-diameter diode before and after annealing. The ideality factor of the diode is 5.48 before annealing and 2.28 after annealing. The inset shows the *I–V* characteristic in linear scale. (b) Current versus device diameter at 1 V reverse bias before and after annealing; circular and square symbols: measured data; solid lines: fit from bulk leakage (per unit area) and surface leakage (per unit diameter).

behaviour. Fig. 2(b) shows the current versus mesa diameter at 1 V reverse bias before and after annealing. The leakage current can be divided into contributions from a bulk leakage current (proportional to device area) and a surface leakage current (proportional to device diameter). Before annealing, the bulk reverse current density was 10.5 mA/cm^2 and the surface leakage current was 31.8 μA/cm. However, after annealing, the bulk leakage current component is increased ($J_{bulk} = 27.8$ mA/cm^2), and the surface leakage is decreased to 9.55 μA/cm. This suggests that the annealing in H_2/N_2 ambient passivates the sidewall dangling bonds and possible damage due to the dry etching. However, the bulk current density is increased which can also be seen in Fig. 2(a). Different surface treatments using dilute hydrofluoric acid and hydrochloric acid were performed after annealing but did not affect the *I–V* characteristic of the diodes.

The carrier conduction mechanism was analysed by performing temperature dependent (20 °C to 100 °C) *I–V* measurements before and after the annealing step. The reverse leakage current was fit to $J = A \cdot \exp(-E_a/kT)$, where J is the diode current density, A is a constant, and E_a is the activation energy. Fig. 3 shows the Arrhenius-fit plots of J (in log scale) versus $1/kT$ for two different reverse bias voltages before annealing. As can be seen, the current density decreases when the measurement temperature is decreased. The value of E_a at −1 V and −2 V is 0.36 eV and 0.3 eV, respectively, which corresponds to almost half the Ge bandgap ($E_{g,Ge} = 0.66$ eV). This suggests that the generation–recombination current (or trap-assisted tunnelling) in the space charge region is dominant for the devices. Although the depletion region in the reverse bias regime expands mostly in the Ge layer, the origin of the generation–recombination component is not due to the quality of Ge film since capacitance–voltage measurements show that the depletion region is in the "damage-free" region of the transferred Ge film.

After annealing, the value of E_a at −1 V and −2 V is 0.022 eV and 0.013 eV, respectively, which is much smaller than the Ge bandgap (inset of Fig. 3). Thus, the leakage current density is relatively temperature independent and the conduction mechanisms are likely to be direct and band-to-band tunnelling through the interfacial oxide rather than

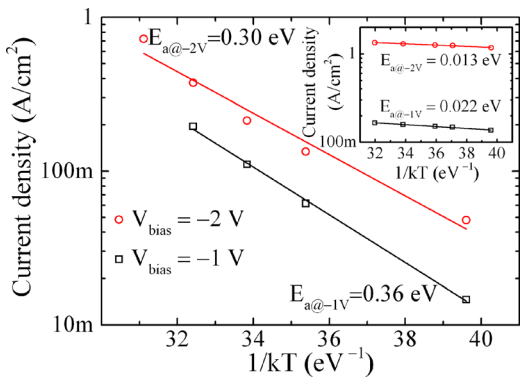

FIG. 3. (Color online) Current density versus $1/kT$ at 1 V and 2 V reverse bias voltages before annealing. The circular and square symbols are the measured data and the solid lines are the Arrhenius-fit plots. The inset shows the same plot after annealing. The value of the activation energy at each bias voltage is also shown.

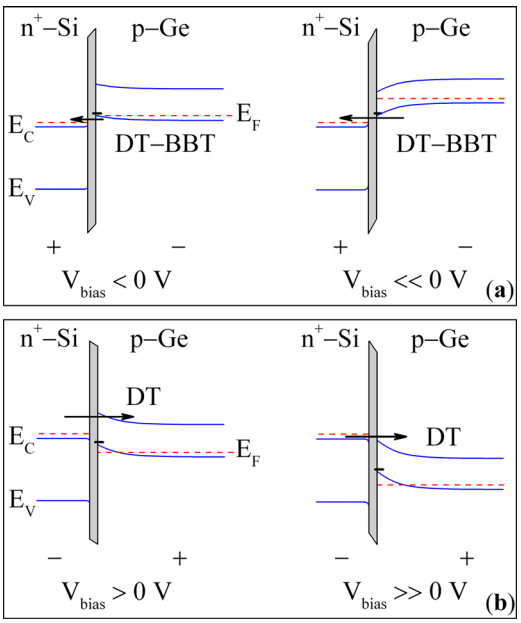

FIG. 4. (Color online) Schematic representation of the Ge/Si band diagram illustrating different carrier transport mechanisms in (a) reverse bias and (b) forward bias regimes. In this figure, DT and BBT stand for direct tunnelling and band-to-band tunnelling, respectively.

generation–recombination mechanism.[10] This can also be confirmed by the improvement of the diode ideality factor after the heat treatment (see Fig. 2(a)). As shown in Fig. 4, the trap energy level is close to the Ge valance band edge and, therefore, below the Fermi level at equilibrium. Assuming the traps to be acceptor-type, these traps would be negatively charged when filled with electron[14] and hence play a significant role in carrier transport by pulling the holes in the Ge substrate toward the Ge/oxide interface which in turn causes Ge band bending upward at low reverse voltages (Fig. 4(a)– left). As a result, electrons directly tunnel through the oxide from Ge valance band to Si conduction band. The band bending caused by traps would be less effective by increasing the reverse bias voltage as shown in Fig. 4(a)– right.

In the forward bias condition, as shown in Fig. 4(b), carrier transport starts with the electrons tunnelling through the oxide from Si conduction band to Ge conduction band. At low forward bias voltages (Fig. 4(b)– left), only the electrons at the tail of the Fermi distribution function of the Si conduction bank can travel to Ge conduction band by tunnelling directly through oxide. By increasing the bias voltage, the electrons which are close to the Fermi level contribute to the current. Based on the exponential behaviour of the Fermi distribution function, the current in the forward bias (in log scale) increases linearly with voltage; however, after reaching high enough bias voltage (~0.9 V), carriers below the Fermi level can travel to Ge conduction band (Fig. 4(b)– right) and the current is limited by the series resistance.

In conclusion, we have shown low thermal budget wafer bonding and layer exfoliation of a 680 nm thick p-type Ge film to bulk n-type Si substrate by fabricating Ge/Si diodes on this bonded pair. A high I_{on}/I_{off} ratio is obtained after low temperature annealing with a significant improvement of diode ideality factor. By performing electrical measurements at different temperatures, the carrier transport mechanism is shown to be dominated by generation–recombination component before annealing and due to direct tunnelling in forward bias and band-to-band tunnelling in reverse bias after annealing.

This work is supported by the Science foundation Ireland under grant numbers 07/SRC/I1173: Photonics Integration from Atoms to Systems, and 07/IN/I937: Low Temperature Wafer Bonding for Heterogeneous Integration. The authors would like to thank Dr. Paul Hurley for his helpful comments.

[1]J. Wang, M. Yu, G. Lo, D.-L. Kwong, and S. Lee, IEEE Photonics Technol. Lett. **23**, 765 (2011).
[2]S. Assefa, F. Xia, and Y. A. Vlasov, Nature **464**, 80 (2010).
[3]J. Michel, J. Liu, and L. C. Kimerling, Nat. Photonics **4**, 527 (2010).
[4]M. Bruel, Electron Lett. **31**, 1201 (1995).
[5]T. Hochbauer, A. Misra, M. Nastasi, and J. W. Mayer, J. Appl. Phys. **89**, 5980 (2001).
[6]I. Radu, R. Singh, M. Reiche, U. Gosele, and S. H. Christiansen, Mater. Sci. Eng., B **124–125**, 158 (2005).
[7]R. E. Hurley, H. Wadsworth, J. H. Montgomery, and H. S. Gamble, Vacuum **83**, S29 (2009).
[8]L. J. Huang, J. O. Chu, D. F. Canaperi, C. P. D'Emic, R. M. Anderson, S. J. Koester, and H.-S. P. Wong, Appl. Phys. Lett. **78**, 1267 (2001).
[9]A. M. Fecioru, S. Senz, R. Scholz, and U. Gosele, Appl. Phys. Lett. **89**, 192109 (2006).
[10]A. M. Kiefer, D. M. Paskiewics, A. M. Clausen, W. R. Buchwald, R. A. Soref, and M. G. Lagally, ACS Nano **5**, 1179 (2011).
[11]K. Y. Byun, P. Fleming, N. Bennett, F. Gity, P. McNally, M. Morris, I. Ferain, and C. Colinge, J. Appl. Phys. **109**, 123529 (2011).
[12]G. S. Khoo and C. K. Ong, J. Phys. C **20**, 1385 (1987).
[13]I. P. Ferain, K. Y. Byun, C. A. Colinge, S. Brightup, and M. S. Goorsky, J. Appl. Phys. **107**, 054315 (2010).
[14]F. Gity, J. M. Hayes, B. Corbett, and A. P. Morrison, IEEE J. Quantum Electron. **47**, 849 (2011).