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Design Procedure for Reduced Filter Size in a Buck Converter Using a 4th Order Resonance Filter

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***Abstract*—This paper presents a novel design procedure for 4th order and 4th order resonance (4thRes) output filters, for given buck converter specifications, making components selection a straightforward process. An accurate filter analysis is provided to predict the filter component currents and voltages in both frequency and time domains. Application of the analysis in a design study of a 20 MHz, 5.4 W buck converter shows that the 4thRes filter has the potential to reduce the output passive components for a wide duty cycle range. As compared with a 2nd order filter at V_{IN} = 6.6 V to V_{OUT} = 1.8 V, total inductance, inductor energy, capacitance and capacitor energy are 58%, 35%, 45% and 31% lower, respectively. Air-core PCB integrated solenoid inductors are considered for implementation and testing within a prototype converter to show the impact of these filters on converter performance. The 4thRes filter achieved 3.7% and 3.6% higher full load efficiency than the 2nd and 4th order filters, respectively, and better load transient performance.**

***Index Terms*—Buck converter, 4th order resonance filter, solenoid inductor, PCB inductor.**

I. Introduction

Passive components in DC-DC converters occupy large volumes and contribute significantly to the overall converter loss, particularly the magnetic components. There are several ways to optimise the utilisation of magnetic components in terms of size or losses, like increasing the switching frequency, using a different converter topology, e.g. multiphase buck [1]–[3], using a different component structure and material, or using a higher order filter for better controlling the output voltage ripple [4]. A 4th-order filter, as in Fig. 1(b), provides twice the roll-off rate of a 2nd-order filter (Fig. 1(a)) and therefore has the potential for size reduction of the filter components to provide the same level of output voltage ripple.

While various benefits of high order filters have been reported in the literature, methods for filter design to achieve given DC-DC converter specifications within a minimum size have not been described. Furthermore, the performance of coupled inductors in high order filters has the potential for significantly reducing the filter size due to the high attenuation they produce through resonance with one of the filter capacitors. However, this has not been fully exploited, partly because there is no detailed analysis available to enable the selection of suitable filter components. These gaps are addressed in this paper.

A design procedure for a 4th order low-pass filter for a DC-DC converter was introduced in [5]. The design procedure focused on increasing the converter bandwidth over a 2nd order filter (for an accelerator application) rather than on the size of the filter's passive components, where Butterworth, Bessel and critically damped filters were considered. The first inductance of the filter (L_1) was designed based on the inductor current ripple. Then, a normalised filter transfer function was applied to determine the remaining filter components needed to achieve the required attenuation at the switching frequency.

In [6], the focus of filter design for a 100 W, 2-phase buck converter was on optimising an envelope tracking system to pass the envelope frequencies of 1.5 MHz and reject the 10 MHz switching harmonic frequencies rather than on minimisation of the passive component sizes. After reviewing the filtering performance for a number of 4th order filters, including Butterworth and Bessel, a Legendre-Papoulis was selected.

A fully integrated 450 MHz buck converter with a 4th order filter was demonstrated in [7] to have a similar area to a 2nd

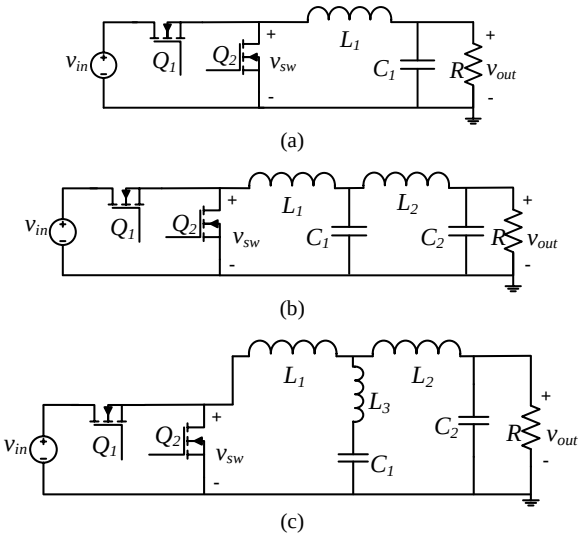


Fig. 1. (a) 2nd order filter, (b) 4th order filter, (c) 4th order resonance filter.

This paper is an extension of the conference paper titled "Design of 4th Order Resonance Filter for 5.4 W 20 MHz Buck Converter with PCB Integrated Inductor", presented in COMPEL proceedings, 2020.

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order filter of 0.4 mm^2; it was implemented with two side-by-side on-chip spiral air-core inductors. It was found that negative coupling (-0.05) due to the placement of the two inductors side-by-side provided greater attenuation than non-coupled at the switching frequency. This is a result of resonance between the mutual inductance and the first stage capacitor, as would be produced between L_3 and C_1 in the 4th-order resonance circuit (4thRes) of Fig. 1(c). However, neither the filter design nor the coupling factor was optimised to target given converter specifications.

A study in [8] investigated the coupled inductor as a filtering block for different applications. A 4th order filter with a coupled inductor was implemented and tested in a 50 kHz buck converter which showed 22 dB extra attenuation of the output ripple compared with a 2nd order filter. However, a size comparison was not presented, and the procedure for selecting filter components to achieve given DC-DC converter specifications was not described.

More studies considered high order filters in different circuit topologies and applications. A 42 kHz, 4 kW 4-phase buck converter with a 4th order filter and damping branch in each phase for a magnet power supply in a linear accelerator was described in [9]. A 500 W, 50 kHz buck converter with a 4th order filter was presented in [10], which utilised the two filter stages to implement two feedback loops for fast envelope tracking. Most recently, a 0.21 W, 118 MHz integrated boost converter with an additional LC stage was presented in [11] to reduce the output ripple for analog applications. However, these studies do not focus on the impact of high order filters on the size of the passive components.

Therefore, this study provides a novel selection procedure for the passive components in 4th order and 4th order resonance (4thRes) output filters with a view to reducing their size for a given buck converter specifications. The performance and size of the resulting filter components are benchmarked against those in a common 2nd order filter.

As mentioned, with a 4th order filter, there is an opportunity to implement the 3rd inductor, L_3, as the mutual inductance between L_1 and L_2. In this case, analysis of the proposed 4thRes filter using a non-coupled inductor is the first step toward component selection; then a coupled inductor can be used to achieve the same resonance feature. For simplicity, a Butterworth filter is chosen as a starting point for the filter design approach in this paper, but other standard filters could be applied.

The comparison is demonstrated for air-core PCB integrated inductors, where the target application is the first stage of a 2-stage step-down solution for Integrated Voltage Regulator (IVR) type loads powered by a wide input voltage battery source, e.g. as in [12], where stages 1 & 2 step down battery voltage from 3.8 to 1.5 V and then from 1.5 to 1 V respectively.

This paper is an extension of our previous conference paper [13], where new s-domain and time-domain analyses are presented to predict the voltages and currents in the filter components. In addition, results of experimental testing of the fabricated inductors with a buck converter are included. Section II presents the filter design procedure for a standard 4th order low pass filter in terms of the specifications for a DC-DC buck converter. Then the same approach is applied to the 4thRes filter. Section III provides methods for accurately predicting the voltages and currents of the filter components in the frequency and time domains so that they can be applied in passive component design. The filter design approach is employed to select passive components for a typical step-down buck converter specification, and these are compared against equivalent standard 2nd order low pass filter components in Section IV. Implementation of the required inductor designs in PCB is described in Section V, and prototype inductor designs are compared for equivalent 2nd order, 4th order and 4thRes filters. Prototype converter testing and simulation results are presented and discussed in Section VI. Finally, conclusions are discussed in Section VII.

II. Low pass filter design for a buck converter

A. Fourth-order low pass filter

To analyse the filter components, the following transfer function is derived by circuit analysis of a 4th order filter as shown in Fig. 1(b):

$$G(s)_{4th} = \frac{v_{out}(s)}{v_{sw}(s)} = \frac{1}{X} \tag{1}$$

where

$$X = 1 + \left(\frac{L_1 + L_2}{R}\right)s + (C_1L_1 + C_2L_1 + C_2L_2)s^2 + \left(\frac{C_1L_1L_2}{R}\right)s^3 + (C_1C_2L_1L_2)s^4 \tag{2}$$

v_{sw} is the switching voltage, v_{out} is the output voltage, R is the load resistance, and L_1, L_2, C_1 & C_2 are the filter's inductive and capacitive elements shown in Fig. 1(b).

The transfer function in (1) is compared with the 4th order normalised filter transfer function, e.g. Butterworth filter:

$$G(s)_{4th_norm} = \frac{1}{1 + a_1\frac{s}{\omega_0} + a_2\frac{s^2}{{\omega_0}^2} + a_3\frac{s^3}{{\omega_0}^3} + a_4\frac{s^4}{{\omega_0}^4}} = \frac{1}{1 + A_1s + A_2s^2 + A_3s^3 + A_4s^4} \tag{3}$$

where a_1, a_2, a_3 & a_4 are the normalized filter parameters i.e. 2.613, 3.414, 2.613 & 1 respectively for a Butterworth filter [14], $A_n = a_n / {\omega_0}^n$ is used in (3) for simplicity, and ω_0 is the cut-off frequency.

By solving (1) and (3) together, we can get the four filter unknowns L_1, L_2, C_1 & C_2 in terms of the load resistor, R:

$$L_1 = RA_1 - \frac{R{A_3}^2}{A_2A_3 - A_1A_4} \qquad L_2 = \frac{R{A_3}^2}{A_2A_3 - A_1A_4}$$
$$C_1 = \frac{(A_1A_4 - A_2A_3)^2}{RA_3\left(A_1A_2A_3 - {A_1}^2A_4 - {A_3}^2\right)} \qquad C_2 = \frac{A_4}{RA_3} \tag{4}$$

ω_0 is chosen to achieve the required attenuation of the output voltage steady-state peak-to-peak ripple ΔV_{OUT} at the switching frequency $\omega_{SW} = 2\pi F_{SW}$. ΔV_{OUT} is specified at 5% for the first

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stage of a 2-stage regulator, where tighter regulation is provided by the second stage on-chip. Note also that in practice, additional output capacitance may be required to satisfy load transient requirements [15], over and above steady-state ripple filtering, but this is not considered at the initial design phase, where the objective is to assess the switching ripple filtering performances of the various filters. The effect of additional output capacitance for transient requirements is considered in the measurements in Section VI.

As an approximation, ω_0 is calculated assuming the gain of the highest order of the filter transfer function in (3) for each nth harmonic as lower orders are negligible at frequencies > ω_0, i.e.:

$$G_n = \frac{\omega_0^4}{a_4 s^4} \quad \text{at } s = jn\omega_{SW} \tag{5}$$

By assuming that ΔV_{OUT} of the filter is the summation of each harmonic amplitude multiplied by the filter gain at the corresponding frequency, then ΔV_{OUT} is represented as:

$$\Delta V_{OUT} = \sum_{n=1}^{Nh} |G_n \Delta V_n| \tag{6}$$

where N_h is the number of harmonics required to be attenuated, considering the first 10 harmonics is accurate enough for this study, and ΔV_n is the peak-to-peak amplitude of the nth harmonic, which is calculated using Fourier analysis as follows:

$$\Delta V_n = \frac{4V_{OUT}}{n\pi D}\sin(n\pi D) \tag{7}$$

where D is the switching duty cycle.

By substituting (5) and (7) into (6), ΔV_{OUT} is found as:

$$\Delta V_{OUT} = \left(\frac{\omega_0}{\omega_{SW}}\right)^4 \frac{4V_{OUT}}{a_4 \pi D} \sum_{n=1}^{Nh} \frac{|\sin(n\pi D)|}{n^5} \tag{8}$$

As ΔV_{OUT} is a predetermined converter specification, then (8) is solved for ω_0 as follows:

$$\omega_0 = \omega_{SW}\sqrt[4]{\frac{\Delta V_{OUT}}{V_{OUT}} \frac{a_4 \pi D}{4\sum_{n=1}^{Nh} \frac{|\sin(n\pi D)|}{n^5}}} \tag{9}$$

In this way, the filter attenuates the switching harmonics to the desired ΔV_{OUT} value at the output signal. This filter design approach for DC-DC converter always results in $L_1 > L_2$ and $C_1 > C_2$.

B. Fourth-order resonance low pass filter (4thRes)

In the proposed 4thRes filter (shown in Fig. 1(c)), the inductor L_3 resonates with the capacitor C_1. Its transfer function was derived using circuit analysis and is simplified to:

$$G(s)_{4thRes} = \frac{v_{out}(s)}{v_{sw}(s)} = \frac{1 + (C_1 L_3)s^2}{X_{Res}} \tag{10}$$

where

$$\begin{aligned} X_{Res} = 1 &+ \left(\frac{L_1 + L_2}{R}\right)s \\ &+ (C_1L_1 + C_1L_3 + C_2L_1 + C_2L_2)s^2 \\ &+ \left(\frac{C_1}{R}(L_1L_2 + L_1L_3 + L_2L_3)\right)s^3 \\ &+ \left(C_1C_2(L_1L_2 + L_1L_3 + L_2L_3)\right)s^4 \end{aligned} \tag{11}$$

The resonance of C_1 with L_3 makes a double zero in the transfer function, which is placed at the switching frequency to attenuate the first harmonic amplitude effectively. For frequencies below the double zero, the resonance filter response follows a 4th order characteristic, and afterwards, it follows a 2nd order characteristic, which makes the gain at the 2nd harmonic greater than the 1st harmonic. This will be considered in the selection of the cut-off frequency. The double zero is added to the normalised filter transfer function as follows:

$$\begin{aligned} &G(s)_{4thRes_norm} \\ &= \frac{1 + \frac{1}{\omega_{SW}^2}s^2}{1 + a_1\frac{s}{\omega_0} + a_2\frac{s^2}{\omega_0^2} + a_3\frac{s^3}{\omega_0^3} + a_4\frac{s^4}{\omega_0^4}} \\ &= \frac{1 + \frac{1}{\omega_{SW}^2}s^2}{1 + A_1 s + A_2 s^2 + A_3 s^3 + A_4 s^4} \end{aligned} \tag{12}$$

By comparing (10) and (12), we can get from the denominator four equations with five unknowns, i.e., L_1, L_2, L_3, C_1 & C_2. One unknown is eliminated with the help of the numerator by placing the double zero at the switching frequency to give:

$$L_3 = \frac{1}{{\omega_{SW}}^2 C_1} = \frac{1}{4\pi^2 {F_{SW}}^2 C_1} \tag{13}$$

Substituting (13) into (11) eliminates L_3, then (11) and the denominator of (12) are solved together to get:

$$L_1 = \frac{R{\omega_{SW}}^2\left({A_1}^2 A_4 - A_1 A_2 A_3 + {A_3}^2\right)}{A_3 + {\omega_{SW}}^2(A_1A_4 - A_2A_3)} \tag{14}$$

$$L_2 = \frac{RA_3(A_1 - A_3{\omega_{SW}}^2)}{A_3 + {\omega_{SW}}^2(A_1A_4 - A_2A_3)} \tag{15}$$

$$C_1 = \frac{\left(A_3 + {\omega_{SW}}^2(A_1A_4 - A_2A_3)\right)^2}{RA_3{\omega_{SW}}^4\left(A_1A_2A_3 - {A_1}^2A_4 - {A_3}^2\right)} \tag{16}$$

$$C_2 = \frac{A_4}{RA_3} \tag{17}$$

Similar to Section II.A, ω_0 calculations assume the gain of the highest order of the filter transfer function in (12) for nth harmonic as follows:

$$G_n = \frac{1 + \frac{s^2}{\omega_{SW}^2}}{\frac{a_4}{\omega_0^4}s^4} \quad \text{at } s = jn\omega_{SW} \tag{18}$$

As equations (6) and (7) apply here as well, then (7) and (18) are substituted into (6) to express ΔV_{OUT} as follows:

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$$\Delta V_{OUT} = \left(\frac{\omega_0}{\omega_{SW}}\right)^4 \frac{4V_{OUT}}{a_4 \pi D} \sum_{n=1}^{Nh} \frac{|(1-n^2)\sin(n\pi D)|}{n^5} \quad (19)$$

Then (19) is solved for ω_0 as follows:

$$\omega_0 = \omega_{SW} \sqrt[4]{\frac{\Delta V_{OUT}}{V_{OUT}} \frac{a_4 \pi D}{4\sum_{n=1}^{Nh} \frac{|(1-n^2)\sin(n\pi D)|}{n^5}}} \quad (20)$$

The formulas (13) to (17) are used to determine the component values of the 4thRes filter in a buck converter. This filter design approach always results in $L_1 > L_2 > L_3$ and $C_1 > C_2$.

Fig. 2 shows a comparison between the calculated cut-off frequency in (9) and (20) at $\Delta V_{OUT}/V_{OUT} = 0.05$, assuming the 1st stage specification of a 2-stage converter as discussed above. It shows that ω_0 is higher for the 4thRes filter over the whole duty cycle range, which means it is expected to require smaller passive components than the normal 4th order filter and allow higher bandwidth of the closed-loop converter. However, closed-loop control is not within the scope of this study.

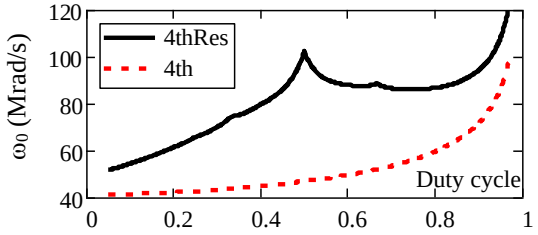


Fig. 2. Comparison of the calculated cut-off frequency at $\Delta V_{OUT}/V_{OUT} = 0.05$.

III. Filter Analysis

In addition to filter component values, the filter size is determined by the voltages and currents carried by each filter component. To predict these voltages and currents, the output filter is first analysed in the s-domain, including the components' parasitic elements as detailed in Fig. 3, and the results are then translated to the time domain.

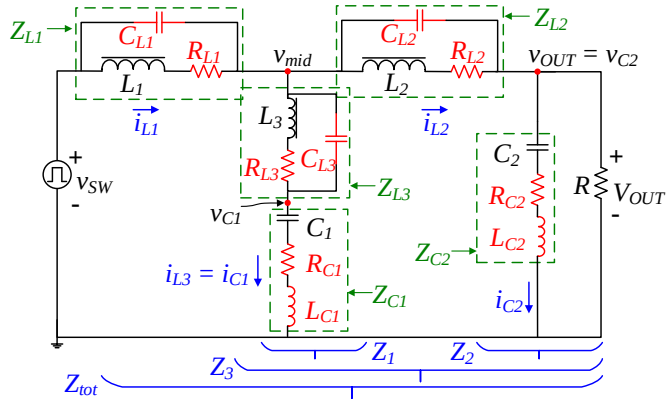


Fig. 3. 4thRes output filter with parasitic elements.

A. s-domain analysis

To simplify the filter analysis, its components are grouped in the s-domain impedances Z_1, Z_2, Z_3 and Z_{tot}, which are:

$$Z_1(s) = Z_{L3}(s) + Z_{C1}(s) \quad (21)$$

$$Z_2(s) = \frac{RZ_{C2}(s)}{R + Z_{C2}(s)} \quad (22)$$

$$Z_3(s) = \frac{Z_1(s)\left(Z_{L2}(s) + Z_2(s)\right)}{Z_1(s) + \left(Z_{L2}(s) + Z_2(s)\right)} \quad (23)$$

$$Z_{tot}(s) = Z_{L1}(s) + Z_3(s) \quad (24)$$

Then the filter gain is divided into two stages, G_1 and G_2 for the 1st and 2nd filter stages, respectively, which are combined to get the overall filter gain G_{filter} as follows:

$$G_1(s) = \frac{v_{mid}(s)}{v_{sw}(s)} = \frac{Z_3(s)}{Z_{L1}(s) + Z_3(s)} \quad (25)$$

$$G_2(s) = \frac{v_{out}(s)}{v_{mid}(s)} = \frac{Z_2(s)}{Z_{L2}(s) + Z_2(s)} \quad (26)$$

$$G_{filter}(s) = \frac{v_{out}(s)}{v_{sw}(s)} = G_1(s)G_2(s) \quad (27)$$

Then the voltages v_{mid}, v_{C1} and v_{C2} are calculated.

$$v_{mid}(s) = G_1(s)v_{SW}(s) \quad (28)$$

$$v_{C2}(s) = v_{out}(s) = G_{filter}(s)v_{SW}(s) \quad (29)$$

$$v_{C1}(s) = v_{mid}(s)\frac{Z_{C1}(s)}{Z_{L3}(s) + Z_{C1}(s)} \quad (30)$$

Then inductor currents i_{L1}, i_{L2} and i_{L3} are calculated:

$$i_{L2}(s) = \frac{v_{mid}(s) - v_{C2}(s)}{Z_{L2}(s)} \quad (31)$$

$$i_{L3}(s) = i_{C1}(s) = \frac{v_{mid}(s)}{Z_{L3}(s) + Z_{C1}(s)} \quad (32)$$

$$i_{L1}(s) = i_{L2}(s) + i_{L3}(s) = \frac{v_{SW}(s) - v_{mid}(s)}{Z_{L1}(s)} \quad (33)$$

This s-domain analysis can accurately predict the frequency components of the voltages and currents of each element. Furthermore, it is used to predict the time domain waveform, which improves the prediction of each component performance and the steady-state output voltage ripple over different loading conditions.

B. Time-domain conversion

Assuming linear characteristics of the filter components, the time-domain calculations are done using the standard amplitude-phase Fourier representation:

$$f(t) = A_0 + \sum_{n=1}^{N} A_n \cos(n\omega t + \varphi_n) \quad (34)$$

where A_0 is the average value, A_n and φ_n are the nth harmonic amplitude and phase, respectively, extracted from the s-domain solution in Section III.A. The number of harmonics N is infinity ideally, but $N = 50$ was found accurate enough for this study, as increasing N increases the computation time. Hence, the switching node voltage is represented as:

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$$v_{SW}(t) = V_{Out} + \sum_{n=1}^{N} V_n \cos\big(n\omega(t - 0.5DT_{SW})\big) \quad (35)$$

where V_n is the harmonic amplitude, $V_n = \Delta V_n/2$, presented in (7), and T_{SW} is the switching period $T_{SW} = 1/F_{SW}$.

Then v_{C1}, v_{C2}, i_{L1}, i_{L2} and i_{L3} are represented (at $s_n = jn\omega_{SW}$) as follows:

$$v_{C1}(t) = V_{OUT} + \sum_{n=1}^{N} \left|\frac{G_1(s_n)Z_{C1}(s_n)}{Z_{L3}(s_n) + Z_{C1}(s_n)}\right| V_n \cos\left(n\omega_{SW}(t - 0.5DT_{SW}) + \angle\left(\frac{G_1(s_n)Z_{C1}(s_n)}{Z_{L3}(s_n) + Z_{C1}(s_n)}\right)\right) \quad (36)$$

$$v_{C2}(t) = V_{OUT} + \sum_{n=1}^{N} |G_{filter}(s_n)| V_n \cos\left(n\omega_{SW}(t - 0.5DT_{SW}) + \angle\left(G_{filter}(s_n)\right)\right) \quad (37)$$

$$i_{L2}(t) = I_O + \sum_{n=1}^{N} \left|\frac{G_1(s_n) - G_{filter}(s_n)}{Z_{L2}(s_n)}\right| V_n \cos\left(n\omega_{SW}(t - 0.5DT_{SW}) + \angle\left(\frac{G_1(s_n) - G_{filter}(s_n)}{Z_{L2}(s_n)}\right)\right) \quad (38)$$

$$i_{L3}(t) = \sum_{n=1}^{N} \left|\frac{G_1(s_n)}{Z_{L3}(s_n) + Z_{C1}(s_n)}\right| * V_n \cos\left(n\omega_{SW}(t - 0.5DT_{SW}) + \angle\left(\frac{G_1(s_n)}{Z_{L3}(s_n) + Z_{C1}(s_n)}\right)\right) \quad (39)$$

$$i_{L1}(t) = i_{L2}(t) + i_{L3}(t) \quad (40)$$

where I_O is the DC output current.

As equations (36) to (40) are in the time domain, they are used to calculate maximum, minimum and RMS values for each filter component, which allows the design and selection of the components.

$v_{OUT}(t)$ from equation (37) is used to predict ΔV_{OUT} versus loading and hence adjust the filter design if needed.

IV. Design Study

The considered converter steady-state specifications for this study are listed in Table I, which are typical of point-of-load converter requirements for an intermediate step-down stage, which then is followed by a second stage with tighter output voltage regulation as in [1][12][16] for IVR application. The basic buck converter 2nd order output filter in Fig. 1(a) is taken as a baseline where the inductance and capacitance are calculated based on inductor current ripple (ΔI_L) and capacitor voltage ripple (ΔV_{OUT}), respectively.

$$L_{2nd} = \frac{V_{OUT}(1 - D)}{\Delta I_L F_{SW}} \quad (41) \qquad C_{2nd} = \frac{\Delta I_L}{8F_{SW}\Delta V_{OUT}} \quad (42)$$

For comparison purposes, the total capacitance is fixed for the 2nd and 4th order filters designs ($C_{2nd} = C_1 + C_2$), so that the improvement in magnetics can be seen. C_1 and C_2 are chosen at the maximum V_{IN} (as a worst-case) according to the procedure explained in Section II.A. As a result, ΔI_L for the 2nd order is set to 36.5%.

To compare the inductors' energy, the calculated currents in the 4th order and 4thRes filters are approximated, as almost all the current ripple in L_1 flows through C_1. So, the current ripple in L_2 can be neglected. This is seen in the inductor current waveforms from the converter simulation in Fig. 4, which shows that the current in L_2 is almost DC with negligible ripple. Therefore, the total inductor peak energy is calculated as:

$$E_L \approx \frac{1}{2}\left[L_1\left(I_{DC} + \frac{\Delta I_{L_1}}{2}\right)^2 + L_2(I_{DC})^2 + L_3\left(\frac{\Delta I_{L_3}}{2}\right)^2\right] \quad (43)$$

where

$$\Delta I_{L_3} \approx \Delta I_{L_1} \approx \frac{V_{OUT}(1 - D)}{L_1 F_{SW}} \quad (44)$$

TABLE I
Converter Steady-State Specifications

Symbol	Quantity	Value	Unit
F_{SW}	Switching frequency	20	MHz
V_{IN}	Input voltage	2.5 – 6.6	V
V_{OUT}	Output voltage	1.8	V
I_{DC}	Output DC current	3	A
ΔI_L	Output current ripple	1.1 (36.5%)	A
ΔV_{OUT}	Output voltage ripple	90 (5%)	mV

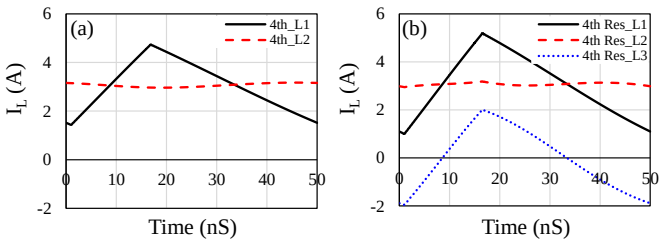


Fig. 4. Simulation inductor currents at V_{IN} = 6.6 V: (a) 4th order, (b) 4thRes.

Fig. 5 compares the resulting passive component specifications for 2nd order, 4th order and 4thRes filters versus the switching duty cycle. Calculations are based on Butterworth filter parameters. The comparison of the total inductance in Fig. 5(a) shows that the 4th order filter required less inductance than the 2nd order filter for duty cycles less than 0.62. Meanwhile, the 4thRes filter achieved smaller inductance than the regular 4th order filter over almost the whole duty cycle range. It achieved smaller inductance than the 2nd order filter for duty cycles less than 0.74.

The total inductor peak energy in Fig. 5(b) reflects a similar relative trend. Moreover, the smallest total inductor peak energy is achieved by the 4thRes filter, which is 35.6% lower than the 2nd order design (at the minimum duty). Note that, practical passive components selection for a converter needs to account for the worst operating condition, i.e. at the minimum duty cycle of 0.27.

The total capacitance comparison in Fig. 5(c) shows that the 4thRes filter achieved smaller steady-state capacitance than

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other configurations. This shows the potential of the 4thRes filter in reducing the size of passive components, with a straightforward design procedure for component selection based on a normalised filter, i.e. a Butterworth filter.

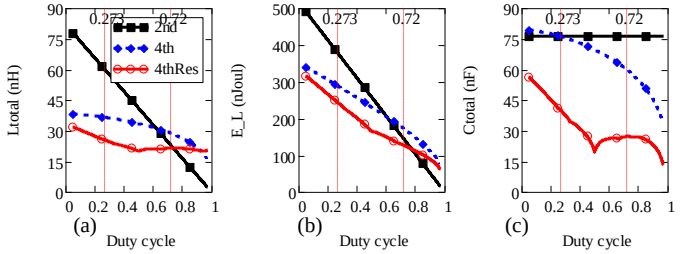


Fig. 5. Comparison of passives between 2nd order, 4th order and 4thRes filters at V_{OUT} = 1.8 V, ΔV_{OUT} = 90 mV, I_{DC} = 3 A, F_{SW} = 20 MHz: (a) Total inductance, (b) Total inductors peak energy, (c) Total capacitance.

With the aid of the filter design and analysis in Section II, the filter components chosen for the worst-case duty cycle are compared in Table II, showing the advantages of the 4thRes filter in reducing the passive components. These calculations assume an ESR value of 5 mΩ for C_1 and C_2 branches to account for the parasitic effect in increasing the output voltage ripple in the real converter.

TABLE II
DESIGN COMPARISON AT MAXIMUM V_{IN}

Quantity	2nd	4th	4thRes
L1 (nH)	59.7	23.4	15.6
L2 (nH)	-	16.6	8.0
L3 (nH)	-	-	2.06
Total inductance (nH)	59.7	40	25.7
Total inductors peak energy (nJoul)	375.8	313	244.5
C1 (nF)	76.2	67	30.8
C2 (nF)	-	16.3	9.6
Total capacitance (nF)	76.2	83.3	40.4
Total capacitors peak energy (nJoul)	129.6	152.2	90

The commercial capacitors selected from Murata for the initial design are shown in Table III. ESR (at 20 MHz) and ESL values were deduced from the datasheet. The 4thRes filter relies on a resonance branch (L_3-C_1), and C_1 consists of four parallel capacitors, each with an effective capacitance of 9.86 nF and parasitic inductance of 0.238 nH. So, the value of L_3 needs to be corrected to 1.55 nH instead of 2.06 nH to maintain resonance at the switching frequency.

TABLE III
SELECTED COMMERCIAL CAPACITORS

Filter	Cap	PN	C (nF)	ESR (mΩ)	ESL (nH)
2nd	C1	3x GRM2165C1H273JA01	3x 26.8	9.55 /3	0.3 /3
4th	C1	3x GRM2165C1H273JA01	3x 26.8	9.55 /3	0.3 /3
	C2	2x GCM033R71A103KA03	2x 9.68	60 /2	0.21 /2
4thRes	C1	4x GRM1555C1E103JE01	4x 9.86	10.4 /4	0.238 /4
	C2	GRM1857U1A103JA44	10.3	18	0.31

The calculated filter gain in (27) is shown in Fig. 6 for the 4th and 4thRes filters, respectively, (considering parasitic elements) at 0.1 and 3 A load. Fig. 6(b) shows the resonance notch at the switching frequency of 20 MHz which attenuates the 1st harmonic significantly, hence allowing for output filter reduction. Furthermore, the predicted time-domain waveforms and ΔV_{OUT} performance of the 4th and 4thRes filters are shown in Fig. 7 and Fig. 8, respectively, at the maximum V_{IN} of 6.6 V. Attenuation at the resonant frequency can also be seen by comparing v_{C2} and i_{L2} waveforms in Fig. 7 and Fig. 8, where the ripple frequency in the 4thRes is dominated by the 2nd harmonic at 40 MHz rather than at 20 MHz.

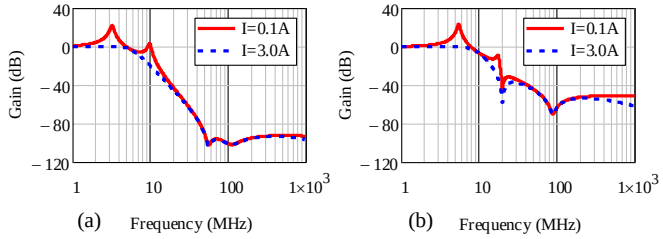


Fig. 6. Calculated filter gain at I_{DC} = 0.1 & 3 A: (a) 4th order filter, (b) 4thRes.

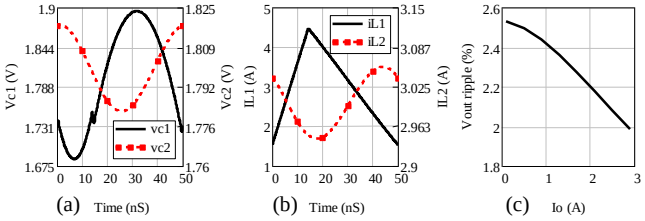


Fig. 7. Predicted steady-state performance of the 4th order filter at V_{IN} = 6.6 V, V_{OUT} = 1.8 V, I_{DC} = 3 A, F_{SW} = 20 MHz: (a) $v_{C1}(t)$ and $v_{C2}(t)$, (b) $i_{L1}(t)$ and $i_{L2}(t)$, (c) ΔV_{OUT} vs load.

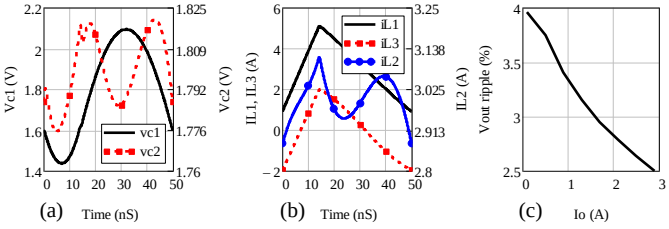


Fig. 8. Predicted steady-state performance of the 4thRes filter at V_{IN} = 6.6 V, V_{OUT} = 1.8 V, I_{DC} = 3 A, F_{SW} = 20 MHz: (a) $v_{C1}(t)$ and $v_{C2}(t)$, (b) $i_{L1}(t)$, $i_{L2}(t)$ and $i_{L3}(t)$, (c) ΔV_{OUT} vs load.

Practically, the choice of C_2 is dominated by specifications for voltage over/undershoot during transient load changes rather than steady-state ripple voltage. This may result in a much larger capacitance value for C_2, as demonstrated in Section VI. However, the procedure outlined here ensures that steady-state specifications are met at least, and any additional transient capacitance would act to reduce the steady-state ripple further.

V. PCB INDUCTOR DESIGN

For the prototype converter design, air-core solenoid designs integrated into a standard 2-layer FR4 PCB are considered to illustrate the relative advantage provided by the circuit topologies for inductors fabricated under the same processing constraints. Therefore, while the inductors are not competitive area-wise with inductors having magnetic cores, they illustrate the potential for relative improvement provided by the 4th order topologies. The inductor design is based on PCB manufacturing constraints, i.e. the copper thickness is 70 µm, PCB height is

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1.6 mm, via diameter is 0.2 mm, minimum copper trace width and spacing is 0.15 mm, the via annular ring is 0.125 mm, and the minimum solder mask width is 0.07 mm. For this study, the conductor widths are calculated based on the standard IPC-2221A [17] for a temperature rise of 50^{O}C for the maximum inductor RMS current considering passive cooling. The newer standard IPC-2152 [18] can be considered in future work. With these assumptions and constraints, the minimum via-to-via centre spacing is 0.52 mm hence the minimum conductor width is 0.37 mm. The inductance of a PCB solenoid inductor, Fig. 9(a), is calculated approximately as:

$$L_S = \frac{\mu_0 {N_T}^2 (W_{Sol} - 2D_{Via})(H_{Sol} - 2T_C)}{(N_T + 1)W_C + N_T S_C} \quad (45)$$

where D_{Via} is the PCB via diameter, W_{Sol} & H_{Sol} are the inductor's overall width and height, W_C and T_C are the conductor width and thickness, respectively, and S_C is the conductors spacing.

DC resistance of the solenoid inductor is calculated as:

$$R_{DC} = (N_T + 1)R_{DC_st} + N_T\left(R_{DC_dia} + 2R_{DC_via}\right) \quad (46)$$

where R_{DC_st}, R_{DC_dia} and R_{DC_via} are DC resistances of top layer straight conductors, bottom layer diagonal conductors, and PCB via, respectively. R_{DC_via} accounts for a via plating thickness of 25 µm.

Photos of the manufactured inductors are presented in Fig. 10, which also shows land footprints for the capacitors listed in Table III. A solenoid design is considered for all inductors except L_3. Its inductance is 1.55 nH which is too small for a solenoid configuration in PCB, so it is achieved by a single strip conductor shown in Fig. 10(c).

The inductor sizes are compared in Table IV, showing the potential of the 4thRes filter in reducing total inductor size while adhering to practical manufacturing constraints. Size reduction of the 4thRes filter versus the 2nd order (48%) correlates to some extent with the percentage reduction in the calculated peak energy in Table II (35%), while there is a similar correlation with the standard 4th order filter (20%) reduction in size versus 17% reduction in peak energy). Differences are due to practical restrictions within a given manufacturing technology. The inductor AC resistance is calculated according to Dowell's analysis [19], similar to [20], $R_{AC,n} = F_n R_{DC}$, where F_n is the resistance factor at the n harmonic. Only the switching frequency component (1st harmonic) is considered for R_{AC} calculation in this study. Then the inductor power loss is calculated as follows:

$$P_{Loss} = \sum_{L_1,L_2,L_3} I_{DC}^2 R_{DC} + \sum_{L_1,L_2,L_3} I_{RMS_AC}^2 R_{AC} \quad (47)$$

The calculated inductor losses of the three output filters are presented in Fig. 11 for the converter specifications listed in Table I. It shows a reduction in full load loss at the cost of light load loss. The AC loss in the 4thRes filter occurs mainly in L_1 (although L_1 and L_3 carry almost the same current ripple) because L_1 is bigger than L_3; hence has a much higher AC resistance of 72.8 vs 7.7 mΩ, as shown in Table IV. Overall, there is a trade-off between inductor size and light-load losses, while both size and full load losses are improved for the 4thRes. The inductors' L_S and R_S were measured using an impedance analyser at 20 MHz and shown in Table IV, which correlates with the design. The difference between measured and simulated R_S values could be due to the following reasons:

- Measurements at 20 MHz are sensitive to accurate calibration of the impedance analyser, particularly short circuit calibration.
- The simulation model used solid vias, but they are drilled in the PCB with 25 µm inner wall copper thickness.
- Accurate simulation at 20 MHz is challenging as it requires a much finer mesh size of the copper and the air nearby, which requires significant computational resources.

With all output filter components chosen, the overall size of the components is compared in Fig. 9(b), which correlates to some extent with the calculated peak energy in Table II.

TABLE IV
DESIGNED INDUCTORS COMPARISON

	Filter	2nd	4th		4thRes		
Design parameters	Inductor	L_1	L_1	L_2	L_1	L_2	L_3
	L (nH)	59.7	23.4	16.6	15.6	8	1.55
	No. of turns	5	3	2	2	1	0
	Length (mm)	2.98	1.94	1.42	1.42	0.89	2.46
	Width (mm)	4.30	2.98	3.15	2.93	2.77	0.37
	Height (mm)	1.6	1.6	1.6	1.6	1.6	0.07
	Total area (mm^2)	12.8	10.2		7.5		
	Total size (mm^3)	20.5	16.4		10.6		
	R_{DC} (mΩ)	45.6	22.4	16.1	15.4	8.3	1.63
	R_{AC} (mΩ)	216.4	106.1	76.3	72.8	39.2	7.7
FEA at 1 Hz	L_S (nH)	59.90	24.07	16.98	15.81	8.20	1.62
	R_S (mΩ)	45.64	22.53	16.54	15.76	8.89	1.64
FEA at 20 MHz	L_S (nH)	58.3	23.5	16.4	15.3	8	1.55
	R_S (mΩ)	72.6	32.5	26.4	25.2	13.6	4.6
Meas. at 20 MHz	L_S (nH)	58.9	21	18.1	13.88	8.78	1.62
	R_S (mΩ)	230.9	100	77.5	69.21	42.21	7.79

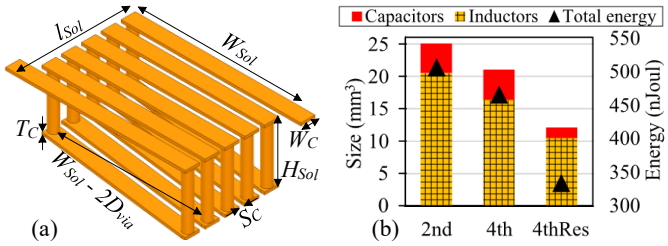


Fig. 9. (a) Solenoid inductor structure, (b) Comparison of the total filter size and predicted total peak energy.

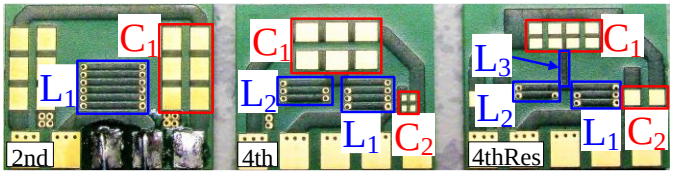


Fig. 10. Manufactured PCB inductors with capacitors land marked.

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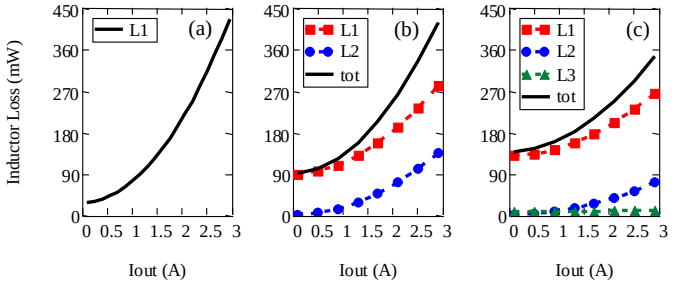


Fig. 11. Calculated inductor loss vs load at V_{IN} = 4.5 V: (a) 2nd order, (b) 4th order, (c) 4thRes.

VI. Prototype Converter Performance

The performance of the converter is investigated in this section with the PCB inductors of Section V, and a buck converter switching stage based on EPC2040 GaN FETs [21] for the high and low sides. The EPC2040 rating is 15 V and 3.4 A, and it has a 745 pC total gate charge, which makes it a suitable device for 20 MHz operation. The switches are driven by the Peregrine PE29102 gate driver, capable of 40 MHz [22]. The Pulse Width Modulation (PWM) input signal is generated using the DIGILENT Nexys3 FPGA development board, i.e. Xilinx Spartan-6 LX16 FPGA chip, and the output is fed into a high-frequency DC/DC converter test motherboard which includes variable resistors for dead-time tuning and output transient capacitors. The FPGA was programmed to generate a 20 MHz signal with the duty cycle adjusted externally. The prototype converter board is shown in Fig. 12.

TABLE V
On-board output capacitors

PN	C (µF)	ESR (mΩ)	ESL (nH)	SRF (MHz)
2x GRM188R61E106KA73	10	20	0.35	2.27
1x GCJ188R71E104KA12	0.1	60	0.3	21.3
4x GCM188R71C105KA49	1	30	0.37	8.7

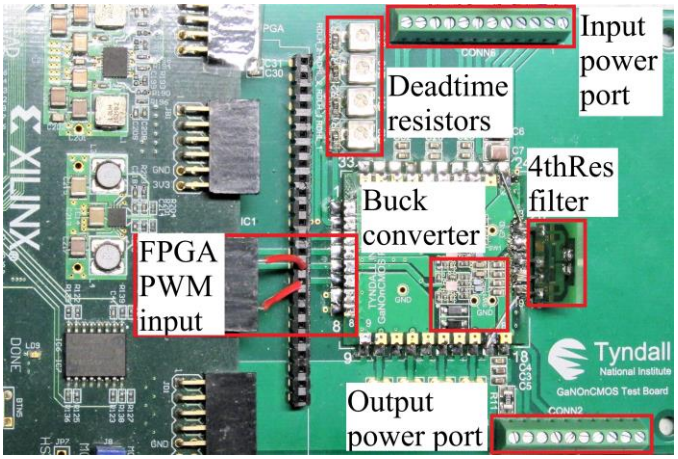


Fig. 12. Picture of the prototype converter connected to a test motherboard.

Details of the output capacitor impedances are given in Table V where parasitic ESR and ESL values were deduced from the datasheet. These values were chosen to enable testing of a range of multi-MHz DC/DC converters under steady-state and transient conditions, including the three converters investigated in this paper. Clearly, they are much larger than values chosen to satisfy steady-state ripple voltage in Section IV. However, as is typical in multi-MHz converters, the self-resonant frequency of the larger capacitors selected to satisfy transient conditions may be lower than the switching frequency. Therefore the smaller capacitors' contribution would be most significant at steady state. The operation of the prototype converter was verified, as shown in the testing waveforms in Fig. 13 with the 4thRes filter.



Fig. 13. Experimental waveforms with the 4thRes filter at V_{IN} = 4.5 V, V_{OUT} = 1.8 V, I_{OUT} = 2 A and F_{SW} = 20 MHz with 9-bit digital filter enabled, showing the high and low side FETs gate voltage (Vg_HS, Vg_LS), and switching node voltage (Vsw).

A. Steady-state performance

1) Output voltage ripple

The measured V_{OUT} waveform is shown in Fig. 14 at the nominal V_{IN} of 4.5 V, F_{SW} = 20 MHz and 2 A load. It was measured with only one oscilloscope probe attached to the board to reduce the probes' capacitance effect on the measurement accuracy. Fig. 14 shows that ΔV_{OUT} value is much lower than the initial specification of 90 mV for the three filters because the fixed output capacitors (in Table V) are much bigger in value than those chosen in Section IV. The measured ΔV_{OUT} value is the same with the 2nd and 4th order filters (9.5 mV), and it is slightly smaller with the 4thRes filter (7.9 mV).

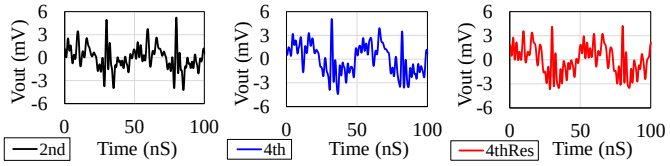


Fig. 14. Experimental waveforms of the output voltage (AC coupled) at V_{IN} = 4.5 V, V_{OUT} ≈ 1.8 V, I_{OUT} = 2 A and F_{SW} = 20 MHz.

2) Converter efficiency

Open-loop circuit simulation is carried out using LTspice with spice models of EPC2040 switches for the high and low sides and for the output capacitors of Table V. To account for parasitic packaging effects, the simulation model considers inductance and resistance values of 400 pH and 0.2 mΩ, respectively at each FET terminal. The gate signal dead time is 1.1 ns resulting in low-to-high and high-to-low dead-times of ~36 & 123 ps, respectively, between the FETs reaching the switching point voltage, i.e. 2.2 V approximately according to

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the datasheet [21]. The experimental dead-time was tuned to minimise the overshoot and undershoot in the switching voltage. Simulated and measured converter efficiencies vs output power at the nominal V_{IN} of 4.5 V are shown in Fig. 15(a) and (b), respectively. Fig. 15(b) includes a curve fit of the measurement data, similar to the method in [23]. The trends in measured efficiency correlate to a large extent with simulation results. Fig. 15(b) shows that the 4thRes filter has slightly lower efficiency than the 4th order filter below ~2.5 W. However, the fitted curves show that the full load (5.4 W) measured efficiency of the 4thRes filter is 3.6% and 3.7% higher than the 4th and 2nd order filters, respectively. Overall, the difference between measured and modelled absolute efficiency is likely because of factors not included in the model, such as PCB packaging interconnect impedances and eddy current effects due to proximity with air-core inductors operating at 20 MHz.

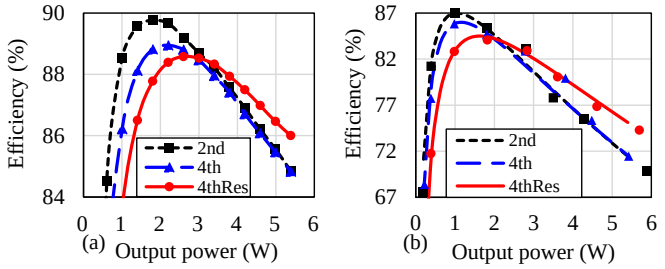


Fig. 15. Converter efficiency vs load at V_{IN} = 4.5 V, V_{OUT} = 1.8 V and F_{SW} = 20 MHz: (a) Spice simulation, (b) Measured data and its curve fitting.

B. *Converter loss breakdown*

The spice simulation loss breakdown at full load of 5.4 W and nominal V_{IN} of 4.5 V in Fig. 16 shows that the reduction in total loss of the 4thRes filter is mainly due to the reduction in inductor DC resistance loss and low side FET switching loss.

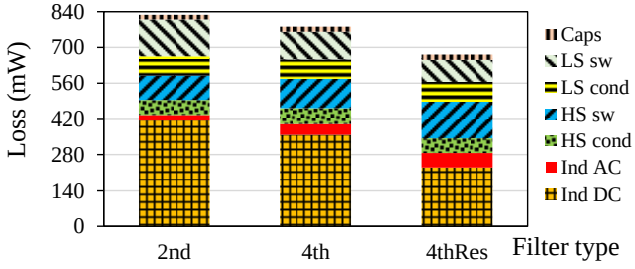


Fig. 16. Simulated full load loss breakdown at V_{IN} = 4.5 V.

C. *Open-loop load transient simulation:*

Spice simulation results of V_{OUT} open-loop instant load transition between 10% to 100% load in Fig. 17 at V_{IN} = 4.5 V shows that the 4thRes filter has a faster settling time during loading and unloading as an advantage of utilising less overall inductance. Future work will consider closed-loop performance for the 2nd order versus 4thRes filters.

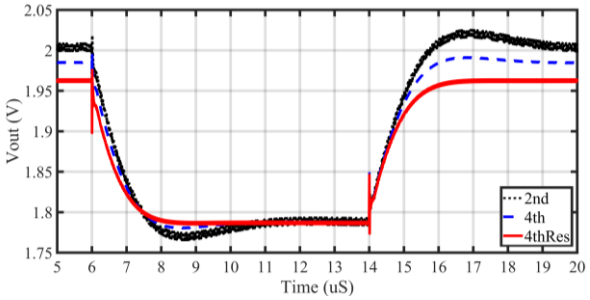


Fig. 17. Simulation load transient loading from 10% to 100% at V_{IN} = 4.5 V.

These results show the opportunity and potential of the 4thRes filter as it resulted in a significant reduction in the passive components' size and an increase in the full load efficiency without sacrificing the output ripple, besides having a faster settling time during load transients.

VII. Conclusion

This paper presents a novel selection procedure for passive components in a buck converter with Butterworth based 4th order and 4thRes filters. The main motivation is to reduce the size of the output filter, particularly the inductor. Previous studies investigated the resonance effect of the output filter of DC-DC converters provided by coupled inductors; however, a selection method for the filter components in terms of the converter specifications was not provided.

The presented study shows the potential of the 4thRes filter to reduce the size of the passive components over a wide duty cycle range. This is confirmed by PCB solenoid inductor structures based on standard PCB manufacturing process limitations. The outcomes of the design study show the potential of the 4thRes filter compared with a 2nd order filter. For the same output voltage ripple, it provides a 2.4% increase in inductor efficiency at full load, while requiring much smaller passives, i.e., 58% less inductance, 35% less inductor peak energy reflected in 48% less inductor volume. Besides, the 4thRes requires 45% less steady-state capacitance, which results in a 31% reduction in capacitor energy. The prototype converter with the 4thRes filter achieves 3.7% and 3.6% higher full load efficiency than the regular 2nd and 4th order filters, respectively. Moreover, the 4thRes filter simulation shows a faster settling time performance during load transients with the same output capacitance, compared with the 2nd and 4th order filters. These results show that the 4thRes filter can be a suitable replacement for the regular 2nd and 4th order filters in DC-DC converters to achieve smaller passive components, particularly for converters operating at higher load and fixed switching frequency.

References

[1] E. A. Burton *et al.*, "FIVR - Fully Integrated Voltage Regulators on 4th Generation Intel® Core™ SoCs," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 432–439.

[2] D. Hou, F. C. Lee, and Q. Li, "Very High Frequency Integrated Voltage Regulator for Small Portable Devices," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–7.

[3] Y. Kandeel and M. Duffy, "Comparison of Coupled vs. Non-Coupled Microfabricated Inductors in 2W 20MHz Interleaved Buck Converter," in

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IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 2638–2645.

[4] S. Nagar, F. Al-Zahara Said, M. Orabi, and A. Abou-Alfotouh, "Design of High Performance Point of Load Converters with Ultra-Low Output Voltage Ripple," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2010, pp. 4145–4150.

[5] R. Künzi, "Passive Power Filters," in *Proceedings of the CAS-CERN Accelerator School: Power Converters*, 2015, vol. 003, pp. 265–289.

[6] J. Sebastian, P. Fernandez-Miaja, F. J. Ortega-Gonzalez, M. Patino, and M. Rodrıguez, "Design of a Two-Phase Buck Converter With Fourth-Order Output Filter for Envelope Amplifiers of Limited Bandwidth," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5933–5948, 2014.

[7] N. Tang *et al.*, "Fully Integrated Buck Converter With Fourth-Order Low-Pass Filter," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3700–3707, 2017.

[8] R. S. Balog and P. T. Krein, "Coupled-Inductor Filter: A Basic Filter Building Block," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 537–546, 2013.

[9] S. C. Kim, K. M. Ha, and J. Y. Huang, "High accuracy and high stability magnet power supply by four-phase buck type DC/DC converter," in *7th Internatonal Conference on Power Electronics (ICPE'07)*, 2007, pp. 232–237.

[10] M. C. W. Høyerby and M. A. E. Andersen, "Ultrafast Tracking Power Supply with Fourth-Order Output Filter and Fixed-Frequency Hysteretic Control," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2387–2398, 2008.

[11] S. Dam and P. Mandal, "An Integrated DC–DC Boost Converter Having Low-Output Ripple Suitable for Analog Applications," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5108–5117, Jun. 2018.

[12] J. T. Doyle, J. C. Stiff, S. Kulkarni, and A. Yildiz, "A Low Cost 100 MHz 2-Stage PSiP and Evolution to a Co-Packaged/Fully-Integrated Voltage Regulator for SoC Power Delivery," in *IEEE Custom Integrated Circuits Conference (CICC)*, 2019.

[13] Y. Kandeel and M. Duffy, "Design of 4th Order Resonance Filter for 5.4 W 20 MHz Buck Converter with PCB Integrated Inductor," in *IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020.

[14] R. Schaumann and M. E. Van Valkenburg, *Design of Analog Filters*. Oxford University Press, 2001.

[15] C. Parisi, "Multiphase Buck Design From Start to Finish (Part 1)," 2021. [Online]. Available: https://www.ti.com/lit/pdf/slva882. [Accessed: 01-Jul-2021].

[16] P. Zou, Q. Xie, W. Song, Q. Jiang, Y. Lu, and B. Huang, "Powering 5G Era Computing Platforms - The Road toward Integrated Power Delivery," in *International Symposium on Power Semiconductor Devices and ICs*, 2019, pp. 1–6.

[17] Institute of Printed Circuits (IPC), "Generic Standard on Printed Board Design, IPC-2221A," 2003.

[18] Institute of Printed Circuits (IPC), "Standard for Determining Current Carrying Capacity in Printed Board Design, IPC-2152," 2009.

[19] P. L. Dowell, "Effects of eddy currents in transformer windings," *Proc. Inst. Electr. Eng.*, vol. 113, no. 8, p. 1387, 1966.

[20] T. M. Andersen, C. M. Zingerli, F. Krismer, J. W. Kolar, N. Wang, and C. Mathuna, "Modeling and Pareto Optimization of Microfabricated Inductors for Power Supply on Chip," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4422–4430, 2013.

[21] EPC Co., "EPC2040-Enhancement Mode Power Transistor," *Datasheet*, 2019. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2040_datasheet.pdf. [Accessed: 21-Jan-2020].

[22] PSemi Co., "PE29102 - GaN FET Drivers," *Datasheet*. [Online]. Available: https://www.psemi.com/products/gan-fet-driver/pe29102. [Accessed: 21-Jan-2020].

[23] V. Vorpérian, "Simple Efficiency Formula for Regulated DC-to-DC Converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 46, no. 4, pp. 2123–2131, 2010.

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