Electrically active defects in Al_2O_3-InGaAs MOS stacks at cryogenic temperatures

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***Abstract*— The effects of defects in $In_{0.47}Ga_{0.53}As/Al_2O_3$/Ni metal-oxide-semiconductor (MOS) stacks at cryogenic temperatures are investigated. The MOS stacks exhibit a hysteresis in the capacitance-voltage (CV) curve, both at room temperature and at 100K, indicating the presence of effective charge capture/emission dynamics in the oxide even at cryogenic temperatures. Border traps (BTs) in the Al_2O_3 close to the $In_{0.47}Ga_{0.53}As/Al_2O_3$ interface are recognized as the best candidate for explaining the experimental CV. The hysteresis shape and its temperature dependence are used to profile the oxide defects' properties, which allow correctly predicting the MOS stacks CV and conductance-voltage (GV) frequency dispersions and gaining insights on the hysteresis dynamics.**

***Keywords*— Al_2O_3, capacitance, cryogenic, hysteresis, InGaAs**

I. Introduction

Low temperature electronics is an extremely relevant topic in growing fields, such as quantum computing [1-3] and space exploration [4-6]. Even in classical applications, low temperature operation is used to enhance the devices' performance and reliability [7-10]. The study of electron-defect interactions remains critical at cryogenic temperatures as quantum effects prevent the complete freeze out of defect-related charge trapping phenomena, along with the related reliability issues and degradation processes [11,12]. Thus, the accurate characterization of defects remains of paramount importance even for low temperature applications.

In this work, we investigate the effects of defects in $In_{0.47}Ga_{0.53}As/Al_2O_3$/Ni MOS stacks down to cryogenic temperatures (i.e. 100 K). The devices exhibit a hysteresis of the CV curve, associated with charge trapping in the oxide. The hysteresis is retained at 100K, providing experimental evidence of effective charge capture/emission dynamics even at very low temperature. The hysteresis is still present at 10 K (not shown), regardless of the doping. First, a comprehensive sensitivity analysis is carried out, determining the effects of the traps space-energy position on the CV hysteresis and identifying the BTs as best candidate for explaining the hysteresis origin and temperature dependence. We therefore use accurate physics-based simulations to reproduce the experimental data, profiling the traps distribution within the oxide, finding agreement with similar MOS systems. The extracted trap distributions allow reproducing the frequency dependent CV and GV of all the considered MOS stacks and gaining insights on hysteresis dynamics.

II. Discussion

$In_{0.47}Ga_{0.53}As/Al_2O_3$/Ni MOS stacks, both n-doped (S at 4×10^{17} cm^{-3}) and p-doped (Zn at 4×10^{17} cm^{-3}), were fabricated as reported in [13] and characterized in a cryogenic probe station. Simulations were performed using the commercial device simulation software Ginestra® [14], in which the carriers' transport, the device electrostatics, the charge trapping/emission dynamics to/from defects in the dielectric, and the related temperature dependencies are self-consistently calculated. Most importantly, the charge trapping phenomena is modeled according to the multi-phonon trap-assisted tunneling theory [15], accounting for electron-phonon coupling and the atomic lattice relaxation associated with the charge trapping. This allows accurately model the charge trapping dynamics in the high-k materials [16] and accounting for important low temperature quantum phenomena, such as the nuclear tunneling [15,17].

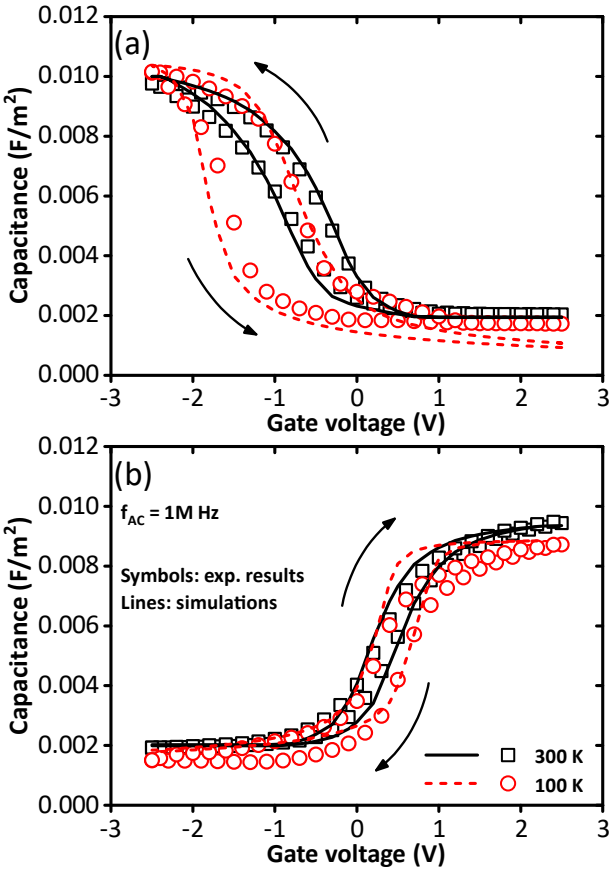

Fig. 1. Experimental (symbols) and simulated (lines) 1MHz CV hysteresis characterization of $In_{0.47}Ga_{0.53}As/Al_2O_3$/Ni MOS stacks for (a) p-InGaAs and (b) n-InGaAs substrate. The hysteresis is exhibited by all the devices and is retained at cryogenic temperatures. The arrows show the bias ramp direction.

Fig. 1 shows the sweep CV curve at 1MHz for the n-doped (a) and p-doped (b) stacks. Both devices exhibit a clear hysteresis window, which could be ascribed to charge

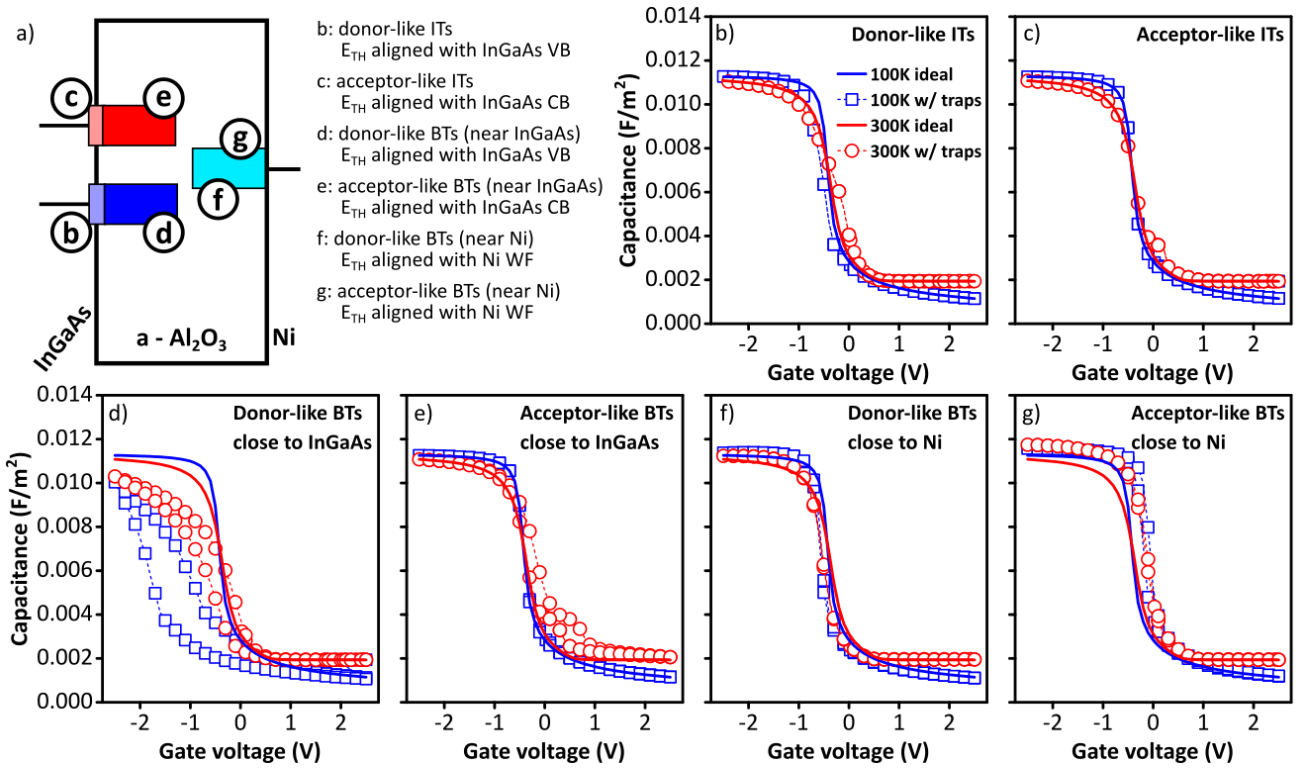

Fig. 3. Sensitivity analysis of the different traps on the CV hysteresis of a p-doped $In_{0.47}Ga_{0.53}As/Al_2O_3$/Ni MOS stack. (a) diagram of the considered defects' location. The letters associated to the different traps correspond to the respective subfigure. The considered trap distributions are gaussian with peak density of 10^{20} cm^{-3} (i.e. 5×10^{12} cm^{-2} for the ITs). (b) donor-like ITs at the $In_{0.47}Ga_{0.53}As/Al_2O_3$ interface aligned with the semiconductor valence band; (c) acceptor-like ITs at the $In_{0.47}Ga_{0.53}As/Al_2O_3$ interface aligned with the semiconductor conduction band; (d) donor-like BTs close to the $In_{0.47}Ga_{0.53}As$ valence band energy; (e) acceptor-like BTs close to the $In_{0.47}Ga_{0.53}As$ conduction band energy; (f) donor-like BTs close to the Ni top electrode; (g) acceptor-like BTs close to the Ni top electrode. Figures (b)-(g) show the effect of the traps on the transient CV characteristic at 100K and 300K. Only the border traps close to the semiconductor (d,e) show a CV hysteresis compatible with the experimental results of Fig. 1.

trapping at the semiconductor-oxide interface (interface traps) and in the oxide bulk, but close to the electrodes (border traps). Noticeably, the CV hysteresis is retained at 100K, although exhibiting a voltage shift towards the stack accumulation region, an increased window width and slope. This strongly suggests that the related defects are still electrically active even at low temperatures. Thus, the negative effects determined by the oxide defects (e.g. lower mobility, V_T shift, increased leakage) cannot be mitigated by lowering the device working temperature, highlighting the importance of their accurate characterization.

The qualitative energy-space position of the traps causing the experimental CV hysteresis are identified by a thorough sensitivity analysis of the different traps that could be taking part in the process, shown in Fig. 2(a). In this study, we investigated the contribution to the CV hysteresis of interface traps (ITs) at the $In_{0.47}Ga_{0.53}As/Al_2O_3$ interface (b and c), border traps (BTs) close to the $In_{0.47}Ga_{0.53}As$ electrode (d and e), and BTs close to the Ni electrode (f and g). Both donor-like (1/0) and acceptor-like (0/-1) traps are considered. Simulating the transient CV for each of the considered trap locations, depicted in Fig.2(b-g) for a p-doped substrate stack, allows determining the respective contribution to the hysteresis. It is worth noting that the simulations of n-doped substrate stacks are qualitatively similar (not shown for brevity). Regardless of the substrate doping, only the BTs close to the $In_{0.47}Ga_{0.53}As/Al_2O_3$ interface, both the donor-like ones and acceptor-like ones, allow reproducing a hysteretic CV characteristic compatible with the experimental one, Fig. 2(d-e). Noticeably, the hysteresis temperature dependence is also well reproduced, showing a widening of the hysteresis window and a voltage shift at 100K. The main effect of the ITs, Fig. 2(b-c), is the well-known distortion of the CV characteristics, increasing the depletion region CV spread [18]. Finally, the BTs close to the top electrode, Fig. 2(f-g), affect the oxide electrostatics modulating the electrode effective work function, thus causing a small voltage shift of the CV characteristics. Upon close inspection, a small, temperature dependent hysteresis can be detected in Fig. 2(g), but its characteristics are not consistent with the experimental one. The BTs near the $In_{0.47}Ga_{0.53}As/Al_2O_3$ interface are thus identified as the best candidate for the origin of the experimental CV hysteresis.

The shape and the temperature dependence of the CV hysteresis was used for quantitatively profiling the BTs defects' energy-space distribution within the oxide. For this purpose, we reproduced the experimental data, Fig. 1, extracting as a result the distribution shown in Fig. 3. Simulation results show that reproducing the experimental CV data requires the introduction of a 3nm region in the oxide with donor-like and acceptors-like BTs at the $In_{0.47}Ga_{0.53}As/Al_2O_3$ interface. The former, characterized by a higher concentration (peak density of 2×10^{20} cm^{-3}) are almost aligned with the $In_{0.47}Ga_{0.53}As$ valence band, being gaussian-distributed with a thermal ionization energy (E_{TH}) mean of 3.34 eV (0.2 eV standard deviation). The latter are less dense (peak density of 8×10^{19} cm^{-3}) and spread above the $In_{0.47}Ga_{0.53}As$ conduction band, being also gaussian-distributed with E_{TH} mean of 2.1 eV (0.2 eV standard deviation).

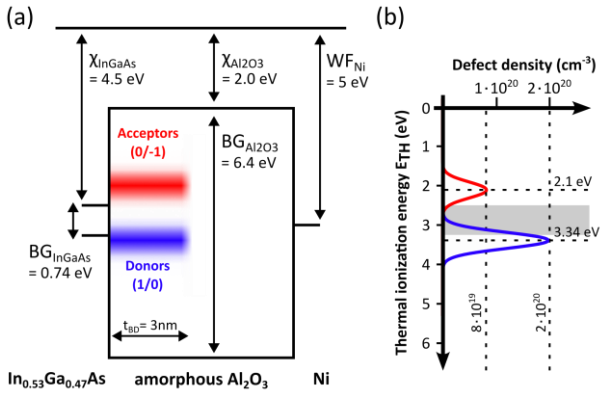

Fig. 3. (a) Band diagram of the considered $In_{0.47}Ga_{0.53}As/Al_2O_3/Ni$ MOS stack. Acceptors-like and donor-like border traps are shown in red and blue, respectively; (b) the energy-density distribution of the border traps. The $In_{0.47}Ga_{0.53}As$ band gap is represented by the shaded area for reference.

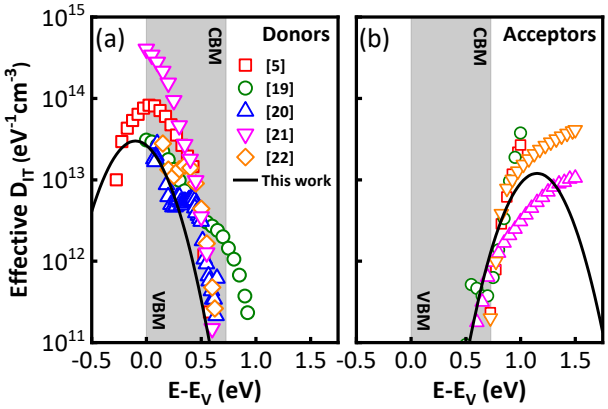

Fig. 4. Comparison between the effective interface traps density corresponding to the extracted defect distributions shown in Fig. 2 (solid line) and the D_{IT} reported in literature for $In_{0.47}Ga_{0.53}As/Al_2O_3$ systems (symbols) for (a) donor-like traps and (b) acceptor-like traps. Energies are referred to the $In_{0.47}Ga_{0.53}As$ valence band maximum (VBM).

The extracted defect distributions, extending deep into the oxide, cannot be directly compared with the ITs density typically extracted with conventional techniques. An effective IT distribution (D_{IT}) corresponding to the extracted distributions can be calculated as in [5], projecting the electrostatic effect of the traps in the oxide bulk to the $In_{0.47}Ga_{0.53}As/Al_2O_3$ interface. The resulting effective D_{IT} for the donors and acceptors trap distributions, shown in Fig. 4, are in very good agreement with previous works [5,19-22] on $In_{0.47}Ga_{0.53}As/Al_2O_3$ stacks. This suggests that the non-ideal distortion/spreading of the CV curves, usually ascribed to ITs at the $In_{0.47}Ga_{0.53}As/Al_2O_3$ interface only, might be instead produced by bulk BTs. The nature of the identified traps cannot be easily ascertained. Interestingly, the extracted energy levels are not compatible with the DFT calculations results for intrinsic Al_2O_3 defects [23,24], finding positively (i.e. potentially donor-like) and negatively (i.e. potentially acceptor-like) charged defects aligned with the $In_{0.47}Ga_{0.53}As$ conduction band and valence band, respectively. The extracted trap levels are also in contrast with the experimental results on $TaN/Al_2O_3/TaN$ stacks [25,26], identifying positive traps with E_{TH} spread around 2.55 eV. This suggests the profiled BTs are a peculiar characteristic of the $In_{0.47}Ga_{0.53}As/Al_2O_3$ interface, requiring further investigation.

To verify the quality and significance of the extracted defects' properties and distributions, we used the results in Fig. 3 to simulate the frequency dependent CV and GV curves measured on the considered MOS stacks at room temperature (295 K). The experimental multifrequency CV and GV, shown in Fig. 5, exhibit a clearly visible frequency dispersion regardless of the substrate doping. Notice that the CV frequency dispersion in the inversion region (i.e. positive and negative voltage for the p-doped and the n-doped semiconductor, respectively), corresponding to the dispersion and high frequency saturation of the GV curves, is determined by the generation/recombination (R/G) of minority carriers in the semiconductor, which is effectively modeled according to the Shockley-Read-Hall (SRH) theory [27].

The simulations of the extracted traps distributions (thus without including SRH G/R processes) allow very well reproducing both the CVs and GVs accumulation frequency dispersion. Further inspection allowed recognizing the BTs aligned with the majority carriers' band (i.e. acceptor-like traps in n-doped stacks and vice versa) as the main origin of the accumulation dispersion. The BTs aligned with the minority carriers' band also contribute to the CV characteristic by introducing the peaks exhibited at the inversion/depletion boundary. These peaks appear, however, smaller than the experimental data show. A comprehensive simulation including the SRH G/R processes in the $In_{0.47}Ga_{0.53}As$ allows capturing all the features exhibited by the experimental CV

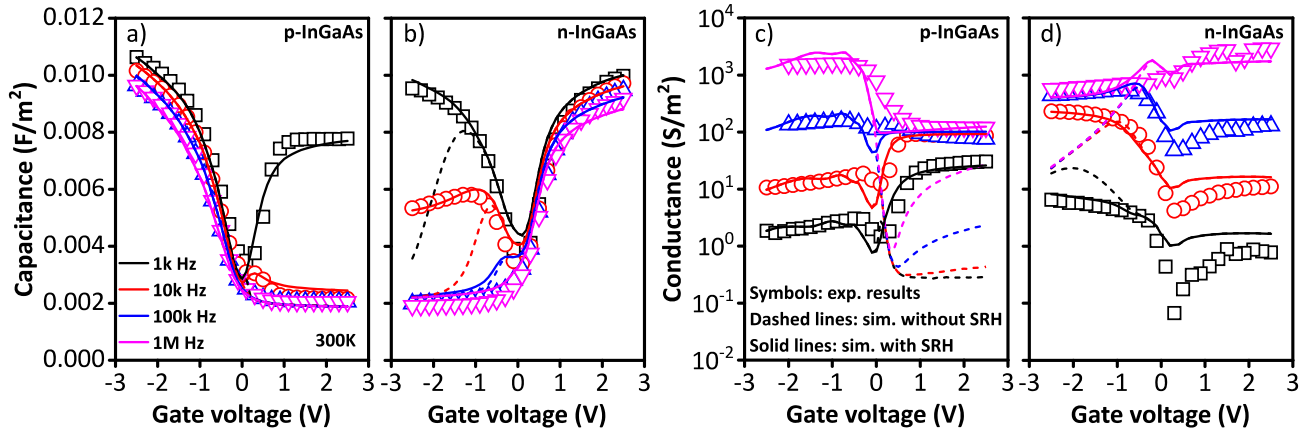

Fig. 5. Comparison of the room temperature experimental frequency dispersion in the CV (a,b) and GV (c,d) curves (symbols) of the p-doped and n-doped stacks with the simulations (lines) including the extracted trap space-energy distribution shown in Fig. 3. The simulations not accounting for the SRH G/R process (dashed lines) correctly reproduce only the accumulation frequency spread, missing the inversion frequency spread and peaks. Accounting for the SRH G/R process (solid lines) allows correctly reproducing the full CV and GV characteristics.

and GV curves. For sake of simplicity, we introduced recombination centers in the $In_{0.47}Ga_{0.53}As$ layer at the intrinsic Fermi level (i.e. the most efficient level for the G/R process), with a density of 6×10^{17} cm^{-3} and 2.5×10^{18} cm^{-3} for the p-doped and the n-doped semiconductor, respectively. Accounting for the SRH G/R process introduces the inversion frequency dispersion and more accurately reproducing the CV peaks. This confirms that the extracted traps distributions are correct, and thus the temperature dependent CV hysteresis can be effectively used for profiling the BTs in MOS systems.

Insights on the hysteresis origin and its temperature dependence were obtained from the MOS stacks simulations of Fig. 1. First, the CV hysteresis is mainly determined by the BTs aligned with the stacks' majority carrier band, with their contribution extending along the whole accumulation region. The BTs aligned with the stacks' minority carrier band provide a smaller contribution, mostly limited to the depletion region. At low temperature the carriers' density is greatly reduced in both the $In_{0.47}Ga_{0.53}As$ bands, affecting the hysteresis shape. At 100K, the majority carriers' density still allows for a clearly visible hysteresis. Conversely, the minority carriers' density is severely limited, suppressing their contribution to the hysteresis, thus contributing to the steepening of the hysteresis window and an apparent voltage shift towards the accumulation region observed in Fig. 1. Finally, the widening of the hysteresis window at low temperature is ascribed to the slower capture/emission dynamics of the oxide's traps, hampering the charge recovery process within the oxide. This bottleneck, combined with a large defect density to recover, results in the exceptionally large hysteresis window exhibited by the p-doped stack (Fig. 1b).

III. Conclusion

The presented study highlights the importance of the carrier/trap interaction even at extremely low temperatures. We used accurate physics-based device simulations to investigate and reproduce experimental CV hysteresis measured on $In_{0.47}Ga_{0.53}As/Al_2O_3/Ni$ MOS stacks, exhibiting a hysteresis in the CV curve persisting down to cryogenic temperatures. Border traps extending in the Al_2O_3 layer and aligned with the $In_{0.47}Ga_{0.53}As$ conduction and valence bands were identified as the origin of the CV hysteresis and profiled. The extracted trap distributions also correctly predicted the CV and GV frequency dispersion and allowed further investigating and understanding the CV hysteresis temperature dependence.

Acknowledgment

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