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Determination of Physical Parameters for $HfO_2/SiO_x/TiN$ MOSFET Gate Stacks by Electrical Characterization and Reverse Modeling

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Abstract – In this paper we present the results of a combined electrical and modeling study to determine the tunneling electron effective mass and electron affinity for HfO_2. Experimental capacitance-voltage (C-V) and current-voltage (I-V) characteristics are presented for HfO_2 films deposited on Si(100) substrates by atomic layer deposition (ALD) and electron beam evaporation (e-beam), with equivalent oxide thickness in the range 10 and 12.5Å. We extend on previous studies by applying a self-consistent 1D-Schrödinger-Poisson solver to the entire gate stack, including the inter-layer SiO_x region *and* to the adjacent substrate for non-local barrier tunneling self-consistently linked to the quantum-drift-diffusion transport model. The reverse modeling is applied to the correlated gate and drain currents in long channel MOSFET structures. Values of 0.11 ± (0.03) m_o and 2.0 ± (0.25) eV were determined for the HfO_2 electron effective mass and electron affinity.

Index Terms – High-*k* gate stacks, HfO_2, reverse modeling, tunneling, electron effective mass, electron affinity.

I. INTRODUCTION

Based on over ten years of research and development the use of high dielectric constant materials, such as HfO_2, have reached the stage where they are now incorporated into the gate stack of silicon based MOSFET's. The HfO_2 insulator is used in conjunction with metal gate electrodes and a thin (typically ~ 10Å) interface silicon oxide layer (SiO_x). Modeling the leakage currents in metal-gate/HfO_2/SiO_x/Si structures requires knowledge of the dominant conduction mechanism and physical parameters of the HfO_2 thin film such as the effective mass of electrons in the HfO_2 energy gap (m_{HfO2}) and the electron affinity of the HfO_2 (χ_{HfO2}). This is of technological importance to allow accurate simulations of the gate leakage current for existing and scaled HfO_2 based gate stacks over a typical bias range from 0 to 1 volt.

A range of publications have examined tunneling in heavily doped polysilicon and metal gate HfO_2/SiO_x/Si structures, including determination of m_{HfO2} and χ_{HfO2} [1-4]. A range of values for m_{HfO2} are reported varying from $0.4m_o$ to $0.08m_o$. The reported values of χ_{HfO2} range from 1.75eV to 2.82eV. Based on the spread of the results it is evident that there is still scope for further experimental analysis and modeling to establish if m_{HfO2} and χ_{HfO2} converge to values which are not varying with the deposition method or gate material. In this paper, we extend on previous reports to examine metal-gate/HfO_2/SiO_x/Si structures formed by electron beam evaporation and ALD. The HfO_2 and silicon oxide interface layer thicknesses are determined by transmission electron microscopy. In the case of the ALD deposited HfO_2 gate stacks, full MOSFETs were available for the C-V and I-V analysis of the $TiN/HfO_2/SiO_x$/Si structures. The availability of the full MOSFET devices allows the simulations to be applied to the condition of tunneling of electrons from the channel inversion region. Moreover, the simultaneous modeling of the gate tunneling current and the drain current (which exhibits two to three sign changes as a function of the gate voltage) provides additional experimental data for narrowing the uncertainty of m_{HfO2} and χ_{HfO2}, as there is a strong correlation between drain and gate currents in a long-channel MOSFET.

In contrast to previous modeling work, we apply a self-consistent 1D-Schrödinger-Poisson solver to the entire gate stack, including the inter-layer SiO_x region, *and* to the adjacent substrate, which goes beyond the WKB approximation and automatically includes quantization effects in the channel. The direct tunnel current in the gate stack is self-consistently coupled to the drift-diffusion current which results from solving the continuity equations including all relevant physical effects, like mobility degradation, fixed oxide charges, and interface traps. [5].

II. EXPERIMENTAL SAMPLES

In the case of the e-beam deposited films the HfO_2 layers are formed on *n* type silicon (100) with a resistivity of 10-20 Ωcm. The Si wafers undergo a standard chemical clean and HF (10:1 DI water / HF for 10 seconds), to result in an H terminated silicon surface. The HfO_2 film (~35Å) was deposited at 150°C from 3-5mm monoclinic HfO_2 pellets of 99.99% purity. MOS capacitors of various areas were formed using photolithography and lift-off process. The metal gate consists of 300nm of Ni deposited ex-situ by e-beam, followed by a final forming gas anneal ($5\%H_2/95\%N_2$) at 400°C for 30 minutes, (referred to subsequently as the e-beam sample).

For the ALD deposited films, the HfO_2 layers with nominal thickness of 16, 20, 24 and 30 Å are formed on *n* type silicon (100) with a ~10Å interface SiO_x layer. The gate electrode is 100 Å TiN. Isolated gate *n* channel MOSFETs with an area of 10 x 10 μm^2 have been used as test devices. Physical and extracted parameters for the devices are presented in Table 1. Further details relating to the devices used in the study can be found in [6].

Table I:

Summary of Physical and Extracted Parameters for the ALD HfO_2/TiN MOSFETs used in the study

Wafer	A	B	C	D
t-HfO_2 [Å]	16	20	24	30
t-SiO_x [Å]	10	10	10	10
$C_{ox\ eff}$ [F/cm^2]	2.43×10^{-6}	2.35×10^{-6}	2.25×10^{-6}	2.16×10^{-6}
V_{FB} [V]	-0.49	-0.51	-0.58	-0.6
E_{OT} [Å]	10.6	11.4	12.1	12.5
Na [x 10^{17} /cm^3]	3	3	3	3
μ_{peak} [cm^2/V.s]	225	212	195	178

Current-voltage (I-V) measurements were performed with a HP4156A Precision semiconductor parameter analyzer and capacitance voltage (C-V) measurements were measured using a HP 4284A precision LCR meter. The measurements were performed on-wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry air environment (dew point ~ -70°C). All measurements were recorded at room temperature, (referred to subsequently as samples A, B C or D).

III. SIMULATION MODEL FOR C-V AND I-V RESPONSE

1D Schrödinger equations are solved along straight lines connecting the channel to the gate contact [7]. The results are self-consistently incorporated into a 2D drift-diffusion simulator [5]. A special-purpose grid has to be generated for the solution of the 1D Schrödinger-Poisson system. It consists of straight lines that are attached to a semiconductor vertex and connect this vertex to the closest grid point on the gate contact. In addition, points not directly situated under the gate can be connected to the gate corners by defining a maximum angle measured to the normal of the gate contact line. Two length parameters serve to include regions below and above the stack. Hence, the transmission probability can be computed not only for the stack barrier alone, but also for a possible potential barrier in the substrate.

Based on interpolation schemes all data, as well as the refinement of the initial mesh, are transferred to the special-purpose grid. The 1D Schrödinger equation is solved in the (one-band) effective mass approximation (EMA) using the scattering matrix approach (SMA) [8]. Denoting coordinates on the lines of the special-purpose grid by *u* or *r* (origin at the metal contact), the electron current density due to direct gate tunneling (by conduction band electrons only) can be written as [5,9];

$$j_n = -\frac{g_n A_0 T}{k_B}\int_{0^-}^{\infty} du\, \mathcal{T}_n\left[u, 0^-, E_c(u)\right]\left|\frac{dE_c}{du}(u)\right|\Theta\left[\frac{dE_c}{du}(u)\right]\times \\ \times \ln\left\{\frac{\exp\left[\frac{E_{F,n}(u)-E_c(u)}{k_B T}\right]+1}{\exp\left[\frac{E_{F,n}(0^-)-E_c(u)}{k_B T}\right]+1}\right\}. \quad (1)$$

Here, $A_0 = 4\pi m_0 k_B^2 q/h^3$ is the Richardson constant for free electrons, T denotes the temperature (drift-diffusion model, no carrier heating), k_B the Boltzmann constant, $E_c(u)$ the position-dependent conduction band edge, $E_{F,n}(u)$ the quasi-Fermi energy, and $\boldsymbol{T}_n$ the tunneling probability resulting from the SMA solution of the 1D Schrödinger equation. The parameter g_n can be used to change the effective DOS mass in the Richardson constant. For tunneling across a (100)-oriented interface, a reasonable choice is $g_n = 2m_t/m_0$ for the valley pair perpendicular to the interface and $g_n = 4(m_t\, m_l)^{1/2}/m_0$ for the two valley pairs parallel to the interface. Separate simulations of the current were performed, to account for the changes of the Si effective mass which enter the transmission probability $\boldsymbol{T}_n$.

The simulated CV characteristics of the e-beam HfO_2 sample are obtained from quasi-static QV curves (charge-voltage) that result from solving the Schrödinger-Poisson system and finally differentiating them. Acceptor-like interface traps between substrate and inter layer can be included.

IV. EXPERIMENTAL RESULTS AND SIMULATIONS

Figure 1 shows the measured and simulated C-V response for the e-beam HfO_2 sample, for a

measurement frequency of 1 kHz. The sample exhibits a low frequency response in inversion as a result of peripheral inversion around the capacitors area defined by the Ni gate. This allows a fit of the simulated QSCV to the measured data across the full range from strong accumulation to strong inversion. The corresponding TEM for the e-beam sample is shown in the inset.

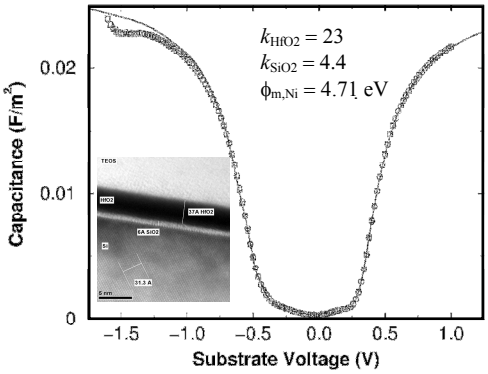


Figure 1. The measured (circles) and simulated (line) C-V response for the e-beam HfO_2 sample. The measured data was recorded at an ac signal frequency of 1kHz. Inset: High resolution cross section TEM of sample showing an interfacial SiO_x thickness of 6 Å and an HfO_2 thickness of 37 Å. The equivalent oxide thickness is 10.9±0.1 Å.

The simulated C-V is in very good agreement with the experimental data over the full bias range from strong accumulation (-1.25V) to strong inversion (1.0V), using the physical thicknesses available from the TEM. Interface trap density following the forming gas anneal are in the range 2-3x10^{11} cm^2 near the mid gap energy. They do not have a significant influence on the C-V response and are not considered further in this paper. The fit of the simulation data to the C-V yields dielectric constants of 4.4 and 23 for the SiO_x interlayer and the HfO_2 respectively. The effective Ni gate work function, which includes the effect of any fixed oxide charges, is 4.71 eV.

The experimental (circles) and simulated (lines) I-V characteristics are presented in Figure 2. The simulation is for direct gate tunneling by conduction band electrons only. An excellent fit to the magnitude and gradient of the measured data is obtained for a substrate voltage (V_s) < -0.7 volts, for: m_{HfO2} = 0.11m_o (0.135m_o), χ_{HfO2}= 1.75 eV (2.0 eV), and $m_{SiOx=}$ 0.5m_o, χ_{SiOx}= 1.4 eV. (The SiO_x electron affinity χ_{SiOx} is reduced from the typical SiO_2 value of 0.9eV as the interface silicon oxide layer is sub-stoichiometric).

From Figure 2 it is evident that while direct conduction band tunneling is consistent with the measured data at V_s < -0.7, for lower absolute values of V_s an additional (temperature dependent) conduction mechanism is present. The leakage current density at V_{fb}+1V into accumulation (-1.3 V) is 1x10^{-3} A/cm^2.

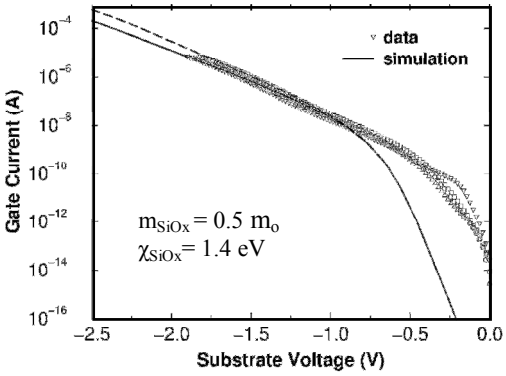


Figure 2. Measured and simulated I-V characteristics for the e-beam HfO_2 sample. The measured current is for various sites across the wafer. The Ni gate area is 55µm x 55 µm. Simulation parameters for SiO_x are inset. Solid curve: m_{HfO2} = 0.11 m_o, χ_{HfO2}= 1.75 eV, dashed curve: m_{HfO2} = 0.135 m_o, χ_{HfO2}= 2.0 eV.

In the case of the ALD deposited films the HfO_2 layers (samples A, B, C and D), the availability of MOSFET structures allows the simultaneous fitting of the coupled gate (I_g) and drain (I_d) currents over a range of HfO_2 film thicknesses. Measured and simulated gate and drain currents are presented in Figures 3a) b) and c).[1] The drain current is the current measured at the drain terminal without gate current partition correction. As a consequence, the measured drain current is influenced by the gate leakage current density, which is evident from the changes in the sign of the drain current with increasing gate voltage. Relatively large devices (10µmx10µm) were deliberately selected so that I_g exceeds I_d at some gate bias within the range 0 to 1.5 V. The gate voltage corresponding to the drain current sign changes provides additional experimental data for the reverse modeling process. The fits to the experimental data are achieved using a fixed parameter set: m_{HfO2} = 0.08mo, χ_{HfO2}= 1.75 eV, $m_{SiOx=}$ 0.5mo, and χ_{SiOx}= 1.4 eV. To achieve the accurate fit to the measured data over the 3 HfO_2 thicknesses, it was required to modify the interface layer thickness, from 9.2 Å (samples B and C), to 7.7Å (sample D), possibly indicating a modification of the interlayer with increasing HfO_2 film thickness.

Based on a series of simulations where: (i) the interface SiO_x layer is fixed and HfO_2 thickness is varied, (ii) the HfO_2 thickness is fixed and the interface SiO_x layer is varied (as in Figure 3) and (iii) both HfO_2 and SiO_x thicknesses are fixed and m_{HfO2} and χ_{HfO2} are varied, the limits for m_{HfO2} and χ_{HfO2} of

[1] Accurate simulations below a gate voltage of 0.6 volts are not possible, as this requires accurate details of the doping profile under the gate corners.

0.11 ± (0.03) m_o and 2.0 ± (0.25) eV are determined. The χ_{HfO2} corresponds to conduction band offsets from the silicon conduction band to the HfO_2 conduction band of ΔE_c = 2.05± (0.25) eV, from the relationship, $\chi_{Si} = \chi_{HfO2} + \Delta E_c$.

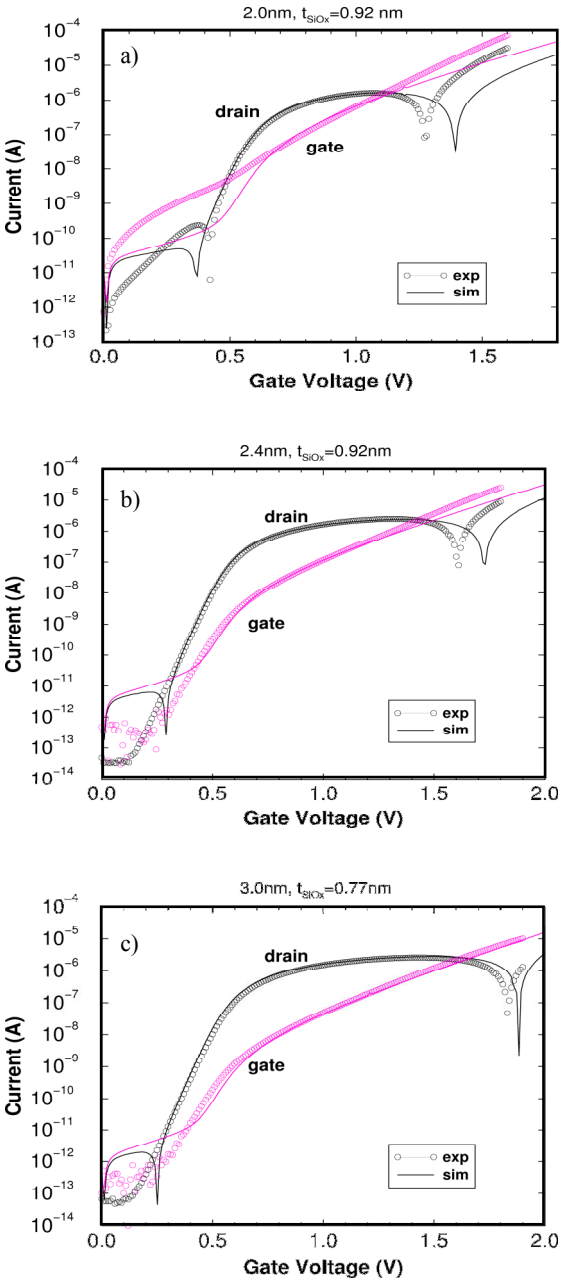


Figure 3. Measured (circles) and simulated (solid) gate and drain currents with V_{ds}=10mV, for (a) sample B 20 Å HfO_2, (b) sample C 24 Å HfO_2, and (c) sample D 30 Å HfO_2. The fit to the measured data for all three samples is obtained for the following parameters: m_{HfO2} = 0.08m_o, χ_{HfO2}= 1.75 eV, $m_{SiOx=}$ 0.5m_o, and χ_{SiOx}= 1.4 eV. The TiN work function, $\phi_{m,TiN,}$ was in the range: 4.58 to 4.63 eV.

V. CONCLUSIONS

Experimental results and physically based modeling of the tunneling currents have been presented for ALD and e-beam deposited metal-gate/HfO_2/SiO_x/Si structures. We have extended on previous studies by applying a self-consistent 1D-Schrödinger-Poisson solver to the entire gate stack, including the inter-layer SiO_x region, *and* to the adjacent substrate, as well as extending the modeling of the gate current to the correlated drain current in full TiN/HfO_2 MOSFETs. The electron effective mass m_{HfO2} and electron affinity χ_{HfO2} of HfO_2 are determined to be within the range 0.11 ± (0.03) m_o and 2.0 ± (0.25) eV for e-beam and ALD deposited HfO_2 films.

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