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Impact of Forming Gas Annealing on the Performance of Surface-Channel $In_{0.53}Ga_{0.47}As$ MOSFETs With an ALD Al_2O_3 Gate Dielectric

Vladimir Djara, *Student Member, IEEE*, Karim Cherkaoui, Michael Schmidt, Scott Monaghan, *Member, IEEE*, Éamon O'Connor, Ian M. Povey, Dan O'Connell, Martyn E. Pemble, and Paul K. Hurley

***Abstract*—We investigated the effect of forming gas (5% H_2/95% N_2) annealing on surface-channel $In_{0.53}Ga_{0.47}As$ MOSFETs with atomic-layer-deposited Al_2O_3 as the gate dielectric. We found that a forming gas anneal (FGA) at 300 °C for 30 min was efficient at removing or passivating positive fixed charges in Al_2O_3, resulting in a shift of the threshold voltage from −0.63 to 0.43 V and in an increase in the I_{on}/I_{off} ratio of three orders of magnitude. Following FGA, the MOSFETs exhibited a subthreshold swing of 150 mV/dec, and the peak transconductance, drive current, and peak effective mobility increased by 29%, 25%, and 15%, respectively. FGA significantly improved the source- or drain-to-substrate junction isolation, with a reduction of two orders of magnitude in the reverse bias leakage exhibited by the Si-implanted $In_{0.53}Ga_{0.47}As$ n^+/p junctions, which is consistent with passivation of midgap defects in $In_{0.53}Ga_{0.47}As$ by the FGA process.**

***Index Terms*—Forming gas anneal (FGA), high-k, InGaAs, metal–oxide–semiconductor field-effect transistor (MOSFET), surface channel.**

I. Introduction

In RECENT years, surface-channel $In_{0.53}Ga_{0.47}As$ metal–oxide–semiconductor field-effect transistors (MOSFETs) have attracted considerable research attention as silicon technology is gradually reaching the limits of dimensional scaling [1]–[4]. One major obstacle to the development of these devices is the integration of high-k gate oxides on the $In_{0.53}Ga_{0.47}As$ surface with sufficiently low density of interface states (D_{it}) and fixed oxide charges. Various methods such as $(NH_4)_2S$ passivation [5]–[8], silicon interlayer [9], [10], interface control layer [11], [12], and InP capping [13] have been explored to reduce D_{it}. Forming gas (H_2/N_2) annealing, which is well known for passivating P_b-like defects in SiO_2/Si and high-$k/SiO_x/Si$ systems [14], [15], represents an alternative or complimentary approach for reducing defects in high-$k/In_{0.53}Ga_{0.47}As$ structures subsequent to the gate oxide deposition.

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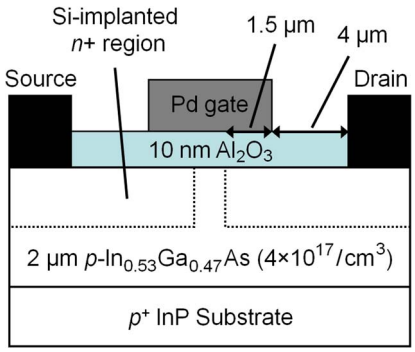

Fig. 1. Schematic cross-sectional diagram of a surface-channel $In_{0.53}Ga_{0.47}As$ MOSFET with a 10-nm-thick ALD Al_2O_3 gate dielectric. The gate overlap is 1.5 μm, and the separation between the gate contact and the source or drain contact is 4 μm.

Recent studies using metal–oxide–semiconductor capacitors (MOSCAPs) have shown that a forming gas anneal (FGA) can reduce the fixed oxide charge density in $Al_2O_3/In_{0.53}Ga_{0.47}As$ systems [16], [17] and reduce D_{it} near the $In_{0.53}Ga_{0.47}As$ conduction band in HfO_2/n-$In_{0.53}Ga_{0.47}As$ systems [18]. However, results reported to date do not indicate any significant influence of FGA on the prominent donor-like defects near midgap [5].

In this paper, we extend on the work reported to date on the effect of FGA on $In_{0.53}Ga_{0.47}As$ MOSCAPs [16], [17] to investigate the impact of FGA on surface-channel $In_{0.53}Ga_{0.47}As$ MOSFETs. The availability of $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSFETs allows not only to study the impact of FGA on the $Al_2O_3/In_{0.53}Ga_{0.47}As$ gate stack but also to investigate its effect on carrier transport at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface and on the Si-implanted $In_{0.53}Ga_{0.47}As$ n^+/p junctions.

II. Device Fabrication

Surface-channel MOSFETs (see Fig. 1) and MOSCAPs were fabricated on a 2-μm-thick Zn-doped $(4 \times 10^{17}\ /cm^3)$ p-$In_{0.53}Ga_{0.47}As$ layer grown on a 2-in p^+ InP wafer by metal–organic vapor phase epitaxy. The $In_{0.53}Ga_{0.47}As$ surface passivation prior to gate oxide deposition was an immersion in 10% $(NH_4)_2S$ at room temperature for 20 min, which was found to be an optimum in terms of D_{it} reduction and native oxide suppression [5], [6]. The transfer time to the atomic layer

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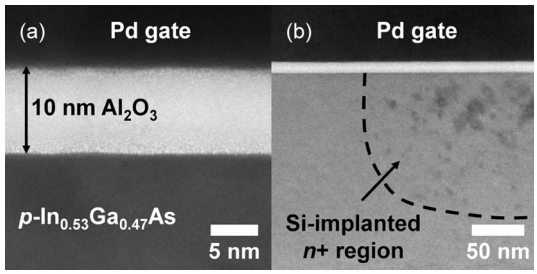

Fig. 2. Cross-sectional TEM images (a) through the gate stack region of the MOSFET confirming the 10-nm Al_2O_3 gate oxide thickness and (b) through the gate overlap region, showing the implant defects in the Si-implanted n^+ region.

deposition (ALD) reactor after surface passivation was less than 5 min. A 10-nm-thick Al_2O_3 gate oxide film was formed by ALD using alternating pulses of $Al(CH_3)_3$ (TMA) and H_2O precursors at 250 °C. The source and drain (S/D) regions were selectively implanted with a Si dose of 1×10^{14} /cm^2 at 80 keV and 1×10^{14} /cm^2 at 30 keV. Implant activation was achieved by rapid thermal annealing at 600 °C for 15 s in a N_2 atmosphere. A 140-nm-thick SiO_2 field oxide was formed by electron-beam evaporation and liftoff to minimize the gate pad capacitance. Nonself-aligned ohmic contacts were defined by lithography, selective wet etching of Al_2O_3 in dilute HF, and electron-beam evaporation of a Au (14 nm)/Ge (14 nm)/Au (14 nm)/Ni (11 nm)/Au (200 nm) metal stack [19]. A 200-nm-thick Pd gate was defined by electron-beam evaporation and liftoff. Forming gas (5% H_2/95% N_2) annealing was carried out at 300 °C for 30 min in an open tube furnace. Tests confirmed the absence of delamination of the Pd metal following FGA.

The finished devices had a nominal gate length (L) of 1, 2, 3, 5, 10, 20, and 40 μm with a 1.5-μm gate metal overlap on the Si-implanted S/D regions, a 4-μm gate-contact-to-source- or drain-contact separation, and a 50-μm gate width. Relatively long-channel-length MOSFETs were intentionally selected to allow the effect of the FGA process on the electrical properties to be examined in the absence of short-channel effects.

III. Results and Discussion

A. TEM Analysis of Gate Stack and Si-Implanted Regions

Cross-sectional transmission electron microscopy (TEM) images through the gate stack region and through the gate overlap region at the end of the MOSFET fabrication are shown in Fig. 2(a) and (b), respectively. Fig. 2(a) confirms the 10-nm Al_2O_3 film thickness, which corresponds to the nominal value from the ALD process and a growth rate per cycle of 1 Å/cycle. There is no evidence of an interface oxide between the $In_{0.53}Ga_{0.47}As$ surface and the Al_2O_3 film, consistent with previous reports for the optimized $(NH_4)_2S$ process and subsequent ALD Al_2O_3 formation [5], and with the reported "self-cleaning" effect of Al_2O_3 formed by ALD on GaAs [20] and $In_{0.15}Ga_{0.85}As$ [21] surfaces. Fig. 2(b) shows the remaining implant defects in the gate overlap region after activation anneal and FGA, indicating that these two anneals are not sufficient to fully remove the defects caused by the Si implantation process.

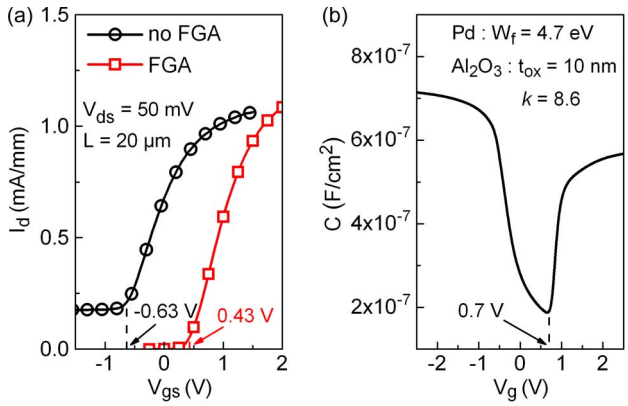

Fig. 3. (a) I_d–V_{gs} obtained on 20-μm-gate-length and 50-μm-gate-width MOSFETs at $V_{ds} = 50$ mV before and after FGA. The MOSFETs feature a V_t of -0.63 and 0.43 V before and after FGA, respectively. (b) Quasi-static C–V simulation of the $Pd/Al_2O_3/p\text{-}In_{0.53}Ga_{0.47}As$ gate stack obtained using a Poisson–Schrödinger simulator [22]. The ideal V_t of 0.7 V was obtained based on a Pd work function of 4.7 eV [24], a 10-nm-thick Al_2O_3 film with a k-value of 8.6, and a $p\text{-}In_{0.53}Ga_{0.47}As$ doping level of 4×10^{17} /cm^3.

B. Fixed Oxide Charge Passivation, Threshold Voltage Shift, OFF-State Leakage, and Subthreshold Swing Reduction

Fig. 3(a) shows the I_d–V_{gs} characteristics at $V_{ds} = 50$ mV obtained on 20-μm-gate-length and 50-μm-gate-width MOSFETs before and after FGA. The threshold voltage (V_t) shifts from -0.63 V before FGA to 0.43 V after FGA. The negative V_t before FGA indicates the presence of fixed positive charges within the Al_2O_3. Fig. 3(b) shows the quasi-static capacitance versus voltage (C–V) simulation of the $Pd/Al_2O_3/p\text{-}In_{0.53}Ga_{0.47}As$ gate stack obtained using a self-consistent Poisson–Schrödinger simulator [22]. The asymmetric shape of the simulated quasi-static C–V response, due to the very low density of states of the $In_{0.53}Ga_{0.47}As$ conduction band, is not experimentally observed. This absence of asymmetry has been attributed to the presence of additional interface defect states in the $In_{0.53}Ga_{0.47}As$ conduction band [23]. In the simulation, the work function (W_f) of Pd on Al_2O_3, the thickness (t_{ox}) and k-value of the Al_2O_3 film, and the $p\text{-}In_{0.53}Ga_{0.47}As$ doping level were set to 4.7 eV [24], 10 nm, 8.6,[1] and 4×10^{17} /cm^3, respectively. Considering an ideal V_t of 0.7 V [see Fig. 3(b)] and an oxide capacitance (C_{ox}) of 7.6×10^{-7} F/cm^2, we calculated an equivalent density of fixed positive oxide charge at the $Al_2O_3/p\text{-}In_{0.53}Ga_{0.47}As$ interface before and after FGA of 6.3×10^{12} /cm^2 and 1.3×10^{12} /cm^2, respectively. Recent studies of $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs over n- and $p\text{-}In_{0.53}Ga_{0.47}As$ prior to FGA reported fixed positive oxide charge densities of $\sim 1 \times 10^{19}$ /cm^3 distributed throughout the Al_2O_3 layer [16]. A density of $\sim 1 \times 10^{19}$ /cm^3 throughout a 10-nm-thick Al_2O_3 film corresponds to an equivalent surface density at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface of $\sim 1 \times 10^{13}$ /cm^2, which is in close agreement with our pre-FGA value of 6.3×10^{12} /cm^2. The reduction in the fixed positive oxide charge after FGA is also in agreement with [16] and [17].

[1]The k-value of 8.6 for Al_2O_3 was obtained from the slope of the capacitance equivalent thickness in accumulation versus the oxide thickness for $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structures with Al_2O_3 thicknesses ranging from 5 to 20 nm.

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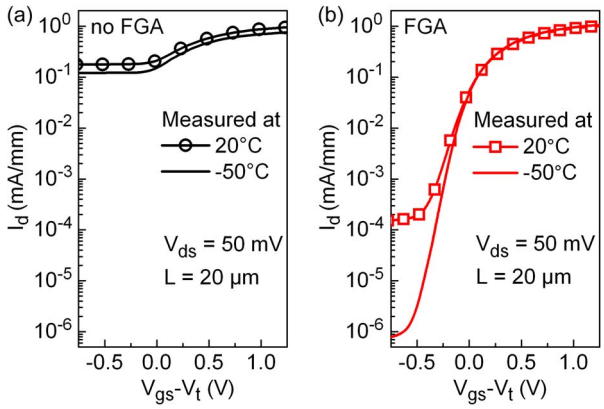

Fig. 4. Comparison of the 20 °C and −50 °C log I_d–V_{gs} measured at V_{ds} = 50 mV on 20-μm-gate-length and 50-μm-gate-width MOSFETs (a) before and (b) after FGA. The log I_d–V_{gs} values are shown with matched gate overdrive ($V_{gs} - V_t$).

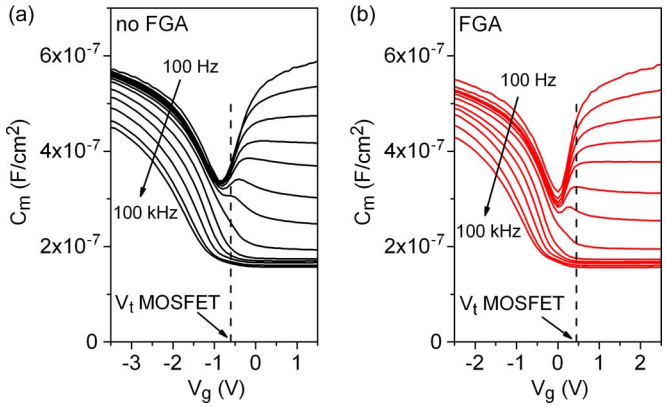

Fig. 5. Multifrequency C–V characteristics of Pd/Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ MOSCAPs measured from 100 Hz to 100 kHz (a) before and (b) after FGA. The V_t of the corresponding MOSFETs is highlighted on the C–V characteristics.

The origin of the fixed positive charge has been assigned to Al dangling bonds based on theoretical modeling [17], and its reduction following FGA is consistent with hydrogen passivation of the dangling bond sites in Al_2O_3.

The fixed charge within the Al_2O_3 gate oxide can have a significant impact on the MOSFET behavior. We calculated that, for a 4×10^{17} /cm^3 p-type $In_{0.53}Ga_{0.47}As$ doping, fixed positive charge densities in excess of 2×10^{12} /cm^2 are sufficient to create an inversion layer at the Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ interface.[2] This indicates that the fixed positive oxide charge density of 6.3×10^{12} /cm^2 before FGA is sufficient to invert the p-$In_{0.53}Ga_{0.47}As$ surface, whereas the fixed positive oxide charge density of 1.3×10^{12} /cm^2 after FGA is not. The strong inversion layer before FGA can be modulated in the region under the Pd gate. However, this inversion charge is also present in the region outside the area defined by the gate and is subsequently referred to as the "peripheral inversion region." We suggest that the high OFF-state leakage and poor subthreshold swing (SS) of the MOSFET before FGA [see Fig. 4(a)] are due to the presence of a peripheral inversion region that cannot be controlled by the gate voltage. The log I_d–V_{gs} characteristics measured at 20 °C and −50 °C before FGA [see Fig. 4(a)] reveals that the OFF-state leakage (I_d at $V_{gs} - V_t < 0$ V) is only weakly temperature dependent, which further indicates that the OFF-state leakage before FGA is due to the peripheral inversion region. It is noted that the formation of a peripheral inversion depends on the substrate doping concentration, the oxide capacitance, and the density and sign of the fixed oxide charge. Moreover, a high leakage current due to a peripheral inversion region will not be observed on a "ring-gate" MOSFET, where the gate encircles the drain and obviates the need for isolation [26]. Fig. 4(b) shows an OFF-state leakage reduction of three orders of magnitude ($I_{on}/I_{off} \sim 10^4$) due to the removal of the peripheral inversion region following FGA. The temperature dependence of the OFF-state leakage after FGA is evident, and the I_{on}/I_{off} ratio at −50 °C is $\sim 10^6$.

Following FGA, a reasonable SS of 150 mV/dec is obtained. This SS yields a midgap D_{it} value of $\sim 5.8 \times 10^{12}$ /cm$^2 \cdot$ eV, which is consistent with our previous work on $In_{0.53}Ga_{0.47}As$ MOSCAPs fabricated with the same surface passivation, transfer time to the ALD reactor after surface passivation, and Al_2O_3 gate oxide [5]. Moreover, the midgap D_{it} value of $\sim 5.8 \times 10^{12}$ /cm$^2 \cdot$ eV is in the range typically reported for high-k/$In_{0.53}Ga_{0.47}As$ MOSCAPs [27] and MOSFETs [28]. It is noted that, for the pre-FGA case, the SS is dominated by the peripheral leakage current and cannot be used for interface state density determination.

C. MOSCAPs Behavior and Density of Interface States

Fig. 5(a) and (b) shows the multifrequency C–V characteristics of Pd/Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ MOSCAPs before and after FGA. The MOSCAPs are adjacent to the MOSFETs. The passivation of fixed positive charges within the Al_2O_3 after FGA results in a voltage shift of the C–V characteristics, consistent with the voltage shift observed on the I_d–V_{gs} characteristics shown in Fig. 3(a). The comparison of the 100-Hz C–V responses at the onset of inversion shows a steeper slope after FGA, indicating a D_{it} reduction near the p-$In_{0.53}Ga_{0.47}As$ conduction band, consistent with [18].

There has been debate over the expected C–V response of $In_{0.53}Ga_{0.47}As$ MOSCAPs in inversion and the method to identify genuine surface inversion [27]. The availability of the MOSCAPs and adjacent MOSFETs on the same wafer allows the V_t obtained from the MOSFETs to be identified on the multifrequency C–V response of the MOSCAPs. Fig. 5(a) and (b) show that, beyond inversion ($V_g > V_t$), the capacitance as a function of applied voltage increases and then acquires an approximately constant value. The value of the capacitance in inversion increases with decreasing ac signal frequency up to a maximum value set by the oxide capacitance. This frequency-dependent C–V behavior has been also obtained following an optimized $(NH_4)_2S$ treatment of n- and p-$In_{0.53}Ga_{0.47}As$ prior to ALD Al_2O_3 deposition [7].

[2]For a doping concentration of 4×10^{17} /cm^3, the maximum depletion width for $In_{0.53}Ga_{0.47}As$ is 50 nm (where the intrinsic carrier concentration for $In_{0.53}Ga_{0.47}As$ is taken as 6.3×10^{11} /cm^3 [25]). Hence, the total density of charge resulting from the ionized acceptor at the onset of inversion is 2×10^{12} /cm^2. Positive oxide charge densities in Al_2O_3 in excess of 2×10^{12} /cm^2 will result in inversion of the p-$In_{0.53}Ga_{0.47}As$ surface.

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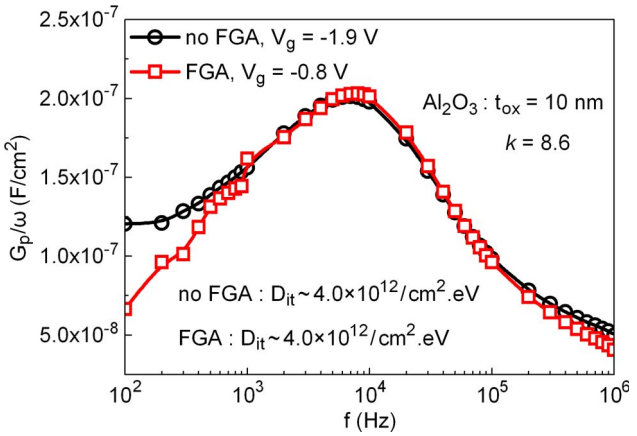

Fig. 6. Normalized parallel conductance (G_p/ω) versus ac signal frequency (f) obtained with the conductance method for a 10-nm-thick Al_2O_3 film with a k-value of 8.6 and considering the nonzero deviation in the semiconductor band bending [29], [30]. The midgap $D_{\rm it}$ before and after FGA is $\sim 4.0 \times 10^{12}$ /cm$^2 \cdot$ eV.

Fig. 6 shows the normalized parallel conductance (G_p/ω) versus ac signal frequency (f) for a selected gate voltage giving the peak G_p/ω, before and after FGA. The peak G_p/ω was observed for a V_g of -1.9 V before FGA and -0.8 V after FGA, corresponding to a $V_g - V_t$ of ~ -1.25 V before and after FGA. The conductance method accounting for the nonzero deviation in the semiconductor band bending [29], [30] was applied for the extraction of the values of midgap $D_{\rm it}$ and trap response time (τ). FGA did not reduce the midgap $D_{\rm it}$ as values of $\sim 4.0 \times 10^{12}$ /cm$^2 \cdot$ eV were extracted before and after FGA. Moreover, the midgap $D_{\rm it}$ value obtained from the conductance method is in reasonable agreement with the midgap $D_{\rm it}$ value of $\sim 5.8 \times 10^{12}$ /cm$^2 \cdot$ eV extracted from the SS of the MOSFETs post FGA. FGA did not have a significant impact on τ as values of ~ 48.5 and ~ 43.8 μs were obtained before and after FGA, respectively.

D. Transconductance, Drive Current, and Effective Mobility Improvement

Fig. 7(a) compares the transconductance (g_m) versus gate overdrive ($V_{gs} - V_t$) obtained on 20-μm-gate-length and 50-μm-gate-width MOSFETs before and after FGA. Whereas the peak g_m increases by 29% after FGA, the higher field values of g_m only slightly improve with FGA.

Fig. 7(b) compares the I_d–V_{ds} output characteristics of 20-μm-gate-length and 50-μm-gate-width MOSFETs before and after FGA. The MOSFETs exhibit well-behaved output characteristics with drain current saturation for $V_{ds} > V_{gs} - V_t$. The drive current at a 2-V gate overdrive was 14.8 mA/mm before FGA and 18.5 mA/mm after FGA, representing a 25% improvement with FGA. These drive current values are comparable with, or slightly higher than, other published values for surface-channel $In_{0.53}Ga_{0.47}As$ MOSFETs [9], [31], assuming drive current scaling with $1/L$.

Fig. 8 shows the effective mobility ($\mu_{\rm eff}$) as a function of the inversion charge density ($N_{\rm inv}$) extracted using the I_d–V_{gs} characteristics [see Fig. 3(a)] and the 2-MHz gate-to-channel split C–V characteristics (see the inset in Fig. 8). The parasitic overlap capacitances were removed from the

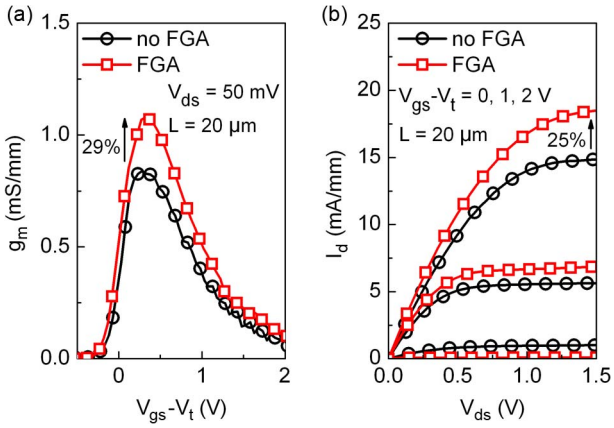

Fig. 7. (a) Transconductance (g_m) versus gate overdrive ($V_{gs} - V_t$) and (b) I_d–V_{ds} characteristics obtained on 20-μm-gate-length and 50-μm-gate-width MOSFETs before and after FGA. After FGA, the peak g_m and drive current increase by 29% and 25%, respectively.

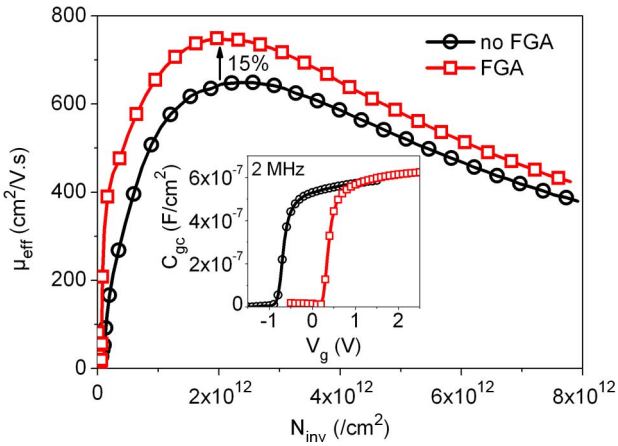

Fig. 8. Effective mobility ($\mu_{\rm eff}$) versus inversion charge density ($N_{\rm inv}$) before and after FGA. The peak $\mu_{\rm eff}$ increases by 15% after FGA. (Inset) 2-MHz gate-to-channel C_{gc} split C–V characteristics before and after FGA.

measured gate-to-channel capacitance (C_{gc}) using the method reported in [32]. MOSFETs with L ranging from 1 to 40 μm were used to extract the S/D resistance (R_{sd}) values used in the mobility correction. R_{sd} values were evaluated at $V_{ds} =$ 50 mV to ensure device operation in the linear region. The MOSFETs featured a R_{sd} of 235 and 103 Ω before and after FGA, respectively. The peak $\mu_{\rm eff}$ increased from 650 to 750 cm^2/V $\cdot$ s with FGA. This 15% improvement in the peak $\mu_{\rm eff}$ after FGA is consistent with a reduction of the positive fixed charge density in the Al_2O_3 gate oxide along with a reduction of $D_{\rm it}$ at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface near the $In_{0.53}Ga_{0.47}As$ conduction band. The peak $\mu_{\rm eff}$ after FGA is comparable with other published values for Al_2O_3-gate surface-channel $In_{0.53}Ga_{0.47}As$ MOSFETs, where the following peak $\mu_{\rm eff}$ values are reported: 725 cm^2/V $\cdot$ s for a 10-nm-thick Al_2O_3 gate oxide and 1×10^{17} /cm^3 p-type doping in the $In_{0.53}Ga_{0.47}As$ channel region [9], 847 cm^2/V $\cdot$ s for a 9-nm-thick Al_2O_3 gate oxide and 2×10^{16} /cm^3 p-type doping in the $In_{0.53}Ga_{0.47}As$ channel region [31], and 1100 cm^2/V $\cdot$ s for a 8-nm-thick Al_2O_3 gate oxide and 1×10^{17} /cm^3 p-type doping in the $In_{0.53}Ga_{0.47}As$ channel region [33]. It is noted that, for the comparative publications cited above, the

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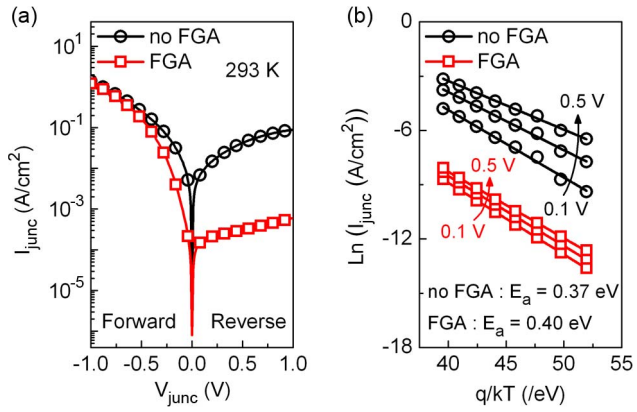

Fig. 9. (a) I–V characteristics of the n^+/p $In_{0.53}Ga_{0.47}As$ junction measured at 293 K before and after FGA. (b) Arrhenius plot from 223 to 293 K for reverse bias going from 0.1 to 0.5 V applied to implanted n^+/p junctions before and after FGA. The area of the n^+/p junction diodes is 10^4 μm^2. The activation energy (E_a) values are 0.37 and 0.40 eV before and after FGA, respectively.

$In_{0.53}Ga_{0.47}As$ channel doping was 4–20 times lower than the value of 4×10^{17} /cm^3 used in this paper.

The published experimental values for the peak μ_{eff} in surface-channel inversion-mode $In_{0.53}Ga_{0.47}As$ MOSFETs remain well below the theoretical values expected for reasonable values of fixed oxide charge, interface states, and surface roughness, where peak values of ~ 4000 cm^2/V $\cdot$ s are calculated [34]. This discrepancy could relate to the approach typically employed to determine μ_{eff}. Indeed, for the calculation of N_{inv} on the x-axis in Fig. 8, it is assumed that the integral of C_{gc} above the threshold voltage yields N_{inv} and is unaffected by trapped charges in interface states or in bulk oxide traps. A number of recent publications have provided evidence that interface states exist with energies aligned with the $In_{0.53}Ga_{0.47}As$ conduction band [18], [23], [35]. In this case, the integral of C_{gc} will contain contributions from both trapped and free charges, which will result in an overestimation of N_{inv} and a corresponding underestimation of μ_{eff}. No corrections for the effect of bulk oxide charge trapping or interface states with energies aligned with the $In_{0.53}Ga_{0.47}As$ conduction band have been applied in this paper, in line with the majority of literature to date [9], [31], [33].

E. Junction Leakage Reduction

FGA also improves the current–voltage behavior of the source- or drain-to-substrate $In_{0.53}Ga_{0.47}As$ n^+/p junctions. Fig. 9(a) shows the current density versus voltage (I–V) characteristics for the n^+/p junctions before and after FGA. The saturation current in reverse bias is reduced by more than two orders of magnitude as a result of FGA. The measurement temperature (223–293 K) and applied bias (0.1–0.5 V) dependence of the n^+/p junction characteristics before and after FGA is shown in Fig. 9(b). The activation energy (E_a) extrapolated to zero bias from Fig. 9(b) yields values of 0.37 and 0.40 eV before and after FGA, respectively. The extracted E_a indicates thermal generation of electron–hole pairs through midgap states in the $In_{0.53}Ga_{0.47}As$ depletion region as the mechanism of the reverse bias leakage both before and after FGA. The reduction of leakage current density is consistent with the passivation of midgap states by FGA. Both before and after FGA, E_a decreases with increasing reverse bias, which is characteristic of a field-enhanced (Poole–Frenkel)-type emission process [36].

IV. Conclusion

We have demonstrated that a FGA $(5\%H_2/95\%N_2)$ at 300 °C for 30 min dramatically improved the performance of surface-channel $In_{0.53}Ga_{0.47}As$ MOSFETs with Al_2O_3 as the gate dielectric. The FGA process reduced the density of fixed positive charges in Al_2O_3, which removed a parasitic peripheral inversion region and resulted in an increase in $I_{\text{on}}/I_{\text{off}}$ by three orders of magnitude. FGA improved the peak g_m, drive current, and peak μ_{eff} by 29%, 25%, and 15%, respectively. Multifrequency C–V measurements of MOSCAPs revealed that FGA reduced the D_{it} value near the $In_{0.53}Ga_{0.47}As$ conduction band but did not reduce the midgap D_{it} value. The reduction of the fixed positive charge in the gate oxide combined with the reduction of D_{it} near the $In_{0.53}Ga_{0.47}As$ conduction band is consistent with the peak μ_{eff} improvement. A reduction of two orders of magnitude was observed in the reverse bias leakage current density in the Si-implanted $In_{0.53}Ga_{0.47}As$ n^+/p junctions in the S/D regions of the MOSFETs, consistent with the passivation of near midgap defects in the $In_{0.53}Ga_{0.47}As$ by FGA.

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References

[1] M. Yokoyama, R. Iida, S. Kim, N. Taoka, Y. Urabe, H. Takagi, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, "Sub-10-nm extremely thin body InGaAs-on-insulator MOSFETs on Si wafers with ultrathin Al_2O_3 buried oxide layers," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1218–1220, Sep. 2011.

[2] H.-C. Chin, X. Liu, X. Gong, and Y.-C. Yeo, "Silane and ammonia surface passivation technology for high-mobility $In_{0.53}Ga_{0.47}As$ MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 5, pp. 973–979, May 2010.

[3] U. Singisetti, M. A. Wistey, G. J. Burek, A. K. Baraskar, B. J. Thibeault, A. C. Gossard, M. J. W. Rodwell, B. Shin, E. J. Kim, P. C. McIntyre, B. Yu, Y. Yuan, D. Wang, Y. Taur, P. Asbeck, and Y.-J. Lee, "$In_{0.53}Ga_{0.47}As$ channel MOSFETs with self-aligned InAs source/drain formed by MEE regrowth," *IEEE Electron Device Lett.*, vol. 30, no. 11, pp. 1128–1130, Nov. 2009.

[4] N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampatic, M. Yakimov, Y. Sun, P. Pianetta, C. K. Gaspe, M. B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, "Addressing the gate stack challenge for high mobility $In_xGa_{1-x}As$ channels for NFETs," in *IEDM Tech. Dig.*, 2008, pp. 1–4.

[5] É. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, "A systematic study of $(NH_4)_2S$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ system for n-type and p-type $In_{0.53}Ga_{0.47}As$ epitaxial layers," *J. Appl. Phys.*, vol. 109, no. 2, pp. 024 101-1–024 101-10, Jan. 2011.

[6] B. Brennan, M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, G. Hughes, and R. M. Wallace, "Optimisation of the ammonium sulphide $(NH_4)_2S$ passivation process on $In_{0.53}Ga_{0.47}As$," *Appl. Surf. Sci.*, vol. 257, no. 9, pp. 4082–4090, Feb. 2011.

[7] É. O'Connor, S. Monaghan, K. Cherkaoui, I. M. Povey, and P. K. Hurley, "Analysis of the minority carrier response of n-type and

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

p-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$ capacitors following optimized $(NH_4)_2S$ treatment," *Appl. Phys. Lett.*, vol. 99, no. 21, pp. 212901-1–212901-3, Nov. 2011.

[8] J. J. Gu, A. T. Neal, and P. D. Ye, "Effects of $(NH_4)_2S$ passivation on the OFF-state performance of 3-dimensional InGaAs metal–oxide–semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 99, no. 15, pp. 152113-1–152113-3, Oct. 2011.

[9] A. M. Sonnet, C. L. Hinkle, M. N. Jivani, R. A. Chapman, G. P. Pollack, R. M. Wallace, and E. M. Vogel, "Performance enhancement of n-channel inversion type $In_xGa_{1-x}As$ metal–oxide–semiconductor field effect transistor using *ex situ* deposited thin amorphous silicon layer," *Appl. Phys. Lett.*, vol. 93, no. 12, pp. 122109-1–122109-3, Sep. 2008.

[10] F. Zhu, H. Zhao, I. Ok, H. S. Kim, J. Yum, J. C. Lee, N. Goel, W. Tsai, C. K. Gaspe, and M. B. Santos, "Effects of anneal and silicon interface passivation layer thickness on device characteristics of $In_{0.53}Ga_{0.47}As$ metal–oxide–semiconductor field-effect transistors," *Electrochem. Solid-State Lett.*, vol. 12, no. 4, pp. H131–H134, Mar. 2009.

[11] A. O'Mahony, S. Monaghan, G. Provenzano, I. M. Povey, M. G. Nolan, É. O'Connor, K. Cherkaoui, S. B. Newcomb, F. Crupi, P. K. Hurley, and M. E. Pemble, "Structural and electrical analysis of the atomic layer deposition of $HfO_2/n-In_{0.53}Ga_{0.47}As$ capacitors with and without an Al_2O_3 interface control layer," *Appl. Phys. Lett.*, vol. 97, no. 5, pp. 052904-1–052904-3, Aug. 2010.

[12] S. Monaghan, A. O'Mahony, K. Cherkaoui, É. O'Connor, I. M. Povey, M. G. Nolan, D. O'Connell, M. E. Pemble, P. K. Hurley, G. Provenzano, F. Crupi, and S. B. Newcomb, "Electrical analysis of three-stage passivated $In_{0.53}Ga_{0.47}As$ capacitors with varying HfO_2 thicknesses and incorporating an Al_2O_3 interface control layer," *J. Vac Sci. Technol. B*, vol. 29, no. 1, pp. 01A807-1–01A807-8, Jan. 2011.

[13] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, "Advanced high-k gate dielectric for high-performance short-channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate for low power logic applications," in *IEDM Tech. Dig.*, 2009, pp. 1–4.

[14] A. Stesmans and V. V. Afanas'ev, "Si dangling-bond-type defects at the interface of (100)Si with ultrathin layers of SiO_x, Al_2O_3, and ZrO_2," *Appl. Phys. Lett.*, vol. 80, no. 11, pp. 1957–1959, Mar. 2002.

[15] R. J. Carter, E. Cartier, A. Kerber, L. Pantisano, T. Schram, S. De Gendt, and M. Heyns, "Passivation and interface state density of SiO_2/HfO_2-based/polycrystalline-Si gate stacks," *Appl. Phys. Lett.*, vol. 83, no. 3, pp. 533–535, Jul. 2003.

[16] R. D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre, and P. K. Hurley, "Charged defect quantification in $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ MOS capacitors," *J. Electrochem. Soc.*, vol. 158, no. 5, pp. G103–G107, Mar. 2011.

[17] B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle, and P. C. McIntyre, "Origin and passivation of fixed charge in atomic layer deposited aluminum oxide gate insulators on chemically treated InGaAs substrates," *Appl. Phys. Lett.*, vol. 96, no. 15, pp. 152908-1–152908-3, Apr. 2010.

[18] É. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, and P. K. Hurley, "Temperature and frequency dependent electrical characterization of $HfO_2/In_xGa_{1-x}As$ interfaces using capacitance-voltage and conductance methods," *Appl. Phys. Lett.*, vol. 94, no. 10, pp. 102902-1–102902-3, Mar. 2009.

[19] P. A. F. Herbert, L. P. Floyd, J. I. Braddell, E. M. Baldwin, and W. M. Kelly, "The application of ohmic contacts to nanometric structures," *Microelectron. Eng.*, vol. 17, no. 1–4, pp. 541–545, Mar. 1992.

[20] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, " HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition," *Appl. Phys. Lett.*, vol. 86, no. 15, pp. 152904-1–152904-3, Apr. 2005.

[21] M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, "Surface passivation of III–V compound semiconductors using atomic-layer-deposition-grown Al_2O_3," *Appl. Phys. Lett.*, vol. 87, no. 25, pp. 252104-1–252104-3, Dec. 2005.

[22] [Online]. Available: http://www.nd.edu/~gsnider/

[23] G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, "On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces," *Appl. Phys. Lett.*, vol. 95, no. 20, pp. 202109-1–202109-3, Nov. 2009.

[24] A. Diligenti and M. Stagi, "Tunnelling in aluminium/aluminium-oxide/palladium junctions: Hydrogen-induced variations," *Electron. Lett.*, vol. 19, no. 18, pp. 717–718, Sep. 1983.

[25] [Online]. Available: www.ioffe.ru

[26] F. Zhu, H. Zhao, I. Ok, H. S. Kim, J. Yum, J. C. Lee, N. Goel, W. Tsai, C. K. Gaspe, and M. B. Santos, "A high performance $In_{0.53}Ga_{0.47}As$ metal–oxide–semiconductor field effect transistor with silicon interface passivation layer," *Appl. Phys. Lett.*, vol. 94, no. 1, pp. 013511-1–013511-3, Jan. 2009.

[27] R. Engel-Herbert, Y. Hwang, and S. Stemmer, "Comparison of methods to quantify interface trap densities at dielectric/III–V semiconductor interfaces," *J. Appl. Phys.*, vol. 108, no. 12, pp. 124101-1–124101-15, Dec. 2010.

[28] A. Ali, H. Madan, S. Koveshnikov, S. Oktyabrsky, R. Kambhampati, T. Heeg, D. Schlom, and S. Datta, "Small-signal response of inversion layers in high-mobility $In_{0.53}Ga_{0.47}As$ MOSFETs made with thin high-K dielectrics," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 742–748, Apr. 2010.

[29] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*. New York: Wiley, 1982, pp. 212–218.

[30] E. H. Nicollian and A. Goetzberger, "The $Si-SiO_2$ interface—Electrical properties as determined by the metal–insulator–silicon conductance technique," *Bell Syst. Tech. J.*, vol. 46, no. 6, pp. 1055–1133, Jul. 1967.

[31] H. Zhao, F. Zhu, Y.-T. Chen, J. H. Yum, Y. Wang, and J. C. Lee, "Effect of channel doping concentration and thickness on device performance for $In_{0.53}Ga_{0.47}As$ metal–oxide–semiconductor transistors with atomic-layer-deposited Al_2O_3 dielectrics," *Appl. Phys. Lett.*, vol. 94, no. 9, pp. 093505-1–093505-3, Mar. 2009.

[32] K. Romanjek, F. Andrieux, T. Ernst, and G. Ghibaudo, "Improved split C–V method for effective mobility extraction in sub-0.1-μm Si MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 583–585, Aug. 2004.

[33] Y. Xuan, Y. Q. Wu, H. C. Lin, T. Shen, and P. D. Ye, "Submicrometer inversion-type enhancement-mode InGaAs MOSFET with atomic-layer-deposited Al_2O_3 as gate dielectric," *IEEE Electron Device Lett.*, vol. 28, no. 11, pp. 935–938, Nov. 2007.

[34] T. P. O'Regan, M. V. Fischetti, B. Sorée, S. Jin, W. Magnus, and M. Meuris, "Calculation of the electron mobility in III–V inversion layers with high-κ dielectrics," *J. Appl. Phys.*, vol. 108, no. 10, pp. 103705-1–103705-11, Nov. 2010.

[35] P. K. Hurley, R. D. Long, T. O'Regan, É. O'Connor, S. Monaghan, V. Djara, M. A. Negara, A. O'Mahony, I. M. Povey, A. Blake, R. E. Nagle, D. O'Connell, M. E. Pemble, and K. Cherkaoui, "Equivalent oxide thickness correction in the high-k/$In_{0.53}Ga_{0.47}As$/InP system," *ECS Trans.*, vol. 33, no. 3, pp. 433–444, Oct. 2010.

[36] S. D. Ganichev, E. Ziemann, W. Prettl, I. N. Yassievich, A. A. Istratov, and E. R. Weber, "Distinction between the Poole–Frenkel and tunneling models of electric-field-stimulated carrier emission from deep levels in semiconductors," *Phys. Rev. B*, vol. 61, no. 15, pp. 10361–10365, Apr. 2000.

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