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Fabrication of micro-thermoelectric devices for power generation and the thermal management of photonic devices

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Abstract

This work demonstrates and discusses the fabrication of cross-plane configured micro thermoelectric devices for the power generation and thermal management of the photonic devices. The device is fabricated using a cost-effective electrodeposition technique on the silicon wafer with 210 pairs of the electrodeposited p-type BiTe and n-type CuTe pillars. The complete device is fabricated using the flip-chip bonding technique. Our focus in this work is on the challenges in the device fabrication and the solutions employed to overcome the obstacles thereby successfully fabricating the micro thermoelectric device.

Keywords: Electrodeposition, Micro-thermoelectric device, MEMS fabrication, Energy-harvesting

1. Introduction

Thermal management of optoelectronics devices is challenging as the device miniaturization generate high heat flux, which makes it difficult to manage the optoelectronic chip within a desired temperature range [1, 2]. One of the solutions to efficiently manage the thermal load of the optoelectronic chip is to use an integrated thermoelectric cooler (TEC) on the chip. Micro TEC (μTEC) offers a wide range of advantages like the small size, quiet operation and reliability [3] compared to the conventional cooling techniques such as fluidics and macro TEC. In addition, μTEC offers precise onsite cooling and high cooling densities due to smaller thermoelectric length, which is very much required for the thermal management of optoelectronic devices [4]. Similarly, the same device can be applied for converting waste heat into usable electricity, when there is a temperature differential. A thermoelectric cooling/ generation can be achieved by applying current/ temperature gradient through single or series of thermoelectric pairs comprising p- and n-type thermoelectric (TE) materials, which are placed electrically in series and thermally in parallel configuration [5-7]. These portable and highly integrated thermoelectric device (TED) are attractive for energy harvesting applications. By miniaturization of these devices and by increasing the density of the thermocouples in the device should lead to high power outputs especially for small temperature differences [8].

Bismuth telluride (Bi-Te) based alloy materials have been extensively studied due to their relatively high thermoelectric efficiency near room temperature regime for the fabrication of thermoelectric devices [9-12]. Different approaches and techniques have been employed to fabricate TE devices in the literature [12, 13]. We employed electrodeposition in the synthesis of thermoelectric materials and devices due to its suitability in terms of cost-effectiveness, up-scalability, and ease of controlling material properties such as composition, crystallinity, and morphology [14-16]. Moreover, because of its compatibility with microelectronic processing techniques, electrodeposition can be used to fabricate micro-thermoelectric device (μTED) directly on the wafer for the thermal management of photonics/ electronic devices and for power generation.

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The thermoelectric device can be broadly classified by its heat flow as in-plane or cross-plane device [13]. Compared to the in-plane, cross-plane setup devices are more advantageous due to their high packing density, low-electrical resistances and improved thermal contacts [12]. However, connecting top contacts in a cross-plane device using the flip-chip bonding process is challenging, which makes the fabrication of cross-plane devices an arduous task.

Previous reports in the literature have demonstrated different approaches to microdevice fabrication, using various material deposition techniques. Most of the works have been demonstrated using single substrate approach, wherein, both the p- and n-type materials are deposited on the single substrate, subsequently etching the bottom interconnects and growing the top interconnects [13, 16]. However, plating two different materials on the same substrate is a complex process involving more number of process steps, thereby adding further to the device cost. Depositing top contacts is always a difficult task, as the use of multiple photoresist layers is involved, and this makes the whole fabrication more complex. In order to address this issue, previous reports in the literature used flip-chip bonding using different solder materials [17, 18]. Fabricating the top interconnects using a different substrate is comparatively an easy process employing the use of bonding material. The bonding material acts as an electrical interconnection material between the thermoelectric leg and the top contact material. There has been a report in the literature for device fabrication using two-substrates, where p- and n-type thermoelectric legs were deposited on two different substrates and bonded in the final stage using a bonding material [19]. However, it should be noted that the materials were deposited using the sputtering method.

In this work, we demonstrate and discuss the fabrication procedure of cross-plane configuration, flip-chip bonded µTED. Developing from our previous work [20], which outlined thermoelectric materials development and initial fabrication steps, this paper deals with the complete fabrication details and initial device characterizations. The device is fabricated using electrodeposition for depositing TE material having 210 leg pairs. P-type BiTe and n-type CuTe pillars are deposited, and the properties of the deposited materials are discussed. Further details can be found in our pervious studies [21-22].

We also discuss the electrodeposition of gold (*Au*) and indium (*In*), which acts as a barrier separation layer for indium diffusion and the bonding material respectively. The impact on the internal resistance of the device by bonding materials and the challenges faced during the flip-chip bonding of the device are discussed. It should be mentioned that such difficulties faced in the fabrication process are not analyzed and reported in the literature. Therefore, in the present work, we discuss various issues faced during the fabrication of the µTED and suggest feasible solutions to overcome the fabrication problems, thereby resulting in the successful manufacturing of electroplated micro thermoelectric devices.

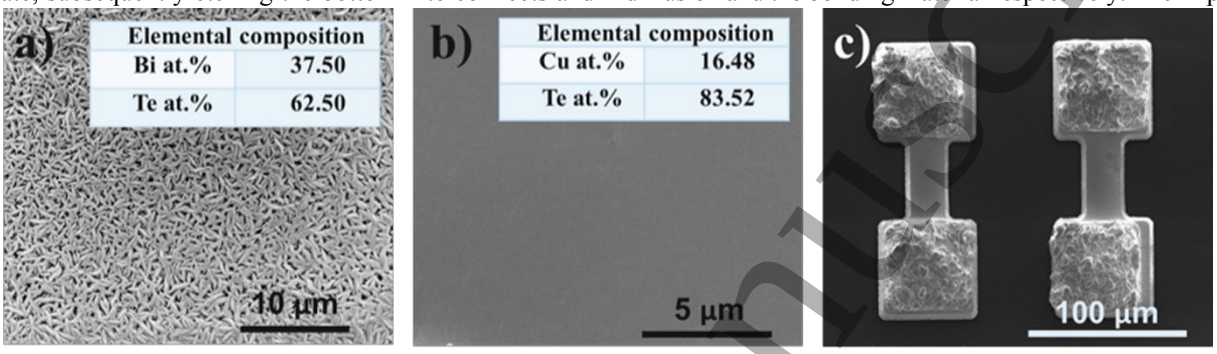


Figure 1: SEM image of electrodeposited pillars along with respective elemental compositions of (a) BiTe, (b) CuTe (c) *In* bump electrodeposited on top of electrodeposited *Au* interconnect material.

2. Experimental procedure

2.1 Thermoelectric pillars deposition

2.1.1 p-type Bi_2Te_3

All the electrochemical depositions during the device fabrication were performed using a CHI600 series electrochemical analyzer/workstation. P-type BiTe pillars of 10 µm thickness were electrodeposited using nitric acid based solution containing 5 mM $Bi(NO_3)_3.5H_2O$, and 15 mM Te. Te and $Bi(NO_3)_3.5H_2O$ were successfully dissolved in 1 M HNO_3 acid. The depositions were performed on Si/SiO_2 substrate with thermally grown oxide having 200 nm of *Au* layer on 20 nm of Titanium (Ti). Platinized titanium mesh was used as the counter electrode and Ag/AgCl as the reference electrode. The pillars were deposited at a constant potential of -40 mV at room temperature without stirring. The deposition rate of BiTe

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in the patterned features was approximately 15 µm/h. The scanning electron microscopy (SEM) [Quanta FEG 450] image of the electrodeposited pillar is shown in Figure 1(a) along with the elemental composition of the deposited TE pillar obtained using energy dispersive spectrometer (EDS) coupled with the SEM.

2.1.2 n-type CuTe

Copper-based thermoelectric materials have not been integrated into a thermoelectric device so far. However, previously Cu pillars have been proposed in the fabrication of the micro thermoelectric device [17]. We report for the first time the use of n-type copper telluride based thermoelectric material in a device, adopting and developing from our previous work. CuTe pillars were electrodeposited using a solution containing 1 M nitric acid, 15 mM pure Te powder and 2 mM copper (II) sulfate pentahydrate. In order to prepare the electrolytic solution, Te was first dissolved in 1 M HNO_3 acid at a temperature of 40 °C while stirring. Copper (II) sulfate pentahydrate, being readily dissolvable in water was separately dissolved in de-ionized (DI) water. Both the solutions were mixed at the later stage while stirring to form the final solution. The depositions were performed using a three-electrode setup at the room temperature. Platinized titanium mesh was used as the counter electrode and Ag/AgCl as a reference electrode. A constant potential of -50 mV was applied to deposit CuTe, which gave better thermoelectric properties obtained from our previous work [21]. The deposition rate of CuTe in the patterned features was approximately 8 µm/h. The SEM image along with the elemental composition is depicted in Figure 1(b).

2.2 The separation layer and bonding material deposition

For the electrodeposition of *Au*, a commercial *Au* bath (Doduco) was used. *Au* was electroplated at a constant current density of 0.02 mA/mm^2 on both the seed layer and the TE materials to serve two different purposes: (1) to increase the thickness of the interconnect material in order to minimize the electrical resistance of the interconnecting material and (2) to act as a barrier separation layer between the BiTe alloy material and the *In* bonding metal. All *Au* depositions were performed at 40 °C, which gave a smooth deposition without stirring.

Commercial *In* bath was used (Indium corp.) to electroplate *In* using the galvanostatic technique with In sheet as a counter electrode. The *In* sheet was thoroughly cleaned before the electrodeposition, using acetone followed by IPA. All the *In* depositions were performed at the room temperature without stirring. *In* was deposited on top of the thermoelectric pillars at a constant current density of 0.05 mA/mm^2. Simultaneously, *In* was deposited on the *Au* interconnect material. The resulting electroplating of *In* was rough with larger grain size as shown in Figure 1(c).

3. Fabrication

The µTED device was fabricated on the 4" <100> Si wafers with 1µm of thermally grown SiO_2 as an insulation layer. A seed layer of *Ti/Au* – 20/200nm was grown using e-beam evaporation on the SiO_2/Si substrate. In order to increase the thickness of the interconnect material, the seed layer was patterned by photolithography using photoresist AZ-9260. This particular photoresist is well known for its stability at very low pH and higher resist thickness. Therefore, AZ-9260 photoresist has been used throughout the device fabrication. *Au* layer of 3 µm was selectively electroplated to increase the interconnect thickness, which will subsequently lower the interconnect resistance between the thermoelectric legs.

Additionally, this electroplated *Au* will act as a seed layer for electroplating of TE material. The photoresist was stripped out after the electroplating of *Au* and the wafer was thoroughly cleaned using Acetone and IPA. Then the wafer was exposed to O_2-plasma for 5 minutes at 50 W, to ensure complete removal of resist residue left on the rough electroplated gold. The wafer was then dried on a hotplate at 110 °C for 5 minutes as a pretreatment for the subsequent photolithographic processes. A fresh layer of photoresist AZ-9260 was spun in order to achieve a uniform thickness of 15 µm for electroplating of TE material. The soft-bake was performed for 5 minutes at 110 °C on a leveled hotplate ensuring the uniformity of the resist. All the baking temperatures were achieved using low ramp rates. After the soft-bake, the wafer was kept at the room temperature for 15 minutes for rehydration before UV exposure. Exposure was done using a mask aligner (MA6) at an intensity of 10 mW/cm^2. The exposed features were developed using AZ-400K developer and then thoroughly rinsed under DI water. The wafer was further exposed under O_2-plasma for 5 minutes at 50 W to remove the residual resist on the electrodeposited *Au*. The O_2-plasma etching also enhances the hydrophilic nature of the photoresist and assists in reducing trapping of air bubbles inside the patterned features, which might hinder the growth of the thermoelectric material during electrodeposition.

CuTe was deposited as n-type thermoelectric material for the device fabrication. A squared thermopile of size 50×50 µm^2 was electrodeposited and the deposition time was managed so that a thickness of 10 µm can be achieved. A higher thickness of the thermopiles is possible with a greater thickness of the photoresist and longer deposition time. After the electrodeposition of TE material, the wafer was thoroughly cleaned under DI water, before it was used for further depositions. Before growing *In* as a bonding material on the thermopile, a thin layer of 200 nm *Au* was electrodeposited on top of the thermopile using the same wafer immediately after TE material deposition. This thin layer of sandwiched *Au* in-

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between TE material and *In* bonding material acts as a barrier separation layer in terms of suppressing the inter-diffusion of *In* into the TE material. Also, this reduces the number of photolithographic steps, which in turn decreases the overall fabrication cost. Similar work showing the barrier nature of *Au* and *T*i was discussed by Lin et al. [23]. An *In* layer of 3 µm thickness was electrodeposited at constant current as explained in the previous section. As the electrodeposited *In* was usually rough and prone to oxidation at elevated temperatures during the bonding process, a thin layer of *Au* of about 50 nm was again deposited to prevent the oxidation of the underlying *In* layer. After this, the supporting photo-resist was removed using acetone and cleaned by isopropanol followed by DI water and dried under nitrogen jet. As the freestanding TE pillars with *Au* and *In* were without structural support, the wafers were handled with utmost care. The photoresist was spun again, to achieve a resist thickness of around 15 µm, similar to n-type thermopile, thereby covering

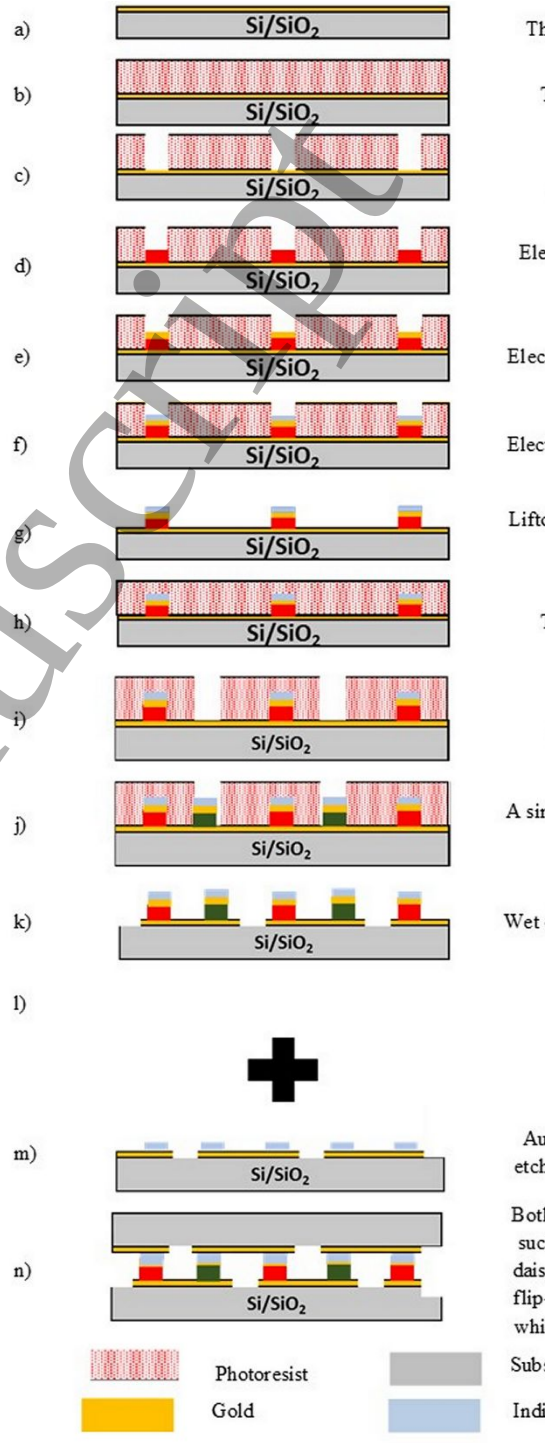


Figure 2: Schematic illustration of device f

and protecting the electrodeposited n-type TE thermopiles. The p-type openings were developed after exposing in the UV light using the mask aligner as described above. All the necessary steps were followed to ensure the verticality of the side walls and removal of the resist residue on the electrodeposited *Au*. P-type BiTe materials were electroplated as explained in the experimental section using a constant

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potential of -40 mV to achieve a thickness of 10 µm (equal to the n-type material) and followed by the electrodeposition of *Au*, *In* and again *Au* in a similar fashion to the previous deposition on the n-type thermopile. The photoresist was removed using acetone, and both the p- and n-type pillars were free standing. The photoresist was spun and exposed on the wafers with p and n-type pillars. The photoresist covers both the pillars and the interconnection, leaving the rest of *Au* seed layer to be etched. The *Au* layer was chemically etched using potassium iodide based solution. The 20 nm of Ti was etched using HF-based solution. After the *Au/Ti* etching, the photoresist was stripped off and the wafer was thoroughly cleaned and exposed under O_2-plasma for 5 minutes as the topography of the pillars was rough due to the rough *In* electrodeposition and the probability of photoresist adhering on to the pillars was very high. Which could lead to a deleterious electrically resistive layer during flip-chip bonding.

In order to connect the p and n-type TE pillars electrically in series, the flip-chip bonding approach was used. Therefore, another wafer which will act as the interconnect material along with the bonding material has to be fabricated. A new Si/SiO_2 wafer with 20 nm of Ti and 200 nm of *Au* was spun with the AZ-9260 photoresist and patterned for the top-interconnect material. *Au* was electrodeposited as a top interconnect material with a thickness of 3 µm, similar to that of wafer 1. In order to make *In-In* bonding possible, *In* metal has to be electroplated as the bonding material. A fresh layer of photoresist was spun on the electrodeposited *Au* covering the interconnect *Au* region and exposing the area where the pillars are expected to bond. *In* layer of 3 µm was electroplated on these exposed areas in a similar way used earlier to deposit *In* on the pillars. Following that, the photoresist was stripped out, and all the cleaning procedures were undertaken. The excess seed layer was chemically wet etched similar to the wafer 1 as shown in Figure 2.

Prior to the bonding, both the wafers were diced into individual dies. The bonding was performed using a FineTech flip-chip bonder by aligning both the bottom and the top interconnect chips in such a way that the pillars form a daisy chain. The challenges and difficulties faced in the fabrication of the device and the proposed feasible solution employed will be discussed in the subsequent section..

4. Results and discussions

4.1 Challenges and feasible solutions

This section of the paper will discuss the different fabrication difficulties and the applied feasible solution.

Au with 200 nm thickness and 20 nm of Ti were grown on a Si/SiO_2 wafer to act as a seed layer for the electrochemical deposition of the thermoelectric pillars. However, the adhesion between the thin layer and the deposited TE pillars were not strong enough to structurally hold the pillars in place as shown in Figure 3. This was due to the photoresist residue still left on the *Au* seed layer, and the induced stress due to the formation of AuTe from the interaction between the Au seed layer and Te from the electrodeposited materials, which can play a role in the detachment of the pillars from the seed layer. The polymer residue at the electrochemically active seed regions were removed by optimizing the photo-lithographic process, mainly by increasing the development time during lithography and exposing the developed wafer to O_2-plasma to ensure the complete removal of the photoresist. Also, this process increases the hydrophilic nature of the photoresist, which helps in the free flow of the electrolyte into the patterns and reduces the air bubble trapping inside the patterns, resulting in the homogeneous growth of the pillars during electrodeposition.

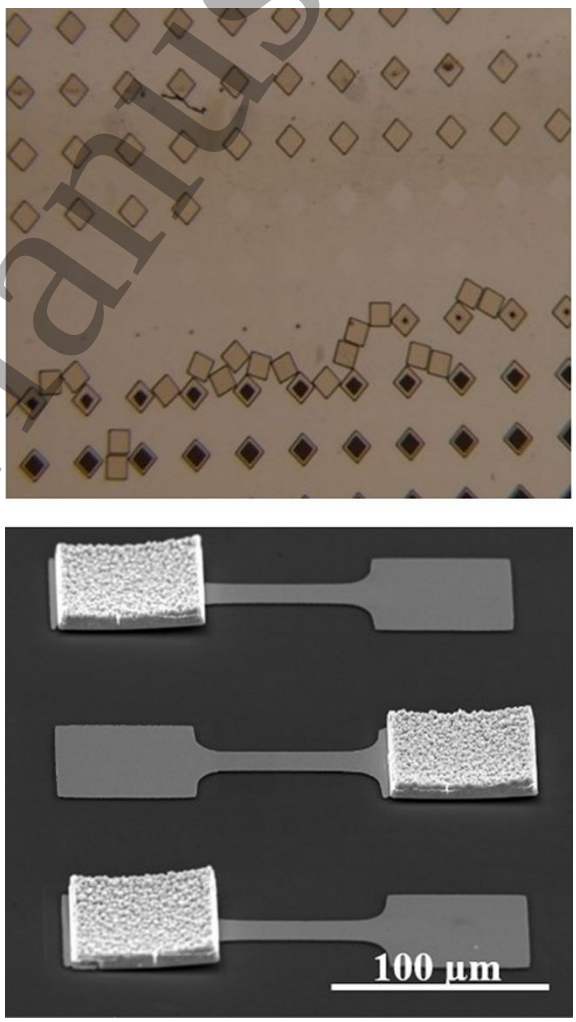


Figure 3: Images show non-adherence of pillars to the seed and delamination of pillars.

The stress from the electrodeposited pillars may lead to the delamination of the pillars along with the seed layer. In order

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to address this issue, the seed layer thickness was increased from 200 nm to 3 µm using the selective electrodeposition of *Au*. As the electrodeposited *Au* has higher roughness than the evaporated *Au*, this further increased the adhesion of pillars on the *Au*. With the increased interconnect material thickness, the at the edges and at the corners compared to the pillars situated at the center of the wafer [24]. This is due to the so-called edge effects where the current density is higher at the edges than in the middle, resulting in faster growth of the pillars at the edge area of the wafer. This height variation resulted in insufficient

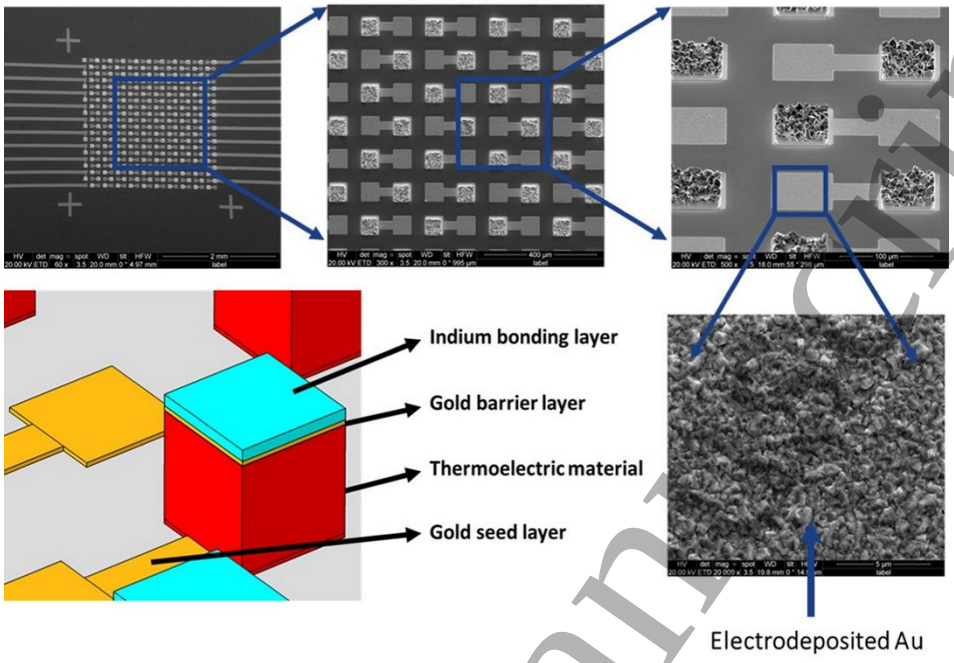


Figure 4: Schematic of sequential electrodeposited materials on the *Au* seed, reprinted from [20] with permission from IEEE.

TE materials, the barrier separation layer, and the bonding materials were electrodeposited on the patterned substrate as shown in Figure 4. The individual thicknesses of the electrochemically deposited materials are listed in Table 1.

Table 1: Individual material thickness of electrochemically deposited materials.

Material	Thickness
Interconnect material	3 µm
TE material thickness	10 µm
Indium thickness	3 µm
Barrier separation thickness	200 nm

However, there were issues during the electroplating of the thermoelectric materials, which led to electrically disconnected structures after the bonding. This issue was due to the difference in height of the electrochemically deposited pillars across the wafer. Figure 5 depicts the height difference of the thermoelectric pillars across each die on a wafer. The pillar heights of the TE materials need to be consistent for proper flip-chip bonding. The electroplated pillars were higher or no contact during the bonding process. The bonding process becomes more challenging when the pillar density is higher and cannot be neglected. Figure 6(a) shows the SEM image of an edge pillar after bonding where the top die was removed in order to analyze the bonding process. It can be seen from the image that the edge pillars were cracked and it appears that pillars are structurally not stable enough to take the bonding force. This was due to the dissimilar (higher in this case) height of the edge pillar, which took the entire load during bonding as the pillars from the central position did not share the bonding loads, leading to the fracture of the edge pillars. Therefore, it is imperative to address the die co-planarity or uniformity, which can be calculated according to equation (1), where Hmax and Hmin are the maximum and minimum heights of the pillars, respectively. The uniformity percentage should be less than 5% for good reliability [25], which is widely accepted in both the industrial and scientific community.

$$\text{Uniformity } (\%) = \frac{(H_{max} - H_{min})}{(H_{max} + H_{min})} \times 100 \qquad (1)$$

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In order to improve the uniformity, we have worked on different approaches. In particular, the use of additives in the electrolytic bath can help to achieve a uniform growth across the substrate. Levelers are preferentially attracted to the regions of higher current density, where they suppress the electroplating rate and create a more uniform array of pillars. However, it should be mentioned that this approach can influence the TE properties of the pillars. To reduce the complexity, we have taken an alternative approach to address this issue by increasing the thickness of the bonding material, which can compensate the height differences across the pillars. We selected *In* as a bonding material, as *In* metal is malleable and can deform easily acquiring the required shape at the applied bonding temperature and the bonding force. However, the risk of overflow of *In* will always be an issue as shown in Figure 6(b). This overflow of *In* can be minimized by the optimization of the *In* height and the bonding forces during the flip-chip bonding of the device.

The SEM image in Figure 6(b) depicts *In* acting as a bonding material on the second bonding wafer with the overflowed *In* metal around the pillars. We can also observe the non-adherence nature of *In* with the *Au*. We assume that this can be due to a thin layer of InO_2 formation over the *In* bumps, which restricts the formation of *Au-In* bonding. To address this issue, a thin layer of 50 nm of *Au* is electrodeposited over the *In* bumps to protect the *In* from oxidation during the flip-chip bonding process at the elevated temperature. As explained in the experimental section, *In* bumps were electrodeposited on both the wafers. This leads to an *In-In* bonding during the bonding process. The optimized bonding parameters are listed in Table 2.

4.2 Structural and electrical characterizations

This section discusses the structural and initial electrical characterizations of the fabricated micro thermoelectric device. After addressing and overcoming various challenges,

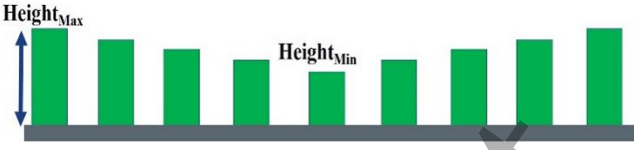


Figure 5: Schematic sketch of the non-uniformity in the electrodeposited pillar height.

the device was fabricated by flip-chip bonding. The bonding was performed at a temperature of 200 °C for 60 s with 300 gf under a continuous nitrogen flow in order to minimize the oxide formation at the elevated temperatures. The heating and cooling rates during the bonding were set at 5 °C/sec. A fully processed, µ-thermoelectric device consists of 210 pairs of p- and n-type TE pillars, connected thermally in parallel and electrically in series as shown in Figure 7. The images were taken using a Nordson Dage Diamond XD7600NT, X-ray Imaging system. The images reveal the underlying top view features through the top silicon substrate. A perfect alignment of both the dies to form an electrical contact of the device and the formation of the daisy chain can be seen in Figure 7. However, a slight overflow of the *In* metal is visible near the edges of pillars, which is significant. Even though there seems to be an overflow of *In* in the pillars at the edges, there has been no visible contact with immediate pillars in the vicinity, which might be deleterious as it will short-circuit the entire device. In order to thoroughly investigate the overflow of *In*, cross-sectional images were recorded.

Table 2: Bonding parameters used in the flip-chip bonding process.

Bonding parameters	Values
Bonding force	250-500 gf

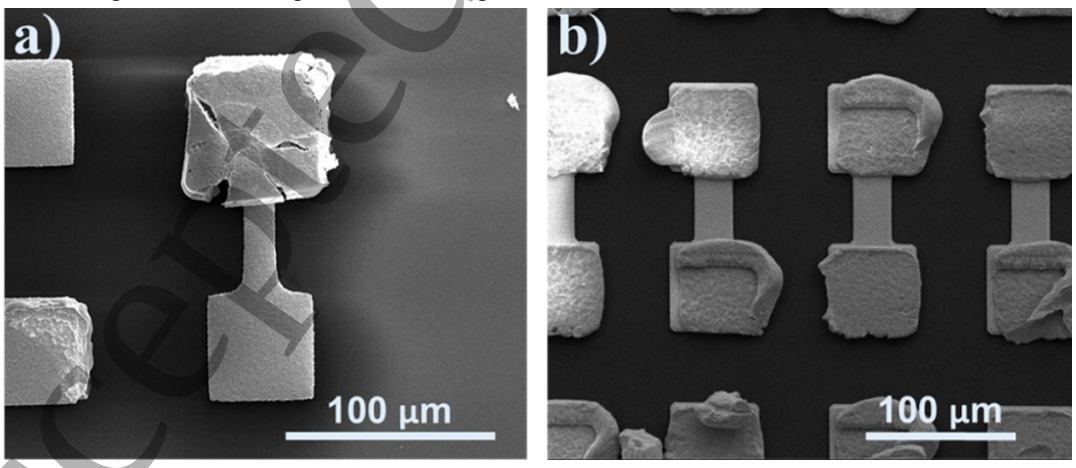


Figure 6: The SEM image of (a) an edge pillar after applying a bonding force, (b) electrodeposited *In* bumps after bond forces are applied.

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Temperature	160 – 200 °C
Atmosphere	Nitrogen
Time	60-120 s

observed as anticipated due to excess *In* owing to the pillar height differences across the substrate. However, this overflowed *In* does not short-circuit the connection as observed from Figure 8. Additionally, the *In* bond formed at the center pillars is perfect without any overflow suggesting an optimized bonding force applied.

Measuring the overall resistance of the fabricated thermoelectric device ensures that all the contacts are formed

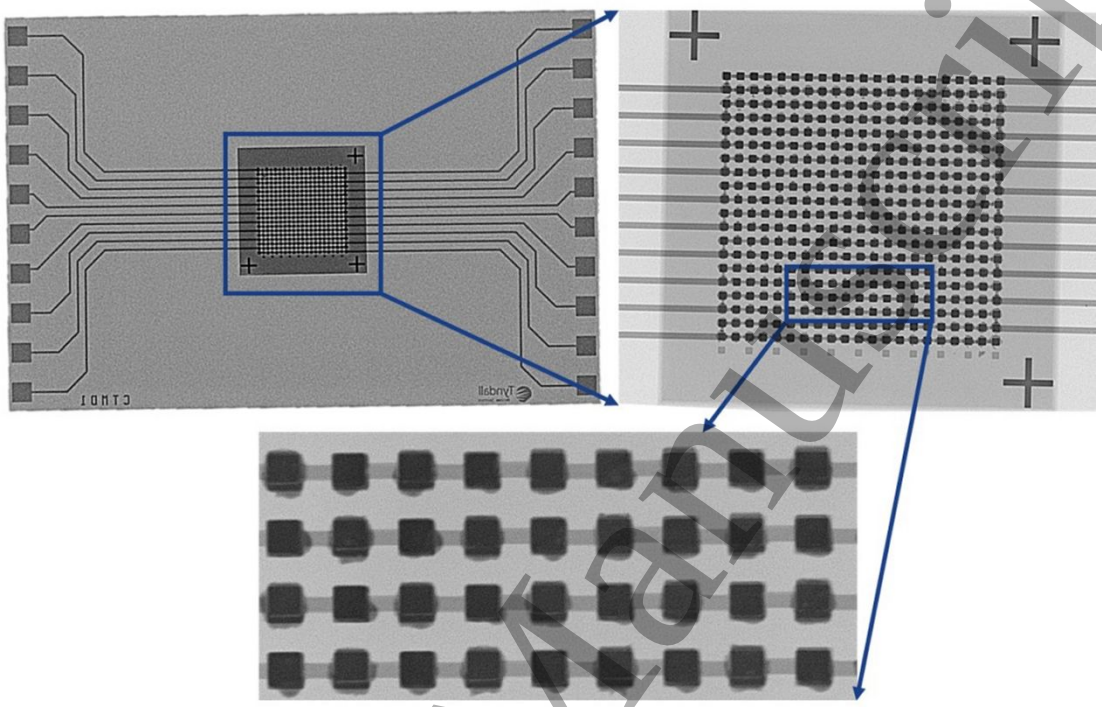


Figure 7: Images of the device using Nordson Dage Diamond XD7600NT X-ray Imaging system.

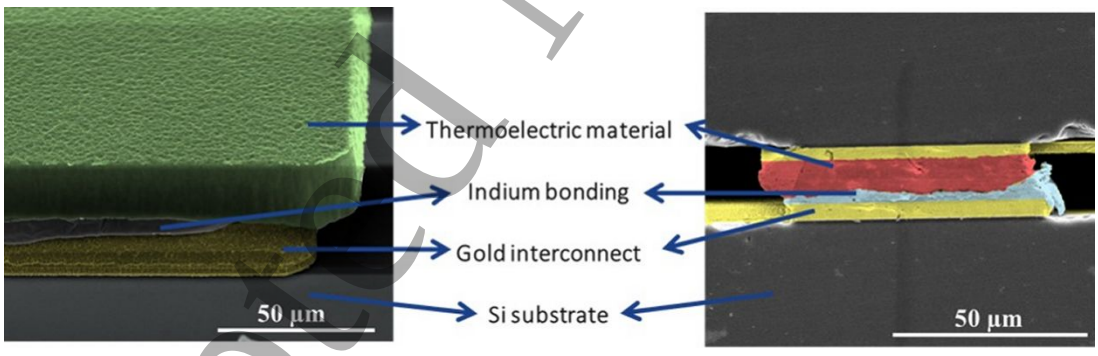


Figure 8: SEM images of the flip-chip bonded device using FineTech flip-chip bonder.

Figure 8 shows the vertical cross-sectional SEM image of the flip-chip bonded device ensuring the bond formation. The gap between the top and the bottom substrates is approximately 20 µm. The *In* bonding material holding the *Au* interconnect metal and the thermoelectric pillar forms an electrical contact between both the materials. The image is taken at the edge pillar, where the possibility of overflowing *In* is maximum due to the height difference of the pillars. From the SEM images, a slight overflow of *In* can be clearly after the flip-chip bonding. The device was designed in such a way that the electrical resistance can be measured for every 22 pairs. The electrical resistance of the device with respect to the number of pillars is plotted in Figure 9. Also, the resistance of single thermoelectric pair was calculated using the materials property in order to estimate the contact resistances formed during the bonding of the materials. The internal resistance of the thermoelectric pillar pair R_d is the sum of the material resistance (R_p+R_n), interconnect material resistance (R_{Au}) and

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the interfacial resistance of the flip-chip bonded joints (R_{Au}+R_{In}) as shown in Figure 10(a). The photograph of a flip-chip bonded device is shown in Figure 10(b). The material resistance (R_p+R_n) comprises of the resistance from the CuTe and the BiTe pillars, interconnect material resistance (R_{Au}) is the electrical resistance from the electrodeposited *Au* and the interfacial resistance (R_{Au}+R_{In}) corresponds to the resistance by the *In-Au* joint after the bonding.

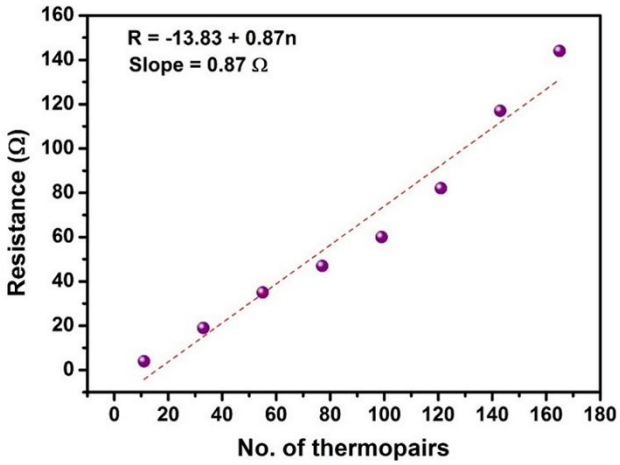


Figure 9: Measured electrical resistance of the flip-chip bonded device.

The average measured electrical resistance of a single thermoelectric pair is 0.87 Ω deduced from the electrical resistance measured on the complete device after performing a linear fit on the obtained values. The deviation of the measured resistances in the plot arises from the change in the distance of the *Au* pads from the pillars to the measuring pads.

The measuring pad itself adds resistance during the measurements, and this resistance will be high for a longer bond pad compared to the shorter pad (see Figure 7). The decrease in the resistance measured can only be seen when the measurements are done using the shorted bond pads as seen in Figure 9. This ensures that the measured electrical resistance is same throughout the device and confirms the homogeneous bond formation over the complete device. The calculated resistance of a thermoelectric pair using material properties is 0.45 Ω, which is 48% lower than the measured value. This higher measured value is due to the contact resistances [3R_{Au}+ 2(R_{Au}+R_{In})] between the p-n leg pairs.

In order to check the functionality of the thermoelectric device, two thermocouples were attached at the top and bottom of the device. A temperature gradient was created using two commercially available Peltier coolers placed over and under the device. A voltage of 90 mV was measured for a temperature difference of 10 K from 60 active TE pairs. This measurement when extrapolated for a complete device using 210 TE pairs, projects a voltage generation of about 315 mV, which indicates a contribution of 143.1 µV/K from each TE pair. This Seebeck coefficient value is, however, lower than the values of individual p and n-type TE films. The lower values compared to the individual materials might stem from the thermal losses at the device interface and not accurate temperature determination in the micro-thermoelectric device in addition to the interfacial electrical losses. However, the calculations were done assuming a negligible thermal loss in the substrate and at the interface between the thermoelectric material and the interconnect material. Further work is required to precisely analyze the device and evaluate the reasons for the measured lower values of the overall device voltage. Additionally, the complete device characterization over a range of temperature interval has to be measured in future.

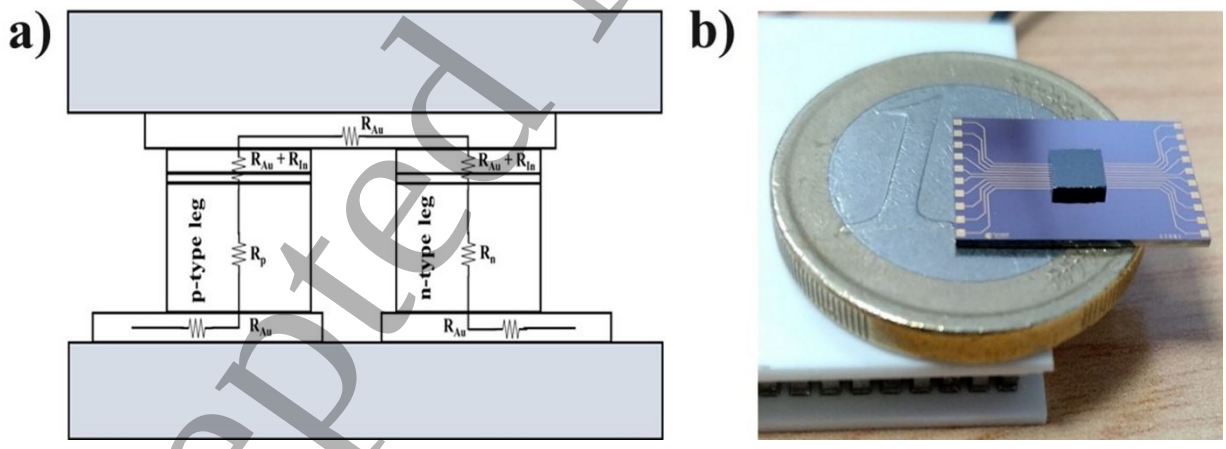


Figure 10: a) The schematic of internal resistances of thermoelectric pillar pair, b) Flip-chip bonded µ-TED device.

5. Conclusions

A micro-thermoelectric device with 210 pairs of thermopiles was fabricated using the flip-chip bonding that are

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connected electrically in series and thermally in parallel on the silicon substrate. Here, we demonstrate and discuss the challenges encountered during the fabrication of a thermoelectric device using flip-chip bonding approach and the solutions employed to overcome these challenges to minimize the processing steps, which leads to the reduction of overall fabrication cost. Different problems, namely adherence issues, delamination, bonding, edge effects, and structural stability are discussed. Cross-sectional characterization reveals that the overflow of In bonding metal does not short-circuit the device. The electrical resistance of the complete device with 210 pairs of thermocouples was about 182.7 Ω, which gives an average electrical resistance of 0.87 Ω for individual thermoelectric pair. The resistance of a single thermopile is higher than the calculated value using material properties, which is due to the contact resistance of the bonding materials. A thermoelectric voltage of about 90 mV is generated when the device with 60 active thermopile pairs was subjected to a temperature gradient of 10 K. Future studies will analyze and evaluate the device performance including the complete thermoelectric characterization.

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