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Stress in silicon interlayers at the SiO_x/Ge interface

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Materials such as germanium display an advantage relative to silicon in terms of carrier mobilities but form poor quality interfaces to oxides. By sandwiching silicon layers between a germanium substrate and the oxide, advantages of the silicon oxide/silicon (SiO_x/Si) interface can be retained combined with the advantage of a high mobility germanium substrate. Using density functional theory calculations, stress within the silicon interlayer is quantified for different interlayer thicknesses revealing that for up to three silicon layers, the stress in the interlayer is compensated for by the energy gained by forming silicon-oxygen bonds at the interface. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2713122]

Growth of semiconductor materials at atomic layer resolution offers unique opportunities for tailoring layer by layer the substrates used in microelectronics and other applications. One such approach is to use silicon interlayers at the semiconductor/oxide interface with germanium substrates, in particular, to reduce interface state densities.[1–3] Alongside oxides on III-V materials, germanium has been studied in conjunction with high-k oxides.[4–7] The advantages of silicon interlayer passivation on germanium metal-oxide-semiconductor (MOS) devices has recently been demonstrated[8] with improvements in the electrical characteristics for devices in terms of interface state density, low capacitance-voltage hysteresis and frequency dispersion, and low gate leakage current density.

Silicon layers on germanium are under tensile strain due to the lattice mismatch and the resulting strain profiles for heterostructures are well understood both experimentally and theoretically. However, the effects of oxidation on strain in silicon and germanium multilayers is not as well understood.[9] In this computational study, we investigate the effect of silicon interlayers on strain relaxation based on models for thin SiO_x layers on silicon;[10] these models are developed by bonding silica in β-tridymite form to a silicon (001) surface; similar models have been developed for the Si (110) and (111) surfaces.[11] Computations are performed using the plane-wave density functional theory program VASP (Ref. 12) using the gradient corrected PW91 (Ref. 13) exchange-correlation potential and ultrasoft atomic pseudopotentials.[14] The plane-wave basis set is chosen with a 395 eV energy cutoff. The convergence for self-consistent steps is accurate to within 10^{-4} eV/system. For SiO_x on silicon models, the lattice constants parallel to the interface are held fixed at the silicon bulk equilibrium value determined from PW91 calculations. Likewise for SiO_x on germanium models, the lattice constants parallel to the interface are held at the PW91 germanium bulk equilibrium value: this remains true when silicon interlayers are introduced as the goal is to model interlayers on a germanium substrate.

To create the SiO_x/Ge interface, the nonbridging structure of Ref. 10 is modified by substituting all substrate Si atoms with Ge, and cell dimensions parallel to the interface are then set to the bulk germanium equilibrium value. The oxide density and residual strain are thus not equivalent to those of the initial SiO_x/Si model. In this idealized case, the surface bonds to the oxide layer are similar to those for a silicon substrate, with the difference that the surface bond density to the oxide is reduced due to germanium's larger lattice size. For these cell sizes, a $2\times2\times1$ k-point mesh is used. To investigate the artifical strain built into the oxide layers by the simulation cell constraints, larger simulation cells are studied: a SiO_x/Si model (208 Si, 112 O atoms) generated from $2\times2\times1$ cells of the original silicon oxide interface model (52 Si, 28 O atoms) (Ref. 10) and a corresponding $2\times2\times1$ model with germanium substrate (48 Si, 160 Ge, 112 O atoms) built using the $1\times1\times1$ model with silicon substrate atoms replaced by germanium (12 Si, 40 Ge, 28 O atoms). For these larger cells, a $3\times3\times1$ k-point mesh is used. The $2\times2\times1$ simulation cells allow for more internal degrees of freedom and the oxide can further relax relative to the smaller cells. For the $2\times2\times1$ SiO_x/Si and SiO_x/Ge models, an annealing procedure was applied using *ab initio* molecular dynamics to allow the oxide layers to reduce residual stress. The annealing schedule consists of two cycles: the first consists of a starting temperature of 833 K, total simulation time of 67.5 fs, and a final temperature of 398 K; the second cycle consists of a starting temperature of 1223 K, total simulation time of 260 fs, and a final temperature of 825 K. In both cycles, the time step is held fixed at 1.3 fs. Following the anneals, a geometry optimization ("quench") is performed.

Comparing bond length distributions between the $1\times1\times1$ and $2\times2\times1$ SiO_x/Si cells, it is clear that frustration has been introduced using the smaller cell, with oxide bonds typically several picometers shorter for the smaller model. Generally speaking for the larger SiO_x/Si model, the bonds are able to increase slightly in length relative to the smaller cell, indicating compression is introduced using the smaller simulation cell. Similarly, comparing the two SiO_x/Ge models, there are differences in the bond length distributions. At longer Si–O bond lengths, the $1\times1\times1$ cell with a germanium substrate shows an increase in bond lengths relative to the $2\times2\times1$ cell, again suggesting that the smaller simulation cell introduces artificial constraints for the oxide. Comparing results between the two large simulation cells, we note that the germanium substrate produces a relative lengthening of the oxide bonds relative to the equivalent simulation for a silicon substrate. The germanium results indicate a quasicontinuous distribution, whereas the

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bond length distribution in the oxide layer with the silicon substrate displays two jumps in the distribution at longer bond lengths—this suggests that even in the larger cell with a silicon substrate, residual strain induced by the finite cell size persists.

The energies for the $1\times1\times1$ simulation cells compared to the larger $2\times2\times1$ models can be quantified relative to the cross sectional area of each cell. For the SiO_x/Si interface, the difference between cells results in a difference in energy per unit area of 11 meV/Å^2. For the SiO_x/Ge system, the difference in energy per unit area is 16 meV/Å^2. This comparison between the cells reveals the energies due to strain relaxation, and computational differences for the two cell sizes compensate to within a few tens of meV/Å^2. This is an order of magnitude smaller than the interface energies we consider. Thus the $1\times1\times1$ simulation cells are as accurate for our purposes as the larger $2\times2\times1$ cells. The simulation cell in Ref. 10 is based on a ten layer silicon substrate. We have repeated our calculations using a 22 layer substrate for three, seven, and ten layer Si interlayers and have found no significant changes in our energies or calculated stresses. Subsequent calculation of surface energies are based on the $1\times1\times1$ cell results with a ten layer model substrate. Introduction of a silicon interlayer introduces an additional energy at the Si/Ge interface. This interface energy has been computed from a 32 atom simulation cell and found to be an order of magnitude smaller than the chemical and strain effects caused by the interlayer.

Most bond lengths using germanium substrate models lie above those calculated from the silicon substrate model, reflecting a "stretching" of the oxide due to the larger germanium lattice constant relative to silicon. However, introducing the silicon interlayer allows the oxide to relax back toward its form for the SiO_x/Si model, particularly for longer Si–O bonds.

In Fig. 1, semiconductor-semiconductor bond lengths within the substrate are compared for 3 and 7 ML interlayers; Si–Si and Ge–Ge bond lengths from similar calculations for bulk silicon and germanium are given for reference. Upon introduction of the silicon interlayer, three types of substrate bonds are formed: Si–Si, Si–Ge and Ge–Ge. From the bond length distributions it is seen that relatively little strain is introduced into the germanium substrate, but the Si–Si bonds within the interlayer are highly strained, tending towards the bulk Ge–Ge bond length.

The interface bonds between the semiconductor layer and the oxide indicate that, from a chemical perspective, the interlayer acts similarly to a silicon substrate. For the SiO_x/Si model, the interface bonds R_{Si-O} range between 1.665 and 1.675 Å in length. At the germanium interface within the SiO_x/Ge model, the corresponding R_{Ge-O} range from 1.805 to 1.813 Å. After introduction of a single silicon monolayer at the interlayer, the interface R_{Si-O} reduce to 1.665 and 1.672 Å.

Finally, the relative stress between the SiO_x/Si and SiO_x/Ge models is considered. The surface or interface energy is defined relative to a reference system as

$$\Delta E_{SiO_x/X} = E_{SiO_x/X} - n_X E(X) - n_{O_2} E(O_2) - n_{H_2O} E(H_2O), \tag{1}$$

with X=Si or Ge, n_X the number of Si and/or Ge atoms in the cell, $E(X)$ the energy per atom in the bulk, n_{O_2} and n_{H_2O} the numbers of reference molecules used to balance the number of oxygen and terminating hydrogen atoms in the simulation cell, and $E(O_2)$ and $E(H_2O)$ the energies of the reference molecules. Similarly, if atoms are substituted within the germanium simulation cell to form a silicon interlayer, a corresponding difference energy may be calculated by correcting for the number of semiconductor (Si/Ge) atoms contained within the cell. Surface energies were also calculated relative to the relaxed SiO_x/Si cell balanced by the number of silicon and germanium atoms in the substrate; relative surface energies using the two different reference systems agree within the errors expected from our density functional theory calculations.

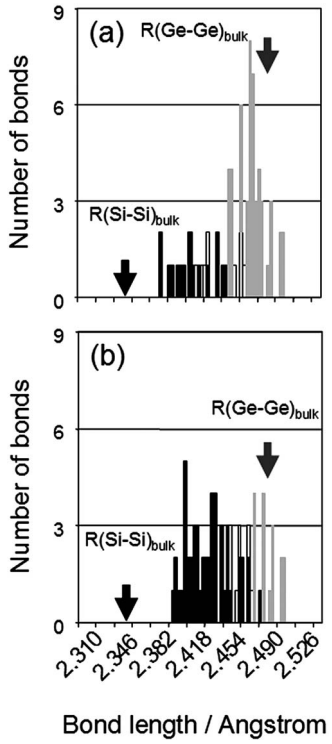


FIG. 1. Comparision of bond length distributions in the substrate for (a) 3 ML silicon interlayer and (b) 7 ML silicon interlayer. The large arrows mark the Si–Si and Ge–Ge bulk bond lengths for reference. Black: Si–Si, gray: Ge–Ge, void: Si–Ge.

In Fig. 2, the computed stress is shown as a function of interlayer thickness. Our assumption based on the bond analysis is that the majority of the strain resides within the interlayer. To calculate relative stress, the surface energies for the SiO_x/Si/Ge and SiO_x/Si interfaces are used to determine an energy difference ΔE. We *assume* that this energy difference corresponds to the work used to strain the silicon interlayer with the magnitude of the strain determined from the difference between the cell dimensions for relaxed silicon and germanium substrates. This allows us to define a force on each face of the interlayer which relates to stress as force per unit area, $\sigma=F/A$. The relative stress is then determined from the relative energy and volume of the silicon interlayer. The relationship between stress and volume is shown, re-expressed as a function of the number of silicon layers, within Fig. 2.

For thicker silicon interlayers, the stress approaches a maximum value of approximately 6.8 GPa. Constant stress implies that the SiO_x/Si/Ge surface behaves according to the relation $\sigma=F/A$ as the number of interlayers increases. As

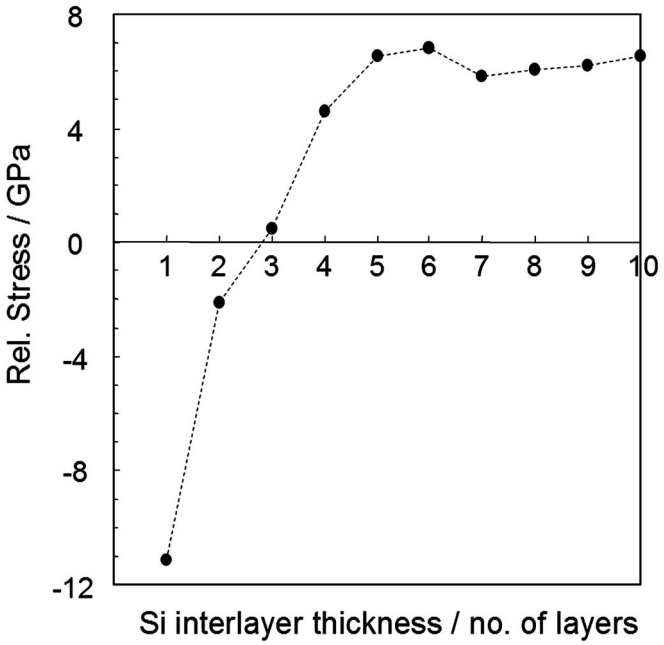


FIG. 2. Relative stress as a function of silicon monolayers used to build the interlayer. Reference system: SiO_x/Si.

the area increases, there is a linear elastic response due to the interlayer undergoing biaxial tensile strain. For the constant stress region, stress in the interlayer dominates the relative interfacial energy. For thinner interlayers, it can be seen that the relative stress is not constant (or positive). The assumptions of the mechanical model are not adequate to describe the interface energies for interlayer thicknesses of two or three layers.

Generally, oxides on the silicon (001) surface are under compressive strain.[15] In contradiction, we find that the interface energy for SiO_x/Ge is larger than for SiO_x/Si within our model system. Next by introducing a single silicon interlayer at the oxide interface within the SiO_x/Ge simulation cell, the interface bonding changes from Si–O–Ge to Si–O–Si. The energy associated with this new interfacial bonding, the so-called chemical stress,[11] results in a lower relative interface energy due to Si–O bonds replacing Ge–O bonds. The introduction of a single silicon interlayer is found to be energetically favorable against SiO_x/Ge and slightly favorable against SiO_x/Si for this interface model.[10] As the number of silicon layers increases, the mechanical stress in the interlayer increases, compensating the chemical stress but resulting in interface energies comparable to the SiO_x/Si reference system for one, two or three silicon interlayer thicknesses.

It is interesting to note that our analysis indicates that after thickness of four layers, the silicon interlayer begins to behave as a continuum layer undergoing tensile strain. This permits our relative stress estimates to be checked against similar estimates based on bulk and Young moduli for silicon. If values appropriate for defect-free crystalline silicon for the bulk modulus of $B=100$ GPa and Young's modulus of $Y=150$ GPa (Ref. 16) are used, stress estimates within the interlayer range between 9 and 12 GPa, comparable to our estimate of 6–7 GPa. However, note that all of these stresses are higher than or comparable to the fracture strength of defect-free silicon of approximately 7 GPa (Ref. 17) and significantly higher than the typical values of several hundred megapascals found for processed silicon.

Hence the following picture for the interlayer emerges. For interlayers composed of one, two or three silicon layers, the favorable chemical energy due to interfacial bonding compensates against increased mechanical stress arising between the silicon and germanium lattice mismatch. As the interlayer thickness increases, the interface energy rises due to increasing mechanical stress and returns to the energy of the SiO_x/Ge interface energy at a thickness of approximately six silicon layers. However, for thicknesses greater than four silicon layers, the stress in the interlayer approaches the fracture strength of silicon, suggesting that the interlayer becomes mechanically unstable, consistent with estimates for the critical thickness of silicon on germanium.

Interfacial stress correlates to defect densities, and the silicon/silicon oxide sets the standard for an acceptable defect density in microelectronic applications. Our work shows that formation of oxide/semiconductor interfaces with germanium can be engineered using silicon interlayers to have effectively the same properties as the Si/SiO_x interface, thus introducing the possibility of high quality semiconductor/oxide interfaces using germanium substrates. In addition to defect densities, roughness scattering is also an important criterion for evaluating the quality of an interface. Producing a Si/SiO_x quality interface with germanium substrates offers the potential for higher mobility devices relative to the Si/SiO_x reference system.

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[1] G. G. Fountain, R. A. Rudder, S. V. Hattangady, D. J. Vitkavage, R. J. Markunas, and J. B. Posthill, Electron. Lett. **24**, 1010 (1988).
[2] S. V. Hattangady, M. J. Mantini, G. G. Fountain, R. A. Rudder, and R. J. Markunas, J. Appl. Phys. **71**, 3842 (1992).
[3] Y. Wang, Y. Z. Hu, and E. A. Irene, J. Vac. Sci. Technol. B **14**, 1687 (1996).
[4] E. P. Gusev, H. Shang, M. Copel, M. Gribelyuk, C. D'Emic, P. Kozlowski, and T. Zabel, Appl. Phys. Lett. **85**, 2334 (2004).
[5] V. V. Afanas'ev and S. Stesmans, Appl. Phys. Lett. **84**, 2319 (2004).
[6] N. Wu, Q. C. Zhang, C. X. Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, A. Chin, and D. L. Kwong, Appl. Phys. Lett. **85**, 4127 (2004).
[7] J. P. Xu, P. T. Lai, C. X. Li, X. Zou, and C. L. Chan, IEEE Electron Device Lett. **27**, 439 (2006).
[8] W. P. Bai, N. Lu, and D. L. Kwong, IEEE Electron Device Lett. **26**, 378 (2005).
[9] A. A. Al-Falou, M. Kammler, and M. H. V. Hoegen, Europhys. Lett. **69**, 570 (2005).
[10] A. Pasquarello, M. S. Hybertsen, and R. Car, Phys. Rev. Lett. **74**, 1024 (1995); Appl. Phys. Lett. **68**, 625 (1996).
[11] A. Korkin, J. C. Greer, G. Bersuker, V. Karasiev, and R. J. Bartlett, Phys. Rev. B **73**, 165312 (2006).
[12] G. Kresse and J. Hafner, Phys. Rev. B **49**, 14251 (1994).
[13] J. P. Perdew, J. A. Chevary, S. H. Vosko, K. A. Jackson, M. R. Pederson, D. J. Singh, and C. Fiolhais, Phys. Rev. B **46**, 6671 (1992).
[14] D. Vanderbilt, Phys. Rev. B **85**, 7892 (1990).
[15] L. E. Katz, in *VLSI Technology*, edited by S. M. Sze (McGraw-Hill, New York, 1983), pp. 131–168.
[16] V. L. Spiering, S. Bouwstra, and R. Spiering, Sens. Actuators, A **39**, 149 (1993).
[17] K. E. Petersen, Proc. IEEE **70**, 420 (1982).