Chemical Approaches for Doping Nanodevice Architectures

John O'Connell[†+ϕ], Subhajit Biswas[†+ϕ], Ray Duffy[+] and Justin D. Holmes[†+ϕ*]

[†]Department of Chemistry, University College Cork, Cork, Ireland. [+]Tyndall National Institute, University College Cork, Cork, Ireland. [ϕ]AMBER@CRANN, Trinity College Dublin, Dublin 2, Ireland.

*To whom correspondence should be addressed: Tel: +353 (0)21 4903608; Fax: +353 (0)21 4274097; E-mail: ray.duffy@tyndall.ie; j.holmes@ucc.ie

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Abstract

Advanced doping technologies are key for the continued scaling of semiconductor devices and the maintenance of device performance beyond the 14 nm technology node. Due to limitations of conventional ion-beam implantation with thin body and 3D device geometries, techniques which allow precise control over dopant diffusion and concentration, in addition to excellent conformality on 3D device surfaces, are required. Spin-on doping has shown promise as a conventional technique for doping new materials, particularly through application with other dopant methods, but may not be suitable for conformal doping of nanostructures. Additionally, residues remain after most spin-on-doping processes which are often difficult to remove. In-situ doping of nanostructures is especially common for bottom-up grown nanostructures but problems associated with concentration gradients and morphology changes are commonly experienced. Monolayer doping (MLD) has been shown to satisfy the requirements for extended defect-free, conformal and controllable doping on many materials ranging from traditional silicon and germanium devices to emerging replacement materials such as III-V compounds but challenges still remain, especially with regard to metrology and surface chemistry at such small feature sizes. This article summarises and critically assesses developments over the last number of years regarding the application of gas and solution phase techniques to dope silicon-, germanium- and III-V-based materials and nanostructures to obtain shallow diffusion depths coupled with high carrier concentrations and abrupt junctions.

Introduction

Semiconductor materials have long been the driving force for the advancement of technology since their inception in the mid-20th century. Traditionally, micro-electronic devices based upon these materials have scaled down in size and doubled in transistor density in accordance with the well-known Moore's law, enabling consumer products with outstanding computational power at lower costs and with smaller footprints. According to the International Technology Roadmap for Semiconductors (ITRS), the scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) is proceeding at a rapid pace and will reach sub-10 nm dimensions in the coming years.[1] This scaling presents many challenges, not only in terms of metrology but also in terms of the material preparation especially with respect to doping which has led to the moniker "More-than-Moore". Current transistor technologies are based on the use of semiconductor junctions formed by the introduction of dopant atoms into the material using various methodologies and at device sizes below 10 nm, high concentration gradients become a necessity. Doping, the controlled and purposeful addition of impurities to a semiconductor, is one of the most important steps in the material preparation, with uniform and confined doping to form ultra-shallow junctions (USJs) at source and drain extension regions being one of the key enablers for the continued scaling of devices. Conventionally, ion implantation has been the method of choice for doping of devices but the technique suffers from a number of drawbacks which make it inefficient and ineffective at sub-10 nm dimensions. The ion implantation process is inherently high-energy due to the acceleration of the ions towards the semiconductor surface at tens to hundreds of keV. This bombardment of the of the surface causes damage to the crystal structure of the semiconductor which must be rectified with a further annealing step. While the dose and concentration may be finely regulated, the spatial distribution of the implanted ions is extremely difficult to control in

addition to the problem of controlling depth and abruptness within 1 nm. Combined with the general incompatibility of ion implantation with 3D nanostructured materials, there is a clear need for new doping methodologies to counter these drawbacks.

Due to the ubiquity of Si, the application of MLD on Si is discussed first with initial focus on approaches involving the use of B- and P-containing molecules in conjunction with conventional rapid-thermal-anneal processes and spike annealing processes. The MLD process can be divided broadly into studies on oxide-free Si surfaces and non-deglazed Si surfaces. Variations of this process such as contact-doping are also discussed. This initial approach is developed in further studies to incorporate scale-up to 100 mm Si wafers and then on to 300 mm wafers. Application of the MLD process to potential future channel materials such as InGaAs and Ge is subsequently discussed. The latter sections of the review discuss the application of wet-chemical hybrid spin-on doping on Si and Ge as a means to realise shallow and high-concentration junctions for future device structures.

Monolayer doping on Si

Monolayer doping is one potential technique for the replacement of ion-implantation. MLD comprises two steps: (1) functionalization of a semiconductor surface with a *p*- or *n*- dopant-containing molecule and (2) subsequent diffusion of the surface-bound, chemisorbed dopant atoms into the semiconductor material *via* a rapid-thermal-anneal step. The functionalisation step is most commonly a thermally-initiated hydrosilylation reaction between a hydrogen-passivated semiconductor surface and a labile C=C site on the dopant-containing molecule. Due to the rich and established chemistry that can be carried out on the semiconductor surfaces, many aspects of the MLD process such as the initial surface preparations, molecular footprints, choice of capping layer and the rapid-thermal-anneal recipe can all be optimised and tailored to the particular process,

material and required dopant concentration and depth.[2–12] **Figure 1** displays an example of a typical MLD process using commercially available triallylphosphine.

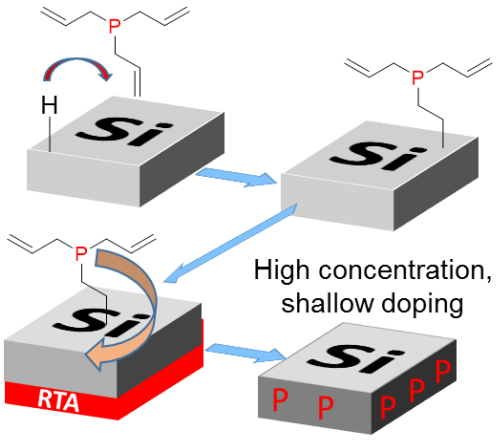

Figure 1. Schematic depicting a typical phosphorus MLD process. A hydrosilylation reaction occurs between a reactive H-passivated Si surface and the labile C=C site on the dopant containing molecule, in this case triallylphosphine, resulting in a covalently bonded molecular layer. The samples are then capped with 50 nm of SiO_2 and subjected to a rapid-thermal-anneal (RTA) step resulting in high concentration, shallow doping of silicon.

Ho *et al.* were the first to report the MLD process on Si where allylboronic acid pinacol ester in a 25 % v/v solution in mesitylene was used to passivate a H-terminated Si surface with a boron-containing monolayer.[13] A standard rapid-thermal-anneal recipe of temperatures between 950 – 1000 ^{o}C temperature for 5 seconds was used. For ultra-shallow junctions, shorter times at a given temperature are required to supress transient-enhanced diffusion and therefore reduce the final dopant diffusion depth. Bulk blanket substrates of Si exhibited B concentrations approaching 5×10^{20} cm^{-3}, with this concentration decreasing sharply to 10^{17} cm^{-3} at depths of 18 nm for a sample annealed at 950 ^{o}C and 43 nm for a sample annealed at 1000 ^{o}C.

Ho and co-workers also applied the MLD process to chemically intrinsic, bottom-up grown nanowires in the same study using a Ti/Al source and drain contacts to form a two-terminal device. Pre-MLD nanowires exhibited resistances on the order of 100 GΩ, partly due to the large Schottky barrier at the metal-nanowire interface. Post-MLD nanowires, while showing a significantly lower resistance of 2 MΩ, still displayed quite a high resistance overall due to the Schottky barriers at the metal-wire interface. The MLD process was also applied to silicon-on-insulator (SOI) substrates in order to fabricate field-effect transistors (FETs). The impact of MLD on the as-fabricated FET electrical characteristics was stark, with undoped tungsten contacts delivering ~ 0.1 μA at 0.5 V. This observation of lower resistance and improved switching properties can be attributed to the thinning of the Schottky barrier at the metal-SOI interfaces. In the same study, Ho functionalised Si with two P-containing molecules, diethyl 1-propyl phosphonate (DPP) and trioctyl phosphine. (TOP) While chemical concentrations exceeding 1×10^{21} atoms/cm^3 were achieved, the bonding mechanism between the DPP and TOP molecules and the Si surface was quite unclear and not very well characterised and will need to be explored further in order to ascertain surface coverage and molecular packing.

This seminal work laid the foundations for future research into MLD but still left many avenues to be explored especially with regard to fine tuning of molecular footprints, the role of carbon-incorporation from the organic molecular precursors, rapid-thermal-anneal parameters, more detailed surface analysis and more complex device characterisation in addition to ensuring the defect-free nature of the nanostructures post-MLD.

Indeed, in further work by Ho and co-workers, to investigate the role of anneal temperature and duration, a similar MLD process was applied on a larger, 4 inch wafer-scale but this time using spike-annealing *i.e.* a high temperature anneal with a dwell time of less than 1s at the target

temperature with a fast ramp-up and ramp-down time, instead of a conventional rapid-thermal-anneal process.[14] For the phosphorus MLD process, surface doping concentrations of ~ 2.5×10^{20}, 3.5×10^{20}, 4×10^{20}, 5.5×10^{20} atoms/cm^3 were observed for 900, 950, 1000, 1050 °C spike anneal temperatures respectively.

Applying a boron-MLD procedure on a 4 inch wafer scale achieved sub-2 nm junction depths for spike anneals at 950-1050 °C. This is expected due to the lower diffusivity of B in Si. Unfortunately a large error is introduced when measuring the dopant diffusion depth at such shallow depths, as the resolution limit of SIMS becomes a limiting factor, again highlighting a need for metrology to catch up with the increasingly stringent characterisation requirements of ultra-shallow junctions. Potential effects of carbon incorporation during dopant diffusion were investigated using a non-contact photovoltage measurement as carbon will always be present at the surface during a SIMS analysis even with a pre-emptive cleaning step.[15] Average leakage currents were found to be much less than the then state-of-the art USJ leakage currents.[16]

With the ability to finely control the dopant diffusion depth and the effect of carbon found to be negligible a logical next step was to scale up the MLD process in order for it to be applied to a full size 300 mm wafer scale as found in the vast majority of the semiconductor manufacturing plants worldwide. Workers at CNSE Albany and SEMATECH first used phosphorus-MLD, using an unnamed P-based molecule, to conformally dope a 300 mm size wafer. In addition they also investigated the application of the P-MLD process to a small feature size (20 nm) FinFET.[17] Ang and co-workers subjected a H-terminated 300 mm Si wafer to a P-MLD process and following SiO_2 passivation utilised a spike anneal between 1000-1100 °C to cause in-diffusion of the dopant. Dopant concentrations for phosphorus achieved using the P-MLD process approached 1×10^{22} atoms/cm^3 at sub 5-nm depths.

An analogous process to that applied to the 300 mm wafers was applied to a FinFET with a fin width of ~20 nm and gate length of ~40 nm. The data obtained demonstrated that MLD permits the formation of uniform silicide contacts whilst maintaining a defect-free fin doping profile, which is advantageous when compared to an ion-implanted fin where a high density of defects is often observed due to implant damage. The damage caused by ion-implantation causes undesirable silicidation along the dislocation path and leads to poor quality silicide formation. This shows the ease with which the MLD process can be tuned in order to optimise the depth which the silicide resides within. Silicide uniformity is a crucial attribute to consider when delivering low parasitic fin resistance. Ang and co-workers demonstrated the application of the MLD process to pseudomorphic SiGe and Si eptaxial films with excellent single crystalline quality which showed significant enhancement over ion-implanted analogues. This makes MLD a very attractive alternative to traditional doping techniques.

The previously mentioned papers gradually built the foundations of MLD techniques through the use of well-established surface chemistries. Sample processing *i.e.* hydrosilylation, capping layer deposition and rapid thermal annealing generally occurred on a single substrate using a single dopant precursor molecule. However, reproducible device fabrication requires a combination of the initial MLD approach with an ability to laterally control the positioning of the molecular monolayer.

Signalling the beginning of a break away from traditional MLD, Voorthuijzen and co-workers combined the MLD process with nano-imprint lithography (NIL).[18] This work involved the utilisation of a method developed previously to directly pattern P-containing organic monolayers onto oxide-free silicon; using a combination of bottom-up monolayer formation and top-down nanoimprint lithography resulting in sub 100 nm highly-doped patterned regions.[19] A schematic

of the process used is shown in **Figure 2**. TOF-SIMS was used to ascertain dopant concentrations and also to image and depth-profile the highly-doped regions. The dopant surface dose on a doped section approached 2.3×10^{19} atoms/cm^3 which corresponded to an areal dose of approximately 5.6×10^{13} atoms/cm^2. Clear differences were observed in the resistances of the doped regions when the current was measured perpendicular to the regions and when measured parallel. Sheet resistance measurements were obtained using a four-point-probe The sheet resistance for an unpatterned sample (Rs) was found to be $7.6 \times 102\ \Omega$ whereas a value of $1.5 \times 103\ \Omega$ was obtained for a patterned sample. Doping efficiencies were extracted to be 26 % for a doped line and 50 % on a full unpatterned sample. This variation of the MLD process proves that, in principle at least, the positioning of the dopants can be laterally controlled which is important on smaller scale devices such as diodes, nanowires and FinFETs.

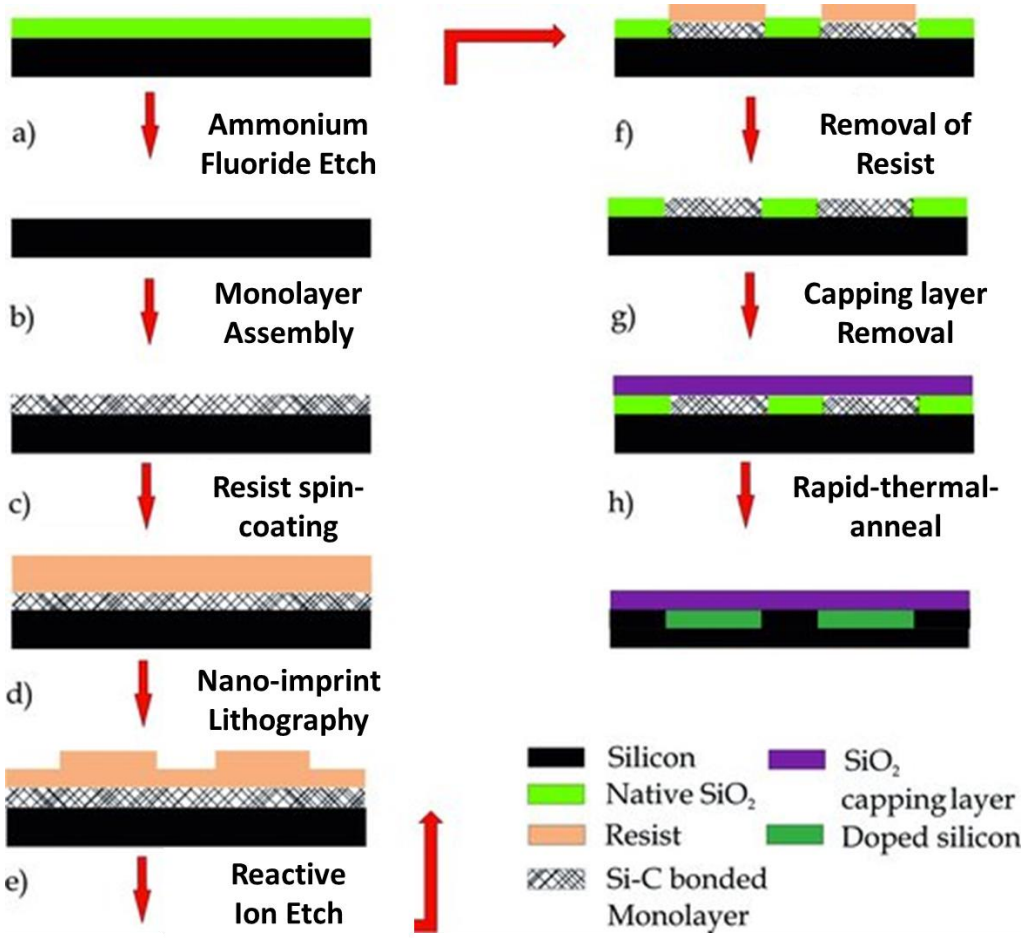

Figure 2. Process flow showing the MLD process combined with nano-imprint lithography. (a) Native oxide is removed by ammonium fluoride followed by (b) monolayer assembly using dopant-containing monolayer. (c) Spin coating of imprint resist. (d) Etch of residual layer by reactive ion etch. (f) Resist removal by sonication in acetone. (g) Deposition of SiO2 capping layer by e-beam evaporation. (h) Rapid thermal anneal treatment to cause dopant diffusion. Modified from ref: [18] Copyright 2011, John Wiley and Sons.

Hazut *et al.* introduced another variation of the MLD process termed monolayer contact doping (MLCD).[20] **Figure 3** shows a schematic representing the MLCD process.

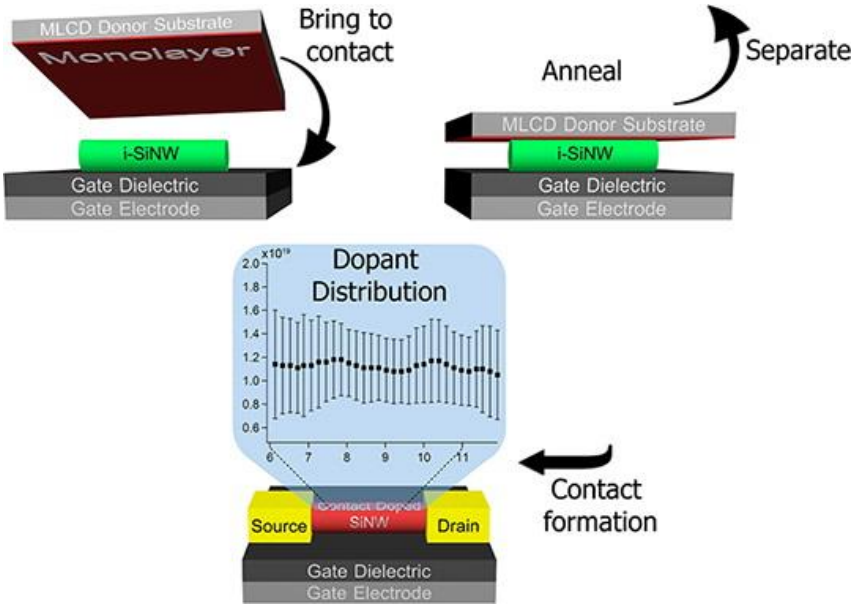

Figure 3. Schematic representation of the MLCD process. A dopant containing monolayer on a donor substrate is brought into contact with the substrate that is intended for doping and the two samples are annealed together. Undoped Si NWs may be sandwiched between the donor and acceptor substrates for controllable doping. Adapted with permission from ref: [20] Copyright 2012, American Chemical Society.

The work reported by Hazut *et al.*[20] involved the characteristic formation of the dopant-containing monolayer, not directly on the material, but on a "donor" substrate which was then brought into contact with an "acceptor" substrate that was intended for doping and both substrates are annealed together. The MLCD process utilised, in comparison to the traditional MLD process, did not require the deposition and removal of a SiO2 capping layer, but instead using more complex phosphine-oxide based molecules (diphenylphosphine oxide (DPPO), triphenylphosphine oxide (TPPO) and tetraethylmethylene diphosphonate) TEMEP in conjunction with optimised RTA recipes. This lends advantages to the MLCD process such as fewer process

steps, removal of any potential sources of damage which may be caused to the monolayer by the layer deposition process and makes the roughness-increasing oxide removal step unnecessary. By using SiO_2 – phosphine oxide chemistry at the native oxide surface of the donor substrate[21], no molecular linker is required which may inadvertently affect diffusion of the dopant atoms during the rapid-thermal-anneal process. The concentration as a function of anneal time was studied initially on blanket Si samples using a constant temperature of 1005 °C for the rapid thermal anneal for each precursor molecule. Four-point-probe measurements were utilised to obtain sheet resistance (R_s) values post-RTA. As expected, R_s values decreased sharply with anneal time on blanket, contact doped samples. Samples with their native oxides and samples with the native oxides removed were tested in tandem. Doping efficiencies for diphenylphosphine oxide were estimated to be 55 and 7 % for H-terminated samples and samples with native oxide respectively.

In order to better understand the difference in sheet resistivities between native-oxide passivated samples and the samples functionalised with DPPO and TEMEP , Hazut et al. functionalised SiO2 nanoparticles (NPs with DPPO and TEMEP in the same study28 and thermally annealed the NPs at various temperatures. X-ray photoelectron spectroscopy (XPS) and thermo-gravimetric analysis (TGA) analysis were performed on each sample to characterise the monolayer surface chemistry and the monolayer decomposition mechanism. Samples functionalised with DPPO and TEMEP exhibited similar results both for XPS and TGA analysis with sharp decreases observed in C 1s and P 2p signals at elevated anneal temperatures. In contrast the TPPO functionalised NPs showed complete depletion of C and P at anneal temperatures over 400 °C. TGA analysis confirmed similar behaviour with monolayer retention of ~70 % for DPPO, ~40 % for TEMEP and ~0 % for TPPO functionalised NPs. This difference was attributed to the different chemical environments of the P=O group(s). The MLCD process has also been applied to CVD-grown intrinsic Si NWs

which were contacted by two terminals with back-gate electrodes. These nanowires were then drop-cast on a p-doped Si/SiO2 (100 nm)/Si¬3N4 (200 nm) substrate and contact-doped using the MLCD process using the TEMEP molecule. Immediately prior to the MLCD process application, the pre-doped nanowires exhibited resistances approaching 20 GΩ at 2 V. The MLCD-doped NW devices exhibited a decrease in resistance around 6 orders of magnitude with a 20 kΩ resistance observed at 2 V. To ascertain the longitudinal dopant distribution of the fabricated devices, Kelvin probe force microscopy (KPFM) was used on the Si NW devices with a 10 μm channel length between the source and drain electrodes. Intrinsic Si NWs (80 nm) were doped using the MLCD process with the TEMEP molecule at 900 °C. The KPFM results demonstrated high dopant uniformity along the length of the nanowires compared to traditional ¬in-situ¬ methods of nanowire doping.

This method was expanded upon again by Hazut, to transform undoped silicon nanowires into p-type/n-type parallel p-n junction configured nanowires using a one-step MLCD process, represented schematically in **Figure 4**.[22] Firstly, two separate Si substrates were functionalised; one functionalised with a P-containing molecule and another substrate functionalised with a B-containing molecule. The B-functionalised substrate also contained intrinsic Si NWs previously grown *via* CVD. Thus, the Si NWs were sandwiched between an n-type and p-type substrate and were annealed together in a rapid-thermal anneal furnace under vacuum which resulted in the controlled decomposition of the dopant-containing monolayers of each substrate and dopant diffusion into the NWs.

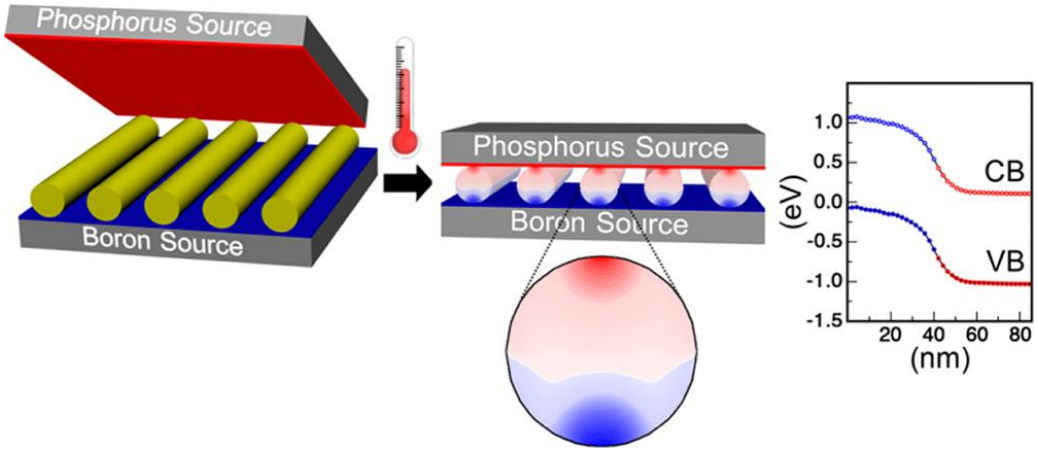

Figure 4. Schematic representation of p-n junction formation using the one-step MLCD process. Firstly, undoped Si NWs are transferred to a substrate that has been functionalised with a B-containing monolayer. A second substrate functionalised with a P-containing monolayer is then brought into contact with the NWs and annealed together to yield p- and n-doped Si NWs. Adapted with permission from ref: [22] Copyright 2014, American Chemical Society.

This MLCD approach shown in **Figure 4** yielded nanostructures which were both p- and n-doped. The junctions were then studied using a combination of scanning tunnelling microscopy and scanning tunnelling spectroscopy to determine the spatial electronic properties of the junctions. The junction configuration was also characterised using off-axis electron holography to provide additional information about the junction formation. STM analysis of the Si substrates doped with B and P showed p- and n-type electronic characteristics respectively. The spatial distribution of the dopants in the nanowires also conformed to expectations, with the highest dopant concentrations at the top and bottom of the nanowires at the point of contact with the donor

substrates. At these points on the nanowires, peak P concentrations were approximately 2.6×10^{19} atoms/cm^3 with highest B concentrations approaching 2.0×10^{20} atoms/cm$^{3.}$

More recently Longo and co-workers published a paper investigating the grafting of alkylphosphonic acids on Si by infrared spectroscopy and density functional theory for MLD of Si.[23] Again, a comparison to traditional MLD approaches was made where a dopant molecule is attached to the Si-H surface by hydrosilylation. Longo *et al.* studied an alternative approach based on work involving the grafting of OH-containing compounds by Michalak.[24–26] The initial process was based on a methodology to covalently bond an alcohol to an Si-H surface and was extended to phosphonic acids. This study differed by attempting to reduce the amount of potentially deleterious carbon in the process which may be a problem with current carbon-based precursors. Here, the molecules attach to the Si via a Si-O-X linker where X can be P, As, B and other dopant atoms. Simple forms of the acids can be used *e.g.* monohydride phosphonate in the work of Longo to reduce carbon contamination. In addition, P-containing moieties with long alkyl chains such as octadecylphosphonic acid (ODPA) contain a "weak link" at the X-C bond, where X is the dopant molecule (P-C in the case of ODPA) with removal of the carbon ligand typically at temperatures approaching 500 °C. This negates the need for the oxide cap that is typical of MLD processes. While the study focused purely on the pre-anneal steps of surface preparation and functionalisation with no electrical studies done on annealed blanket samples or nanostructured samples, the highly-optimised surface chemistry investigated could prove useful in future MLD studies.

There is still much to understand regarding the diffusion of dopants from an organic self-assembled monolayer especially regarding chemical information so close to the surface where the SIMS resolution limit becomes an issue. Shimizu and co-workers studied the behaviour of phosphorus

and contaminants from the MLD method used in conjunction with a conventional spike anneal.[27] Time-of-flight secondary ion mass spectrometry (TOF-SIMS) does not provide useful information within the first 5 nm of a sample again highlighting the need for metrology improvements. By using laser-assisted atom probe tomography (APT), a 3D distribution of the diffused dopant atoms was created to determine the dopant distributions in device structures. By combining the APT technique with a low-energy Si beam deposition step, termed focused ion beam direct deposition (FIBDD), a promising technique to obtain accurate near-surface quantitative dopant information was realised. To investigate ultra-shallow doping using this technique, a Si sample was functionalised with diethyl diphosphonate (DPP) and annealed at 800, 875, 950 and 1025 °C for 5 s in order to achieve different concentrations and differing depths. For anneals at 800 and 875 °C, no significant diffusion of P from the monolayer into the Si surface was observed which is in contrast to the latter two anneal temperatures where diffusion is observed. SIMS showed that at temperatures of 950 and 1025 °C, all samples exhibited an intense P signal just 2 nm beneath the surface. This was attributed to the pre-equilibrium erosion regime during which the sputtering and ionisation probabilities change constantly. Due to this variation, the P concentration as measured by TOF-SIMS is difficult to interpret quantitatively. The same sample was analysed using the APT technique. **Figure 5** compares SIMS measurements against APT measurements.

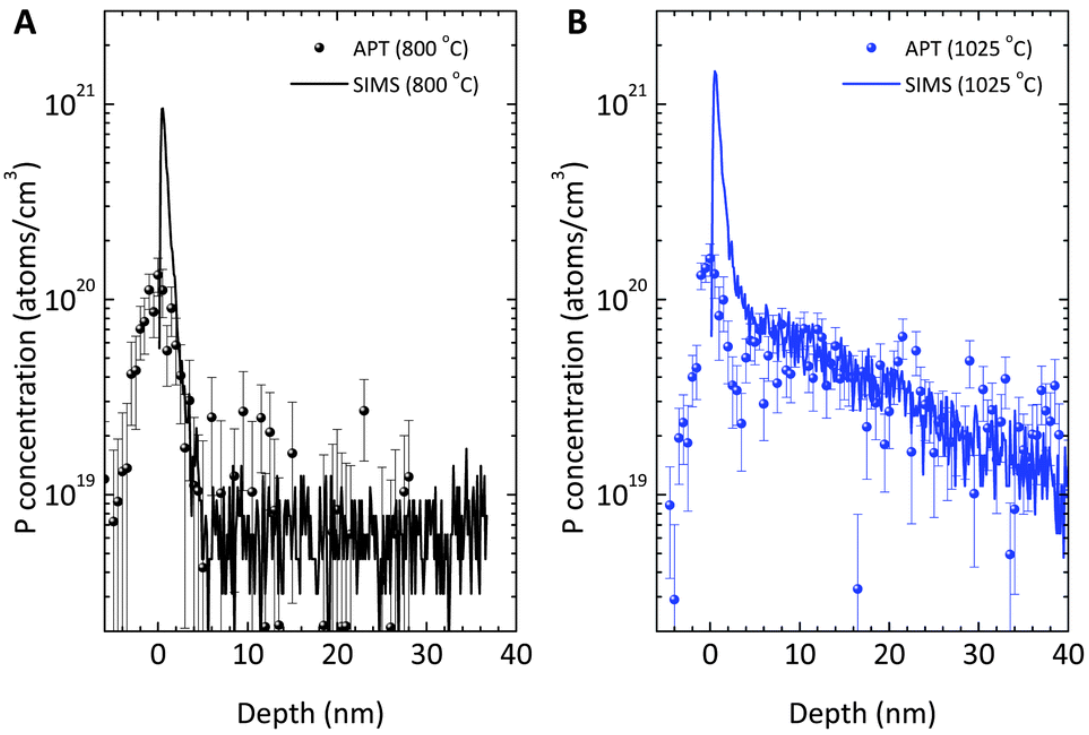

Figure 5. (a) Phosphorus concentration depth profiles obtained by the APT technique and (b) TOF-SIMS analysis from the two samples annealed at 800 and 1025 °C. Good agreement between the two techniques is observed over the range of validity for the TOF-SIMS measurements with the APT technique providing a more accurate measurement in the transient region of TOF-SIMS (< 3nm). Reproduced from ref: [27] with permission from The Royal Society of Chemistry.

The results of the two techniques are quite similar with the peak concentration of P obtained by the APT technique observed as slightly lower than the solubility limit of P in intrinsic Si. The APT technique also allowed contaminants (C and O) to be studied. C and O were limited to the first few monolayers with no difference in diffusivity between 800 and 1025 °C. This could be attributed to the Si-C bond formation during the hydrosilylation reaction.

While the vast majority of MLD literature to date has focussed primarily on applications for the semiconductor and microelectronics industry, there have been a number of interesting studies performed on photovoltaic (PV) materials for solar sell and energy purposes. Notably, Puglisi and

co-workers recently published a study where MLD-doped Si NWs integrated into complete solar cells exhibited higher short circuit currents and fill factors than planar reference cells.[28] CVD-grown *i*-SiNWs were immersed in a gold-cleaning solution to remove traces of the NW growth catalyst. Following a quick HF dip to remove surface oxides and provide the required H-termination, the NWs were immersed in a solution of diethyl 1-propylphosphonate (DEPP) and mesitylene (25%, v/v) at 160 °C for 2.5 h. Scanning electron microscopy (SEM) showed nanowires with an average length of 500 nm with transmission microscopy used to show diameter ranges between 2.5 and 70 nm. The TEM analysis also showed the presence of a 1 nm thick oxide layer on the wire. Spreading resistance profiling measurements showed a peak carrier concentration of 1.0×10^{19} atoms/cm^3 in the growth substrate with a junction depth of approximately 120 nm. The improved photovoltaic properties were attributed to two aspects. The MLD-doped NWs allowed a large increase in the photogeneration efficiency due to the reflectivity factor being 2-3 times larger than the equivalent planar diode. Additionally, the absorption factor approaches the ideal value of 1 due to the light trapping effect. In contrast, values of 0.1-0.5 were achieved for planar diodes. Puglisi *et al.* noted that the improvement in the light trapping alone could not account for the difference between the NW sample and the planar diode and postulated that the decreased sheet resistance between the top silver contact and the emitter was significantly reduced due to the better conformal doping achievable on the nanostructured surface using the MLD technique. An in-depth study of the MLD process with regard to solar cell applications is outside the scope of this review, and the reader is directed to excellent reviews by Caccamo [29] and Elbersen. [30]

Ye and co-workers further fine-tuned the MLD process through use of mixed-monolayers[31]. Although Ho[13] initially reported two mixing ratios, a more in depth study was required to

investigate the effect of mixed monolayers on the MLD process. By mixing dopant-containing alkenes with structurally analogous alkenes that do not contain a dopant, varying ratios of the dopant-containing molecule were grafted onto the Si-H surfaces. **Figure 6** shows a schematic detailing the sample preparation process for the mixed monolayer doping strategy. XPS and contact angle analysis were used to characterise the functionalised surfaces. A roughly linear relationship existed between the fraction of the dopant molecule on the surface and the amount of dopant-molecule present in the initial liquid mix.

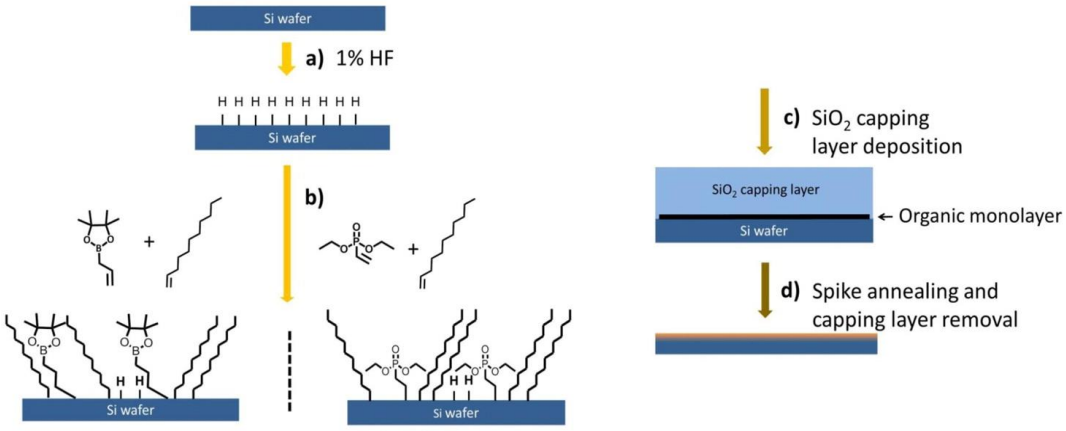

Figure 6. Process flow diagram for mixed monolayer doping. (a) Etching of the native oxide with HF removes the oxide and H-terminates the Si surface (b) hydrosilylation attached dopant and dilution molecules onto the H-terminated Si surface (c) capping of monolayer with SiO2 and (d) rapid-thermal-anneal and capping layer removal results in shallowly doped surface. Adapted with permission from ref: [31] Copyright 2015, American Chemical Society.

Following surface analysis, the samples were capped with 50 nm of SiO_2 and subjected to a high temperature anneal at 1000°C for 5 min. SIMS was used to investigate the incorporation of the dopant molecules into the Si substrates. Surface concentrations of approximately 1.6×10^{19} atoms/cm^3 were observed for B-MLD when using the undiluted molecule, with a junction depth of 125 nm. Surface concentrations of 4.2×10^{18} atoms/cm^3 were achieved for B-MLD with the most diluted dopant-alkene mix with a junction depth of 50 nm. A similar trend was observed for the P-MLD process with surface concentration values of 2.4×10^{19} atoms/cm^3 achieved with a junction depth of 125 nm for the pure undiluted molecule, with the most diluted dopant-alkene mix giving a concentration of 2.2×10^{18} atoms/cm^3 with a junction depth of about 50 nm. The study showed that using mixed monolayers is an important feature for controlling the MLD technique and will potentially enhance the usability of the approach in the formation and fabrication of functional nanoscale devices.

Until very recently only B- and P-containing molecules had been used in MLD studies. Limiting the anneal time to less than 5 s using advanced annealing techniques aids in the formation of sub-10 nm junctions in Si for dopants with fast diffusion rates, such as B and P. Despite the negligible electrical activity of N in Si[32,33], an alternative method was utilised by Guan and co-workers where N, a dopant with a low thermal diffusion coefficient, was introduced onto the Si surface using a standard hydrosilylation reaction.[34] All samples were then capped and then annealed at 1050 °C for 2 min. Nitrogen doping by the use of self-assembled monolayers can potentially form ultra-shallow junctions in Si. For a sample functionalised with an N-containing molecule only, N concentrations were observed as dropping from 4×10^{19} atoms/cm^3 near the surface to approximately 1×10^{17} atoms/cm^3 at 100 nm deep. A similar trend was observed for a sample functionalised with a molecule containing both P and N with N remaining in the top 100 nm and

P diffusing to 200 nm below the interface. The activation rates and diffusion coefficient of the N were found to be consistent with literature values. While an interesting application of surface functionalisation, the MLD of Si with N is unlikely to satisfy the need for the high dopant concentration and abrupt junction formation required for future device technologies due to the almost electrically-inactive nature of N in Si.

Mathey and co-workers recently functionalized Si NPs and native Si oxide with tailored boron molecular precursors in order to predictively and efficiently dope Si.[35] The method applied does not require an additional oxide capping step and minimizes carbon contamination while avoiding the use of hydrofluoric acid and the necessity for a capping layer. B-containing molecules were custom synthesized to react with silanol groups on the substrate surface at one end and a large, bulky backbone to act as a capping layer on the other end. This approach has been used for oxide functionalization and catalysis purposes but has not been applied to semiconductor materials for electronics. Similarly to the work of Hazut, silica NPs were used as a model to aid characterization of the surfaces. Surfaces were functionalized in a range of different solvents. The substrates were subjected to a rapid thermal treatment in low pressure nitrogen and heated to 985 °C from 300 °C at a rate of 10°C / s. **Figure 7** displays SIMS data extracted for those samples showing peak concentrations exceeding 1×10^{21} atoms/cm^3 for samples functionalised in toluene and concentrations of approximately 1×10^{20} atoms/cm^3 for samples similarly functionalised in dichloromethane.

The use of boron molecular precursors that combine both the dopant molecule and a bulky backbone to act as a capping layer, in addition to containing a moiety with anchoring ability on the surface of non-deglazed Si wafers is beneficial to incorporate controlled doses of boron without potential deleterious carbon contamination. This interesting approach to surface functionalisation

allows for a molecular level understanding of the surface species using silica NPs as model surfaces. This approach could well prove to be beneficial for advanced CMOS manufacturing processes where few-step process are desired.

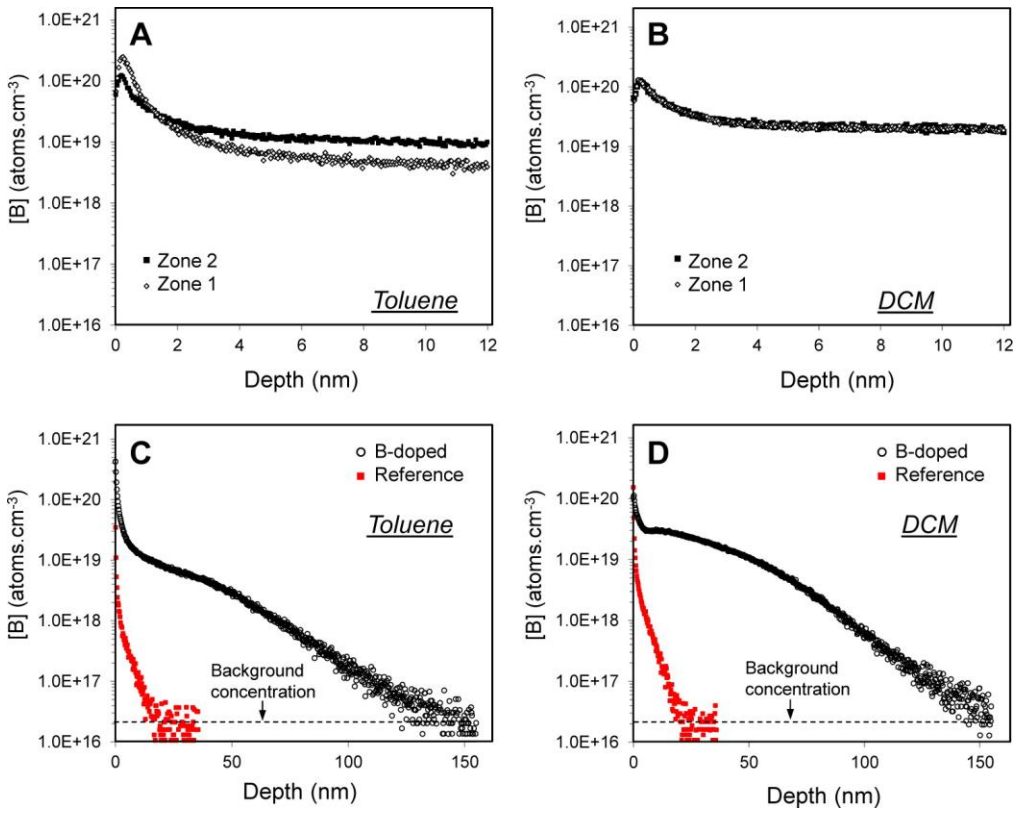

Figure 7. Magnetic SIMS depth profiles of boron treated wafers functionalised in toluene (a) and (c) and those grafted in dichloromethane (b) and (d). The profiles shown in (a) and (b) show data obtained over the first 12 nm of the depth for two different areas at a low ion impact energy of 250 eV. Shown in (c) and (d) are profiles containing concentration vs depth data for the control wafer and B-doped wafers. Adapted with permission from ref: [35] Copyright 2015, American Chemical Society.

Recently, Arduca and co-workers studied the functionalisation of non-deglazed Si substrates using DPP.[36] The monolayer of DPP on the native Si oxide was capped further to form a P δ-layer. Arduca *et al.* noted that at a processing temperature of 165 ºC the maximum P dose within the δ-

layer was dependant on the footprint of the dopant-containing molecules. At a processing temperature of 100 ºC the dopant dose was found to be dependent on the availability of reactive sites on the native Si oxide substrates. The approach studied here would prove useful for the transfer of MLD to CMOS manufacturing facilities as it avoids the use of hydrofluoric acid by using non-deglazed substrates.

Semiconductor devices rely on the ability to form two types of electrically-conducting layers: n-type and p-type. An electrically active dopant atom contributes a free carrier to the conduction band or valence band by creating an energy level that is very close to either band. An ideal dopant atom should therefore have a shallow donor/acceptor level and a high solubility. Arsenic and phosphorus are considered to be the most suitable n-dopants based on their high solubilities in Si[37] and also due to their ionisation energies.[38] For continued fabrication of devices with complex and non-planar 3D geometries which require abrupt, conformal and shallow doping profiles, it is desirable that the diffusion rate of the dopant is small. As has a much smaller diffusion coefficient when compared to P, making it the ideal dopant for heavy and shallow n-type doping of silicon.[39] O'Connell *et al.* recently published the first application of As-MLD on planar Si and a number of Si nanowire devices.[40] **Figure 8** shows the general scheme applied in their study. Using a custom-synthesised As-containing molecule, planar Si substrates and Si NW devices were functionalized *via* a hydrosilylation reaction.

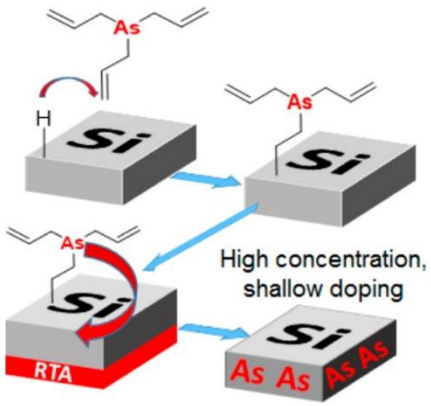

Figure 8. Schematic representing the As-MLD process on Si. A hydrosilylation reaction occurs between a reactive H-passivated Si surface and the labile C═C site on the dopant containing molecule, resulting in a covalently bonded molecular layer. The samples are then capped with 50 nm of SiO_2 and subjected to a rapid-thermal-anneal (RTA) step resulting in high concentration, shallow doping of silicon. Adapted with permission from ref: [40] Copyright 2015, American Chemical Society

The samples were then capped and annealed at various temperatures for a constant time of 5 s. The planar substrates were analysed using XPS and SIMS with the NW samples analysed using four-point-probe measurements, SEM and TEM. **Figure 9** shows SIMS-derived chemical concentrations for three samples analysed at 950, 1000 and 1050 ^{o}C respectively showing an increase in concentration in line with increasing anneal temperature.

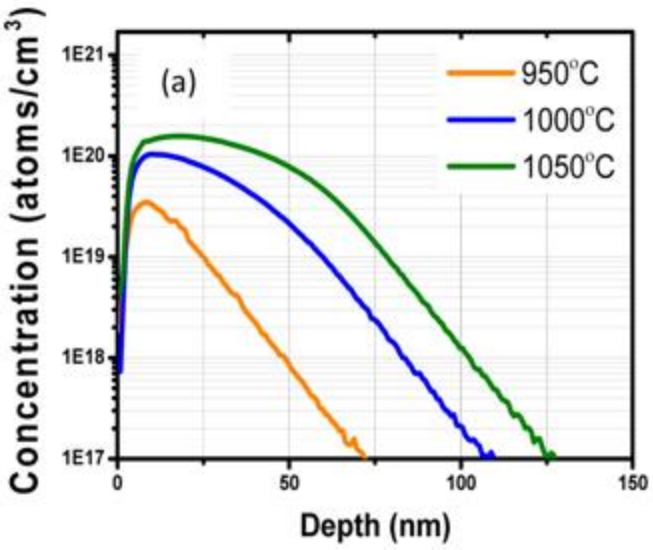

Figure 9. Secondary ion mass spectrometry profiles of three samples processed at varying temperatures for 5 s. The carrier depths were observed to be extremely shallow with peak concentrations achieved at less than 25 nm. The dopant concentration increased with an increase in rapid-thermal-anneal temperature. Junction depths ranged from 75 nm at 950 °C to 125 nm at 1050 °C. Adapted with permission from ref: [40] Copyright 2015, American Chemical Society

Diffusivity data showed that extrinsic diffusivity regimes were observed. Electrical performance was evaluated on a number of nanowire devices ranging from 1000 to 20 nm in width. As most current device dimensions are currently < 40 nm, current was assumed to flow uniformly through the entire cross-section of the nanostructure, like that of a metal track. This model is applicable to nanostructures with sub-40 nm dimensions such as FinFETs and remains applicable as the device feature size continues to scale down due to the probability of having a uniformly doped cross-section being higher. **Figure 10 (a)** shows nanowire resistivity data with **Figure 10 (b)** showing a HRTEM image highlighting the lack of visible extended defects in the NW. As can be seen from the resistivity data, there is a significant difference in the resistivity between the pre-MLD wires and the post-MLD wires. Much lower resistivities were observed for the nanowires with

dimensions lower than 40 nm, with a resistivity reduction of 5 orders of magnitude measured for the larger nanowires and a reduction of 7 orders of magnitude observed for the smallest sized nanowires. This highlights the efficacy of the MLD technique on small, 3D devices. The HRTEM image shown in **Figure 10(b)** shows no indications of any visible extended defects while the FFT inset shows the highly crystalline nature of the nanostructure has been maintained. In the past, {111} twin boundary defects and stacking faults have been the most commonly encountered problems during ion implantation doping of NW structures where crystal damage is very easily visible.

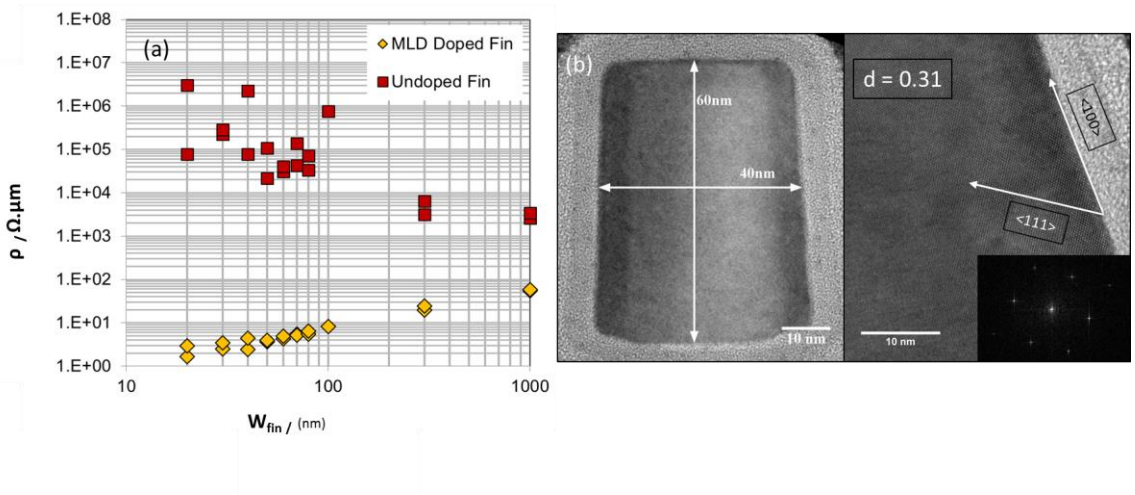

Figure 10. (a) Resistivity of NWs as a function of width for pre-MLD and post-MLD wires. The best results were observed for nanowires < 40 nm in width, showing that the MLD strategy employed works extremely well for small feature sizes. (b) TEM image of a section of the 40 nm Si nanowire test device, (b) magnified HRTEM micrograph of the nanowire with the ⟨111⟩ and ⟨100⟩ directions indicated. (b, inset) FFT showing the highly crystalline nature of the nanowire. There are no indications on either micrograph of any defects or damage to the crystal lattice. Adapted with permission from ref: [40] Copyright 2015, American Chemical Society.

These developments in MLD on Si so far have focused on molecules which contain only one dopant atom. Using molecules containing more than one dopant atom should yield a higher concentration when compared to a structurally analogous molecule containing only one dopant atom. Most recently, Ye *at al.* published a study on B-MLD of Si, where they used several carborane molecules containing 8 -10 times more B than the frequently used allylboronic acid pinacol ester.[41] Once again utilizing the hydrosilylation reaction to functionalize the Si surface, samples were annealed at temperatures between 950 and 1050 ^{o}C and characterized using XPS, SIMS and four-point-probe using the van der Pauw method. The XP spectra shown in **Figure 11 (a)** displays the B *1s* signal intensity for the different bonding configurations for each tested molecule. A stark difference is seen between the first molecule and latter two molecules showing preferential binding for the allyl group on the dopant-containing molecules. The SIMS profiles shown in **Figure 11 (b)** show peak concentrations near the surface approaching 1×10^{20} atoms/cm^3 with junction depths of 40 nm reported for lower anneal temperatures and approaching 60 nm for higher annealing temperatures. XPS measurements indicated approximately 10 times more boron present on the carborane-modified Si surface when compared to the monolayer composed solely of the ABAPE functionalized samples. SIMS and sheet resistance measurements also confirmed the increase in the dopant dose under the same annealing conditions.

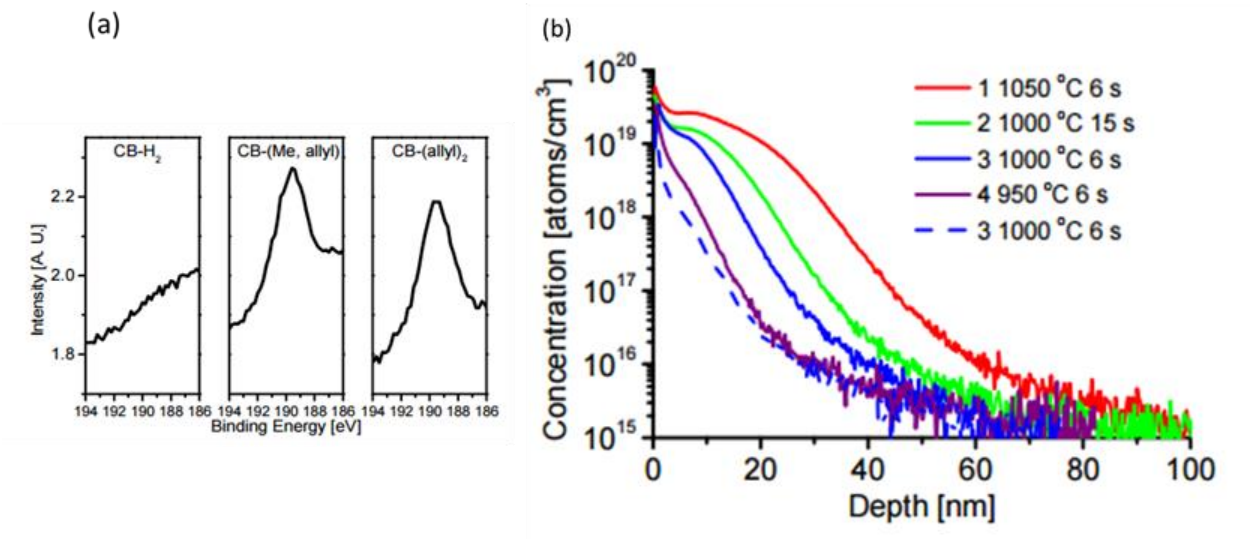

Figure 11. (a) XPS B *1s* spectra showing the presence of large intensity signal on substrates treated with three boron-containing carborane derivatives. (b) SIMS profiles for samples doped by MLD using (CB-Me, allyl) (solid line) and ABAPE (dashed line) for varying times and temperatures. Peak concentrations near the surface approached 1×10^{20} atoms/cm^3 with junction depths of 40 nm reported for lower anneal temperatures and approaching 60 nm for higher annealing temperatures. Error in concentrations did not exceed 10 %. Adapted with permission from ref: [41] Copyright 2015, American Chemical Society.

Most recently, O'Connell *et al.* reported the application of a two-step MLD process using azide-alkyne cycloaddition reactions.[42] The hydrosilylation reaction has featured throughout the vast majority of MLD processes as the main method for attaching dopant containing molecules to the Si surface. Molecules suitable for this approach typically contain both the dopant atom and the labile C=C site in the same molecule. Often, these molecules are air-sensitive and difficult to purify, in addition to being unstable at the required hydrosilylation temperatures. O'Connell and co-workers employed a two-step process where a dialkyne was initially grafted onto a Si surface. The resulting tightly packed monolayer of linear alkynes offered excellent protection of the Si surface while providing a reactive "handle" to which dopant-containing azides could be attached

via a Huisgen 1,3-dipolar cycloaddition reactions. This approach greatly suppresses the effect of ambient conditions on the Si surface. Additionally the dopant-containing azides were resilient towards attack from atmospheric water and oxygen, allowing for a very robust functionalisation procedure. Si substrates were functionalised with 1,7 octadiyne and then further functionalised with the dopant-containing azides according to the scheme shown in **Figure 12.**

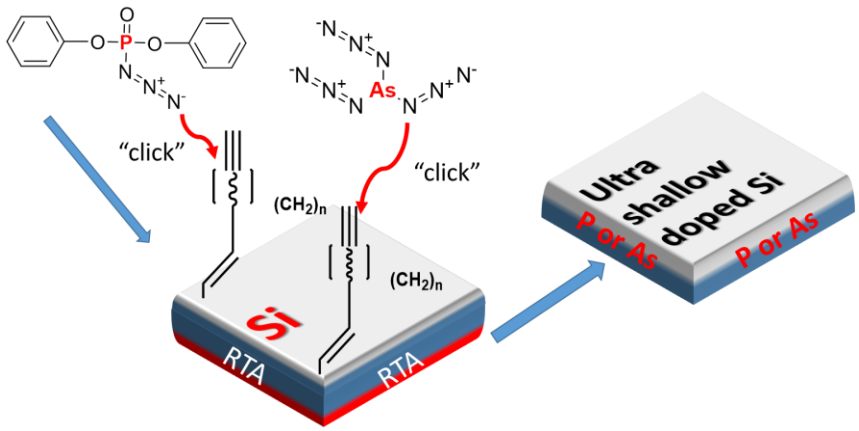

Figure 12. Si was functionalised with dialkynes of varying length between 7 and 10 carbons. The terminal alkyne groups were then reacted with P- and As-containing azides *via* an alkyne-azide cycloaddition reaction to form dopant-containing monolayers on the Si surface. These substrates were then capped and annealed to form ultra-shallow doped Si. Adapted with permission from ref: [42] Copyright 2016, American Chemical Society.

Samples were annealed at 1050 ^{o}C for 5 s to diffuse the attached dopants into the Si. To compare the oxidation resistance and dopant profiles to a traditional P-MLD process, a sample of Si was functionalised with allyl diphenyl phosphine using a one-step hydrosilylation process. Both samples exhibited similar dopant profiles with peak concentrations approaching 1×10^{19} atoms/cm^3 with junction depths of approximately 25 nm. The stability of the P-functionalised

samples were monitored via XPS. The two-step click chemistry approach offered superior resistance to oxidation, especially in the first 24 h whereas the sample functionalised using a one-step hydrosilylation showed the presence of oxide after 24 h. This stability might prove advantageous for potential integration into future device fabrication process to prevent oxidation of the Si surface between processing steps.

Monolayer doping on Ge

While Si has been the material of choice in the semiconductor and microelectronics industry for many decades, germanium (Ge) has been put forward as a viable alternative for future CMOS processes. The question remains whether or not scaled Ge FETs can outperform the equivalent Si FET device. Experimentally, the answer may be unclear for now but Eneman et al. performed interesting analysis comparing Ge with Si FinFETs in the presence of strain.[43] They concluded that relaxed Ge p-FinFETs cannot outperform strained Si, but needed a mobility boost to do so, possibly through embedded stressors. For Ge n-FinFETs, relaxed channels already outperform strained Si primarily due to favourable fin sidewall mobility. Adding stressors will increase that benefit to more than double the Si performance, in terms of mobility. In addition to the performance differences between such devices, Ge displays more complex oxidation chemistry at its surface. Ge forms oxides in the 2+ (GeO) and the water soluble 4+ (GeO_2) oxidation state. This oxide instability makes surface treatment and passivation strategies and hence, monolayer doping on Ge, much more challenging than analogous chemistry on Si. For example, hydrogermylation, requires much higher temperatures which will reduce the number of molecules available for surface functionalisation. Additionally oxide removal steps using HF tend to roughen Ge surfaces more than the same process on Si. Ge also has a lower melting point than Si which

limits thermal budgets for dopant activation and diffusion processes.[10] Nanoscale doping has been carried out on Ge by other means such ion beam irradiation[44] but monolayer doping has not been as prevalent on Ge as it has on Si, purely due to the challenging surface chemistry and CMOS processing limitations. Nevertheless, Long *et al.* recently published a study on As-MLD of Ge.[45] The molecule previously utilised by O'Connell and co-workers[40] was used but was dissolved in IPA as opposed to mesitylene. As the hydrogermylation temperature of 200 ^{o}C greatly exceeds the decomposition temperature of the TAA molecule, UV-initiated hydrogermylation was used. The sample was illuminated with a 254 nm UV pen lamp for 3h. The sample was then rinsed to remove physisorbed species, capped and annealed. Due to the lower melting point of Ge, the thermal budget for the rapid thermal anneal treatments needs to be accordingly adjusted. The anneal temperature was held at 650 ^{o}C with the anneal time varied between 1, 10 and 100 s. **Figure 13** shows the active carrier concentration vs depth as extracted from ECV measurements. The peak active carrier concentration approached 6×10^{18} atoms/cm^3 with a maximum junction depth of just under 100 nm. The peak concentration did not change with the differing thermal budgets, showing that the As-MLD process on Ge is likely limited by the solubility of As in Ge at 650 ^{o}C, again highlighting the need to explore more advanced annealing techniques. Inset shows roughness measurements as obtained by atomic force microscopy (AFM).

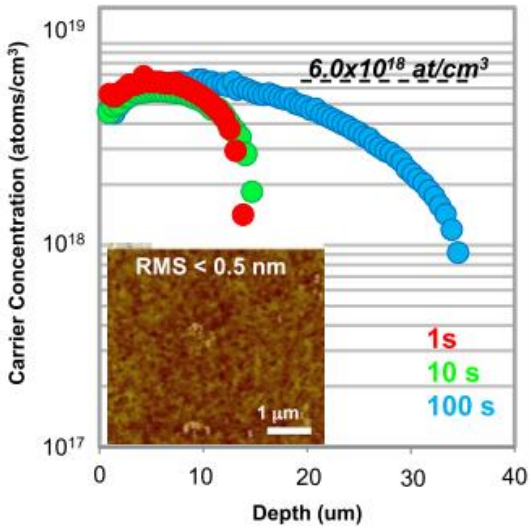

Figure 13. Active carrier concentration vs depth extracted by electrochemical capacitance-voltage profiling of As-doped Ge. The peak active carrier concentration approaches 6×10^{18} atoms/cm^3 with inset showing an AFM image of the Ge substrate after the MLD process. Adapted with permission from ref: [45] Copyright 2014, IEEE.

Duffy and co-workers built on the work carried out by Long *et al.*[45] by using an MOVPE-based process to deposit monolayers of P and As on Ge substrates and nanowire devices.[46] **Figure 14 (a)** shows chemical concentration *vs.* depth profiles as extracted from SIMS analysis on samples with deposited AsH_3. A higher thermal treatment temperature was more effective at incorporating As at the cost of a much deeper junction depth. **Figure 14 (b)** shows ρ *vs.* W_{fin} profiles where ρ refers to resistivity and W_{fin} refers to the nanowire width, for Ge nanowires doped using AsH_3 and PH_3 at 650 ^oC in the case of AsH_3 and 650 and 700 ^oC in the case of PH_3. The higher temperature is shown to be more effective for P incorporation with both dopant species producing similar results in the larger devices while P-doped fins exhibited better electrical characteristics for the

smaller-scaled devices. Duffy and co-workers attributed this to As trapping at the Ge surface in the case of smaller devices.

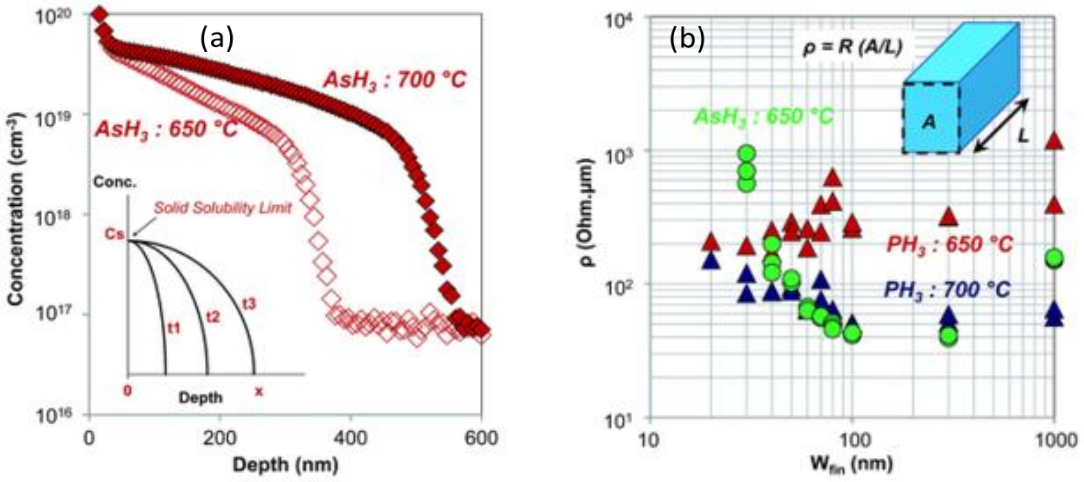

Figure 14. (a) Chemical concentration *vs.* depth profiles as extracted from SIMS analysis on samples with deposited AsH_3. A higher thermal treatment temperature was more effective at incorporating As at the cost of a much deeper junction depth. **(b)** showing ρ *vs.* W_{fin} for Ge nanowires doped using AsH_3 and PH_3 at 650 °C in the case of AsH_3 and 650 and 700 °C in the case of PH_3. A higher temperature is shown to be more effective for P incorporation with both P and As species producing similar results in the larger devices while P-doped fins exhibited better electrical characteristics for the smaller-scaled devices. Reproduced from ref: [46] with permission from The Royal Society of Chemistry.

While MLD is in its infancy with respect to its applications on Ge, other methods of achieving ultra-shallow and abrupt junctions such as δ-doping are promising.[47–51]

Monolayer doping on InGaAs

III-V semiconductors such as InGaAs have great promise for the active channel materials of proposed device geometries that are conducive to aggressive scaling, such as field-effect transistors. However significant improvements in the source and drain resistances are required if InGaAs is to scale beyond the 22 nm technology node. Advanced III-V based CMOS technologies need ultra-thin body channel materials to maintain the electrostatic integrity of the devices and thicker source/drain regions to keep access resistances to a minimum. Again, similarly to Ge, the surface chemistry of InGaAs is challenging and must be overcome in order to find suitable monolayer doping strategies. MLD is well suited for this purpose due it to its highly conformal nature, ability to provide ultra-shallow junctions and lack of damage to the III-V zinc blende lattice structure as shown by Yum *et al.* in the first report of solution-based MLD on InGaAs.[52] Here, ammonium sulphide $(NH_4)_2S$ was used to clean the InGaAs substrates which also resulted in the S-termination of the surface. While this study focused more on the effect of differing capping layers on the surface, mean concentrations of S ranged from 5×10^{20} atoms/cm^3 to 1×10^{21} atoms/cm^3 with average junction depths of 11 nm, depending on the particular capping layer used, were reported. The study showed that S-MLD is sensitive to the capping layer growth temperature and precursor reaction energy at the channel surface, and concluded that a SiN_x/BeO bilayer structure may be a more useful solution to improve the activation efficiency of S-MLD to realise small feature sized III-V devices.

Further studies on this S-MLD process were carried out by Kort and co-workers, where Raman spectroscopy was used to probe the electron-phonon coupling in InGaAs epilayers doped using a S-MLD method.[53] The process showed an interesting application of Raman and may prove promising as a method to probe dopant incorporation within shallow junctions formed using the

MLD technique. D'Costa and co-workers utilised infrared spectroscopic ellipsometry to study S-MLD doped InGaAs ultra-shallow junctions.[54] The samples were prepared using the previously mentioned $(NH_4)_2S$ cleaning method. The optical response of the epitaxial layer was described with a Drude-like free carrier response from which the carrier relaxation time and electrical resistivity could be extracted. Extracted doping levels approached 1.7×10^{19} atoms/cm^3 at depths of approximately 3-4 nm.

Kong *et al.* recently reported the first application of Si MLD on InGaAs, applying a disilane and silane treatment and using laser annealing (LA) to form conformal, ultra-shallow and highly n-doped regions.[55] Despite not being a traditional solution-based MLD approach, there is an advantage in that an *in-situ* clean may be performed in the vacuum system without exposing the substrate to atmosphere, potentially ensuring a high-quality oxide free surface for MLD. The introduction of the silanes selectively form conformal monolayers of Si which are then annealed in the LA apparatus. LA can potentially overcome the solid solubility of the Si dopant, in addition to reducing the thermal budget and minimizing the dopant diffusion to realize abrupt, ultra-shallow junctions. **Figure 15(a)** displays SIMS profiles for samples treated with silane (SiH_4) at 500 ^oC for 120 s and then subsequently laser-annealed at 100, 120 and 140 mJ/cm^2. Diodes were also fabricated from the SiH_4-treated samples with dimensions of $L_{diode} \times L_{diode}$ with L_{diode} ranging from 50 to 150 μm. Ni liftoff was used to form the top contacts with Au used to form an ohmic contact on the back side of the InP substrate. **Figure 15(b)** plots the I-V characteristics of the 50 μm diodes showing showing a large difference of between five and seven orders of magnitude between forward and reverse currents. **Figure 15(c)** displays the diode ideality factor, n , plotted against L_{diode}, showing that the samples annealed at 100 mJ/cm^2 exhibited very low values of n, which may be attributed to the absence of implant damage. . Diodes annealed at a fluence of 100 mJ/cm^2

had a low ideality factor that is independent of L_{diode} while those annealed at 120 and 140 mJ/cm^2 had a higher ideality factor due to defects induced by melting at the liquid-solid interface during the LA process. HRTEM imaging showed that the crystallinity of the diodes was not affected by the MLD process.

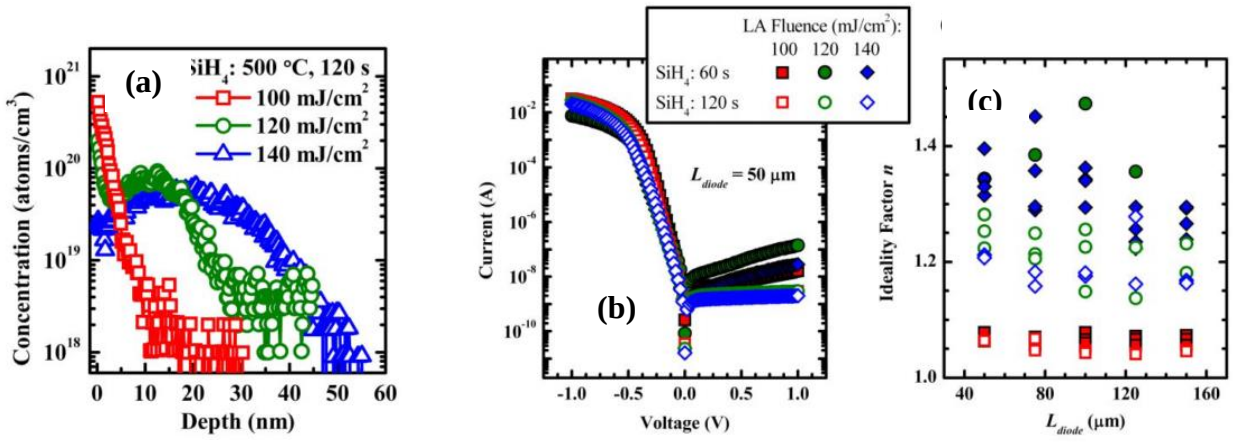

Figure 15. (a) SIMS profiles for samples treated with SiH_4 at 500 ^oC for 120 s and laser annealed at 100, 120 and 140 mJ/cm^2. The profiles for fluences of 120 and 140 mJ/cm^2 exhibit a box like profile while the profile for a fluence of 100 mJ/cm^2 has a very high Si concentration of approximately 5. × 10^{20} atoms cm^{-3} at the InGaAs surface. **(b)** Diode I-V characteristics showing high forward to reverse current ratio of between 5 and 7 orders of magnitude and **(c)** showing the ideality factor of the diodes plotted against diode size. Diodes annealed at a fluence of 100 mJ/cm^2 had a low ideality factor that is independent of L_{diode} while those annealed at 120 and 140 mJ/cm^2 had a higher ideality factor due to defects induced by melting at the liquid-solid interface during the LA process. Adapted with permission from ref: [55] Copyright 2014, IEEE.

Most recently, Kort and co-workers reported a method of determining the free electron density in sequentially doped InGaAs using Raman spectroscopy.[56] Again, using the commonly-used

ammonium sulfide treatment was used to passivate the InGaAs surface with S, and the substrate was then thermally treated and annealed. They showed that the technique, when used to determine the dopant activation and free carrier density is agnostic to the nature of the individual dopants or the manner in which they are incorporated. The relative intensities of the GaAs-like feature and the high frequency coupled mode (HFCM) in the optical phonon region provided a good indication of the surface depletion layer.

Hybrid spin-on doping on Si

Spin on-doping (SOD) is a doping process involving the spin-coating of a dopant-containing solution onto semiconductor substrates, which is followed by a rapid-thermal annealing step during which the dopants diffuse into the substrate. Often, a pre-diffusion annealing step is required to "glassify" the spin-on dopant layer. The dopant-containing solution usually contains either a mixture of SiO2 and dopant-containing molecule or silicon-containing polymers with dopant atoms already incorporated into the polymer. Spin-on doping is a simple, low-cost, and essentially non-destructive technique, but can suffer from dose control problems in addition to uniformity over large areas and on 3D structures. Additionally, spin-on dopants often leave residual components behind. While pure SiO2 and silicates are easily removed *via* a wet chemical etch, the presence of residual organics from the solvent during the annealing process results in chemically modified layers that can be quite difficult to remove.

Despite Si being the current material of choice for the semiconductor industry, there have been relatively few reports of spin-on doping in recent years. Hoarfrost and co-workers recently employed spin-on doping using a dopant-containing polymer to demonstrate a hybrid technique

that lies between MLD and traditional spin-on doping.[57] Unlike traditional spin-on doping where the dopant-containing layers survive the annealing step, dopant-containing polymer films are easily burned off at the film-air interface. **Figure 16(a)** is a schematic showing the approach used in the study by Hoarfrost *et al.* utilising the dopant-containing molecules poly(vinylboronic acid pinacol ester) [PVBAPE] and poly(diethylvinylphosphonate) [PDEVP]. **Figure 16(b)** shows sheet resistances of B and P-doped Si using polymeric spin-on dopant films of varying thicknesses. All substrates for the sheet resistance studies were annealed at 1000 °C for 30 s.

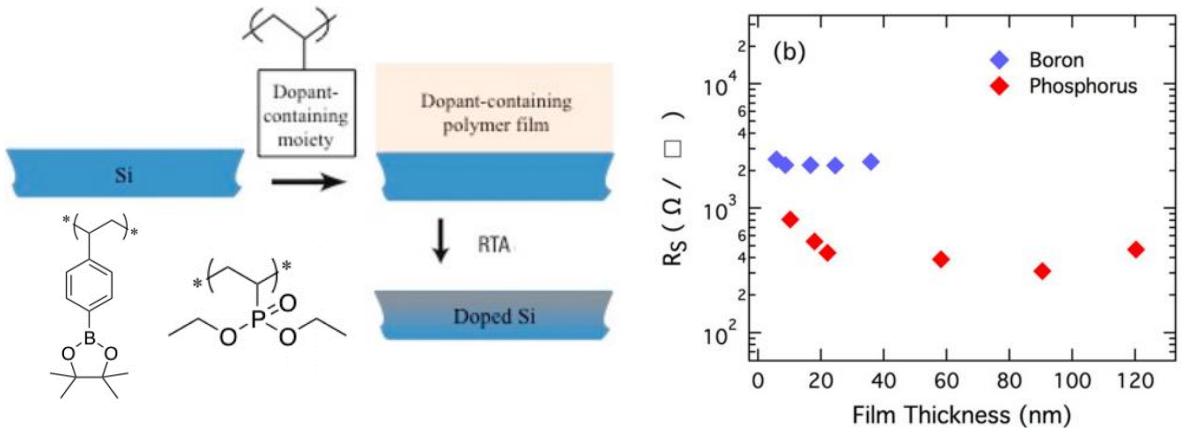

Figure 16. (a) Schematic representation of the polymeric spin-on doping process. An organic dopant-containing polymer film is spun onto an oxide-free Si surface from solution and the dopant atoms are diffused into the Si surface using a rapid-thermal-annealing step. The dopant molecules (PVBAPE) and (PDEVP) are shown. (b) Sheet resistance measurements for boron- and phosphorus-doped Si substrates using polymer films of varying thicknesses. All substrates were thermally treated at 1000 °C for 30 s. Peak concentrations for P-doped samples approached 1×10^{21} atoms/cm^3 with average junction depths between 40 – 60 nm. For B-doped samples, peak concentrations reached just over 1×10^{20} atoms/cm^3 with a junction depth of approximately 30 nm for a sample annealed for 10 s and approaching 70 nm for a sample annealed for 60 s. Adapted with permission from ref: [57] Copyright 2013, American Chemical Society.

Sadhu and co-workers used a two-step spin-on doping process to dope electrolessly etched Si NW arrays.[58] Etching of highly doped Si NWs leads to porous structures with high defect densities. This causes difficulties in forming electrical side-contacts to these NWs. Additionally, integrating such chemically-etched nanowires into high performance devices is non-trivial. While MLD would be suitable for the doping of such structures, the porosity of these structures complicates

the surface chemistry. Although dopant depth and concentration can be controlled by anneal temperature and time, Sadhu chose to control the concentration by deposition of various thicknesses of oxide < 25 nm, to act as diffusion barrier layers. Borofilm and Phosphorofilm (Filmtronics©) were used as the spin-on dopants. SIMS was used to verify the concentration and depth profiles with peak B concentrations approaching 2×10^{19} atoms/cm^3 and lowest concentrations approaching 4×10^{18} atoms/cm^3. P-doped NW arrays exhibited peak dopant concentrations approaching 1×10^{20} atoms/cm^3 without the barrier layer and 6×10^{19} atoms/cm^3 using a barrier layer. **Figure 17(a)** shows SIMS profiles for the B-doped NW arrays. Additionally, **Figure 17(b)** shows four-point-probe measurements used to obtain *I-V* characteristics and resistances from the doped arrays. **Figure 17(c)** shows how the *ex-situ* SOD process applied reduces the electrical resistivity of the Si NWs by over three orders of magnitude to between 15-30 mΩ cm and relates the electrical resistance of six nanowire devices with their cross section. The SIMS data obtained for the NW array shows dopant concentrations ranging from 8×10^{18}- 1×10^{19}atoms/cm^3 across the cross section. The resistivity values are within a factor of two-four when compared to bulk Si doped to similar levels.

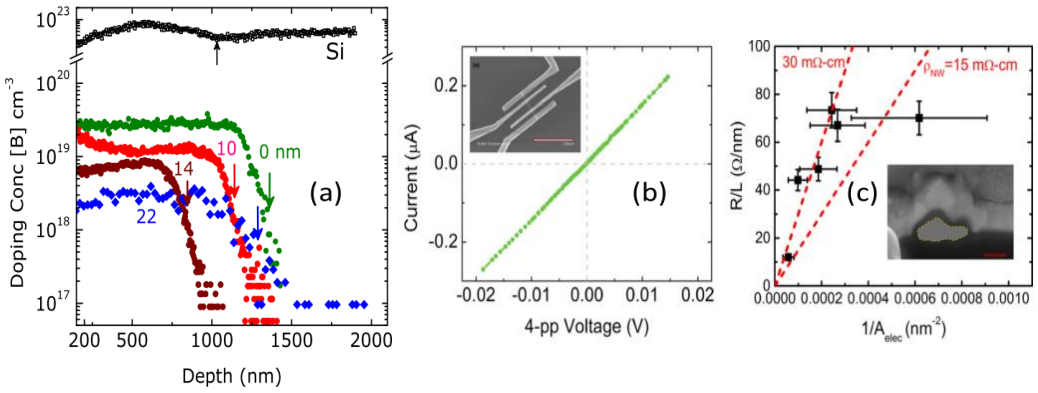

Figure 17. (a) SIMS concentration and depth profile data of the B-doped Si NW arrays doped using the SOD process and combined with a PECVD-deposited barrier layer of thickness labelled against each profile with arrows representing length of NW array measured from SEM before analysis. (b) Four-point-probe measurements of single NWs from the doped array. (c) Four point probe resistance values for varied NWs with different diameters taken from an array that was doped to approximately 1×10^{19}atoms/cm^{3}. Inset shows the focused ion beam (FIB) cross-section of the NW with scale bar indicating 100 nm. Adapted with permission from ref: [58] 2008, IOP Publishing.

Spin-on doping in Ge

Despite the scarce use of Ge in the semiconductor industry, reports of spin-on doping in the last number of years have been more frequent than on Si. Jamil *et al*. recently applied the spin-on doping process in the fabrication of high-mobility P-doped Ge nMOSFETS.[59] Using similar dopants to Sadhu[58], they showed that the SOD-doped nMOSFETS showed improved junction characteristics and an approximately 1.3x enhancement in drive current over the ion-implanted control devices. **Figure 18** shows I_d-V_d characteristics of the Ge (100) nMOSFETS. Scanning resistance probe (SRP) measurements showed peak electrical activation approaching 7×10^{19}

atoms/cm^3 which is up to 3 times higher than that of the ion-implanted control sample. This higher activation may be attributed to the lower defect density. Raman studies showed an intensity close to pristine Ge, which is in stark contrast to the implanted Ge where the much lower intensity showed significant residual crystal damage. The *I-V* characteristics of the diodes showed a lower defect density when doped using the SOD technique, with approximately two orders of magnitude lower reverse junction leakage when compared to analogous structures doped by ion-implantation. nMOSFETS exhibited good I_{on}-I_{off} ratios of between 10^4 and 10^5. The MOSFETS exhibited high mobility with a μ_{eff} approaching 679 cm^2.V^{-1}.s^{-1}. TEM imaging would have been useful in the study to confirm the minimization of crystal lattice damage on the fine feature sizes.

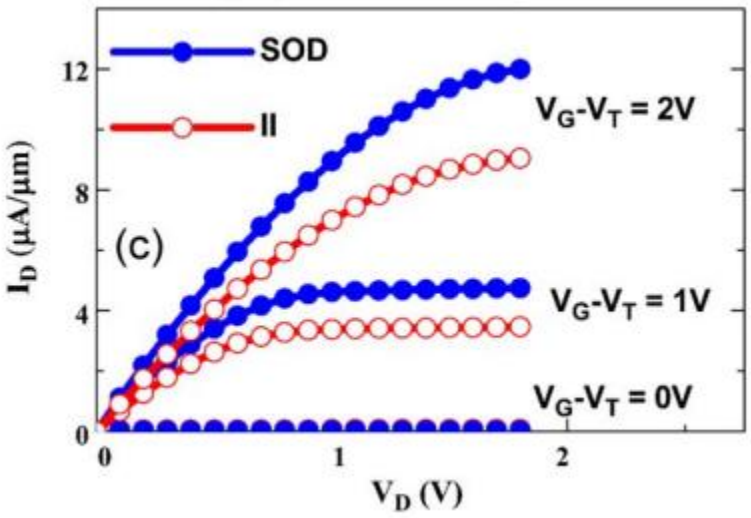

Figure 18. I_d-V_d characteristics of the Ge (100) nMOSFETS at V_G-V_T intervals of 1Vshowing a 1.3 enhancement in drive current over ion-implanted control samples. Reproduced with permission from ref: [59] Copyright 2011, IEEE.

Sharp and co-workers used a spin-on sol-gel dopant film containing Ga as the dopant to dope Ge exceeding 10^{20} atoms/cm^3.[60] Sheet resistance and SIMS profiling were used to determine the dopant profiles. Peak dopant concentrations approached 2 × 10^{20} atoms/cm^3. Unfortunately,

junction depths varied with temperature from 80 nm to well over 2 μm showing a lack of control over the diffusion depth. While this approach may prove useful to due to its simplicity and cost-effectiveness, it is unlikely to satisfy the requirements to form ultra-shallow junctions.

More recently, Sorianello *et al.* published a study of SOD phosphorus diffusion in Ge thin films on Si for near-infrared (NIR) detectors.[61] Using a Filmtronics© phosphorus SOD, a layer of the dopant was spun onto a substrate and then annealed at 580 °C. SIMS analysis showed peak concentrations approaching 1×10^{20} atoms/cm^3. The profile was not box-like, which is expected due to potential inhomogeneity of thermally grown Ge films. The group also applied the SOD process to Ge on Si heterojunction detectors with high responsiveness of 0.1 A/W with a signal-to-noise ratio of 25 dB at 1.55 μm. The junction depth approached 1 μm, again highlighting an application where MLD could provide for a much reduced dopant diffusion depth. The authors also reported cracking in the SOD thin film post-annealing, an issue which would not be encountered in a typical MLD process.

Kim and co-workers reported the application of an Sb containing SOD to GeOI inversion-type nMOSFETS, with a body thickness of 16 nm, fabricated by a Ge condensation technique.[62] They first applied the process to bulk GeOI before transferring to MOSFETS. After annealing at 650 °C, peak chemical concentrations approached 1×10^{23} atoms/cm^3. In order to estimate the free electron concentration after Sb diffusion, accumulation-type GeOI nMOSFETS were fabricated and the threshold voltage was monitored before and after doping. The electron concentration after Sb diffusion was observed to be approximately 3×10^{18} atoms cm^3. Ultrathin nMOSFETS were fabricated and doped using the Sb SOD process. A high threshold voltage was

observed due to the device operating in back-gate mode with the 100 nm BOX gate insulator as well as the high hole concentration on the Ge p-body.

Bao and co-workers recently applied laser annealing combined with a P-based SOD to dope n-type Ge (100) to form p-n junctions.[63] Photodetectors were fabricated to test the combined SOD and laser anneal process. Peak concentrations approached 1×10^{19} atoms/cm^3 for the laser annealed blanket samples. This is a shallower depth than that reported by Sharp and co-workers[60], but nevertheless is still quite a deep junction depth. A low junction bulk leakage current density of 5.4 mA/cm^2 and surface leakage current density of 5.4 mA/cm were achieved. The photodetector had a responsiveness of 0.46 A/W at 1.55 μm wavelength at 0 V bias. The 130-μm diameter detector had an approximately -3 dB bandwidth of 190 MHz, highlighting that laser doping is a useful method for forming Ge p-n junctions for microelectronic and photonic device applications. Peak chemical concentrations approached 1 × 1019 atoms/cm3 for the laser annealed blanket samples but with a junction depth of approximately 850 nm. Although the junction depth reported by Bao and co-workers is a shallower depth than that reported by Sharp *et al*.[63] future work may require the adaptation of an MLD process to this work to allow for shallower diffusion depths while maintaining the high P-concentration.

Most recently, Al-Attili and co-workers applied SOD using P-containing dopants from two different suppliers with differing physical properties to dope GeOI wafers for monolithic light sources on Si.[64] Using commercially available GeOI wafers, P-containing SODs from Emulsitone© and Filmtronics© at varying ratios of SOD-to-IPA, were spin-coated at a constant speed for a constant time. All samples were annealed at 580 °C. Active carrier concentrations approached 2×10^{19} atoms/cm^3. The study showed that SOD of Ge is not straightforward, and there are numerous practical process issues still to be resolved. In this work, most of the problems

arose from the poor adhesion between Ge and the BOX layer. In particular, uniform coating was very important to avoid the formation of cracks during annealing. Additionally the authors used a ramp of the bake temperature in the case of B and P SOD to minimise cracking of the SOD film which could lead to non-uniformity of the film. This could affect dopant dose uniformity during the rapid thermal anneal treatment to yield irregular dopant profiles. The minimisation of damage at the surface is one of the advantages of the MLD process and may be more suited to such applications.

Conclusions and Outlook

While the use of gas-phase and solution-phase surface chemistry for ultra-shallow doping of semiconductors is in its infancy, a vast body of research has accumulated over the last 5-10 years. In-situ doping of nanostructures, especially of bottom-up grown nanostructures, will remain challenging in terms of scale-up and reproducibility which, for now, makes it unsuitable for integration into CMOS manufacturing processes. Spin-on doping remains a cheap and effective method for doping semiconductor materials but much work remains to be done with respect to their use in nanoscale device structures. The majority of recent studies report that many practical issues remain, such as cracking of the SOD glass post RTA treatment. With device dimensions and geometries becoming smaller and three-dimensional, this aspect of the SOD process is undesirable for doping of such nanostructures. In contrast, the monolayer doping (MLD) technique is a strong candidate to replace ion-implantation, spin-on-doping and in-situ doping for thin-body devices and extreme-3D structures due to its conformality, controllable dopant profiles and lack of damage to the semiconductor substrates and devices. The process has also shown great promise on many materials which are relevant to the micro- and nano-electronics industries such

as Si and Ge, in addition to upcoming replacement material such as InGaAs. However, work must continue into applications of the MLD process on new device architectures such as junction-less transistors and gate-all-around transistors.[65,66] Aside from microelectronics, the MLD process has also been successfully applied with great success to solar cell materials and optoelectronic materials. Concurrently, there is a need for innovative improvements to metrological techniques to be made in order for the ultra-shallow junctions to be characterised to ensure conformality and abruptness. Additionally, the challenge of scaling up the MLD process from a Schlenk flask to a semiconductor processing line will need to be met if MLD is to be integrated into future CMOS fabrication facilities. There is much scope, in terms of surface chemistry, to finely tune the process to each material. To date, there have been no MLD studies using Al ,Ga, Sn and Sb dopants. Synthesis of suitable precursor molecules for these MLD processes will be challenging with respect to air-sensitivity and toxicity. Despite the challenges, the grafting of organic molecules onto semiconductor surfaces offers an exciting approach over the conventional doping methods. Applications of MLD to next-generation device architectures such as gate-all-around FETs and tunnel FETs may prove interesting and will require the bringing together of expertise from device physicists, chemists and engineers to realise the next building blocks for our electronic devices.

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