# The effect of interfacial charge on the development of wafer bonded silicon-on-silicon-carbide power devices.

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**Abstract**

A new generation of power electronic semiconductor devices are being developed for the benefit of space and terrestrial harsh-environment applications. 200-600 V lateral transistors and diodes are being fabricated in a thin layer of silicon (Si) wafer bonded to semi-insulating 4H silicon carbide (SiC) leading to a Si/SiC substrate solution that promises to combine the benefits of silicon-on-insulator (SOI) technology with that of SiC. Here, details of a process are given to produce thin films of silicon 1 and 2 µm thick on the SiC. Simple metal-oxide-semiconductor capacitors (MOS-Cs) and Schottky diodes in these layers revealed that the Si device layer that had been expected to be n-type, was now behaving as a p-type semiconductor. Transmission electron microscopy (TEM) of the interface revealed that the high temperature process employed to transfer the Si device layer from the SOI to the SiC substrate caused lateral inhomogeneity and damage at the interface. This is expected to have increased the amount of trapped charge at the interface, leading to Fermi pinning at the interface, and band bending throughout the Si layer.

**Introduction**

A novel silicon-on-silicon-carbide (Si/SiC) power device is being designed and fabricated, conceived to be both radiation hard and able to operate in extreme temperatures, both high and low. This is being produced specifically for space power conversion applications such as electric propulsion [1] and high voltage transmission [2], where efficient and, potentially, uncooled electronics could increase the overall lifetime, reliability, and science capability of a mission [3].

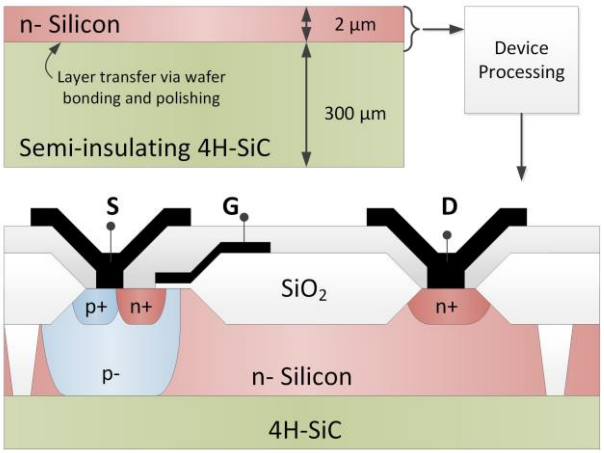


Figure 1: Top, the Si/SiC material system that has been developed. Bottom, proposed Si/SiC LD-MOSFET transistor.

The device concept [4, 5], shown in Figure 1, combines the benefits of silicon-on-insulator (SOI) technology (device confinement, radiation tolerance, high and low temperature performance) with that of SiC (high thermal conductivity, radiation hardness, high temperature performance). The Si/SiC substrates that result from the intimate connection of a 2 µm thick Si device layer and a semi-insulating SiC wafer, allow for the efficient handling of self-heating effects. In fact, given the

thickness of the Si, the thermal performance of the substrate is almost equivalent to SiC [5]. Therefore, in comparison to bulk Si or SOI, a Si/SiC device can operate either: in exactly the same ambient temperature, dissipating the same power, but with improved performance due to a reduction in the effects of self-heating; at a much higher temperature (as much as 100°C higher) for the same performance; or at the same temperature but at much higher power (as much as 4×), for the same performance. Furthermore, the Si/SiC substrate is expected to offer high radiation hardness. Immunity to single event effects is expected for the same reason as SOI, due to the small volume of active material. Compared to SOI, Si/SiC devices are expected to have a higher TID tolerance due to the absence of a thick buried oxide (BOX) layer under the active Si film and thus a lesser effect from radiation-induced oxide charge trapping on device performance. Finally, without the issues of SiC channel mobility, the thermal benefit of a SiC substrate can be utilised in the low-medium voltage range. Hence, power electronics solutions, both diodes and laterally-diffused (LD) MOSFETs have been optimised in simulation [4], for blocking voltages of 200 to 600 V.

In this paper, we will introduce an early method used to fabricate wafer bonded Si/SiC wafers. We will discuss the results of MOS capacitors and diodes fabricated in this substrate and show how the results produced were affected by the interface.

**Fabrication of Si/SiC Substrates**

100 mm Si/SiC wafers were fabricated by wafer bonding Norstel semi-insulating ($\geq 1.10^7$ Ω-cm) on-axis 4H-SiC to IceMOS Technology Ltd SOI with a buried oxide 2 µm thick, and a lightly n-doped device layer (5 - 45 Ω-cm). Wafers have been produced with a device layer thicknesses 1 and 2 µm thick. The full process used to develop the wafers can be seen in Figure 2.

Initial trials at IceMOS Technology Ltd, directly bonding the two virgin wafers via a number of hydrophilic and hydrophobic methods all resulted in either the handle wafer shearing under the strain, or in a high density of voids, visible in the hydrophobic bonded wafers in the inset to Figure 2. The problem of the voids was suspected to be the result of outgassing while the layers were undergoing a long high temperature anneal to form a permanent bond between the wafers. To overcome this problem, the first step taken in the bonding process (Figure 2) was to etch a grid of trenches 2 µm deep into the SiC surface prior to bonding, giving any gas an escape route during annealing. Next, after a proprietary surface plasma treatment, a hydrophobic bonding process was performed to form a temporary bond between the wafers. A 2 hour, 1200°C anneal was then performed to form a permanent bond between the wafers, and to remove an interfacial oxide, as shown previously in [6]. During annealing, the lattice mismatch between the materials caused a visible bow, the Si side of the wafer being convex. However, this still allowed, in the fourth step, for the Si handle wafer to be ground away down to the oxide layer, releasing the strain. Finally, the oxide, which had been the buried oxide of the SOI wafer, is simply removed with hydrofluoric acid.

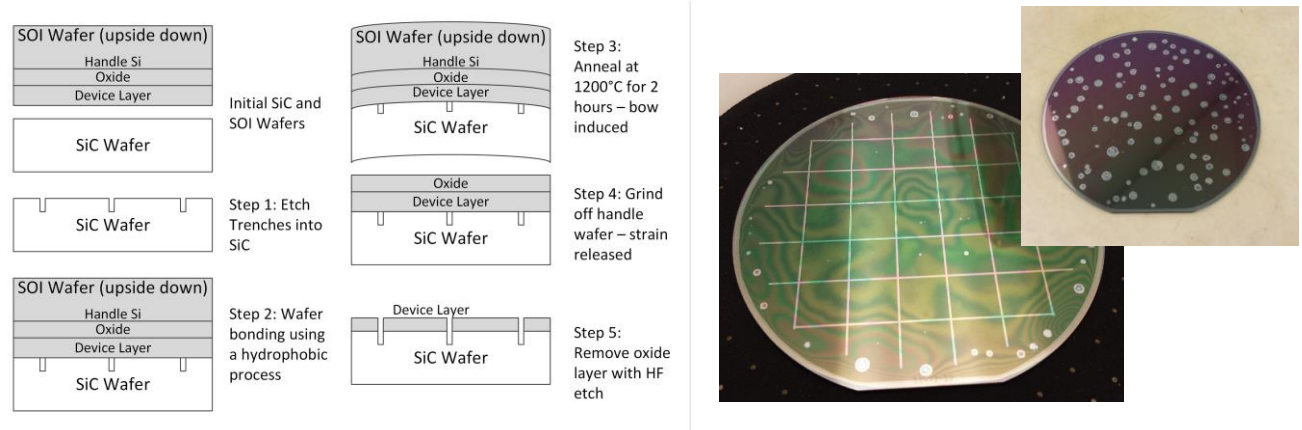


Figure 2: Left, the Si/SiC substrate fabrication process. Right, a 100 mm wafer bonded Si/SiC wafer with a 1 µm Si device layer. Inset, the results of bonding without the grid etching

**Electrical Characterisation**

Issues surrounding the doping of the Si device layers soon became apparent as simple test structures were made and tested in the Si/SiC substrate.

First, identical lateral MOS capacitors (MOS-Cs) were fabricated in both the original SOI wafers and within the Si top layer of the Si/SiC substrates. Ohmic contacts were formed using a heavily n-type arsenic implant and aluminium (Al) contact metal. The MOS interface consisted of 55 nm of thermally grown oxide, again using an Al contact, which was annealed in forming gas for 2 hours at 450°C. MOS-Cs formed in the original SOI wafers produced a typical n-type response, with the doping extracted from the slope of around $7\times10^{14}$ cm$^{-3}$. However, for the Si/SiC wafers, which use the identical Si device layer after it has been transferred onto the SiC, the C-V responses shown in Figure 4a suggested that the substrates were now p-type. Furthermore, the depletion capacitance was inconsistent from device to device, while oxide thickness extracted from each is grossly exaggerated. Both results suggested the presence of a second depletion region at the N+/p interface that skews this data extraction technique. Repeating the MOS-C fabrication process, this time using boron P+ implants to form the ohmic contacts, the results in Figure 4b consistently yield the correct oxide thickness, while a p-type doping of $1.9\times10^{15}$ cm$^{-3}$ was extracted.

Using the same P+ ohmic contacts, simple titanium (Ti) lateral Schottky diodes were formed in all the substrates. CV results on these structure (not shown) confirmed the doping and polarity above, while the results of I-V characterisation is shown in Figure 4c. Once again, a difference between the Si layer before and after layer transfer is shown, with the Si/SiC wafers displaying the behaviour of Schottky diodes with a very low barrier (~0.65 eV), which are hence leaky with poor turn-on characteristics. However, the SOI devices require more consideration. They still act like p-type devices of sorts, given that the device is on with a negative voltage. This means that the rectification is not happening from an n-type Schottky at the surface. However, as seen Figure 3, if the Si layer is n-type then there is now a p+-n diode, which will have formed next to the P+ implant. From Figure 4c we can see significant evidence that the rectification is coming from this p+-n, overcoming the relatively small n-type Schottky contact at the surface, given the SOI device has a much higher 'barrier' (~0.9 eV); a leakage current 100x smaller than the Si/SiC; and a much lower resistance (conductivity modulation).

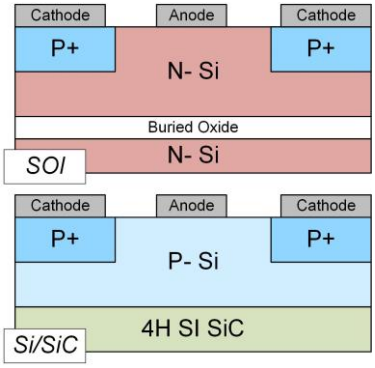


Figure 3: The layout of the SOI and Si/SiC diodes.

The results combined provided proof that the Si/SiC development process has caused the polarity of the Si layer to switch from n-type ($N_D = 7 \times 10^{14}$ cm$^{-3}$) to p-type ($N_A = 1.9 \times 10^{15}$ cm$^{-3}$).

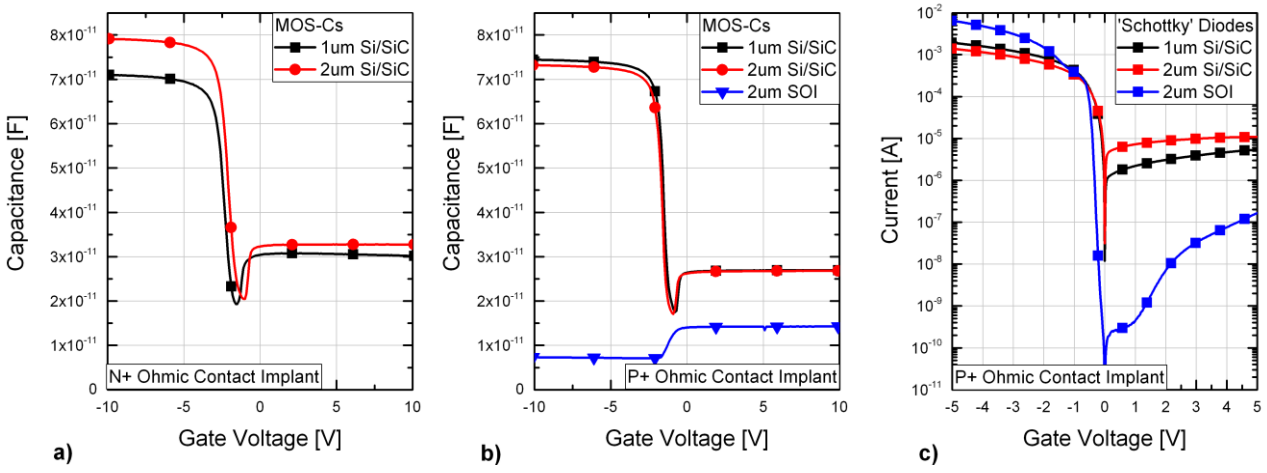


Figure 4: Electrical results from the 1 and 2 µm Si/SiC, and 2 µm SOI devices. C-V results are shown from MOS-Cs with a) N+ implanted ohmic contacts and b) P+ implanted ohmic contacts. c) I-V results from diodes formed after the formation of P+ ohmic contacts. The Si/SiC didoes appear to be Schottky diodes, the SOI, p-n diodes.

**Physical Characterisation of the Interface**

Transmission Electron Microscopy (TEM) imaging of the Si/SiC interface revealed the suspected reason for the change in polarity of the Si device layer. In areas, such as Figure 5 (top), a perfectly homogeneous interface was found with no interfacial oxide. In other places, a 1 nm amorphous layer is seen, presumed to be $SiO_2$. Furthermore, in places, features such as those seen in Figure 5 (bottom) are seen, where these are presumed to be pits or voids. This inhomogeneous interface is likely the source of significant charge trapped at the interface. This has been shown in [7] at the Ge/SiC heterojunction to cause Fermi-level pinning, and hence a conduction band offset very different from that expected. Here, it is expected that a high density of interfacial charge causes band bending, which in such a thin, lightly doped Si layer inverts the doping polarity of the entire layer resulting in the p-type behaviour witnessed.

Work is underway to further analyse and to counteract this effect, while a new low temperature bonding process is being trialled to minimise the stress imparted into the wafer pair during fabrication.

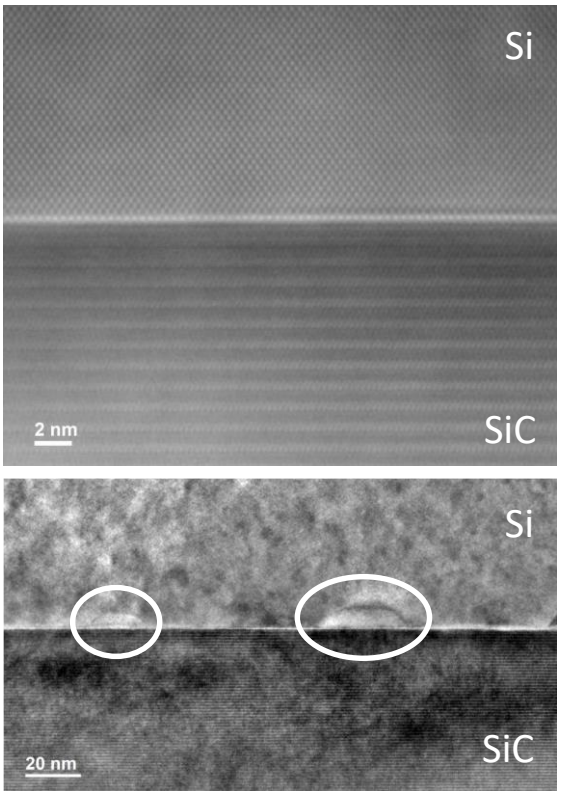


Figure 5: A TEM image of a homogeneous, oxide and defect free area of the Si/SiC interface. Bottom, another area, where voids or pits are clearly visible at the interface.

**Conclusion**

The results presented detail an on-going project to fabricate lateral power devices for space applications, using a novel Si/SiC substrate that better deals with the effects of self-heating and radiation. The process used to form the Si/SiC substrate employed a high temperature anneal to remove or reduce any oxide at the heterojunction interface. This is believed to have resulted in an inhomogeneous and damaged interface that will likely have increased the charge residing at the interface. Electrical results on the wafers showed that as a result, the same Si device layer, once transferred onto the SiC had completely changed its polarity from n-type ($N_D = 7 \times 10^{14}$ cm$^{-3}$) to p-type ($1.9 \times 10^{15}$ cm$^{-3}$).

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