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WAFER-SCALE VERY LARGE MEMORY WINDOWS IN GRAPHENE MONOLAYER/HfZrO FERROELECTRIC CAPACITORS

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Abstract

We have fabricated and electrically characterized at the wafer scale tens of metal-ferroelectric (HfZrO)-semiconductor capacitors and metal-graphene monolayer-ferroelectric (HfZrO)-semiconductor capacitors with the same top electrode dimensions. We have found that the memory windows of the capacitors containing graphene are 3-4 times larger than those of ferroelectric capacitors without graphene, and increase even more after annealing. This physical effect can be attributed to the additional electric field exerted by the graphene monolayer on the HfZrO ferroelectric, and to the negative thermal extension coefficient of graphene, respectively.

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Ferroelectrics, especially HfO_2-based ferroelectrics grown via Atomic Layer Deposition (ALD), are considered to be among the best substrates for graphene monolayers because their root mean square (rms) surface roughness is very small, around 0.2-0.3 nm [1], much smaller than the corresponding parameter of SiO_2, which ranges between 1 nm and 3 nm depending on the deposition technique [2], and even smaller or comparable with the rms surface roughness of hexagonal boron nitride (h-BN), which is about 0.4-0.6 nm [3]. In addition, h-BN monolayers cannot be deposited at the wafer scale, whereas HfO_2 is fully CMOS-compatible. Moreover, graphene/ferroelectric heterostructures behave similarly to suspended graphene structures in terms of mobility, due to the reduction of Coulomb scattering on charge impurities at the interface by the built-in field induced by the ferroelectric. Thus, an extraordinary room-temperature mobility of 70000 cm^2/Vs was obtained in field-effect-transistors (FETs) based on ferroelectrics in a backgate configuration [4], the result being still a record mobility in graphene FETs on substrates, surpassing all other graphene FETs on dielectrics such as Al_2O_3, SiC, SiO_2, Y_2O_3, or non-ferroelectric HfO_2.

The most studied devices based on graphene/ferroelectric structures are non-volatile memories, reviewed in [5,6], which are FETs with graphene acting as the transistor channel while the ferroelectric plays the role of the insulating dielectric for top- or back-gate configurations. Accumulation and depletion of carriers is controlled by the gate voltage, and the dependences of the drain voltage or drain conductance G versus gate voltage show a hysteretic behavior. When the gate voltage V_G reaches the threshold value $\pm V_C$, determined by the coercive electric field E_C and the thickness t of the

ferroelectric as $V_C = E_C t$, the carriers are depleted and G becomes zero. So, the drain conductance modulation by the gate voltage displays a bowtie-like shape. However, the development of these memories are impeded by the fact that ferroelectrics are not CMOS-compatible, displaying rather reduced sizes, while very often the graphene used in such devices is in the form of flakes, which affects drastically their reproducibility. The same lack of reproducibility is encountered in the recently developed applications of ferroelectrics as negative capacitances in atomically thin transistors. Here, MoS_2 flakes play the role of FET channel and show subthreshold swing (SS) below 60 mV/decade [7,8], although HfZrO ferroelectric (more precisely, $Hf_xZr_{1-x}O_2$) is grown at the wafer scale. On the other hand, HfZrO ferroelectrics are used for CMOS transistors at the wafer scale [9], showing SS lower than 60 mV/decade and, often, hysteretic drain-current versus gate voltage dependences. This latter behavior is detrimental in logic applications, but can be minimized via capacitor matching between dielectric and the ferroelectric layer.

In this paper, we have developed at the wafer scale graphene/HfZrO heterostructures, consisting of HfZrO ferroelectric layers grown by ALD directly on a Si wafer and CVD-grown monolayer graphene subsequently transferred on the HfZrO/Si wafer. We have fabricated HfZrO capacitors, as well as graphene/HfZrO capacitors, to study the physical effects of graphene monolayers on the properties of HfZrO capacitors on tens of structures.

The nominally 6-nm-thick $Hf_xZr_{1-x}O_2$ layers were grown at 250 ^oC on a *p*-doped Si(100) substrate by ALD using a Cambridge NanoTech F200 reactor. The ALD precursors were Tetrakis(ethylmethylamido) hafnium ($TEMAH_f$), Tetrakis(ethyl-

methylamido) zirconium (TEMAZr), and water. The oxide film was deposited in a laminate growth method employing 30 super cycles of $TEMAH_f$-H_2O-TEMAZr-H_2O. with all precursors separated by purges. Growth was assumed to be 0.1 mm/cycle for metal oxides with no nucleation delay between two materials. The thickness was confirmed by spectroscopic ellipsometry (Woollam M2000) to be 5.8±0.2 nm using a four layer optical model: air/$Hf_xZr_{1-x}O_2$/SiO_2/Si [10]. The chemical composition of the $Hf_xZr_{1-x}O_2$ films was investigated by X-ray photoelectron spectroscopy (XPS) using a Kratos AXIS ULTRA spectrometer with a source of monochromatic Al K_α, of 1486.58 eV, and was found to be $Hf_{0.45}Zr_{0.55}O_{1.76}$. More details on XPS measurements can be found in the Supporting Information. GIXRD patterns for the $Hf_xZr_{1-x}O_2$ thin film on high resistive Si (see Fig. S1) show the formation of the HfO_2(ZrO_2) orthorhombic phase with Pbc21 symmetry, indicating the ferroelectric behavior of the sample.

Further assessments of the ferroelectric property of the $Hf_{0.45}Zr_{0.55}O_{1.76}$ thin film was performed by Piezoelectric Force Microscopy (PFM) obtained using the NT-MDT Solver Pro P-47 AFM. Measurements were collected in piezoresponse force mode with a low-stiffness conductive probe (platinum-coated tip with a spring constant of 0.003-0.13 N/m (Tips Nano, CSG01/Pt)), by applying a bias between the conductive tip and the sample. Height and phase images were obtained by using 256×256 (x,y) positions (pixels). The images in Figs. 1(a) and 1(b) show the surface morphology and the phase while a bias was alternated between +2/-2 V. As already reported [11,12], the PFM phase image has a stripe domain structure induced by the electrically biased scanning tip, while the respective topography is characterized by a flat structure.

The ferroelectric behavior is evidenced in PFM measurements by the well-defined dark and bright contrast areas created as a function of the applied bias. Indeed, the probe oscillates at a frequency close to the characteristic frequency of the cantilever-probe-sample system, the oscillation of the cantilever in contact with the sample being resonant. For this reason, the oscillation phase differs for domains of the $Hf_{0.45}Zr_{0.55}O_{1.76}$ film with different orientations of the polarization vector. Further details of PFM investigations can be found in the Supporting Information.

After growing the ferroelectric layer, the wafer was cut into two chips. Graphene monolayer grown by CVD was transferred to the entire area of one chip by Graphenea, Raman spectroscopy showing the peaks in the G and 2D bands having a 2D/G ratio > 1.9 (the fingerprint of a graphene monolayer) over 80% of the graphene area, where the peak associated to the D band is missing (see Fig. S6). We note that graphene monolayer on HfZrO is not optically visible, as is graphene on SiO_2 with the thickness of 300 nm due to the high permittivity of the ferroelectric, which renders the lithography process more difficult.

The Cr (5 nm)/Au (100 nm) top electrodes with the dimensions 150 μm ×150 μm were deposited using a Temescal FC200 e-beam evaporation system, and were photolithographically configured using a standard lift-off process for both chips, with and without graphene. A bottom electrode of Al, with the thickness of 100 nm, was deposited in the same way on the back of the chips. Figure 2(a) illustrates a top view of the chip containing 88 metal-HfZrO-semiconductor (MFS) capacitors, the chip with graphene-MFS (GMFS) capacitors looking very similar. The cross-sections of the two types of devices are schematically represented in Fig. 2(b).

The electrical characterization of all fabricated devices (more than 160) were performed between the top electrode and the bottom electrode, assigned as the ground electrode, using a Keithley SCS 4200 station, all channels being equipped with low noise amplifiers and connected to a probe station enclosed in a Faraday cage. All experiments were carried out inside the probe station covered with the Faraday cage. Numerous measurements were performed on the devices at various voltage sweeps. Double sweeps were used to find hysteretic behavior. No fitting algorithms were applied during or after measurements. The yield was very good, with 85% of the MFS capacitors having similar capacitance-voltage (C-V) characteristics within ±5% dispersion, while the remaining 15% capacitors displayed distorted C-V dependences due to partial exfoliation of the thin (100 nm) metallic top electrodes under the action of the probe tips. For GMFS devices, 70% have shown similar C-V characteristics within ±5% dispersion. The remainder of the GMFS devices displayed modified C-V behaviours, again as a consequence of partial exfoliation of the contacts by the probe tips, but also due to incomplete coverage of graphene under some contacts. The imperfections of the graphene monolayer are unavoidable, being a product of either transfer or metallization process.

In Figs. 3(a) and 3(b) we have represented the C-V dependences for different sweeping ranges, at a frequency of 100 kHz. All C-V characteristics show a hysteretic behavior with a counterclockwise trace, due mainly to the interfacial layer between the ferroelectric and the Si substrate formed during ALD deposition [13,14]. Indeed, due to the specifics of the ALD growth method detailed above, a significant concentration of residual impurities, behaving as slow states, are expected to exist at the HfZrO/Si interface related to the hydroxyl groups originating from water. From Fig. 3 it follows

that the memory window (the width of the hysteresis loop) increases significantly in the presence of the graphene monolayer, the ratio *R* between the memory windows in GMFS and MFS capacitors being in average about 3.5. The respective memory windows and the ratio *R* are plotted in Fig. 4 with solid lines. We have checked (not shown) that these parameters do not vary with frequency, at least in the frequency range 100 kHz – 1 MHz. Similar wider memory windows in graphene-ferroelectric (PZT) FETs have also been observed [15]. The wider memory window in GMFS structures could be accounted for, in part, by the presence of a larger number of residual impurities/defects at the additional graphene/ferroelectric interface that form during the transfer process of graphene.

The memory windows initially increase with the applied voltage and then slightly decrease for larger applied voltage ranges, the largest memory windows being found for 4 V and 5 V for MFS and GMFS capacitors, respectively. The decrease of the memory window with increasing the sweeping voltage can be associated to an increased number of charge carriers penetrating through the very thin ferroelectric layer.

To investigate the conduction mechanism in MFS and GMFS structures, we have plotted their nonlinear current-voltage characteristics in Fig. 5(a). As expected, in structures containing graphene the current is higher since an additional number of charge carriers can contribute to conduction. The best fit for both types of structures was found for the Schottky emission mechanism, for which the current *I* at a given temperature *T* depends on the applied field *E* as [16]

$$I \propto T^2 \exp\left(\frac{-e(\phi - \sqrt{eE/4\pi\varepsilon})}{k_B T}\right). \quad (1)$$

As illustrated in Fig. 5(b), the fit is not perfect because of the variety of barrier heights associated to the traps at interfaces, which follow generally a disordered-induced-gap states model [17], and/or to the variation with the voltage V of the trapped charges/effective dielectric constant ε, due to changes of the potential barriers shapes with the applied bias. What is revealing for our study is that for both low and high bias ranges linear fitting regions can be found, depicted with blue lines in Fig. 5(b), the adjacent numbers indicating the slopes, and, most importantly, that the respective slopes for GMFS and MFS structures have similar ratios: 0.65 and 0.71 for the low and high voltage ranges, respectively. Because the thickness of the graphene layer is very small, the square roots of these ratios determine in fact the ratios between the effective fields in GMFS and MFS structures. More precisely, we have found that, in average the electric field on GMFS structures is about 0.82 times that in MFS structures for the same applied voltage. This means that part of the applied voltage falls on graphene and thus enhances the polarization P of the ferroelectric layer, acting as another cause of a wider memory window in GMFS compared to MFS. Indeed, as shown in [18], by treating graphene as a perfect metal with conductivity σ and mobility μ, the continuity of the electric displacement field D at graphene/ferroelectric interface requires that

$$\varepsilon_f E_f + P = \sigma / \mu \tag{2}$$

where ε_f and E_f are the electric permittivity and electric field in the ferroelectric layer. Thus, graphene modifies the polarization in HfZrO and, eventually, the potential

landscapes of trapped charges, the graphene conductivity being determined in turn by the applied voltage that falls on this layer.

Because the interfacial layers formed during ALD at the HfZrO/Si interfaces are mainly responsible for the hysteretic behavior of both MFS and GMFS capacitors, the observed memory windows are expected to be affected by a subsequent annealing process. Therefore, we have subjected the devices to an 80 ^{o}C annealing process in vacuum during 24 hours.

The C-V dependences after annealing for both MFS and GMFS capacitors are shown in Figs. 6(a) and 6(b), respectively, the corresponding memory windows and the R parameter being indicated in Fig. 4 with dashed lines. From these experimental data it follows that the capacitance, as well as the memory windows for MFS capacitors decreases after annealing, whereas for GMFS structures the opposite behavior is displayed. As a result, the parameter R increases to a record value of about 17.35 for the sweeping range (-4,4) V, by just inserting a graphene layer with a thickness of only 0.34 nm in the MFS structure.

The decrease of the hysteresis width after annealing in MFS structures is consistent with the findings in [13,14], where this behavior was attributed to the oxidation of the Si interface after annealing and/or to the reduction of hydroxyl groups in excess in the layer formed during ALD growth. The same phenomena should be present also in GMFS structures after thermal annealing, but the increase of the hysteresis width and capacitance in this case suggests that another mechanism should be accounted for. We attribute this behavior in GMFS capacitors to an opposite change in the physical ferroelectric film thickness/effective oxide thickness after annealing compared to MFS

structures. There are conflicting reports in literature regarding the behavior of this parameter after annealing (see [13] and [14]), which suggests that it depends on the particular structure under investigation. In our case, the HfZrO layer is subjected to different boundary conditions/strains during annealing in GMFS and MFS capacitors, because graphene is among the few materials with a negative thermal expansion coefficient (about -8×10^{-6} K^{-1} [19]), whereas both Cr and Au have large positive thermal expansion coefficients (about 5×10^{-6} to 8×10^{-6} K^{-1} and 14×10^{-6} K^{-1}, respectively [20]). As a result, GMFS capacitors outperform even more MFS capacitors in terms of memory window after annealing, showing an enhancement of this parameter after the thermal treatment.

In conclusion, the performances of MFS capacitors in terms of charge storage/hysteretic behavior can be improved several times by inserting monolayer graphene, the performance enhancement reaching values of about 17 after thermal treatment. Our experimental data could be explained by the strong influence of graphene on the polarization of the ferroelectric layer.

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Figure captions

Fig. 1 (a) Topography and (b) PFM phase images of the $Hf_{0.45}Zr_{0.55}O_{1.76}$ thin film

Fig. 2 (a) Optical microscope image (top view) of the chip containing metal-HfZrO-semiconductor capacitors with electrode dimensions of 150 μm ×150 μm and (b) cross-sections of the MFS and GMFS based on HfZrO ferroelectrics.

Fig. 3 Capacitance-voltage dependences for different voltage sweeps, at a frequency of 100 kHz, for (a) MFS and (b) GMFS capacitors before thermal annealing

Fig. 4 Memory windows for MFS and GMFS capacitors (left axis), and their ratio R (right axis) before (solid line) and after (dashed line) thermal annealing

Fig. 5 (a) Current-voltage characteristics for MFS and GMFS structures, and (b) their fitting corresponding to Schottky emission

Fig. 6 Capacitance-voltage dependences for different voltage sweeps, at a frequency of 100 kHz, for (a) MFS and (b) GMFS capacitors after thermal annealing

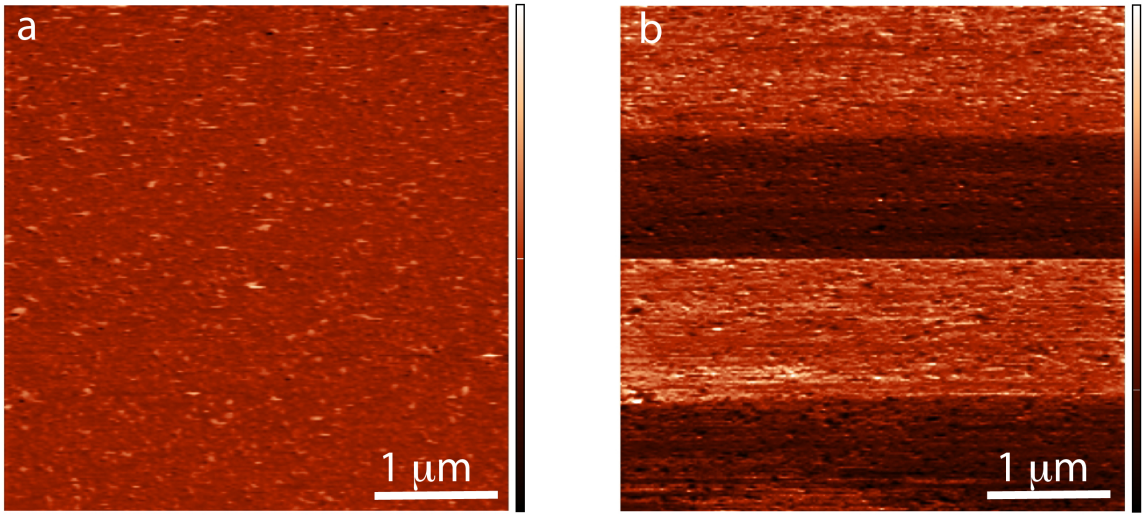
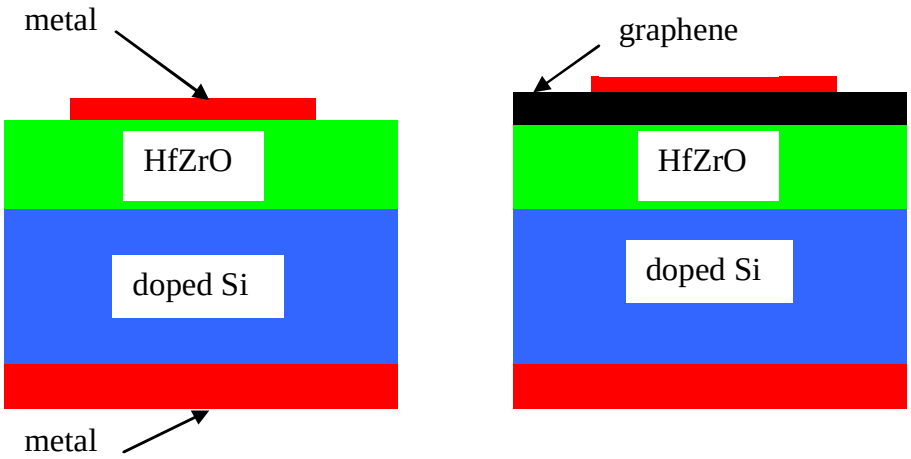


Fig. 1

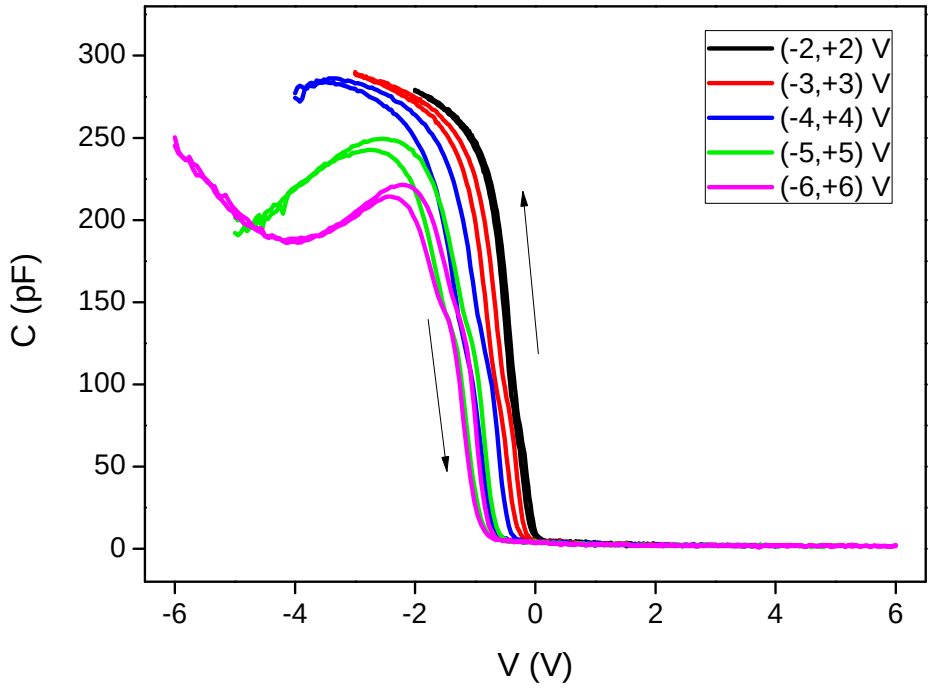


(a)

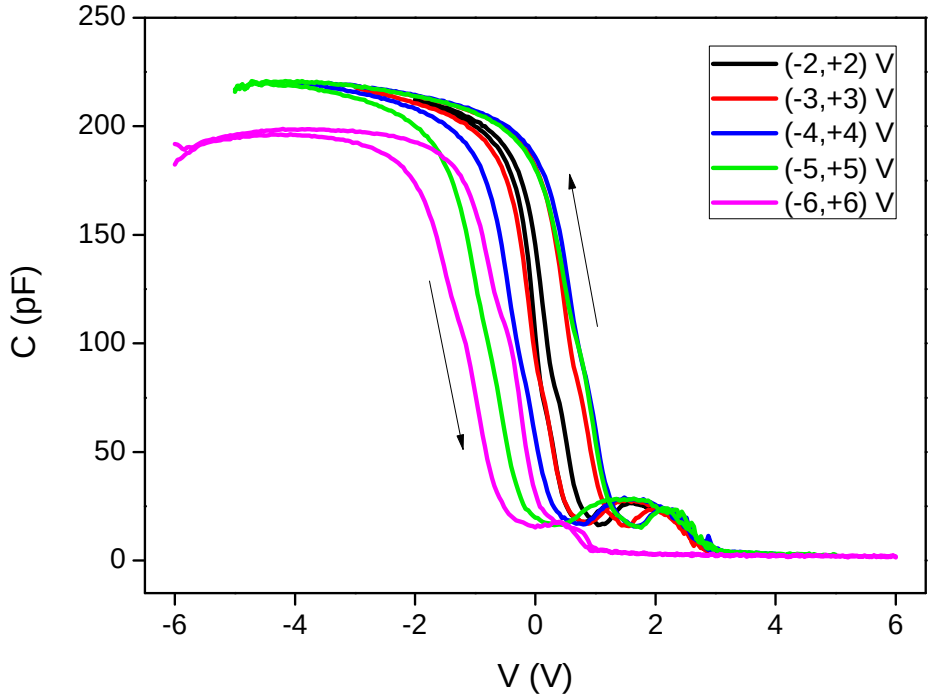


(b)

Fig. 2


(-2,+2) V
(-3,+3) V
(-4,+4) V
(-5,+5) V
(-6,+6) V
C (pF)
V (V)
300
250
200
150
100
50
0
-6
-4
-2
0
2
4
6

(a)


(-2,+2) V
(-3,+3) V
(-4,+4) V
(-5,+5) V
(-6,+6) V
C (pF)
V (V)
250
200
150
100
50
0
-6
-4
-2
0
2
4
6

(b)

Fig. 3

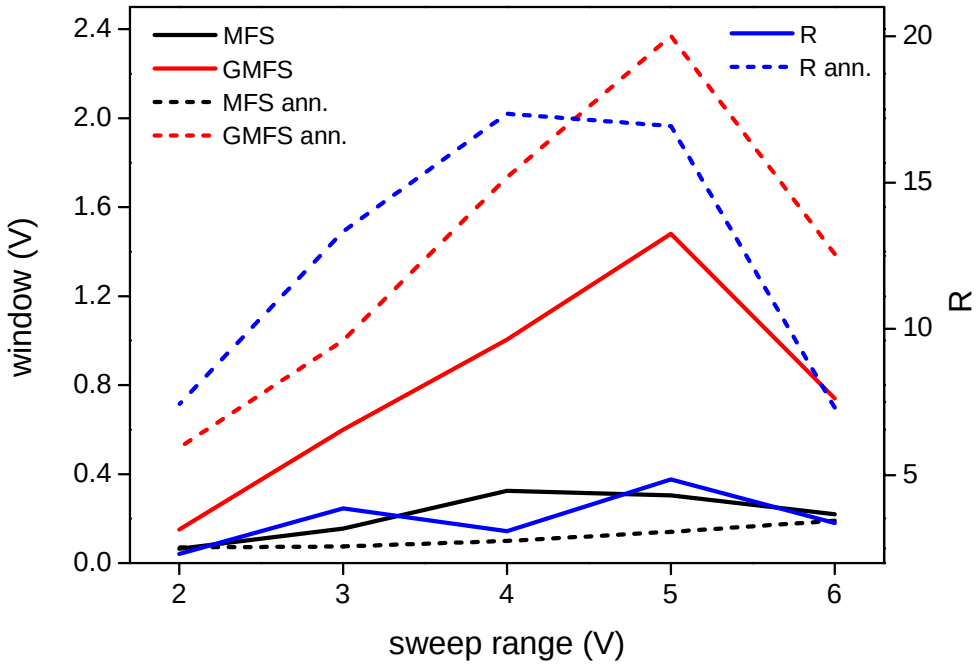
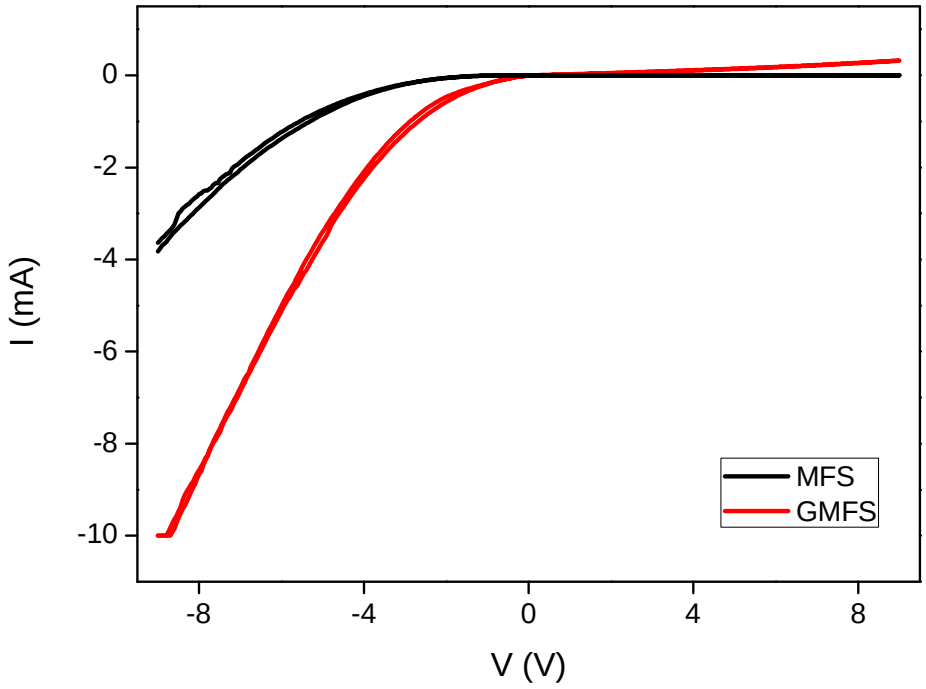
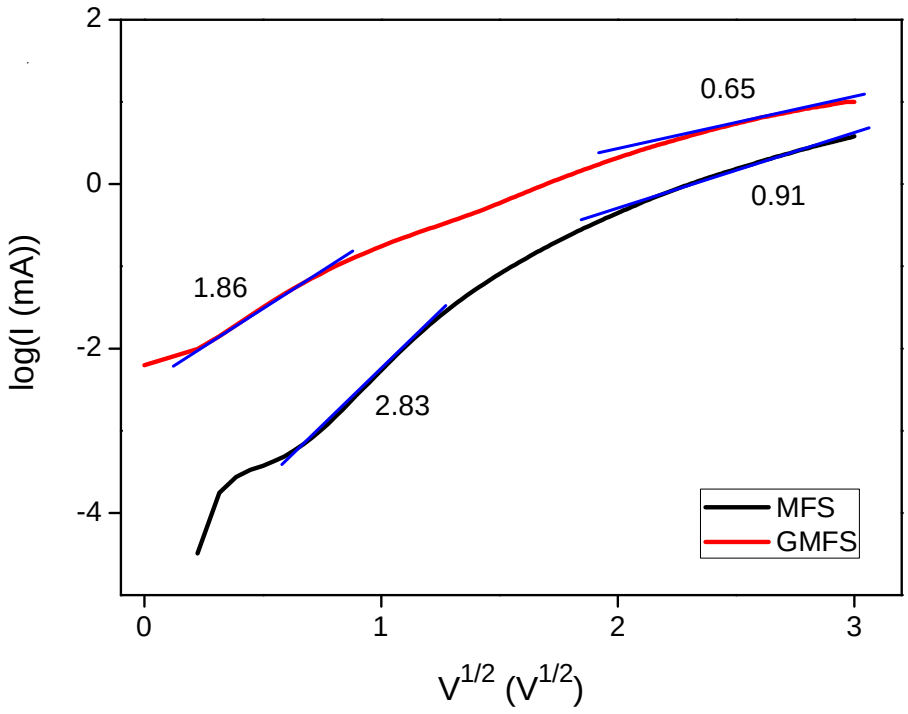

MFS
GMFS
MFS ann.
GMFS ann.
R
R ann.
window (V)
R
sweep range (V)
2.4
2.0
1.6
1.2
0.8
0.4
0.0
20
15
10
5
2
3
4
5
6

Fig. 4

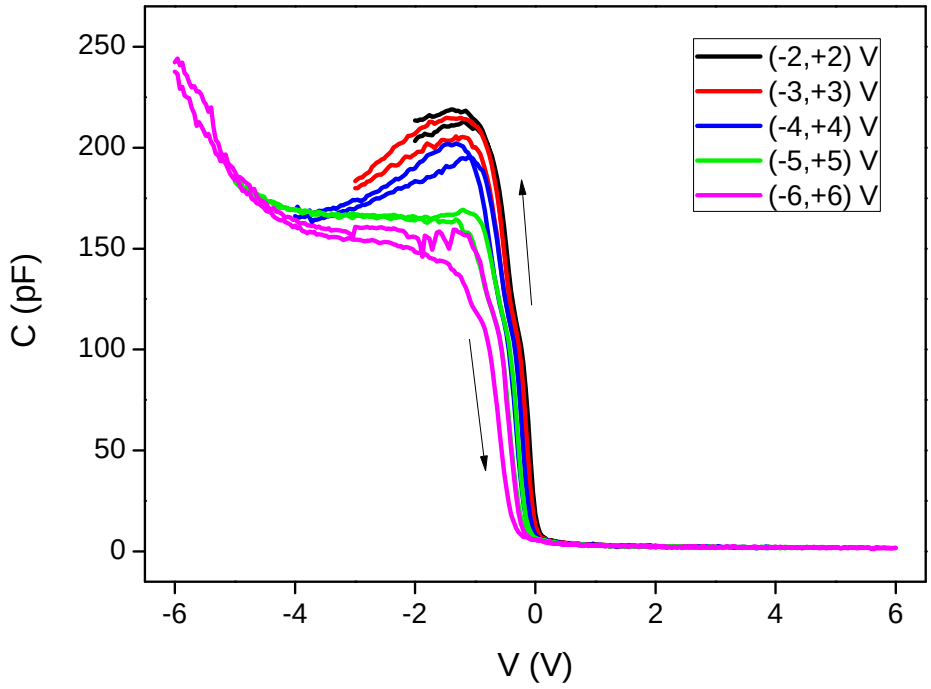

0
-2
-4
-6
-8
-10
I (mA)
-8
-4
0
4
8
V (V)
MFS
GMFS

(a)

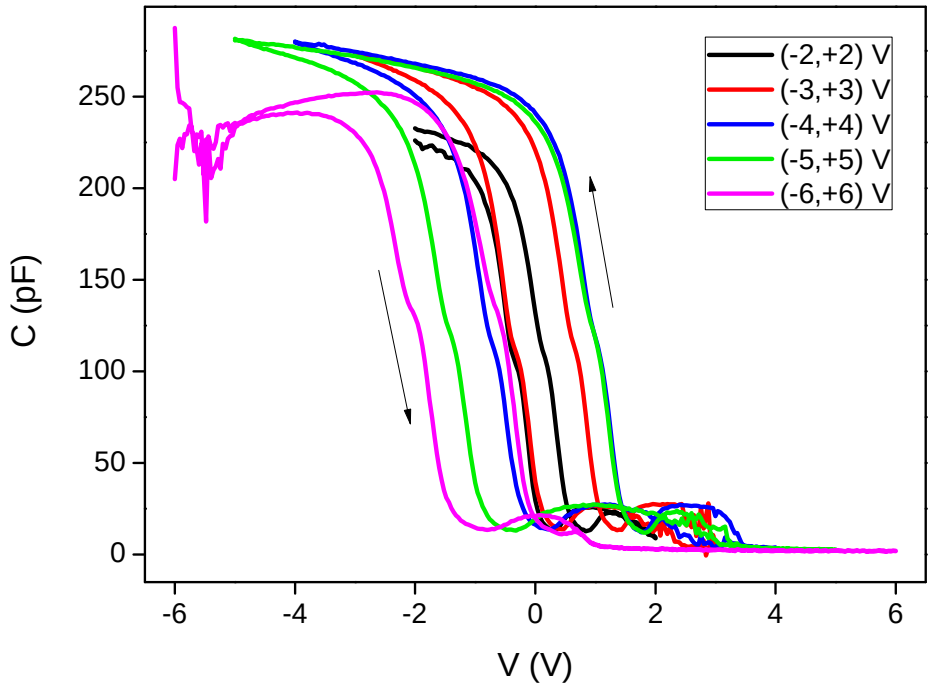

2
0
-2
-4
log(I (mA))
0.65
0.91
1.86
2.83
MFS
GMFS
0
1
2
3
V1/2 (V1/2)

(b)

Fig. 5


(-2,+2) V
(-3,+3) V
(-4,+4) V
(-5,+5) V
(-6,+6) V
C (pF)
V (V)
250
200
150
100
50
0
-6
-4
-2
0
2
4
6

(a)


(-2,+2) V
(-3,+3) V
(-4,+4) V
(-5,+5) V
(-6,+6) V
C (pF)
V (V)
250
200
150
100
50
0
-6
-4
-2
0
2
4
6

(b)

Fig. 6

Supporting Information for

WAFER-SCALE VERY LARGE MEMORY WINDOWS IN GRAPHENE MONOLAYER/HfZrO FERROELECTRIC CAPACITORS

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A. XPS

The composition of the $Hf_xZr_{1-x}O_2$ films were investigated by X-ray photoelectron spectroscopy (XPS) using a Kratos AXIS ULTRA spectrometer with a source of monochromatic Al Kα, of 1486.58 eV. The Hf*x*Zr1-*x*O2 film is clearly non-stoichiometric, exhibiting a significant oxygen deficiency (see Table I).

The grazing incidence X-ray diffraction (GIXRD) pattern of the $Hf_xZr_{1-x}O_2$ film has been measured on a Rigaku Smartlab system using the Cu K_α line at an angle of incidence of 0.35^o. The measured GIXRD pattern is presented in Fig. S1 and shows two broad peaks, at around 30.5^o and 55^o, which were previously assigned to $(111)_O$ and $(022)_O/(220)_O$ reflections of the $HfO_2(ZrO_2)$ orthorhombic phase with Pbc21 symmetry, which is ferroelectric [S1,S2,S3]. The corresponding Si substrate peaks are also indexed in Fig. S1.

Table I. XPS data for the Hf*x*Zr1-*x*O2 sample

Identified composition	Name	Position	Concentration [%]
$Hf_{0.45}Zr_{0.55}O_{1.76}$	O 1s	530.4	62.1
	C 1s	284.7	2.6
	Zr 3d	182.4	15.7
	Hf 4f	17.1	15.7

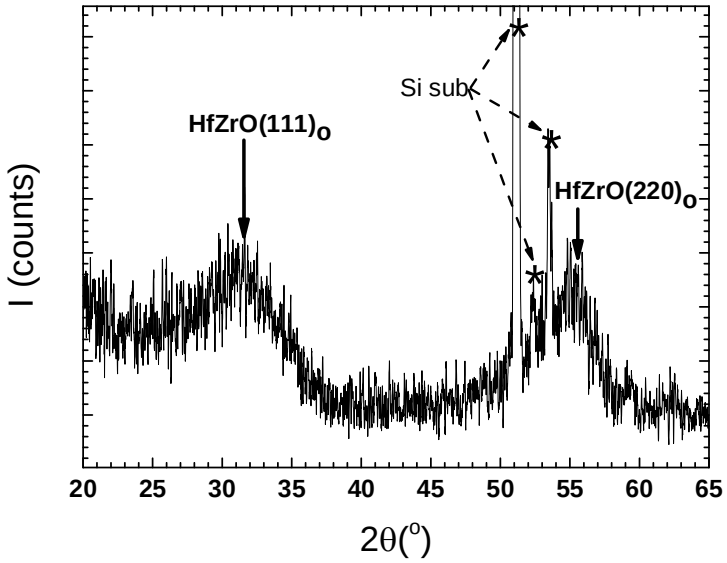


Fig. S1 *GIXRD pattern for the $Hf_xZr_{1-x}O_2$ thin film on high resistive Si. The peaks at 30.5° and 55° are assigned to $(111)_O$ and $(022)_O/(220)_O$ reflections of the $HfO_2(ZrO_2)$ orthorhombic phase with Pbc21 symmetry.*

[S1] T.S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, Ferroelectricity in hafnium oxide thin films, Appl. Phys. Lett. 99, 102903 (2011).

[S2] M. Dragoman, M. Modreanu, I.M. Povey, S. Iordanescu, M. Aldrigo, C. Romanitan, D. Vasilache, A. Dinescu, and D. Dragoman, Very large phase shift of microwave signals in a 6 nm $Hf_xZ_{1-x}rO_2$ ferroelectric at ±3 V, Nanotechnology 28, 38LT04 (2017).

[S3] A. Pal, V.K. Narasimhan, S. Weeks, K. Littau, D. Pramanik, and T. Chiang, Enhancing ferroelectricity in dopant-free hafnium oxide, Appl. Phys. Lett. 110, 022903 (2017).

B. PIEZOFORCE MICROSCOPY (PFM) ON FERROELECTRIC HfZrO THIN FILM

Experimental data were extracted by using the NT-MDT Solver Pro P-47 AFM. Measurements were collected in the piezoresponse force mode though a low-stiffness conductive probe (Platinum-coated tip with a spring constant of 0.003-0.13 N/m (Tips Nano, CSG01/Pt)). Images were obtained by scanning a region of 256 x 256 points, over 500 nm x 500 nm area. Topography evaluation was performed by Nova Software using only a fit line flatten correction. The frequency and amplitude of the oscillating voltage applied in Piezoresponse Force Microscopy (PFM) were around 100 KHz and 0.3 V, respectively.

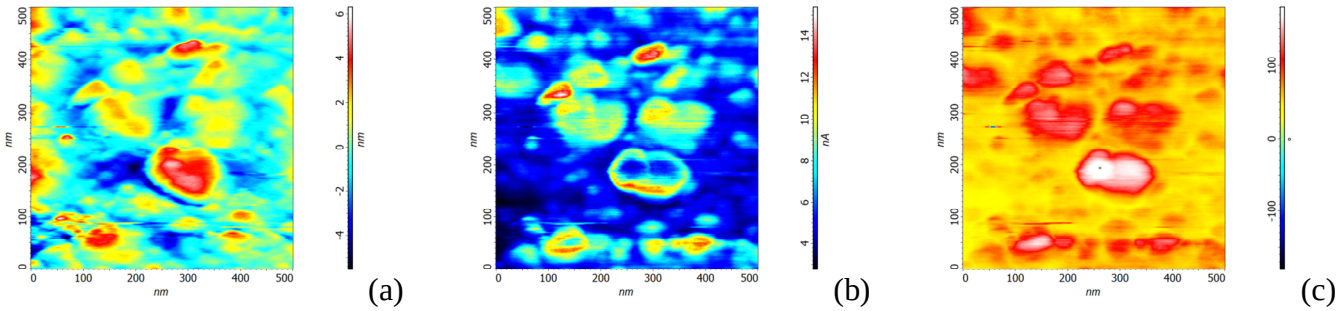


Fig. S2 *(a) Topography, (b) PFM magnitude and (c) PFM phase. The images were acquired by applying a modulating voltage with a zero-mean value (V_{DC} = 0).*

In the PFM technique, the conductive probe is brought into contact with the sample. The piezoelectric activity is stimulated with an AC voltage applied between the tip and the sample, which causes the periodic expansion or contraction of the sample while the scanning tip is working in the contact mode. The changes of the sample dimensions are detected by the cantilever deflection. In this technique, the amplitude (PFM amplitude) and phase (PFM phase) of the vertical tip displacement are recorded by a lock-in amplifier. The images reported in Figures S2(a), (b) and (c), respectively, show the surface morphology, the PFM amplitude and PFM phase recorded with a zero DC voltage applied between tip and sample. The images reported in Figures S3(a), (b) and (c), respectively, show the surface morphology, the PFM amplitude and PFM phase recorded while the bias DC voltage was changed between 0 V and +/- 4 V, highlighting the ferroelectric behavior of the sample.

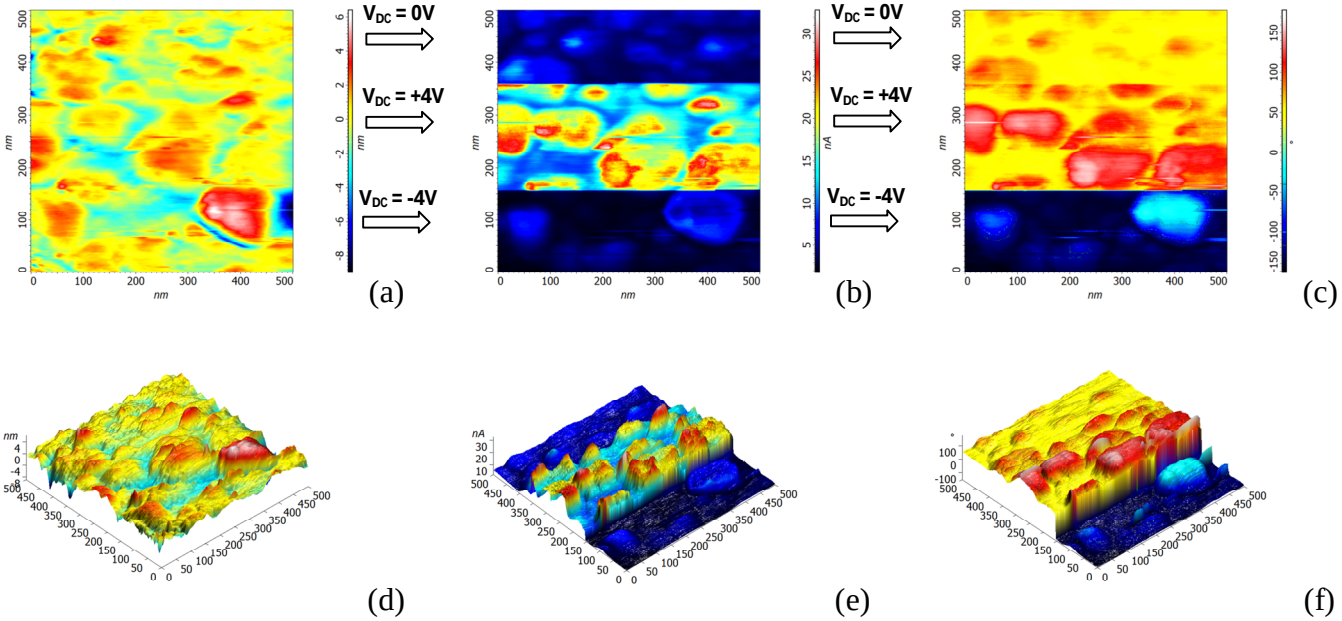


Fig. S3 *(a, d) Topography, (b, c) PFM magnitude and (c, f) PFM phase. During the scan the DC voltage is varied according to the sequence: V_{DC} = 0, V_{DC} = +4 V and V_{DC} = -4 V, inducing a different polarization in the material.*

Studies of local properties can be performed at individual surface locations by recording the amplitude and phase signals when the bias DC voltage is changing between defined limits with different polarities. The amplitude versus bias voltage curve defines the local strain response, while the phase versus bias voltage dependence reflects the sample polarization behavior, as reported in Figs. S4-S5, for two different points, where the blue and red curves correspond to different sweeping directions.

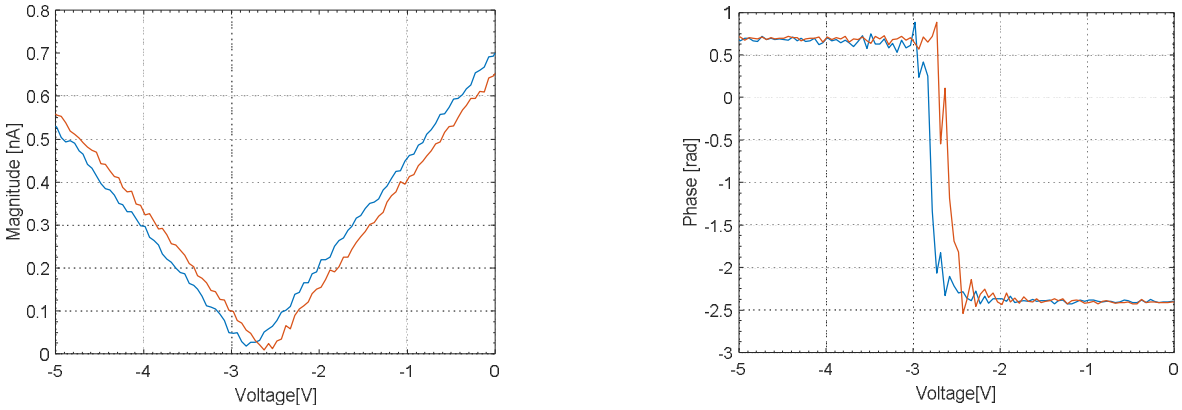


Fig. S4 *PFM spectroscopy obtained by varying the tip-sample DC voltage. (a) PFM Magnitude and (b) PFM Phase curve recorded in a single point with the tip in contact with the surface.*

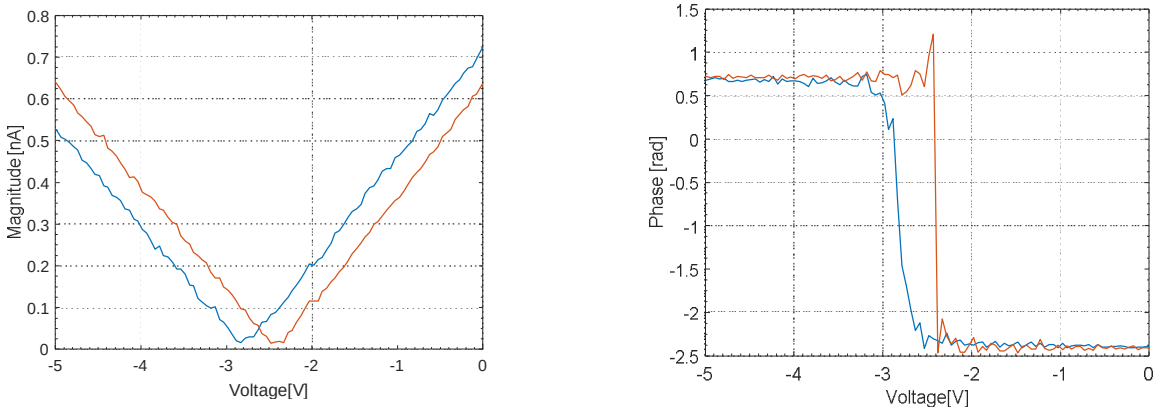


Fig. S5 *PFM spectroscopy obtained by varying the tip-sample DC voltage. (a) PFM Magnitude and (b) PFM Phase curve recorded in a single point with the tip in contact with the surface.*

C Raman spectrum of graphene on HfZrO

The Raman spectra were performed by dr. Florin Comanescu, IMT Bucharest using a Labram Hr800 Raman spectrometer, at a laser wavelength of 633 nm. From the Raman spectrum displayed in Fig. S6, it can be seen that the D band is missing, meaning a high-quality monolayer. The ratio between the intensities of 2D and G peaks is around 2, which confirms that we have a single layer of graphene. The same spectrum can be retrieved on a large part of graphene/ferroelectric monolayer.

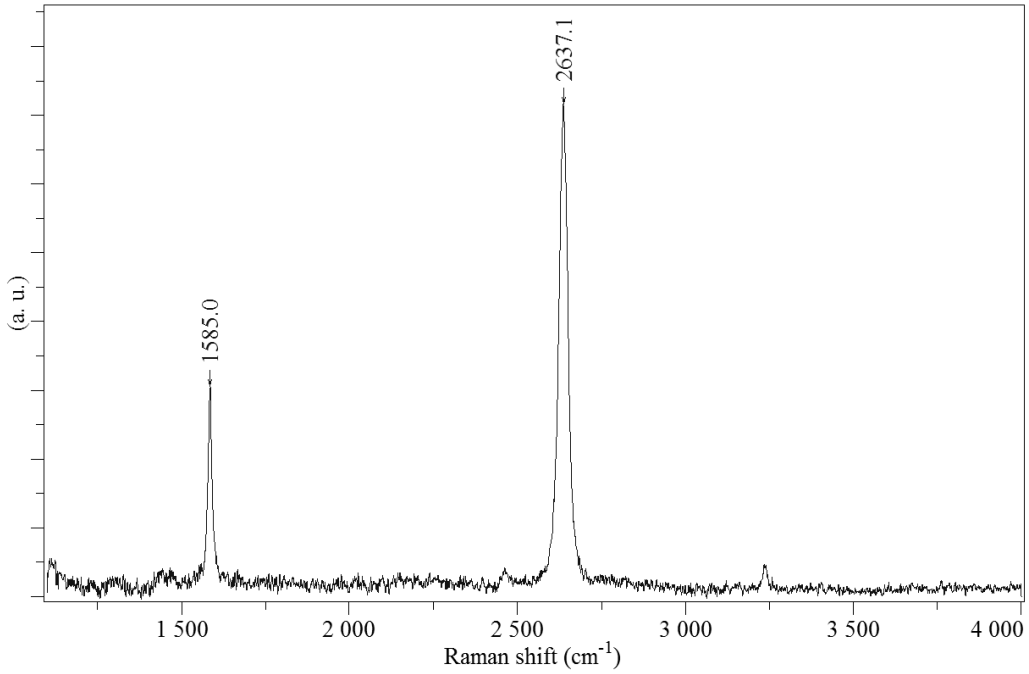


Fig. S6 *Raman spectrum of graphene/HfZrO*