Thin-film Magnetics-on-Silicon Integrated Transformer for Isolated Signal and Power Coupling Applications

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Abstract

Smart Switches for future generation power systems will be realised by densely integrating GaN switches with CMOS drive and control logic, enabling higher switching frequencies, greater efficiency and smart gate driver features such as for improved switch protection and offering improved control telemetry. The realization of such systems will benefit from the integration of power coupling and signal isolating transformers, either on-chip or at package-level. This work reports the development of a thin-film magnetics-on-silicon (MoS) micro-transformer for functional (operational grade insulation) galvanic isolation of the gate drive logic signal. The micro-transformer will be integrated with GaN switches and CMOS logic circuits to implement applications such as high frequency resonant LLC converter, in lower voltage applications, such as for 12, 24 or 48V systems.

1 Introduction

The emergence of portable electronic devices and equipment in the recent decades has driven the development of miniaturized and more highly integrated power converters. This trend has motivated research interest towards the integration of passive magnetic components for power system-in-package (PwrSiP)/ on-chip (PwrSoC) applications. The integration of thin-film magnetics components on silicon can substantially reduce the size of power module, while enhancing the system efficiency [1]. This work reports the development of a thin-film magnetics-on-silicon (tf-MoS) integrated micro-transformer for galvanic signal isolation. The target application of this micro-transformer is for gate drive, [2]-[6], logic signals transfer in a high frequency (10 – 30 MHz) LLC resonant converter. The tf MoS gate drive transformer performs drive signal isolation for both of the primary side bridge switch drives and the secondary side synchronous rectifiers.

In [3] a monolitic coreless transforemer solution for galvanic isolation in gate driver application is demonstrated using 3.3GHz modulated control signal. 3D TSV (Through-Silicon-Via) transformer technology for low frequency (tens of MHz) high-voltage digital isolator gate driver applications is proposed and demonstrated in [5]. In this work we used and edge triggered pulse generator and pulse transformer-coupled gate driver circuit to allow operation at any switching frequency up to a limit determined only by the minimum edge generated pulse width.

Thin-film power magnetics technology may become available as a standard technology offering from the major pure-play silicon foundries, [7], [8]. This will enable a step function improvement in volume and cost for ultra-low profile and very highly integrated point-of-load (POL) and system-on-chip (SoC) voltage regulation circuits [7]-[8]. This work suggests that tf-MoS transformer devices will enable applications such as smart gate drivers requiring galvanic signal and power isolation, or other converter topologies requiring coupled-inductors or transformers.

2 Device design

2.1 Transformer design specifications

The target application of the integrated MoS (Magnetics-on-silicon) transformer is functional grade (per IEC950, EN60950) galvanic isolation for signal and power coupling in a custom CMOS gate driver IC. The transformer design specifications are tabulated in Table 1. The insulation level has not yet been fully explored, but the distance through the dielectric between the coils (20µm spacing) suggests a level of up to 1.5kV is achievable.

Table 1 Gate drive isolation transformer specifications

Parameters	Values
Turns ratio	1:1
Transformer volt-seconds	10 V.ns
Magnetizing inductance (L_{11})	40 nH
Swtching frequency (f_{SW})	20 MHz
Coupling coefficient (k_{12})	> 0.8
DC resistance (R_{DC})	< 500 mΩ
Saturation current (I_{SAT})	> 500 mA
Parasitic capacitance (C_{12})	As low as possible (to minimise CM injections) duw to switching node dV/dt.

2.2 Design of tf-MoS Transformer

The tf-MoS transformer is designed as a solenoidal structure, with the thin-film magnetic core wrapped by interleaved primary and secondary copper windings (Figure 1).

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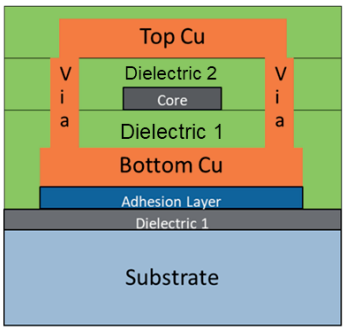

Figure 1 Schematic cross-section view of the thin-film magnetics on silicon solenoid transformer

The solenoid construction is cost-effective for micro-fabrication as it involves deposition of a single layer magnetic core. Laminated thin films of a cobalt based amorphous alloy (Co-Zr-Ta or "CZT") and dielectric (AlN) layers are used to create the magnetic core. The complex permeability spectrum of a laminated CZT/ AlN stack is shown in Figure 2. The real component of the permeability remains stable up to 100 MHz frequency, while the imaginary component (contributes to loss) remains low. Therefore, the CZT/AlN multi-layer stack is suitable for high frequency low loss integrated passive magnetic device applications.

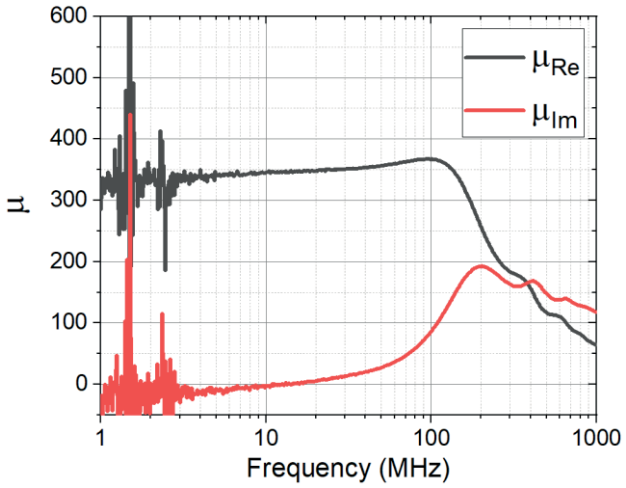

Figure 2 Complex permeability spectrum for 20-layer CZT/ AlN (250nm/ 15nm) stack.

A thermally grown silicon oxide layer on the substrate wafers provide electrical isolation between the copper traces and the silicon (p-doped, conductivity 20 S/m) substrate. The 3D solenoid model of the thin-film transformer is designed in Ansys Maxwell FEA (finite element analysis) package (Figure 3(a)). The magnetic flux density distribution in the magnetic core is plotted in Figure 3(b), where the maximum flux density (~ 1T) is in the central region of the solenoid core.

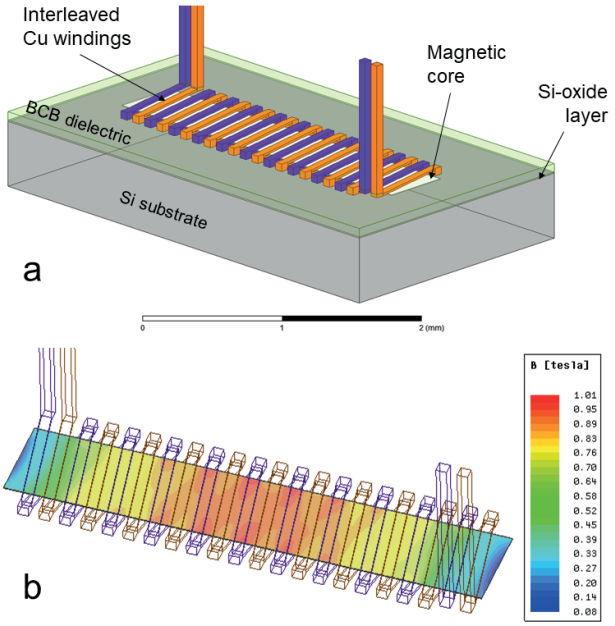

Figure 3 a) 3D FEM model of the thin-film magnetics-on- silicon transformer. b) Magnetic flux density distribution in the core for 20 MHz 500 mA applied current.

In order to reduce common mode capacitive current spike injections from input to the output of the transformer, a low parasitic capacitance between the primary and secondary windings is required. The electrostatic FEM model of the transformer indicates that most of the parasitic capacitance contributions are due to the capacitances between the copper traces and the silicon substrate.

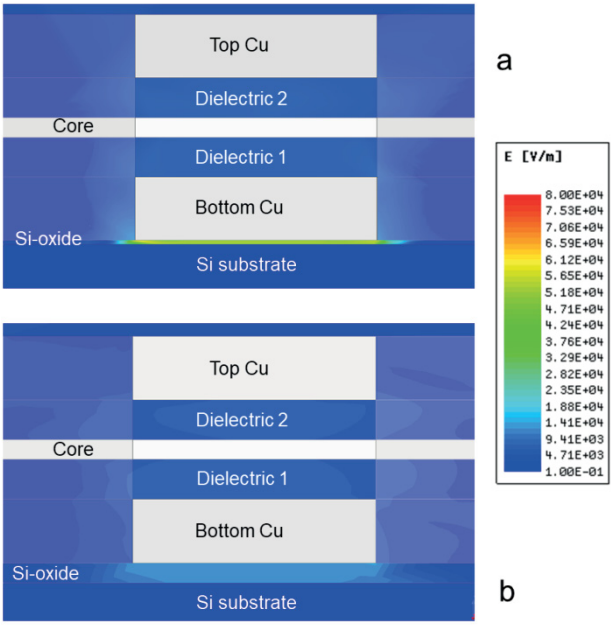

Figure 4 DC Electric field distribution in vertical cross-section of transformer for 1V potential difference between copper windings. Si-oxide thickness a) 1μm, b) 5μm to investigate parasitic capacitance.

The simulated DC electric field distribution between the transformer windings and the silicon substrate for two dif-

ferent thermal oxide thickness (1µm and 5µm) are illustrated in Figure 4. The results show ~3X reduction in electric field intensity between copper traces and silicon substrate due to 5X thicker oxide, which results into ~3X reduction in the parasitic capacitance between the transformer windings. The FEM simulation results are summarised in Table 2.

Table 2 Summary of FEM simulation results

Parameter	Values	
Swtching frequency (f_{SW}) [MHz]	20	
Magnetizing inductance (L_{11}) @ f_{SW} [nH]	39.3	
Coupling coefficient (k_{12})	0.83	
DC resistance (R_{DC}) [mΩ]	310	
Quality factor @ f_{SW}	13.7	
Si-oxide base thickness [µm]	1	5
Parasitic capacitance (C_{12}) [pF]	10.76	3.68

3 Fabrication of tf-MoS Transformer

The optimized solenoidal micro-transformer is fabricated in a CMOS compatible back-end-of-line (BEOL) process. A layer of thick thermal oxide (1µm and 5µm on either of two substrates) is grown on the silicon wafer. Ti/Cu seed layers (20nm/ 200nm) are sputter deposited on the wafer. Bottom copper traces are patterned by photolithography, and electroplated within photoresist moulds. Then the vias are patterned, and electroplated, followed by spin-coating a layer of dielectric. The anisotropic CZT/ AlN laminated core layer is sputter deposited on the spin-coated dielectric layer and patterned by lift-off lithography. A second dielectric layer is spun-on the magnetic core, and the vias are opened by dry etching the dielectric layers. The top copper trace are then patterned, and electroplated to complete the transformer windings. The fabricated transformer device is shown in Figure 5.

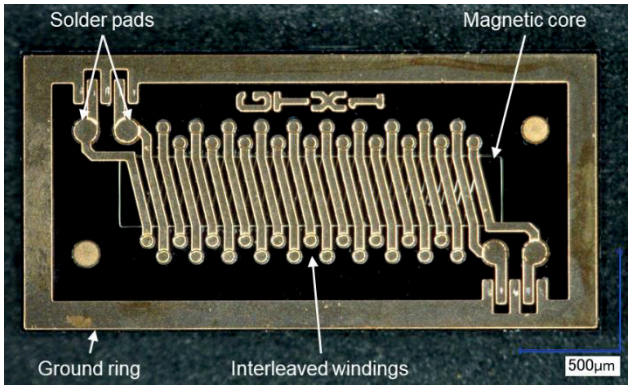

Figure 5 Fabricated micro-transformer.

4 Device characterization

The fabricated tf-MoS transformers are characterized using 4-port network analyser and 100 um pitch GSGSG RF probes in a frequency range 10 MHz – 1 GHz. Transformer electrical parameters such as magnetizing inductance, coupling coefficient, AC resistance, Quality factor are extracted from the S-parameters.

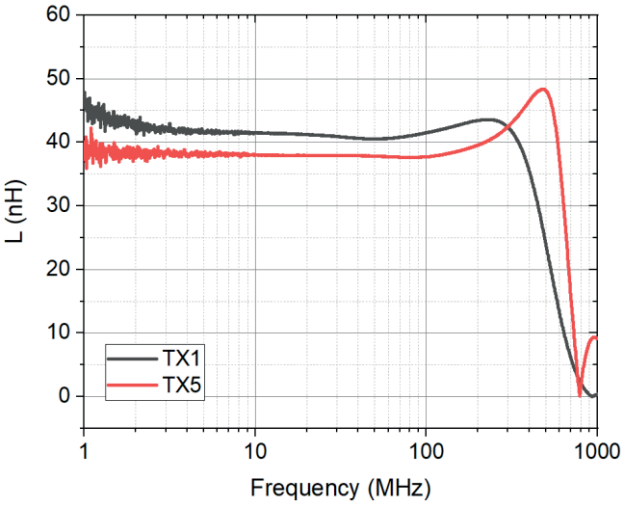

Figure 6 Magnetizing inductance vs frequency plots for devices with 1µm (TX1) and 5µm (TX5) thick base Si-oxide.

The magnetizing inductance (Figure 6) and coupling coefficients (Figure 7) remain stable up to 200 MHz frequency, which suggests a broad frequency range of operation.

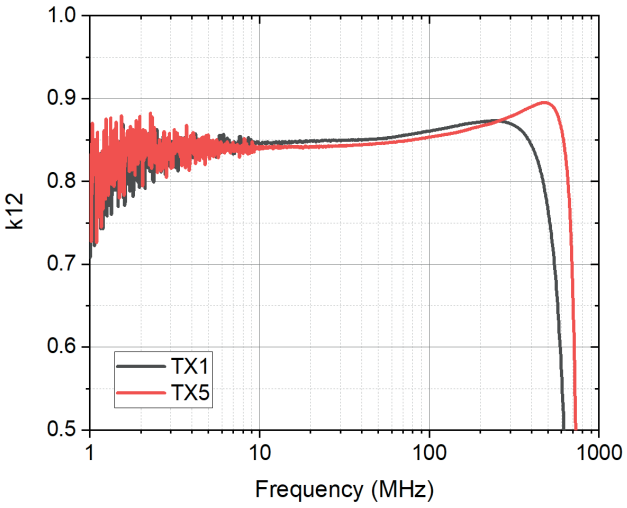

Figure 7 Coupling coefficient vs frequency plots for devices with 1µm (TX1) and 5µm (TX5) thick base Si-oxide.

The measured low frequency (1 MHz) resistance is ~ 300 mΩ, which is very close to the simulated DC resistance value of 310 mΩ. Also, the AC resistance at 20 MHz increases approximately 30% from the DC value, which indicates low loss contributed by the magnetic core (Figure 8).

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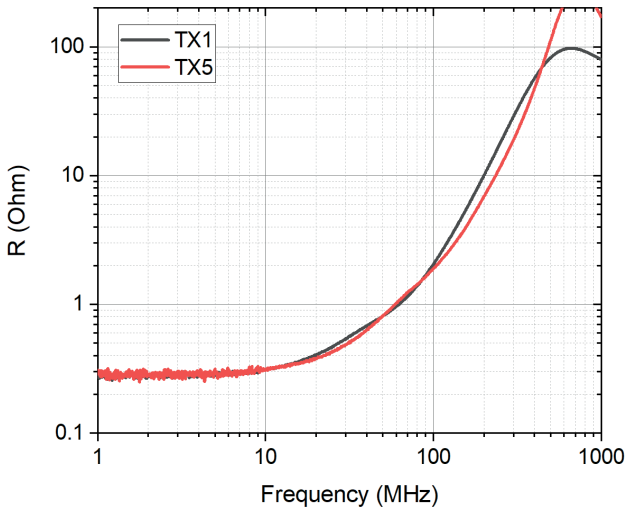

Figure 8 AC resistance vs frequency plots for devices with 1µm (TX1) and 5µm (TX5) thick base Si-oxide.

Quality factors of 12.8 and 12.6 are achieved for the transformer windings at the switching frequency (20 MHz). However, the quality factors reach their peak values (16 for TX1, 15.2 for TX5) at 60 MHz and 40 MHz respectively. These results demonstrate that the transformers are capable of operating at any frequency in the range 20 MHz to 100 MHz. The measured data are summarized in Table 3 and exhibit compliance with the gate drive transformer specifications outlined in Table 1.

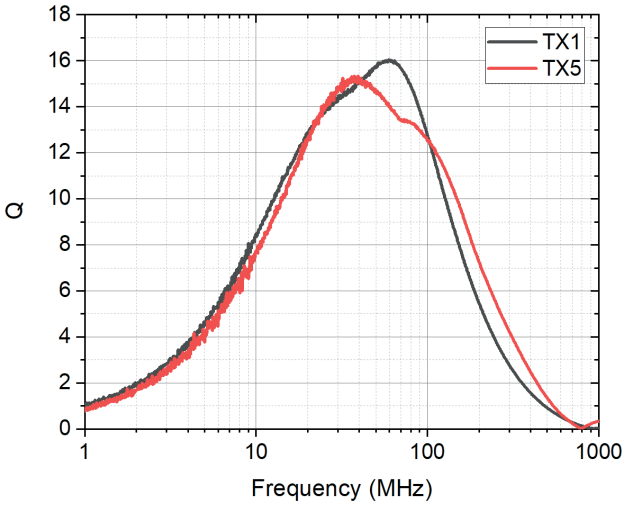

Figure 9 Quality factor vs frequency plots for devices with 1µm (TX1) and 5µm (TX5) thick base Si-oxide.

The parasitic capacitance between the primary and secondary windings was obtained from the measured S-parameter data by fitting the extracted Y parameters to an equivalent circuit model of the transformers. The results show a 3X reduction in C_{12} (primary to secondary capacitance) with the 5 µm thick oxide, matching the capacitance reduction predicted by the 3D FEM model.

The low parasitic I-O capacitance will mitigate against capacitive current spike injections to low-voltage, ground-referenced control circuits from the high dV/dt slewing node in the power switching bridge. In summary, the fabricated micro-transformer characterization results match-

with the FEM simulation results (Table 2) and with the specified parameter values (Table 1).

Table 3 Summary of measured transformer parameters

Parameters	**TX1**	**TX5**
Si-oxide base thickness	1 µm	5 µm
Swtching frequency (f_{SW}) [MHz]	20	20
Magnetizing inductance (L_{11}) @ f_{SW} [nH]	41.2	38
Coupling coefficient (k_{12})	0.85	0.84
DC resistance (R_{DC}) [mΩ]	286	301
Quality factor @ f_{SW}	12.8	12.6
Parasitic capacitance (C_{12}) [pF]	13	3.5

5 Simulation results

The transformer model for TX5, using measured data from Table 3, was simulated in Cadence in a 130nm CMOS gate driver signal coupling circuit. Circuitry was used to create sub-10V.ns pulses on the rising and falling edges of a gate driver signal and these were used to drive the pulse transformer. Signal recovery circuitry on the secondary side of the transformer was used as input for gate driver circuitry. The simulation results, at 10MHz switching frequency, are shown in Figure 10. The transformer is magnetized with a very short pulse (1.5ns) at the rising edge of the PWM primary side signal and demagnetized with the same negative pulse generated on the falling edge to minimize volt-second applied to the transformer. The input stage of the secondary side driver is designed to prevent the secondary side reconstructed PWM signal from changing state due to the ringing between the transformer inductance and silicon parasitic capacitances after the short pulse is removed. The integrated transformer will have controlled values for the leakage inductance.

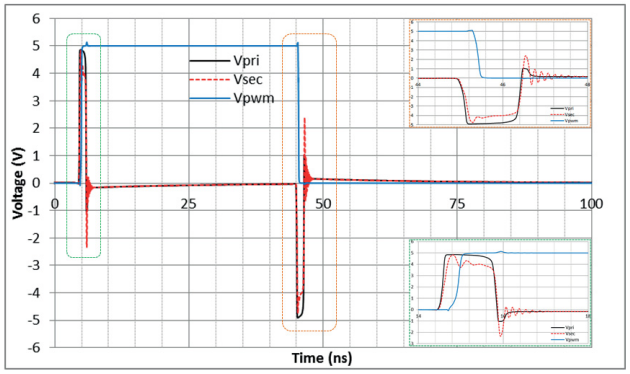

Figure 10 TX5 transformer primary (black) and secondary (red) side voltage waveforms @ 10MHz with PWM driving signal (blue) past the isolation barrier.

6 Conclusion

This work presents the design, fabrication, and characterization of a thin-film magnetics-on-silicon micro-transformer for low voltage operationally isolated signal and power conversion applications. Finite-element electromagnetic simulation tools were used to model the transformer electrical parameters, and to obtain parameter

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values to achieve a given set of design specifications. The target application of the micro-transformer is galvanic isolation for signal and power coupling in a custom CMOS gate driver IC. This requires high coupling coefficient, and low primary to secondary parasitic capacitance in order to reduce common mode capacitive current injections to the low-voltage controller circuits. The parasitic capacitance reduction is achieved by utilizing a thicker isolation oxide layer between the copper trace windings and the substrate silicon wafer. The micro-transformers were fabricated in a CMOS-compatible back-end-of-line (BEOL) fabrication process. The measured electrical parameters such as magnetizing inductance, coupling coefficient, resistance, quality factor and inter-winding parasitic capacitances exhibit good match with the modelled parameter values.

In the future, large signal behaviour and losses for power coupling applications will be analysed. Ultimately, the transformer is intended for assembly together with custom CMOS gate driver IC and GaN power switches to create highly coupled gate driver and power switch circuits, with minimal gate driver loop inductance and the prospect of using the galvanic isolation to locally couple gate driver power and control/telemetry signals.

Furthermore, the low-loss tf MoS platform can be extended to other converter applications such as integrated voltage regulators (iVR for SoC) or point-of-load (POL) DC-DC converters.

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