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LED flip-chip assembly with electroplated AuSn alloy

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InGaN based high brightness (HB)-LED chips have been fabricated and bonded to substrates that were coated with electroplated Au/Sn/Au solder. The assemblies yielded a forward voltage of 5.6 V and an optical output power of 42 mW when tested at 1,000 mA bias. The electroluminescence distribution was mapped with a CCD camera to determine the current spreading into the p-contact region. Computational fluid dynamics (CFD) was used to check the effect of non-uniform current spreading on the thermal resistance of the assemblies. We show that a good knowledge of the non-uniform heat generation is required to obtain accurate modelling results. The bond strength of the AuSn solder joints exceeded the norm, when shear tested according to MIL-STD-883E (method 2019.5).

1 Introduction The market for high brightness LEDs is growing rapidly, especially in mobile applications, signage and automotive applications [1]. One factor that affects the uptake of HB-LEDs is the cost per lumen. This cost can be lowered by increasing the photon flux per square centimeter of wafer material. This photon flux ϕ_{pa} (photons per second per square centimeter of wafer material) can be written as

$$\phi_{pa} = (J/q) \times IQE \times EE \qquad (1)$$

where J is the average current density through a square centimeter of wafer material, IQE the internal quantum efficiency, q the electron charge, and EE the light extraction efficiency. GaN-based laser diodes are capable of operating at current densities of 10 kA/cm^2 through the junction [2, 3]. However, such high current densities cannot be maintained on large area HB-LED chips due to several limitations. Firstly, the thermal resistance between the junction and ambient limits the amount of heat that can be dissipated at the junction before overheating occurs, resulting in a sharp drop in IQE. Secondly, the high defect density in standard LED wafer material limits the device lifetime at elevated current densities. Finally there are the considerations of dropping efficiency at high current density due to dropping IQE (the result of carrier overshoot) and an increased voltage drop across the p-contact, which in turn reduces the power conversion efficiency and further increases the thermal load. All these limitations will have to be addressed to make significant progress towards low-cost HB-LEDs. At our institute these issues are being addressed through a novel approach for defect density reduction in the wafer material [4], improved p-contact metallisations and reduction of the thermal resistance through flip-chip mounting. This last item is the subject of this paper. Wierer et al. [5] have shown that flip-chip mounting can significantly reduce the thermal resistance between the junction and ambient for sapphire based devices. Flip-chip mounted commercial HB-LEDs now run at typically 33 A/cm^2 through the p-contact area [6]. We present initial results on large area flip-chip mounted HB-LEDs that employ electroplated Au/Sn/Au for

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the flip-chip assembly. This lead-free solder can be bonded without flux and has the potential of reliable operation [7, 8]. In our approach more than 65% of the chip surface is in direct contact with the solder. The first indications are that these devices are able to operate with a continuous current density of 165 A/cm^2 through the junction area.

2 Experimental

2.1 Device design and fabrication Figure 1a shows a plan view of the electrode layout. The p-contacts are elongated, cigar-shaped, and measure 1,000 µm x 200 µm. The p-contact metallisation consists of EB-evaporated Pd-Ag-Ni-Au (3-50-30-300 nm). This metallisation scheme yields ohmic contacts "as deposited" [9], with a specific contact resistivity of 3.5 x 10^{-3} Ω.cm^2 on p-type GaN with a hole concentration of 3.5 x 10^{17} cm^{-3}.

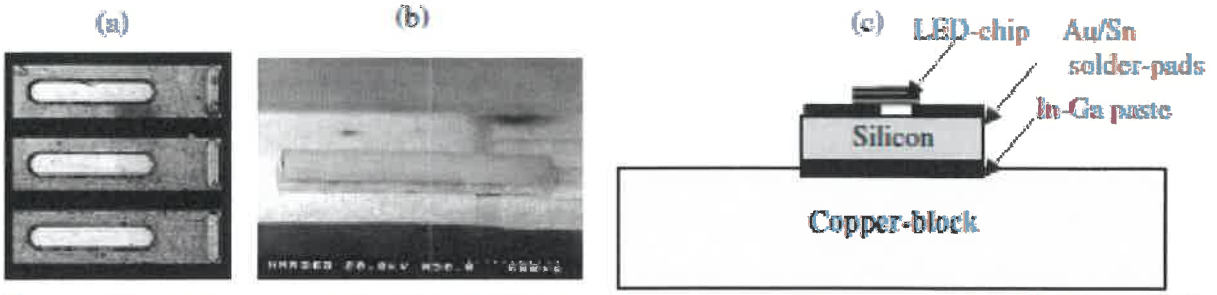


Fig. 1 a) Photograph of three LED-chips, showing the layout of the p-and n-contact pads, b) flip-chip assembly, showing an LED-chip, mounted across two solder pads, and c) schematic view of a flip-chip assembly (side view).

The n-contact metallisation consists of Ti-Al-Pt-Au (50-100-30-300 nm). The contacts are ohmic "as deposited", with a specific contact resistivity of 5 x 10^{-5} Ω.cm^2 when n= 4 x 10^{18} cm^{-3}. The n-contact fully surrounds the p-contact, with a 10 µm wide gap between the two contacts. A 200 nm thick SiN_x-layer, deposited by plasma enhanced CVD (PECVD), lies over the n-contact layer to provide electrical insulation to the p-solder pad. It has a 400 µm x 100 µm wide n-contact window as shown on the right hand side of Fig. 1a. The device wafer consisted of a sapphire substrate and a 2 µm thick LED structure (n-GaN, InGaN MQW, p-GaN). The EL emission peaked at 484 nm.

GaN was cleared from the scribing channels by inductively coupled plasma etching (ICP) and the wafer piece was thinned down to 100 µm thickness before scribing it into individual LED chips. The chip sizes tested were 1800 µm x 600 µm (single p-contact), and 1800 µm x 1200 µm (dual p-contact). Figure1b shows a flip-chip assembly with an LED chip bonded across the gap between two solder pads on the silicon substrate. This silicon wafer piece was in turn attached to a copper heat sink with a liquid indium-gallium mixture. This is shown schematically in Figure 1c. A sputtered Ti-Cu (20-200 nm) layer on the silicon wafer acted as the seed layer for the electroplating. The silicon wafer was patterned with photo resist, and the windows in the photo resist were plated up with Ni-Au-Sn-Au (1-6-6-1 µm). After plating both the photo resist and the exposed seed metal were removed. The nickel in this metallisation scheme served as a diffusion barrier.

2.2 Flip-chip bonding We performed flip-chip bonding trials at various temperatures. Table 1 gives an overview of the results. These trials were done with special test chips, measuring 325 µm x 375 µm x 110 µm thick, and having two 90 µm diameter bond pads. The gold layer on the bond pads was about 750 nm thick. The flip-chip bonding was done on a Fineplacer System from FINETECH Electronics, Berlin. Once contact had been made, two separate heaters were turned on to heat both the substrate and the chip. These heaters were turned off as soon as the set point had been reached. No flux was used. Table 1 shows that the chip bonded at 275 °C exhibited the highest bond strength. The shear testing was done on a commercial Royce 552 shear tester, according to the military standard MIL-STD-883E method 2019.5. This method is designed to test die attachment strength. In our case the required shear strength was 72-144 gram, the exact value depending on the failure mode. The device bonded at 275 °C exceeded

the highest required value, even though only 10% of the test chip area was occupied by the two 90 µm diameter bondpads.

Table 1 Overview of the measured shear force on small test chips with two 90 µm diameter bond pads.

Sample no.	Indicated bonding temperature (°C)	Shear force (g)
1	270	131
2	275	164
3	280	103
4	285	86
5	290	94
6	295	64
7	300	42

2.3 Electrical and optical testing The assemblies were placed inside an integrating sphere to measure their L-I and the I-V curves. These are shown in Fig. 2. The L-I curve was calibrated by fibre-injection of a known amount of light (of the same colour) into the sphere, alongside the assembly under test. The measurements were done without any encapsulation over the LED chip.

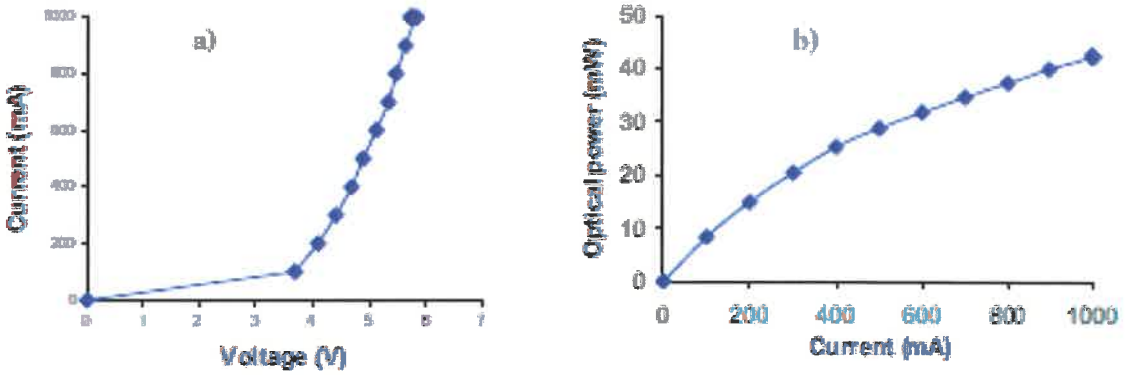


Fig. 2 a) I-V curve for a 1800 µm x 1200 µm LED chip, mounted on a copper heat sink. b) EL intensity as a function of bias current for the same copper assembly, as measured inside an integrating sphere.

At high current, I>500 mA, the series resistance of the total assembly is about 2 Ω. This means that the contribution of the p-contact resistance is less than 2 Ω under these bias conditions, so that the specific p-contact resistance ρ_c is less than 8×10^{-3} Ω.cm² on this LED chip with two p-contacts areas of 1000 µm x 200 µm each. The wall plug efficiency is 2.3% at 100 mA bias, and drops to 0.7% at 1A bias. This value could be improved with better wafer material, enhanced light extraction efficiency and encapsulation.

The EL-intensity distribution on a single 1800 µm x 600 µm chip was measured with a CCD-camera, through a microscope objective. The EL distribution at 500 mA bias is shown in Fig. 3a. The bottom part of the p-contact in this figure is the part that is closest to the n-contact. Figures 3b and 3c show the intensity distribution across the width of the contact, at two different bias currents, 500 mA and 100 mA respectively. The absolute light intensity is higher in Fig. 3b than in Fig. 3c.

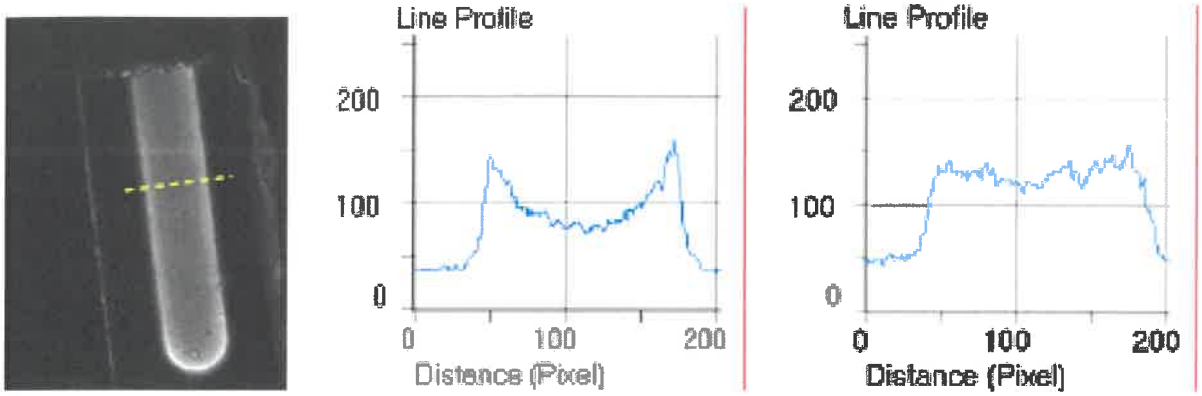


Fig. 3 a) EL-intensity distribution at 500 mA bias. The dotted line indicates the location of the intensity profiles. b) Intensity profile across the width of the p-contact at 500 mA bias. c) Intensity profile across the width of the p-contact at lower bias (100 mA). NB. Figures 3b and 3c show relative intensities. The absolute intensity in Fig. 3b is higher than in Fig. 3c.

2.4 Thermal modelling Thermal modelling was performed to calculate the thermal resistance between the junction and the heat sink for the configuration illustrated in Fig. 1c, and also to quantify the effect of a non-uniform current distribution as observed in Fig. 3b. Computational Fluid Dynamics (CFD) thermal analysis software was used. The programme took into account convection into the surrounding air (set at 35 °C), as well as thermal conduction towards the copper heat sink. In the simulations the bottom of the copper block was kept at a fixed temperature of 35 °C. The simulations were done in three dimensions. The heat dissipation inside the device was modelled as a heat source in the active region. Figure 4 shows the simulation results for a scenario where 2 Watt of heat was dissipated in a 20-µm wide rim along the edge of the p-GaN contact. The maximum junction temperature was 51.5 °C, and the thermal resistance between the junction and the bottom of the copper heat sink was therefore 8.3 °C/W. The maximum surface temperature on the LED top surface (sapphire) was 39.5 °C.

A different configuration, this time with uniform heat dissipation across the whole device junction area was also modelled. The total heat dissipation was again 2 W. In this case the calculated maximum junction temperature came out at 48 °C, and the corresponding thermal resistance between the junction and the heat sink was reduced to 6.3 °C/W. The results of these two chosen scenarios show that accurate thermal simulations for LED-assemblies need to take the non-uniform heat dissipation into account.

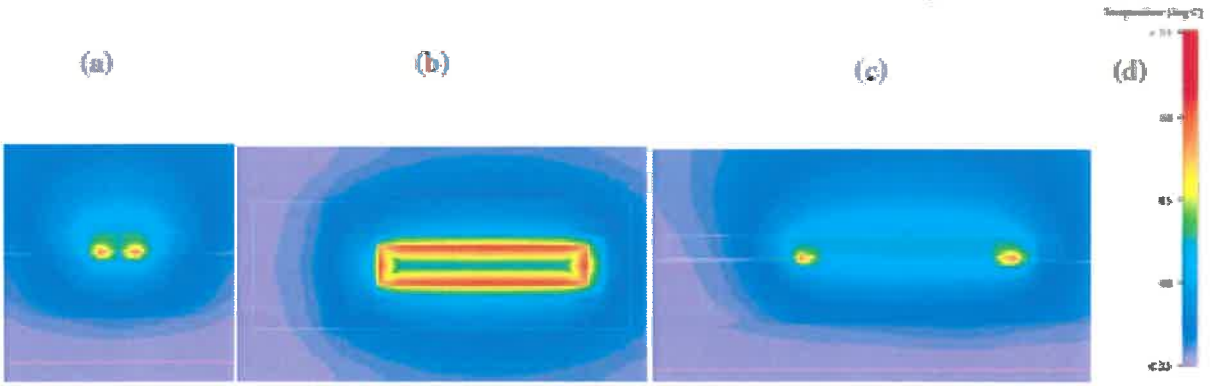


Fig. 4 a) Thermal simulation results for a heat dissipation that is concentrated along the p-contact perimeter (side view). The white rectangle shows the outline of the LED chip, b) top view, c) side view, and d) temperature scale (colour coding).

3 Conclusions InGaN based HB-LED chips have been fabricated and assembled to substrates coated with electroplated AuSn solder. At 1,000 mA forward current the assemblies showed a forward voltage

of 5.6 V and an optical output of 42 mW. Shear testing according to MIL-STD-883E (method 2019.5) was performed on small test chips, and the bonding temperature was optimised. The best result was obtained at 275 °C and the shear strength exceeded the MIL-STD-883E norm for die attachment, even though only 10% of the available die area on the test chips was covered with a bond pad metallisation. The EL intensity distribution was measured with a CCD camera, and computational modelling was employed to determine the effect of current spreading on the thermal resistance of the assemblies.

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