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Examining the relationship between capacitance-voltage hysteresis and accumulation frequency dispersion in InGaAs metal-oxide-semiconductor structures based on the response to post-metal annealing

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Abstract

In this work, we investigated the effect of forming gas annealing (FGA, 5% H_2 / 95% N_2, 250 °C to 450 °C) on border trap density in high-*k*/InGaAs metal-oxide-semiconductor (MOS) systems using accumulation frequency dispersion and capacitance-voltage (CV) hysteresis analysis. It is demonstrated that the optimum FGA temperature that reduces the accumulation frequency dispersion is 350 °C for HfO_2/*n*-InGaAs and 450 °C for Al_2O_3/*n*-InGaAs MOS system. Volume density of border traps (N_{bt}) is estimated using the accumulation frequency dispersion based on a distributed model for border traps. It is shown that for HfO_2/*n*-InGaAs MOS system, N_{bt} is reduced from 9.4×10^{19} $cm^{-3}eV^{-1}$ before FGA to 6.3×10^{19} $cm^{-3}eV^{-1}$ following FGA at 350 °C. For the case of Al_2O_3/*n*-InGaAs MOS system, N_{bt} is reduced from 5.7×10^{19} $cm^{-3}eV^{-1}$ for no FGA to 3.4×10^{19} $cm^{-3}eV^{-1}$ for FGA at 450 °C. Furthermore, it is shown that the most pronounced reduction in border trap density estimated from CV hysteresis analysis is observed at the same optimum FGA temperature that reduces the accumulation frequency dispersion, indicating that these two techniques for border trap analysis are correlated.

Keywords – border traps; high-k; InGaAs; CV hysteresis; accumulation frequency dispersion; forming gas annealing

1. Introduction

One of the main challenges facing the development of metal-oxide-semiconductor field effect transistors (MOSFETs) and Tunnel FETs based on InGaAs channels is the understanding and passivation of border traps which are predominantly located near the high-*k*/InGaAs interface layer and can exchange charges with the semiconductor bands via a tunnelling process [1, 2]. Border traps have now been understood to result in accumulation frequency dispersion in InGaAs MOS structures, leading to a drop in measured total capacitance (C_{tot}) with frequency (ω) [3], and the impact of border traps is evident up to 1 GHz and beyond [4]. Border traps with relatively long time constants can also be manifest as capacitance-voltage (CV) hysteresis. In this work, we reported on the effect of forming gas annealing (FGA) on border trap density estimated from accumulation frequency dispersion and CV hysteresis in high-*k*/InGaAs MOS structures. Furthermore, we examined the correlation between accumulation frequency dispersion and CV hysteresis.

2. Experimental

The samples used in this work were *n*-doped and *p*-doped InP (100) substrates with 2 μm *n*-type (S at 4×10^{17} cm^{-3}) and *p*-type (Zn at 4×10^{17} cm^{-3}) $In_xGa_{1-x}As$ (x = 0.53) epitaxial layers, respectively, grown by metal organic vapour phase epitaxy (MOVPE). Prior to oxide deposition, all the samples were treated in the optimized 10% $(NH_4)_2S$ passivation and then transferred to the atomic layer deposition (ALD) chamber within a minimum time (~ 3 min) as described in [5]. Either Al_2O_3 or HfO_2 was deposited as the high-*k* oxide on the InGaAs surface. The Al_2O_3 has a nominal thickness of 8 nm and was deposited by ALD at 300 °C using $Al(CH_3)_3$ (TMA) and H_2O. The HfO_2 has a nominal thickness of 8 nm and was deposited by ALD at 250 °C using $Hf[N(CH_3)C_2H_5]_4$ (TEMAH) and H_2O. Ni(70 nm)/Au(90 nm) was used as the metal gate and was formed by electron beam evaporation and a lift-off process. Both the Au/Ni/Al_2O_3/InGaAs and Au/Ni/HfO_2/InGaAs MOS capacitors were treated by post-metal FGA (5% H_2 / 95% N_2) at a series of temperatures (250 °C, 300 °C, 350 °C, 400 °C and 450 °C) for 30 min, and one sample from each MOS structure was not treated by FGA as a control sample. Annealing after metal deposition is beneficial as the metal plays a role in dissociating H_2 into atomic H which is needed for the passivation of defects.

All the CV measurements were recorded at room temperature using an E4980 LCR meter. The CV hysteresis sweeps were measured starting from inversion and sweeping upwards to accumulation, and without a stress time, subsequently sweeping downwards to inversion. In addition, all CV hysteresis sweeps were recorded at 1 MHz in order to minimize the interface state responses. The surface charge trapping density is quantified using the equation

$$Q_{trapped} = (\Delta V \times C_{ox})/q \quad (1)$$

where $Q_{trapped}$ is the density of trapped charge in cm^{-2}, ΔV is the CV hysteresis in V, C_{ox} is the oxide capacitance in F/cm^2, and q is the elementary charge in C. Equation (1) assumes the trapped charge is located at the high-*k*/InGaAs interface.

3. Results and Discussion

The multi-frequency (20 Hz to 1 MHz) CV characteristics for Au/Ni/HfO_2(8nm)/*n*-InGaAs MOS structure (no FGA) and the corresponding CV hysteresis are illustrated in Fig. 1, demonstrating a large frequency dispersion of ~4.6%/decade estimated at the maximum voltage (V_{max}) in accumulation and a surface border trap density ($Q_{trapped}$) of 5.9×10^{12} cm^{-2} from the CV hysteresis.

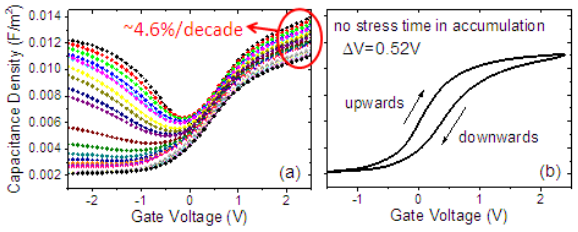

Fig. 1: (a) Multi-frequency (20 Hz to 1 MHz) CV characteristics, and the corresponding (b) CV hysteresis (1 MHz) for Au/Ni/HfO_2(8nm)/n-InGaAs MOS capacitor with no FGA. The frequency dispersion estimated in accumulation (at V_{max} = 2.5 V) in (a) is ~4.6%/decade and the CV hysteresis (ΔV) in (b) corresponds to a surface trapping density of 5.9×10^{12} cm^{-2}.

In order to reduce the density of border traps, which cause both accumulation frequency dispersion and CV hysteresis, FGA with a temperature series was performed. Accumulation frequency dispersion for HfO_2(8nm)/*n*-InGaAs MOS structures treated by FGA temperature series is shown in Fig. 2 (a), illustrating that the accumulation frequency dispersion goes through a valley with the increasing FGA temperature, and the optimum FGA temperature (T_{opt}) is observed to be 350 ºC. The increase in frequency dispersion above 350 ºC could be due to diffusion of As and In into the oxide, which is known to occur at ≥ 350 ºC [6, 7] and can create more oxide defects. For Al_2O_3(8nm)/*n*-InGaAs MOS structure, the accumulation frequency dispersion decreases with increasing FGA temperature up to 450 ºC as shown in Fig. 2 (b). This suggests that Al_2O_3 can suppress elemental diffusion compared to HfO_2. For the case of *p*-InGaAs, increase in accumulation frequency dispersion is also observed in HfO_2(8nm)/*p*-InGaAs (Fig. 2 (c)) at higher FGA temperatures due to elemental diffusion, and for Al_2O_3(8nm)/*p*-InGaAs (Fig. 2 (d)), no clear trend is observed and the average frequency dispersion is ~5.2%/decade.

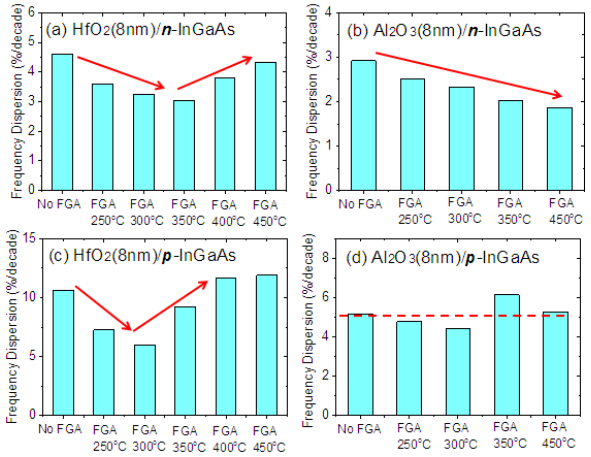

Fig. 2: Accumulation frequency dispersion for Au/Ni gate over (a) HfO_2(8nm)/n-InGaAs, (b) Al_2O_3(8nm)/n-InGaAs, (c) HfO_2(8nm)/p-InGaAs and (d) Al_2O_3(8nm)/p-InGaAs MOS capacitors treated by FGA temperature series. The Al_2O_3 samples treated by FGA 400 ºC exhibits non-regular behavior in terms of gate leakage and CV responses and are therefore omitted in the discussions.

Moreover, a significant accumulation frequency dispersion is observed in HfO_2/*p*-InGaAs and Al_2O_3/*p*-InGaAs when compared to their *n*-type InGaAs counterparts. This indicates that the Fermi level movement is strongly restricted in the InGaAs lower bandgap and is even being pinned (especially for HfO_2/InGaAs); therefore accumulation of holes is unlikely achieved. Hence, the discussion of border traps will be focused only on *n*-InGaAs.

Based on a distributed model for border traps using the measured total capacitance (C_{tot}) and measured total conductance (G_{tot}) in accumulation as a function of frequency (ω) [3], the volume density of border traps (N_{bt}) is estimated for HfO_2 and Al_2O_3 *n*-type samples treated with the optimum FGA temperatures compared to the no FGA samples as shown in Fig. 3 (G_{tot} versus ω not shown). The fitting was performed using equation (2) and the fitting parameters are listed in Table I. It is demonstrated that N_{bt} is reduced from 9.4×10^{19} $cm^{-3}eV^{-1}$ to 6.3×10^{19} $cm^{-3}eV^{-1}$ following FGA at 350 ºC for HfO_2 sample, and N_{bt} is reduced from 5.7×10^{19} $cm^{-3}eV^{-1}$ to 3.4×10^{19} $cm^{-3}eV^{-1}$ following FGA at 450 ºC for Al_2O_3 sample. Based on the model, border traps located ~ 1 nm to 2 nm into the oxide are probed under the frequency range investigated. The drop in capacitance below ω = 6283 rad/s (i.e. 1 kHz) for both HfO_2 and Al_2O_3 samples is possibly due to the effect of noise at low frequencies. Moreover, it is observed that for Al_2O_3 sample in Fig. 3 (b) above 300 kHz the experimental data deviates from the fitting and exhibits a higher slope of C_{tot} versus log(ω). This abrupt increase in the gradient of the capacitance versus log (ω) at higher frequencies is consistent with the measurement frequency range probing the border trap population located at < 1 nm from the oxide/InGaAs interface, where very large N_{bt} values (> 1×10^{21} $cm^{-3}eV^{-1}$) are reported [4]. It is noted that this high density of border traps located at < 1 nm from the oxide/InGaAs interface will also respond at all frequencies lower than 300 kHz. However, for frequencies of 300 kHz and below, there is no change in the response of these near interface border traps with reducing frequency, and consequently they are not manifest in the gradient C_{tot} versus log(ω) from which N_{bt} is determined. The abrupt change in gradient of C_{tot} versus log(ω) above 300 kHz in the Al_2O_3/InGaAs MOS is consistent with the sharp increase in N_{bt} towards oxide/InGaAs interface in the HfO_2/Al_2O_3/InGaAs gate stack reported in [4]. It is noted that this gradient change is not detected for the HfO_2/InGaAs MOS structure within the measurement window (20 Hz to 1 MHz), indicating that the increase in N_{bt} towards the oxide/InGaAs interface is not as large, or that the peak density is located outside the measurement window for the HfO_2/InGaAs samples studied.

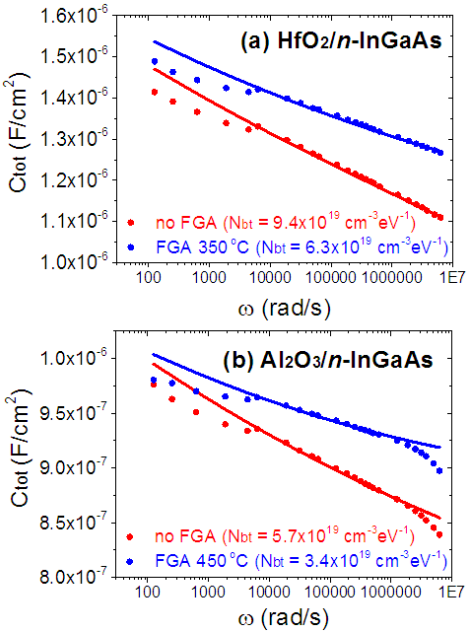

Fig. 3: Measured C_{tot} versus frequency (solid symbols) for Au/Ni gate over (a) HfO_2(8nm)/n-InGaAs and (b) Al_2O_3/(8nm)/n-InGaAs MOS. The fittings (solid lines) were performed based on the border trap model in [3].

Table I: Ref. [3] fitting parameters for Fig. 3 for HfO_2/*n*-InGaAs and Al_2O_3/*n*-InGaAs MOS systems

Sample /parameter	HfO_2 no FGA	HfO_2 FGA 350^{0}C	Al_2O_3 no FGA	Al_2O_3 FGA 450^{0}C
N_{bt}	9.4×10^{19}	6.3×10^{19}	5.7×10^{19}	3.4×10^{19}
t_{ox} (cm)	7.5×10^{-7}	7.5×10^{-7}	7.38×10^{-7}	7.38×10^{-7}
κ_{ox}	12	13.45	8.6	8.6
C_s (F/cm^2)	2.2×10^{-6}	4.2×10^{-6}	3.4×10^{-6}	6.5×10^{-6}
m*	0.22	0.22	0.23	0.23
E_{ox}-E (eV)	1.5	1.5	2.2	2.2
τ_0 (s)	2.9×10^{-10}	2.9×10^{-10}	2.8×10^{-10}	4.8×10^{-11}

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\kappa_{ox}\varepsilon_0} + \frac{q^2 N_{bt}\ln(1+j\omega\tau_0 e^{2(\sqrt{2m^*m_0(E_{ox}-E)}/\hbar)x})}{\tau_0 e^{2(\sqrt{2m^*m_0(E_{ox}-E)}/\hbar)x}} \quad (2)$$

where Y(x): the equivalent admittance at a point x looking into the semiconductor, ω: angular frequency, κ_{ox}: relative permittivity of the high-k oxide, ε_0: vacuum permittivity, q: elementary charge, border traps = $N_{bt}\times(1/q)$ cm^{-3}eV^{-1}, $m^*(m_0=9.11\times10^{-31}$ kg): effective mass of electron in the oxide, E_{ox} - E: energy level of border traps near E_C with respect to the energy of the top of the dielectric tunnelling barrier [8], τ_0: time constant associated with the tunnelling process. The boundary condition is Y (x = 0) = $j\omega C_s$, where C_s: InGaAs semiconductor capacitance. Equation (2) is solved from x = 0 to x = t_{ox}, where t_{ox}: oxide thickness. Equation (2) is reproduced from [3] equation (7).

The effect of FGA on CV hysteresis (ΔV) was also analyzed based on a study of ΔV (or $Q_{trapped}$) versus overdrive voltage (V_{ov}), where $V_{ov} = V_{max} - V_{fb}$ and V_{fb} is the nominal flatband capacitance. $Q_{trapped}$ versus V_{ov} is plotted in a log-log scale in Fig. 4 (a) for HfO_2(8nm)/*n*-InGaAs and Fig. 4 (b) for Al_2O_3(8nm)/*n*-InGaAs. The power law exponent is referred to as the voltage acceleration factor (γ-factor) [9, 10]. A higher γ-factor is required as this indicates a reduced trap density at operating voltage. The γ-factor and $Q_{trapped}$ (at V_{ov} = 2 V) are also presented for HfO_2 (Fig. 4 (c) and (e)) and for Al_2O_3 (Fig. 4 (d) and (f)). For the HfO_2/*n*-InGaAs MOS structure, an improvement in γ-factor is observed at intermediate FGA temperatures (T_{opt} = 350 ^{o}C), indicating that the width of the energy distribution of trapping defects is narrower, resulting in a lower trap density that the Fermi level can access near the conduction band edge. Therefore this results in a significant reduction in $Q_{trapped}$ as shown in Fig. 4 (e). For the case of Al_2O_3/*n*-InGaAs, γ-factor stays almost a constant following FGA at 250 ^{o}C and 300 ^{o}C, however, $Q_{trapped}$ is decreased. This suggests that the distribution of border traps remains unchanged but the density of total border traps is reduced. Following FGA at ≥ 350 ^{o}C, γ-factor is improved, resulting in a further reduction in $Q_{trapped}$ as shown in Fig. 4 (f). It is noted that the most pronounced improvement in γ-factor and reduction in $Q_{trapped}$ based on CV hysteresis measurements are observed at the same FGA temperature that reduces the accumulation frequency dispersion, where T_{opt} = 350 ^{o}C for HfO_2/*n*-InGaAs and T_{opt} = 450 ^{o}C for Al_2O_3/*n*-InGaAs. This observation implies that CV hysteresis and accumulation frequency dispersion are likely probing the same underlying oxide defects, even though the probing distance into oxide varies between the two analysis techniques.

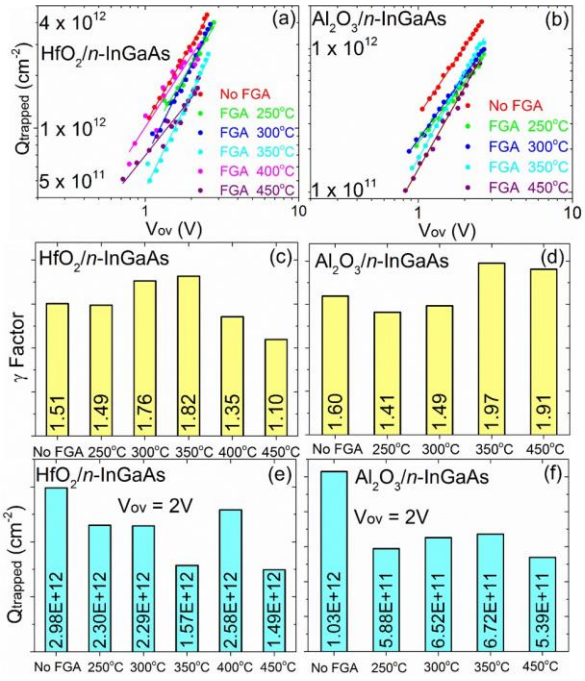

Fig. 4: $Q_{trapped}$ (from CV hysteresis) versus overdrive voltage (V_{ov}), voltage acceleration factor (γ-factor) versus FGA temperature and $Q_{trapped}$ (at V_{ov} =2 V) versus FGA temperature for Au/Ni gate over HfO_2(8nm)/n-InGaAs and Al_2O_3/(8nm)/n-InGaAs MOS. Note that the improvement in γ-factor results in significant reduction in $Q_{trapped}$.

The optimum $Q_{trapped}$ for HfO_2 sample (Fig. 4 (e)) and Al_2O_3 sample (Fig. 4 (f)) corresponds to a volume density of 1.57×10^{19} cm^{-3} and 5.39×10^{18} cm^{-3}, respectively, assuming the CV probes defects over a distance of 1 nm within the oxide with a spatially uniform trap density. These values are lower than those estimated from Fig. 3 using accumulation frequency dispersion (V_{ov} ~ 2 V). The discrepancy between accumulation frequency dispersion and CV hysteresis is due to the fact each technique is partially probing border traps, which can have a wide distribution in energy levels and also a spatial distribution into the oxide [11]. As illustrated in Fig. 5, accumulation frequency dispersion only probes border traps around a single energy level (with N_{bt} in unit of cm^{-3} per eV) at V_{max}. However, CV hysteresis arises from the filling the border trap energy levels below the Fermi level (E_f) at V_{max}, and at distances into the oxide, which do not re-emit the trapped charge during the reverse sweep of the CV response. The calculation of N_{bt} from the accumulation capacitance frequency dispersion at various values of V_{max} in accumulation yields the energy distribution of N_{bt}, which can be subsequently be integrated to obtain the N_{bt} value in units [cm^{-3}]. This analysis allows a more detailed correlation analysis to be undertaken, and is the subject of on-going studies.

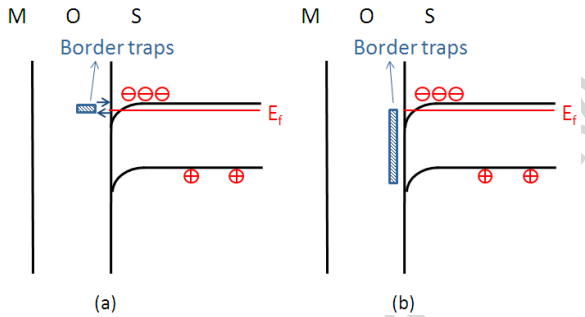

Fig. 5: Band diagram for n-InGaAs MOS capacitor showing (a) accumulation frequency dispersion which probes border traps at a single energy level at V_{max}, and (b) CV hysteresis measures border traps filled with electrons below E_f (at V_{max}).

5. Conclusion

The effect of FGA (5% H_2 / 95% N_2) on border trap density in high-*k*/InGaAs MOS systems was studied using accumulation frequency dispersion and CV hysteresis. The optimum FGA temperature to reduce accumulation frequency dispersion is observed to be 350 ^oC for HfO_2/*n*-InGaAs, where N_{bt} is reduced from 9.4×10^{19} $cm^{-3}eV^{-1}$ to $6.3\times10^{19}cm^{-3}$ eV^{-1}. For the case of Al_2O_3/*n*-InGaAs, continuous reduction in N_{bt} with FGA temperature is recorded, where N_{bt} is reduced from 5.7×10^{19} $cm^{-3}eV^{-1}$ for no FGA, to 3.4×10^{19} $cm^{-3}eV^{-1}$ for a 450 ^oC FGA. Moreover, the most pronounced reduction in border trap density estimated from CV hysteresis is observed at the same optimum FGA temperature that reduces the accumulation frequency dispersion, suggesting the two techniques, even though they probe different distances into the oxide, are correlated.

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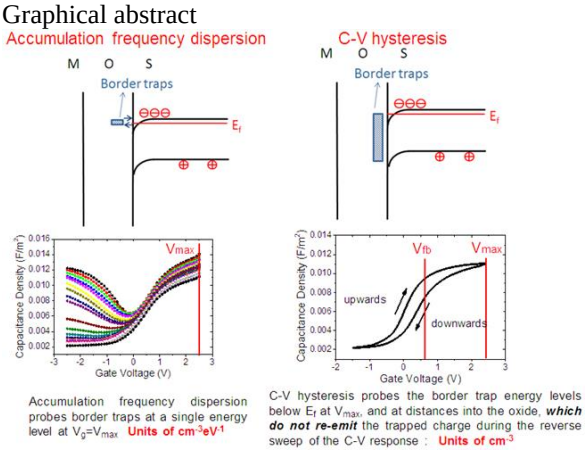
Graphical abstract



Highlights

- Border traps in HfO_2/InGaAs and Al_2O_3/InGaAs MOS structures were studied
- Forming gas annealing temperature series was performed
- C-V hysteresis and accumulation frequency dispersion were analysed and compared
- C-V hysteresis probes the border traps below the Fermi level
- Accumulation frequency dispersion probes border traps at a single energy level