CORA Cork Open Research Archive
Cartlann Taighde Oscailte Chorcaí

Title	Architecture and design of an RF receiver front-end and transmitter for wireless sensor networks, healthcare and smart energy systems
Authors	Shanan, Hyman
Publication date	2016
Original Citation	Shanan, H. 2016. Architecture and design of an RF receiver front-end and transmitter for wireless sensor networks, healthcare and smart energy systems. PhD Thesis, University College Cork.
Type of publication	Doctoral thesis
Rights	© 2016, Hyman Shanan. - http://creativecommons.org/licenses/by-nc-nd/3.0/
Download date	2026-11-06 12:41:00
Item downloaded from	https://hdl.handle.net/10468/6373

UCC
University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

ARCHITECTURE AND DESIGN OF AN RF RECEIVER FRONT-END AND TRANSMITTER FOR WIRELESS SENSOR NETWORKS, HEALTHCARE AND SMART ENERGY SYSTEMS

HYMAN SHANAN

A Dissertation Submitted to the

NATIONAL UNIVERSITY OF IRELAND, CORK

In Partial Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY

MICROELECTRONIC ENGINEERING

Committee

Prof. Michael Peter Kennedy, *IEEE Fellow, Supervisor*

Dr. Sven Mattisson, *Ericsson R&D and Lund University, Examiner*

Prof. Nabeel Riza, *IEEE Fellow, Head of School*



School of Electrical and Electronic Engineering

National University of Ireland, Cork

Copyright © Hyman Shanan, 2016

Architecture and Design of an RF Receiver Front-End and Transmitter for Wireless Sensor Networks, Healthcare and Smart Energy Systems

Hyman Shanan



All Rights Reserved. No Part of this Publication May Be Reproduced in Any Form by Print, Photoprint, Microfilm or Any Other Means Without Written Permission From the Author

Abstract

One of the quintessential challenges facing the planet is finding new energy resources to sustain our consumption in addition to preserving the trickle of energy resources we have left. Another significant challenge is reducing the costs of our ever increasing healthcare needs and providing electronic point-of-care health monitoring. Yet another challenge is making better use of farm lands to produce crops by means of utilizing better irrigation and plant monitoring systems. These challenges present invaluable opportunities for innovative solutions utilizing electronic circuits.

Wireless communication networks have in no small part affected our everyday lives. They revolutionized the way humans interact with each other and with the world around them. The pervasive use of wireless networks to access and relay information is evident in our use of mobile phones, wireless local area networks, wireless broadband services and global positioning systems to mention a few. The ubiquitous use of the available spectrum is turning the world we live into a connected wireless medium in which devices can intelligently connect to a suitable wireless network and provide or access information to or from the network. As a result, wireless communication networks are poised to play a greater role in solving some of our key future challenges. We are at the cusp of having the technology and the infrastructure to connect everything humans interact with using wireless networks. The internet of everything is almost a reality; it is our profession's next frontier. At the heart of this challenge is the need for ubiquitous wireless communications utilizing RF transceivers which consume the lowest possible energy.

A significant body of research has been carried out to implement RF integrated circuits which serve as workhorses for wireless communications. These RF integrated circuits have focused on various aspects such as the integration of the receiver and transmitter functions of a wireless communications system using silicon processes. These functions include low noise

amplification, mixing, low noise oscillators and frequency synthesizers, as well as high power amplification. More recently, there has been a significant focus on the design paradigms for energy consumption of these integrated circuits which is an area of research that offers its own set of challenges.

The thesis focuses on the architecture, design, implementation and evaluation of an RF transmitter and receiver front-end which are part of the foundations of a commercial RF system on a chip. The use of a number of digitally-assisted analog and RF techniques enables a fully integrated, low energy, low cost and high performance RF transmitter and receiver. In addition, a digitally assisted design simplifies the migration of the design from one process technology node to another with a smaller feature size. More specifically, the thesis addresses four key challenges in low energy RF transceivers:

1. The design of a low power zero-IF receiver for wireless sensor networks by overcoming the challenges posed by the need for a fast yet accurate offset cancellation loop. This is the key obstacle in the adoption of zero-IF receivers in wireless sensor networks. This work shows a novel digitally-assisted offset cancellation loop which enables the higher RF blocking performance of the zero-IF receiver architecture over the widely used low-IF architecture. This performance is achieved while minimizing the energy consumed by the zero-IF receiver.

2. The design of a low power and high performance RF mixer and associated LO circuit. The RF mixer sets the dynamic range of the receiver. Hence, challenging noise figure and linearity requirements are placed on the mixer with an equally challenging low power consumption budget. The LO circuitry of the RF mixer consumes the most power since the LO needs to drive a large load presented by the RF mixer's transistors. Research typically focuses on improving the RF mixer performance without considering the LO driver's power consumption. This is not the case with

low power transceivers used in wireless sensor networks. The thesis presents an LO driver circuit which substantially reduces its power consumption and makes the choice of a zero-IF receiver even more attractive than its counterparts. Furthermore, the zero-IF architecture of this work demonstrated an adjacent channel rejection which is about 20dB better than the best low-IF architecture in the prior art.

3. The architecture and design of a wide-bandwidth low power RF transmitter using a digitally-assisted pre-emphasis technique to extend the analog bandwidth of the frequency synthesizer by at least a factor of four. This enables RF modulation of FSK signals up to 2Mbps while reusing the frequency synthesizer circuitry and avoiding the area and power consumption which comes with traditional RF transmitters. The RF transmitter has 60% smaller die area, 50% less power consumption and its calibration system consumes 90% less energy when compared to the best prior art.

4. The architecture and design of a novel digitally-assisted calibration system to maintain the accuracy of the digital modulation at the output of the RF transmitter in the presence of process, temperature and supply variations. The use of a number of digitally assisted calibration techniques simplifies the hardware requirements for the calibration as well as its energy consumption.

Overall, the architecture selection and novel circuit design coupled with the use of novel digitally-assisted analog techniques, enabled a multi-standard RF transceiver which can operate in compliance with the IEEE 802.15.4 WPAN standard and also supports proprietary communication protocols with data rates between 50kbps and 2Mbps, while consuming a mere 31mW and 33mW in receive and transmit modes respectively.

Acknowledgements

A doctoral degree is an endeavor. The support and encouragement of colleagues, friends and family made the journey both enjoyable and rewarding. First and foremost, I would like to extend my thanks to Analog Devices for its support and for fostering a culture of innovation without which this work would not have come to light. In particular, I would like to thank Philip Quinlan for giving me the opportunity to innovate and develop the ideas presented in this work despite a tight product schedule. My sincere thanks to Prof. Peter Kennedy for his diligent review of the thesis, his encouragement, support and sponsorship of my doctoral degree.

The work presented here is part of the foundation of a commercial RF transceiver which was brought to life with the help of many people. I had the privilege of working with Guido Retz, my colleague at Analog Devices and my friend. The technical discussions and cooperation we had along the way made this transceiver a successful product for Analog Devices. I also acknowledge Guido's design of the LNA and the base-band filter section of the RF receiver. I would like to thank Cormac O'Shea, Kenneth Mulvaney and Finbarr O'Regan who worked on the digital implementation of the chip. My special thanks go to Tony O'Connell for his considerable help with some of the measurement results noted in this work. I worked with an exceptionally talented layout team during the development of this work including Leonel Bombio and Mary Carty. I also thank Dr. Jack Kenney of Analog Devices for his invaluable feedback on various sections of the thesis.

I am grateful for the time I spent at Analog Device's Cork design centre. The impromptu technical discussions with Colin Lyden were always intellectually stimulating. The hiking and soccer games with Christian Birk, John Healy and David Harty were precious recharging time.

My family has been a continuous source of encouragement over the course of this work. I sincerely thank my uncle for his insights into what it means to embark on the journey of a doctoral degree. I cannot find enough words to express my deepest thanks to my mother for being a source of inspiration, an example in hard work, dedication and persistence, and for encouraging me to change the world by doing this work. I will not be able to thank my beautiful sister enough for her unconditional love, kindness and support in this journey and for being my best friend. Finally and most importantly, I dedicate this work to the loving memory of my father who instilled the fighter spirit and the ethics required to be an innovator and a human being. I know you witness every success in my life.

To the Loving Memory of My Father,

To My Mother and Sister,

I Hope this Work Helps Make the World a Better Place

Statement of Originality

I hereby certify that all of the work described within this thesis is the original work of the author. Any published (or unpublished) ideas and/or techniques from the work of others are fully acknowledged in accordance with the standard referencing practices.

Hyman Shanan

August, 2016

List of Publications and Awards

Journal and Conference Papers

1. *"A 2.4GHz 2Mb/s versatile PLL-based transmitter using digital pre-emphasis and auto calibration in 0.18µm CMOS for WPAN",* **H. Shanan**, G. Retz, K. Mulvaney, P. Quinlan, IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2009, pp.420-421.
2. *"A highly integrated low-power 2.4GHz transceiver using a direct-conversion diversity receiver in 0.18µm CMOS for IEEE802.15.4 WPAN",* G. Retz, **H. Shanan**., K. Mulvaney, S. O'Mahony, M. Chanca, P. Crowley, C. Billon, K. Khan, P. Quinlan, IEEE International Solid-State Circuits Conference (ISSCC), Feb 2009, pp. 414-416
3. *"Radio transceivers for wireless personal area networks using IEEE802.15.4",* G. Retz and **H. Shanan**., K. Mulvaney, S. O'Mahony, M. Chanca, P. Crowley, C. Billon, K. Khan, J. Lopez, P. Quinlan, IEEE Communications Magazine, Vol. 47, Issue 9, 2009.
4. *"A Calibrated Wide-Bandwidth 2.4GHz ISM Band Transmitter",* **H. Shanan**, Analog Devices General Technical Conference, Apr. 2008.
5. *"A 23-mW Direct Conversion Receiver Front-end for the ADF7240 Low-Power 2.4 GHz RF",* G. Retz and **H. Shanan**, Analog Devices General Technical Conference, Apr. 2008.

Patents

1. *"Calibration system and method for phase-locked loops"*, **H. Shanan**, U.S. Patent No. 8,049,540, Nov 2011
2. *"Calibration for phase-locked loop",* **H. Shanan**, U.S. Patent No. 8,188,778, May 2012
3. *"Low-Power Frequency Dividers",* **H. Shanan**, U.S. Patent No. 8,294,493, Oct 2012

4. *"Low-Power Frequency Dividers",* **H. Shanan**, U.S. Patent No. 8,598,923, Dec 2012
5. *"DC-Offset-Correction System and Method for Communication Receivers",* **H. Shanan**, U.S. Patent No. 8,666,343, Mar 2014.

Awards

The author was recognized for part of this work by the *Analog Devices 2010 Product Line Innovation Award*.

Table of Contents

Abstract 5
Acknowledgements 9
Statement of Originality 12
List of Publications and Awards 13
List of Figures 18
List of Abbreviations 24
Chapter 1 27
Chapter 2 37
2.1 Problem Description and Introduction 37
2.2 Comparison between RF Modulator Architectures 38
2.2.1 Cartesian-Based RF Modulator 38
2.2.2 Frequency Synthesizer-Based RF Modulator 40
2.3 Wide Bandwidth RF Modulator Architecture 44
2.3.1 Two-Port RF Modulator 44
2.3.2 Digital Pre-Emphasis RF Modulator 46
2.4 Implementation of a Wide Bandwidth RF Modulator using Digital Pre-Emphasis 49
2.5 Conclusions 65
Chapter 3 67
3.1 Mathematical Analysis of the Calibration System 67
3.2 Implementation of the RF Modulator Calibration System 77
3.3 Mitigating the Calibration System Error Sources 87
3.3.1 Cancellation of Charge Pump Mismatch Errors 87
3.3.2 Calibration Capacitor Variation Detection and Calibration 96
3.4 Conclusions 102
Chapter 4 103
4.1 Simulation Results for the RF Modulator and its Calibration System 103
4.2 Measurement Results for the RF Modulator and its Calibration System 106
4.3 Comparison with the Prior Art 118
4.4 Conclusions 119
Chapter 5 121
5.1 Introduction 121
5.2 Linearity of RF Systems 122
5.2.1 Parameters Describing Non-Linear Systems 122
5.2.1.1 Gain Compression 123
5.2.1.2 Desensitisation and Blocking 124

5.2.1.3 Inter-Modulation Distortion 125
5.2.1.4 Linearity of Cascaded Systems 130
5.2.2 Noise in RF Systems 130
5.2.2.1 Definition of Noise Figure 130
5.2.2.2 RF System Sensitivity 131
5.2.2.3 Noise Figure of Cascaded Systems 132
5.3 RF Receiver Specifications 132
5.3.1 Thermal Noise Figure Specification 133
5.3.2 Linearity Specifications 135
5.3.3 LO Phase Noise Specification 142
5.4 RF Receiver Architecture 144
5.5 Concluding Remarks 149
Chapter 6 151
6.1 RF Receiver Architecture Details 151
6.1.1 Architecture Block Diagram 151
6.1.2 Architecture Analysis 154
6.2 RF Front-End Implementation 159
6.2.1 Transistor Behaviour in a 0.18μm CMOS Process 159
6.2.2 Introduction to RF Mixers 163
6.2.3 Active RF Mixers 166
6.2.4 Passive RF Mixers 171
6.2.4.1 Current-Commutating RF Passive Mixers 172
6.2.4.2 Noise in Current-Commutating RF Passive Mixers 177
6.2.4.3 Trade-offs in Current-Commutating RF Passive Mixers 185
6.2.4.4 Implementation of the RF Transconductor of the Current-Commutating RF Passive Mixer 188
6.2.4.5 Simulation Results of the Current-Commutating RF Passive Mixer 193
6.2.5 Passive Mixer Quadrature Signal Generation 195
6.3 Measurement Results of the RF Receiver 206
6.4 Comparison with Prior Art 216
6.5 Concluding Remarks 217
Chapter 7 219
7.1 Challenges of Offset Correction Systems in Zero-IF Receivers 219
7.2 RF Receiver's Offset Correction Architecture 221
7.2.1 Static DC Offset Cancellation Phase 222
7.2.2 Dynamic Offset Cancellation Phase 230
7.3 Measurement Results 245

7.4 Conclusions 248
Chapter 8 Conclusions 251
Bibliography 255

List of Figures

Figure 1-1 A smart electric grid application 28
Figure 1-2 Wireless sensor networks applications 29
Figure 1-3 Communication layers for a wireless sensor network 30
Figure 1-4 Block diagram of the RF transceiver. The areas highlighted in red are the focus of this work 31
Figure 2-1 Simplified Cartesian RF Modulator Architecture 39
Figure 2-2 Trade-offs in Frequency Synthesizer-Based RF Modulator 41
Figure 2-3 Two-Port RF Modulator using a Frequency Synthesizer 45
Figure 2-4 Conceptual block diagram of the frequency synthesizer-based RF modulator architecture using digital pre-emphasis for 2-FSK 47
Figure 2-5 Mathematical representation of the pre-emphasis process 50
Figure 2-6 2Mbps GFSK and MSK spectra using PN-9 data sequence generated by a Rhode and Schwartz SMA100A RF modulation source 51
Figure 2-7 Concept of a dual-path frequency synthesizer. (a) Conventional frequency synthesizer (b) Frequency synthesizer with an integrated loop filter 52
Figure 2-8 Block diagram of the full dual-path frequency synthesizer design 55
Figure 2-9 Details of the digital scaling block and ΣΔ modulator of Figure 2-8 when GF and DPEF are bypassed 56
Figure 2-10 Second-order filters for the LPF and integrator paths 57
Figure 2-11 Contributors to phase noise of the frequency synthesizer in transmit mode at 2.48GHz 61
Figure 2-12 Spectral emissions masks for the transmitter in various regulatory standards at 2.48GHz 63
Figure 2-13 Digital pre-emphasis filter implementation 64
Figure 3-1 Response of a closed loop system with an input step 69
Figure 3-2 Relationship between the double integral of the error signal *e(t)* and the normalized inverse of the open-loop gain and UGF for a second order system 74
Figure 3-3 Applying an input frequency step to the frequency synthesizer 78
Figure 3-4 Conceptual view of applying an input frequency step to the frequency synthesizer 79
Figure 3-5 Calibration system for the frequency synthesizer. 81
Figure 3-6 Relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* in the presence of *R, C,* K_{vco}, V_{bg} and $f_{channel}$ variation 83

Figure 3-7 Comparison between the relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* in the presence of simultaneous variations of *R, C,* K_{vco} and $f_{channel}$ and simultaneous variations of only K_{vco} and $f_{channel}$ 85
Figure 3-8 Relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* in the presence of I_{cp}, K_{vco} and $f_{channel}$ variation 86
Figure 3-9 Simplified circuit schematic of the integrator path and the calibration charge pumps. *OP1* is used once for all integrator path charge pump units and once for all calibration charge pump units. 89
Figure 3-10 Digital detection and cancellation system for the mismatch between the integrator-path and the calibration-path charge pumps 91
Figure 3-11 Digital integral of the mismatch value given by A_m in the presence of up-down current and delay mismatches between the integrator-path and calibration-path charge pumps while the frequency synthesizer is locked to $f_{channel} - \Delta f$ 93
Figure 3-12 Deviation of the double integral of the error signal *e(t)* in the presence of up-down current and delay mismatches between the integrator-path and calibration-path charge pumps after a frequency step of Δf has been applied to the frequency synthesizer 95
Figure 3-13 Error in the deviation of the double integral of the error signal *e(t)* in the presence of up-down current and delay mismatches between the integrator-path and calibration-path charge pumps after mismatch cancellation 96
Figure 3-14 System to calibrate C_{cal} due to process variations 97
Figure 3-15 Deviation of the ADC integrator from nominal value (ΔA_c) versus the percentage of adjustment required for the calibration capacitor. 99
Figure 3-16 Error in the value of the calibration capacitor C_{cal} when the fitting parameters of Figure 3-15 are used 101
Figure 4-1 Sequence of calibration system events for the frequency synthesizer. 104
Figure 4-2 Integrator path and LPF path charge pump DAC codes generated by the calibration system. 105
Figure 4-3 Un-calibrated vs. Calibrated RMS phase error performance of the transmitter for a 2Mbps GMSK signal. 106
Figure 4-4 Time capture of the ADC output while applying a frequency step to the PLL input in the presence of ±50% variation in the PLL bandwidth in steps of 10% 107
Figure 4-5 Linearity of the calibration signal and the effect of mismatch between the calibration and the integrating-path charge pumps on the accuracy of the calibration. 108
Figure 4-6 The calibrated performance of the RF transmitter's RMS phase error in the presence of ±50% variation in the PLL bandwidth at 3dBm for a 2Mb/s GMSK signal. 109
Figure 4-7 The calibrated performance of the RF transmitter's MER in the presence of ±50% variation in the PLL bandwidth at 3dBm for an IEEE802.15.4 signal 109

Figure 4-8 The calibrated performance of the RF transmitter's spectra in the presence of ±50% variation in the PLL bandwidth at 3dBm for an IEEE802.15.4 signal and a 2Mb/s GMSK signal 110
Figure 4-9 Measured un-calibrated and calibrated eye diagram for an IEEE802.15.4 modulated signal in the presence of a -50% deviation in the PLL nominal bandwidth..... 111
Figure 4-10 Minimum, Maximum and Mean C_{cal} calibration error versus variation in C_{cal} across 8 devices 113
Figure 4-11 Comparison between calibrated and un-calibrated IEEE802.15.4 *mean* transmitter MER versus channel frequency in the 2.4GHz band, ±40% variation in C_z and -35% to +20% variation in R_p across 8 devices 113
Figure 4-12 Comparison between calibrated and un-calibrated IEEE802.15.4 *minimum* transmitter MER versus channel frequency in the 2.4GHz band, ±40% variation in C_z and -35% to +20% variation in R_p across 8 devices 114
Figure 4-13 Comparison between calibrated and un-calibrated 2Mbps GMSK transmitter *mean* phase error versus channel frequency in the 2.4GHz band, ±40% variation in C_z and -35% to +20% variation in R_p across 8 devices 115
Figure 4-14 Comparison between calibrated and un-calibrated 2Mbps GMSK transmitter *maximum* phase error versus channel frequency in the 2.4GHz band, ±40% variation in C_z and -35% to +20% variation in R_p across 8 devices..... 115
Figure 4-15 Comparison between calibrated and un-calibrated IEEE802.15.4 transmitter MER versus channel frequency in the 2.4GHz band, ±40% variation in C_z and -35% to +20% variation as well as ±3% calibration error in C_{cal}..... 116
Figure 4-16 Measured eye diagram for 1Mbps GFSK modulated signal with PRBS9 (2^9 pseudo-random binary sequence) data sequence 117
Figure 4-17 Die photo of the RF modulator 118
Figure 5-1 Fundamental challenges with an RF receiver..... 122
Figure 5-2 Gain compression and A_{1dB} 124
Figure 5-3 Definitions of second- and third-order intercept points. 127
Figure 5-4 Input intercept point estimation (a) IIP3 and (b) IIP2 129
Figure 5-5 Required blocker rejection according to different standards..... 136
Figure 5-6 In-band IIP3 with CW adjacent and alternate channels 138
Figure 5-7 In-band IIP3 with modulated adjacent and alternate channels..... 139
Figure 5-8 Reciprocal mixing effect in RF receivers due to the LO phase noise 142
Figure 6-1 RF receiver block diagram 151
Figure 6-2 RF receiver noise figure contributions in dB from the receiver blocks 157
Figure 6-3 Voltage level diagram for the desired signal, a 5MHz blocker signal and a 13MHz blocker signal through the signal chain 158

Figure 6-4 Comparison between the theoretical and simulated I_D-V_{GS} characteristics for a 2.5µm × 0.18µm NMOS transistor in the saturation region 159
Figure 6-5 2.5µm × 0.18µm NMOS transistor parameters (g_m, I_D and g_m/I_D) versus V_{GS} for 8, 16 and 32 stripes (RF model and BB model depicted) 162
Figure 6-6 2.5µm × 0.18µm NMOS transistor parameters (f_t and I_D/W) versus V_{GS} for 8, 16 and 32 stripes using the RF transistor model 163
Figure 6-7 Principle of an RF mixing operation 163
Figure 6-8 Noise folding in the presence of a periodic signal 165
Figure 6-9 Double-balanced active RF mixer 168
Figure 6-10 Double-balanced passive mixer circuit used in this work (DC biasing details are not shown) 175
Figure 6-11 Modes of operation of a current-commutating RF passive mixer. (a) off-overlap mode and (b) on-overlap mode 180
Figure 6-12 Equivalent circuit for the RF passive mixer during an on-overlap period 183
Figure 6-14 RF transconductor implementation of the passive mixer 189
Figure 6-15 Dependency of the linearity of MOS devices on the gate-source voltage 192
Figure 6-16 IIP3 and IM3 versus RF input power at the RF mixer input 194
Figure 6-17 Input-Referred Noise PSD of the RF Mixer 194
Figure 6-18 A block diagram for a frequency divide-by-2 circuit. 195
Figure 6-19 A transistor-level schematic showing the implementation of the D-type latch used in the divide-by-2 circuit 196
Figure 6-21 Block diagram of LO distribution using multiple buffered paths for the VCO . 198
Figure 6-22 Block diagram for the LO distribution network in this work. 202
Figure 6-23 Simplified schematic for the bias control of the divider circuit. 204
Figure 6-24 Current and voltage waveforms for the CLK PMOS 205
Figure 6-25 Die photo of the RF transceiver 207
Figure 6-26 Evaluation board of the RF Transceiver 207
Figure 6-27 (a) Input-referred noise voltage density and (b) Noise figure of the RF receiver 208
Figure 6-28 Measured IEEE 802.15.4 PER sensitivity versus temperature and supply voltage for RF channels 2.405GHz, 2.45GHz and 2.475 GHz 210
Figure 6-29 Measured 2Mbps GFSK PER sensitivity versus temperature and supply voltage for channel 2.45GHz 211
Figure 6-30 Measured CW blocker level for 2Mbps GFSK desired packets at the sensitivity level + 3dB versus temperature for a narrow-band frequency offset from the RF carrier 212
Figure 6-31 Measured CW blocker level for 2Mbps GFSK desired packets at the sensitivity level + 3dB versus temperature for a wide-band frequency offset from the RF carrier 213

Figure 6-32 Measured CW blocker level for IEEE 802.15.4 desired packets at the sensitivity level + 3dB versus temperature for narrow-band frequency offset from the RF carrier 214
Figure 6-33 Measured CW blocker level for IEEE 802.15.4-2006 desired packets at the sensitivity level + 3dB versus temperature for a wide-band frequency offset from the RF carrier 214
Figure 7-1 Simplified block diagram of the OCL 223
Figure 7-2 Simplified block diagram of the OCL (only the I channel of the receiver is shown) 224
Figure 7-3 Effect of changing the digital feedback gain on the closed-loop transfer function of the OCL 227
Figure 7-4 Effect of adjusting the digital feedback gain to keep the high-pass corner of the OCL closed-loop transfer function constant with PGA gain changes 228
Figure 7-5 Simulation result of the static DC offset cancellation phase. 230
Figure 7-6 Block diagram of the dynamic time-varying offset cancellation loop 231
Figure 7-7 Simplified block diagram of the concept of an error-feedback ΣΔ modulator 232
Figure 7-8 Details of a third-order error-feedback ΣΔ DAC 234
Figure 7-9 Power spectral density of the input and output of the ΣΔ DAC 235
Figure 7-10 Simulation of the OCL during the dynamic offset cancellation phase 240
Figure 7-11 Simulation of the OCL during LNA gain changes after the AGC system is enabled in the dynamic offset cancellation phase. 241
Figure 7-12 Simulation of the OCL showing the wide bandwidth phase during and after LNA gain changes in the dynamic offset cancellation phase 243
Figure 7-14 Measurement result of the static DC offset cancellation phase at the PGA output 245
Figure 7-15 Measurement result of the receiver's noise performance during the dynamic offset cancellation phase using the ΣΔ DAC at the PGA output 246
Figure 7-16 Measurement result for the settling performance of the dynamic OCL during an LNA gain at the PGA output 247
Figure 7-17 Measurement result for the RSSI error of the received signal after an OCL and AGC acquisition 247

List of Tables

Table 2-1 Typical Parameters of a Cartesian RF Modulator 39
Table 2-2 Comparison between RF modulator architectures 49
Table 4-1 Measurements for the eye diagram of a 1Mbps GFSK modulated signal with PRBS9 data sequence showing compliance with Bluetooth v1.2 specifications 117
Table 4-2 Comparison of the RF transmitter performance with the prior art 119
Table 5-1 Phase noise specification according to different standards and modulation schemes 144
Table 5-2 Comparison between ZIFR and LIFR architectures 148
Table 6-1 Analysis of the RF specifications for the receiver signal chain blocks 155
Table 6-2 Trade-offs in RF passive mixer design 187
Table 6-3 Table summarizing the current consumption savings using the *bias current shaping technique.* 206
Table 6-4 Comparison of the RF receiver performance with the prior art 217

List of Abbreviations

ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AM	Amplitude Modulation
BB	Baseband
BT	BT product where, B: Bandwidth, T: Bit duration for a modulation scheme
BW	Bandwidth
CLBW	Closed-Loop Bandwidth
CP	Charge Pump
CW	Continuous Wave
DAC	Digital-to-Analog Converter
DPEF	Digital Pre-Emphasis Filter
DSSS	Direct Sequence Spread Spectrum
ETSI	European Telecommunications Standards Institute
EVM	Error Vector Magnitude
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
HPF	High Pass Filter
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IIP2	Second-Order Input Intercept Point
IIP3	Third-Order Input Intercept Point
IMD	Inter-Modulation Distortion
ISI	Inter-Symbol Interference
LIFR	Low-IF Receiver
LNA	Low Noise Amplifier

LO	Local Oscillator
LPF	Low-Pass Filter
LSB	Least Significant Bit
LUT	Look-Up Table
MA	Moving Average
Mbps	Mega-Bits per Second
MCU	Micro-Controller Unit
MDS	Minimum Detectable Signal
MER	Modulation Error Rate
MOS	Metal Oxide Semiconductor
MSK	Minimum Shift Keying
NF	Noise Figure
OCL	Offset Correction Loop
OOB	Out Of Band
OPBW	Occupied Power Bandwidth
OQPSK	Offset Quadrature Phase Shift Keying
P1dB	Input 1-dB Compression Point
PA	Power Amplifier
PDSU	Physical Layer Service Data Unit
PER	Packet Error Rate
PFD	Phase Frequency Detector
PGA	Programmable Gain Amplifier
PHY	Physical Layer
PM	Phase Modulation
PN	Pseudo Noise
PSS	Periodic Steady State
RF	Radio Frequency

RMS	Root-Mean Square
RX	Receiver
SNR	Signal-to-Noise Ratio
SRD	Short Range Device
SSB	Single Side-Band
TRX	Transceiver
TSPC	True Single-Phase Clock
TX	Transmitter
UGF	Unity-Gain Frequency
VCO	Voltage-Controlled Oscillator
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
ZIFR	Zero-IF Receiver
ΣΔ	Sigma-Delta

Chapter 1

Introduction

The proliferation of wireless transceivers has changed the landscape of the future of our planet. While their most recognized use is in mobile phones, they have been making further inroads in areas that are not immediately visible to the masses. Of significance to our most pressing challenges are the areas of energy and healthcare. The concept of remote sensing and control applies to these areas and the term wireless sensor networks is generally used to describe a class of applications where wireless connectivity plays a vital role in overcoming the imminent challenges found in these applications.

One of the most recent uses of wireless transceivers is in the area of energy monitoring and control, which is often referred to as the smart grid. Figure 1-1 shows an electric smart grid application utilizing wireless transceivers.

The majority of houses get their electricity over the electric grid. Electric appliances in the house consume the electricity and the electricity supplier dispatches someone, usually with a wireless device, to read the electric meter by the end of the billing period. This paradigm is now changing as appliances in the house such as the air conditioner, the washing machine or the lighting system will have embedded wireless devices. The appliances will be able to register how much electricity they consume. Moreover, the meter will have a similar wireless device which can communicate with the appliances over a bi-directional RF wireless link. This wireless link could be a 2.4GHz link governed by the IEEE 802.15.4 standard or any other proprietary communication protocol.

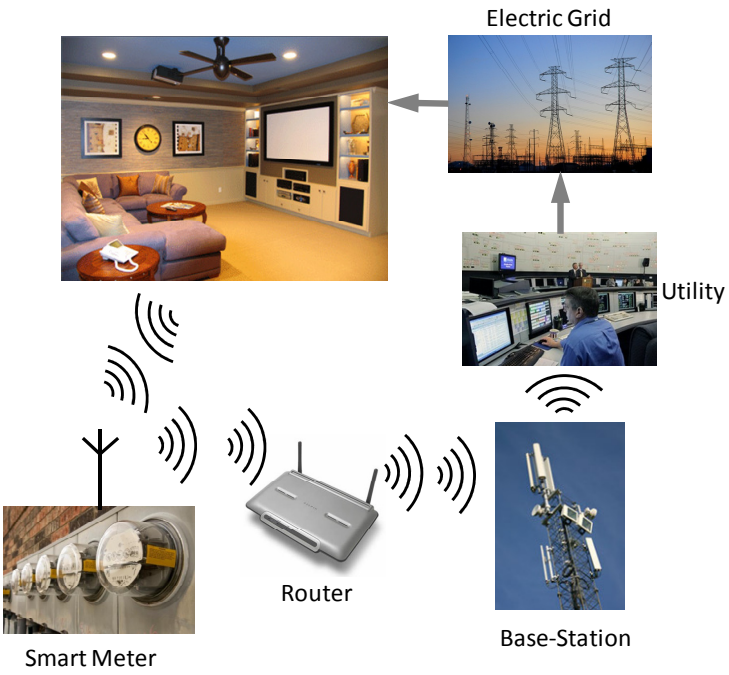


Figure 1-1 A smart electric grid application

The meter will collect data from appliances of many houses and send it to a router over a second wireless link. The router will relay this data to a base-station over a wireless gateway which in turn routes the data to the control centre of the utility company. The utility company can now control the electric grid according to the data being supplied by all the appliances consuming electricity from the grid. More interestingly, the utility company can potentially control the house itself by using the same bi-directional wireless link which the house used to transmit the data in the first place.

This system offers interesting possibilities for smart energy applications. For example, the utility company could lower the temperature of the air conditioner by a couple of degrees when peak load conditions occur in the grid, saving billions of dollars and reducing outages. It could also give the consumer a breakdown of the consumption of various appliances in the house and puts the consumer in control by offering a flexible billing system.

Figure 1-2 shows other areas where wireless sensor networks will become ubiquitous. For example, in the area of patient monitoring in hospitals, nursing homes or even in residential areas, where the number of hospital and physician visits can be minimized, reducing the burden on the healthcare system. Other areas include environmental monitoring and smart agriculture, where millions of wireless sensor networks can be deployed in the countryside to monitor every aspect of the environment such as water and air quality, soil temperature and humidity. These parameters can be used to provide accurate irrigation and harvest times. In short, wireless sensor networks are on the cusp of improving the quality of life for all of us on planet earth.



Figure 1-2 Wireless sensor networks applications

Figure 1-3 shows the communication layers of a typical wireless sensor network. The physical layer is the layer which interfaces to the actual physical medium. The media access control (MAC) layer controls the physical layer in terms of receive and transmit operations. For example, the MAC layer determines when the physical layer should turn on or off to receive or transmit a signal. The data link layer is responsible for correcting the data being

received by the physical layer. It typically employs block and convolutional decoding structures for error detection and correction in the data being processed by the physical layer.

The upper communication layers are mainly responsible for traffic at the network level. These layers assign addresses to each physical layer and manage data routing tables. They also interface with the applications layer at the user end. The transceiver presented in this work implements both the physical and MAC layers.

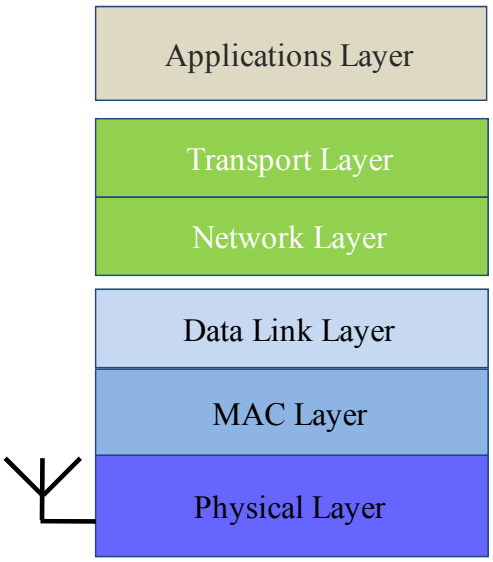


Figure 1-3 Communication layers for a wireless sensor network

Figure 1-4 shows the block diagram of the RF transceiver [1]. This work illustrates the architecture, design and measurement results of the RF transmitter, the RF receiver front-end and LO generation which are the most critical components of the RF transceiver in terms of power consumption and RF performance.

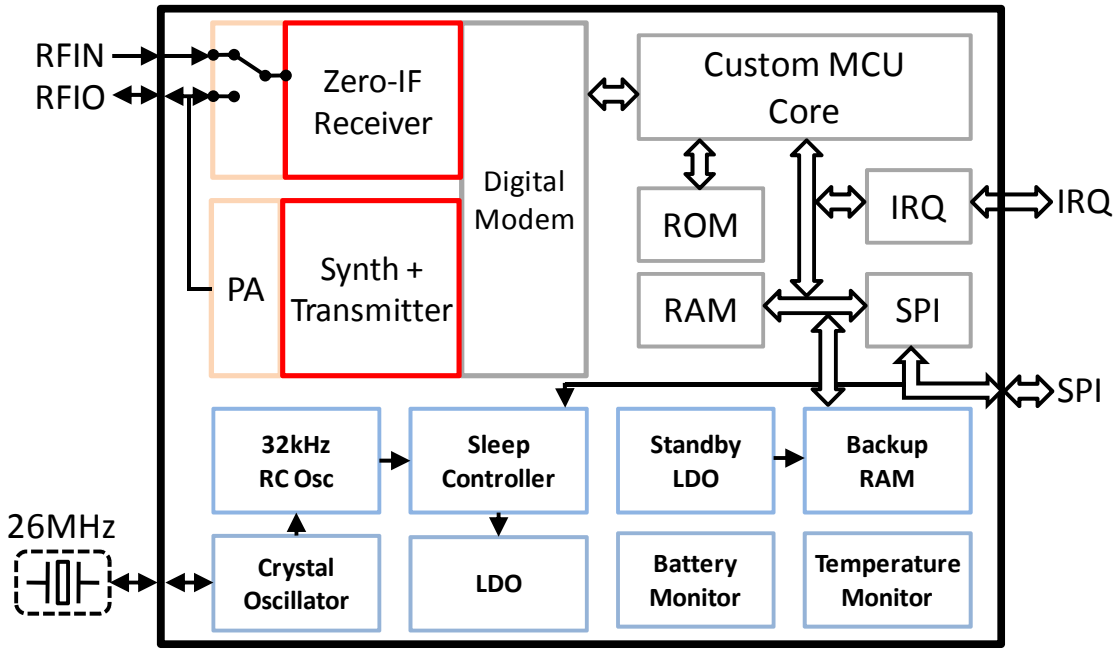


Figure 1-4 Block diagram of the RF transceiver. The areas highlighted in red are the focus of this work

Based on the illustrated applications, there is a need for a fully integrated, low energy, low cost and high performance RF transceiver system-on-chip. The high level of integration is required to allow users who are not familiar with wireless communications to install a wireless link rapidly and easily; the transceiver can become an immediate replacement for wired communications. The low energy aspect of the transceiver allows it to operate using AAA batteries for a period up to 15 years for a given communication protocol. Despite the need for a high level of integration, low energy and low cost, the transceiver should possess a relatively high RF performance, especially where it concerns RF blocking performance. This is required due to the need for the RF transceiver to operate in hostile and often times unregulated environments. For example, the 2.4GHz industrial, scientific and medical (ISM) band is unregulated and the transceiver has to coexist with a large number of wireless local area network (WLAN) transceivers.

Towards this end, the transceiver is implemented in a 0.18µm CMOS process which is a reasonably cost efficient process with a high gate density. The receiver uses a zero-IF

architecture which avoids any external components and saves significant power consumption in the baseband circuits compared to a low-IF receiver. The use of a zero-IF receiver comes with a set of design challenges, such as the implementation of the offset cancellation system and the presence of flicker noise at the RF mixer output. Those challenges are the subject of this work. The receiver has two RF inputs to support antenna diversity. One of the RF ports is bi-directional and is shared between the receiver and the transmitter to avoid using an RF switch. The use of antenna diversity significantly improves the reliability of the wireless link in the presence of interference or other environmental factors such as fading [1]. Owing to the use of a zero-IF architecture and a novel digitally-assisted offset cancellation loop, the receiver achieves a state of the art continuous wave RF blocking performance of -31dBm at ±5MHz offset and as high as -20dBm at frequency offsets of up to ±100MHz offset from a 2.45GHz RF carrier. This is achieved while receiving a 2Mbps GFSK signal and consuming 17mA from a 1.8V supply. The receiver is only 1dB short of meeting the stringent ETSI EN 300 440-1 class 1 CW blocking specifications which often requires substantially higher levels of power consumption. The receiver achieves a noise figure of 9.5dB, an RF sensitivity of -95dBm and a close-in IIP3 of -14dBm. Furthermore, the zero-IF architecture of this work demonstrated an adjacent channel rejection which is about 20dB better than the best low-IF architecture in the prior art.

The transmitter is based on a wide-bandwidth, low noise and low energy ΣΔ fractional-N frequency synthesizer with a fully integrated loop filter and direct digital frequency modulation using a second order IIR digital pre-emphasis filter. A novel digitally-assisted calibration scheme is used to prevent degradation in the transmitter's performance in the presence of process, temperature and supply voltage variations in the transceiver. The transmitter is versatile and can transmit continuous phase signals with data rates between 50kbps and 2Mbps and is compliant with the IEEE 802.15.4 standard as well as the Bluetooth v1.2 standard. It consumes 18mA from a 1.8V supply while transmitting +3dBm output power. It achieves an RMS phase error of 9.5° for GMSK signals and an RMS EVM of 2%

for IEEE802.15.4-compliant signals in the presence of ±50% variation in the frequency synthesizer bandwidth while meeting the FCC restricted band emissions in the 2.4GHz band. The RF transmitter has 60% smaller die area, 50% less power consumption and its calibration system consumes 90% less energy when compared to the best prior art.

A custom micro-controller unit (MCU) forms the heart of the digital section. A custom MCU was chosen since its command set can be optimized for the best compromise between complexity and program code density which translates into power consumption savings. The ROM holds the program code of the RF transceiver and the RAM stores data packets that have been received or are to be transmitted by the transceiver. The MCU interfaces to both the ROM and the RAM, controls the RF front-end, implements data packet handling functions, and provides low-level MAC functions [2].

The RF transceiver has an integrated 32kHz RC oscillator which is calibrated from the main 26MHz crystal oscillator. The RC oscillator clocks the sleep controller, which can be configured to wake the RF transceiver up periodically to search for an incoming RF signal. An ultra-low power standby LDO supplies the backup RAM which holds the configuration data of the RF transceiver while the transceiver is inactive in the sleep state. Integrated on the RF transceiver are additional support blocks such as a battery monitor and a temperature monitor. An interrupt request (IRQ) unit is available on the transceiver and interfaces to the host MCU. The transceiver can send interrupts to the MCU such as data received and data transmitted interrupts. A serial port interface (SPI) is also available to receive data and commands from the host MCU.

The architecture selection of the transceiver, novel circuit design and the use of digitally-assisted analog techniques enable a multi-purpose multi-standard RF transceiver which can operate in compliance with the IEEE 802.15.4 WPAN standard and also support proprietary

communication protocols with data rates between 50kbps and 2Mbps while consuming a mere 31mW and 33mW in receive and transmit modes respectively.

The thesis is organized as follows; Chapter 2 will discuss the RF transmitter's architecture and design choices. Chapter 3 will illustrate the need for a calibration system for the RF modulator and discusses the novel digitally-assisted calibration system adopted for this work. Chapter 4 will show simulation and measurement results for the RF transmitter. Chapter 5 discusses the RF receiver's specifications and architecture choices. Chapter 6 details the RF receiver's circuit design, with a focus on the RF mixer and low power frequency dividers. Chapter 7 shows the details of the RF receiver's offset cancellation system using digitally-assisted techniques to overcome key challenges associated with zero-IF receiver architectures. The major conclusions of the thesis are highlighted in Chapter 8.

The author was recognized for part of this work by the *Analog Devices 2010 Product Line Innovation Award*. In addition, the work presented in this thesis resulted in three major publications and five granted US patents. The list of publications and patents are as follows;

Publications

1. *"A 2.4GHz 2Mb/s versatile PLL-based transmitter using digital pre-emphasis and auto calibration in 0.18µm CMOS for WPAN",* **H. Shanan**, G. Retz, K. Mulvaney, P. Quinlan, IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2009, pp.420-421.
2. *"A highly integrated low-power 2.4GHz transceiver using a direct-conversion diversity receiver in 0.18µm CMOS for IEEE802.15.4 WPAN",* G. Retz and **H. Shanan**., K. Mulvaney, S. O'Mahony, M. Chanca, P. Crowley, C. Billon, K. Khan, P. Quinlan. IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2009, pp. 414-416.

3. *"Radio transceivers for wireless personal area networks using IEEE802.15.4",* G. Retz and **H. Shanan**., K. Mulvaney, S. O'Mahony, M. Chanca, P. Crowley, C. Billon, K. Khan, J. Lopez, P. Quinlan, IEEE Communications Magazine, Vol. 47, Issue 9, 2009.
4. *"A Calibrated Wide-Bandwidth 2.4GHz ISM Band Transmitter",* **H. Shanan**, Analog Devices General Technical Conference, Apr. 2008.
5. *"A 23-mW Direct Conversion Receiver Front-end for the ADF7240 Low-Power 2.4 GHz RF",* G. Retz and **H. Shanan**, Analog Devices General Technical Conference, Apr. 2008.

Patents

1. *"Calibration system and method for phase-locked loops"*, **H. Shanan**, U.S. Patent No. 8,049,540, Nov 2011
2. *"Calibration for phase-locked loop",* **H. Shanan**, U.S. Patent No. 8,188,778, May 2012
3. *"Low-Power Frequency Dividers",* **H. Shanan**, U.S. Patent No. 8,294,493, Oct 2012
4. *"DC-Offset-Correction System and Method for Communication Receivers",* **H. Shanan**, U.S. Patent No. 8,666,343, Mar 2014
5. *"Low-Power Frequency Dividers",* **H. Shanan**, U.S. Patent No. 8,598,923, Dec 2012

Chapter 2

RF Transmitter Architecture and Design

2.1 Problem Description and Introduction

As highlighted in Chapter 1, wireless communication transceivers used in wireless sensor networks, healthcare applications, point-to-point data links, data streaming applications and the energy smart grid operating in the 2.4GHz ISM band and regulated by the IEEE802.15.4, IEEE802.15.4g, SP100 and WirelessHART standards, require unprecedented levels of ultra-low power consumption and low selling price, which translates to the need for a small silicon area, and increasingly higher levels of integration of the DSP functions. These requirements are essential for large scale deployment of the transceivers which serve those applications.

In addition, wireless sensor networks using Direct Sequence Spread Spectrum (DSSS) modulation, as well as high quality audio and video streaming applications, require high transmission data rates in the range of 2Mbps to 4Mbps. These applications need a low modulation error rate (MER) or equivalently low error-vector magnitude (EVM) and high signal-to-noise ratio (SNR) at the transmitter output to preserve the modulation accuracy. Moreover, applications which are battery-operated often require transmissions in the form of short bursts, i.e, transmission at high data rates for a short period of time.

Hence, the design objective of this work is a versatile RF transmitter for as many wireless personal area network (WPAN) standards as possible, specifically the IEEE802.15.4 standard, the Bluetooth version 1.2 standard, as well as proprietary GFSK/GMSK systems at 2.4GHz. These supported standards operate with bit rates up to 2Mbps. In addition, these WPAN devices need to operate with the least amount of power; e.g. on AAA batteries for up to 10 years, and have very small area and little cost. The design described in this work is implemented on a 0.18μm CMOS process which is a good compromise between performance

and cost. In addition, the design is as digitally-assisted as possible. The transmitter also operates in the world-wide 2.4GHz band so it needs to comply with world-wide emission regulations.

There are a number of architectures which can satisfy the requirements of low power consumption and small implementation area while satisfying the requirements for low MER at the required high data rates. Those architectures can be grouped in two categories; frequency synthesizer-based modulators and Cartesian RF modulators. Traditionally, Cartesian RF modulators have been used to transmit high data rate signals. Despite being versatile, they suffer from being analog intensive. Analog circuit imperfections such as quadrature phase and gain mismatches, single side-band suppression, as well as direct LO feed-through considerably impair the modulation accuracy of the transmitter. Furthermore, they require, in addition to a frequency synthesizer, two channels of digital-to-analog converters, low-pass filters and RF mixers with inductive loads. These circuits have an insatiable appetite for silicon area and power consumption. By contrast, a frequency synthesizer-based modulator uses the existing frequency synthesizer found in any RF transceiver for transmission, hence providing an architecture which can achieve both low power consumption and occupy a small silicon area. In Section 2.2, we will highlight the differences between various architectures given the requirements for the RF transceiver under consideration in this work.

2.2 Comparison between RF Modulator Architectures

This section will present the key advantages and disadvantages of Cartesian and Synthesizer-based RF modulator architectures.

2.2.1 Cartesian-Based RF Modulator

Figure 2-1 shows a simplified Cartesian RF modulator architecture. The main advantage of this architecture is its versatility. While frequency synthesizer-based architectures only

support continuous phase modulation schemes, Cartesian RF modulators have the potential to support both amplitude modulation (AM) and phase modulation (PM) schemes. A Cartesian RF modulator comprises an in-phase channel and a quadrature channel. Each channel has a cascade of a digital-to-analog (DAC) converter, a low-pass filter (LPF), and an RF mixer driven by quadrature signals generated by the frequency synthesizer. The outputs of the in-phase and quadrature RF mixers are summed together and act as an input to a power amplifier (PA). The input to each DAC are the data symbols to be transmitted in the form of binary phase shift keying (BPSK), quadrature amplitude modulation (QAM) or frequency shift keying (FSK). The RF mixer up-converts the base-band data symbols to the RF carrier frequency ω_{lo}. The amplitude, $A(t)$, and phase, $\emptyset(t)$, of the RF signal are modulated according to the data symbols being transmitted on the in-phase and quadrature channels. Typical parameters for the cascade of blocks in the RF modulator system are shown in Table 2-1.

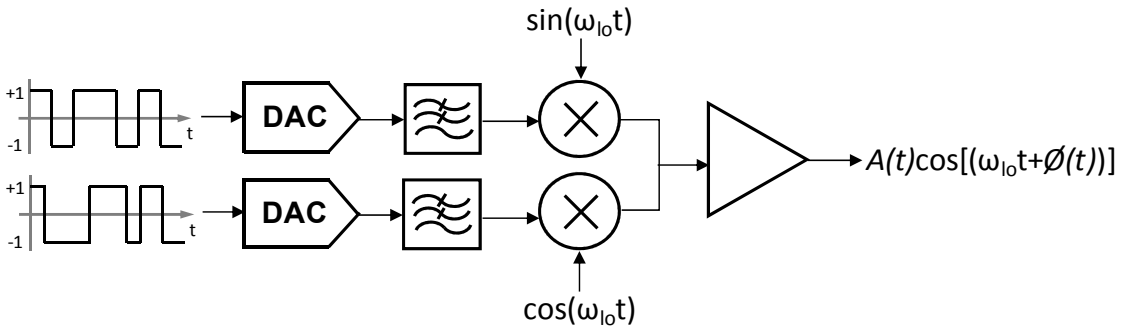


Figure 2-1 Simplified Cartesian RF Modulator Architecture

Parameter	Unit	DAC	LPF	Mixer	PA
Voltage Gain	dB	0	20	0	3
Cumulative Voltage Gain	dB	0	20	20	23
Output Noise Voltage	dBVrms	-92	-86	-60	-73
Cumulative Noise Voltage	dBVrms	-91.6	-71.4	-58.9	-55.8
SNR	**dB**	**64.5**	**64.3**	**51.8**	**51.7**

Table 2-1 Typical Parameters of a Cartesian RF Modulator

The parameters shown in Table 2-1 are for a typical Cartesian RF modulator. Based on simulation results of a 14-bit DAC, a LPF and an RF mixer similar to those used in the receive path, some estimates can be made for the voltage gain of each block and its output noise voltage. A total voltage gain of 23dB and cumulative noise voltage of -55.8dBVrms yields an SNR of about 52dB at the PA output for an input signal of -27dBVrms and an output power of approximately 4dBm. The achievable SNR of 52dB is sufficient for most modulation schemes in the application space this work addresses. However, the Cartesian RF modulator architecture suffers from several drawbacks; most notably its single-sideband (SSB) image rejection at the transmitter output. This is due to phase and gain mismatch in the base-band as well as the RF circuits. This effectively causes cross-talk between the I and Q data streams when modulated onto the RF carrier. Gain and phase mismatches in the I and Q paths cause a degradation in the modulation quality in terms of inter-symbol interference (ISI) and error vector magnitude (EVM) [3]. In addition, Cartesian RF modulators require additional circuitry besides a frequency synthesizer; a DAC, LPF, and an RF mixer that uses inductive loads which tend to occupy significant silicon area.

2.2.2 Frequency Synthesizer-Based RF Modulator

RF modulator architectures based on frequency synthesizers overcome the main drawbacks found in Cartesian RF modulator architectures by avoiding the need for an analog signal path with all its imperfections. These architectures also tend to have smaller silicon area and power consumption due to the fact that they use the existing frequency synthesizer to perform RF modulation as well as carrier generation. The need for high data rate transmission translates to the need for having a wide bandwidth for the frequency synthesizer. There are conflicting requirements between the need for a wide-bandwidth frequency synthesizer for high data-rate transmission to meet the MER and a narrow bandwidth and the RF spectral mask requirements of the modulated signal. This trade-off is illustrated in Figure 2-2 which shows a conventional ΣΔ fractional-N frequency synthesizer.

The frequency synthesizer shown in Figure 2-2 is a closed loop system comprised of a reference signal generated by a crystal oscillator feeding into a phase-frequency detector (PFD). The output of the PFD represents the phase error between the reference signal and the divided-down RF signal generated by the VCO. The charge pump is enabled according to the outputs of the PFD and generates an amount of charge which is proportional to the phase error at its input. This charge is integrated onto an RC passive loop filter which can be either external or internal to the IC. The output of the loop filter controls the frequency of the VCO. The output of the VCO is divided down by a factor *N* and is fed back to the PFD. The resolution of this *N*-divider is greatly improved using a ΣΔ modulator.

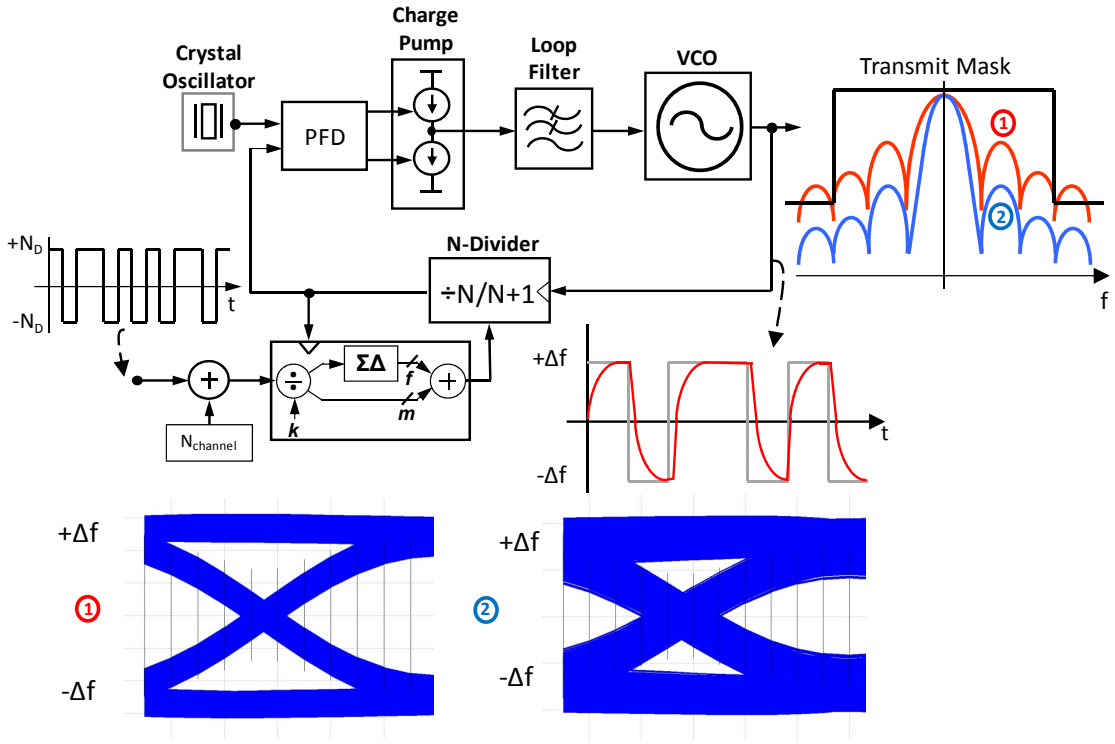


Figure 2-2 Trade-offs in Frequency Synthesizer-Based RF Modulator

A fractional RF channel frequency can be programmed with the aid of a ΣΔ modulator to tune the VCO to the correct fractional frequency. The channel frequency is programmed as a digital word represented by $N_{channel}$ in the figure. As an example, consider that the channel frequency resolution at the RF output of the frequency synthesizer is 10kHz and a channel frequency of 2.45GHz is required. $N_{channel}$ is programmed as a digital word of

2.45GHz/10kHz=245000. If the reference frequency of the synthesizer is 52MHz and the frequency resolution is 10kHz, the parameter k is set equal to 52MHz/10kHz=5200. The result of dividing 245000 by 5200 is 47.1153846. The modulus of the division acts as an input to the ΣΔ modulator whose output represents the high resolution input with f bits on average. The ΣΔ modulator's output is added to the integer part of the division which is 47 in this example. The output of this summation controls the N-divider of the frequency synthesizer to generate the correct frequency at its RF output on average. The N-divider is implemented as a pulse-swallow counter which consists of a prescalar with a width, N, that can either divider by N or $N+1$, a program counter with a width, B, a swallow counter with a width, A. The ratio between the output frequency of the frequency synthesizer to the reference frequency is given by $B \cdot N + A$. More details on the implementation of the pulse-swallow counter can be found in [3].

As a transmitter, data is added to the channel frequency represented by $N_{channel}$. The data to be transmitted is represented by digital words $\pm N_D$ in Figure 2-2 corresponding to bits '1' or '0'. For example, if a frequency deviation of ±300kHz is required at the output of the frequency synthesizer, N_D is set to 300kHz/10kHz=30. The frequency synthesizer produces the correct frequency deviations $\pm \Delta f$ around the RF channel frequency according to the input data.

The RF modulator architecture shown in Figure 2-2 uses only a fractional-N frequency synthesizer so no other RF components are required and hence, by construction, this architecture has only a small number of impairment sources. However, this architecture has an inherent trade-off between meeting the spectral mask requirement of a modulated signal and its MER. Figure 2-2 illustrates this trade-off, for example at 2Mbps. An eye diagram is a useful visual aid to assess the quality of the RF modulation. It is an overlay of all frequency transitions due to the 2Mbps input data at the RF output. For the lowest MER, the jitter around the zero crossings of the eye as well as around its maxima and minima at $\pm \Delta f$ has to be minimized. In the absence of quantization noise from the frequency synthesizer's ΣΔ

modulator and if the frequency synthesizer bandwidth is too wide, for example 2MHz, the modulated signal at the output of the frequency synthesizer will have excellent MER as indicated by the eye diagram labelled by (1) in Figure 2-2. However, the RF spectrum of the modulated signal could fail the spectral mask assigned for the frequency band of interest as shown by the spectrum labelled (1) in the figure. This is due to the absence of any attenuation for the side lobes of the modulated signal when using a wide bandwidth such as 2MHz. On the other hand, if the frequency synthesizer bandwidth is too low, the modulated spectrum at the frequency synthesizer output, labelled by (2) in Figure 2-2, will meet the spectral mask, since the side lobes are now attenuated. However, this occurs at the expense of a degraded MER due to inter-symbol interference (ISI), as shown in the eye diagram labelled by (2) in the same figure.

In the presence of the ΣΔ modulator's quantisation noise, the use of a frequency synthesizer bandwidth of 2MHz can produce excessive ΣΔ quantisation noise at the transmitter output around half of the sampling frequency of the ΣΔ modulator as well as within the bandwidth of the synthesizer due to PFD and charge pump non-linearities which mix the quantization noise down from around the sampling frequency of the ΣΔ modulator to lower in-band frequencies. The presence of such quantization noise can ultimately degrade the MER of modulated signals. Hence, there is an inherent limitation on the highest data-rate that can be supported by a frequency synthesizer design, given the required MER of the modulated signal as well as the spectral mask and emission requirements in the RF band of interest. In summary, selecting a wide bandwidth for the frequency synthesizer to support high data rates comes at the expense of degraded MER due to the presence of high levels of ΣΔ quantization noise and failure to meet a desired spectral mask. On the other hand, selecting a narrower bandwidth for the frequency synthesizer can help meet the spectral mask requirement. However, it also degrades the MER of the modulated signal due to ISI.

2.3 Wide Bandwidth RF Modulator Architecture

A number of architectures have been developed to decouple the requirement to transmit high data-rates using a frequency synthesizer from having a wide frequency synthesizer bandwidth. These architectures can be grouped in two categories; the first category provides a wide bandwidth path for the data yet a narrow bandwidth for the frequency synthesizer such that the ΣΔ modulator quantization noise and spurious components meet emission and regulation requirements. The second category provides techniques for cancellation of the ΣΔ modulator quantization noise thereby allowing the frequency synthesizer to have a wide bandwidth.

Quantization noise suppression techniques (also known as phase noise cancellation techniques) can provide superior phase noise and MER performance [4] [5]. However, due to using quantisation noise suppression DACs and intensive digital circuitry, they're relatively power hungry and consume a large area. On the other hand, architectures which use a wide bandwidth path for the data, yet a narrow bandwidth for the frequency synthesizer, require less complex and no additional low noise circuitry. Ferriss et al. shows an example of such an architecture in [6] using a digital PFD while Filiol et al. shows the use of a two-port modulation technique in [7] to extend the modulation bandwidth of a frequency synthesizer.

2.3.1 Two-Port RF Modulator

The concept of two-port modulation is depicted in Figure 2-3. Data to be transmitted is passed through two ports; the first port is a LPF path representing the frequency synthesizer transfer function and the second port is a HPF path representing direct VCO modulation. In Figure 2-3, $\emptyset_o(s)$ is the phase change at the output of the frequency synthesizer in response to phase changes $\emptyset_{lp}(s)$ and $\emptyset_{hp}(s)$ due to the data being transmitted through the LPF and the HPF paths of the frequency synthesizer respectively.

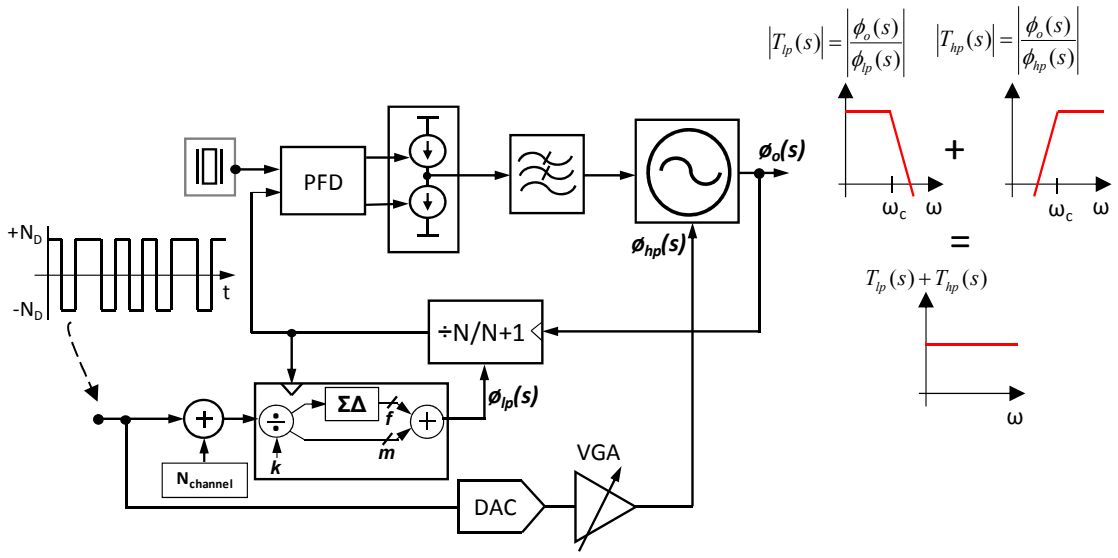


Figure 2-3 Two-Port RF Modulator using a Frequency Synthesizer

The transfer function representing the phase change at the output of the frequency synthesizer in response to the phase change in the LPF path can be modelled as:

$$T_{lp}(s) = \frac{G_{lp} \cdot \omega_c}{s + \omega_c} \tag{2.1}$$

where, G_{lp} is the frequency synthesizer's LPF path gain and ω_c is its cutoff frequency.

The transfer function representing the phase change at the output of the frequency synthesizer in response to the phase change in the HPF path is given by:

$$T_{hp}(s) = \frac{G_{hp} \cdot s}{s + \omega_c} \tag{2.2}$$

where, G_{hp} is the frequency synthesizer's HPF path gain and ω_c is its cutoff frequency.

The summation of both transfer functions $T_{lp}(s)$ and $T_{hp}(s)$ at the output of the frequency synthesizer is given by:

$$T_{hp}(s) + T_{lp}(s) = \frac{G_{hp} \cdot s + G_{lp} \cdot \omega_c}{s + \omega_c} \tag{2.3}$$

If the two transfer functions $T_{lp}(s)$ and $T_{hp}(s)$ are perfectly matched, i.e, G_{hp}=G_{lp}, the summation of the two transfer functions at the frequency synthesiser output is ideally a transfer function with an infinite bandwidth as given by (2.3) and shown in Figure 2-3.

Hence, the data being transmitted can ideally have an arbitrarily high rate. Practically, the bandwidth is limited by how well the two transfer functions are matched. The gain of the HPF path of the two-port modulation scheme can be adjusted using a variable gain amplifier (VGA) via a calibration algorithm. The calibration algorithm would attempt to match the gains of the HPF and LPF paths of the two-port modulation scheme.

The output of the second port feeds directly to the VCO, in most cases through a varactor. This port needs to have a very low noise because any noise on this port will translate directly to phase noise at the VCO output. This is one of the major drawbacks of this architecture especially when signals with high data-rates which require very low MER (or low EVM) need to be transmitted.

It is worth noting that all-digital frequency synthesizer architectures [8] can alleviate the requirement that the HPF and LPF paths have to be perfectly matched since the frequency synthesizer is fully implemented in the digital domain with the exception of the VCO. A fully digital frequency synthesizer has a superior phase noise and MER performance. However, it requires a high clock frequency to dither the VCO's digital varactor used for modulation to achieve the correct frequency deviation; this results in relatively higher power consumption.

2.3.2 Digital Pre-Emphasis RF Modulator

The transmitter architecture adopted for this work is shown in Figure 2-4 and is based on digital pre-emphasis of the input data to eliminate some of the major drawbacks of other architectures. Some of the early work describing the concept of digital pre-emphasis for RF transmitters using frequency synthesizers was reported in [9].

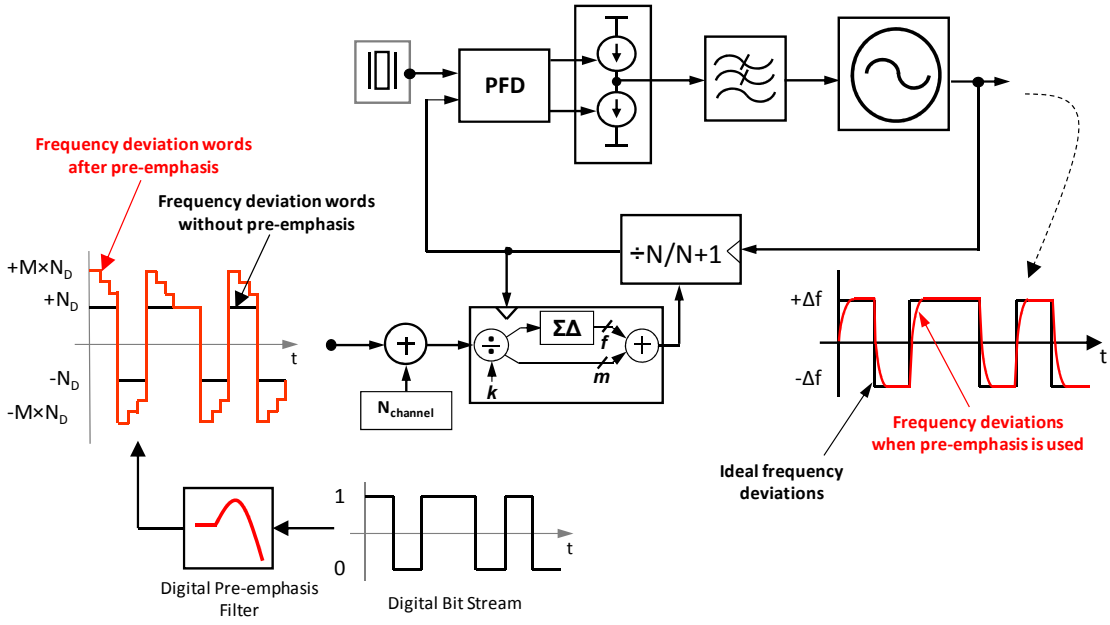


Figure 2-4 Conceptual block diagram of the frequency synthesizer-based RF modulator architecture using digital pre-emphasis for 2-FSK

The frequency synthesizer transmits data by changing the N-divider value in response to data bit '1' or '0'. For bit '1', the VCO frequency is shifted by a positive frequency deviation, $+\Delta f$, depending on the N-divider value and for bit '0', the VCO frequency is shifted by a negative frequency deviation, $-\Delta f$. The digital bit stream is represented by digital frequency deviation words $\pm N_D$ which are added to the digital word, $N_{channel}$, representing the channel frequency. The digital pre-emphasis filter (DPEF) pre-emphasizes the high frequency content of the data to be transmitted. This is shown conceptually in Figure 2-4, where the high frequency transitions of the digital frequency deviations representing the data are pre-emphasized by a factor of M. The pre-emphasized digital frequency deviations act as an input to the frequency synthesizer's N-divider after being added to the channel frequency represented by $N_{channel}$. Due to the low-pass filtering nature of the frequency synthesizer, the pre-emphasized digital frequency deviations are attenuated to the level needed to produce the correct frequency deviations, $\pm\Delta f$, at the output of the frequency synthesizer.

The frequency response of the digital pre-emphasis filter ideally approximates the inverse of the low-pass frequency response of the frequency synthesizer. Hence, the cascaded bandwidth of the digital filter's transfer function and the frequency synthesizer's transfer function is seen by the modulated data being transmitted as an extended bandwidth. As a result, the frequency synthesizer bandwidth can be made relatively low; this filters the ΣΔ modulator quantization noise with a narrower bandwidth than that required for the modulated data with a high data rate. For the same cascaded bandwidth, if the frequency synthesizer bandwidth is too narrow, the digital pre-emphasis filter order needs to be high in order to correctly approximate the inverse of the frequency synthesizer's transfer function. If the frequency synthesizer's bandwidth is too wide, the digital filter order is lower at the expense of increased ΣΔ modulator quantization noise.

In addition to having a smaller area and lower power consumption, using a digital pre-emphasis filter has several advantages compared to two-port modulation architecture in terms of extending the closed-loop bandwidth of frequency-synthesizer based transmitters. The first advantage is being able to transmit any modulation scheme such as 2-FSK, 4-FSK and other higher order modulation schemes which are used for high data rate transmission. Thanks to its digital implementation, the digital pre-emphasis filter can easily be configured to support any continuous phase modulation scheme.

A two-port modulation scheme can be designed to support a higher order modulation scheme. However, due to its analog implementation, a higher resolution DAC is needed to tune the VCO. This makes the implementation far more complex than the full digital implementation of a digital pre-emphasis filter. Another advantage is that the digital pre-emphasis scheme does not introduce any noise in the frequency synthesizer as is the case with the two-port modulation scheme.

Table 2-2 compares various RF modulator architectures discussed thus far. It can be seen from the table that quantization noise cancellation and fully digital frequency synthesizer architectures offer the best phase noise and MER. However, they suffer from a large area and high power consumption.

Architecture	*Phase Noise*	*MER*	*Area*	*Power Consumption*
Digital pre-emphasis	*Medium*	*Low*	*Medium*	*Low*
Two-Port with analog second-port	*High*	*High*	*High*	*High*
Two-Port with digital second-port	*High*	*Medium*	*Low*	*Medium*
Quantization noise cancellation	*Low*	*Low*	*High*	*High*
All-digital frequency synthesizer	*Low*	*Low*	*Medium*	*High*
Cartesian RF modulator	*Medium*	*Medium*	*High*	*High*

Table 2-2 Comparison between RF modulator architectures

Two-port modulation, especially using a digital second-port, on the other hand, offers moderate MER as well as moderate power consumption and low area. Digital pre-emphasis provides superior MER, low power consumption and small area. However, it has higher phase noise than the quantization noise cancellation and fully digital architectures due to the fact that it does not change the architecture of the basic frequency synthesizer and hence does not improve its inherent ΣΔ modulator quantization noise. Nevertheless, as will become evident in subsequent sections, its phase noise performance is more than adequate for the target applications of this transceiver.

2.4 Implementation of a Wide Bandwidth RF Modulator using Digital Pre-Emphasis

As shown previously in Figure 2-4 the digital pre-emphasis filter pre-emphasizes the high frequency components of the input digital bit stream, producing pre-emphasized frequency

deviation inputs, $\pm M \times N_D$, for the fractional-N frequency synthesizer. Due to the closed loop nature of the frequency synthesizer, the VCO will generate frequency deviations, $\pm \Delta f$, in response to the input frequency deviation values at the input data rate. In effect, the digital pre-emphasis filter extends the analog bandwidth of the frequency synthesizer seen by the input modulated data.

This effect is equivalent to a cascade of two transfer functions as shown in Figure 2-5. $H_{pe}(s)$ is the digital pre-emphasis transfer function, $H_{synth}(s)$ is the analog transfer function of the frequency synthesizer and $H_{eff}(s)$ is the pre-emphasized transfer function of the cascade. $H_{synth}(s)$ has a closed-loop bandwidth of f_c which is extended to f_{cpe} in $H_{eff}(s)$ as a result of the pre-emphasis provided by $H_{pe}(s)$ at f_{pe}.

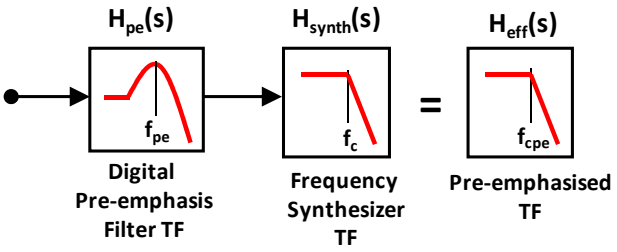


Figure 2-5 Mathematical representation of the pre-emphasis process

In order to design the digital pre-emphasis filter, we will need to develop the architecture of the frequency synthesizer and set the requirements for the filter according to the modulation schemes it intends to support. Figure 2-6 shows the measured spectra of 2Mbps GFSK and MSK with modulation indices of 0.32 and 0.5, respectively, using a 9-bit pseudo-random (PN9) data sequence generated by a Rhode and Schawrtz SMA 100A RF source versus the frequency offset from an RF carrier. The spectra shown in the figure are those which have to be supported by the transmitter to comply with the IEEE802.15.4 standard, as well as proprietary applications that require 2Mbps data-rates. The occupied power bandwidth (OPBW) is defined as the bandwidth containing 99% of the total integrated power of the transmitted spectrum, centered on the assigned channel frequency. The figure shows that the

OPBW for 2Mbps GFSK and MSK modulation schemes are 1.8MHz and 2.3MHz, respectively, which means that the frequency synthezier bandwidth has to be extended to a bandwidth close to these values in order to preserve the fidelity of a signal with a high MER.

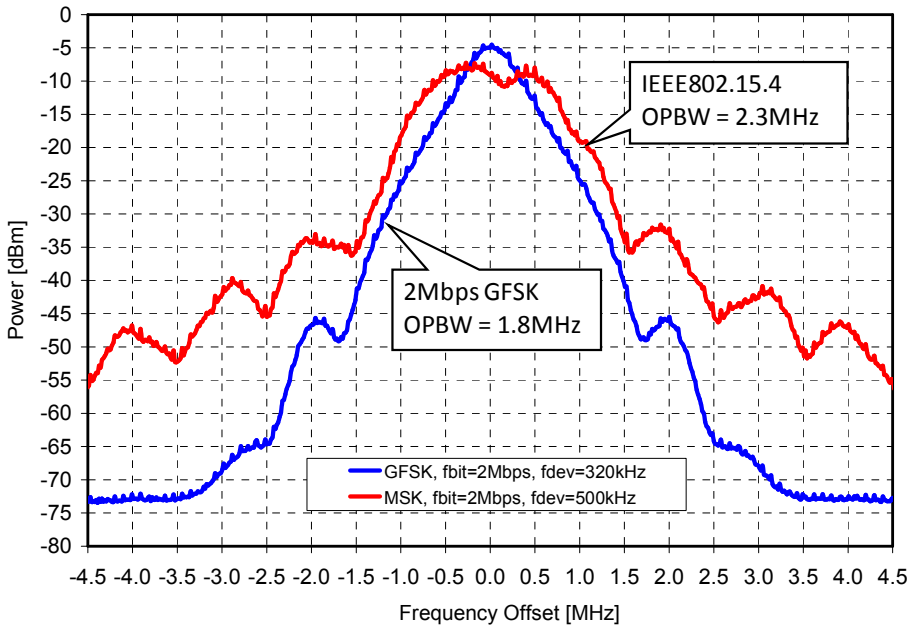


Figure 2-6 2Mbps GFSK and MSK spectra using PN-9 data sequence generated by a Rhode and Schwartz SMA100A RF modulation source

Since a low cost system is desired for wireless sensor nodes, all the components of the transmitter are integrated on the chip including the loop filter's passive components. In order to integrate the loop filter's passive components, a dual-path filter architecture is used [10] [11]. Figure 2-7 (a) shows a conventional frequency synthesizer loop filter implementation where the zero capacitor, C_z, is typically a large off-chip component. A large off-chip capacitor is needed to set the very low frequency, f_z, of the zero formed by C_z and R_z to about quarter of the cut-off frequency, f_c, in order to guarantee around 60˚ of phase margin for the design. The open-loop transfer function of a conventional frequency synthesizer is given by [12]:

$$H_{ol,conv}(s)=\left(\frac{I_{cp}K_{vco}}{2\pi\cdot N\cdot(C_P+C_z)\cdot s^2}\right)\frac{1+s\cdot R_zC_z}{1+s\cdot R_z\left(\frac{C_zC_p}{C_z+C_p}\right)} \tag{2.4}$$

where, I_{cp} is the charge pump current, K_{vco} is the VCO gain and N is the feedback divider ratio. The zero and pole frequencies of the open-loop transfer function of the conventional frequency synthesizer are given by:

$$\omega_{zero,conv}=\frac{1}{R_zC_z} \tag{2.5}$$

$$\omega_{pole,conv}=\frac{1}{R_z\left(\frac{C_zC_p}{C_z+C_p}\right)} \tag{2.6}$$

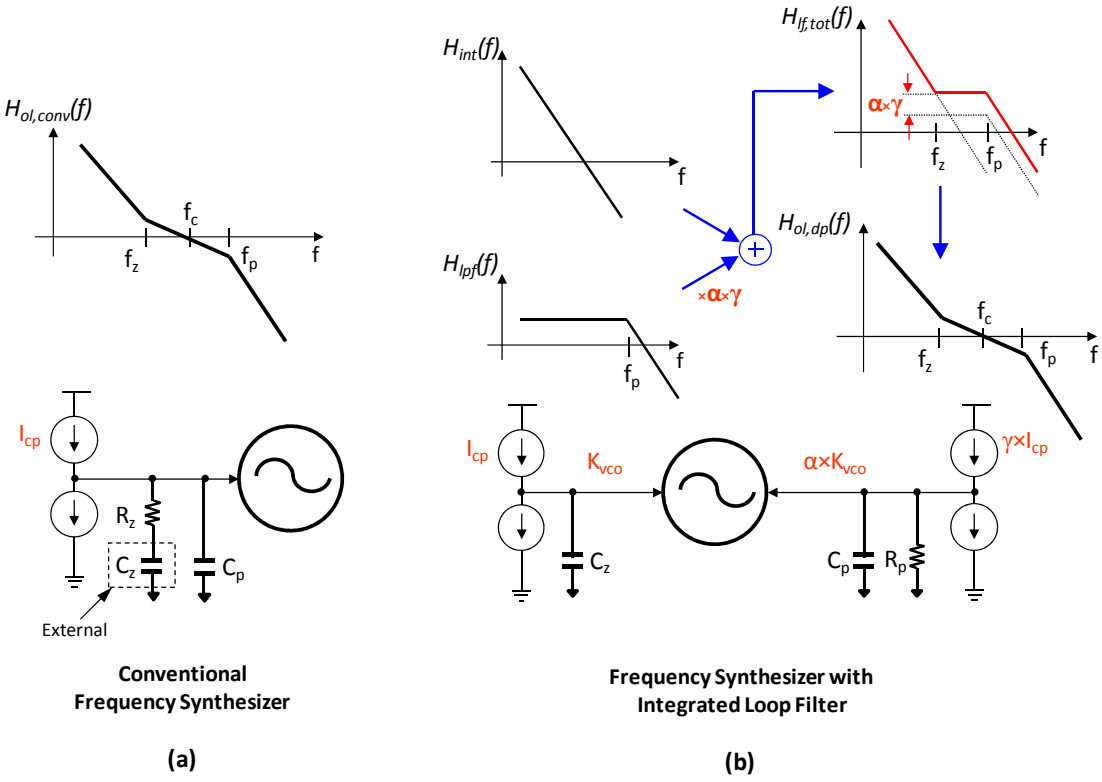


Figure 2-7 Concept of a dual-path frequency synthesizer. (a) Conventional frequency synthesizer (b) Frequency synthesizer with an integrated loop filter

A dual-path frequency synthesizer integrates the zero capacitor, C_z. This is accomplished as shown in Figure 2-7 (b) where two transfer functions are summed together; the first

represents an integrator transfer function, $H_{int}(f)$, and the second represents a LPF transfer function, $H_{lpf}(f)$, which is scaled by a factor, $\alpha \cdot \gamma$. The resulting transfer function, $H_{lf,tot}(f)$, represents the total loop filter transfer function with a zero at f_z, whose frequency can be controlled by the value of the scaling factor, $\alpha \cdot \gamma$, and a pole at f_p. Using this architecture, the value of the zero capacitor is effectively $\alpha \cdot \gamma \cdot C_z$.

The addition of the integrator path and the LPF path transfer functions can be performed in the charge and the capacitance domains. The integrator path is formed by the capacitor, C_z, and a charge pump whose current is I_{cp}. The LPF path is formed by the resistor R_p, capacitor C_p and the charge pump whose current is $\gamma \cdot I_{cp}$, where γ is a scaling factor. The summation is done directly at the VCO input using two varactors, one for each path. The integrator path has a varactor which provides a gain of K_{vco} MHz/V and the LPF path has a varactor which provides a gain of $\alpha \cdot K_{vco}$ MHz/V. The open-loop transfer function of the dual-path frequency synthesizer due to the summation of the integrator and the LPF paths is given by:

$$H_{ol,dp}(s) = \frac{I_{cp}}{2\pi} \frac{1}{s \cdot C_z} \frac{K_{vco}}{s} \frac{1}{N} + \frac{\gamma I_{cp}}{2\pi} \frac{R_p}{1 + s \cdot R_p C_p} \frac{\alpha K_{vco}}{s} \frac{1}{N} \tag{2.7}$$

which can be simplified as:

$$H_{ol,dp}(s) = \left[\frac{I_{cp} K_{vco}}{2\pi \cdot N \cdot C_z \cdot s^2} \right] \frac{1 + s \cdot R_p (C_p + \gamma \cdot \alpha \cdot C_z)}{1 + s \cdot R_p C_p} \tag{2.8}$$

The zero and pole frequencies of the open-loop transfer function of the dual-path frequency synthesizer are given by:

$$\omega_{zero,dp} = \frac{1}{R_p (C_p + \gamma \cdot \alpha \cdot C_z)} \tag{2.9}$$

$$\omega_{pole,dp} = \frac{1}{R_p C_p} \tag{2.10}$$

It can be observed from equations (2.5) and (2.9) that the effective zero capacitor in a dual-path frequency synthesizer is $\alpha \cdot \gamma \cdot C_z$. The multiplication factor $\alpha \cdot \gamma$ paves the way for integrating the zero capacitor on the IC by proper selection of the parameters α and γ.

The complete design of the dual-path frequency synthesizer for this work is shown in Figure 2-8 [13]. The frequency synthesizer has a fully integrated passive loop filter using an integrator path and a LPF path with capacitive summation at the VCO tuning ports based on the architecture shown in Figure 2-7 (b). The charge pumps (CPs) are designed as binary-weighted charge pump 6-bit DACs to allow for bandwidth programmability. The least-significant bit (LSB) sizes of the integrator and the LPF CPs are 0.5μA and 4μA respectively. The VCO operates at 4.8GHz followed by true single-phase clock (TSPC) frequency dividers with a 4/5 prescalar for low power consumption.

A third order multi-stage noise shaping (MASH) ΣΔ modulator is used for the fractional-N operation of the frequency synthesizer. The ΣΔ modulator has a modulus of 5200·32 which yields an intrinsic frequency deviation resolution of 52MHz/(5200·32)=312.5Hz at the RF transmitter output. The frequency deviation is programmable via $N_{deviation}$, which is conceptually shown in Figure 2-8. For example, a modulated 2Mbps FSK signal can have a frequency deviation of ±250kHz around an RF channel of 2.45GHz. The frequency deviation of this FSK-modulated signal can be programmed with a ±10kHz resolution via $N_{deviation}$. The data to be transmitted can optionally pass through a DPEF as well as a GFSK filter before being scaled by $N_{deviation}$. In addition, the user can program the RF channel frequency of the transmitter using $N_{channel}$ with a 10kHz resolution.

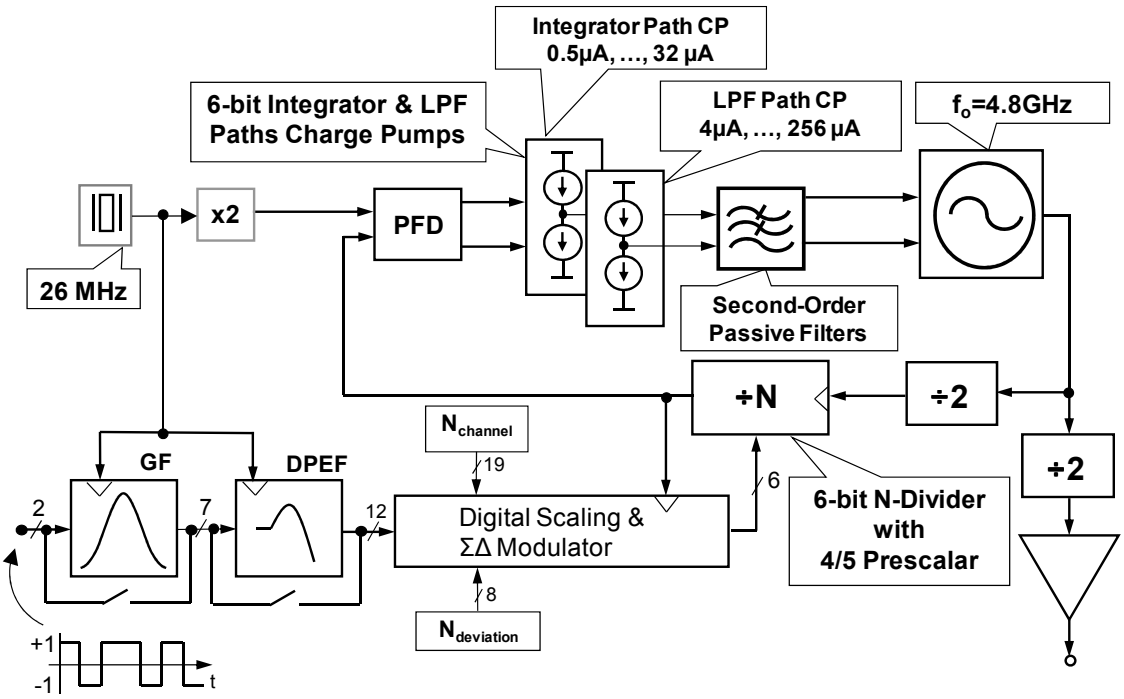


Figure 2-8 Block diagram of the full dual-path frequency synthesizer design

Figure 2-9 shows the details of the digital scaling block of Figure 2-8[1]. For simplicity, assume that both the Gaussian filter (GF) and the digital pre-emphasis filter (DPEF) are bypassed. An input FSK data stream represented by ±1 is first scaled by 32 to match the 7-bit output of the GF shown in Figure 2-8. It should be noted that scaling by 32 is not required if the GF is used. In addition, the input of the digital scaling and ΣΔ modulator block would be 12 bits instead of 7 bits if the DPEF is used as shown in the figure. The scaled FSK data is further scaled by a digital value, $N_{deviation}$, representing the RF frequency deviation around the RF carrier. A second digital value, $N_{channel}$, representing the channel frequency is scaled by 32 and added to the result of scaling the FSK data by $N_{deviation}$. The summation is then divided by a factor of 5200•32. A scaling of 32 for the data and the channel frequency gives an effective resolution of 10kHz for $N_{deviation}$ and $N_{channel}$ respectively when the result of the summation is divided by 5200·32. The modulus of the division by 5200·32 is 18 bits and acts as an input to a third-order MASH ΣΔ modulator. The output of the ΣΔ modulator represents the input by a 4-bit digital value between -7 and +7. On average, the ΣΔ modulator's 4-bit output represents

[1] This block was designed by Cormac O'Shea and Kenneth Mulvaney

its 18-bit input. The output of the ΣΔ modulator is added to the 6-bit integer part of the division. The result of the summation is 6 bits and act as an input to the N-divider of the frequency synthesizer as shown in Figure 2-9.

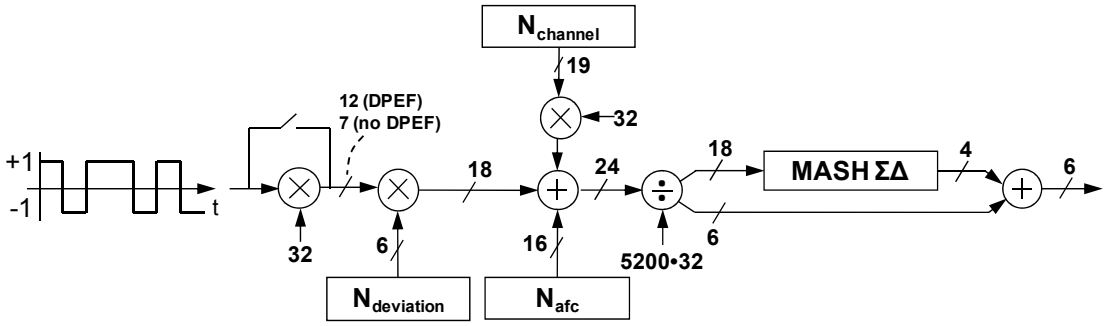


Figure 2-9 Details of the digital scaling block and ΣΔ modulator of Figure 2-8 when GF and DPEF are bypassed

As an example, consider that the required RF frequency deviation is ±500kHz around an RF channel frequency of 2.45GHz. The RF frequency deviation resolution as well as the RF channel frequency resolution is 10kHz. This yields $N_{channel}$=2.45GHz/10kHz and $N_{deviation}$=500kHz/10kHz. According to Figure 2-9, the RF frequency deviation for the input data stream of ±1 is given by:

$$f_{rfdev} = 52MHz \cdot \left[\frac{\left(\frac{2.45GHz}{10kHz} \cdot 32 \pm 1 \cdot \frac{500kHz}{10kHz} \cdot 32 \right)}{5200 \cdot 32} - \frac{2.45GHz}{52MHz} \right] = \pm 500kHz \qquad \textbf{(2.11)}$$

The architecture shown in Figure 2-8 avoids the use of quantization noise suppression techniques by using a digital pre-emphasis filter (DPEF) for the input data. High data-rate proprietary systems require a data rate of 2Mbps with a nominal RMS phase error of 10° for GMSK signals. Hence, the bandwidth of the cascade of the analog frequency synthesizer transfer function and the DPEF transfer function should be at least 2MHz. In order to reduce the power consumption of the DPEF, the bandwidth of the frequency synthesizer was chosen

to be as wide as 520 kHz which limits the required magnitude of digital pre-emphasis to 23.5dB while meeting the most stringent FCC spectral mask requirement in the restricted band at 2.4835MHz as will be shown in Figure 2-12. As a result, the DPEF can be implemented as a second order IIR filter with 16-bit coefficients. The wider the frequency synthesizer bandwidth, the lower the magnitude of the digital pre-emphasis required, the lower the order of the DPEF and ultimately the lower the power consumption which is a critical goal of the design. The design also features a digital Gaussian filter to generate GFSK or GMSK signals.

To further relax the design requirements to meet the FCC emission requirements, a frequency doubler is used to double the crystal oscillator frequency, hence reducing the effect of the in-band quantization noise of the digital ΣΔ modulator on the MER. The 52MHz clock is used to operate the frequency synthesizer, while the DPEF and the Gaussian filter operate at 26MHz.

The open-loop transfer function of the frequency synthesizer can be described by equations (2.12) to (2.30) where I_{cp} is the charge pump current for the integrator path, γ is the scaling factor for the charge pump current of the LPF path, K_{vco_integ} is the VCO gain for the integrator path, K_{vco_lpf} is the VCO gain for the LPF path, $Z_{integ}(s)$ is the impedance for the integrator path and $Z_{lpf}(s)$ is the impedance for the LPF path. The integrator and the LPF paths are constructed of second-order filters as shown in Figure 2-10.

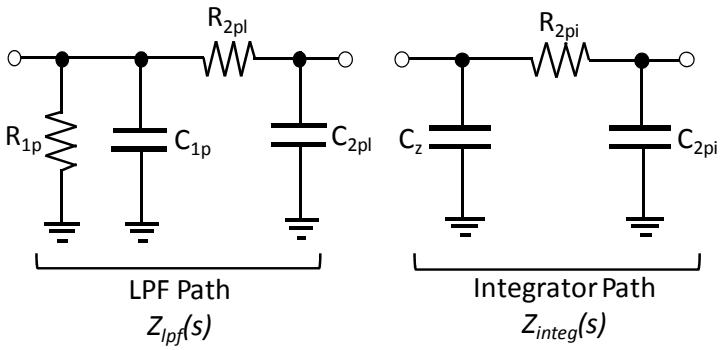


Figure 2-10 Second-order filters for the LPF and integrator paths

$$H_{ol}(s) = \left[\frac{I_{cp}}{2\pi} \cdot Z_{\text{int}eg}(s) \cdot \frac{K_{vco_\text{int}eg}}{s} + \gamma \cdot \frac{I_{cp}}{2\pi} \cdot Z_{lpf}(s) \cdot \frac{K_{vco_lpf}}{s} \right] \cdot \frac{1}{N} \quad \textbf{(2.12)}$$

where,

$$K_{vco_\text{int}eg} = K_{vco} \quad \textbf{(2.13)}$$

$$K_{vco_lpf} = \alpha \cdot K_{vco} \quad \textbf{(2.14)}$$

which yields,

$$H_{ol}(s) = \frac{I_{cp}}{2\pi} \cdot \left[Z_{\text{int}eg}(s) \cdot + \gamma \cdot \alpha \cdot Z_{lpf}(s) \right] \cdot \frac{K_{vco}}{s} \cdot \frac{1}{N} \quad \textbf{(2.15)}$$

where, assuming $R_{2p} = R_{2pi} = R_{2pl}$ and $C_{2p} = C_{2pi} = C_{2pl}$,

$$Z_{\text{int}eg}(s) = \frac{1}{s} \cdot \frac{1}{s \cdot R_{2p} C_{2p} C_z + (C_{2p} + C_z)} \quad \textbf{(2.16)}$$

$$Z_{lpf}(s) = \frac{R_{1p}}{s^2 \cdot R_{1p} C_{1p} R_{2p} C_{2p} + s\left[(R_{1p} + R_{2p}) C_{2p} + R_{1p} C_{1p} \right] + 1} \quad \textbf{(2.17)}$$

To obtain a more concise form for $H_{ol}(s)$, we can write the following time constants:

$$\tau_i = R_{2p} \cdot \frac{C_{2p} \cdot C_z}{C_{2p} + C_z} \quad \textbf{(2.18)}$$

$$\tau_{l0} = R_{1p} \cdot C_{1p} = \tau_l \quad \textbf{(2.19)}$$

$$\tau_{l1} = R_{2p} \cdot C_{2p} = k_1 \cdot \tau_l \quad \textbf{(2.20)}$$

$$\tau_{l2} = \left(R_{1p} + R_{2p} \right) \cdot C_{2p} = k_2 \cdot \tau_l \quad \textbf{(2.21)}$$

The open-loop transfer function given by (2.15) can be rewritten as:

$$H_{ol}(s) = \frac{G \cdot \left(s - z_1 \right) \cdot \left(s - z_2 \right)}{s^2 \cdot \left(s - p_1 \right) \cdot \left(s - p_2 \right) \cdot \left(s - p_3 \right)} \quad \textbf{(2.22)}$$

where,

$$G = \frac{I_{cp}}{2 \cdot \pi} \cdot \frac{1}{C_t} \cdot \frac{K_{vco}}{N} \quad \textbf{(2.23)}$$

$$R_t = R_{1p} \tag{2.24}$$

$$C_t = C_{2p} + C_z \tag{2.25}$$

The poles and zeros in equation (2.22) are given by:

$$z_1 = \frac{-\left[\left(1+k_2\right)\cdot\tau_1 + \gamma\cdot\alpha\cdot R_t\cdot C_t\right]}{2\left(k_1\cdot\tau_1^{\,2} + \gamma\cdot\alpha\cdot R_t\cdot C_t\cdot\tau_i\right)} + \sqrt{\left[\frac{\left(1+k_2\right)\cdot\tau_1 + \gamma\cdot\alpha\cdot R_t\cdot C_t}{2\left(k_1\cdot\tau_1^{\,2} + \gamma\cdot\alpha\cdot R_t\cdot C_t\cdot\tau_i\right)}\right]^2 - \left(\frac{1}{k_1\cdot\tau_1^{\,2} + \gamma\cdot\alpha\cdot R_t\cdot C_t\cdot\tau_i}\right)} \tag{2.26}$$

$$z_2 = \frac{-\left[\left(1+k_2\right)\cdot\tau_1 + \gamma\cdot\alpha\cdot R_t\cdot C_t\right]}{2\left(k_1\cdot\tau_1^{\,2} + \gamma\cdot\alpha\cdot R_t\cdot C_t\cdot\tau_i\right)} - \sqrt{\left[\frac{\left(1+k_2\right)\cdot\tau_1 + \gamma\cdot\alpha\cdot R_t\cdot C_t}{2\left(k_1\cdot\tau_1^{\,2} + \gamma\cdot\alpha\cdot R_t\cdot C_t\cdot\tau_i\right)}\right]^2 - \left(\frac{1}{k_1\cdot\tau_1^{\,2} + \gamma\cdot\alpha\cdot R_t\cdot C_t\cdot\tau_i}\right)} \tag{2.27}$$

$$p_1 = \frac{-\left(1+k_2\right)}{2\cdot k_1}\cdot\frac{1}{\tau_1} + \sqrt{\left(\frac{1+k_2}{2\cdot k_1}\cdot\frac{1}{\tau_1}\right)^2 - \left(\frac{1}{k_1\cdot\tau_1^{\,2}}\right)} \tag{2.28}$$

$$p_2 = \frac{-\left(1+k_2\right)}{2\cdot k_1}\cdot\frac{1}{\tau_1} - \sqrt{\left(\frac{1+k_2}{2\cdot k_1}\cdot\frac{1}{\tau_1}\right)^2 - \left(\frac{1}{k_1\cdot\tau_1^{\,2}}\right)} \tag{2.29}$$

$$p_3 = \frac{1}{\tau_i} \tag{2.30}$$

The closed-loop transfer function of the frequency synthesizer is given by:

$$H_{cl}(s) = \frac{H_{ol}(s)\cdot N}{1 + H_{ol}(s)} = \frac{G\cdot N\cdot\left(s - z_1\right)\cdot\left(s - z_2\right)}{s^2\cdot\left(s - p_1\right)\cdot\left(s - p_2\right)\cdot\left(s - p_3\right) + G\left(s - z_1\right)\cdot\left(s - z_2\right)} \tag{2.31}$$

The components of the frequency synthesizer are chosen to yield a closed-loop bandwidth of approximately 520 kHz which is the widest bandwidth to meet the FCC emission limits in the restricted band close to the 2.4GHz band.

Figure 2-11 shows the calculated phase noise contributions to the total phase noise of the frequency synthesizer using a Matlab model based on the system of equations described by (2.12) to (2.31). In a typical frequency synthesizer design, it is expected that the phase noise

of the VCO would dominate the phase noise at high frequency offset from the RF carrier. However, this is not the case in this transmitter design where, as shown in the figure, the phase noise of the ΣΔ modulator dominates the phase noise at high frequency offsets. This is acceptable in this design since wide bandwidth of operation is desired to support a high-data rate transmission as long as the transmitter RF emission requirements are met.

As with a conventional frequency synthesizer, it can be seen in the figure that the phase noise contributed by the resistors of the passive loop-filter is high-pass filtered at the frequency synthesizer's output by the transfer function, $1/(1+H_{ol}(s))$. Similarly, the VCO phase noise and the low-pass filter path charge pump noise are high-pass filtered by the same transfer function at the output of the frequency synthesizer. The integrator-path charge pump noise current is converted to voltage in the integrator path of the loop-filter given by $Z_{integ}(s)$. The presence of an integrator in $Z_{integ}(s)$ cancels the effect of high-pass filtering of the transfer function, $1/(1+H_{ol}(s))$, by which the integrator-path charge pump noise voltage is shaped. Hence, the integrator-path charge pump phase noise is effectively low-pass filtered as shown in Figure 2-11

Due to the low power consumption nature of the transceiver, it is required that biasing circuits consume a very small amount of power since they're required to be powered-up during the standby mode of the transceiver. For example, the chip's band-gap voltage reference used in the transceiver consumes several hundreds of nano-amperes from 1.8V supply. This ultra-low power consumption trades-off with its noise performance. The frequency synthesizer's charge pumps as well as the VCO use the chip's band-gap voltage reference. Hence, it is inevitable that the contribution of the charge pumps' flicker noise as well as the VCO's flicker noise are relatively high. This is evident in Figure 2-11 where the integrator-path charge pump and the VCO flicker noise components dominate the low frequency phase noise of the frequency synthesizer. By the same token, the crystal oscillator is needed in the standby mode of the transceiver. Hence, its power consumption directly trades-off with its phase noise

performance. As a result, the flicker noise of the crystal oscillator also contributes to the low frequency phase noise of the frequency synthesizer

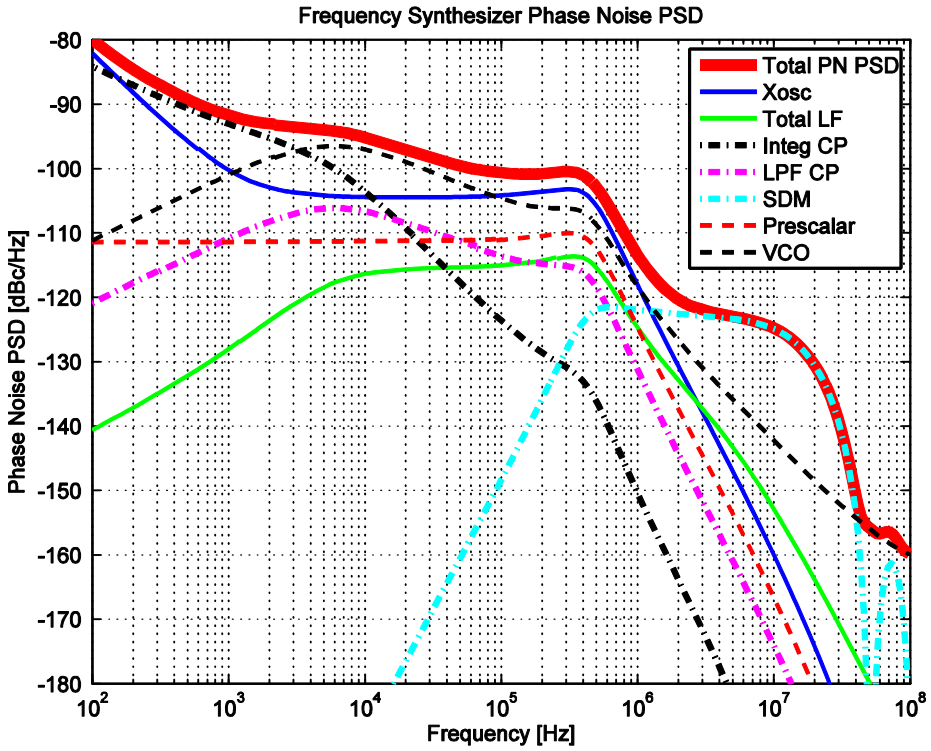


Figure 2-11 Contributors to phase noise of the frequency synthesizer in transmit mode at 2.48GHz

The prescalar noise appears at the frequency synthesizer output after being shaped by the closed-loop transfer function given by (2.31). The phase noise power spectral density due to the quantization noise of the third-order ΣΔ modulator (SDM) used in this design is given by [14]:

$$P_{npsd,sdm} = \frac{(2\pi)^2}{12 \cdot f_{clk,sdm}} \cdot \left(2 \cdot \sin\left(\frac{2\pi \cdot f_{offset}}{2 \cdot f_{clk,sdm}}\right) \right)^{2(N_{sdm}-1)} \qquad \textbf{(2.32)}$$

where, $f_{clk,sdm}$, is the ΣΔ modulator's sampling clock which is 52MHz and N_{sdm} is the order of the ΣΔ modulator which is three in this design. The ΣΔ modulator's phase noise power spectral density $P_{npsd,sdm}$ translates to phase noise at the frequency synthesizer output according to the following equation:

$$P_{opnpsd,sdm} = P_{npsd,sdm} \cdot \left| \frac{H_{ol}(s)}{1 + H_{ol}(s)} \right|^2 \quad \textbf{(2.33)}$$

It should be noted that there are non-linear mechanisms by which the phase noise of the ΣΔ modulator converts to phase noise at the output of the frequency synthesizer. These mechanisms are not captured in the linear time-invariant (LTI) analysis used in (2.33). Examples of such non-linear mechanisms are static and dynamic mismatches between the up and down currents of the charge pumps as well as reset delay mismatches in the logic cells used in the phase frequency detector (PFD).

The phase noise of the third-order ΣΔ modulator increases by 40dB per decade as shown in Figure 2-11. According to (2.31), the closed-loop transfer function of the frequency synthesizer has a fifth order response. The frequency synthesizer of this design has single poles approximately at 6kHz, 6MHz and 19 MHz and a double pole at 445kHz. However, the zero locations are approximately at 6kHz and 6MHz. Hence, there is a pole-zero cancelation at 6kHz and 6MHz. Effectively, the frequency synthesizer exhibits a third-order response with a double pole at 445kHz and a single pole at 19MHz. The double pole at 445kHz filters the ΣΔ modulator's phase noise. As a result, the phase noise of the ΣΔ modulator remains approximately flat between around 445kHz and 10MHz at the output of the frequency synthesizer. The phase noise of the ΣΔ modulator is filtered by the pole located at 19MHz as shown in Figure 2-11.

The ΣΔ modulator noise dominates the phase noise at the output of frequency synthesizer between 1MHz and 40MHz. The transmitter's phase noise level shown in Figure 2-11 has to be considered in the context of the various spectral emission requirements of several transmission standards which have to be met by the design. Figure 2-12 shows the calculated phase noise of the transmitter in dBc/MHz at 2.48GHz with +3dBm output power with respect to the most stringent spectral emissions masks for the ETSI EN 300-328 standard, the FCC 15.247 GL-36 standard and Bluetooth versions 1.2 and 2.0 standards. The FCC 15.247

GL-36 restricted-band specification at 2483.5 to 2500 MHz and at 2310 to 2390 MHz specifies a limit of -41.25dBm/MHz. Figure 2-12 shows that the transmitter design has a margin of 8dB on that specification at 3.5MHz offset from a 2.48GHz RF carrier.

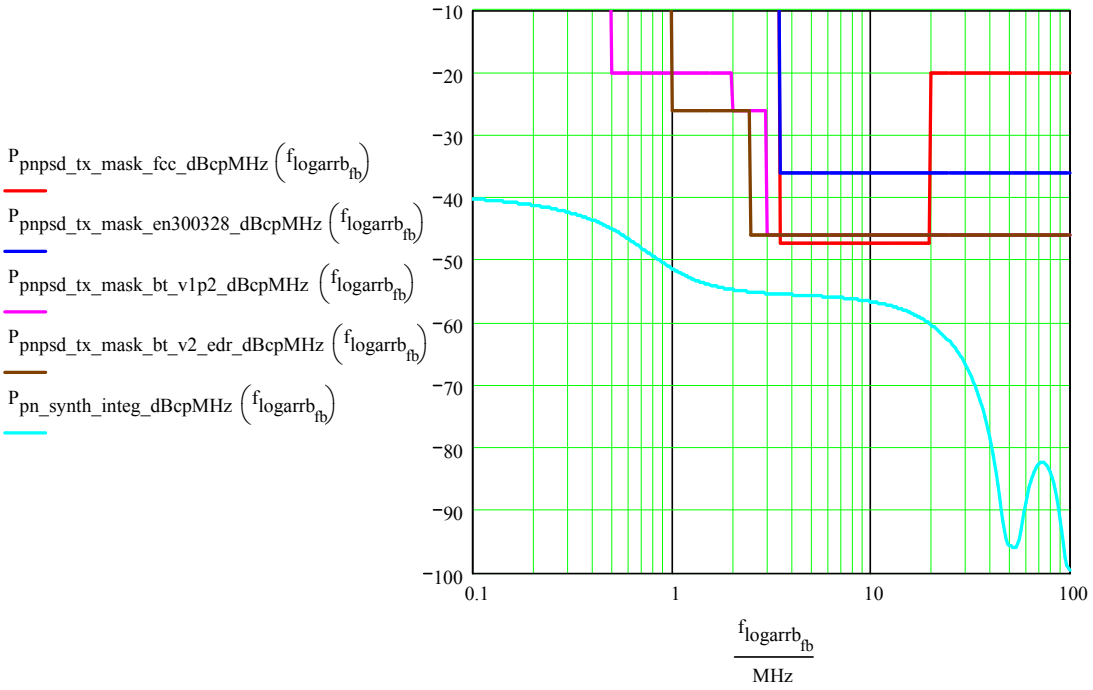


Figure 2-12 Spectral emissions masks for the transmitter in various regulatory standards at 2.48GHz

Having selected the frequency synthesizer bandwidth as wide as possible at 520kHz, the digital pre-emphasis filter (DPEF) shown in Figure 2-13 is implemented as a second order IIR filter with 16-bit coefficients. At a clock rate of 26MHz, it has about 24dB of digital pre-emphasis to extend the frequency synthesizer closed-loop bandwidth from 520kHz to 2MHz under nominal conditions. The IIR filter has a non-linear phase response; however, the non-constant group delay of the pre-emphasized phase response does not significantly affect the modulation quality as will be evident from simulation results and silicon measurements in subsequent sections.

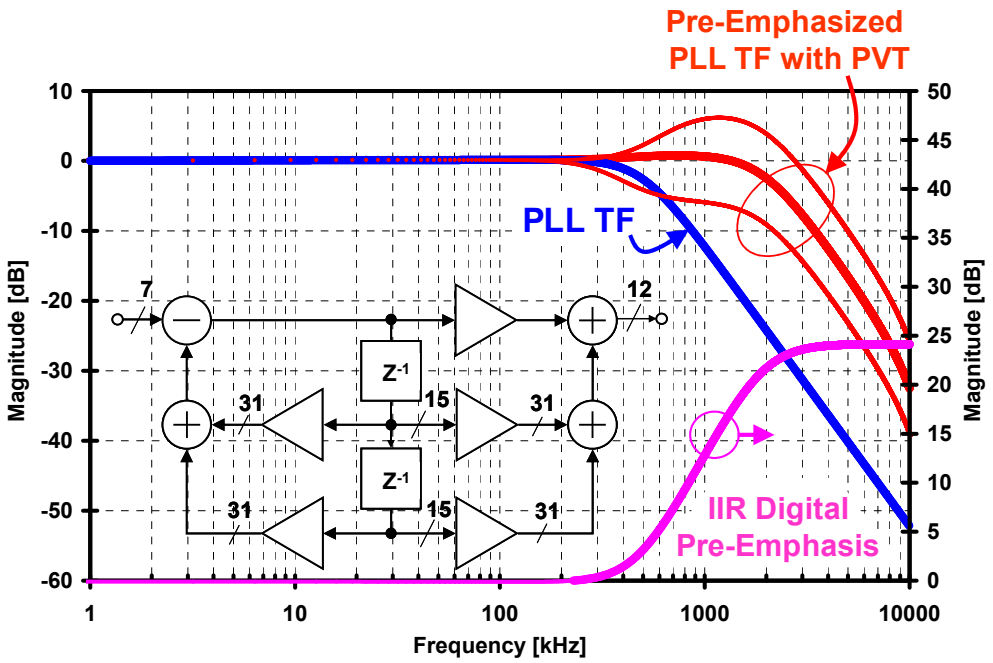


Figure 2-13 Digital pre-emphasis filter implementation

The frequency synthesizer's analog transfer function varies with process tolerances and temperature variations while the digital pre-emphasis filter, on the other hand, has a fixed digital transfer function. This gives rise to a mismatch between the analog and digital transfer functions. This mismatch causes the cascaded (analog+digital) bandwidth of the frequency synthesizer based transmitter to deviate significantly from the target bandwidth. As shown in Figure 2-13, in the presence of PVT variations such as VCO gain and RC variations, the effective pre-emphasized bandwidth can be as low as 1MHz. This seriously impairs the MER and phase error for GFSK and MSK modulation schemes typically processed by the transmitter.

It is crucial to maintain the accuracy of the match between the digital and analog transfer functions in order to guarantee a minimal variation of the cascaded frequency synthesizer transfer function. From simulations, the GMSK demodulator in the receiver requires that to receive a data rate of 2Mbps at the receiver sensitivity level, a worst-case RMS phase error of 10° for GMSK signals is required. This translates to the need to keep the bandwidth of the

cascade of the analogue frequency synthesizer transfer function and the DPEF to within ±10% of 2MHz. Hence, a calibration system is needed to maintain this level of accurate matching between the digital and analog transfer functions in the presence of process, temperature and supply variations. The details of this calibration system will be discussed in Chapter 3.

2.5 Conclusions

This chapter compared various RF modulator architectures. In particular, Cartesian- and frequency synthesizer- based RF modulators. From a survey of different frequency synthesizer-based RF modulators, a digital pre-emphasis architecture was shown to provide the lowest MER and power consumption using moderate silicon area with reasonable phase noise performance. A dual-path frequency synthesizer approach, with capacitive summation at the VCO tuning port, was selected for the implementation of the frequency synthesizer.

The bandwidth of the frequency synthesizer was chosen to be as wide as 520kHz while ensuring that its phase noise meets the spectral emission masks specified by various standards. As a result of using a frequency synthesizer with a wide bandwidth, the complexity of the digital pre-emphasis filter was reduced where it was implemented as a second order IIR filter with 16-bit coefficients. At a clock rate of 26MHz, it provided about 24dB of digital pre-emphasis to extend the frequency synthesizer closed-loop bandwidth from 520kHz to 2MHz under nominal conditions.

Since frequency synthesizer's analog transfer function varies with process tolerances and temperature variations while the digital pre-emphasis filter has a fixed digital transfer function, mismatch between the cascaded (analog+digital) bandwidth of the frequency synthesizer based transmitter deviate significantly from the target bandwidth. This mismatch requires a calibration system to maintain a relatively accurate match between the digital and analog transfer functions.

Chapter 3

Calibration System for the RF Transmitter

3.1 Mathematical Analysis of the Calibration System

Various schemes to calibrate the closed loop bandwidth of the frequency synthesizer exist in the literature. Some calibration schemes are closed-loop [15] [16] [17] while others are open-loop [18] [19]. McMahill *et al.* [15] show a closed-loop calibration system using an RF phase quantiser at the VCO output which is implemented using an RC phase splitter. This splitter needs to operate at the VCO frequency, which can be as high as 5GHz, thereby consuming a substantial amount of power; this is unacceptable for ultra-low power systems. Fontaine *et al.* [16] show an implementation of a wide bandwidth transmitter using a frequency synthesizer with a calibration scheme based on a frequency discriminator. The frequency discriminator operates on the RF output of the VCO where it is divided down from 1.8GHz to 270kHz and the peak amplitude of this signal is estimated and used as an input to a digital multiplier which scales the input data bit stream. This scheme is very power intensive and does not lend itself to ultra-low power transceivers. A closed loop calibration scheme is proposed in [17] which can calibrate out the variations of all the individual contributors to the overall variation of the closed loop bandwidth of the frequency synthesizer; however this method suffers from requiring an additional calibration port at the VCO input during calibration. Although the additional calibration port could also be used for modulation, extra circuitry is required for the second port in the case of the proposed transmitter where a pre-emphasis filter is needed. In addition, this closed-loop calibration scheme using a second port would introduce errors of its own once it is removed after calibration.

An open-loop calibration scheme is described in [18]. A calibration system is presented which applies a frequency step to the frequency synthesizer input and monitors the transient response at the VCO output. The most power consuming block in a frequency synthesizer is

the frequency divider which divides the RF signal down to the reference frequency. This block accounts for at least 50% of the overall power consumption. The scheme proposed in [18] uses at least two counters (8-bits each) and an accumulator (at least 16 bits) to count the VCO cycles. The VCO in our application operates at around 5 GHz. This means that during the calibration phase, the current consumption of the calibration circuit substantially exceeds that of the frequency synthesizer itself for a considerable period of time. In ultra-low power system this excess current consumption is not acceptable, even for a short amount of time. The proposed calibration system of this work consumes a maximum of 2% of the transmitter's overall power consumption.

The calibration scheme used in [19] is also open-loop and is based on locking the frequency synthesizer at two different frequencies with a known difference, Δf_{cal}, and measuring the difference, ΔV_{cal}, between the loop filter tuning voltages at each frequency. Using the value of $\Delta f_{cal}/\Delta V_{cal}$, the VCO gain and hence its variation from the nominal value can be estimated. These schemes use either a high-resolution analog-to-digital converter (ADC) to measure the loop filter tuning voltage directly or use an amplifier circuit which measures ΔV_{cal} and subsequently uses an ADC to digitize this value. The output of the ADC is then used to address a look-up table (LUT) whose output sets the charge pump current of the frequency synthesizer. By increasing (or decreasing) the charge pump current, the closed loop bandwidth of the frequency synthesizer increases (or decreases). This scheme has the main shortcoming that a high resolution ADC or a high accuracy difference amplifier is required to measure the frequency synthesizer's tuning voltage directly which can consume a large proportion of the chip area. In a wireless sensor node, low cost is critical and every effort is made to minimize the silicon real estate.

Given the above shortcomings of existing calibration systems, there is a need to develop a simple, accurate, area-efficient yet accurate calibration scheme for the target application. The proposed calibration system uses a mathematical property of closed-loop control systems.

Consider the second-order control system shown in Figure 3-1. The open-loop transfer function of this system can be written as:

$$G_{ol}(s) = \frac{\omega_n^{\,2}\left(1 + \frac{s}{(\omega_n / 2\zeta)}\right)}{s^2} \tag{3.1}$$

A zero was added at $\omega_n/(2\zeta)$ to the open-loop transfer function given by (3.1) in order to be consistent with the open-loop transfer function of the frequency synthesizer given by (2.22). The closed-loop transfer function of the system shown in Figure 3-1 is given by:

$$H_{cl,so}(s) = \frac{G_{ol}(s)}{1 + G_{ol}(s)} = \frac{\omega_n^{\,2}\left(1 + \frac{s}{(\omega_n / 2\zeta)}\right)}{s^2 + (2\zeta\omega_n)s + \omega_n^{\,2}} \tag{3.2}$$

where, $G_{ol}(s)$ is the open-loop transfer function of the system, $H_{cl,so}(s)$ is the closed-loop second-order transfer function, ζ is the damping factor and ω_n is the natural frequency [20].

If an input step, $x(t)$, is applied to the system, the output $y(t)$ will follow the input. The settling time of the output, $y(t)$, depends on the closed-loop bandwidth of the system. The error signal, $e(t)$, is the difference between $y(t)$ and $x(t)$. Although the figure shows an over-damped response for $y(t)$, the analysis below applies to any response.

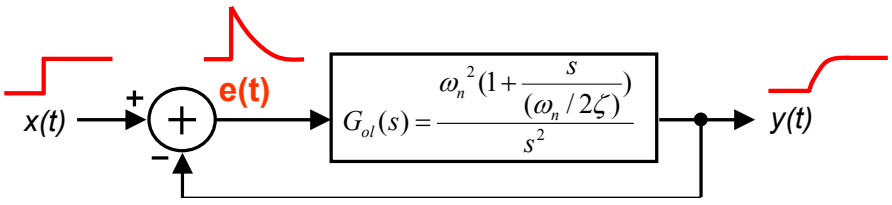


Figure 3-1 Response of a closed loop system with an input step

The error signal, $e(t)$, can be described in the s-domain by:

$$E(s) = X(s) - Y(s) = X(s) \cdot [1 - H_{cl,so}(s)] \tag{3.3}$$

this implies that,

$$E(s) = X(s) \cdot \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^{\,2}} \tag{3.4}$$

If a step is applied to the input of the closed-loop system shown in Figure 3-1, *X(s)* is given by *1/s* which yields:

$$E(s) = \frac{s}{s^2 + 2\zeta\omega_n s + \omega_n{}^2} \tag{3.5}$$

The double integral of the error signal *e(t)* is given by:

$$E_{di}(s) = \frac{1}{s^2} E(s) = \frac{1}{s(s^2 + 2\zeta\omega_n s + \omega_n{}^2)} \tag{3.6}$$

The reason for the use of double-integration in (3.6) is related to the use of both analog integration as well as digital integration in the calibration system. This will be further explained with the aid of Figure 3-5 in section 3.2. The final value of the double integral of the error signal *e(t)* can be predicted using the final value theorem **[21]** . The theorem calculates the final value of the double integral of the error signal *e(t)* as time approaches infinity using the frequency domain representation given in (3.6) as follows:

$$\lim_{t\to\infty} e_{di}(t) = \lim_{s\to 0} s \cdot E_{di}(s) = \frac{1}{\omega_n{}^2} \tag{3.7}$$

By inspecting equation (3.1), it can be seen that the open-loop gain of the second order system of Figure 3-1 is given by $\omega_n{}^2$. Equation (3.7) indicates that the final value of the double integral of the error signal *e(t)* is equal to the inverse of the loop gain of the system shown in Figure 3-1.

The relationship given in (3.7) can be generalized for any open-loop transfer function, $G_{ol,n}$, with an *n* and *m* number of zeros and poles respectively. Consider a system with the following open-loop transfer function:

$$G_{ol,n}(s) = \frac{\omega_n{}^2}{s^2} \frac{(1 + \frac{s}{\omega_{z1}})(1 + \frac{s}{\omega_{z2}})...(1 + \frac{s}{\omega_{zn}})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})...(1 + \frac{s}{\omega_{pm}})} \tag{3.8}$$

The closed-loop transfer function of such a system is given by:

$$H_{cl,so,n}(s) = \omega_n{}^2 \frac{(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})...(1+\frac{s}{\omega_{zn}})}{s^2(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})...(1+\frac{s}{\omega_{pm}}) + \omega_n{}^2(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})...(1+\frac{s}{\omega_{zn}})} \quad \textbf{(3.9)}$$

The s-domain representation of the error signal, *e(t)*, is given by:

$$E_n(s) = X_n(s) - Y_n(s) = X_n(s) \cdot [1 - H_{cl,so,n}(s)] \quad \textbf{(3.10)}$$

which yields,

$$E_n(s) = \frac{s \cdot (1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})...(1+\frac{s}{\omega_{zn}})}{s^2(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})...(1+\frac{s}{\omega_{pm}}) + \omega_n{}^2(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})...(1+\frac{s}{\omega_{zn}})} \quad \textbf{(3.11)}$$

The double integral of the error signal $E_n(s)$ is given by:

$$E_{n,di}(s) = \frac{1}{s} \frac{(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})...(1+\frac{s}{\omega_{zn}})}{s^2(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})...(1+\frac{s}{\omega_{pm}}) + \omega_n{}^2(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})...(1+\frac{s}{\omega_{zn}})} \quad \textbf{(3.12)}$$

Using the final value theorem given by (3.7):

$$\lim_{t\to\infty} e_{n,di}(t) = \lim_{s\to 0} s \cdot E_{n,di}(s) = \frac{1}{\omega_n{}^2} \quad \textbf{(3.13)}$$

Equation (3.13) indicates that the final value of the double integral of the error signal $e_{n,di}(t)$ is equal to the inverse of the open-loop gain of the system shown in Figure 3-1 with an open-loop transfer function of *n* and *m* number of zeros and poles respectively.

Equation (3.1) can be used to compute the unity-gain frequency (UGF) of the system described in Figure 3-1 as follows:

$$\left\|G_{ol}(j\omega)\right\| = \frac{\omega_n{}^2}{\omega_{ugf}{}^2}\sqrt{1+\left[\frac{\omega_{ugf}{}^2}{(\omega_n/2\zeta)^2}\right]} = 1 \quad \textbf{(3.14)}$$

In practice, the UGF of the open-loop response of a frequency synthesizer is much higher than the open-loop zero frequency located at $\omega_n/(2\zeta)$. Using $\omega_{ugf}/[\omega_n/(2\zeta)] >> 1$ in equation (3.14) yields,

$$\omega_{ugf} \approx 2\zeta\omega_n \tag{3.15}$$

In addition, equation (3.2) can be used to compute the closed-loop 3dB bandwidth of the system described in Figure 3-1 as follows:

$$\left\|H_{cl,so}(j\omega)\right\| = \sqrt{\frac{1+\left[\frac{\omega_{clbw}}{(\omega_n/2\zeta)}\right]^2}{(1-\frac{\omega_{clbw}^{\ 2}}{\omega_n^{\ 2}})^2+\left[\frac{\omega_{clbw}}{(\omega_n/2\zeta)}\right]^2}} = \frac{1}{\sqrt{2}} \tag{3.16}$$

The CLBW of the closed-loop response of a frequency synthesizer is much higher than the open-loop zero frequency located at $\omega_n/(2\zeta)$. Using $\omega_{clbw}/[\omega_n/(2\zeta)] >> 1$ in equation (3.16) yields,

$$\omega_{clbw} \approx 2\zeta\omega_n\sqrt{1+\frac{1}{2\zeta^2}} \tag{3.17}$$

To gain further insight into the foregoing system of equations, Figure 3-2 shows the relationship between three parameters; the first parameter, represented on the x-axis of the figure, is the deviation of the double integral (DI) of the error signal $e(t)$ from its nominal value as defined by:

$$\iint_T e(t)dt - \left[\iint_T e(t)dt\right]_{nom}, \tag{3.18}$$

where, $\iint_T e(t)dt$ is the double integral (DI) of the error signal and $\left[\iint_T e(t)dt\right]_{nom}$ is the nominal value of the double integral (DI) of the error signal which corresponds to the nominal bandwidth of the system described in (3.1). The double integral used in Figure 3-2 is computed by applying a step function to the system shown in Figure 3-1 and described by (3.1) using Matlab simulations.

The second parameter is the normalized inverse of the open-loop gain with respect to its nominal value. The third parameter is the normalized inverse of the UGF with respect to its nominal value for the second order system described in (3.2). The second and third parameters are represented by:

$$\frac{1/OLG}{1/OLG_{nom}} \text{ and } \frac{1/\omega_{ugf}}{1/\omega_{ugf,nom}} \tag{3.19}$$

where, OLG and ω_{ugf} are the open-loop gain and the UGF respectively as defined by equations (3.1) and (3.15). OLG_{nom} and $\omega_{ugf,nom}$ are the nominal open-loop gain and the nominal UGF respectively. The parameters OLG and ω_{ugf} shown in Figure 3-2 are computed using Matlab simulations.

Figure 3-2 shows the relationship between these parameters for values of ω_n between $2\pi\cdot125$kHz and $2\pi\cdot375$kHz with the parameter ζ held constant at 0.9. The choice of the values of ζ and ω_n is sufficient for the purpose of illustration. It will be illustrated shortly that both parameters depend on the actual system's components and are inter-dependent. Figure 3-2 shows the simulated and theoretical values for the OLG and UGF versus the deviation of the double integral (DI) of the error signal *e(t)* from its nominal value. As shown in the figure, the relationship between the deviation of the double integral (DI) of the error signal *e(t)* from its nominal value and the inverse of the OLG is linear as expected from (3.7). On the other hand, the relationship between the deviation of the double integral (DI) of the error signal *e(t)* from its nominal value and the inverse of the UGF is non-linear as expected from (3.7) and (3.15). It should be noted that the relationship depicted in Figure 3-2 is for a constant value of ζ which makes the UGF proportional to the square-root of the OLG.

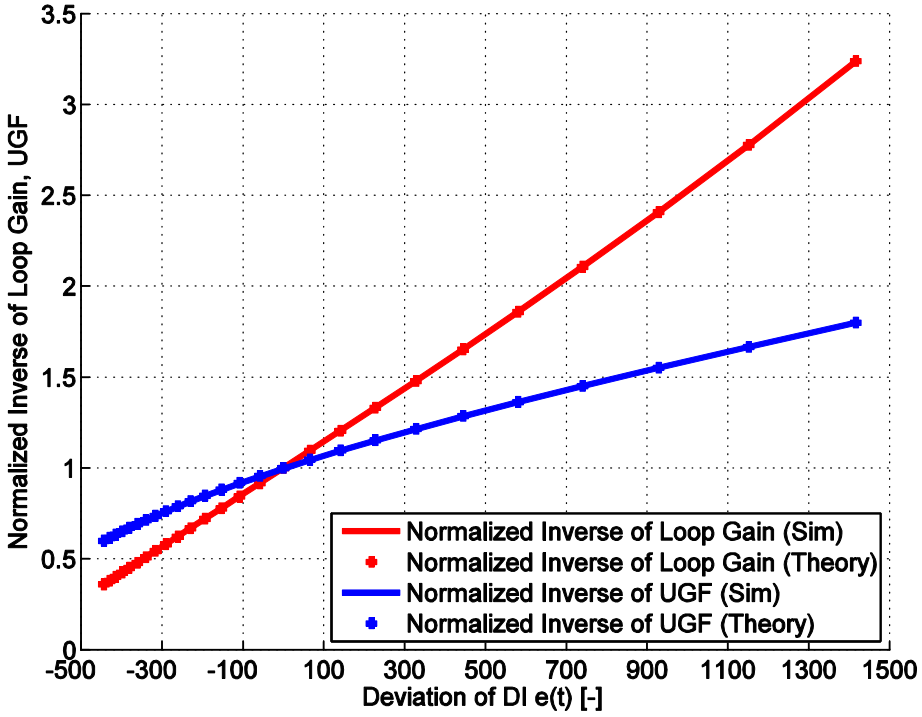


Figure 3-2 Relationship between the double integral of the error signal *e(t)* and the normalized inverse of the open-loop gain and UGF for a second order system

Intuitively, it can be deduced from Figure 3-2 that the time spent by the output to reach its target value, and hence the time spent by the error signal to decay to zero, increases, as the closed-loop bandwidth of the system decreases, resulting in an increase in the value of the integral of the error signal. The inverse of this relationship holds when the closed-loop bandwidth of the system increases.

The closed-loop transfer function of a conventional second order type-II frequency synthesizer similar to the one shown in Figure 2-2 is given by [22]:

$$H_{cl,conv}(s) = \frac{\frac{I_{cp}K_{vco}}{2\pi C_P}(R_p C_p s + 1)}{s^2 + \frac{I_{cp}K_{vco}R_p}{2\pi \cdot N}s + \frac{I_{cp}K_{vco}}{2\pi C_P \cdot N}} \quad \textbf{(3.20)}$$

where, I_{cp} is the charge pump current of the frequency synthesizer, K_{vco} is the VCO gain. The frequency synthesizer's loop filter is a series combination of the resistor, R_p, and the

capacitor, C_p. The denominator of the closed-loop transfer function given by (3.20) can be used to determine the values of ζ and ω_n by inspecting the closed-loop transfer function of the second-order system given by (3.2). The values of ζ and ω_n are thus given by:

$$\omega_n = \sqrt{\frac{I_{cp} \cdot K_{vco}}{2\pi \cdot C_P \cdot N}} \tag{3.21}$$

$$\zeta = \frac{R_p}{2} \cdot \sqrt{\frac{I_{cp} \cdot C_P \cdot K_{vco}}{2\pi \cdot N}} \tag{3.22}$$

By using the following simplifications:

$$I_{cp} = \frac{V_{bg}}{m \cdot R} \tag{3.23}$$

where, V_{bg} is the IC's band-gap reference voltage, R is a unit resistor and m is a multiplying factor.

$$R_p = n \cdot R \tag{3.24}$$

where, n is a multiplying factor. Based on equations (3.21) to (3.24), ζ and ω_n can be rewritten as:

$$\omega_n = \sqrt{\frac{V_{bg}}{m} \cdot \frac{K_{vco}}{2\pi \cdot N} \cdot \frac{1}{RC_p}} \tag{3.25}$$

and

$$\zeta = \frac{n}{2} \cdot \sqrt{\frac{V_{bg}}{m} \cdot \frac{K_{vco}}{2\pi \cdot N} \cdot RC_p} \tag{3.26}$$

According to (3.15), the unity-gain frequency of a conventional second order type-II frequency synthesizer is given by:

$$\omega_{ugf} \approx 2\zeta\omega_n = \frac{n}{m} \frac{V_{bg} \cdot K_{vco}}{2\pi \cdot N} \tag{3.27}$$

It can be seen from equations (3.20), (3.25) and (3.26) that a second-order type-II frequency synthesizer posses similar characteristics to those of the second order system described by the system of equations (3.2) to (3.17). Hence, it would exhibit a similar relationship to that

depicted in Figure 3-2. The parameters ζ and ω_n of the frequency synthesizer are dependent on the same set of the parameters; V_{bg}, K_{vco}, N and RC_p as noted previously. Hence, a method to stabilize those parameters in the presence of various manufacturing, supply and temperature variations would stabilize the dynamics of the frequency synthesizer.

It is interesting to note that equation (3.27) shows that the UGF is independent of the RC time-constant of the frequency synthesizer. This can be attributed to the formula for the UGF of the open-loop response of a frequency synthesizer in (3.14) which was computed with the assumption that the UGF is much higher than the open-loop zero frequency located at $\omega_n/(2\zeta)$ and using the approximation $\omega_{ugf}/[\omega_n/(2\zeta)] >> 1$. This approximation will be validated with the aid of Figure 3-7.

The frequency synthesizer used in this work is shown in Figure 2-8 and described by the closed-loop transfer function in equation (2.31). It can be seen that the frequency synthesizer has a fifth order closed-loop transfer function. However, there is a pole-zero cancelation at 6kHz and 6MHz. Effectively, the frequency synthesizer exhibits a third-order response with a double pole at 445kHz and a single pole at 19MHz. This does not affect the generality of the argument being discussed regarding the fundamental trade-off between the bandwidth of a closed-loop system and the settling of its error signal.

Based on the analysis shown in equations (3.8) to (3.13), a relationship similar to the one shown in Figure 3-2 can be developed for a frequency synthesizer of any order since this relationship depicts the fundamental trade-off between the bandwidth of a closed-loop system and the settling of its error signal. The linearity of such a relationship can be investigated with the aid of simulations based on a mathematical model for the frequency synthesizer used in this work. Section 3.2 will illustrate the existence of such a relationship and describe a calibration system for the RF modulator based on the aforementioned mathematical analysis for second-order systems.

3.2 Implementation of the RF Modulator Calibration System

By examining the system of equations given by (3.20) to (3.26), it can be seen that in order to keep the transfer function constant in the presence of parameter variations, the values of V_{bg}, K_{vco}, N and RC_p potentially need to be kept relatively constant by means of a calibration. These parameters are not specific to a second order frequency synthesizer. Examining the closed-loop transfer function of a fifth order frequency synthesizer given by equations (2.23) and (2.31) shows an equivalent requirement to stabilize (or calibrate) the parameters V_{bg}, K_{vco} and N in the presence of manufacturing, supply and temperature variations. The RC time constants of a fifth order frequency synthesizer are given by equations (2.18) to (2.21). Although the number of time constants is higher than that of a second-order frequency synthesizer, the potential requirement of maintaining a constant RC time constant is the same in both cases. To be able to perform the required calibration, the relationship between the double integral of the error signal of the frequency synthesizer's transfer function and these parameters needs to be examined.

A frequency synthesizer is a closed loop control system as shown in Figure 3-3. When a frequency synthesizer is used as a transmitter, the average value of the N-divider is determined by the channel frequency, the deviation frequency set by the modulation scheme and the digital data to be transmitted. The ΣΔ modulator provides the noise-shaping required to achieve the fractional part of the N-divider. If bit '1' is to be transmitted, the average effective value of the N-divider, $N = N_{channel} + \Delta N_D$, is used. If bit '0' is to be transmitted the average value $N = N_{channel} - \Delta N_D$ is used, where $N_{channel}$ is the average N-divider value corresponding to $f_{channel}$, the center frequency of the synthesizer and ΔN_D is the digital value corresponding to the required frequency deviation, Δf, at the frequency synthesizer output. As a result, the center frequency, $f_{channel}$, of the frequency synthesizer changes to $f_{channel} + \Delta f$ in response to bit '1' and to $f_{channel} - \Delta f$ in response to bit '0'.

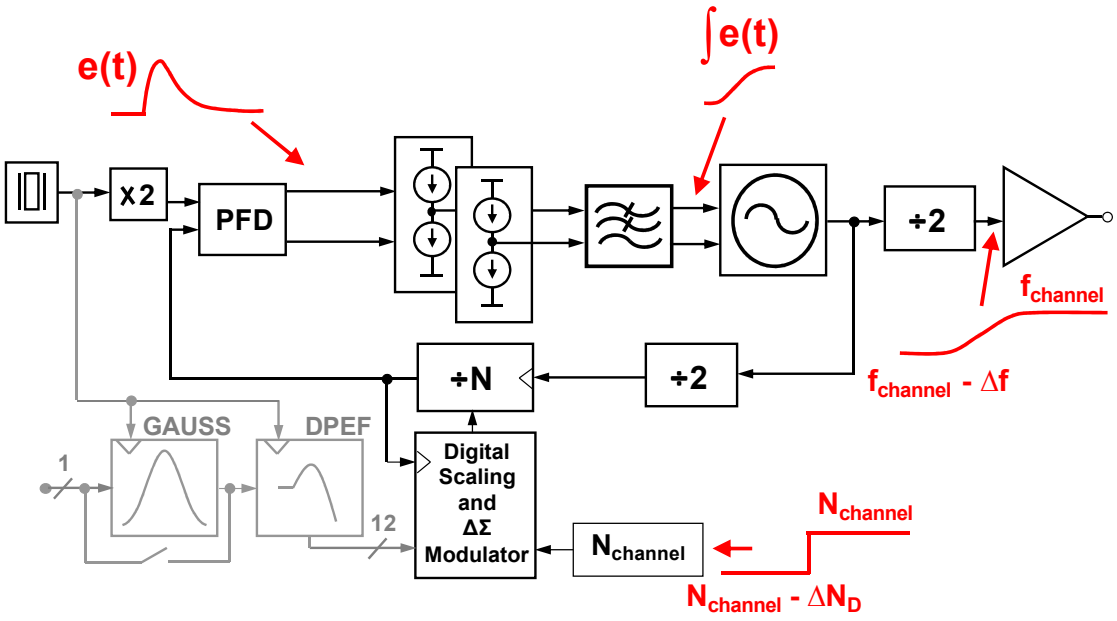


Figure 3-3 Applying an input frequency step to the frequency synthesizer

Considering the idea illustrated in Figure 3-1, a step input from $N = N_{channel} - \Delta N_D$ to $N = N_{channel}$ is applied to the frequency synthesizer. As a result, the output of the frequency synthesizer transitions from $f_{channel} - \Delta f$ to $f_{channel}$, as shown in Figure 3-3. The amount of time it takes this transition to occur depends on the bandwidth of the frequency synthesizer. The error signal, *e(t),* as shown in Figure 3-4, is the difference between the input, *x(t)*, and the output, *y(t)*, of the frequency synthesizer when a frequency step of Δf is applied to the input *x(t)* corresponding to the transition from data bit '0' to data bit '1'. The area under the error curve of *e(t)* is the integral of this error signal. This is illustrated conceptually in Figure 3-4 for the system shown in Figure 3-1.

If the bandwidth of the frequency synthesizer is lower than the nominal value, illustrated by the blue curve, it takes a longer time for the frequency synthesizer output, *y(t)*, illustrated by the green curve, to reach its final level and hence the area under the error curve is higher with respect to the nominal area. On the contrary, if the bandwidth of the frequency synthesizer is higher than the nominal value, it takes a shorter time for the frequency synthesizer output, illustrated by the red curve, to reach the final level and hence the area under the error curve is

lower with respect to the nominal area. The area under this error curve represents the integration of the error signal, *e(t)*. From simulations of Figure 3-2, it has been shown that the relationship between the double integral of *e(t)* and the inverse of the UGF could potentially be approximated by a linear relationship. Simulations to validate this statement will follow.

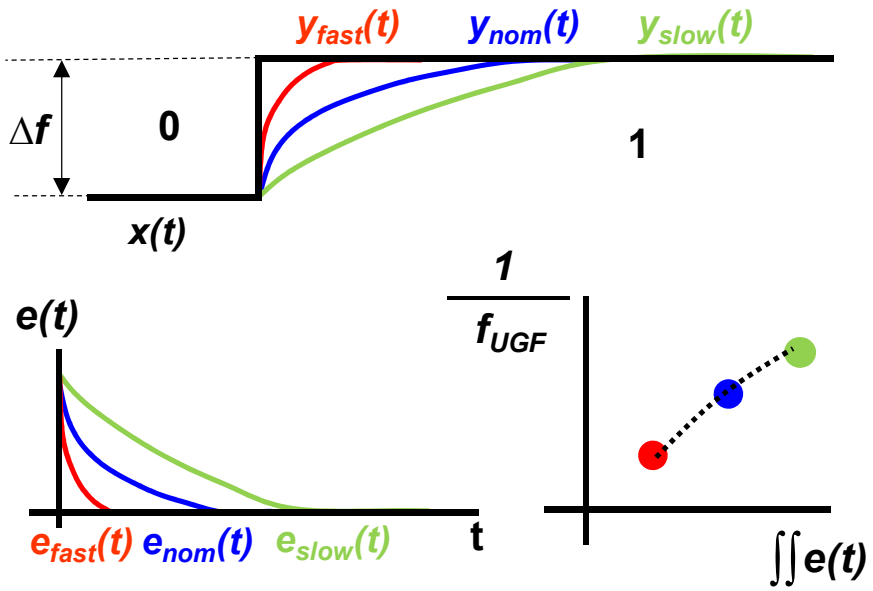


Figure 3-4 Conceptual view of applying an input frequency step to the frequency synthesizer

In order to utilize the mathematical property between the double integral of *e(t)* and the inverse of the unity-gain frequency to predict the bandwidth of the frequency synthesizer, the error signal *e(t)* needs to be identified. As shown in Figure 3-3, when an input frequency step is applied, the outputs of the PFD will generate up and down pulses to the charge pump. The net width of a pulse is proportional to the phase error between the VCO and the crystal oscillator reference frequency, hence this is the error signal, *e(t)* that we require in the frequency synthesizer to predict its bandwidth. The integral of this error signal is also available at the integrator path of the loop filter. The integral of the error signal can be digitized directly with a high resolution ADC. For example, if a value of N_D which is equivalent to a 1.5MHz step is applied and the VCO has a gain of 40MHz/V, the steady-state value of the integrated error signal, which is also the tuning voltage port to the VCO, is about

37.5mV. A 12-bit ADC has an LSB of 0.3mV from a 1.2V reference, yielding 125 LSBs which can capture the transient of the error signal. For ultra-low power devices, such a high-resolution ADC is not practically available on the chip; therefore, a method needs to be devised to extract the integral of the error signal from the frequency synthesizer system. It is possible to use an amplifier to amplify the integral of the error signal available at the integrator path of the loop filter in order to use a lower resolution ADC. However, with a steady-state value of 37.5mV for the integrated error-signal, the amplifier impairments such as DC offset voltage become comparable to the signal which needs to be measured. A switched-capacitor amplifier can be used to cancel the DC offsets. However, a switched capacitor amplifier will need to be placed very close to the integrator path loop filter due to the absence of a differential voltage for the integral of the error signal. This necessitates the generation of a divided down clock from the reference clock that physically runs close to the loop filter. It is a design risk to run that reference clock or any fraction of it close to the loop filter since reference spurs can be generated by direct coupling to the loop filter's output even if the clock path is switched off, for example, via direct capacitive coupling. In addition, the large size of the capacitors typically used in switched-capacitor amplifiers make this design choice less attractive.

Figure 3-5 shows a very low power, digitally-assisted and area-efficient system of extracting an amplified replica of the integral of the error signal from the frequency synthesizer, without using a high resolution ADC or a voltage summing amplifier [23], [24]. The system detects the error signal, *e(t)* at the PFD outputs. A calibration charge pump is used to convert the digital pulses at the output of the PFD to current pulses at the charge pump output. This calibration charge pump is tightly matched to the integrating charge pump of the frequency synthesizer. The current pulses from the calibration charge pump are integrated on an integrating capacitor, C_{cal}, for a predetermined amount of time, T_{int}, to generate a voltage signal which represents the integral of the error signal *e(t)*. Since a calibration charge pump is being used, it is possible to scale its current to a higher value relative to the integrating charge

pump current if required. This can be used to amplify the error signal such that the voltage level created on the integrating capacitor can be digitized with a low-resolution 6-bit pipelined ADC. The use of a charge pump and an integrating capacitor also controls the ramp rate of the integral of the error signal which allows for digitizing this signal in the most linear region of the transient response of the frequency synthesizer and hence improving the accuracy of the measurement.

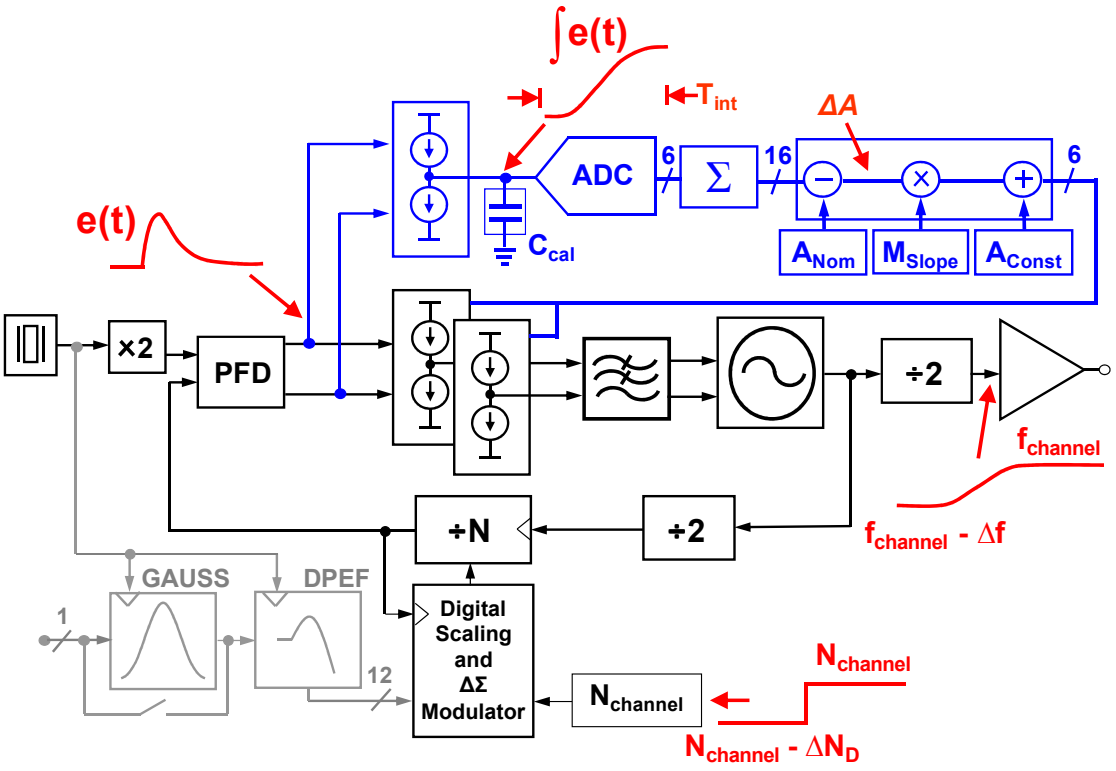


Figure 3-5 Calibration system for the frequency synthesizer.

The voltage developed on the capacitor, C_{cal}, is digitized by the ADC. Since the ADC resolution is only 6 bits, it is not sufficient to accurately detect the steady state of the integral of *e(t)* in the presence of various parameter variations. Hence, the output of the ADC is further digitally integrated to capture the transient behavior of the analog integral of the error signal, *e(t)*. This is further illustrated by the measurements depicted in section 0.

Using a mathematical model for the frequency synthesizer shown, Figure 3-6 shows the results of a Matlab simulation for the relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* from the nominal value representing the nominal bandwidth of the frequency synthesizer. The simulations were performed in the presence of ±20% variation in the loop filter resistors, R, ±10% variation in the loop filter capacitors, C, ±25% variation in the VCO gain, $K_{vco,}$ ±5% variation in the band-gap reference voltage, V_{bg} and ±5% variation in the channel frequency, $f_{channel}$, which also leads to a variation in the effective value of the N-divider, N. The deviation of the double-integral of *e(t)* from the nominal value is shown as ΔA in Figure 3-5. The relationship, shown in Figure 3-6, is obtained using the double-integration of the error signal, *e(t),* due to the step response of the frequency synthesizer transfer function described by the system of equations defined by (2.12) to (2.31). No approximations were made to the frequency synthesizer's transfer function to obtain the results of Figure 3-6. The inset shows the error signal, *e(t),* in the presence of V_{bg}, K_{vco}, N, R and C variations. It is to be noted that the sweep of N is replaced by a sweep of $f_{channel}$ which is the practical parameter to be considered. It is also worth noting that the mathematical model of the frequency synthesizer includes the practical dependence of K_{vco} on $f_{channel.}$ This dependency is due to employing a multi-band VCO which uses switched capacitors across its tuning inductor. At one end of the tuning range, all the switched capacitors are switched on and the VCO gain, K_{vco}, is lowest compared to the other end of the tuning range with all the switched capacitors switched off.

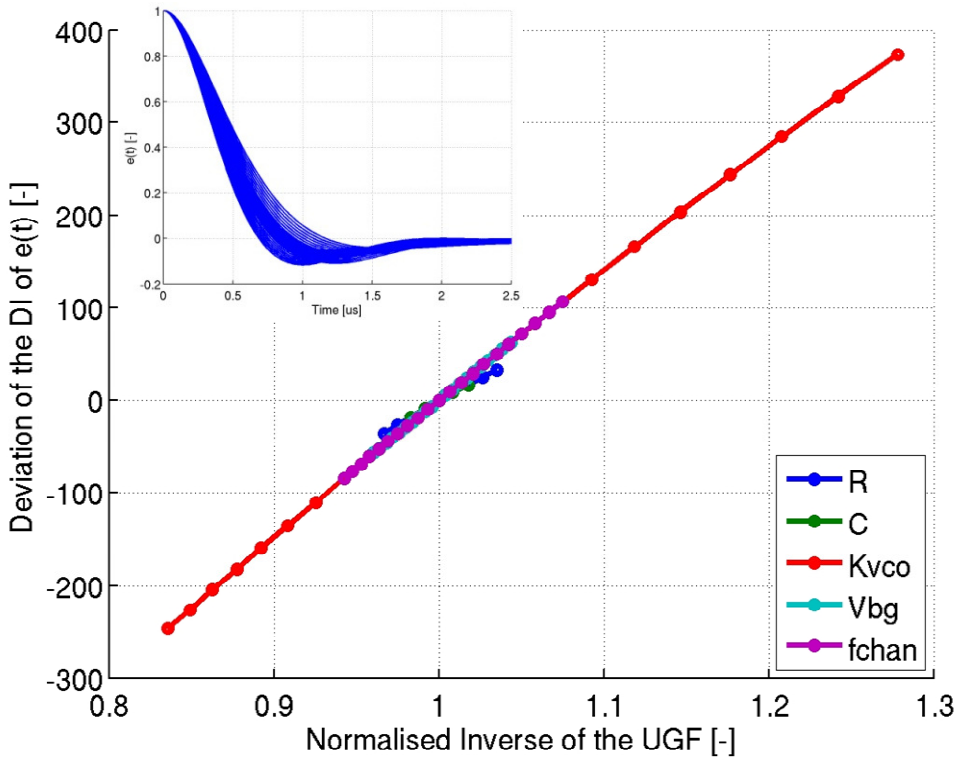


Figure 3-6 Relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* in the presence of *R, C,* K_{vco}, V_{bg} and $f_{channel}$ variation

The following observations can be made from Figure 3-6:

1. The deviation of the double-integral of *e(t)* from its nominal value in the presence of each of ±25% variation in K_{vco}, ±5% variation in V_{bg} and ±5% variation in $f_{channel}$ can be each approximated as a linear function of the normalized inverse of the UGF with approximately the same slope. In addition, the deviation of the double-integral of *e(t)* from its nominal value in the presence of each of ±20% variation in *R* and ±10% variation in *C* can be approximated as a linear function of the normalized inverse of the UGF, albeit, with a different slope. The intuitive reason that the slopes of these functions are different is the fact that the *R* and *C* components of the frequency synthesizer set the open-loop gain at frequencies close to DC in addition to the locations of poles and zeros of the open-loop transfer function given by (2.22). In the presence of *R* and *C* variations, the low frequency gain of the open-loop transfer function, as well as the locations of its poles and zeros, will vary. On the other hand,

$K_{vco,}$ V_{bg} and $f_{channel}$ set the low frequency gain of the open-loop transfer function of the frequency synthesizer, without affecting its poles and zeros.

2. The dominant sources for the variation of the UGF of the frequency synthesizer are K_{vco} variation, followed by $f_{channel}$ variation. It is to be noted that the variation of $f_{channel}$ also contributes to the variation of K_{vco} since they are inter-dependent in the VCO design.
3. Despite the variation of C by almost the same amount as $K_{vco,}$ its contribution as well as that of R to the overall variation of the UGF is much smaller. This can be explained by noting that the UGF of a second order system in the form given in (3.1) is, to a first order, independent of R and C as shown in equation (3.27).
4. The variation in V_{bg} contributes to the variation of the UGF of the frequency synthesizer. However this variation cannot be compensated for or calibrated by the calibration system of Figure 3-5 since both the calibration charge pump and the integrator path charge pump share the same band-gap reference voltage, V_{bg}. Hence, the calibration system is insensitive to its variation. This is not unique to this calibration system since any calibration system will use a band-gap reference for its measurement circuitry. The goal is to reduce the variation of V_{bg} in the first place. This is helped by the fact that the design of the band-gap reference is independent of the design of the frequency synthesizer. A typical target for the on-chip band-gap reference is ±3% without any circuit calibration.

Figure 3-7 compares the relationship between the deviation of the double-integral of *e(t)* and the normalized inverse of the UGF in the presence of simultaneous variations in the parameters; *R, C,* K_{vco} *and* $f_{channel}$ versus the relationship between the deviation of the double-integral of *e(t)* and the normalized inverse of the UGF in the presence of only simultaneous variations in K_{vco} and $f_{channel}$. Simultaneous variations in *R, C,* K_{vco} *and* $f_{channel}$ mean that Figure 3-7 shows all possible combinations of *R, C,* K_{vco} and $f_{channel}$ when they are varied unlike Figure 3-6 which showed the independent variations of each of *R, C,* K_{vco} and $f_{channel}$.

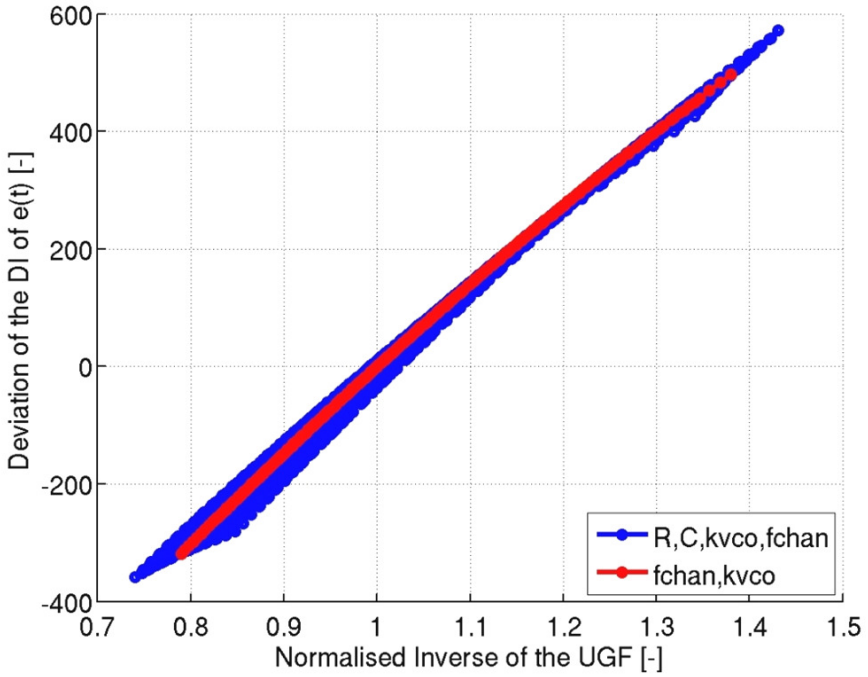


Figure 3-7 Comparison between the relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* in the presence of simultaneous variations of *R, C,* K_{vco} and $f_{channel}$ and simultaneous variations of only K_{vco} and $f_{channel}$

It can be observed from Figure 3-7 that it would be possible to consider only variations in K_{vco} and $f_{channel}$ and ignore the variations in R and C for the purpose of calibrating the frequency synthesizer bandwidth. This observation will be utilized and further verified in subsequent sections. Figure 3-8 shows the relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* in the presence of ±25% variation in the frequency synthesizer's LPF path and integrator path charge pump unit currents given by I_{cp}**.** It can be observed from the figure that the relationship can be approximated by a linear relationship and the slope of this relationship is almost identical to the slope of the relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* in the presence of K_{vco} and $f_{channel}$ variations. The purpose of examining this relationship is to verify that the frequency synthesizer's LPF path and integrator path charge pump currents can be

used to control its bandwidth based on the deviation of the double-integral of *e(t)* from the nominal value.

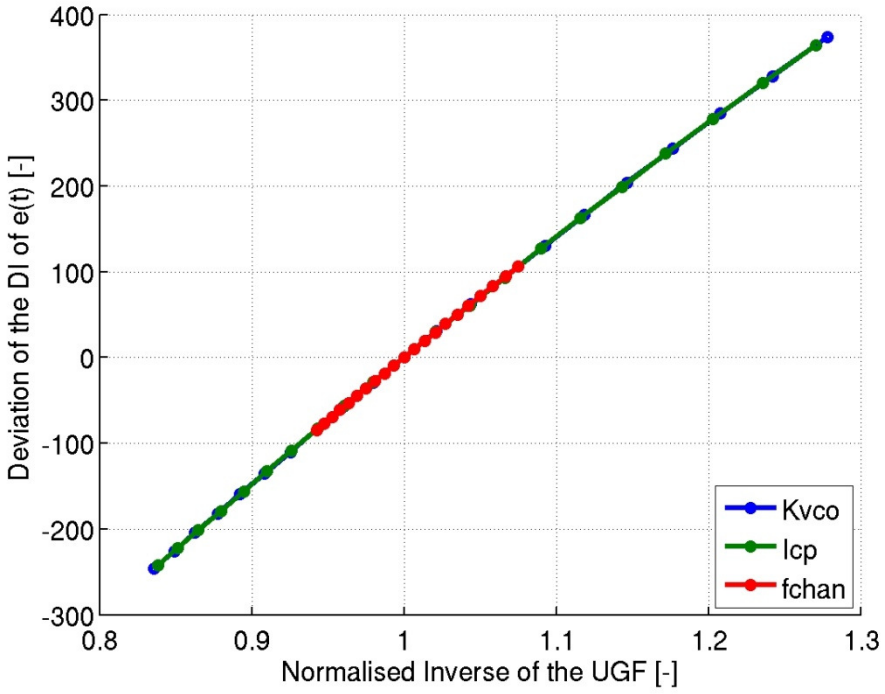


Figure 3-8 Relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* in the presence of I_{cp}, K_{vco} and $f_{channel}$ variation

Referring back to Figure 3-5, the goal of examining the relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* from a nominal value (ΔA in Figure 3-5) in the presence of the frequency synthesizer's component variations is to use this relationship to calibrate the bandwidth of the frequency synthesizer. From Figure 3-6 and Figure 3-7, it can be observed that the deviation of the double-integral of *e(t)* from the nominal value (which represents the nominal bandwidth) is inversely proportional to the UGF of the frequency synthesizer and hence its closed-loop bandwidth. The relationship in Figure 3-7 can be approximated by a linear function, whose slope is given by M_{slope} and constant given by A_{const}, as shown in Figure 3-5. Furthermore, Figure 3-8 shows that the relationship between the normalized inverse of the UGF and the deviation of the double-integral of *e(t)* in the presence of variation in the frequency synthesizer's LPF path and integrator path charge

pump, I_{cp}, can be approximated by a linear relationship with the same slope as the relationship which involves K_{vco} and $f_{channel}$ variations. This relationship can also be observed in view of the frequency synthesizer open-loop transfer function given by (2.23), where the low frequency gain of the open-loop transfer function is proportional to $I_{cp} \cdot K_{vco} / N_{channel}$.

From the foregoing analysis and simulation results, the frequency synthesizer's charge pump current can be used to control its bandwidth based on the deviation of the double-integral of *e(t)*. For example, if the bandwidth of the frequency synthesizer is 20% lower, the double integral of the error signal *e(t)* will increase beyond its nominal value that corresponds to the nominal bandwidth. If the frequency synthesizer charge pump current is increased by 20%, the bandwidth of the frequency synthesizer should remain almost constant. On the other hand, if the bandwidth is 20% higher, the charge pump current needs to be reduced by the same percentage to keep the bandwidth almost constant. Hence the result of the linear fitting of the double-integral of *e(t)* by M_{slope} and A_{const} can be directly used to control the frequency synthesizer charge pump current as shown in Figure 3-5. The output of the 6-bit ADC is integrated using a 16-bit digital integrator. The value of A_{nom}, representing the nominal frequency synthesizer bandwidth, is subtracted from the output of the digital integrator. The result is then linearly fitted using M_{slope} and A_{const} to produce a 6-bit charge pump code which controls the frequency synthesizer's bandwidth.

3.3 Mitigating the Calibration System Error Sources

3.3.1 Cancellation of Charge Pump Mismatch Errors

The calibration system described in Figure 3-5 has two main error sources which will be described in details and addressed here:

1. The statistical mismatch between the up-down current mismatch values of the integrator-path charge pump and the up-down current mismatch values of the calibration charge pump.

2. The variation of the calibration capacitor, C_{cal}, used to integrate the error signal *e(t)*.

The integrator-path, the calibration-path and the LPF-path charge pumps of the frequency synthesizer are implemented as unary-weighted 6-bit charge pump current DACs. The calibration charge pump which is part of the calibration system shown in Figure 3-5 is used to convert the digital pulses at the PFD output into a voltage on a capacitor, replicating the operation of the charge pumps in the frequency synthesizer. As a consequence, the calibration charge pump has to be very well matched to the frequency synthesizer's charge pumps. In the physical design of the frequency synthesizer, the calibration charge pump is also designed as a unary-weighted 6-bit charge pump DAC whose units are embedded within the integrator-path charge pump DAC units to guarantee accurate matching between both charge pumps. The calibration charge pump needs to be matched to the integrator-path charge pump rather than the LPF-path charge pump. By construction, upon applying a frequency step to the frequency synthesizer, the integrator-path charge pump generates the transient voltage response as well as the steady state of the frequency synthesizer on the loop filter C_z shown in Figure 2-10. On the other hand, the LPF-path charge pump participates in the transient response; however, its steady-state voltage settles to zero at the end of the transient response.

Figure 3-9 shows the implementation of the frequency synthesizer's integrator-path and the calibration-path charge pumps. The reference frequency at the PFD input is 52MHz. Hence, the charge pumps need to operate at this frequency. The charge pumps are designed to have an LSB current of 0.5μA. Due to the small LSB size of the charge pumps and its relatively high speed of operation, current sources M_{PCS} and M_{NCS} are differentially drain switched and their currents are steered to node *M* when no charge is delivered to the loop filter capacitor, C_{int} (C_z in Figure 2-10). To reduce the charge sharing between nodes *P* and *N* when the charge pump turns on, amplifier, *OP1,* is used to force node *M* to the loop filter voltage. Amplifier, *OP2,* maintains the matching between M_{PCS} and M_{NCS} using a replica biasing circuit.

Amplifier, *OP2,* senses the loop filter voltage and regulates the gate of current source M_{PCS} accordingly to keep an accurate match between the M_{PCS} and M_{NCS} current sources.

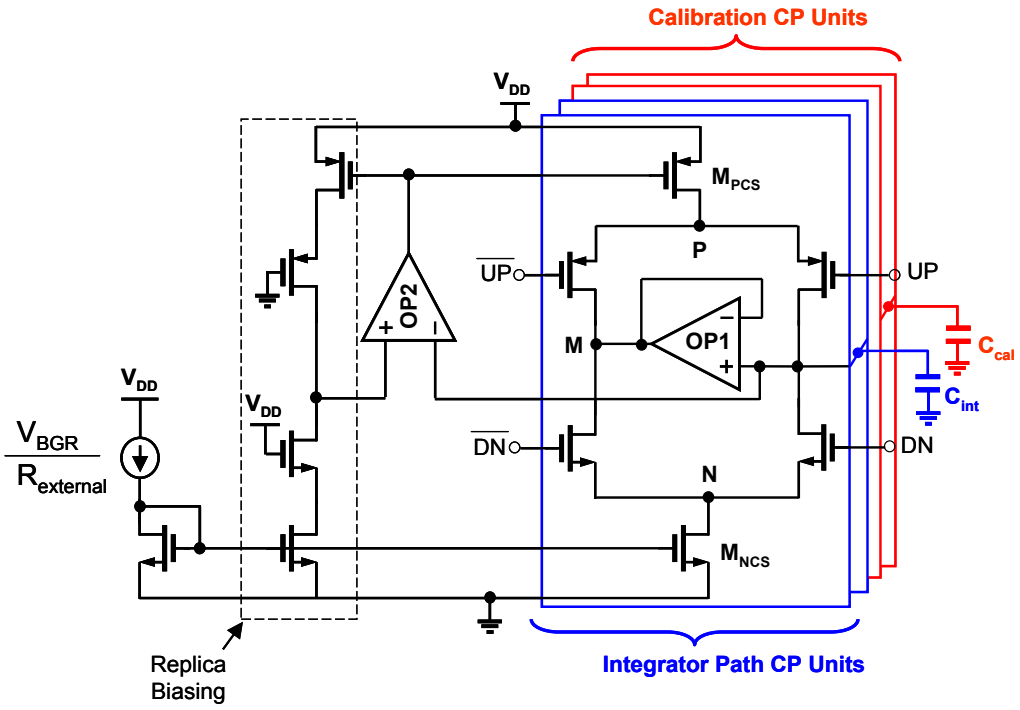


Figure 3-9 Simplified circuit schematic of the integrator path and the calibration charge pumps. *OP1* is used once for all integrator path charge pump units and once for all calibration charge pump units.

The reference current to the charge pump is generated using a band-gap reference voltage and an external resistor to deliver a relatively constant charge to the integrating and calibration capacitors, C_{int} and C_{cal} respectively, in the presence of process, voltage and temperature variations. Since matching between the integrator path and the calibration charge pump DACs is critical, they are laid out as interleaved units.

Although the circuit techniques described above are used to minimize the mismatch between the calibration-path charge pump and the integrator-path charge pump, it is necessary to ensure that any residual mismatch does not affect the calibration system. To that end, a digital mismatch detection and cancellation system was developed to cancel any residual mismatch. The system is based on the observation that when the frequency synthesizer is locked, the net

charge delivered from the integrator-path charge pump to the loop filter is zero and hence the net charge delivered to the calibration capacitor, C_{cal}, at the output of the calibration charge pump should also be zero (before applying any frequency step to the input of the frequency synthesizer). If there is a mismatch between the calibration and the integrator-path charge pumps, the net charge delivered to the calibration capacitor by the calibration charge pump is non-zero. This property can be used to detect the mismatch between the charge pumps. Prior to applying a frequency step to the frequency synthesizer, the calibration charge pump is allowed to integrate any *mismatch charge* on the calibration capacitor for a predetermined amount of time equal to the time T_{int}, used for integrating the error signal when applying a frequency step. A voltage will develop on the calibration capacitor which is proportional to the amount of the mismatch. This voltage can be digitized by the ADC and integrated using the same digital circuitry depicted in Figure 3-5.

Figure 3-10 shows the digital detection and cancellation system for the mismatch between the integrator-path and the calibration-path charge pumps. I_B is the charge pump current of both the integrator-path and the calibration-path charge pumps. The parameter β is the mismatch between the up-down current mismatch, ε, of the integrator-path charge pump and the up-down current mismatch of the calibration-path charge pump.

The mismatch detection and cancellation system uses two phases; the first phase is the mismatch detection phase and takes place while the frequency synthesizer is locked to $f_{channel} - \Delta f$ for a period of T_{int}. In the presence of the mismatch, β, between the up-down current mismatch of the integrator-path charge pump and the up-down current mismatch of the calibration-path charge pump, the net charge delivered to the calibration capacitor is non-zero while the frequency synthesizer is locked to $f_{channel} - \Delta f$. The value of the charge delivered to the calibration capacitor is directly proportional to the value of mismatch between both charge pumps. The voltage developed as a result of this charge is digitized and accumulated in the digital domain for a predetermined amount of time, T_{int}.

Mismatch cancellation takes place in a second phase where a step Δf is applied to the frequency synthesizer and the double integral of the error signal, $e(t)$, is generated. The digitally integrated value of the mismatch obtained in the first phase is subtracted from the double integral of the error signal, $e(t)$, before the linear fitting operations described in Figure 3-5 are performed and shown again in Figure 3-10 for convenience.

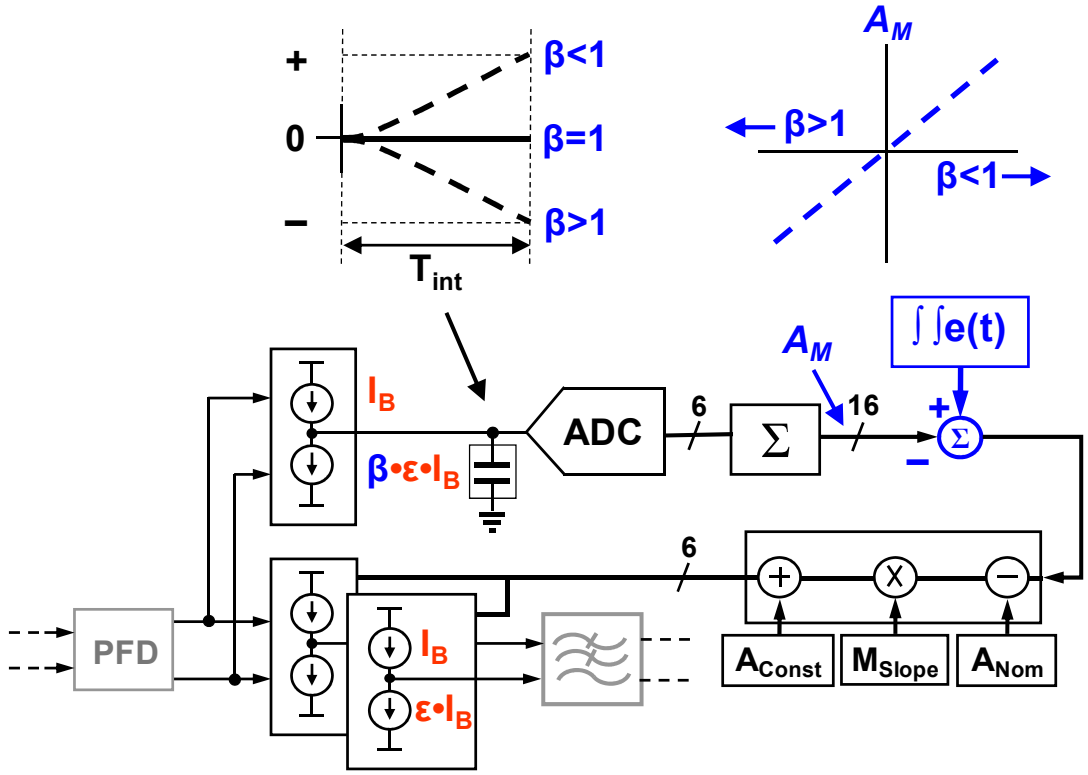


Figure 3-10 Digital detection and cancellation system for the mismatch between the integrator-path and the calibration-path charge pumps

The operation of the digital mismatch detection and cancellation system is as follows:

1. *Mismatch detection phase :*

    a. This phase takes place when the frequency synthesiser is locked to $f_{channel} - \Delta f$, *and* before applying a frequency step to its input. If the up-down current mismatch of the integrator charge pump and the up-down current mismatch of the calibration charge pump are identical ($\beta = 1$ in Figure 3-10), the voltage on the calibration capacitor is zero on average in a period of T_{int}

which is equivalent to the period used to integrate the error signal after the frequency step, Δf, is applied. The output of the digital integrator, A_m, will be zero in this case.

b. If the up-down current mismatch of the integrator charge pump and the up-down current mismatch of the calibration charge pump are different, for example $\beta < 1$, the voltage on the calibration capacitor will increase in proportion to the value of the mismatch and the output of the digital integrator, A_m, will increase linearly.

c. On the other hand, if $\beta > 1$, the voltage on the calibration capacitor will decrease and A_m will decrease linearly.

2. *Mismatch cancellation phase :*

   A_m, which now represents the digital value the mismatch, is then subtracted from the digital double integral of the error signal, $e(t)$, after a frequency step, Δf, is applied and before performing the linear fitting operation of the double integral of the error signal $e(t)$ as shown in Figure 3-10.

Figure 3-11 shows the results of a time-domain simulation for the digital integral of the mismatch value given by A_m in the *mismatch detection phase* shown in Figure 3-10 versus a ±3% mismatch between the up-down current mismatches in the integrator-path and calibration-path charge pumps (equivalent to β in Figure 3-10) while the frequency synthesizer is locked to $f_{channel} - \Delta f$. In addition, the simulation includes up to ±0.1ns delay mismatch between the up and down signals of the integrator-path and calibration-path charge pumps. The integration period, T_{int}, is set to 48μs for the data shown in the figure.

The digital integral of the mismatch has an almost linear relationship with the percentage of mismatch between the up-down current mismatch of the calibration charge pump and those of the integrator charge pump. In the figure, if the mismatch, β, is greater than 1, a negative

voltage with respect to the common-mode voltage will develop on the integrating capacitor, as shown in Figure 3-10**,** and the deviation of the double integral of the error signal will decrease. On the other hand, if the mismatch, β, is less than 1, a positive voltage with respect to the common-mode voltage will develop on the integrating capacitor and the deviation of the double integral of the error signal will increase.

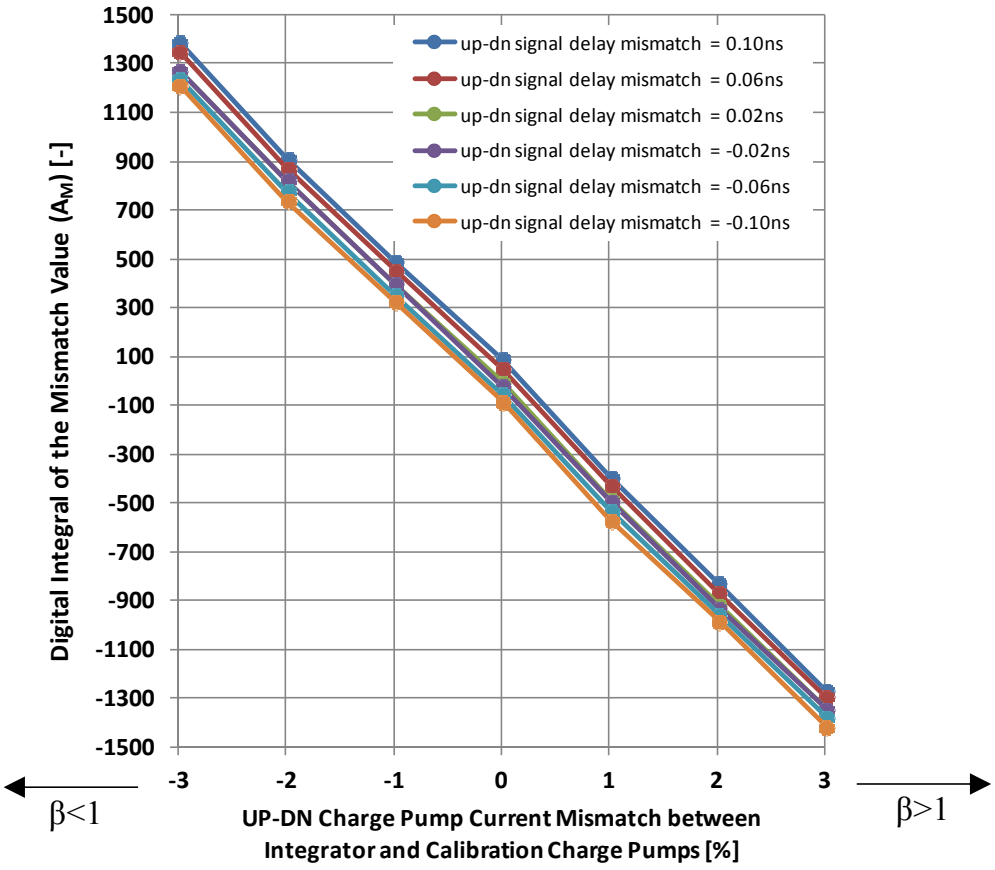


Figure 3-11 Digital integral of the mismatch value given by A_m in the presence of up-down current and delay mismatches between the integrator-path and calibration-path charge pumps while the frequency synthesizer is locked to $f_{channel} - \Delta f$

Figure 3-12 shows the time-domain simulation results of the frequency synthesizer of Figure 3-5 for the deviation of the double integral of the error signal $e(t)$ in the presence of ±3% mismatch between the up-down current mismatches in the integrator-path and calibration-path charge pumps under nominal conditions after a frequency step of Δf is applied. In addition, the simulation includes up to ±0.1ns delay mismatch between the up and down

signals of the integrator-path charge pump and those of the calibration-path charge pump. It should be noted that the integrator path and the calibration path charge pumps are laid out as interleaved units and every care was taken to match the layout of these units including the routing of the up and down signals from the PFD.

The deviation of the double integral of the error signal, *e(t)*, from the nominal value should *ideally* remain constant in the presence of up-down current mismatches as well as up-down delay mismatches. This is important in order to be able to detect the variations in the frequency synthesizer bandwidth using the calibration system of Figure 3-5**,** even in the presence of such mismatches. As shown in Figure 3-12, the deviation of the double integral of the error signal, *e(t)*, has an almost linear relationship with the percentage of mismatch between the up and down signals of the calibration charge pump and those of the integrator charge pump. This relationship can be explained using the same analysis for the relationship shown in Figure 3-11**.**

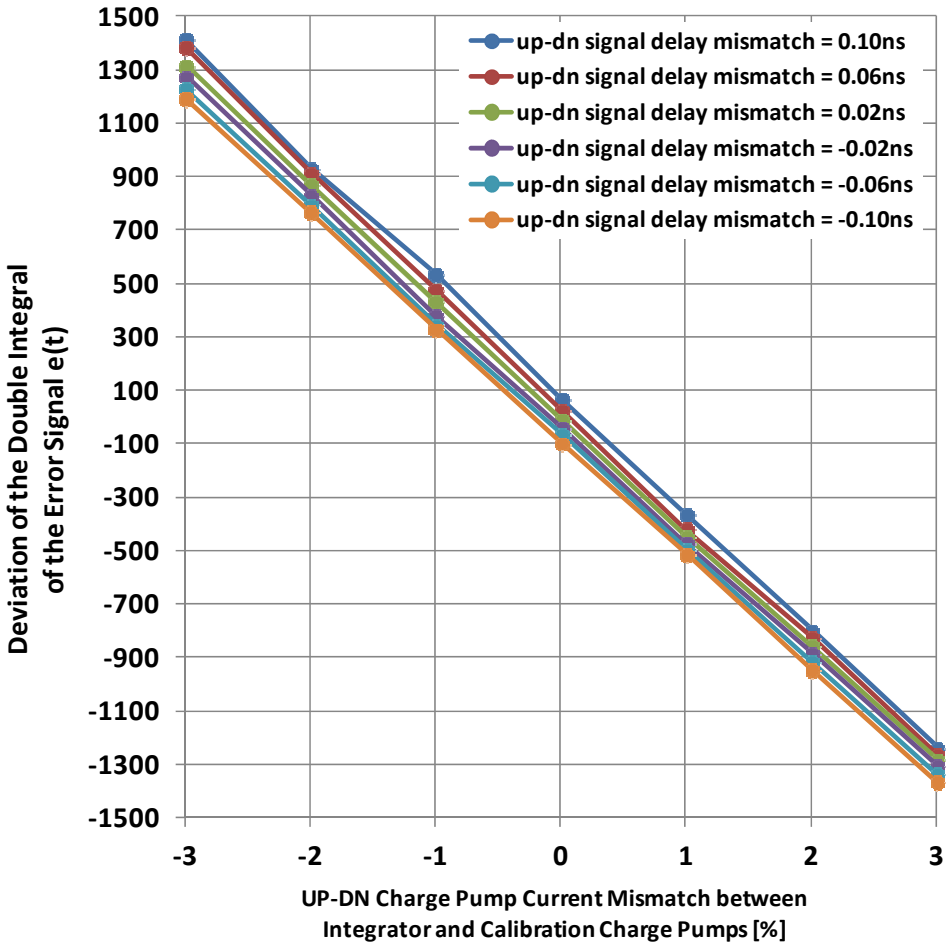


Figure 3-12 Deviation of the double integral of the error signal *e(t)* in the presence of up-down current and delay mismatches between the integrator-path and calibration-path charge pumps after a frequency step of *Δf* has been applied to the frequency synthesizer

Figure 3-13 shows the error in the deviation of the double integral of the error signal *e(t)* in the presence of up-down current and delay mismatches between the integrator-path and calibration-path charge pumps *after mismatch cancellation*.

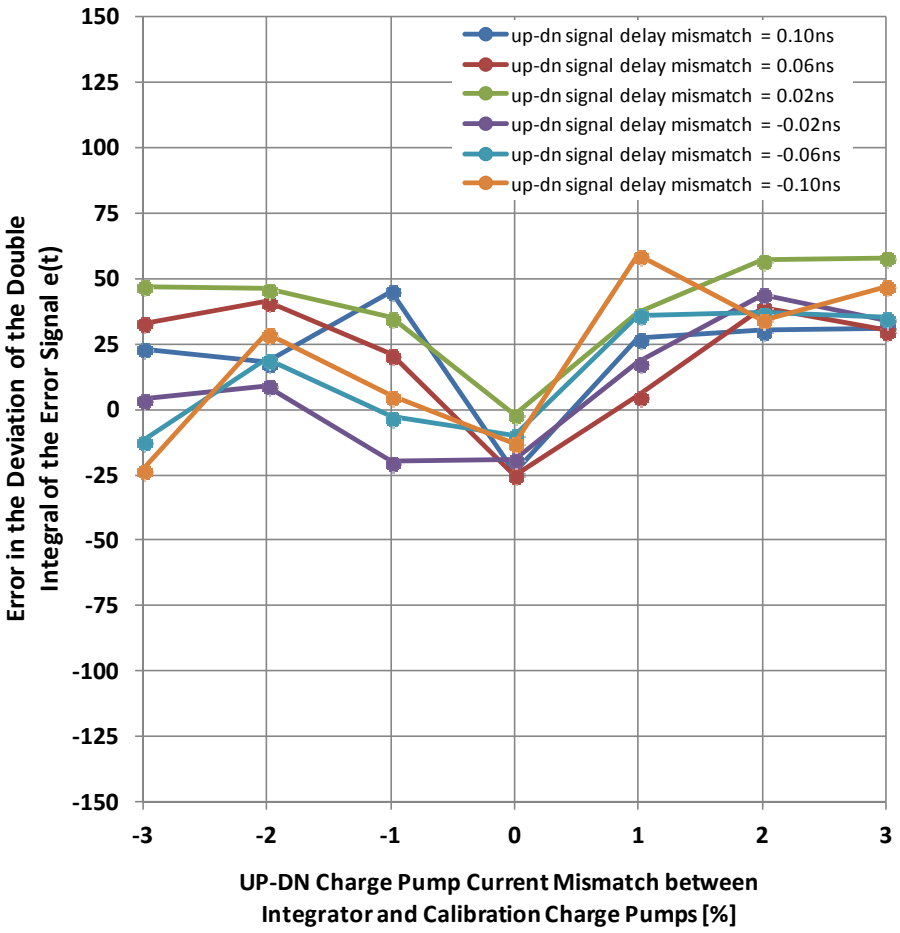


Figure 3-13 Error in the deviation of the double integral of the error signal *e(t)* in the presence of up-down current and delay mismatches between the integrator-path and calibration-path charge pumps after mismatch cancellation

The error shown in Figure 3-13 should ideally be zero. However, the accuracy of the mismatch cancellation is limited by the ADC resolution. This double integral error is approximately 100 LSBs in total and, as will be shown in Figure 4-2, this translates to a maximum error of 1 LSB in the calibrated charge pump DAC code which controls the calibrated bandwidth of the frequency synthesizer.

3.3.2 Calibration Capacitor Variation Detection and Calibration

The second source of inaccuracy in the calibration system of Figure 3-5 is the variation of the calibration capacitor, C_{cal}, which is used to integrate the output of the calibration charge

pump. The value of the calibration capacitor, C_{cal}, can change by as much as ±20% in the presence of process variations (±10% variation is the practical variation in most advanced fabrication processes). This requires the capacitor to be calibrated in order to achieve an accurate calibration of the frequency synthesizer bandwidth.

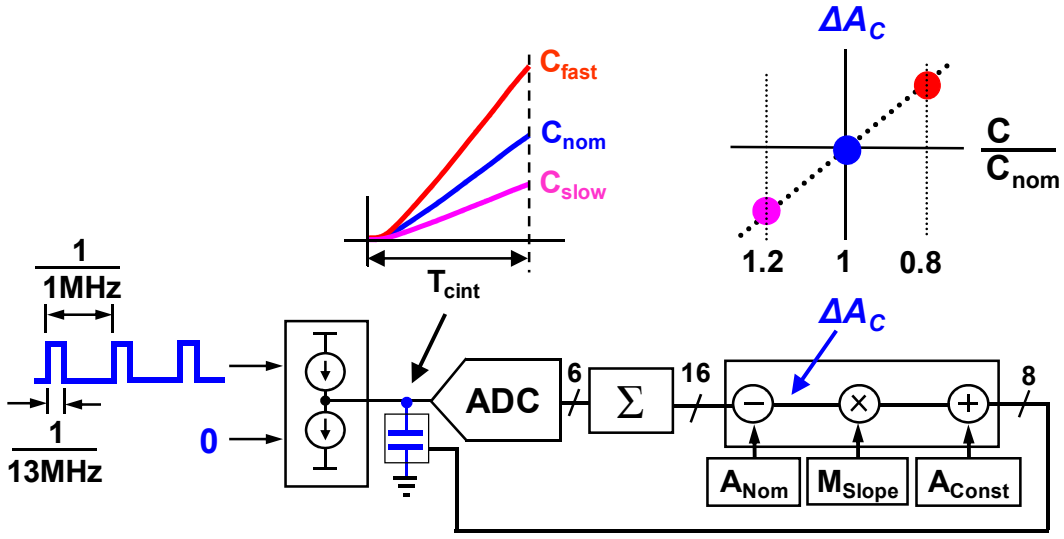


Figure 3-14 System to calibrate C_{cal} due to process variations

Figure 3-14 shows a system to calibrate C_{cal} due to process variations. The calibration capacitor does not exhibit significant variations with temperature. The capacitor is calibrated using the calibration charge pump itself. A multiplexer is used to reuse the inputs to the calibration charge pump where a 1MHz digital clock is enabled with a duty cycle of 1/13 as shown in the figure. The digital clock is an input to the up current source of the calibration charge pump whereas the down current source is switched off. The digital clock will enable the up current source when it has a "high" level and will disable it when it has a "low" level. The calibration capacitor will integrate the charge delivered by the charge pump and will generate a voltage ramp whose slope is a function of the absolute value of the charge pump current and the calibration capacitor value. The absolute value of the charge pump current is made very stable by using a bias current whose value is equal to V_{bg}/R_{ext}, where V_{bg} is the on-chip band gap reference voltage and R_{ext} is an accurate external bias resistor. The external bias resistor is not required specifically for calibration; it is also part of the charge pump circuit

shown in Figure 3-9. The voltage reference of the ADC used in the calibration system is also set by V_{bg}, hence the variation of the on-chip band-gap reference voltage does not affect the capacitor calibration accuracy. The initial tolerance of the external resistor, R_{ext}, can be very low in the order of 0.1%. Hence, the calibration charge pump current is very accurate and does not affect the calibration accuracy. As a result, the only parameter which affects the voltage ramp integrated on the calibration capacitor is the capacitor value which needs to be calibrated.

The calibration is performed by enabling the digital clock to the calibration charge pump for a predetermined amount of time, T_{cint}. During this time, the voltage ramp on the capacitor is digitized using the ADC and the output of the ADC is digitally integrated after initially being reset. If the value of the capacitor is nominal (denoted by C_{nom} in Figure 3-14), the slope of the voltage ramp on the capacitor will have a nominal value and the digital integrator value, integrating this voltage ramp for the amount of time, T_{cint}, will also have a nominal value. Due to process variations, a process corner can be either fast or slow. The capacitor value will be too low in the fast process corner (denoted by C_{fast} in Figure 3-14 where $C_{fast}/C_{nom}=0.8$), and hence, the voltage ramp speed will be faster than nominal. As a result, the integrator will integrate more than the nominal value and will have a higher final value relative to the nominal value. On the other hand, for a slow process corner, the capacitor value will be too high (denoted by C_{slow} in Figure 3-14 where $C_{slow}/C_{nom}=1.2$), the voltage ramp speed will slower than nominal and, as a result, the integrator will integrate less than the nominal value and will have a lower final value relative to the nominal value.

The difference, ΔA_c, between the digital integrator values at different process corners relative to the nominal integrator value, A_{nom}, which corresponds to the nominal calibration capacitor value, is a measure of the deviation of the capacitor value from its nominal value. This property can be used to calibrate the capacitor to its nominal value. The calibration capacitor is made of 256 unary capacitor units. The calibration system, shown in Figure 3-14,

determines the correct number of capacitor units, based on the value of ΔA_c, after performing a linear fitting operation. To assess the principle of operation of the calibration system, the relationship between the percentage variation in the calibration capacitor value and ΔA_c needs to be examined.

Figure 3-15 shows the time-domain simulation results for the deviation of the ADC integrator from the nominal value (ΔA_c) versus the percentage of adjustment required for the calibration capacitor. The simulation was performed by sweeping the calibration capacitor units around its nominal value by ±25% and observing the value of ΔA_c. For example, if ΔA_c = -900, the percentage adjustment required for the calibration capacitor is -20% which means that a calibration capacitor value of +25% higher than its nominal value caused ΔA_c to be equal to -900.

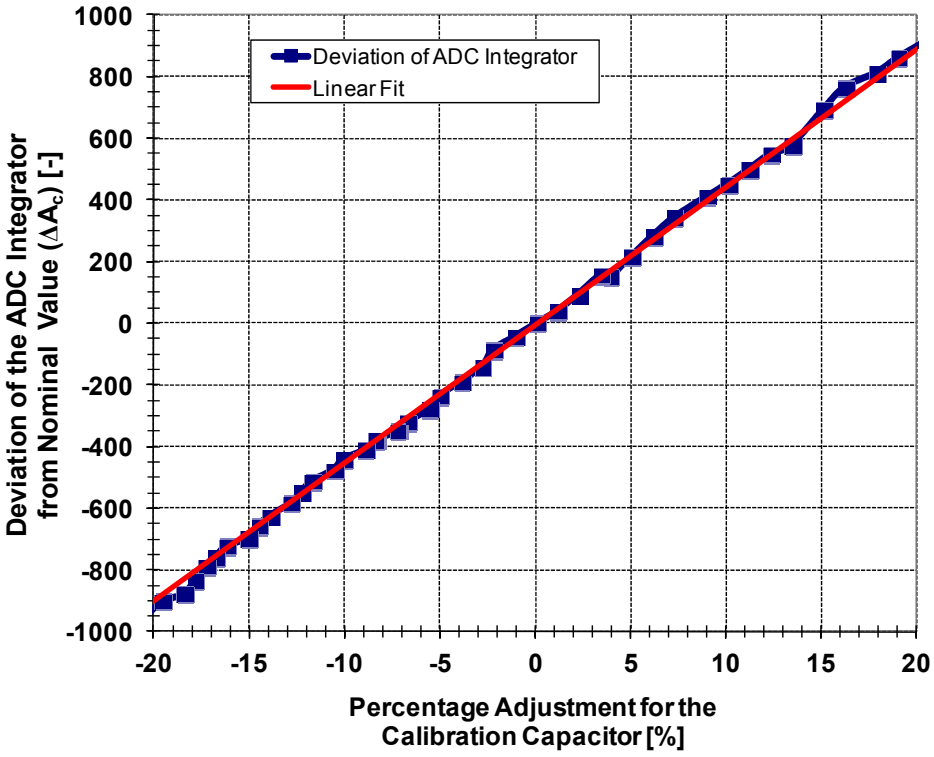


Figure 3-15 Deviation of the ADC integrator from nominal value (ΔA_c) versus the percentage of adjustment required for the calibration capacitor

The relationship in Figure 3-15 is an almost linear relationship and can be used to calibrate C_{cal} using the parameters A_{nom}, M_{slope} and A_{const} in Figure 3-14. The deviation from a perfectly linear relationship when a relatively high positive percentage of adjustment is needed for C_{cal}, is attributed to the quantized nature of the digital system used for calibration where the ADC resolution is 6 bits and the width of the ADC accumulator is 16 bits. Furthermore, when the capacitor value is small relative to its nominal value at the fast process corner, a fast voltage ramp is developed on the capacitor. In a given integration time, T_{cint}, in Figure 3-14, the voltage level at the end of the voltage ramp can be close to the reference voltage of the ADC. This can introduce a non-linearity in the characteristics shown in Figure 3-15. In particular, when the capacitor is smallest, i.e. when the percentage adjustment needed is close to +20%

An 8-bit code is generated at the output of the calibration system, as shown in Figure 3-14, to calibrate C_{cal} which is made up of 256 unary units. The calibration system can handle variations up to ±20%, which is almost twice as much for practical capacitor variations.

Figure 3-16 shows the error in the value of the calibration capacitor, C_{cal}, relative to the nominal capacitor value using the fitting parameters in Figure 3-15. A calibration error of less than ±1.2% is achieved when linear fitting is used. This error can be reduced, if needed, to less than ±0.5% if a look-up table method is used for calibration whereby for each ΔA_c an 8-bit calibration capacitor code is directly used without the need for any mathematical operation that could potentially introduce errors. It is worth noting that the arithmetic unit used to subtract A_{nom}, multiply by M_{slope}, add A_{const} and generate calibration codes, is shared among all calibration procedures shown in Figure 3-5, Figure 3-10 and Figure 3-14.

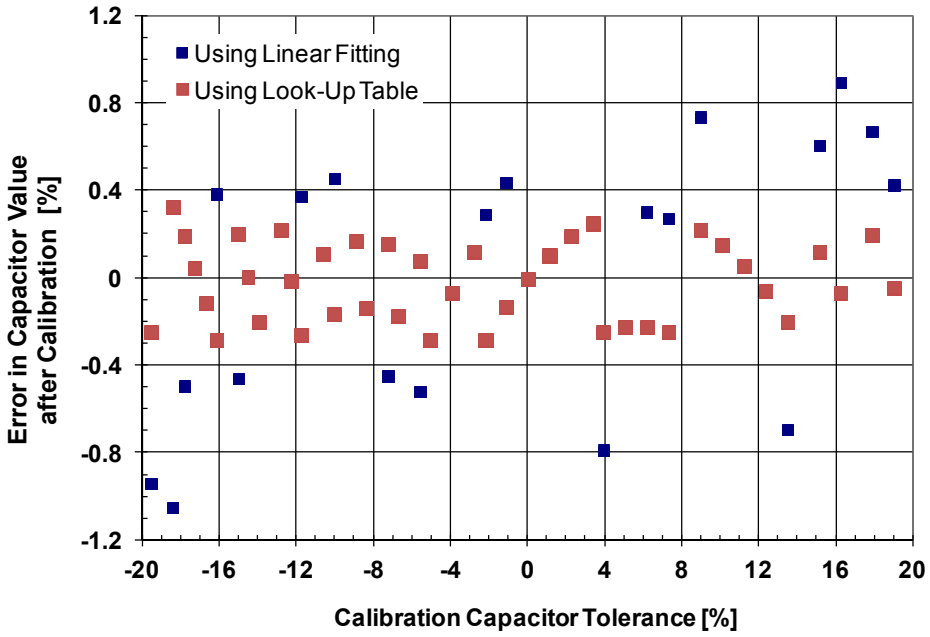


Figure 3-16 Error in the value of the calibration capacitor C_{cal} when the fitting parameters of Figure 3-15 are used

From the foregoing simulations in Figure 3-6 and Figure 3-7 and subsequent discussions, it was noted that it would be possible to only consider variations in K_{vco} and f_{chan} and ignore the variations in R and C for the purpose of calibrating the frequency synthesizer bandwidth. However, the system described in Figure 3-14 already calibrates capacitor C_{cal}, which is of the same type as the loop filter capacitors; C_z, C_{1p}, C_{2pl} and C_{2pi} shown in Figure 2-10. These capacitors have different values from C_{cal} but are made from the same unit capacitor. The calibration code generated by the capacitor calibration system of Figure 3-14 is scaled to provide a calibration code for each of the capacitors of the loop filter[2]. Hence, the only component which is not calibrated in the frequency synthesizer is the resistor component of the loop filter, R_p. However, it will be shown in Figure 4-11 and Figure 4-13 of Chapter 4 that the variation of this resistor does not significantly affect the MER of the transmitter.

[2] It was only possible to vary and calibrate capacitor C_z in this work. C_z has the largest value among other loop filter capacitors by a factor of 18.5 and was varied by up to ±40% to assess the capacitor calibration system. Hence, it is not expected that the absence of varying and calibrating the rest of the loop filter capacitors would affect the MER of the transmitter.

3.4 Conclusions

This chapter surveyed various schemes for the calibration of the closed-loop bandwidth of a frequency synthesizer. Based on the survey, the need for a simple, power-efficient and digitally-assisted scheme was identified. The chapter presented a calibration system which is based on a mathematical property of second-order control systems. This mathematical property is that the double integral of the error signal between the input and the output of a closed loop transfer function is a linear function of the reciprocal of the system's open-loop gain and an almost linear function of the reciprocal of its unity-gain frequency. This property was applied to a frequency synthesizer whose closed-loop transfer function is at least a third order system. The calibration system uses an area-efficient scheme and does not require significant additional circuitry, apart from calibration charge pump DAC units embedded within the layout of the frequency synthesizer's integration path charge pump units, a calibration capacitor and a simple digital accumulate-multiply-and-add unit to complete the calibration system. The ADC used in the calibration is part of the receiver chain and is re-used during the transmitter calibration. Hence, overall, there is negligible die area penalty.

The calibration system eliminates its own measurement errors using simple digital techniques. It eliminates the mismatch between the calibration charge pump and the integrator-path charge pump, as well as eliminates the variation in the calibration capacitor, by reusing the same digital circuitry for the whole calibration system.

Chapter 4

RF Transmitter Simulation Results and Measurements

4.1 Simulation Results for the RF Modulator and its Calibration System

Figure 4-1 shows a timeline for the sequence of events during the calibration process of the frequency synthesizer. The calibration is preceded by a VCO calibration which is a standard calibration in integrated frequency synthesizers. After resetting the calibration capacitor and the digital integrators, the frequency synthesizer's bandwidth calibration process starts with calibrating the calibration capacitor, C_{cal}, as well as the integrator path capacitor, C_z. Once finished, the frequency synthesizer is locked at a frequency difference of Δf below the desired channel, $f_{channel}$. The calibration capacitor is reset while the frequency synthesizer locks to this frequency.

After the frequency synthesizer is locked, the mismatch detection algorithm of the calibration charge pump is activated for a period of 48µs. The calibration capacitor is reset once more for a period of 6µs and a frequency step is applied to the frequency synthesizer by simply removing the equivalent value of Δf from the frequency synthesizer divider control word. During the transient response of the frequency synthesizer, its bandwidth is estimated. The value of the ADC integrator is used during this phase as well as the value obtained during the calibration charge pump mismatch detection phase to generate a charge pump DAC control word which is used to calibrate the bandwidth of the frequency synthesizer. The overall calibration time is 158µs in addition to the 120µs required to settle the frequency synthesizer to $f_{channel}$-Δf. This settling time is required by the frequency synthesizer to settle to a specific channel, even in the absence of any calibration. A period of 30µs is included in the calibration time due to the need to resettle the frequency synthesizer to $f_{channel}$ after bandwidth calibration.

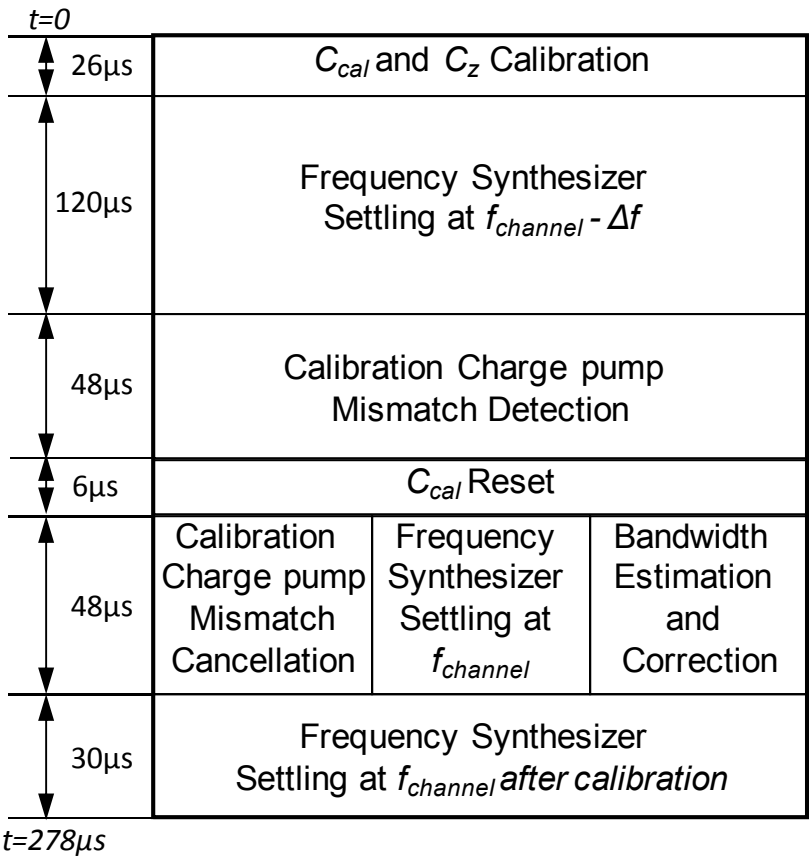


Figure 4-1 Sequence of calibration system events for the frequency synthesizer

Figure 4-2 shows the time-domain simulation results for the overall calibration system. The calibration is performed on the frequency synthesizer under the following conditions: ±20% R and C variation, ±6% V_{bg} variation, ±25% K_{vco} variation, 2% up-down current mismatch for the integration-path and calibration charge pumps, ±4% mismatch between the up-down current mismatch of the calibration charge pump and the integrator path charge pump, ±2% mismatch in the timing of the up and down pulses from the PFD to each of the calibration and the integrator-path charge pumps. For these simulations, the PLL closed loop bandwidth was 520 kHz and the frequency step applied for calibration was 500 kHz.

From the foregoing analysis, the calibration system controls both the integrator-path and the LPF-path charge pump currents of the frequency synthesizer based on the deviation of the double integral of the error signal, after performing mismatch cancellation. As shown in

Figure 4-2, as the deviation increases, indicating a decrease in bandwidth, the charge pump codes are increased accordingly to increase the bandwidth to the nominal value. As the deviation decreases indicating an increase in bandwidth, the calibration decreases the charge pump codes to decrease the bandwidth.

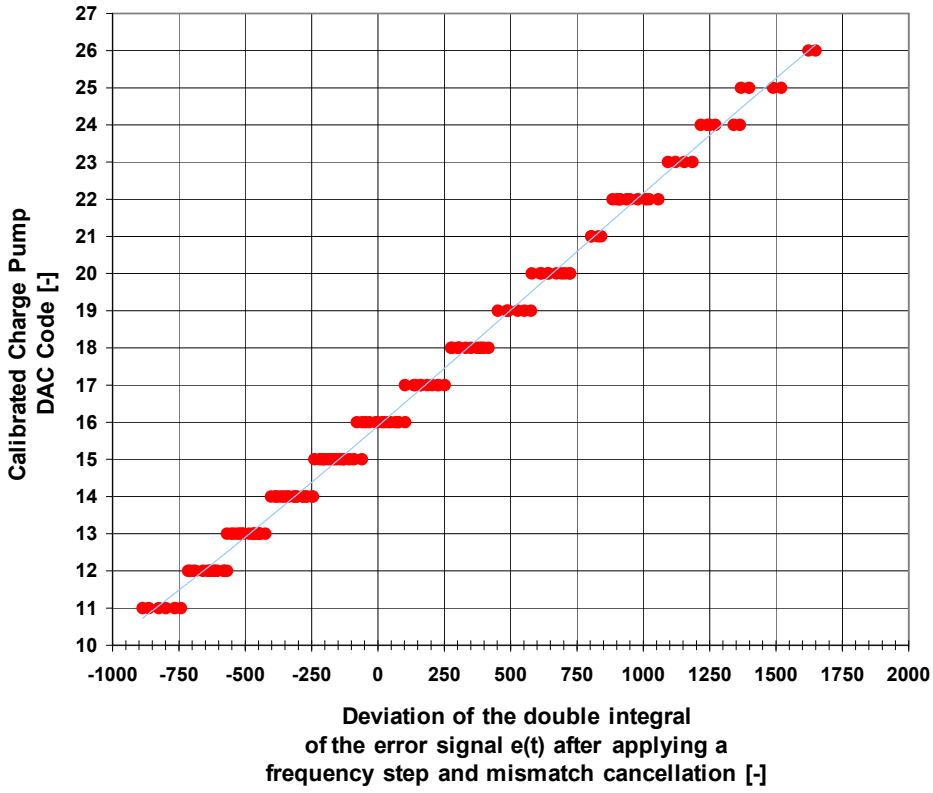


Figure 4-2 Integrator path and LPF path charge pump DAC codes generated by the calibration system

Figure 4-3 shows the time-domain simulation results for the effect of the calibration on the RMS phase error of a 2Mbps GMSK signal transmitted using the frequency synthesizer. The figure shows the un-calibrated versus the calibrated RMS phase error for different simulation conditions based on the same parametric variations used in Figure 4-2. The un-calibrated RMS phase error can be as high as 16° under some parametric variation conditions exceeding the target of 10˚ set by the receiver's demodulator requirements. The calibrated RMS phase error is less than 7° under the same conditions.

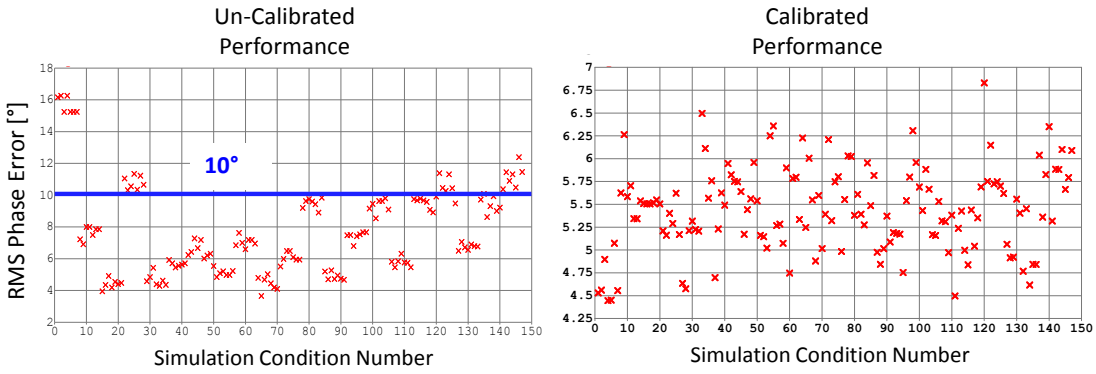


Figure 4-3 Un-calibrated vs. Calibrated RMS phase error performance of the transmitter for a 2Mbps GMSK signal

4.2 Measurement Results for the RF Modulator and its Calibration System

Figure 4-4 to Figure 4-8 show the measurement results, demonstrating the functionality of the calibration system on the IC. Figure 4-4 shows a time-domain capture of the on-chip ADC output while applying a frequency step to the PLL input in the presence of ±50% variation in the PLL bandwidth in steps of 10%. To assess the functionality of the calibration system, the PLL bandwidth is varied using the LPF-path charge pump while keeping the integrating-path charge pump constant. The PLL bandwidth used in subsequent discussions refers to the closed-loop bandwidth of the PLL. The ADC output represents the digitized value of the analogue integral of *e(t)* developed on the calibration capacitor. If the PLL bandwidth is 50% higher than the nominal bandwidth, the voltage ramp caused by *e(t)* on the calibration capacitor is fastest in the given observation period at the ADC output. If the bandwidth is 50% less, the ramp at the ADC output is slowest during the same period and, if the bandwidth is close to its nominal value, then the ramp at the ADC output is somewhere in between. A digital accumulator at the ADC output accumulates the digitized integral of the error signal, *e(t)*, shown by the digital ramps in Figure 4-4 for each case.

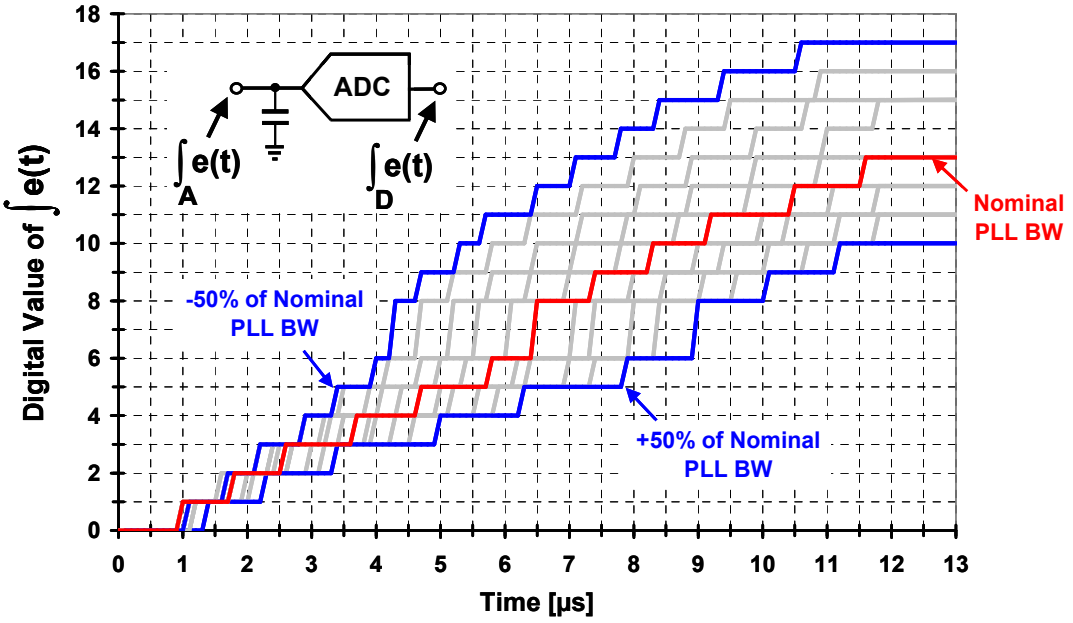


Figure 4-4 Time capture of the ADC output while applying a frequency step to the PLL input in the presence of ±50% variation in the PLL bandwidth in steps of 10%

A 13µs digital integration window was used for the initial silicon revision. However, subsequent revisions used the timing diagram of Figure 4-1. Figure 4-5 shows the value of ΔA versus the normalized inverse of the PLL bandwidth. ΔA represents the digital integral of the error signal after subtracting a nominal value corresponding to the nominal PLL bandwidth and subtracting the mismatch cancellation value. In the figure, if the PLL bandwidth is lower than the nominal PLL bandwidth, the value of ΔA is high relative to zero (where zero corresponds to the nominal PLL bandwidth) and vice versa, if the bandwidth is higher than the nominal PLL bandwidth. The relationship between the value of ΔA and the normalized inverse of the PLL bandwidth can be approximated by a linear relationship.

To assess the performance of the mismatch cancellation system, an approximate ±4% mismatch between the calibration and the integrating-path charge pumps, is introduced by adjusting the bias current of the calibration charge pump using a separate biasing branch in the circuit shown in Figure 3-9. The value of ΔA is observed in each case and the relationship between ΔA and the normalized inverse of the PLL bandwidth is used to determine the error

introduced in the PLL bandwidth as a result of the mismatch. It is estimated that the ±4% mismatch introduced causes approximately 2% error in the PLL bandwidth estimation after the mismatch has been cancelled from the value of ΔA. This is a small error and does not affect the charge pump DAC codes generated by the calibration system.

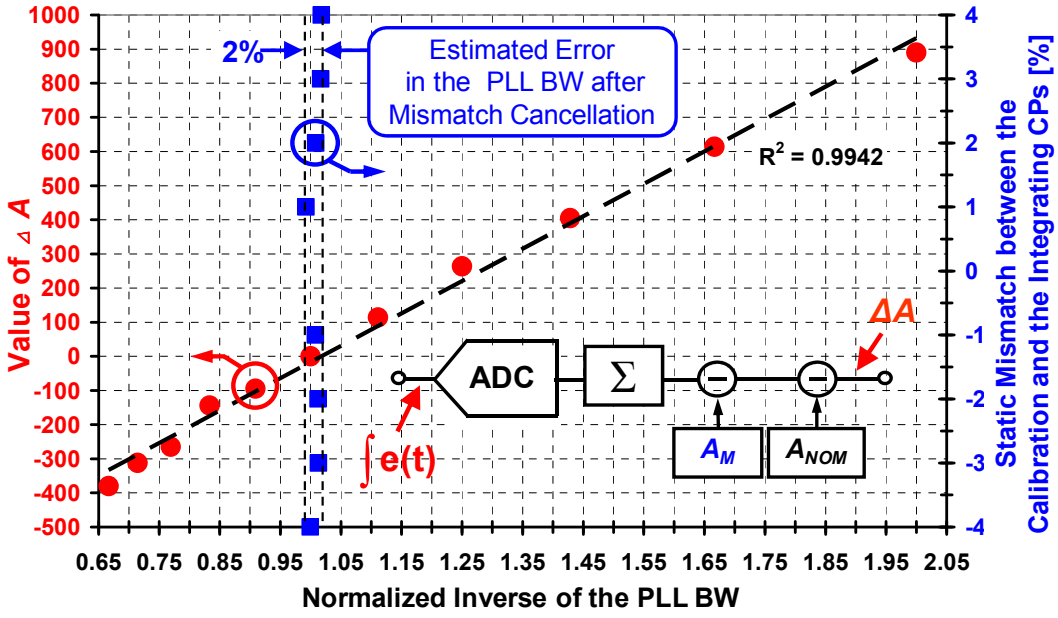


Figure 4-5 Linearity of the calibration signal and the effect of mismatch between the calibration and the integrating-path charge pumps on the accuracy of the calibration.

Figure 4-6 and Figure 4-7 show the calibrated performance of the RF transmitter in the presence of ±50% variation in the PLL bandwidth in steps of 10% at 3dBm output power at 2.48GHz RF carrier. For 2Mb/s GMSK signals (with BT = 0.5) the un-calibrated RMS phase error can be as high as 35 degrees whereas it stays below 8.4 degrees after calibration, which is equivalent to an MER of 32dB. The desired system target, accounting for all calibration errors, is 10˚ as required by the receiver's demodulator. For MSK signals complying with the IEEE802.15.4 standard, the calibrated MER stays above 34.5 dB, which is equivalent to 2% RMS EVM. The desired system target, accounting for all calibration errors, is 23dB as required by the receiver's demodulator.

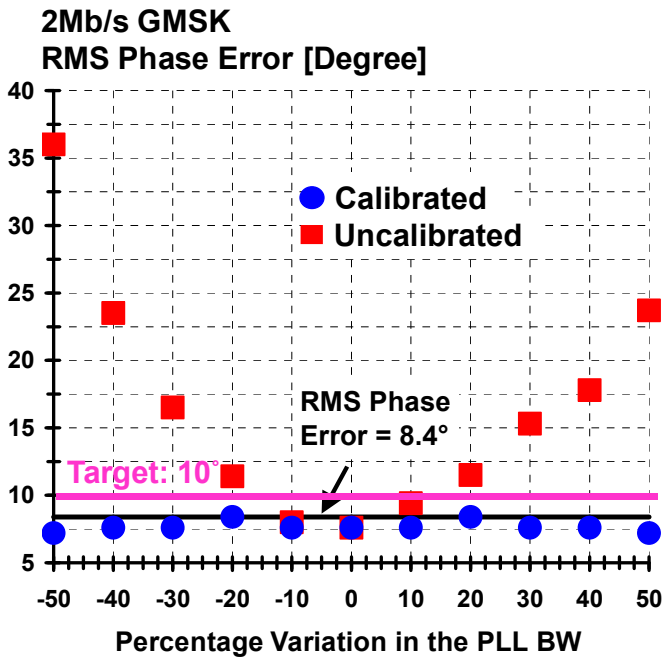


Figure 4-6 The calibrated performance of the RF transmitter's RMS phase error in the presence of ±50% variation in the PLL bandwidth at 3dBm for a 2Mb/s GMSK signal.

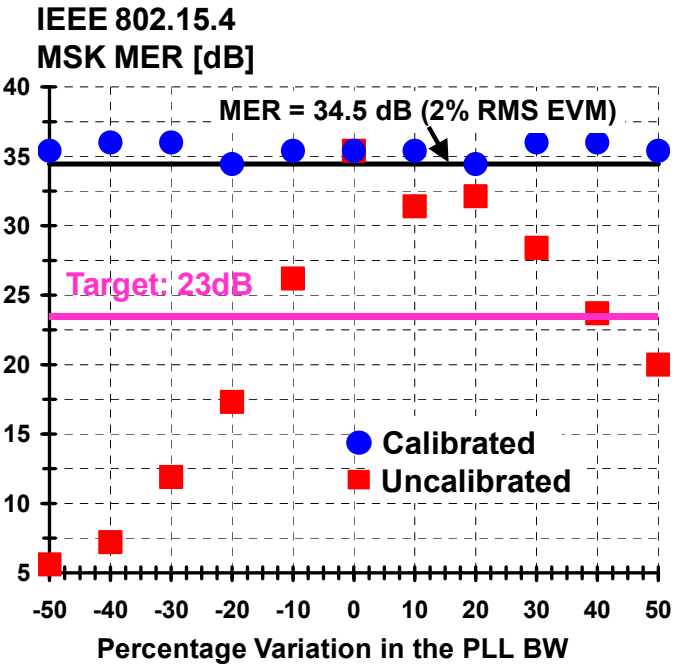


Figure 4-7 The calibrated performance of the RF transmitter's MER in the presence of ±50% variation in the PLL bandwidth at 3dBm for an IEEE802.15.4 signal

Figure 4-8 shows the RF transmitter's calibrated spectra at 3dBm output power at 2.48GHz RF carrier in the presence of ±50% variation in the PLL bandwidth. Both 2Mbps GMSK and IEEE 802.15.4 MSK signals spectra comfortably meet the FCC mask, which is the most stringent at 3.5MHz offset from the RF carrier at 2.48GHz. With 100% transmit duty cycle, the RF spectra are within the FCC mask with approximately 12dB margin. In addition, all spurious components at the output of the PLL are below 50dBc for GMSK and IEEE 802.15.4 MSK signals.

Figure 4-9 shows the un-calibrated and the calibrated eye diagrams for an IEEE802.15.4 MSK signal in the presence of a -50% deviation from the PLL nominal bandwidth. It can be seen that the un-calibrated eye diagram is almost completely closed and cannot be demodulated by the receiver.

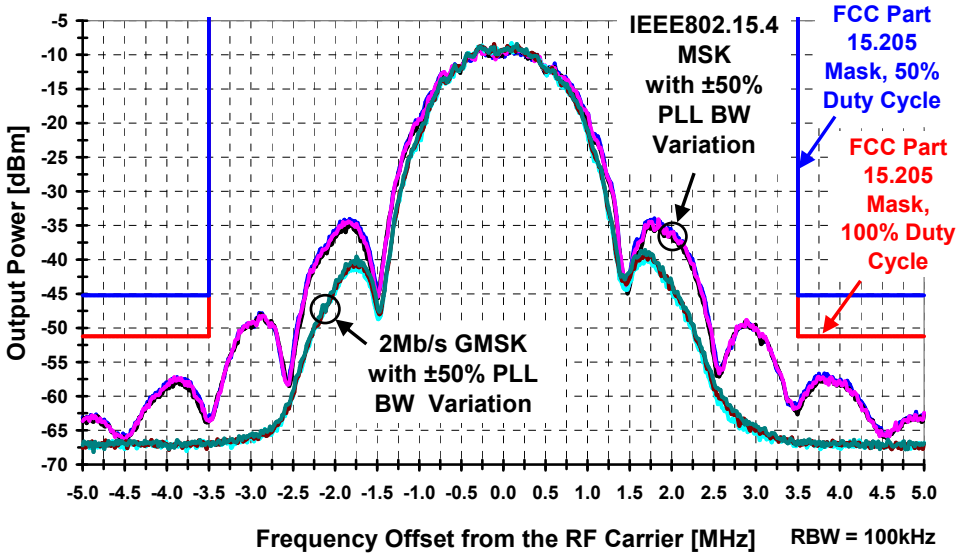


Figure 4-8 The calibrated performance of the RF transmitter's spectra in the presence of ±50% variation in the PLL bandwidth at 3dBm for an IEEE802.15.4 signal and a 2Mb/s GMSK signal

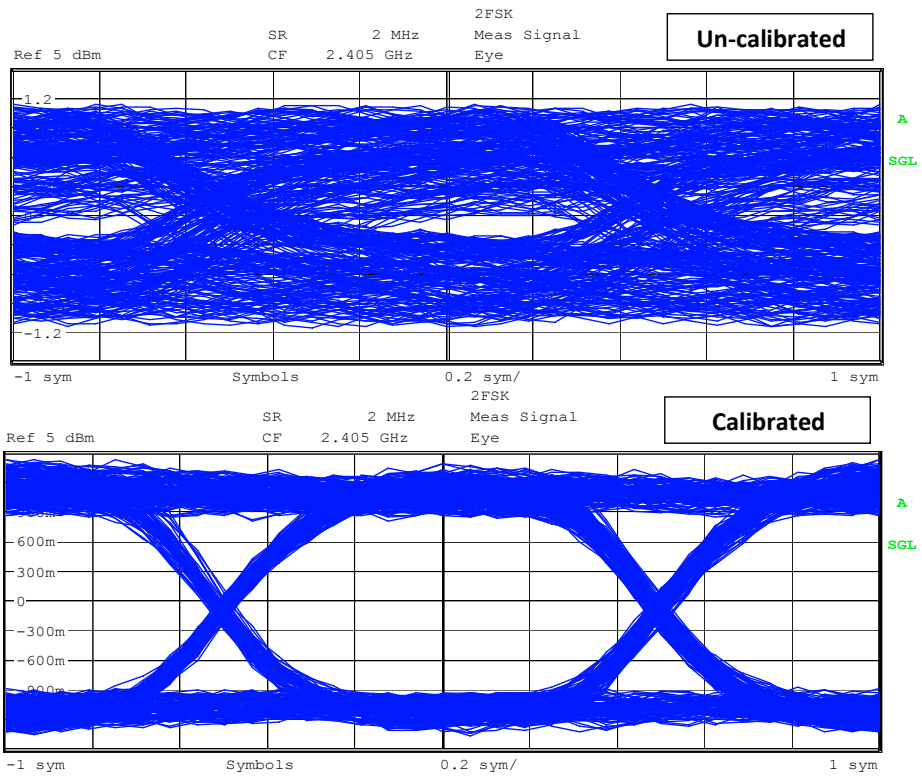


Figure 4-9 Measured un-calibrated and calibrated eye diagram for an IEEE802.15.4 modulated signal in the presence of a -50% deviation in the PLL nominal bandwidth

Figure 4-10 to Figure 4-15 show measurement results for a sample of devices to assess the transmitter performance as well as the calibration system performance in the presence of:

1. Mismatch between the integrating path charge pump and the calibration path charge pump. This is captured by measuring eight different devices
2. Variation in the channel frequency, $f_{channel}$, and K_{vco}. Although the 2.4GHz ISM band spans the frequency range from 2.4GHz to 2.4835GHz, the frequency range used for the measurements was extended from 2.335GHz to 2.60GHz to capture the effect of variation in K_{vco} beyond the nominal variation in the desired frequency range.
3. ±40% variation in the calibration capacitor C_{cal} as well as C_z . The variation considered in the measurements is well beyond the typically simulated process variation of ±20%. An extended range of variation was used to assess the capability of the calibration algorithm beyond its target range.

4. -35% to +20% variation in R_p. This variation was limited by the programmability available on the chip for R_p. Nevertheless, it also goes beyond the typical variation of ±20% in the resistance value over process. It should be noted that this variation is not calibrated, as discussed in previous sections.

Figure 4-10 shows the minimum, maximum and mean calibration error for the calibration capacitor C_{cal}. In this measurement, the calibration capacitor is varied by ±40%. The calibration error is maintained to less than ±5% using the calibration system shown in Figure 3-14. Given the simulation results in Figure 3-16, it was expected that the calibration error would be around ±2%. An investigation into the root cause of this discrepancy between simulations and measurements revealed that errors were inadvertently introduced in the capacitor calibration system of Figure 3-14 in the presence of chip-to-chip mismatches since the nominal value, A_{nom}, corresponding to the nominal capacitor for each chip is different and not constant. The calibration system would perform better in the presence of a higher oversampling clock for the digital integration performed at the ADC output. This modification can be implemented in future work.

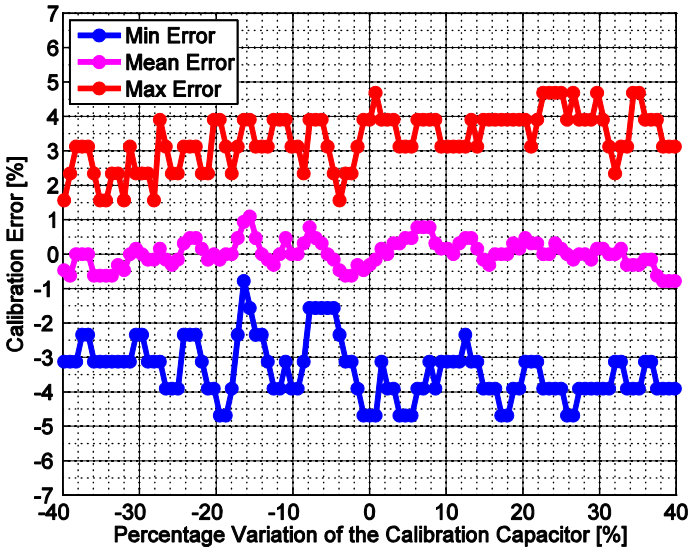


Figure 4-10 Minimum, Maximum and Mean C_{cal} calibration error versus variation in C_{cal} across 8 devices

Figure 4-11 shows the calibrated and un-calibrated *mean* transmitter MER across eight devices for the IEEE802.15.4 standard versus the transmit frequency using the calibration sequence illustrated in Figure 4-1. Figure 4-12 shows the calibrated and un-calibrated *minimum* transmitter MER across eight devices under the same conditions.

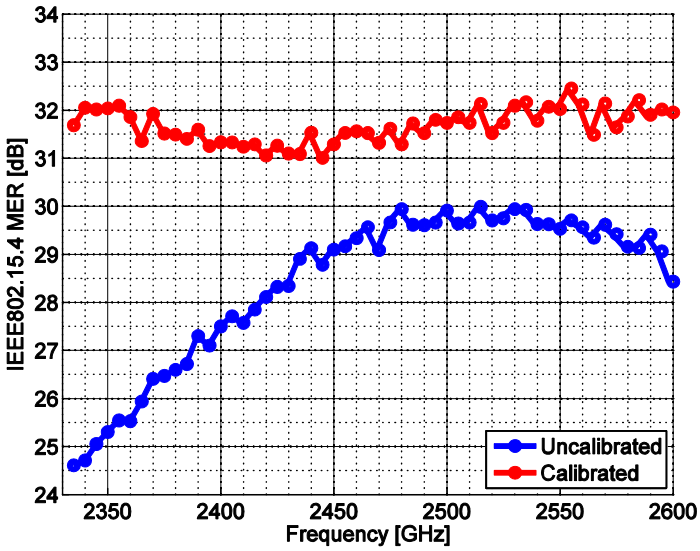


Figure 4-11 Comparison between calibrated and un-calibrated IEEE802.15.4 *mean* transmitter MER versus channel frequency in the 2.4GHz band, ±40% variation in C_z and -35% to +20% variation in R_p across 8 devices

At each frequency in both figures, the capacitor, C_z, is varied by ±40% and the resistor, R_p, is varied from -35% to +20%. The mean and the minimum of the MER measured across eight devices at each frequency for the calibrated and un-calibrated case is reported. It can be seen that the calibration system maintains the mean MER above 31dB and the minimum MER above 28.5dB across all frequencies. It is to be noted that there are 54 channel frequency points in each figure and for, each channel frequency, there are 54 cases of C_z and R_p variations.

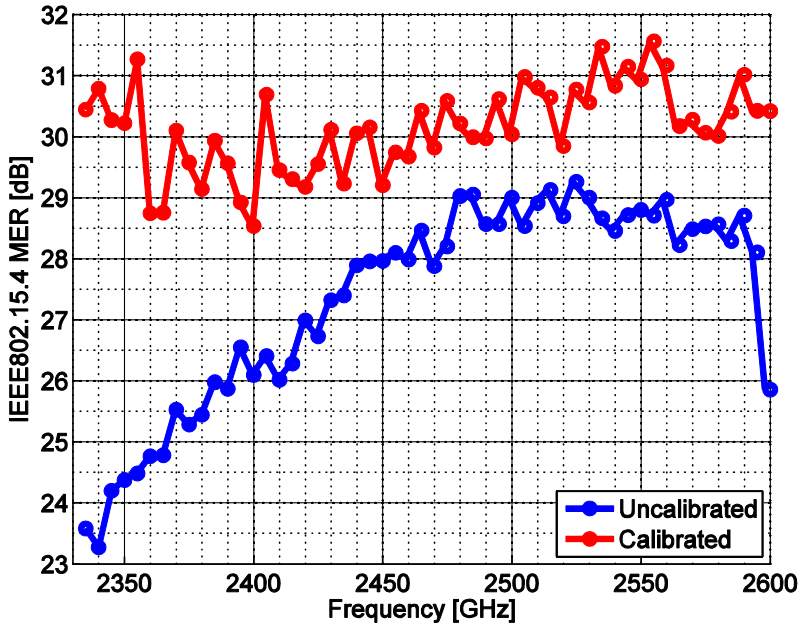


Figure 4-12 Comparison between calibrated and un-calibrated IEEE802.15.4 *minimum* transmitter MER versus channel frequency in the 2.4GHz band, ±40% variation in C_z and -35% to +20% variation in R_p across 8 devices

Figure 4-13 shows the calibrated and un-calibrated *mean* transmitter phase error across eight devices for a 2Mbps GMSK transmit signal versus the transmit frequency using the calibration sequence illustrated in Figure 4-1. Figure 4-14 shows the calibrated and un-calibrated *minimum* transmitter phase error across eight devices for a 2Mbps GMSK transmit signal under the same conditions. At each frequency in both figures, the capacitor C_z is varied by ±40% and the resistor R_p is varied from -35% to +20%. It can be seen that the calibration

system maintains the mean phase error below 8.5˚ and the maximum phase error below 9.5˚ across all frequencies.

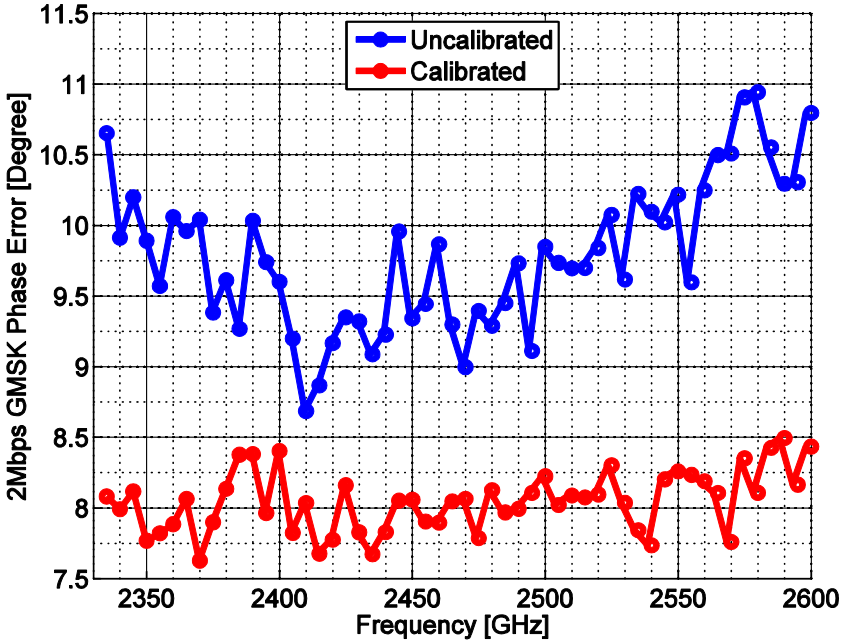


Figure 4-13 Comparison between calibrated and un-calibrated 2Mbps GMSK transmitter *mean* phase error versus channel frequency in the 2.4GHz band, ±40% variation in C_z and -35% to +20% variation in R_p across 8 devices

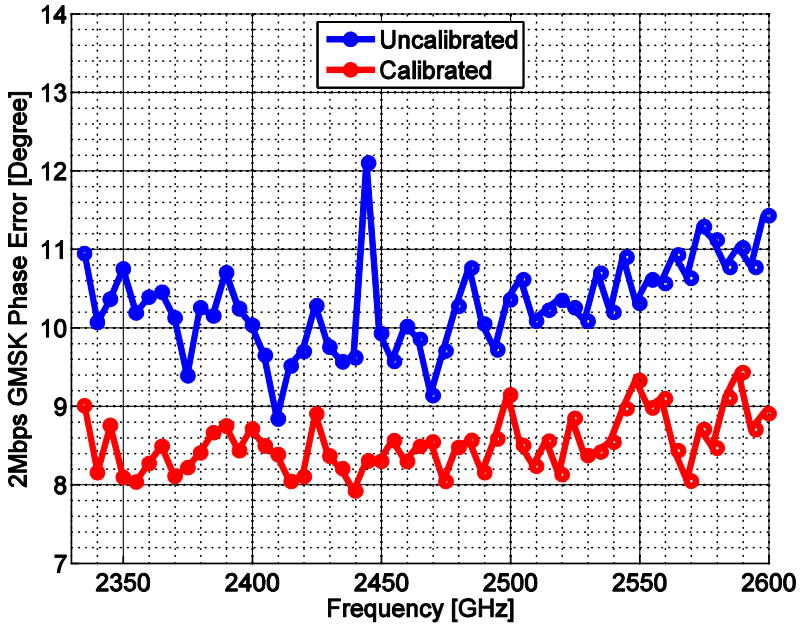


Figure 4-14 Comparison between calibrated and un-calibrated 2Mbps GMSK transmitter *maximum* phase error versus channel frequency in the 2.4GHz band, ±40% variation in C_z and -35% to +20% variation in R_p across 8 devices

To assess the performance of the calibration system in the presence of errors in the calibration capacitor, C_{cal}, the calibration capacitor was varied by ±3%, which is equivalent to the calibration error that would be achievable by the C_{cal} calibration system. Figure 4-15 shows the MER of an IEEE802.15.4 signal in the presence of ±3% error in the calibration of C_{cal}. It can be seen from the figure that the MER does not change significantly in the presence of C_{cal} calibration errors.

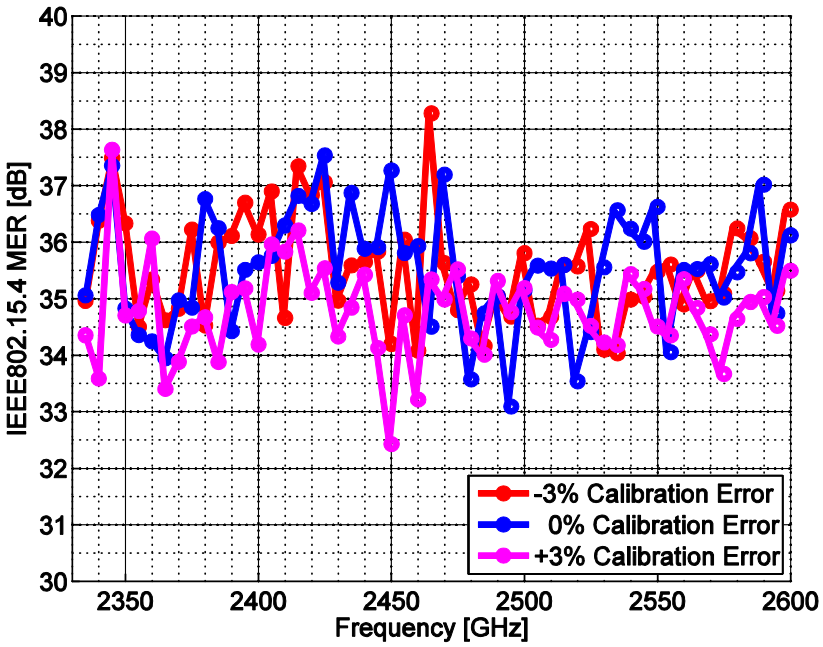


Figure 4-15 Comparison between calibrated and un-calibrated IEEE802.15.4 transmitter MER versus channel frequency in the 2.4GHz band, ±40% variation in C_z and -35% to +20% variation as well as ±3% calibration error in C_{cal}

In order to highlight the versatility of the transmitter in this work, Figure 4-16 shows the measured eye diagram for a 1Mbps GFSK modulated signal with a 2^9-pseudo-random binary sequence (PRBS9) data sequence. The eye diagram is measured according to the Bluetooth v1.2 compliance tests. The results of these measurements are summarized in Table 4-1. It can be seen that the transmitter is compliant with all the Bluetooth v1.2 specifications.

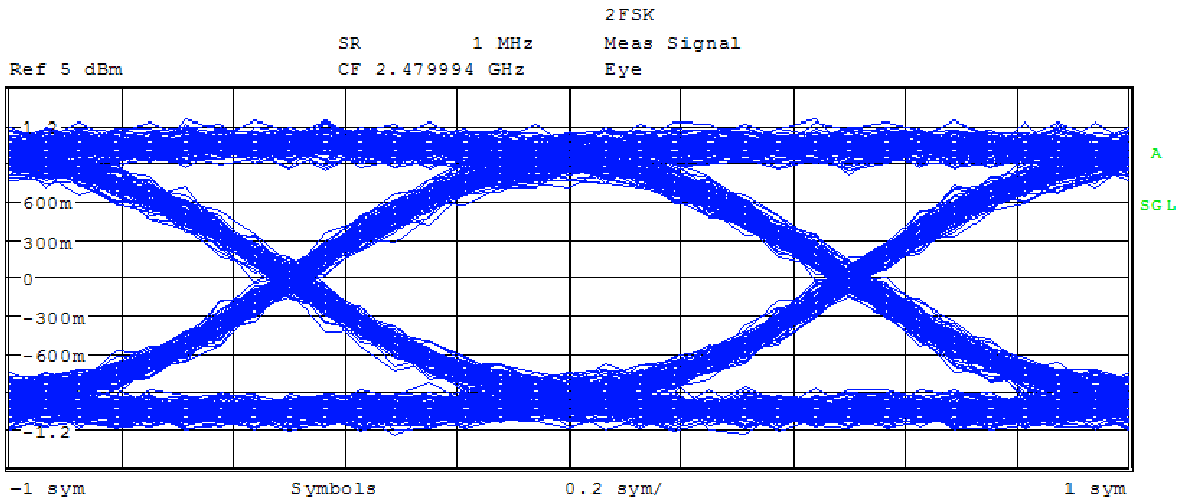


Figure 4-16 Measured eye diagram for 1Mbps GFSK modulated signal with PRBS9 (2^9 pseudo-random binary sequence) data sequence

Specification	Requirement	Measurement Result
Modulation Index	0.28 – 0.35	0.33
Zero Crossing error	$1/8^{th}$ of a symbol time	$1/16^{th}$ of a symbol
Average frequency deviation for 00001111 sequence	140kHz < Δf_{1avg} < 175kHz	166kHz
Minimum frequency deviation for 010101 sequence	Δf_{2max}> 115kHz	128kHz
20-dB Bandwidth	< 1.1MHz	0.9MHz
Adjacent Channel Power (1MHz frequency offset)	< -20dBm	-26dBm
Alternate Channel Power (2MHz frequency offset)	< -40dBm	-58.5dBm

Table 4-1 Measurements for the eye diagram of a 1Mbps GFSK modulated signal with PRBS9 data sequence showing compliance with Bluetooth v1.2 specifications

Figure 4-17 shows a die photo of the RF modulator within the RF transceiver IC. The RF modulator design occupies a total area of 1.1mm^2. From a 1.8V supply, the transmitter consumes a total of 18.2mA. The frequency synthesizer consumes a total of 6.6mA, the

digital pre-emphasis filter and the digital modulator circuitry consume 2.3mA and the power amplifier consumes 9.1mA.

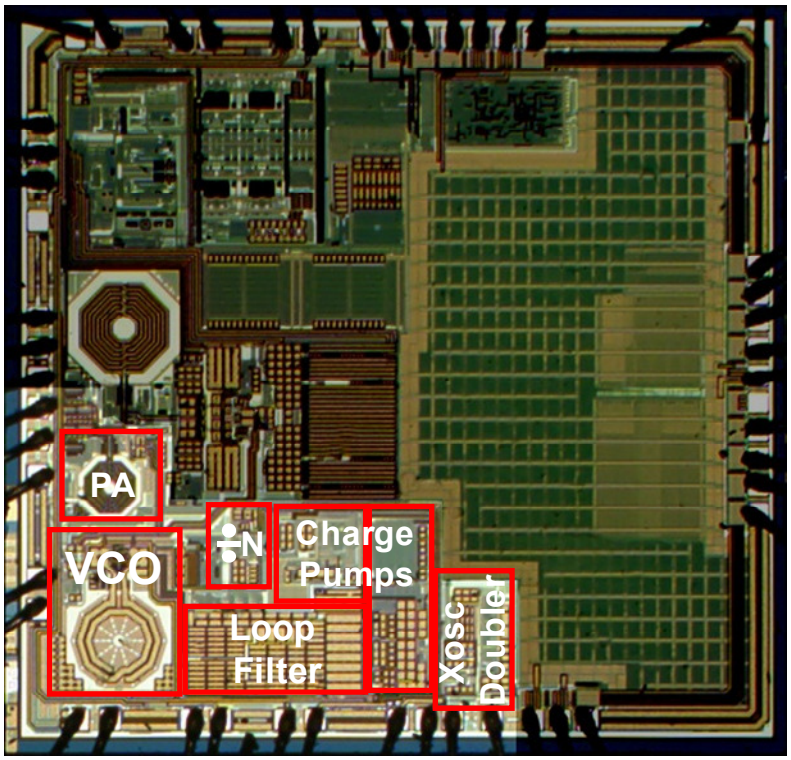


Figure 4-17 Die photo of the RF modulator

4.3 Comparison with the Prior Art

Table 4-2 shows a comparison of the RF transmitter performance with the prior art. Compared to Pamarati et al., [4], Menginer et al., [5], Ferriss et al. [6], and Akamine et al. [18], this work has the highest data-rate at 2Mb/s. In addition, the area of this work is almost one third of the area of the smallest transmitter implemented in the same process node while consuming 85% less power. At the ISM band edge of 3.5MHz offset, the phase noise of the RF transmitter is better than the referenced transmitters with the exception of the GSM transmitter in [18] which is not considered a low power transmitter. In addition, the calibration scheme of this work consumes one tenth of the energy of the closest prior art in [18].

	This Work (ISSCC'09)	JSSC'04, Pamarati [4]	JSSC'06, Menginer [5]	JSSC'08 Ferriss [6]	JSSC'08, Akamine [18]
Technology	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.13um CMOS	0.25um BiCMOS
Technique	Digital Pre-Emphasis with Calibration	Quantization noise suppression	Quantization noise suppression	Digital PFD	Conventional
Frequency Range	2.335-2.6GHz	2.402-2.48GHz	3.6GHz	2.24GHz	1.7-1.9GHz
Reference Frequency	52MHz	48MHz	50MHz	185.5MHz	26MHz
Analog PLL Bandwidth	520kHz	460kHz	1000kHz	142kHz	100kHz
Max. Data Rate	**2Mb/s**	**1Mb/s**	**1Mb/s**	**1Mb/s**	**0.271Mb/s**
GMSK *Max RMS Phase Error*	9.5°	Not Reported	Not Reported	Not Reported	2°
Calibrated Min MER for IEEE802.15.4	29dB	Not Applicable	Not Applicable	Not Applicable	Not Applicable
Calibration Scheme	**Observe Step Response at PFD**	**Not Applicable**	**Not Applicable**	**Not Applicable**	**Observe Step Response at RF**
Calibration Energy Consumption	**142nJ**	**Not Applicable**	**Not Applicable**	**Not Applicable**	**1350nJ**
Phase Noise at 3.5MHz	**-126dBc/Hz**	**-121dBc/Hz**	**-125dBc/Hz**	**-121dBc/Hz**	**-148dBc/Hz**
Reference Spurs	55dBc	65dBc	45dBc	N/R	> 60dBc
Area (excl. PA)	**1mm²**	**5.7mm²**	**2.7mm²**	**1.4mm²**	**3.8mm²**
Power Consumption	**16mW (excl. PA) 33mW (incl. 4dBm PA)**	**67mW**	**110mW**	**14mW**	**177mW (incl. 3dBm PA)**

Table 4-2 Comparison of the RF transmitter performance with the prior art

4.4 Conclusions

To summarize the key aspects of the RF transmitter of this work:

1. The work presented a calibration system for the bandwidth of a frequency synthesizer-based RF modulator which maintains stable modulation quality in terms of EVM and phase error for high data rate signals across process and temperature variations. The calibration system is based on a mathematical property of second-order control systems. This mathematical property is that the double integral of the error signal between the input and the output of a closed loop transfer function is a linear function of the reciprocal of the system's open-loop gain and an almost linear function of the reciprocal of its unity-gain frequency. This property has been applied to a frequency synthesizer whose closed-loop transfer function is at least a third order system. It was shown in Figure 3-7, that the relationship between the double integral of the error signal and the reciprocal of the unity-gain frequency of the frequency synthesizer design in this work can be approximated by a linear function which is sufficient for the accuracy requirements of the calibration system.

2. The calibration system in this work extracts the error signal and integrates it using an area-efficient and a low-power scheme. The calibration system does not require significant additional circuitry, apart from calibration charge pump DAC units embedded within the layout of the frequency synthesizer's integration path charge pump units. A calibration capacitor and a simple digital accumulate-multiply-and-add unit complete the calibration system. The ADC used in the calibration is part of the receiver chain and is reused during the transmitter calibration. Hence, overall, there is negligible die area penalty. The power consumption during calibration is around 500uA, which is less than 3% of the transmitter's overall active power consumption.

3. The calibration system eliminates its own measurement errors using simple digital techniques. It eliminates the mismatch between the calibration charge pump and the integrator-path charge pump, as well as eliminates the variation in the calibration capacitor, by reusing the same digital circuitry for the whole calibration system.

4. The transmitter design of this work has 60% smaller die area and 50% less power consumption when compared to that of Pamarti *et al.* [4] and Meninger *et al.* [5]. In addition, the calibration system consumes 500µA from 1.8V supply for a period of 158µs compared to 20mA from a 2.7Vsupply for 25µs in the work of Akamine *et al.* [18]. In terms of energy consumption, the calibration system of this work consumes 142nJ compared to 1350nJ in the work of Akamine *et al.*[18].

Chapter 5

RF Receiver Specifications and Architecture

5.1 Introduction

The performance of an RF receiver is determined by a set of parameters which capture how the receiver extracts a desired signal from a very hostile wireless environment. There is a wide range of signal powers involved in an RF system. The transmitter is required to deliver watts of signal power, yet several orders of magnitude of attenuation await this signal once it is launched from the RF transmitter antenna. By the time it reaches the destined RF receiver, the signal can be a mere femto-watts of RF power. The receiver is required to amplify this received signal despite being a very low power signal, sometimes very close to, or in certain systems below, the receiver's own noise floor. In addition, the receiver has to be able to cope with undesired signals located within or very close to the frequency band where the desired signal is located. These undesired signals, also known as blockers, can be several orders of magnitude higher than the desired signal itself. It is no wonder why receiver circuits are one of the most demanding electronic circuits. Figure 5-1 depicts a typical receiver circuit comprising a low noise amplifier (LNA), RF mixer, a local oscillator (LO), a LPF, a PGA and an ADC. The desired signal is located at $f_{RF,}$ with possible blockers located at f_{BLK1} and f_{BLK2}. The blocker located at f_{BLK1} could be an adjacent or alternate channel according to the RF system while f_{BLK2} could be located several channels away from the desired channel or at the edge of the frequency band of interest. The blocker levels can exceed 50dB and 70dB at f_{BLK1} and f_{BLK2} respectively relative to the desired signal. A typical RF receiver is equipped with an LO at f_{LO} which downconverts the RF signal located at f_{RF} to a base-band frequency at $f_{BB.}$ The fundamental challenge with RF receivers is that they should be able to down-convert an RF signal with several fW of power undisturbed in the presence of the very large blockers at f_{BLK1} and f_{BLK2}. The ability of a receiver to perform this function is characterized by two critical performance parameters, namely, its noise figure (NF) and linearity. The latter is

characterized by parameters such as the receiver's input-referred third-order intercept point (IIP3), input-referred 1-dB compression point (P1dB), input-referred second-order intercept point (IIP2) and LO phase noise. These parameters will be discussed in the following sections.

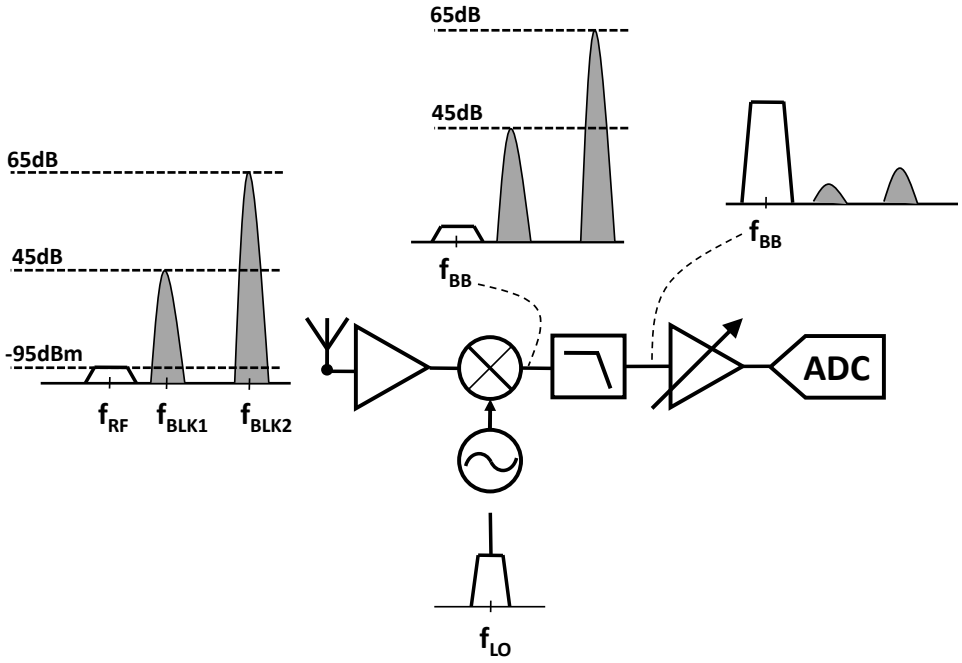


Figure 5-1 Fundamental challenges with an RF receiver

5.2 Linearity of RF Systems

5.2.1 Parameters Describing Non-Linear Systems

A large class of static non-linear time-invariant system with an output *y(t)* and an input *x(t)* can be approximated by the following polynomial equation:

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + ... + \alpha_n x^n(t) \quad \textbf{(5.1)}$$

Where, α_0, α_1, α_2, ..., α_n are constants that are independent of time in time-invariant systems. For a simple input, $x(t) = A\cos(\omega t)$, and assuming α_0=0 and n = 3 in equation (5.1), we have,

$$y(t) = \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4})\cos(\omega t) + \frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) \quad \textbf{(5.2)}$$

Equation (5.2) indicates that the output of a non-linear system will produce frequency components that are not present at the input by means of a mechanism called *harmonic distortion.* This, on its own, will cause the signal quality to degrade as it passes through the

non-linear system. Intuitively, an audible tone at a certain frequency at the input of a non-linear amplifier will sound differently when it is processed by the amplifier and passed through to the output. Hence, it is necessary to maintain the linearity of the components that constitute the front-end of the RF system for the same reason. There is more than one parameter to describe the deviation of circuits in an RF system from linear operation; these parameters are addressed in the following sub-sections.

5.2.1.1 Gain Compression

Gain compression is a manifestation of non-linearity. It occurs when a circuit does not increase its output amplitude linearly in response to its input amplitude. This will ultimately cause the output of the circuit to saturate. The magnitude of the *1-dB compression point,* A_{1dB}, captures this effect as shown in Figure 5-2. A_{1dB} is the point at which the small-signal voltage gain of the circuit in response to a single-tone signal at the input drops by 1dB from the ideal linear behaviour.

Analytically from equation (5.2), it can be deduced that the amplitude 1-dB compression point is given by [3]:

$$A_{1dB} = \sqrt{0.145 \cdot \left|\frac{\alpha_1}{\alpha_3}\right|} \qquad \textbf{(5.3)}$$

where, it was assumed that the small-signal gain factor α_3 is negative which is a reasonable assumption since the gain of practical circuits approaches zero, i.e. saturates, for sufficiently high input amplitude.

Figure 5-2 visually illustrates the concept of gain compression. From the figure, it can be seen that the actual small-signal voltage gain deviates from the linear behaviour at high input signal levels. A_{1dB} can be specified with respect to the input or the output; hence, we refer to the input 1-dB compression point and the output 1-dB compression point.

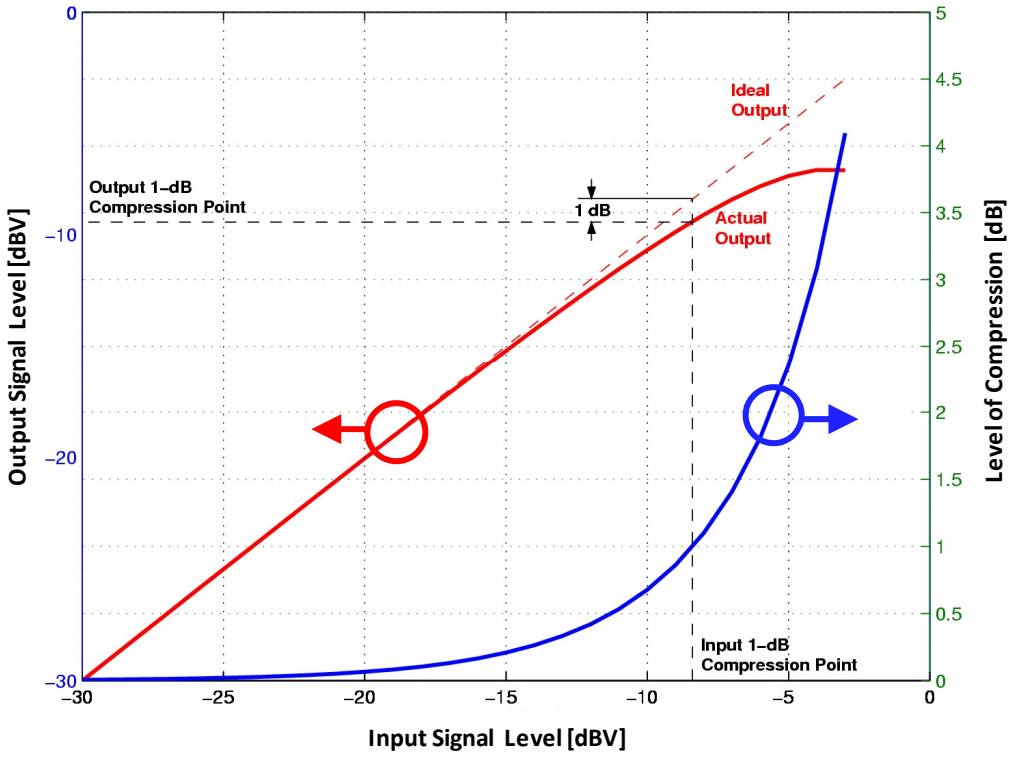


Figure 5-2 Gain compression and A_{1dB}

5.2.1.2 Desensitisation and Blocking

Desensitisation is a special case of gain compression; it measures how the receiver of an RF system will react to a desired signal of amplitude, A_1, in the presence of a strong interfering signal of amplitude, A_2. For this purpose, consider, as an input, the signal $x(t)=A_1 cost(\omega_1 t)+A_2 cost(\omega_2 t)$. Applying equation (5.1) with this input yields:

$$y(t)=\left[\alpha_1 A_1+\frac{3\alpha_3 A_1^{\,3}}{4}+\frac{3\alpha_3 A_1 A_2^{\,2}}{2}\right]\cos(\omega_1 t)+\ldots \qquad \textbf{(5.4)}$$

In practical receivers, the interfering signal level is much higher than the desired signal level, thus $A_2>>A_1$ and equation (5.4) can be re-written as:

$$y(t)\approx\left[\alpha_1+\frac{3\alpha_3 A_2^{\,2}}{2}\right]\cdot A_1\cdot\cos(\omega_1 t) \qquad \textbf{(5.5)}$$

As highlighted before, the factor α_3 is negative, and consequently, for very high interfering signal levels, the small-signal gain of the circuit approaches zero and the receiver cannot

receive the desired signal i.e. the desired signal is *blocked*. Thus, a *blocking signal* is an interfering signal that could severely desensitise the receiver, even if the gain with respect to the desired signal is non-zero.

5.2.1.3 Inter-Modulation Distortion

A receiver can be affected by strong signals that do not fall directly in the desired channel being received. Two interferers outside the bandwidth of the channel can cause inter-modulation distortion (IMD) products that fall directly in the channel. IMD can occur even if the circuit is operated well below its 1-dB compression point. Second order IMD, IM2, occurs if two tones, ω_1 and ω_2, result in the two tones $\omega_1 \pm \omega_2$ that fall within the channel bandwidth. Third order IMD, IM3, occurs if the tones, ω_1 and ω_2, result in tones at $2\omega_1 \pm \omega_2$ or $2\omega_2 \pm \omega_1$ that fall within the bandwidth. Typically, the difference component, $\omega_1 - \omega_2$, is the most critical component for the system and is likely to fall within the desired bandwidth, and the sum component, $\omega_1 + \omega_2$, is likely to be filtered by the system. Similarly, for the IM3 components, the difference components $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, are likely to fall in the desired signal band for the same reasons.

If the circuit operates in its linear region, which is defined as the region below its 1-dB compression point, the IM2 component will increase by 2dB per 1dB increase in the input signal amplitude and the IM3 component amplitude will increase by 3dB per 1 dB increase in the input signal amplitude [25].

To characterize the linearity of a receiver, a figure of merit called the intercept point, *IP*, is used, where the amplitude of the fundamental tone is increased at the receiver input and the fundamental output power is monitored, as well as the powers of the IM2 and the IM3 components. The extrapolated behaviour of the fundamental component and the IM2

components determines the IP2 or the second-order intercept point. The extrapolated behaviour of the fundamental component and the IM3 component determines the IP3 point or the third-order intercept point. Figure 5-3 shows the graphical representation of the intercept point. The values of $IP3_{IN}$ and $IP2_{IN}$ are the third- and second-order intercept points, respectively, referred to the input of the system under consideration. The values of $IP3_{OUT}$ and $IP2_{OUT}$ are the third- and second-order intercept points, respectively, referred to the output of the system under consideration.

Second-order non-linearity is lower in differential non-linear systems. Thus, in practical IC implementations, the IM2 components are less significant than the IM3 components. However, in RF system implementations, such as direct conversion (zero-IF) receivers, the IM2 components are critical, even if the receiver circuits are balanced, because of the possibility of the appearance of DC components or wide-band signal components as a result of second order distortion. These components can compete with the desired signal.

The prediction of the intercept points of the system is important in the early design phases in order to set the requirements on the individual circuit blocks. In time-domain simulators, prediction of the intercept points can consume considerable simulation time since the channel spacing is relatively very small compared to the carrier frequency in most RF systems. Thus, for a simulation in which a two-tone test with two RF carriers in two adjacent channels is used, the simulation time needed is at least the inverse of the frequency difference between these two RF carriers. Given the narrow channel spacing, which can be in the order of tens of kHz, and the high frequency of the carrier, the simulation time for one input power level can be very long, let alone having to sweep the power of the input as shown inFigure 5-3.

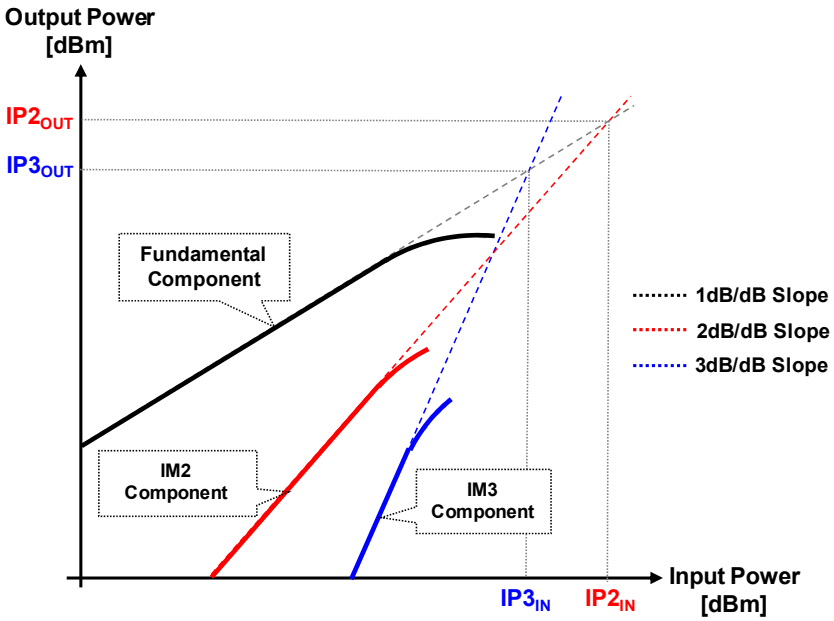


Figure 5-3 Definitions of second- and third-order intercept points.

One method to estimate the intercept point in an RF system is to calculate it mathematically. Setting $x(t)=A[cost(\omega_1 t)+ cost(\omega_2 t)]$ in equation (5.1), where ω_1 and ω_2 are the two interferers with the same amplitude, A, one can deduce that for a balanced narrow-band system:

$$y(t) = A(\alpha_1 + \frac{9\alpha_3 A^2}{4})[\cos(\omega_1 t) + \cos(\omega_2 t)] + \frac{3\alpha_3 A^3}{4}[\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t] + \ldots \quad \textbf{(5.6)}$$

If the circuit is operating in its linear region, such that $\alpha_1 >> \frac{9\alpha_3 A^2}{4}$, then the output amplitudes of the fundamental components at ω_1 and ω_2 are equal to the output amplitudes of the IM3 components at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ at a certain input amplitude $A_{IP3,IN}$ if:

$$\alpha_1 A_{IP3,IN} = \frac{3\alpha_3 A_{IP3,IN}^3}{4} \quad \textbf{(5.7)}$$

This implies that the input intercept point is given by:

$$A_{IP3,IN} = \sqrt{\frac{4}{3}\frac{\alpha_1}{\alpha_3}} \quad \textbf{(5.8)}$$

Using equations (5.8) and (5.3), it can be seen that the ratio between $A_{IP3,IN}$ and $A_{1\text{-}dB}$ is -9.6dB for sinusoidal signals. Since the amplitude of the 1-dB compression point is much easier to predict from simulations, one can predict the third order intercept point by adding 9.6 dB to the 1-dB compression point. This general rule is applicable if the two inputs are sinusoidal. If the inputs have other non-sinusoidal characteristics, the ratio between the 1-dB compression point and the third-order input intercept point will deviate from this value.

Another method to estimate the third-order input intercept point is by using two tones at the input of the non-linear system and measuring the difference in power between the fundamental and the IM3 components at its output, as shown in Figure 5-4 (a). From the figure, it can be seen that if the difference between the output power level of the fundamental components, at ω_1 and ω_2, and that of the IM3 components at, $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, is ΔP at a certain input power level, P_{in}, then the fundamental component and the IM3 component, if extrapolated, will have to meet at a point equal to $P_{in} + \Delta P_3/2$ to satisfy the slopes depicted in the figure; this point is the third-order input intercept point, *IIP3*. Similarly in Figure 5-4 (b), if the difference between the output power level of the fundamental components at, ω_1 and ω_2, and that of the IM2 components at, $\omega_1 - \omega_2$ and $\omega_2 - \omega_1$, is ΔP_2 at a certain input power level, P_{in}, then the fundamental component and the IM2 component, if extrapolated, will have to meet at a point equal to $P_{in} + \Delta P_2$ to satisfy the slopes depicted in the figure; this point is the third-order input intercept point, *IIP2*.

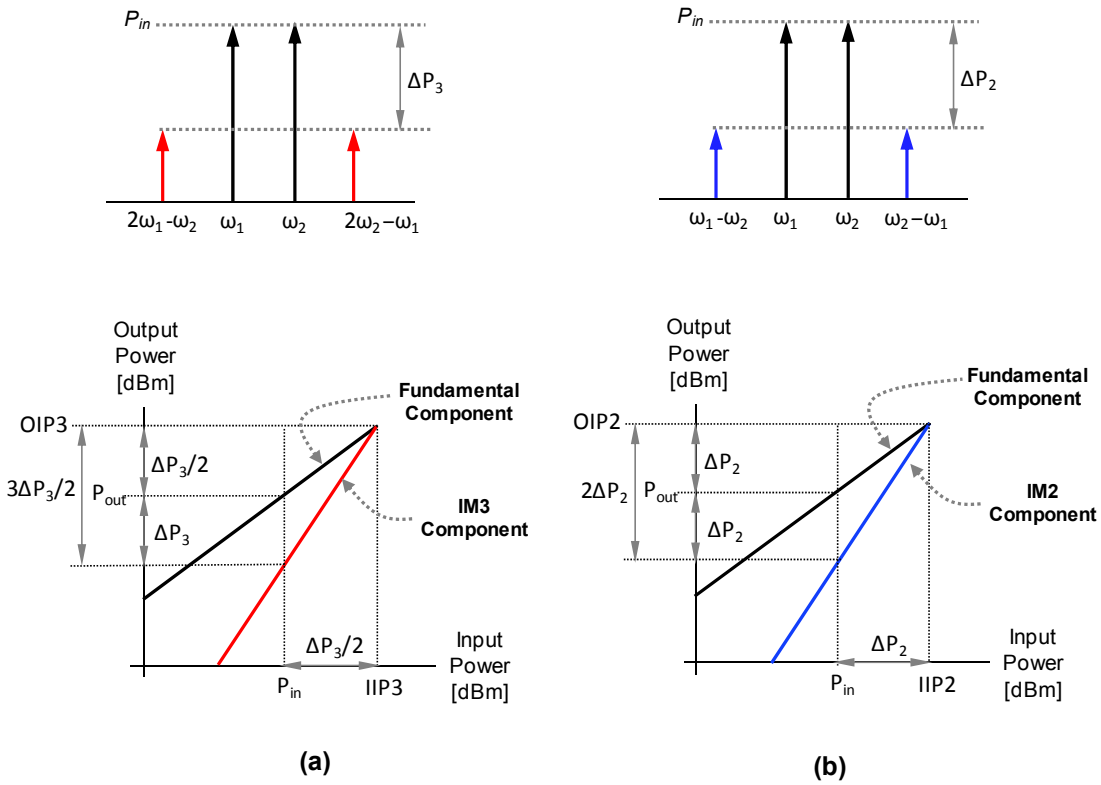


Figure 5-4 Input intercept point estimation (a) IIP3 and (b) IIP2

Note that the input power, P_{in}, of the fundamental components has to be such that the circuit is operating in its linear region and well below the compression point. The difficulty in measuring the intercept point is that it lies beyond the 1-dB compression point, as highlighted earlier. Thus, physically the circuit will not operate at the intercept point and will operate in a very non-linear region before reaching it where other non-linear components such as those arising from the fifth or seventh order inter-modulation can easily result in inaccurate prediction of the intercept point. Hence, it is necessary that the circuit behaves in its linear region before the fundamental and IM3 or IM2 component powers are extrapolated in real measurements or when the intercept point is predicted from a single-power level. In summary, the IIP3 and IIP2 formulae are given by:

$$IIP3 = P_{in} + \frac{\Delta P_3}{2} \tag{5.9}$$

$$IIP2 = P_{in} + \Delta P_2 \tag{5.10}$$

5.2.1.4 Linearity of Cascaded Systems

Any RF system is a cascade of circuits implementing different functions as was shown in Figure 5-1 . Each circuit has its own third-order intercept point and voltage gain. It can be shown that for a cascade of N circuits with third-order intercept points given by $IP3_{IN,1}$, $IP3_{IN,2}$, $IP3_{IN,3}$, ..., $IP3_{IN,N}$. and voltage gains of A_1, A_2, A_3,…, A_N, the overall third-order intercept point, in voltage terms, is given by [3]:

$$\frac{1}{IP3_{IN,TOT}^2} = \frac{1}{IP3_{IN,1}^2} + \frac{A_1^2}{IP3_{IN,2}^2} + \frac{A_1^2 A_2^2}{IP3_{IN,3}^2} + \ldots + \frac{A_1^2 A_2^2 \ldots A_N^2}{IP3_{IN,N}^2} \quad \textbf{(5.11)}$$

The above equation indicates that the IP3 value of the last stage of the cascade is the most critical in the system because this stage will receive the signal after being amplified by a large amount. Thus, if its IP3 is not high enough, it could be the limiting factor in the linearity of the whole cascade.

5.2.2 Noise in RF Systems

The receiver has to be able to receive signals that can be very close to the circuit's internal noise. Thus, it is important to quantify the receiver's noise floor and the minimum signal it can detect.

5.2.2.1 Definition of Noise Figure

It is of interest to determine by how much the system will degrade a signal that has a certain signal-to-noise ratio, SNR_{IN}. The noise figure of a system is a measure of this degradation. It compares the case where the signal is processed by a noiseless system to the real case where the signal is processed by a noisy system. In the case of a noiseless system, the *SNR* at the output of the system will be equal to the *SNR* at the input. In the real case, the *SNR* at the output of the system will be given by SNR_{OUT}. The noise figure, *NF*, in units of decibels is defined by:

$$NF = 10 \times \log_{10}\left(\frac{SNR_{IN}}{SNR_{OUT}}\right) \quad \textbf{(5.12)}$$

The noise figure of a noiseless system is 0 dB and that of a real network is always higher than 0 dB because the *SNR* at the output of the system will always be lower than that at the system's input due to the inherent noise in the circuits involved.

5.2.2.2 RF System Sensitivity

The Minimum Detectable Signal, *MDS*, in dBm, has to be processed by the cascade of circuits in the receiver and produce a certain *SNR* at its output given by SNR_{OUT}. At the receiver input, both the *MDS* and the noise will be amplified by the same gain, *G*, in decibels. Thus, we have:

$$SNR_{OUT}\,[dB] = (MDS + G) - (N_{O,IN} + G), \quad \textbf{(5.13)}$$

where, $N_{O,IN}$ is the noise at the output of the receiver when referred to the input in dBm. Therefore, rearranging equation (5.13) gives,

$$N_{O,IN} = MDS - SNR_{OUT}\,[dB] \quad \textbf{(5.14)}$$

At the receiver input, the *MDS* is limited by thermal noise, which is equal to the available thermal noise power[3] from a resistor at a reference temperature, *T*, of 290°K in a brick-wall bandwidth, *B*, in which this noise appears or the measurements are taken. The noise power, N_{IN}, is given, in dBm, by:

$$N_{IN} = 10\times\log_{10}(kTB/1mW) = -174dBm/Hz + 10\times\log_{10}(B) \quad \textbf{(5.15)}$$

where, *k* is Boltzmann's constant. From the definition of the *NF* in equation (5.12), we can write:

$$NF = N_{O,IN} - N_{IN} = 174dBm/Hz - 10\times\log_{10}(B) + MDS - SNR_{OUT}\,(dB) \quad \textbf{(5.16)}$$

This implies that the MDS is given by:

$$MDS = -174dBm/Hz + 10\times\log_{10}(B) + NF + SNR_{OUT}\,(dB) \quad \textbf{(5.17)}$$

[3] The available noise power is the maximum power that can be delivered by a noisy resistor to a second resistor. The value of the second resistor, according to the maximum power transfer theory, is equal to the value of the noisy resistor.

The noise floor of the receiver, given by $N_{O,IN}$, is determined by its output noise when referred to the input in the presence of the available thermal noise power. Thus, in terms of the *NF* of the system, we deduce that:

$$Noise\ Floor\ (dBm) = N_{O,IN} = MDS - SNR_{OUT} = -174dBm/Hz + 10\times log_{10}(B) + NF \quad \textbf{(5.18)}$$

Any signal whose power level is below this noise floor cannot be detected by the receiver.

5.2.2.3 Noise Figure of Cascaded Systems

As in the case of the intercept point, any RF system is a cascade of circuits. Each circuit has its own noise figure and voltage gain. For a cascade of *N* circuits having noise figures NF_1, NF_2, NF_3, ..., NF_N and voltage gains of A_1, A_2, A_3,…, A_N, the overall *NF* of the cascade is given by the Friis formula [26]:

$$NF_{TOT} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_1^2} + \frac{NF_2 - 1}{A_1^2 A_2^2} + \ldots + \frac{NF_N - 1}{A_1^2 A_2^2 \ldots A_N^2} \quad \textbf{(5.19)}$$

From equation (5.19), it can be noted that the *NF* of the first stage in the receiver is the most critical because its noise appears directly at the receiver's input, without any reduction to its contribution by the receiver's cascaded gain. The first stage of the receiver is usually preceded by a lossy component which raises the *NF* of the whole receiver when referred to the antenna of the RF system. Hence, it is critical to minimize the power loss of any circuit at the RF receiver input.

5.3 RF Receiver Specifications

The design of the RF transceiver of this work, for wireless sensor networks, healthcare, and energy systems draws from the specifications of various regulatory standards. The following is a subset of these standards:

1. IEEE802.15.4 (worldwide) [27]
2. FCC CFR47 part 15 (US), sections 15.109 (unintentional radiators, radiated emission limits), 15.205 (intentional radiators, restricted bands of operation), 15.209

(intentional radiators, radiated emission limits) and 15.247 (intentional radiators, operation within bands 2400 – 2483.5 MHz)

3. ETSI EN 300 440: "Short-range devices; Radio equipment to be used in the 1 GHz to 40 GHz frequency range" [28]; applicable for generic short-range devices (SRD) with up to 4 W EIRP
    a. receiver class 2 (medium reliable SRD communication medium)
    b. receiver class 1 (highly reliable SRD device)
4. ETSI EN 300 328: "Data transmission equipment operating in the 2.4 GHz ISM band and using wide band modulation techniques" [29]
5. ARIB STD T-66 (Japan)
6. Industry Canada document GL36 (Canada)

5.3.1 Thermal Noise Figure Specification

The maximum frequency error of the TX carrier (LO frequency) is ±40 ppm defined by the IEEE802.15.4-2003 standard. Hence, the total frequency error between the centre of the RX channel and the TX carrier is ±80 ppm or approximately ±200 kHz at 2480 MHz. From Figure 2-6, the occupied power bandwidth (OPBW) of an IEEE802.15.4 modulated signal is approximately 2.3 MHz at the receiver RF input. There is a trade-off when selecting the LPF bandwidth of the RF receiver. On the one hand, a narrower LPF improves the adjacent channel rejection of the receiver, but may degrade its sensitivity due to inter-symbol interference (ISI). On the other hand, a wider LPF bandwidth captures more of the desired signal power; this improves the sensitivity of the receiver at the expense of degradation in its adjacent channel rejection. From system simulations, and considering a ±200 kHz frequency error as well as a ±3% calibration error in the LPF bandwidth, the LPF bandwidth is chosen to be 1.3 MHz at the base-band of the receiver [30].

The IEEE 802.15.4 standard specifies a minimum transmit power of -3dBm and a minimum sensitivity of -85dBm for 1% packet error rate (PER) with a physical layer data service unit

(PDSU) length of 20 octets in the absence of interference. The link budget of a wireless link is defined by the difference between the power transmitted at the transmitter's antenna and the signal received at the receiver's antenna. This results in a link budget of 82dB for a typical IEEE802.15.4 transceiver. Gutierrez *et al.* [31] describe a commonly used model that approximates the propagation behavior of RF signals in real environments based on a log-normal shadowing model. This model takes into account several environmental parameters which impair the RF signal propagation such as reflection, diffraction and scattering. Under typical indoor propagation effects, it has been observed that the distance covered by an IEEE802.15.4 signal is a function of the characteristics of the wireless channel which can be modeled with a path loss coefficient and a variance in the range of the wireless link due to the effects of various environmental impairments. For example, with a path loss coefficient of 4 and a variance of 7dB in the received signal power, the mean distance covered by the signal is approximately 7 meters, which is quite low for a wireless sensor network link. It is desirable to maximize the indoor propagation range. Hence, a link budget of about 100dB is set as a target for the RF receiver which, according to [31], translates to a mean propagation range of 20 meters. This link budget can be achieved by increasing the output power to up to 5dBm which is achievable but limited by the break-down voltage of the devices available in the 0.18μm manufacturing process selected for this work. This transmit power level is compliant with local regulatory requirements world-wide. In addition, increasing the target sensitivity of the receiver to -95dBm will yield 100dB in terms of link budget. Furthermore, assuming a minimum demodulator SNR of 5dB at the sensitivity level, the noise figure at the RF receiver's antenna input can be calculated from (5.16) as:

$$NF_{thermal} = 174dBm/Hz - 10\times log_{10}(2\times 1.3MHz) - 95dBm - 5dB \approx 9.85 \text{ dB} \quad \textbf{(5.20)}$$

This *NF* serves as an aggressive target for a low-power receive chain for wireless sensor networks.

The receiver also operates in other non-standard proprietary modes which support bit-rates up to 2Mbps using GFSK modulation. The NF level required for the IEEE 802.15.4 standard is

sufficient to meet the required sensitivity levels for proprietary FSK, MSK, GFSK and GMSK modulation schemes with data rates between 125 kbps to 2 Mbps in the 2.4GHz band. For example, considering the 2Mbps GFSK case, the OPBW for this modulation scheme is 1.8MHz as shown in Figure 2-6. From system simulations, the LPF bandwidth is chosen to be 1 MHz at the base-band of the receiver for the 2Mbps GFSK case. The LPF bandwidth was selected based on a ±200 kHz TX-RX crystal frequency error as well as a ±3% calibration error in the LPF bandwidth. The minimum required SNR at the demodulator input is about 15dB for a 2Mbps GFSK signal. From (5.20), the target NF for the IEEE 802.15.4 mode is 9.85dB. Using (5.17), this yields a required sensitivity level of:

$$MDS = -174dBm/Hz + 10\times\log_{10}(2\times 1MHz) + 9.85dB + 15dB \approx -86dBm \quad \textbf{(5.21)}$$

5.3.2 Linearity Specifications

As indicated earlier, an RF receiver has to cope with relatively large blocking signals. The receiver's blocking rejection, measured using a continuous wave (CW) or a modulated blocker, is a figure of merit that describes the aggregate effect of the dynamic range, filtering characteristics and phase-noise performance of the receiver. The following describes the most relevant specifications set by various standards:

1. The IEEE802.15.4 standard's minimum receiver blocker rejection requirements for the 2450 MHz physical layer (PHY) are shown in Figure 5-5 and are summarized as follows:
    a. Adjacent channel rejection is 0 dB for an input RF power of -82dBm for the wanted signal when the unwanted signal is another IEEE802.15.4 signal.
    b. Alternate channel rejection is 30 dB for an input RF power of -82dBm when the unwanted signal is another IEEE802.15.4 signal. This corresponds to a signal power of –52dBm in the alternate channel.
2. The ETSI EN 300 440-1 class 2 standard for medium reliability short-range device (SRD) devices specifies a minimum CW blocker rejection for a wanted signal whose

level is 3 dB above the system sensitivity level. This specification is shown in Figure 5-5. In this figure, the sensitivity level is -95dBm.

3. The ETSI EN 300 440-1 class 1 standard for highly reliable SRDs specifies a minimum CW blocker rejection for a wanted signal whose level is 3 dB above the system sensitivity level. This standard applies to systems with greater than 1 MHz channel spacing. This specification is also shown in Figure 5-5.

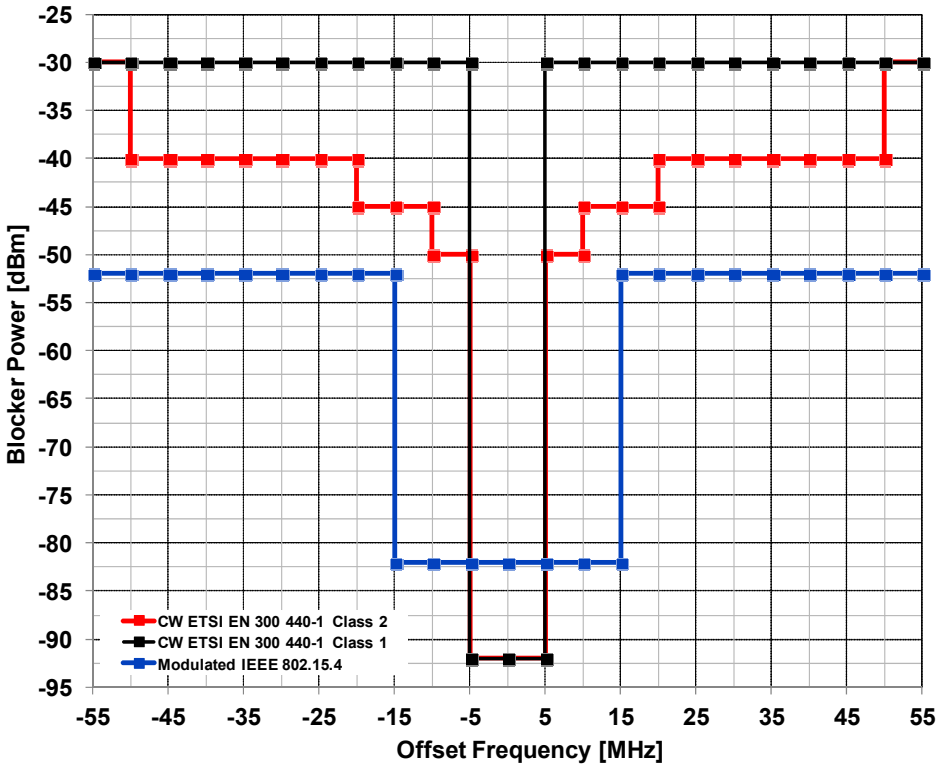


Figure 5-5 Required blocker rejection according to different standards

It can be noted from Figure 5-5 that the blocking rejection specification of the ETSI EN 300 440-1 class 1 standard is the most stringent. Since the 2.4 GHz band is an unlicensed world-wide band, wireless systems operating in this band are susceptible to interference from other co-existing systems. Hence, for a more reliable RF system operating in this frequency band, it is important to target the highest possible level of blocker rejection for a given power consumption budget. We deemed it necessary to exceed the blocker rejection specifications of the ETSI EN 300 440-1 class 2 for this RF transceiver at the lowest possible power

consumption to ensure reliable operation of all wireless networks in which the RF receiver will be potentially used. The ETSI EN 300 440-1 class 1 standard is reserved for the most robust SRD devices and is usually used for mission-critical applications such as in industrial applications. Achieving the blocking rejection specification of this standard is expected to require higher power consumption than that of the ETSI EN 300 440-1 class 2 standard due to the more demanding phase noise and linearity requirements. Hence, it is envisioned that the RF receiver in this work will exceed the requirements of the ETSI EN 300 440-1 class 2 specification sufficiently to make it the best-in-class RF receiver at the lowest possible power consumption.

The blocker rejection profile shown in Figure 5-5 suggests that blocker rejection for frequency offsets greater than 50 MHz needs to be at least -30dBm for ETSI EN 300 440-1 class 2 operation. The cost of RF transceivers developed for wireless sensor networks has to be kept to a minimum; this translates to avoiding any expensive RF filtering. Hence, the RF receiver will have to meet a 1-dB compression point of at least -30dBm in order to meet this specification. This 1-dB compression point level will insure that the RF receiver front-end will linearly process a desired signal level of 3 dB above the system sensitivity level (-95dBm in this case) with a reduction in the maximum gain of 1dB in the presence of a -30dBm CW blocker.

The blocker rejection specification defined by the EN 300 440-1 class 2 standard in Figure 5-5 specifies a CW blocker. Although, strictly speaking, there is no IIP3 specification in the standard, it is important to examine the conditions under which an IIP3 specification is necessary for the correct operation of the receiver. Theoretically, the IIP3 of the RF receiver should be 9.6dB above its 1-dB compression point for CW blockers. Hence, the IIP3 is expected to be -30dBm + 9.6dB = -20.4dBm. The in-band IIP3 of the RF receiver can be derived based on the blocking rejection requirements depicted in Figure 5-5 by assuming two

RF tones at 5MHz and 10MHz frequency offsets from the desired channel. These two tones will generate an IM3 component which will fall in the desired channel.

Figure 5-6 shows the IM3 component due to CW blockers in the adjacent and the alternate channels. The level of this IM3 component is given by:

$$\begin{aligned} P_{im3} &= P_{adj.chan} - 2 \times \left(IIP3 - P_{alt.chan} \right) \\ &= -50dBm - 2 \times \left(-20.4dBm - (-45dBm) \right) \\ &= -99.2dBm \end{aligned} \tag{5.22}$$

From (5.22), it can be seen that the IM3 component is 4.2dB below the sensitivity level of the receiver and, as a result, has a negligible effect on the receiver's performance. The adjacent and alternate channels in the 2.4GHz band can also be modulated channels. For example, they can be neighbouring IEEE 802.15.4 channels. Hence, it is important to examine this particular case.

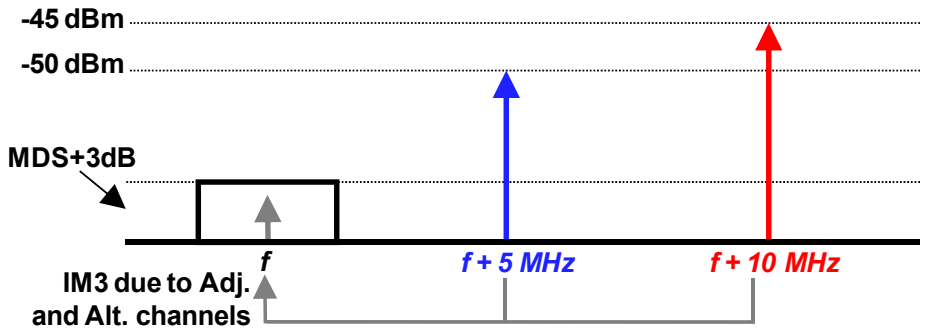


Figure 5-6 In-band IIP3 with CW adjacent and alternate channels

Figure 5-7 shows the case where the adjacent and alternate channels are modulated. In this case, the IM3 component should be below the minimum detectable signal by at least the SNR required to receive the signal in order to avoid any degradation to the receiver's sensitivity. According to the EN 300 440-1 class 2 specification, the desired signal is set at 3dB above the sensitivity level of the receiver at the antenna input. Hence, the IIP3 from the scenario depicted in the figure can be calculated as:

$$
\begin{aligned}
IIP3 &= P_{alt.chan} + \frac{P_{adj.chan} - P_{im3}}{2} \\
&= -45dBm + \frac{-50dBm - (-95dBm + 3dB - 5dB)}{2} \\
&= -21.5dBm
\end{aligned}
\tag{5.23}
$$

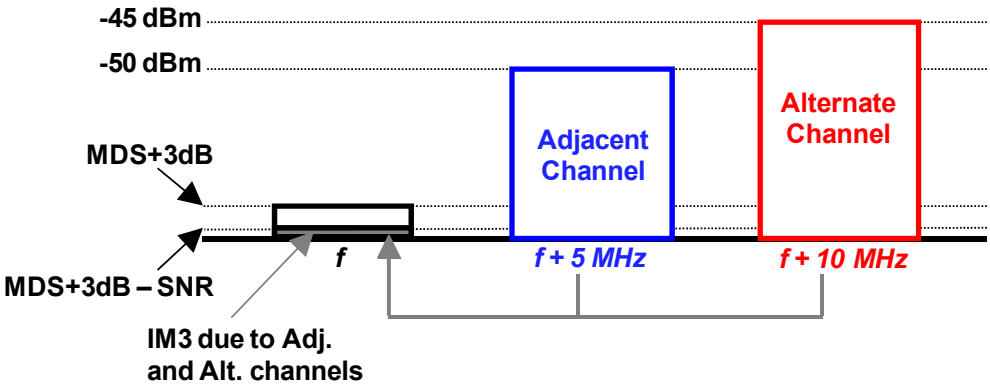


Figure 5-7 In-band IIP3 with modulated adjacent and alternate channels

The calculation in (5.23) assumes that the effect of an uncorrelated IEEE 802.15.4 MSK signal is approximately equivalent to the effect of white noise of the same power in the same channel bandwidth. An IIP3 of -21.5dBm is in line with the estimate that the IIP3 should be 9.6dB higher than the 1-dB compression of -30dBm. It should be noted that other blockers can cause an IM3 component to appear in the desired channel. For example, according to Figure 5-5, two -45dBm RF tones at 10MHz and 20MHz frequency offsets from the desired channel or two -40dBm RF tones at 25MHz and 50MHz frequency offsets from the desired channel would require an IIP3 of -19dBm and -11.5dBm respectively for a sensitivity level of -95dBm and SNR of 5dB. Moreover, two -30dBm RF tones at 50MHz and 100MHz would require an IIP3 of -1.5dBm under the same conditions. The ETSI EN 300 440-1 class 2 specifies the blocker rejection levels depicted in Figure 5-5 and does not specify an IIP3 level. In a wireless system, it is expected that the receiver has to meet a certain level of IIP3.

There could be a scenario in which two temporary RF tones generate an IM3 component that approaches the sensitivity level of the receiver and hinders it from receiving a desired signal. In this case, the communication link will retry sending the desired signal which was blocked until such time that those two temporary RF blocking signals cease to exist and the receiver is able to receive that desired signal. Hence, the receiver should achieve the highest possible IIP3 given a certain power consumption budget. It is expected that the receiver will be blocked in the presence of blocker signal levels that are higher than those for which it was designed for. However, even in this case, the communication system will still be able to function correctly with a number of transmit attempts for the desired signal at the expense of a relatively higher power consumption for that particular communication link during the period of time in which the receiver remains blocked. The design target for the IIP3 of the receiver is chosen to be at least -19dBm.

As with the NF consideration, the receiver also operates in other non-standard proprietary modes which support bit-rates up to 2 Mbps using GFSK modulation. For the 2Mbps GFSK mode, the blocker rejection specification is also defined by the ETSI EN 300 440-1 class 2 standard shown. However, it is possible that the RF channel spacing in this mode be less than 5MHz due to the smaller OPBW for a 2Mbps GFSK signal. For example, the channel spacing could be 3MHz. For any channel spacing, the IIP3 can be calculated based on the receiver sensitivity calculated in (5.21) as follows:

$$\begin{aligned} IIP3 &= P_{alt.chan} + \frac{P_{adj.chan} - P_{im3}}{2} \\ &= -45dBm + \frac{-50dBm - (-86dBm + 3dB - 15dB)}{2} \\ &\approx -21dBm \end{aligned} \quad \textbf{(5.24)}$$

The IIP3 for the 2Mbps GFSK mode is 2dB lower than that for the IEEE 802.15.4 mode. Hence, the target for the RF receiver's IIP3 is -19dBm. A design margin of 3dB is added, yielding design targets of -16dBm and -25dBm for the IIP3 and the P1dB respectively.

There is no explicit specification for the IIP2 of the receiver in standards regulating short-range devices. However, an estimation of the IIP2 required for the receiver can be made from the blocker levels highlighted in Figure 5-5. Due to second-order non-linearity, two -50dBm RF blockers present at 5MHz and 5.1MHz will generate an IM2 component at 100kHz which can fall in the base-band of a direct-conversion receiver. Similarly, two -40dBm blockers present at 30MHz and 30.1MHz can also generate an IM2 component at 100kHz at base-band due to second order non-linearity. Based on (5.10), the IIP2 can be calculated in the various blocker scenarios assuming that the IM2 component will fall below the minimum detectable signal by at least the SNR required to receive the signal in order to avoid any degradation to the receiver's sensitivity. Borrowing from the EN 300 440-1 class 2 specification, the desired signal is set at 3dB above the sensitivity level of the receiver at the antenna input. Hence, the IIP2 can be calculated for two -40dBm blockers and a desired IEEE802.15.4 signal as follows:

$$\begin{aligned} IIP2 &= P_{bloc\,\mathrm{ker},1} + (P_{bloc\,\mathrm{ker},2} - P_{im2}) \\ &= -40dBm + \left[-40dBm - (-95dBm + 3dB - 5dB)\right] \\ &= 17dBm \end{aligned} \quad \textbf{(5.25)}$$

Based on (5.25), and adding 3dB as a design margin, the receiver should achieve an IIP2 of at least 20dBm for the conditions outlined.

Overall, in order to meet the ETSI EN 300 440-1 class 2 specification, an IEEE 802.15.4 or a 2Mbps GFSK modulated signal is placed 3dB above the receiver sensitivity and a single CW blocker is swept at the frequency offsets shown in Figure 5-5. The effect of the receiver's LPF order, LO phase noise, compression and demodulator characteristics determine the receiver's blocker rejection performance. The calculations illustrated in this section are an important first step to specify the basic requirements of the receiver which can be used to predict the receiver's blocker rejection performance in the presence of various impairments.

5.3.3 LO Phase Noise Specification

LO phase noise has a detrimental effect on an RF receiver's performance. If the LO is ideal and produces an ideal sine wave, all channels in an RF system will be down-converted to their respective base-band channels with no adverse effect of one channel on the other. However, in practice, the LO exhibits a non-ideal behaviour which can be characterized by its phase noise spectrum. The effect of phase noise can be explained with the aid of Figure 5-8. Without loss of generality, it is assumed that the base-band frequency, f_{bb}, is equal to zero. Hence, a desired channel at f_{lo} mixes with the LO frequency through the receiver's RF mixer and down-converts to $f_{bb}=0$. However, in the presence of phase noise, blockers in the RF system, for example, at the adjacent and the alternate channels, will also be down-converted to the same channel at $f_{bb}=0$ due to the presence of an LO signal (in the form of phase noise) at the adjacent and the alternate channel frequencies, f_{adj} and f_{alt}, respectively. This effect is known in receiver design as *reciprocal mixing*. Hence, it is critical to impose the necessary specification on the phase noise of the LO such that blockers do not significantly degrade the sensitivity of the receiver after down-conversion.

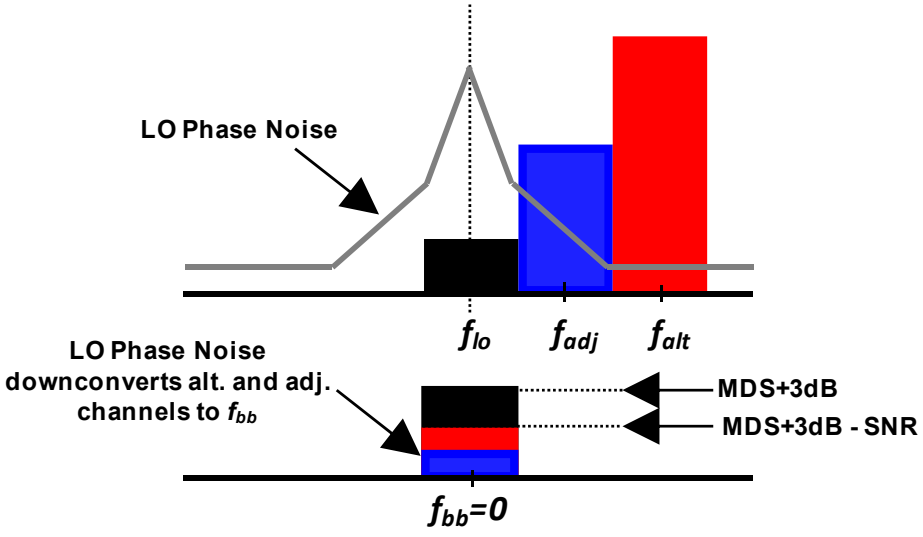


Figure 5-8 Reciprocal mixing effect in RF receivers due to the LO phase noise

In order to avoid degradation in the receiver's sensitivity, the reciprocal mixing products should be below the level of the desired signal by an amount that is at least equal to the signal-to-noise ratio of the system after down-conversion. There is no separate reciprocal

mixing test in the ETSI EN 300 440-1 class 2 standard since it is implicit in the blocker rejection specification. Hence, for a desired signal level of 3dB above the receiver's MDS of -95dBm, the reciprocal mixing products should be lower by at least the amount of SNR required to demodulate the signal, which is 5dB. Hence, the phase noise in this case is given by:

$$PN(\Delta f) = P_{sense} + 3dB - SNR - P_{blocker}(\Delta f) - 10\log_{10}(BW) \quad \textbf{(5.26)}$$

where, P_{sense} is the sensitivity level of the receiver at the antenna, SNR is the minimum SNR required to demodulate the desired signal, $P_{blocker}$ is the blocker power at an offset, Δf, from the desired signal, and BW is the RF bandwidth of the desired signal. It is worth noting that (5.26) assumes that phase noise at a frequency offset, Δf, is flat within the signal bandwidth. Although this is not a very accurate assumption, it is sufficient for the purpose of preliminary system calculations. For P_{sense}=-95dBm, SNR = 5dB, $P_{blocker}$ =-50dBm at Δf = 5MHz and BW = 2×1.3MHz and using (5.26), the required phase noise is approximately -112dBc/Hz at 5MHz offset from the LO for the desired channel. This level of phase noise can be readily achieved using a low power receiver.

Table 5-1 shows the phase noise specifications for different standards and modulation schemes. It can be seen from the table that the requirements for the IEEE 802.15.4 standard and the 2Mbps GFSK modulation scheme are almost the same. Assuming a -20dB/decade slope for the LO phase noise, the phase noise requirements at 10MHz and 50MHz will be met if the phase noise specification at 5MHz is met. Furthermore, the table shows that for the ETSI EN 300 440-1 class 1 standard, where a -30dBm blocker is present at 5MHz offset from the desired channel, a phase noise level of -132dBc/Hz is required at this frequency offset. Despite being challenging at low power consumption, this LO phase noise requirement would be attractive if it could be met since it has a direct impact on the blocker rejection performance of the receiver. However, it should be noted, as indicated earlier, that blocker rejection is a complex process and meeting the phase noise requirements for ETSI EN 300 440-1 class 1 does not directly translate to meeting its blocker rejection specification since the

amount of rejection due to the LPF as well as the demodulator characteristics play a significant role in determining the overall receiver rejection. The philosophy adopted for the receiver design is to try to maximize the RF performance with a power consumption budget of 30mW to achieve best-in-class RF performance.

Blocker Rejection Specification	Modulation	RF BW [MHz]	Offset [MHz]	$P_{blocker}$ [dBm]	P_{sense}+3dB [dBm]	SNR [dB]	PN [dBc/Hz]
EN 300 440-1 class 2	IEEE802.15.4	2.6	5	-50	-92	5	-112
	IEEE802.15.4	2.6	10	-45	-92	5	-117
	IEEE802.15.4	2.6	50	-30	-92	5	-132
	2Mbps GFSK	2.1	5	-50	-83	15	-112
	2Mbps GFSK	2.1	10	-45	-83	15	-117
	2Mbps GFSK	2.1	50	-30	-83	15	-132
EN 300 440-1 class 1	2Mcps MSK	2.6	5	-30	-92	5	-132
	2Mbps GFSK	2.1	5	-30	-83	15	-132

Table 5-1 **Phase noise specification according to different standards and modulation schemes**

5.4 RF Receiver Architecture

Due to the large scale deployment expected for wireless sensor networks for various applications, the cost of manufacturing and testing the transceiver IC as well as the host system is critical. This calls for architectures and circuit design techniques which require no external components, calibration-at-test or calibrations that take a significant amount of time during power-up.

Among receiver architectures, the low-IF receiver (LIFR) and zero-IF receiver (ZIFR) are the most viable choices for a fully integrated receiver since neither of these receiver architectures requires any external components and both are designed with a single down-conversion stage. Table 5-2 compares the two architectures in terms of the aspects that are most relevant to receivers used in wireless sensor networks, healthcare and energy systems.

	ZIFR	***LIFR***
Flicker Noise	Since the ZIFR down-converts RF signals to base-band, flicker noise degrades the signal's SNR; however, circuit techniques exist to minimize the degradation. In addition, the effect of this SNR degradation is reduced for wide-band signals.	The LIFR down-converts RF signals to an IF frequency. Hence, flicker noise does not affect the signal's SNR.
Static Offsets	Present due to systematic and random circuit mismatches but can be readily cancelled after receiver power-up and before receiving the desired signal.	Have the same effect as a ZIFR since DC offsets can saturate the receiver. Hence, static DC offsets also need to be cancelled after receiver power-up and before receiving the desired signal.
Dynamic Offsets	Present due to time-varying LO and blocker self-mixing and need to be cancelled quickly since these offsets are present during signal reception and while the receiver changes its gain. Inserting a wide bandwidth HPF is not an option in ZIFR since the signal is at base-band and only a very small part of the spectrum around DC can be removed by a HPF. This translates into the need for a fast offset correction loop (OCL).	Present due to time-varying LO and blocker self-mixing as well. However, a wide bandwidth HPF can be used in the signal path to cancel these offsets quickly since the signal is at an IF and not at base-band. Hence, these offsets can be removed without any degradation in the signal SNR.
RF Mixer Image	In a ZIFR, the RF mixer image is the signal itself. Hence, unlike IF architectures, the RF mixer does not down-convert an undesired blocker	In a LIFR, the RF mixer image is another uncorrelated signal which can be much higher than the desired signal. For example, if the IF

	to the signal band. Nevertheless, image rejection is still relevant in a quadrature ZIFR from the point of view of SNR. In the presence of quadrature errors, the down-converted signal constellation can degrade. However, a 5° phase imbalance could slightly degrade the SNR in a ZIFR while yielding an image rejection of only 27 dB in a quadrature LIFR which is detrimental to the performance of the latter while being a small performance degradation in the former [32].	frequency is 6MHz and for an offset frequency between 10MHz and 20MHz, the finite image rejection of a LIFR receiver limits the blocker rejection to around 34dB [33], which is too low to meet the target value of at least 47dB specified by the ETSI EN 300 440-1 class 2 specification as shown in Figure 5-5. Image rejection calibration schemes can be used but they typically require injection of a signal at the image frequency at the receiver input which is complex to generate. The target of this receiver is to exceed the ETSI EN 300 440-1 class 2 specification. Hence a ZIFR excels in this regard without needing a complex calibration scheme.
SSB versus DSB Noise Figure	Double-side band (DSB) NF is used to measure the noise figure of a ZIFR where the image band contains both noise and an image signal identical to the desired band. The NF is given by $NF_{DSB} = 1 + N_{mix}/N_d$ [34]. Where N_{mix} is the intrinsic mixer noise, N_d is the noise in the desired signal band. If the mixer is noiseless ($N_{mix}=0$), the NF is 0dB which is 3dB lower than the NF of the LIFR.	Single-side band (SSB) NF is used to measure the noise figure of a LIFR where there is no signal at the image frequency but the source noise exists. The NF is given by $NF_{SSB} = 2 + 2\times N_{mix}/N_d$ [34], where N_{mix} is the intrinsic mixer noise, and N_d is the noise in the desired signal band. If the mixer is noiseless ($N_{mix}=0$), the NF is 3dB which is 3dB higher than the NF of the ZIFR. However, it should be noted that flicker noise present around DC in the ZIFR architecture will degrade its NF and the full 3dB improvement over the LIFR architecture will not be fully attainable

IIP2 Requirements	Second-order distortion in the RF mixer can cause an AM blocker to produce a wide-band signal at the base-band. This signal cannot be removed with the OCL because of the OCL's low bandwidth. Hence, the receiver will have to cope with an AM blocker while receiving a desired signal at the sensitivity level which translates to the need for an adequate IIP2 performance for the receiver.	Second-order distortion in the RF mixer can also cause an AM blocker to produce a wide-band signal at the base-band. However, due to the presence of a wide-bandwidth HPF for static and dynamic offset correction, the resulting wide-band signal can also be removed to a large extent. The requirement to reject an AM blocker can be factored in the design of the HPF. As a result, the IIP2 requirement for a LIFR is more relaxed than a ZIFR.
AGC Requirements	Since the ZIFR down-converts phase –modulated signals to the base-band, it effectively down-converts the phase information of these signals to amplitude information. This requires a fast and accurate AGC circuit to avoid any signal amplitude compression in the receiver chain. This is made more complex by the need for a fast and continuous offset correction loop to cancel dynamic offsets. The interaction of the OCL and AGC loops needs to be carefully considered.	Since the LIFR down-converts phase –modulated signals to an IF frequency, the receiver is more amenable to signal compression since the signal's phase information is preserved. This translates into more relaxed requirements for the AGC in terms of speed. In addition, this also enables the use of limiters in the base-band instead of an ADC at the expense of not having digital filtering [35].
BB Filter and ADC Requirements	Since the ZIFR down-converts RF signals to base-band, the implementation of high-order LPFs is more power efficient which	The LIFR down-converts RF signals to an IF frequency. The IF frequency is selected based on the received signal bandwidth. A higher IF

	translates to better blocker rejection. In addition, a power-efficient ADC with a high sampling rate can be implemented since the received signal is at base-band. The high sampling rate for the ADC relaxes the filtering requirements for its sampling image.	frequency is needed for wide-bandwidth signals. For the same LPF order as a ZIFR, the LIFR will consume much higher power. In addition, if an ADC is required for an LIFR, it would have a bandwidth which is at least equal to the IF frequency plus the signal bandwidth. This makes the ADC design more complex and likely to consume higher power than the equivalent ADC needed for a ZIFR.

Table 5-2 Comparison between ZIFR and LIFR architectures

Based on the comparison in Table 5-2, one can observe that the ZIFR architecture offers significant performance advantages over a LIFR, namely, the ZIFR's ability to be a receiver with a high blocker rejection at all frequency offsets from the desired channel (including the image channel) yet consume less power than a LIFR. However, as with any engineering design, this comes with a set of challenges which need to be overcome. A ZIFR design will require the following to be addressed in order of difficulty:

1. A continuous offset correction loop (OCL) which
    a. Needs to operate with a low bandwidth to avoid introducing inter-symbol interference (ISI) or degradation in the signal's SNR yet be fast enough to cancel dynamic offsets in the presence of the desired signal and receiver gain changes.
    b. Needs to operate in conjunction with a fast AGC which does not allow the OCL enough time to detect dynamic offsets.
2. Circuit designs which reduce the effect of flicker noise on the signal's SNR.
3. Relatively high IIP2 performance for the receiver.

Furthermore, the receiver's blocker rejection performance in the unlicensed 2.4GHz band is the most critical performance specification. The receiver's ability to reject high power blockers translates into a reliable wireless network which in turn translates into wider adoption in the areas of healthcare, energy and, in general, a true replacement for wired connectivity. This is in addition to lower cost which translates into large scale deployment of the wireless networks that utilize the receiver. This work adopts the ZIFR architecture and addresses those engineering challenges.

5.5 Concluding Remarks

This chapter introduced the fundamental challenges in an RF receiver design. These challenges are translated into a set of specifications such as linearity and noise. The concepts of a receiver's gain compression, desensitization, blocking, inter-modulation distortion and noise figure were introduced. The RF receiver's specifications for thermal noise figure, linearity and phase noise were derived based on the requirements of various proprietary communication protocols and RF standards such as IEEE802.15.4 and ETSI EN 300 440 class 2. Two competing RF receiver architectures were introduced and compared; the low-IF receiver (LIFR) and the zero-IF receiver (ZIFR). Due to the ZIFR's high blocker rejection at all frequency offsets, it was the architecture of choice for this work.

Chapter 6

RF Receiver Design

6.1 RF Receiver Architecture Details

Following the system level discussions of the receiver architecture in the previous chapter, this chapter will detail the receiver architecture and develop specifications for the blocks which constitute the ZIFR.

6.1.1 Architecture Block Diagram

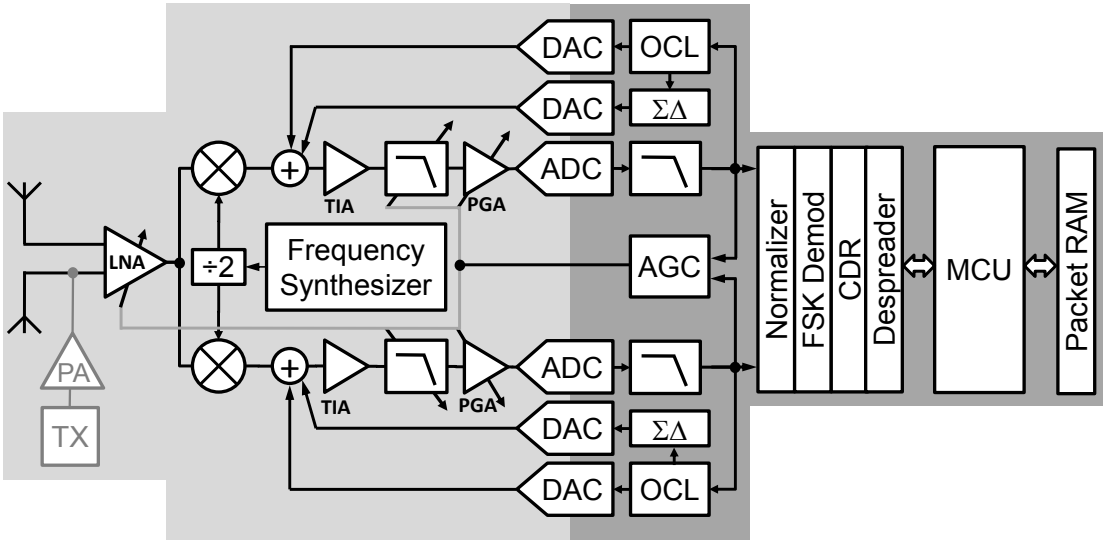


Figure 6-1 RF receiver block diagram

Figure 6-1 shows the block diagram of the receiver adopted for this work [1]. For reasons outlined in Chapter 5, the receiver is based on a ZIFR architecture. The LNA has two differential input ports; they are used for switched antenna diversity in order to improve the range and reliability of the wireless network [36]. One of the differential ports is shared between the LNA and the transmitter's PA; this avoids the need for a transmit/receive switch for this half-duplex receiver at the expense of a negligible degradation in noise figure and output power. One of the LNA inputs can be disabled using a switch to ground and the second input can be disabled using the PA devices. This grounds the LNA's differential inputs. The

ability to disable the LNA inputs is part of the OCL and will be explained in Chapter 8. The LNA has two 12dB attenuation steps. As explained in Chapter 5, flicker noise is one of the main challenges in ZIFR. A current-commutating passive RF mixer is an effective circuit technique to combat the effects of flicker noise in a ZIFR [37]. A comparison between active and passive RF mixers will be provided later in subsequent sections of this chapter.

The IEEE 802.15.4 standard uses an OQPSK modulation scheme in which each 4-bit data symbol is mapped onto a 32-chip pseudo-random spreading sequence which is a form of DSSS. The bit rate for the IEEE 802.15.4 standard is 250kbits/s and the symbol rate is 62.5ksymbols/s (4-bits per symbol). The chip rate is 2Mchips/s (32 chips × 63.5ksamples/s). Even-indexed chips are transmitted as an in-phase (I) component and odd-indexed chips are transmitted as a quadrature (Q) component. The chip rate for either the I or Q channels is 1Mchips/s whereas the aggregate chip rate for both I and Q channels is 2Mchips/s [27]. The 90˚ phase shift between the I and Q data channels is introduced using one chip delay between the I and Q components. Each chip on either the I or the Q channel is passed through a half-sinusoidal pulse shaping filter. In effect an OQPSK modulation with half-sinusoidal pulse shaping is equivalent to MSK modulation; this greatly simplifies the transmission and reception of this modulation scheme [38]. Since the IEEE 802.15.4 standard uses a complex modulation scheme, I and Q mixers are used in the receiver. The quadrature LO signals are generated using a frequency divider which divides by two the frequency generated by the frequency synthesizer at 4.8GHz. The trade-off between the noise, gain and linearity of the passive mixer will be studied in subsequent sections. Following the passive mixer is a trans-impedance amplifier (TIA), which converts the base-band currents from the passive mixer into the voltage domain. The virtual ground of the TIA is used as the summing node for the current outputs of the OCL DACs to cancel both static and dynamic offsets in the receiver.

The TIA is followed by a base-band LPF and a programmable gain amplifier (PGA). The LPF serves as the channel filter as well as an anti-aliasing filter for the ADC. It is implemented as

a third order active-RC Chebychev low-pass filter with 1.3MHz bandwidth and 0.25dB ripple. The LPF attenuates the adjacent channel at a frequency offset of 5MHz by about 40dB in order to prevent interferers from saturating the ADC and to meet the ETSI EN 300 440-1 class 2 blocker resilience specification at that frequency. Using OTAs, the LPF is implemented as an active single-pole stage in cascade with a biquad stage. The LPF has a gain control range from 12dB to 24dB in steps of 6 dB and consumes 0.54mA from a 1.8V supply. The RC time-constant of the LPF is calibrated using an on-chip reference RC oscillator. The PGA implements a gain control range from 0dB to 24dB in steps of 3dB. It is implemented using an OTA with resistive feedback and consumes 0.35mA from a 1.8V supply while driving the ADC.

A low-power 13Msps 6-bit ADC is used. This gives a total dynamic range of 45dB, where the dynamic range is the difference between the maximum signal level at the ADC input relative to its integrated quantization noise in the signal bandwidth. The desired signal, blockers after being filtered by the LPF, residual static and dynamic offsets, as well as margin for AGC gain errors have to fit in this dynamic range. This aggressive scaling of the dynamic range is necessary for the ADC to operate with very low power consumption. The ADC is implemented using a pipelined architecture with shared OTAs for minimum silicon area and power consumption. Including the reference buffer, both I and Q ADCs consume 0.9mA from a 1.8V supply [2].

A third-order digital LPF follows the ADC; this reduces the integrated noise in the signal bandwidth prior to the demodulator and effectively increases the ADC's SNR by about 6dB. The digital LPF also further attenuates the blocker at 5MHz by an additional 35dB. In addition, the AGC and OCL are both implemented in the digital domain.

The digital LPF is followed by an MSK demodulator which is implemented as a complex frequency correlator (CFC) followed by a PLL-based clock and data recovery circuit [39].

The IEEE802.15.4 standard uses a 32-chip pseudo-random spreading sequence for each 4-bit symbol being transmitted. The spreading sequence is implemented by means of rotation and conjugation (inversion of chips with odd indices). Symbols 0-7 represent cyclic shifts in multiples of four chips, while symbols 8-15 use the same shifts as symbols 0-7 but use a conjugated sequence, i.e, the odd-indexed chips are inverted. Hence, the 16 symbols are represented by only two unique 32-chip sequences and rotated versions thereof [27]. By using this property, the complexity of the de-spreader is significantly reduced. A serial-to-parallel converter collects the output of the de-spreader and routes it to the MCU. In turn, the MCU handles the interface to a 256-byte packet RAM where it stores the packet being received.

6.1.2 Architecture Analysis

The design of the RF receiver requires a careful balance between the performance parameters imposed by various standards and environmental conditions on the one hand, and circuit implementation as well as power consumption on the other hand. Typically, the RF mixer is the bottleneck for the receiver's linearity. This is attributed to the need for an LNA preceding the RF mixer to amplify the desired RF signal such that it overcomes the noise of the receiver chain. This translates to the presence of relatively high signal levels for both the wanted signal and the unwanted RF blockers at the RF mixer input. The RF mixer is required to amplify both the wanted and unwanted signals linearly while contributing very little noise to the RF receiver. Ideally, the LNA should dominate the noise figure of the RF receiver with a smaller contribution from the mixer and an even a smaller contribution from the rest of the RF receiver circuitry. Hence, there is a delicate balance in the gain distribution between the LNA and RF mixer on the one hand and their noise and linearity contributions on the other hand.

Table 6-1 summarizes the RF specifications for the various blocks of the RF receiver and the overall receiver performance when operating in the IEEE 802.15.4 mode. As shown, the cumulative voltage gain in the receiver is 85dB. The input-referred (IR) thermal noise PSD

and the input-referred flicker noise corner are shown for each block in the RF signal chain. The IR thermal noise PSD quoted in the table does not take into account the thermal noise of the source impedance of the preceding blocks, hence voltage gain rather than power gain is considered in this analysis. The ADC has 6-bit resolution with a 37.5mV LSB and 13MHz sampling frequency; this translates to a noise power spectral density (NPSD) of approximately -107.4dBV_{rms}/Hz. The OCL DAC is implemented as a third-order sigma-delta DAC whose simulated in-band thermal noise PSD is approximately -154dBV_{rms}/Hz. The cumulative IR thermal noise PSD at the RF receiver's balun input is -177.8dBV_{rms}/Hz which is equivalent to a thermal noise figure of 9.2dB relative to -186.9dBV_{rms}/Hz, or -173.97dBm/Hz, which is the *kT* noise at the receiver's antenna input, where *k* is the Boltzman constant and *T* is 290K.

Parameter	Unit	Balun	LNA	Mixer	OCL DAC	LPF	PGA	ADC
Voltage Gain	dB	-1	23	15	0	24	24	0
Cumulative Voltage Gain	dB		22	37	37	61	85	85
IR Thermal Noise PSD	dBV_{rms}/Hz	-186.8	-177.6	-161.0	-154.0	-149.0	-149.4	-107.4
Cumulative IR Thermal Noise PSD	dBV_{rms}/Hz	-177.8	-179.0	-158.6	-147.2	-148.1	-131.4	-107.4
Cumulative IR Total Thermal Noise Voltage	dBV_{rms}	-113.6	-114.9	-97.4	-86.0	-87.0	-70.3	-46.4
Cumulative IR Total Thermal + Flicker Noise Voltage	dBV_{rms}	-113.6	-114.9	-97.3	-85.7	-86.9	-70.2	-46.2
IIP3	dBV_{rms}		-16	-4.0				
Cumulative IIP3	dBV_{rms}	-27.9	-26.9	-4.0				
Receiver IIP3	dBm	**-12.9**						
Receiver Thermal NF	dB	**9.2**						

Table 6-1 Analysis of the RF specifications for the receiver signal chain blocks

The integrated noise in the analysis that led to Table 6-1 assumes a 15kHz high-pass filter corner due to the offset-correction loop in the RF receiver. The offset correction loop will be described in detail in Chapter 8. It can be seen that the difference between the cumulative IR

integrated thermal noise voltage and the cumulative IR integrated thermal and flicker noise voltage is negligible. This is primarily due to the very low flicker noise corner of the RF mixer facilitated by the use of a passive mixer. The cumulative integrated thermal and flicker noise voltage at the antenna (the balun input) amounts to -113.6dBVrms. The theoretical SNR requirement for an IEEE802.15.4 signal with a 10^{-3} BER is around -1dB due to the use of DSSS [27]. This translates to a theoretical RF receiver sensitivity of -101.6dBm. However, the receiver's demodulator is not ideal and requires 5dB of SNR. Hence, the expected sensitivity of the RF receiver is -95.6dBm. It can also be seen from the table that the RF mixer's IIP3 is -4dBVrms, which is 20dB higher than that of the LNA. However, the RF mixer's IR thermal noise PSD is approximately 17dB higher than that of the LNA. Overall, the receiver's IIP3 is -12.9dBm and its noise figure is 9.2dB. Considering the performance of individual circuits of the receiver, the noise figure and the IIP3 performance targets indicated in Table 6-1 exceed the system specifications outlined in sections 5.3.1 and 5.3.2 by 0.65dB and 3dB respectively.

Figure 6-2 shows a breakdown for the contributors to the receiver noise figure from the various receiver blocks. At 5dB, the LNA is the biggest contributor to the 9.2dB receiver noise figure, followed by the RF mixer at 2.16dB. The balun contributes a significant, yet unavoidable, 1dB to the noise figure due to its loss at 2.4GHz. Note that the balun is implemented using discrete components which also act as the matching network for the RF receiver. A balun with a lower loss can be used at the expense of increased system cost. The LPF of the receiver contributes 0.662dB to the noise figure, followed by the offset correction DAC, the ADC and the PGA.

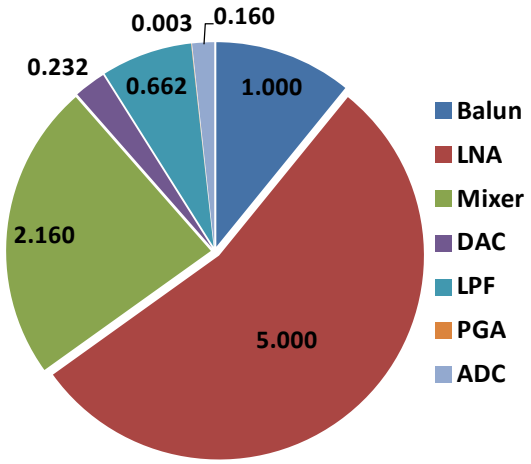


Figure 6-2 RF receiver noise figure contributions in dB from the receiver blocks

Figure 6-3 shows a voltage level diagram for a -92dBm desired signal, a -40dBm 5MHz blocker signal a -27dBm 13MHz blocker signal at the input of the RF receiver. Also shown is the integrated output-referred (OR) thermal noise voltage along the signal chain while the receiver is operating in the IEEE 802.15.4 mode. Since the ADC sampling rate is 13MHz, a 13MHz blocker is considered here to show the effect of the receiver's ADC sampling image. The signal and blocker levels were chosen at the limits of the receiver's noise figure and filtering performance. The voltage levels are shown in dBV_{rms} at the outputs of the individual blocks of the RF receiver. The desired signal and the blockers are received at the antenna and, after 1dB attenuation through the balun, are amplified by the LNA and mixer. It can be noted from the figure that the mixer raises the 13MHz blocker level to a level of about $-3.5dBV_{rms}$ at its output, while amplifying the desired signal level to $-68.51dBV_{rms}$. This is attributed to the relatively high output 1-dB compression point of the mixer of $11dBV_{rms}$.

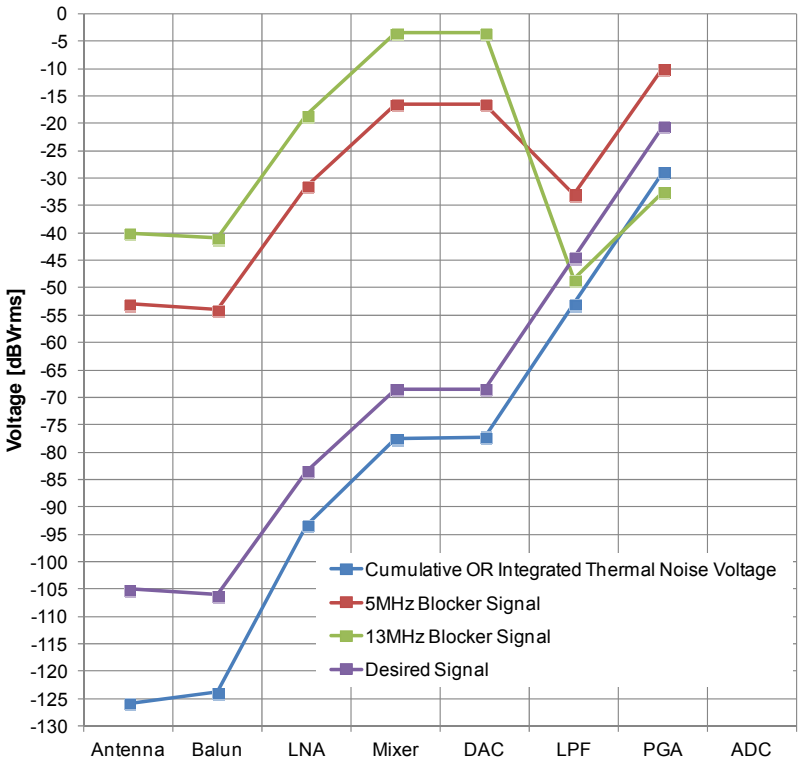


Figure 6-3 Voltage level diagram for the desired signal, a 5MHz blocker signal and a 13MHz blocker signal through the signal chain

The receiver's LPF and PGA attenuate the 5MHz and 13MHz blockers after being down-converted to the base-band by the RF mixer. The receiver's LPF has the function of both a channel filter and an anti-aliasing filter. The LPF has an attenuation of 69dB at a frequency of 13MHz, to prevent interferers from being aliased into the signal band by the ADC. At a frequency of 5MHz, corresponding to the adjacent channel, the LPF has an attenuation of 40dB in order to prevent interferers at that frequency from saturating the ADC. At the output of the PGA, the 13MHz blocker is attenuated by a further 8dB which places it 3.6dB below the output-referred integrated thermal noise voltage at the PGA output. Hence, a blocker at the sampling image of the ADC of a level up to -27dBm at the receiver's antenna input will cause negligible degradation to the SNR of the desired signal being received. At the ADC's input, the SNR for the desired signal is around 8.4dB which is sufficient for the receiver's demodulator while the 5MHz blocker level is about -10dBV_{rms} (0.45V_{pk}) which is well within the ADC's dynamic range.

6.2 RF Front-End Implementation

This section focuses on the implementation of the RF front-end, specifically, the implementation of the RF mixer. As discussed in section 6.1.2, the RF mixer sets the entire dynamic range for the receiver. Hence, it is imperative to focus on examining the design choices for this circuit block.

6.2.1 Transistor Behaviour in a 0.18µm CMOS Process

The transceiver IC is implemented in a 0.18µm CMOS process. The process selection was based on considerations of cost, leakage and digital gate density. Short-channel effects have a non-negligible effect on the transistor performance in this process. Hence, using well-known square-law transistor formulae to predict the performance is not sufficiently accurate.

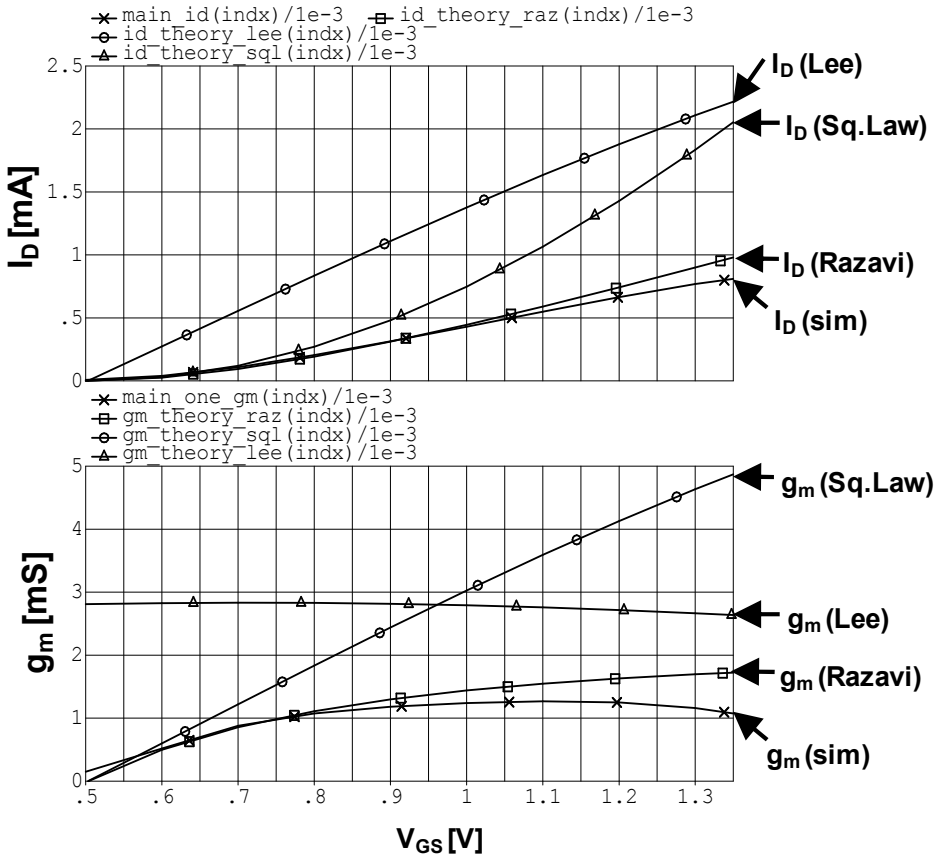


Figure 6-4 Comparison between the theoretical and simulated I_D-V_{GS} characteristics for a 2.5µm × 0.18µm NMOS transistor in the saturation region

Figure 6-4 shows a comparison between the theoretical and simulated drain current, I_D, and transconductance, g_m, versus the gate-source voltage, V_{GS}, for a 2.5µm × 0.18µm NMOS transistor in the saturation region with a drain-source voltage, V_{DS}, of 0.9V according to the formulae given by equations (6.1) to (6.6):

$$I_{D,razavi} = \frac{1}{2}\mu_{eff} C_{ox} \frac{W}{L}\left(V_{GS} - V_{th}\right)^2 \left(\frac{1}{1 + \frac{\left(V_{GS} - V_{th}\right)}{E_{sat} L}} \right) \tag{6.1}$$

$$g_{m,razavi} = \frac{I_{D,razavi}}{V_{GS} - V_{th}} \left(1 + \frac{1}{1 + \frac{\left(V_{GS} - V_{th}\right)}{E_{sat} L}} \right) \tag{6.2}$$

$$I_{D,lee} = \frac{1}{2}\mu_{eff} C_{ox} W \left(V_{GS} - V_{th}\right) E_{sat} \tag{6.3}$$

$$g_{m,lee} = \frac{1}{2}\mu_{eff} C_{ox} W E_{sat} \tag{6.4}$$

$$I_{D,sql} = \frac{1}{2}\mu_{eff} C_{ox} \frac{W}{L}\left(V_{GS} - V_{th}\right)^2 \left(\frac{1}{1 + \theta\left(V_{GS} - V_{th}\right)} \right) \tag{6.5}$$

$$g_{m,sql} = \frac{2 I_{D,sql}}{V_{GS} - V_{th}} \left(1 - \frac{0.5 \times \theta\left(V_{GS} - V_{th}\right)}{1 + \theta\left(V_{GS} - V_{th}\right)} \right) \tag{6.6}$$

where, $I_{D,razavi}$, $I_{D,lee}$ and $I_{D,sql}$ are the drain currents according to Razavi [3], Lee [40] and the square law models respectively, $g_{m,razavi}$, $g_{m,lee}$ and $g_{m,sql}$ are the transconductances according to Razavi [3] , Lee [40] and the square law models respectively. μ_{eff} is the MOS transistor's effective mobility obtained from the circuit BSIM4 simulator, which takes into account the dependency of the transistor's intrinsic mobility on the gate-source voltage, C_{ox} is the MOS transistor gate oxide capacitance per unit area, W is the transistor width, L is the transistor length, V_{GS} is the transistor gate-source voltage, V_{th} is the transistor threshold voltage and Θ is a fitting parameter roughly equal to $10^{-7}/t_{ox}$ where t_{ox} is the oxide thickness [41]. Short channel effects are non-negligible when the ratio of $V_{GS} - V_{th}/L$ to E_{sat} is high enough such that the

drain current ceases to depend on the channel length as indicated by (6.3). The primary short channel effect is velocity saturation which occurs when the carrier velocity in the MOS transistor channel ceases to increase with an increasing electric field. Velocity saturation is quantified by the saturation electric field, E_{sat}, which is defined as the field strength at which the transistor carrier velocity drops to one half the value extrapolated from the low-field mobility region [40].

It can be seen from Figure 6-4, that the square-law relationship between I_D and V_{GS} does not accurately predict the transistor *I-V* characteristics. Hence, theoretical analysis of I_D and g_m has to take account of the short-channel effects in this process. The most accurate formulae for I_D and g_m are those predicted by Razavi [3].

Note also form Figure 6-4 that the relationship between I_D and V_{GS} at higher V_{GS} is more linear than what the traditional square law predicts; this offers the possibility of designing more linear circuits in this particular 0.18µm process compared to other processes with a higher feature size. Short-channel effects also translate into the possibility of the transistor entering the saturation region at a lower value of the drain-source voltage, $V_{DS,SAT}$, due to velocity saturation. Nevertheless, short-channel effects are not all beneficial. For example, the transistor efficiency, g_m/I_D, can be quite low and hot carriers at high values of V_{DS} can cause a reduction in the transistor output impedance [3].

Figure 6-5 shows the g_m, I_D and g_m/I_D parameters for the RF and base-band (BB) models of a 2.5µm × 0.18µm NMOS transistor in a common-source/diode-connected-load configuration with 8, 16 and 32 stripes and a supply voltage of 1.8V. The diode-connected load transistor is connected to the supply and has the same dimensions as the common-source transistor. The figure serves as a guide for biasing the transistors used in the design for a specific V_{GS}. Note that the RF and BB models of the transistor are quite close in terms of their DC parameter

prediction which suggest that the RF model is accurate at DC (this is typically done as a sanity check on the RF model). It can also be seen from the figure that the transistor is most efficient in terms of its g_m/I_D ratio in the region of moderate inversion, i.e. when V_{GS} is close to the threshold voltage, V_{th}, of the transistor. This is interesting for low power design, since it is important to get the maximum transconductance of the transistor at the lowest possible drain current. Figure 6-6 shows the transit frequency, f_t, and current density, I_D/W, versus V_{GS} for a 2.5µm × 0.18µm NMOS transistor with 8, 16 and 32 stripes using the RF transistor model. The figure shows that an NMOS transistor on this process is capable of achieving an f_t of about 25GHz with a current density of 25µA/µm. Hence, we can conclude that this process is suitable for our receiver operating at 2.4GHz, as well as the frequency synthesizer's VCO operating at 4.8GHz given its capability of operating at such high frequency with a relatively low current density.

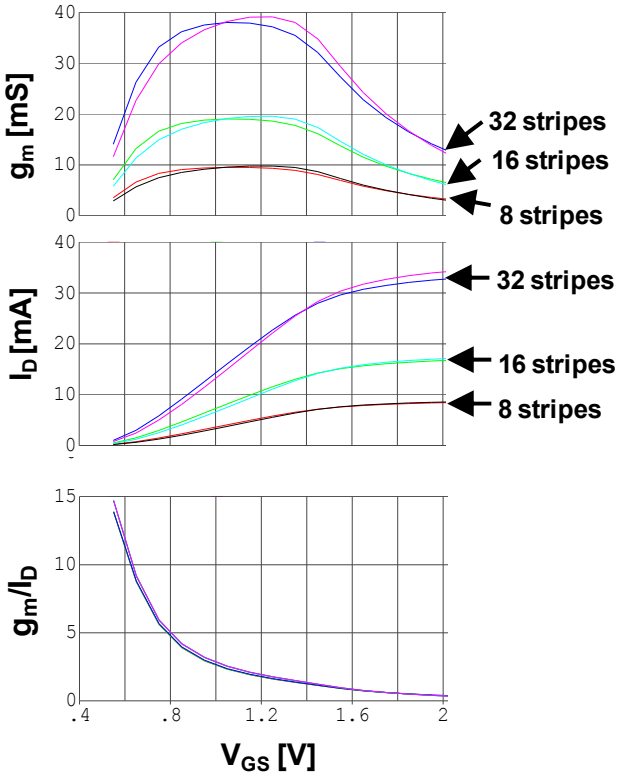


Figure 6-5 2.5µm × 0.18µm NMOS transistor parameters (g_m, I_D and g_m/I_D) versus V_{GS} for 8, 16 and 32 stripes (RF model and BB model depicted)

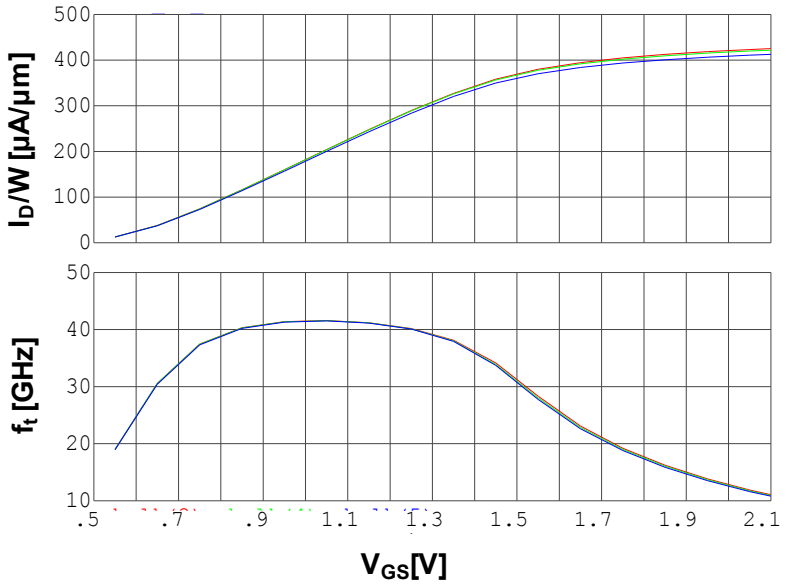


Figure 6-6 2.5µm × 0.18µm NMOS transistor parameters (f_t and I_D/W) versus V_{GS} for 8, 16 and 32 stripes using the RF transistor model

6.2.2 Introduction to RF Mixers

In this section, we will detail the circuit design of the RF mixer. A brief comparison between the most commonly used circuit architectures of the RF mixer will be introduced, followed by the details of the design adopted for this work.

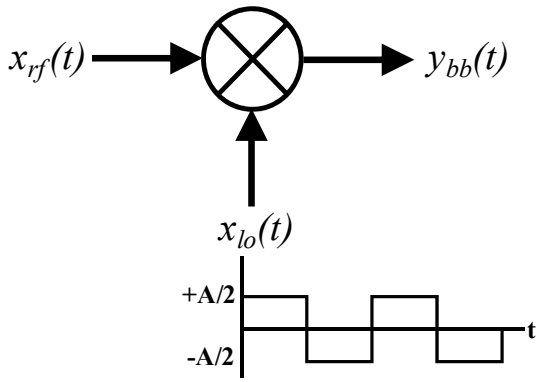


Figure 6-7 Principle of an RF mixing operation

Figure 6-7 shows an RF mixer which operates on the principle of periodic switching using a switching signal called the local-oscillator (LO). The LO signal, $x_{lo}(t)$, is a square wave which can be decomposed using Fourier series as:

$$x_{lo}(t) = \frac{4A}{\pi}\left[\cos(\omega_{lo}t) + \frac{1}{3}\cos(3\omega_{lo}t) + \frac{1}{5}\cos(5\omega_{lo}t) + \ldots\right] \quad \textbf{(6.7)}$$

The output of the mixer, $y_{bb}(t)$, is given by:

$$y_{bb}(t) = G \cdot x_{rf}(t) \cdot x_{lo}(t), \quad \textbf{(6.8)}$$

where, G is the intrinsic conversion gain of the RF mixer. Multiplication of two signals in the time domain is equivalent to convolution in the frequency domain. Hence, for $A=1$,

$$Y_{bb}(\omega) = \frac{G}{2\pi}\int_{-\infty}^{+\infty} X_{rf}(\omega - \Omega) \cdot X_{lo}(\Omega) \cdot d\Omega, \quad \textbf{(6.9)}$$

where,

$$X_{lo}(\omega) = \frac{4}{\pi}\left[\pi \cdot \delta(\omega \pm \omega_{lo}) + \frac{1}{3}\pi \cdot \delta(\omega \pm \omega_{lo}) + \frac{1}{5}\pi \cdot \delta(\omega \pm \omega_{lo}) + \ldots\right]. \quad \textbf{(6.10)}$$

This yields,

$$Y_{bb}(\omega) = \frac{2G}{\pi}\left[X_{rf}(\omega \pm \omega_{lo}) + \frac{1}{3}X_{rf}(\omega \pm 3\omega_{lo}) + \frac{1}{5}X_{rf}(\omega \pm 5\omega_{lo}) + \ldots\right]. \quad \textbf{(6.11)}$$

Based on equation (6.11), it can be seen that the RF mixer performs a frequency translation from the RF frequency, ω, to frequencies around the LO harmonics at $\omega \pm n\omega_{lo}$ where $n=1,3,5,\ldots$ The RF mixer employs a frequency selective circuit which typically selects one of the two side-bands at $\omega - n\omega_{lo}$ or $\omega + n\omega_{lo}$. For the RF receiver in this work, the side-band at $\omega - \omega_{lo}$ is is selected. Note also that, the conversion gain of an ideal mixer is given by $2/\pi$ or about -3.9dB for $G=1$. In the case of a receiver, equation (6.11) also indicates that the LO signal would mix the frequency content in the RF signal, $x_{rf}(t)$, around the harmonics of the LO down to the base-band frequency. This is an important point to keep in mind, especially when

performing noise analysis on the mixer. Theoretically, noise at the mixer's input will be translated by all LO harmonics to the mixer output; this is depicted in Figure 6-8.

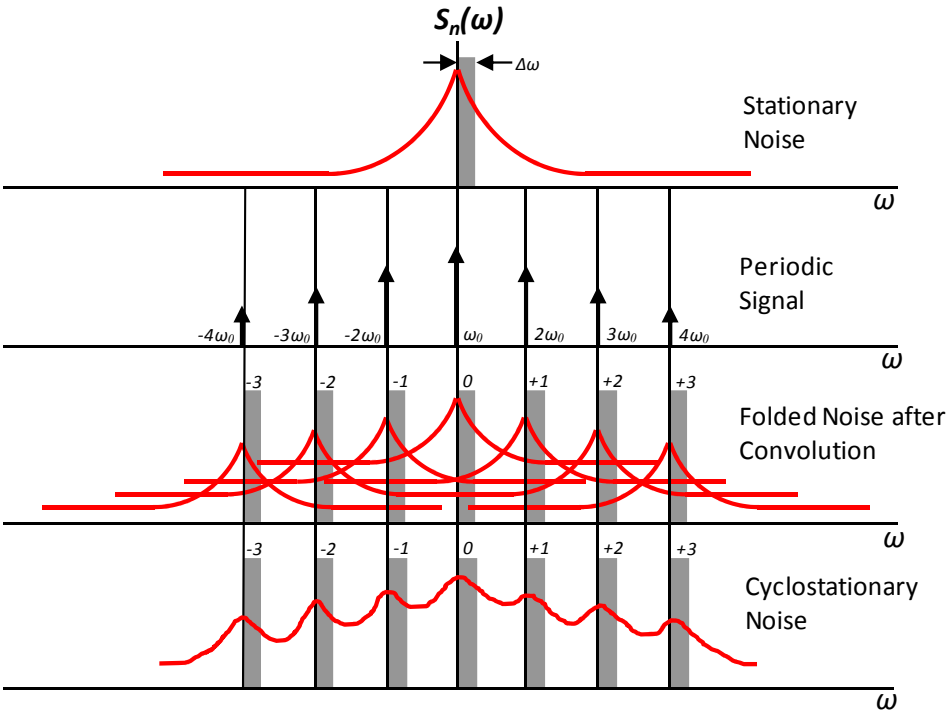


Figure 6-8 Noise folding in the presence of a periodic signal

Figure 6-8 shows the concept of noise folding in the presence of a periodic signal with a fundamental frequency, ω_o. A stationary noise source with an arbitrary spectrum is convolved with the fundamental of the periodic signal and its harmonics at $\pm 2\omega_o$, $\pm 3\omega_o$, $\pm 4\omega_o$ and so on. The convolution operation scales and translates the stationary noise to the sidebands (harmonics) of ω_o. In any given frequency band, $\Delta\omega$, the total noise is the summation of the noise contributions from sidebands, 0, ±1, ± 2 and ±3 and so on to this specific frequency band as shown in the figure. Based on Figure 6-8, the noise at the output of the mixer can be expressed as:

$$S_{bbn}(\omega) = \sum_{k=-\infty}^{+\infty} |a_k|^2 S_{rfn}(\omega + k\omega_{lo}), \qquad \textbf{(6.12)}$$

where, $S_{bbn}(\omega)$ is the noise power spectral density at the base-band output, $S_{rfn}(\omega)$ is the noise power spectral density at the RF input, and a_k is given by:

$$a_k = \frac{2}{k\pi}, \text{ where } k = -\infty,...,+\infty \quad \textbf{(6.13)}$$

From the foregoing discussion, it is critical to take into account frequency translations performed by the LO signal on the RF signal itself, as well as noise present at the RF input and within the mixer. Simulations using small-signal AC and noise analysis cannot be used to predict an RF mixer's performance since they do not capture such frequency translations. On the other hand, RF simulators such as SpectreRF by Cadence can be used to predict the noise, conversion gain and linearity of RF mixers using periodic steady state (PSS) and periodic noise simulations. It is also worth pointing out that RF mixer can be a time-varying circuit in the presence of noise which modulates the zero crossing instants of the LO signal. This adds to the need for advanced RF simulators for this type of circuit to predict its performance correctly.

One might argue the need of using a square wave for the LO, especially if it causes such undesirable frequency translations. A sinusoidal LO could be a better choice. The use of an ideal square wave is essentially an approximation for the LO signal. However, as will be highlighted in subsequent sections, in practical circuit implementations, it is desirable to use a large LO signal with very small rise and fall times to be able to turn on and off the RF mixer switches in a very short period of time. This translates into an improved conversion gain, noise and linearity performance for the RF mixer. Hence, a model with a square wave best approximates the practical case.

6.2.3 Active RF Mixers

Two common RF mixer architectures were considered for the RF receiver; an active double-balanced mixer and a double-balanced passive-mixer. Recall that the main challenges with a ZIFR lie in the competition of flicker noise with the received signal since they are both

present around DC. In addition, the RF receiver of this work aspires for the best-in-class blocker rejection which translates to the need for an RF mixer with the highest possible linearity.

Figure 6-9 shows the schematic diagram of a double-balanced active RF mixer. A double-balanced mixer refers to having both differential RF and differential LO paths. Differential paths are commonly used in IC design for better rejection against spurious coupling to the RF inputs, voltage supply variations and any common-mode circuit noise in general. A double-balanced mixer also ideally cancels all even harmonics at the mixer output and doubles all odd harmonics including the desired signal. In addition, double-balanced mixers have traditionally been used in IF receivers where the output of the mixer is at a high frequency IF rather than at base-band. In this case, the double-balanced architecture cancels any LO harmonics at the IF outputs, which is critical for IF receivers since the stages following the mixer in the receiver could saturate as a result of the LO appearing at the mixer output. The LO could also mix with undesired signals and down-covert those signals to the IF stage following the mixer.

The active mixer shown in Figure 6-9 uses a differential amplifier stage for the RF input which is biased by the current source implemented using the transistor M_B. For low voltage supplies, this current source transistor ceases to provide the necessary common-mode rejection it is intended for due to low voltage headroom. The load of the active mixer is formed by the parallel network of R_L and C_L. The load capacitor, C_L, is used to filter undesired components at the mixer output and in some cases form the first pole of the LPF stage of the receiver.

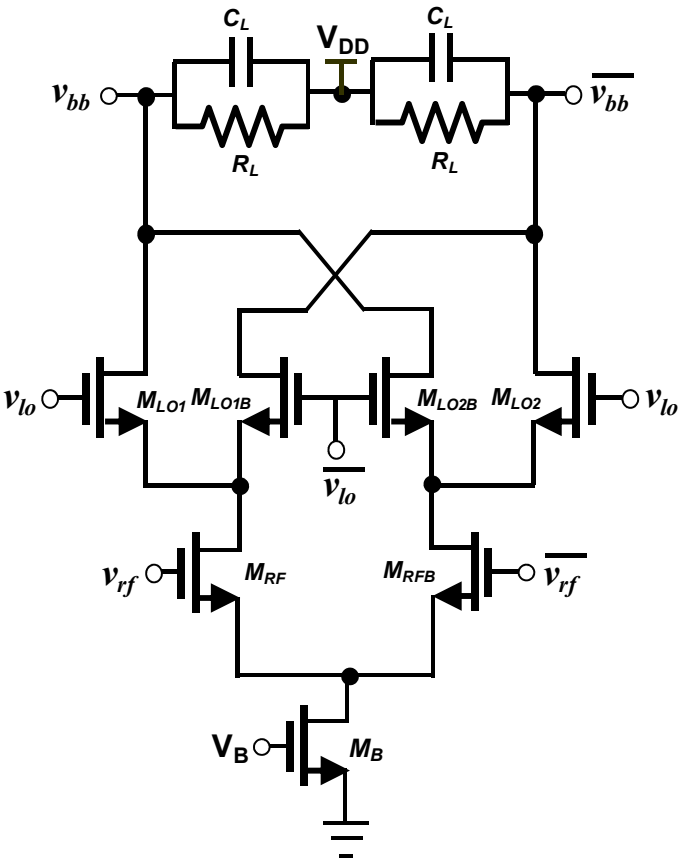


Figure 6-9 Double-balanced active RF mixer

The active RF mixer circuit of Figure 6-9 performs three main functions; the differential amplifier formed by M_{RF}, M_{RFB} and M_B converts the RF signal into an RF current based on the RF transconductance, g_m, of transistors M_{RF} and M_{RFB}. The RF current is down-converted to the base-band frequency using switches M_{LO1}, M_{LO1B}, M_{LO2} and M_{LO2B} which are driven by the LO signal. The load resistor R_L converts the base-band current into a base-band voltage which drives the following stage in the receiver path. For an RF input, $V_{rf}(\omega)$, the differential RF current from the transconductance stage is given by:

$$I_{rf}(\omega) = g_m \cdot V_{rf}(\omega) \tag{6.14}$$

Using equation (6.11), the output signal, $V_{bb}(\omega)$, at low frequencies, when down-converted by the LO signal fundamental at, ω_{lo}, is given by:

$$V_{bb}(\omega) = \frac{2}{\pi} \cdot g_m \cdot R_L \cdot V_{rf}(\omega - \omega_{lo}) \tag{6.15}$$

Hence, the conversion gain of this active mixer at DC is given by:

$$A_{vc,active} = \frac{2}{\pi} \cdot g_m \cdot R_L \quad \textbf{(6.16)}$$

The mixer conversion gain will have a first order low-pass characteristic determined by R_L and C_L. The reader should note that the conversion gain in equation (6.16) assumes that the LO switches are perfectly switched by the LO ideal square wave signal. However, this is not the case in practice where the non-zero rise and fall times for the LO signal will reduce the conversion gain somewhat below that predicted by (6.16).

In [42], Darabi *et al.* provide a comprehensive noise analysis for the active mixer shown in Figure 6-9. The paper shows that flicker noise at the output of an active mixer appears from all three stages of the mixer; the mixer input transconductance, the mixer switches and the mixer load as follows:

1. *Flicker noise due to the active mixer's load*. Poly-silicon resistors available on the 0.18μm process have very low flicker noise and can be used as a load for the active mixer. However, one might use a PMOS diode-connected load, for example, to reduce the voltage headroom required by the resistor. In this case, the PMOS load will contribute to the flicker noise at the mixer's output.
2. *Flicker noise due to LO switching*. This appears through one of two mechanisms:
    a. *Flicker noise of the LO switches*, $V_{n,flicker,sw}$, can be modeled by a noise voltage source at the inputs of the switches. This noise source randomly modulates the zero-crossing instants of the LO waveform, producing noisy current pulses at twice the LO frequency. The height of the pulses is approximately equal to twice the bias current of the mixer, I_B. The width of the pulses is modulated by the noise at the input of the LO switches. For a sinusoidal LO waveform of slope *S*, the average of these current pulses at the mixer output produces a low frequency noise current component without any frequency translation and is given by:

$$i_{n,flicker,0} = 4I_B\omega_{lo} \cdot \frac{V_{n,flicker,sw}}{2\pi \cdot S} \quad \textbf{(6.17)}$$

Flicker noise due to the LO switches also appears at the mixer output via another mechanism which depends on the LO frequency, ω_{lo}, the LO switch transconductance g_{msw}, and the parasitic capacitance at the common source node of the LO switches, C_p. The output flicker noise current in this case is given by [42]:

$$i_{n,flicker,1} = 2C_P \frac{\omega_{lo}}{2\pi} V_{n,flicker,sw} \cdot \frac{(C_p\omega_{lo})^2}{g^2_{msw} + (C_p\omega_{lo})^2} \quad \textbf{(6.18)}$$

Hence, it can be concluded from equations (6.17) and (6.18) that, to reduce the flicker noise contribution from the LO switches of an active mixer, one has to reduce the flicker noise of the switches themselves; this corresponds to using PMOS rather than NMOS devices for the switches and/or using larger LO switches, thereby requiring greater power consumption in the LO buffers driving those switches. One can also reduce the flicker noise contribution from the LO switches by using an LO signal with a very high slope, S, at the zero-crossing instants; this corresponds to a larger amplitude for a sinusoidal LO. Nevertheless, even if the LO signal is a square wave with negligible rise and fall times, flicker noise would still appear at the output of the mixer due to the LO switches because of the parasitic capacitance, C_p, as indicated by (6.18). In general, to reduce the flicker noise for an active RF mixer due to the flicker noise of the LO switches, the LO frequency has to be kept low and the switching waveform should have very small rise and fall times.

b. *Flicker noise originating in the RF transconductance devices.* This flicker noise leaks through the switch transistors when they are unbalanced by a DC offset. Assuming that the LO signal is a sinusoid, this DC offset causes current pulses in the switches at the zero-crossing instants of the LO signal.

The height of these current pulses is modulated by the flicker noise of the transconductor. According to [42], the flicker noise current appearing at the output of the mixer is given by:

$$i_{n,flic\ \mathrm{ker},2} = \frac{1}{\pi A} \cdot g_m \cdot V_{n,flic\ \mathrm{ker},gm} \cdot V_{os,lo} \qquad \textbf{(6.19)}$$

where, A is the amplitude of the sinusoidal LO signal, $V_{n,flicker,gm}$ is the flicker noise of the transconductance and $V_{os,lo}$ is the DC offset of the LO switch transistors. Flicker noise at the mixer output due to this mechanism may be eliminated if the LO waveform is a perfect square-wave with infinite slope at zero crossing. However, as the LO slope rises, the flicker noise mechanism described in (6.18) becomes more important.

6.2.4 Passive RF Mixers

Based on the foregoing analysis, it can be observed that if there is no DC current in the LO switching devices of the active mixer then there will be no flicker noise associated with these devices [43]. In other words, with $V_{n,flicker,sw}=0$ in equations (6.17) and (6.18) there is no flicker noise that would appear at the mixer output. In addition, in the absence of a DC current path between the RF transconductor and the LO switches, the flicker noise mechanism described by (6.19) due to the RF transconductor is suppressed. Typically, the RF transconductor is AC-coupled to the passive mixer's LO switches. This provides no DC current path between the RF transconductor and the LO switches.

The absence of a DC current in the LO switches and in the path between the RF transconductor and the LO switching transistor is *the* key feature that a passive RF mixer possesses, and is one of the main reasons it has gained significant popularity in the implementation of a ZIFR in recent publications [44]-[45]. There are two types of passive mixers depending on how its RF input is driven. Voltage-commutating passive mixers are

driven by an RF voltage signal where the driving impedance is relatively low while current-commutating passive mixers are driven by an RF current signal where the driving impedance is relatively high.

6.2.4.1 Current-Commutating RF Passive Mixers

For this work, the RF receiver's base-band signal chain operates in the voltage domain. Hence, the output from the passive mixer needs to be in the voltage domain at some point in the signal path before the base-band input, more specifically before the LPF. This is typically accomplished using an OTA with a resistive or a resistive-capacitive (RC) feedback network. If a voltage-commutating passive mixer is used, the switches in the passive mixers will act as an RF V-to-I converter and the feedback network of the OTA will act as an I-to-V converter. This leads to two main challenges:

1. The RF V-to-I conversion performed by the switches of the passive mixer places significant linearity requirements on these switches. This translates to the need for a larger switch size, a larger over-drive voltage or a combination thereof in order to reduce the intrinsic non-linearity of the switch [46]. Having a larger switch or a larger overdrive voltage translates to the need for a larger LO amplitude, which typically dominates the power consumption of the passive mixer, especially at 2.4GHz, and consequently raises the power consumption of the RF receiver significantly.
2. The low-frequency gain of the passive mixer will be set by the ratio between the feedback resistor of the OTA and the on-resistance of the passive mixer. In this case, the type of resistors used to set the gain of the passive mixer is different; the feedback resistor is typically a poly-silicon resistor and the passive mixer's on-resistance is set by a MOS switch resistance. This means that the voltage gain of the passive mixer will be subject to process, temperature and voltage variations with no straightforward means of keeping this gain constant; this is undesirable for an RF receiver since it introduces AGC errors.

Based on the foregoing discussion, avoiding the RF V-to-I conversion in the voltage-commutating passive mixer's switches is the desirable design choice especially from the point of view of power consumption which is one of the most critical design aspects of this work. This design choice motivates the use of a current-commutating passive mixer design. A current-commutating passive mixer is driven by an RF current signal which can be either generated directly by the LNA or by a separate RF transconductance stage. In either case, the LNA or a separate RF transconductance act as a V-to-I converter at the passive mixer input.

Current-commutating passive mixers alleviate the main challenges highlighted for the voltage-commutating mixers by considering the following:

1. Current-commutating passive mixers save power consumption in the LO driver circuitry since the mixer switches can be made relatively small due to the relaxation of the linearity constraints imposed on them by avoiding their use in RF V-to-I conversion. The linearity of the RF V-to-I conversion in the LNA or in a separate RF transconductance is typically determined by the over-drive voltage of the MOS transistors in the differential amplifier implementing the V-to-I conversion. The power consumption needed for this V-to-I conversion is substantially less than the LO driver whose power consumption is dominated by the switching power of CV^2f, where C is the load of the LO driver, V is the supply voltage and f is the switching frequency. For example, a 20% increase in the capacitance, C, driven by the LO translates into a 20% increase in its power consumption. Being the dominant contributor to the power consumption of the RF receiver, as will be shown in subsequent sections, a 20% increase in the LO driver's power consumption is substantial.
2. The passive mixer's low-frequency gain is determined by the product of the transconductance of the RF V-to-I conversion stage, g_{mrf}, and the resistive feedback, R_{fb}, of the OTA which performs the I-to-V conversion. This gain can be made relatively constant across process, temperature and voltage variations by using a

constant-g_m biasing circuit for the RF transconductance stage. This biasing circuit sets the value of the RF transconductance, g_{mrf}, to approximately $1/R_{fb}$, thereby, keeping the product $g_{mrf} \cdot R_{fb}$ relatively constant in the presence of process, temperature and voltage variations.

Figure 6-10 shows the current-commutating double-balanced passive mixer used in this work's ZIFR. The RF mixer is driven by a dual-input common-gate LNA with an inductive load [1]. The LNA drives both the I- and Q-paths of the double-balanced RF mixers. The I-path mixer is shown in detail in the figure. The passive mixer's LO switches are driven by the RF current output of an RF transconductor G_m. The LNA could have been used to drive the passive mixer directly and act as its V-to-I conversion stage. However, since a ZIFR is used, LO leakage to the LNA input needs to be minimized. This would not be the case if the LNA drives the passive mixer's switching core directly. In this case, the LO signal can couple to the LNA output due to imbalances in the RF mixer and in turn couple to the LNA input. Hence, a separate RF transconductor acts as a buffering stage between the LNA and the switching core of the RF mixer, thereby minimizing LO coupling to the LNA input.

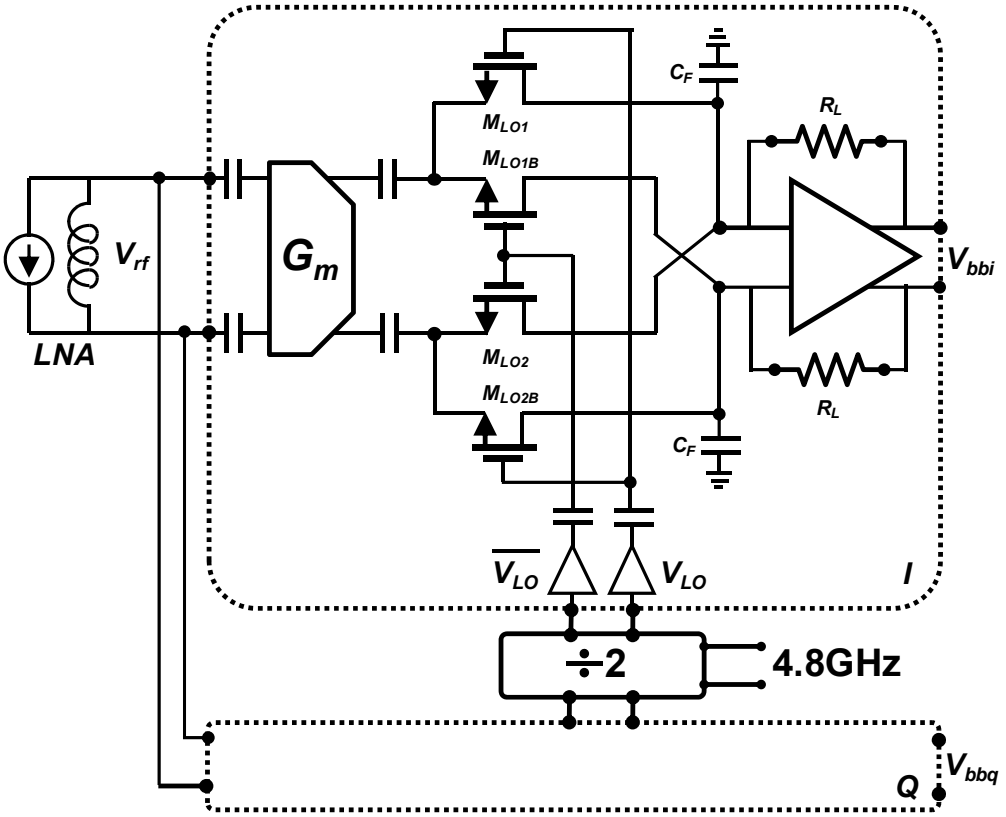


Figure 6-10 Double-balanced passive mixer circuit used in this work (DC biasing details are not shown)

In order to separate the DC biasing points of the input and output of the RF transconductor from the LO switches, the RF transconductor is AC-coupled to the mixer's LO switches M_{LO1}, M_{LO1B}, M_{LO2} and M_{LO2B}. The input of the RF transconductor is also AC-coupled to the LNA output. The quadrature LO is generated using a divide-by-2 frequency divider whose input is the 4.8GHz VCO signal; the design details of the quadrature generation circuit will be discussed in section 6.2.5. The base-band current of the passive mixer is converted to a base-band voltage using a trans-impedance amplifier (TIA) which is implemented using a two-stage OTA with a feedback resistor, R_L. The capacitors denoted by C_F in Figure 6-10 are used to reduce the input impedance of the TIA at the LO frequency and its harmonics. Reducing the input impedance of the TIA eliminates any signal swing at its virtual grounds at the high frequencies of the LO and its harmonics. Eliminating the signal swing at the virtual ground

nodes of the TIA avoids degrading the linearity of the mixer by eliminating any high frequency signal swing at the drain and source nodes of the LO switches of the passive mixer.

The passive mixer in the Q path is identical to that of the I path with the exception of being driven with the quadrature phase of the LO. Overall, the passive RF mixer circuit of Figure 6-10 performs three main functions; the differential transconductance converts the RF signal into an RF current based on the RF transconductance, g_m. The RF current is down-converted to the base-band frequency using switches M_{LO1}, M_{LO1B}, M_{LO2} and M_{LO2B} which are driven by a quadrature LO signal. The TIA feedback resistor R_L converts the base-band current into a base-band voltage which drives the following stage in the receiver path. For an RF input, $V_{rf}(\omega)$, the differential RF current from the transconductance stage is given by:

$$I_{rf}(\omega) = g_m \cdot V_{rf}(\omega), \tag{6.20}$$

Using equation (6.11), the output signal, $V_{bb}(\omega)$, at low frequencies, when down-converted by the LO signal fundamental at, ω_{lo}, is given by:

$$V_{bb}(\omega) = \frac{2}{\pi} \cdot g_m \cdot R_L \cdot V_{rf}(\omega - \omega_{lo}) \tag{6.21}$$

Hence the conversion gain of this passive mixer at DC is given by:

$$A_{vc,passive} = \frac{2}{\pi} \cdot g_m \cdot R_L \tag{6.22}$$

Owing to its current-commutating operation, the conversion gain of a double-balanced passive mixer, given by (6.22), is identical to the conversion gain of an active mixer given by (6.16). The reader should note that the conversion gain of an active mixer, as given by (6.16), or that of a passive mixer, as given by (6.22), assumes that the LO switches are perfectly switched by the LO ideal square wave signal. However, this is not the case in practice. In [47] Zhou *et al.* provide some insight into the case assuming a non-ideal square wave LO. Although the analysis is provided for voltage-commutating passive mixers, it is relevant to note that the conversion gain of an ideal voltage-commutating mixer is given by $1/\pi \cdot T_{lo}/\Delta T_{lo} \cdot \sin(\pi \cdot \Delta T_{lo}/T_{lo})$ where T_{lo} is the LO period and ΔT_{lo} is the on-time for the LO

signal; the off-time is T_{lo}-ΔT_{lo} . For example, for a mixer driven by an ideal square-wave LO, $\Delta T_{lo} = 0.5 \cdot T_{lo}$, and the conversion gain is $2/\pi$ or about -3.9dB. However, in a case with a non-zero rise and fall times for the LO signal, for example, $\Delta T_{lo} = 0.6 \cdot T_{lo}$, the conversion gain is about -5.9dB. Although this analysis was developed for voltage-commutating passive mixers and does not fully extend to current-commutating passive mixers, a similar observation can be made regarding the effect of the duty cycle of the LO signal on the conversion gain of current-commutating passive mixers.

6.2.4.2 Noise in Current-Commutating RF Passive Mixers

As discussed earlier, the key feature of passive RF mixers is the absence of a DC current in the LO switches and in the path between the RF transconductor and the LO switching transistors which should, at least theoretically, lead to the absence of flicker noise at the base-band output of the mixer. However, Redman-White *et al.* in [37] first noticed that flicker noise exists at the output of voltage-commutating passive mixers, even in the absence of DC current in the LO switches. Using periodic steady-state (PSS) simulations, Redman-White *et al.,* showed that flicker noise appears in MOS transistors in the presence of time-varying AC drain current even with a zero mean. In a passive mixer, the drain current in an LO switch transistor is the RF signal current which is typically small. However, the LO signal is a large signal which couples to the channel of the MOS transistors constituting the LO switches. This coupling occurs in the presence of any imbalance in the source-gate and drain-gate capacitances. It is through this coupling that a large time-varying drain current appears in the MOS transistors of the LO switches causing flicker noise to appear at the output of a passive mixer. Through simulations, Redman-White *et al.* verified their findings in [37].

In addition, Chehrazi *et al.*, [48] provided an insight into the mechanisms by which flicker noise appears at the output of voltage-commutating passive mixers in the absence of a DC current in the LO transistors. [48] postulates that input-referred flicker noise at the gates of the LO switches randomly modulates the instants of turn on and turn off of the switches when

they are driven by the LO signal. This causes random commutation of the *input* RF voltage signal through the LO switches by a train of pulses which is either periodic at $2 \cdot f_{lo}$ or f_{lo}. The rate of this train of pulses depends on the mode of operation of the LO switches in the on-overlap or the off-overlap modes respectively. These modes of operation will be illustrated shortly. The width of the train of pulses with a rate of $2 \cdot f_{lo}$ or f_{lo} is randomly modulated by the input-referred flicker noise at the gates of the LO switches. The height of the pulses is proportional to the input RF voltage signal. According to [48], as a result of the random commutation, the input-referred flicker noise at the gates of the LO switches translates to the output of the mixer at $f_{rf,fn}$, $2f_{lo} \pm f_{rf,fn}$, $4f_{lo} \pm f_{rf,fn}$, and so on, whereas the RF signal appears at $|f_{rf} - f_{lo}|$. f_{rf} is the frequency of the RF input signal and $f_{rf,fn}$ is the frequency of the RF input signal which translates the flicker noise at the gates of the LO switches to the mixer output. Hence, flicker noise will coincide with the signal at the output of the mixer if, for example, $f_{rf,fn}=f_{rf}$ and $f_{rf}=3f_{lo}/2$ where both the flicker noise and the signal appear at $f_{lo}/2$.Since the input-referred flicker noise at the gates of the LO switches is commutated with pulses whose height is proportional to the input RF voltage signal, the flicker noise voltage at the output of the mixer will be proportional to the input signal amplitude.

It is worth pointing out, based on [48], that the presence of a large blocker at the input of the RF mixer, for example at $f_{lo}+f_{rf}$ or $3f_{lo}-f_{rf}$, causes flicker noise to appear at $f_{lo}-f_{rf}$ or $f_{rf}-f_{lo}$ at the output of the mixer where $f_{rf,fn}$ in this case is equal to $f_{lo}+f_{rf}$ or $3f_{lo}-f_{rf}$. This means that a large blocker at the RF input of the mixer has the potential to translate the flicker noise at the gates of the LO switches to the same frequency of the down-converted signal at the mixer output. In the case of a blocker at $f_{lo}+f_{rf}$ or $3f_{lo}-f_{rf}$, the flicker noise is translated to $f_{lo}-f_{rf}$ or $f_{rf}-f_{lo}$ which is the same frequency at which the desired RF signal is down-converted. The flicker noise voltage at the mixer output, in this case, is proportional to the amplitude of the large blocker at the RF input which can potentially degrade the SNR of the signal being received at the mixer output.

The analysis carried out by Chehrazi *et al.* in [48] suggest that the flicker noise voltage at the output of a voltage-commutating passive mixer depends on the amplitude of the input signal to the mixer; if the input to the passive mixer is zero, there is no flicker noise at its output. This is a fundamentally different view from the one presented by Redman-White *et al.* in [37] which showed that flicker noise arises in a single MOS transistor due to AC currents circulating in that transistor. At the time of writing, no comprehensive analysis exists to formally resolve the differences between [37] and [48]. The author believes that both views have merits which should be considered in the design phase of a passive mixer.

It is worth pointing out that in [49], Chehrazi *et al.* extended their analysis to the current-commutating passive mixer architecture which is similar to that shown in Figure 6-10. In the case where the RF transconductor is AC-coupled to the LO switches, the flicker noise at the gates of the LO switches is translated to the mixer output only when a blocker is present at specific frequencies. Similar to voltage-commutating mixers, the flicker noise voltage at the mixer output is proportional to the amplitude of the large blocker at the RF input which can potentially degrade the SNR of the signal being received at the mixer output. For example, if there is a blocker with an amplitude, A_b, present at a frequency of $f_{lo}+f_{rf}$, the spectral density of the flicker noise voltage, translated to $f_{lo}-f_{rf}$ is given by[49]:

$$v_{n,fn,out}^2 \equiv \left(\frac{2g_m R_L A_b}{ST_{LO}} \right)^2 v_{n,fn,losw}^2 \qquad \textbf{(6.23)}$$

where, S is the slope of the LO signal, T_{LO} is the LO period, g_m is the RF transconductance, and $v_{n,fn,losw}^2$ is the spectral density of the flicker noise voltage at the gates of the LO switches.

There are two different modes of operation for the current-commutating RF passive mixer. These are depicted in Figure 6-11. In the figure, V_G is the DC bias voltage for the gates of the LO switches. As shown in Figure 6-10, the gates of the LO switches are driven by the

complementary LO signals, V_{LO} and $\overline{V_{LO}}$. The gates of the LO switches are AC-coupled to the local LO buffers driven by the VCO frequency divider. V_{CM} is the common-mode voltage of the drains and sources of the LO switches. This common-mode voltage is set to $V_{DD}/2$ by the common-mode feedback loop of the transimpedance amplifier's OTA where V_{DD} is 1.8V in this design. V_{th} is the threshold voltage of the LO switch transistors. The LO switches turn on during the time when V_{LO} and $\overline{V_{LO}}$ is greater than $V_{CM}+V_{th}$. Figure 6-11shows two modes of operation assuming that the LO amplitude is greater than $|V_{CM}+V_{th}-V_G|$. The first mode (a) is one in which $V_G < V_{CM}+V_{th}$. In this mode, there is a period of time in which LO switches M_{LO1} and M_{LO1B} are simultaneously off. This mode is called the *off-overlap* mode. The second mode (b) is one in which $V_G > V_{CM}+V_{th}$. In this case, there is an interval during which LO switches M_{LO1} and M_{LO1B} are simultaneously on. This case is called the *on-overlap* mode. These two modes of operation also apply to LO switches M_{LO2} and M_{LO2B}.

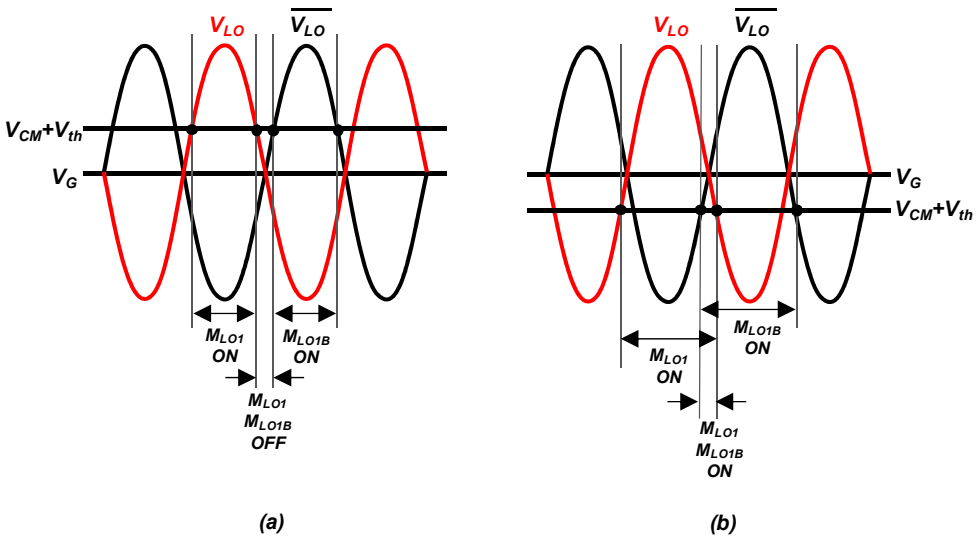


Figure 6-11 Modes of operation of a current-commutating RF passive mixer. (a) off-overlap mode and (b) on-overlap mode

The mode of operation (on-overlap or off- overlap) of the passive mixer has an effect on the mechanism by which thermal noise from the LO switches appear at the mixer's output. According to [49], there are two mechanisms for the thermal noise of the LO switches to

appear at the mixer output; a direct and an indirect mechanism. Noise contribution in the direct mechanism occurs during the period of time when two LO switches, for example, M_{LO1} and M_{LO1B} in Figure 6-10, are on in an on-overlap mode as shown in Figure 6-11 (b). If one of the LO switches is off, it obviously contributes no noise, and neither does the other switch that is on, assuming the mixer is driven by an ideal RF transconductance with infinite impedance, because the noise current from the single switch that is on has no return path to ground. Therefore, differential noise rather than single-ended noise appears at the mixer output due to the LO switches when they are in an on-overlap mode. The spectral density of the differential thermal noise voltage at the mixer output, due to the thermal noise of the LO switches, is given by:

$$v_{n,therm,losw,direct}^2 = \frac{32 \cdot 4KT\gamma}{3 \cdot ST_{LO}} \cdot \beta V_{eff}^2 \cdot R_L^2, \quad \textbf{(6.24)}$$

Where, S is the slope of the LO signal, T_{LO} is the LO period, γ is the excess noise factor of the transistor, $\beta=\mu C_{ox}W/L$ where μ is the transistor's channel mobility, C_{ox} is the transistor's gate oxide capacitance, W is its width and L is its length and $V_{eff} = V_G-V_{CM}-V_{th}$. From (6.24), it can be seen that increasing the W/L of the LO switches results in an increased noise voltage at the mixer output. This can be explained by observing that as the W/L of the LO switch increases, its on-resistance decreases and hence its noise current increases, resulting in an increased noise voltage at the mixer output. Given that the ideal passive mixer's gain is $(2/\pi)\cdot g_m R_L$. The input-referred spectral density of the differential thermal noise voltage at the mixer output, due to the thermal noise of the LO switches, is given by:

$$v_{n,therm,losw,direct,in}^2 = \frac{8\pi^2 \cdot 4KT\gamma}{3 \cdot ST_{LO} g_m^{\ 2}} \cdot \beta V_{eff}^2 \quad \textbf{(6.25)}$$

The indirect mechanism by which the thermal noise from the LO switch appears at the mixer's output is described in [49]. This mechanism causes thermal noise to appear at the output when the LO switches operate in the off-overlap mode shown in Figure 6-11 (a). The charging and discharging of the parasitic capacitance present at the tail of the mixer through the resistance of the LO switches is responsible for causing the thermal noise of those

switches to appear at the output of the mixer. The spectral density of the differential thermal noise voltage at the mixer output, due to the thermal noise of the LO switches in an indirect mechanism, is given by [49]:

$$v_{n,therm,losw,indirect}^2 \approx 8KT\gamma\beta \cdot \left(V_{eff} + \frac{A_{LO}}{2} \right) \cdot R_L^2 \quad \textbf{(6.26)}$$

where, A_{LO}, is the amplitude of the LO Signal. Given that the ideal passive mixer's gain is $(2/\pi) \cdot g_m R_L$. The input-referred spectral density of the differential thermal noise voltage at the mixer output, due to the thermal noise of the LO switches in an indirect mechanism, is given by:

$$v_{n,therm,losw,indirect,in}^2 \approx \frac{2\pi^2 KT\gamma\beta}{g_m{}^2} \cdot \left(V_{eff} + \frac{A_{LO}}{2} \right) \quad \textbf{(6.27)}$$

The RF transconductor contributes thermal noise to the output of the RF mixer regardless of its mode of operation. The thermal noise originating from the transconductor itself is indistinguishable from the RF input signal. Therefore, the LO switches will down-convert the wide-band thermal noise of the RF transconductance at the LO frequency and its odd harmonics to the base-band frequency. Hence, the spectral density of the thermal noise voltage at the mixer output, due to the thermal noise of the RF transconductance, is given by [49]:

$$v_{n,mix,rfgm}^2 = 4KTg_m R_L^2 \cdot \rho \quad \textbf{(6.28)}$$

where, g_m is the RF transconductance and ρ is a factor which accounts for the total noise contribution of the RF transconductor from all side-bands of the LO. This factor can be determined by PSS simulations which take frequency translation effects into account. The input-referred spectral density of the thermal noise voltage at the mixer output, due to the thermal noise of the RF transconductance, is given by:

$$v_{n,mix,rfgm}^2 = \frac{8KT \cdot \rho}{\pi^2 \cdot g_m} \quad \textbf{(6.29)}$$

The base-band OTA's noise contributes to the RF mixer's output noise according to its mode of operation. There is an interaction between the OTA's noise and the RF mixer's output impedance which determines the noise at the mixer output [37]. This interaction is explained as follows:

1. In the on-overlap mode, there is an interval during which all LO switches are on. Figure 6-12 shows the equivalent circuit of the mixer in this case where the LO switches are represented by their on-resistance, $R_{lo,sw}$. For simplicity, it is assumed that the LO mixer switches are driven in the current domain by an ideal current source with infinite output impedance. In the interval of time during which all LO switches are on, the noise of the TIA's OTA will be amplified based on the on-resistance of the LO switches, $R_{lo,sw,}$ and the feedback resistor of the TIA, R_l. If the thermal and flicker input-referred noise of the TIA's OTA is $v_{n,ota}$, the noise voltage at the mixer output during the on-overlap period is given by:

$$v_{n,mix,ota,onov} = (1 + \frac{2 \cdot R_l}{R_{lo,sw}}) \cdot v_{n,ota} \qquad \textbf{(6.30)}$$

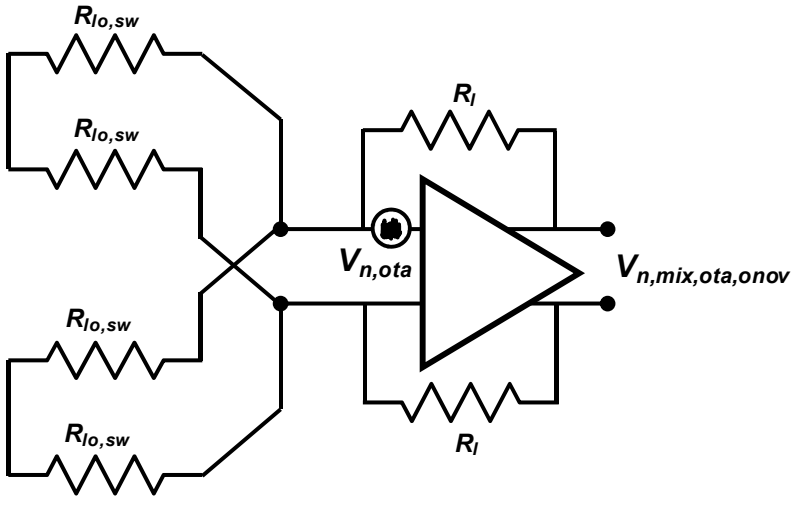


Figure 6-12 Equivalent circuit for the RF passive mixer during an on-overlap period

Equation (6.30) indicates that the OTA noise is amplified by the factor $1 + 2R_l/R_{lo,sw}$ during the on-overlap period. It should be noted that the output noise given in (6.30)

is not the total noise of the mixer; it only shows the noise contribution of the TIA's OTA in the mixer's *on-overlap* mode.

2. If the passive mixer operates in the off-overlap mode, it behaves like a switched-capacitor circuit, as shown in Figure 6-13, where the LO switches are driven by non-overlapping LO signals. The capacitors labeled C_p in the figure include the source-bulk parasitic capacitances of the LO switches, the capacitances present at the output of the RF transconductance stage and any other parasitic capacitances at the input of the LO switches. These parasitic capacitances are charged and discharged at the LO frequency, f_{LO}. If test voltages, $+V_t$ and $-V_t$, are applied to the outputs of the LO switches and produce a total test current I_t, the total charge transferred during one period is given by:

$$Q_{tot,mix} = 2 \cdot C_p V_t - (-2 \cdot C_p V_t) = 4 \cdot C_p V_t \tag{6.31}$$

This is equivalent to a total current given by:

$$I_t = Q_{tot,mix} \times f_{LO} = 4 \cdot C_p V_t \cdot f_{LO} \tag{6.32}$$

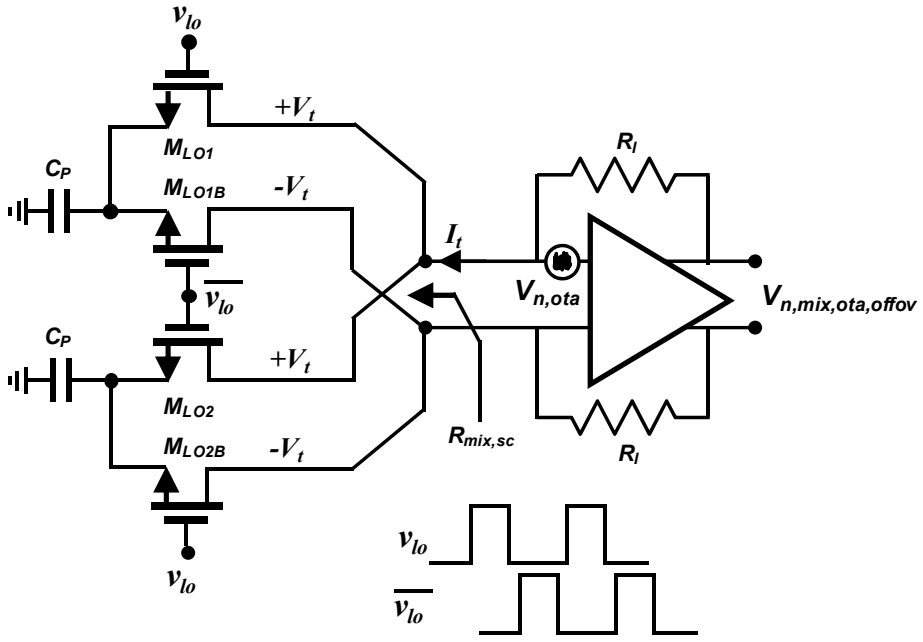


Figure 6-13 Equivalent circuit for the RF passive mixer in an off-overlap mode

Hence, the equivalent switched-capacitor resistor at the output of the LO mixer switches is given by:

$$R_{mix,sc} = \frac{2 \cdot V_t}{I_t} = \frac{1}{2 \cdot C_p \cdot f_{LO}} \quad \textbf{(6.33)}$$

The noise of the TIA's OTA will be amplified based on the effective switched-capacitor resistor given in and the feedback resistor of the TIA, R_l. If the input-referred thermal and flicker noise of the TIA's OTA is $v_{n,ota}$, the noise voltage at the mixer output in off-overlap mode is given by:

$$v_{n,mix,ota,offov} = (1 + \frac{2 \cdot R_l}{R_{mix,sc}}) \cdot v_{n,ota} \quad \textbf{(6.34)}$$

Equation indicates that the OTA noise is amplified by the factor $1 + 2R_l/R_{mix,sc}$ in the off-overlap mode. It should be noted that the output noise given in is not the total noise of the mixer; it only shows the noise contribution of the TIA's OTA in the mixer's *off-overlap* mode.

6.2.4.3 Trade-offs in Current-Commutating RF Passive Mixers

As discussed earlier, the operation of the current-commutating passive mixer relies on the fact that the V-to-I conversion does not occur in the LO switches. This translates to a smaller contribution from the non-linearity of the LO switches to the total non-linearity of the RF mixer. The contribution of the LO switches can be understood by observing that the RF current from the RF transconductance will be split between the output impedance of the RF transconductance itself and the input impedance of the RF mixer. The ratio between these two impedances will determine the RF current flowing into the LO switches. Hence, any non-linearity in the RF mixer's on-resistance will cause a non-linear RF current division ratio. In practice, the RF transconductance's output impedance cannot be infinite. Hence, maximizing the RF transconductance's output impedance will reduce the impact of the non-linearity of the LO switches' on-resistance. Alternatively, one can reduce the LO switches' on-resistance, by increasing its *W/L*, to reduce the contribution of its non-linearity to the total non-linearity of the RF mixer at the expense of an increased power consumption.

From the foregoing discussions, Table 6-2 aids in summarizing the various trade-offs in an RF passive mixer design. It should be pointed out that it is desirable to increase the slope of the LO signal driving the RF mixer. Intuitively, this approximates the design to the ideal case where the mixer is driven by an ideal square wave LO signal, thereby producing the highest conversion gain. In addition, an LO signal with small rise and fall times reduces the time when both LO switch transistors are on; this reduces the amplification of the base-band OTA thermal and flicker noise as well as the LO switch thermal noise. In addition, an increase in the LO signal slope translates into improved linearity for the passive mixer. A finite period of time between the turn-on and the turn-off instants of the LO switches means that the MOS transistors making up the LO switches transition through multiple operating regions which leads to an increase in the time-averaged non-linearity of the mixer's input impedance while the LO switch transistors transition between the off state and the triode state. This leads to an increase in the overall non-linearity of the passive mixer due to the non-linear current division ratio at the output of the RF transconductance stage.

	Linearity	Flicker Noise	Thermal Noise	Conversion Gain
Increasing LO switch width	Increased	Increased flicker noise due to an increase in LO currents in the LO switch [37]. In addition to an increase in the amplification of the base-band OTA flicker noise	Increased thermal noise due to an increase in the thermal noise current of the LO switches. In addition to an increase in the amplification of the base-band OTA noise	Decreased if the increase in switch capacitance presents significant loading on the RF trans-conductance
Increasing the RF trans-conductance	Increased if the increase in trans-conductance is via an increase in the over-drive voltage of the input transistors	Unaffected	Decreased input-referred thermal noise due to the RF trans-conductance noise	Increased
Increasing LO signal slope	Increased due to the fast turn-on and turn-off times of the LO switches.	Decreases the time when both LO switches are on, hence, decreases the amplification of the base-band OTA flicker noise	Decreases the time when both LO switches are on, hence decreases the amplification of the base-band OTA thermal noise, in addition to decreasing the thermal noise of the LO switches themselves	Increased since the time when both differential LO switches are on is reduced. Hence, decreasing any common-mode signal current

Table 6-2 Trade-offs in RF passive mixer design

Overall, to get the best performance from the RF passive mixer, it is desirable to:

1. Increase the LO signal slope in order to increase the mixer's linearity and conversion gain and to reduce the amplification of the base-band OTA's thermal and flicker noise as well as to reduce the contribution of the thermal and flicker noise of the LO switches. This comes at the expense of an increase in power consumption.
2. Increase the RF transconductance by using a higher over-drive voltage for the input transistors in order to increase the linearity and conversion gain of the mixer as well as to reduce the contribution of the input-referred thermal noise of the RF transconductance stage to the mixer's total thermal noise
3. Increase the width of the LO switches if they limit the linearity of the passive mixer at the expense of increased amplification of the base-band OTA thermal and flicker noise, as well as an increased contribution from the thermal noise of the LO switches and an increase in power consumption. Decrease the width of the LO switches if linearity of the passive mixer is not the dominant contributor to the mixer's linearity in order to save power consumption in the LO driver circuit.

6.2.4.4 Implementation of the RF Transconductor of the Current-Commutating RF Passive Mixer

Figure 6-14 shows the implementation of the RF transconductor of the RF passive mixer which is indicated by G_m in Figure 6-10. The RF transconductor is based on a pseudo-differential common-source amplifier cascoded with a common-gate amplifier. The common-source amplifier comprises M_{rf} and M_{rfb} while the common-gate amplifier is made of M_{casc} and M_{cascb}. The inputs of the common-source amplifier are AC-coupled to the outputs of an inductively-loaded LNA [1]. The common-gate amplifier can be viewed as a cascode stage for the pseudo-differential common-source amplifier. The primary function of the cascode stage is to provide isolation between the LO switch transistors connected to the output of the RF transconductor and the RF inputs of the transconductance stage. Any leakage from the LO path to the input RF path causes time-varying offsets at the base-band of a ZIF receiver and

needs to be minimized to avoid corrupting the desired signal's SNR. In addition, the common-gate amplifier acting as a cascode reduces the capacitive load presented to the LNA inductor by reducing the gain of the Miller capacitance formed by the gate-drain capacitor of the common-source amplifier.

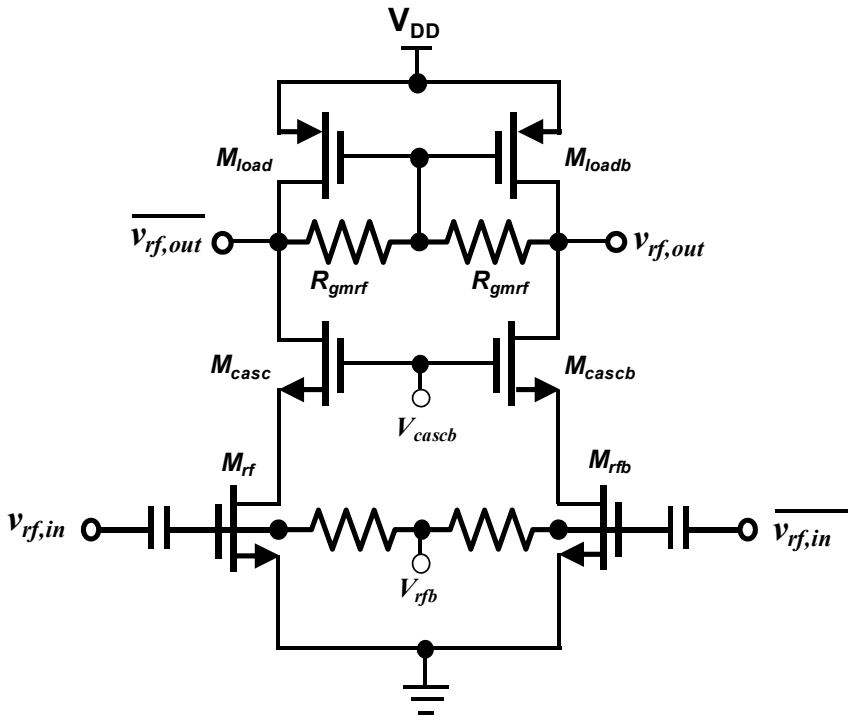


Figure 6-14 RF transconductor implementation of the passive mixer

In the absence of the cascode stage, the low-frequency gain of the Miller gate-drain capacitor of transistor M_{rf} is given by:

$$A_{v,miller,nocasc} \approx -g_{m,rf} \times (r_{o,load} // R_{gm,rf}) \tag{6.35}$$

where $g_{m,rf}$ is the transconductance of the common-source amplifier, $r_{o,load}$ is the output resistance of M_{load} and M_{loadb}, and $R_{gm,rf}$ is the load resistance of the transconductance stage. In the presence of the cascode stage, the low-frequency gain is reduced to:

$$A_{v,miller,casc} \approx -\frac{g_{m,rf}}{g_{m,casc}} \times (1 + \frac{r_{o,load} // R_{gm,rf}}{r_{o,casc}}) \tag{6.36}$$

which assumes a large output resistance for transistor M_{rf} and $g_{m,casc} \times r_{o,casc} >> 1$, $g_{m,casc}$ is the transconductance of the common-gate amplifier, $r_{o,casc}$ is the output resistance of M_{casc} and M_{cascb}.

The load of the RF transconductor stage is formed by transistors M_{load}, M_{loadb} and the load resistors $R_{gm,rf}$. This configuration allows the use of a large load resistance relative to the input impedance of the passive mixer looking into the LO switch transistors. Maximizing the output impedance of the RF transconductance stage relative to the input impedance of the mixer is essential to maximize the overall gain of the passive mixer since it is required that all the output RF current from the RF transconductor flows into the LO switch transistors. If the load resistors were connected directly to the supply, the value of the load resistors are restricted by the voltage drop across them which conflicts with the requirements for the maximum possible load resistor for a given current consumption in the RF transconductance stage. At DC, transistors M_{load} and M_{loadb} form diode-connected PMOS loads. Hence, the voltage drop required for these transistors is only their gate-source voltage in saturation mode. In the differential mode of operation, the gates of M_{load} and M_{loadb} are virtual grounds and the PMOS transistors behave like current sources. Hence, the differential low-frequency transconductance for this stage is given by:

$$G_{v,rfgm} \approx -g_{m,rf} \times \left(\frac{R_{gm,rf}}{R_{gm,rf} + R_{mix,in}}\right) \quad \textbf{(6.37)}$$

where, $R_{mix,in}$ is the mixer's input impedance. Hence, if $R_{gm,rf} >> R_{mix,in}$, the transconductance is simply given by $- g_{mrf}$.

The bias voltage of the common-source amplifier, V_{rfb}, and the bias voltage of the common-gate amplifier, V_{cascb}, are set by a constant-g_m bias circuit. This biasing scheme keeps the value of the transconductance proportional to $1/R_{poly}$, where R_{poly} is a poly resistor of the same type as the load of the transimpedance amplifier. In addition, the bias voltage V_{rfb} plays a key role in the linearity of the RF passive mixer.

This can be illustrated using a basic analysis of the MOS linearity characteristics. The small-signal i_D-v_{GS} characteristics of a MOS device configured as a common-source amplifier can be written as:

$$i_D = g_m \cdot v_{GS} + \frac{g'_m}{2!} \cdot v_{GS}^2 + \frac{g''_m}{3!} \cdot v_{GS}^3 \quad \textbf{(6.38)}$$

where, g_m, g_m' and g_m'' are the zeroth-order, first-order derivative and second-order derivative of the MOS transistor transconductance respectively. Using the IIP3 expression of a non-linear system [3], the peak IIP3 amplitude using a two-tone test is given by:

$$A_{IIP3} = \sqrt{8 \times \frac{g_m}{g''_m}}\,. \quad \textbf{(6.39)}$$

Figure 6-15 shows the I_D-V_{GS} characteristics of a MOS device configured as a common-source amplifier for various process corners (nominal, fast and slow) as well as various device temperatures (-40˚C, 27˚C and 85˚C) for a device width of 2.5µm×8 and length of 0.18µm using BSIM4 models for a drain-source voltage of 1V. Also shown is the g_m'' (denoted as g_3 in the figure) and the theoretical A_{IIP3} parameter of the transistor. It can be seen that the g_m'' parameter crosses zero when the gate-source voltage, V_{GS}, is such that the transistor is biased at the transition from weak inversion to moderate inversion. From equation (6.39) this ideally translates to an infinite IIP3 for the MOS transistor. Limited by the resolution of the V_{GS} sweep, the figure shows that the IIP3 peaks when the parameter g_m'' changes sign. The figure also shows that the gate-source voltage, V_{GS}, of the MOS transistor corresponding to the peak IIP3 is different for each of the process and temperature corners. This makes the task of biasing the transistor at these optimum points difficult for a stable linearity performance across process variations and temperature. There are circuit techniques which attempt to take advantage of this property by using multiple transistors biased in different regions of operation. For example, this can be achieved by using two parallel MOS devices, one biased in the weak inversion region (positive g_m'') and one biased in the moderate or strong inversion region (negative g_m''). The composite transistor will have close to zero g_m'' in a small range

between the gate-source voltages corresponding to the nulls in the characteristics of each of the individual transistors [50].

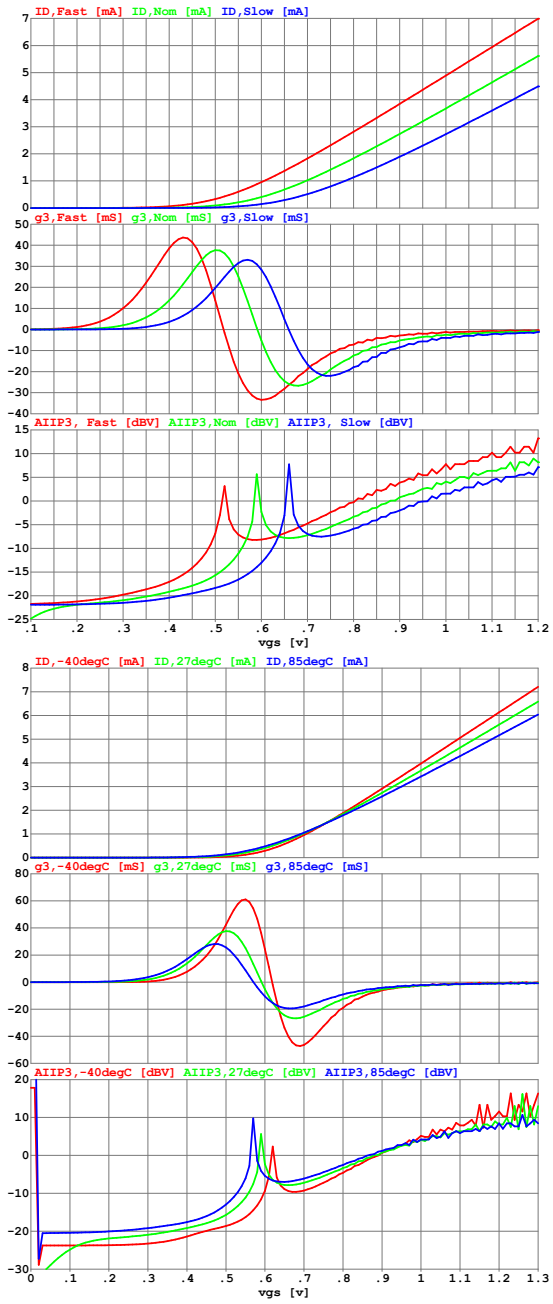


Figure 6-15 Dependency of the linearity of MOS devices on the gate-source voltage

This work did not take advantage of this property. Instead, and since minimizing power consumption is paramount, the MOS transistors in the RF transconductance stage were biased at a gate-source voltage with a relatively high g_m/I_D. Figure 6-5 shows that this corresponds to

using a relatively low overdrive voltage. The gate-source voltage of choice is approximately 0.6V, yielding a g_m/I_D ratio of about 11.

6.2.4.5 Simulation Results of the Current-Commutating RF Passive Mixer

Through simulations, the design of the passive RF mixer was optimized for the best noise-linearity-power consumption trade-off. Towards that end, the RF mixer operates close to the off-overlap mode for the best performance trade-off. Figure 6-16 and Figure 6-17 show the simulated linearity and noise performance of the RF mixer.

Figure 6-16 shows the RF mixer's IIP3 and IM3 performance versus the RF input power at the mixer input using BSIM4 MOS transistor models. PSP models, which better capture the non-linearity of the MOS transistors, were not available for this process node during the design phase. The IIP3 simulation, shown in the figure, uses two RF tones which generate baseband tones at 600kHz and 1000kHz and IM3 components at 200kHz and 1200kHz. The IIP3, shown in the figure, is calculated for the IM3 components at 200kHz and 1200kHz for various gate-source voltage biases for the RF transconductance. It can be seen that there is a negligible difference in the IIP3 performance of the mixer for over-drive voltages of 150mV to 300mV (equivalent to V_{GS} between 0.6V to 0.75V). For maximum g_m/I_D ratio, a gate-source voltage of 0.6V was selected. This yields an IIP3 of -4dBV$_{rms}$.

Figure 6-17 shows the input-referred noise PSD in dBV$_{rms}$/Hz. The input-referred thermal noise floor of the RF mixer is -161.7 dBV$_{rms}$/Hz. The flicker noise corner at the input of the RF mixer is 7.5kHz, as simulated with the base-band flicker noise models of the MOS transistors. This performance is achieved with a total current consumption of 4mA from 1.8V supply, including the current consumption of the LO buffers and that of the trans-impedance amplifiers. The total RF mixer conversion gain from the RF transconductance input to the transimpendence output at the baseband is 15.6dB. This is very close to the ideal conversion gain of 15.3dB, as given by equation (6.22).

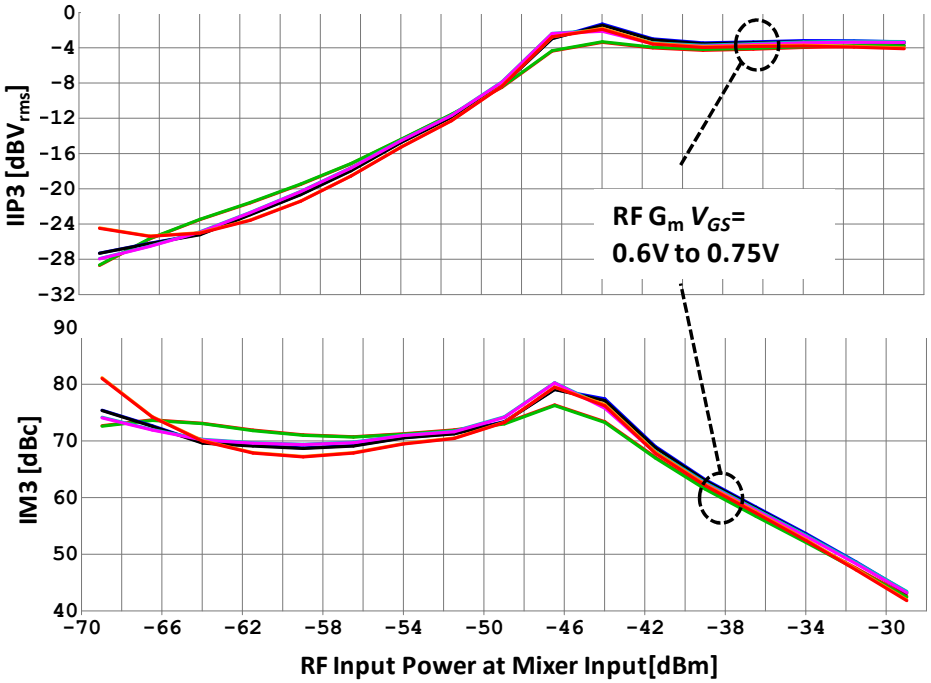


Figure 6-16 IIP3 and IM3 versus RF input power at the RF mixer input

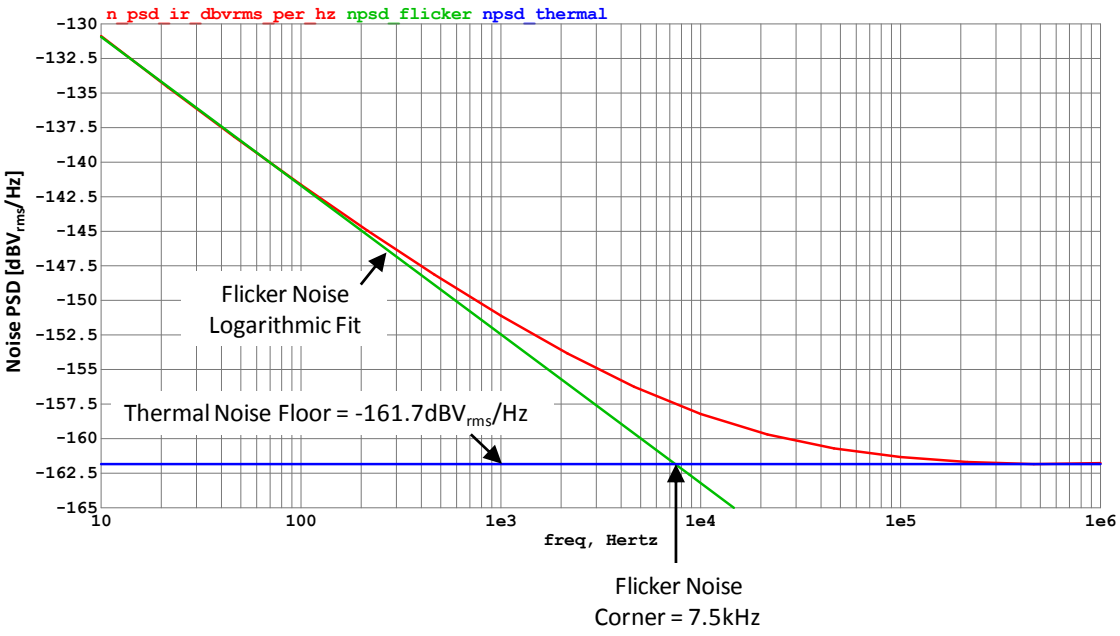


Figure 6-17 Input-Referred Noise PSD of the RF Mixer

6.2.5 Passive Mixer Quadrature Signal Generation

The quadrature LO signals for the RF passive mixer of Figure 6-10 are generated using a frequency divider. The VCO of the receiver operates at twice the fundamental frequency of 2.4GHz. This is critical in a ZIFR to avoid LO self-mixing in the passive mixer causing significant time-varying offsets in the receiver. In addition, operating the VCO at twice the transmitter frequency avoids pulling the VCO frequency when the transmit PA turns on, which would otherwise cause undesirable spectral emissions. The frequency divider divides the VCO frequency from 4.8GHz to 2.4GHz. Figure 6-18 shows a block diagram of the frequency divider based on two D-type latches [51] [52]. The input to the latch is the differential LO signal labeled as CLK and $\overline{CLK}$. The divider block divides both the frequency and the phase of the input differential signal, generating the output differential in-phase and quadrature signals labeled as I, $\overline{I}$, Q and $\overline{Q}$ respectively. Although a quadrature oscillator can be used to generate the quadrature signals, the area that would be occupied by the additional inductor needed for the quadrature oscillator is prohibitive for a low cost transceiver. In addition, the quadrature oscillator would have to operate at the RF frequency which is detrimental for a ZIFR architecture given the drawback of LO self-mixing.

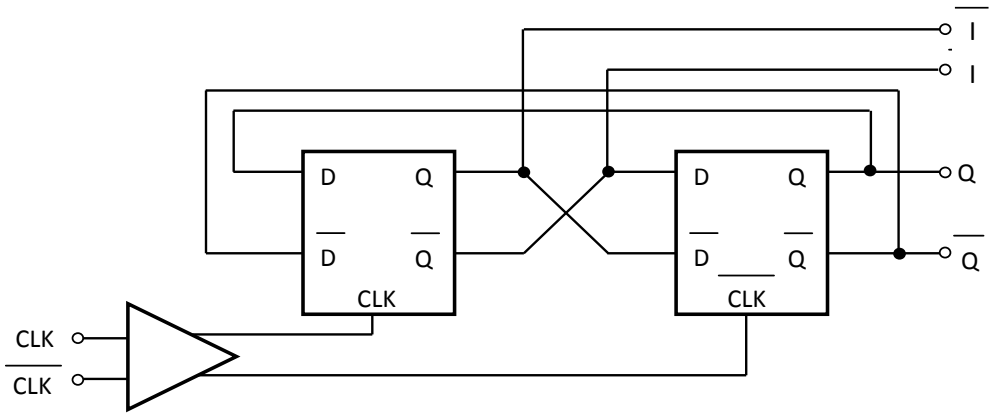


Figure 6-18 A block diagram for a frequency divide-by-2 circuit.

The transistor-level implementation of the D-type latch is shown in Figure 6-19. The latch is composed of only a stack of two transistors; a PMOS and an NMOS between the supply and

ground rails. Hence, the design can operate at a very high frequency from the low supply voltage of 1.8V which translates to lower power consumption than divider architectures which stack more than two transistors between the supply and ground nodes.

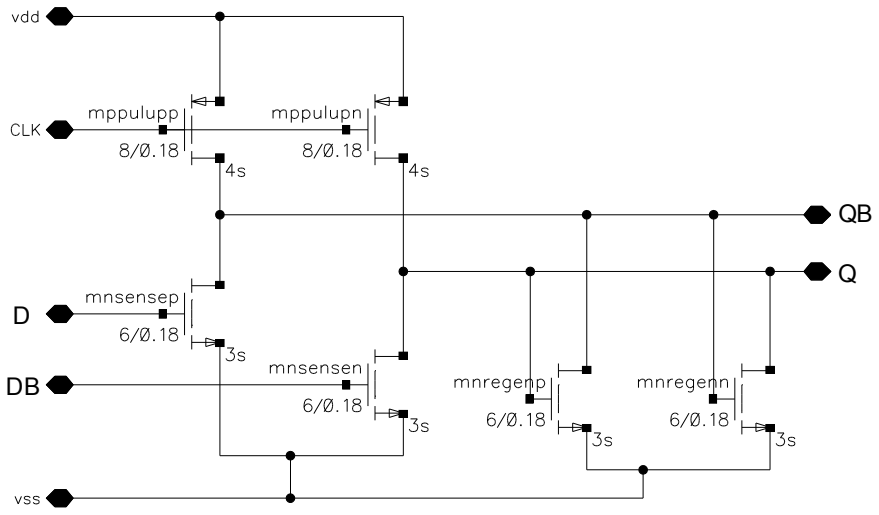


Figure 6-19 A transistor-level schematic showing the implementation of the D-type latch used in the divide-by-2 circuit

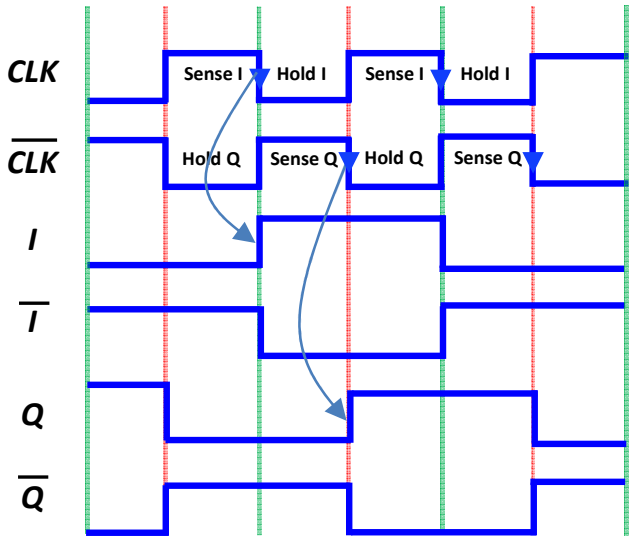


Figure 6-20 Timing diagram for the operation of the divide-by-2 circuit

The circuit employs two D-type latches in a master-slave configuration with negative feedback as shown in Figure 6-18. Each latch consists of two NMOS sense devices; *mnsensep* and *mnsensen*, an NMOS regenerative loop composed of *mnregenp* and *mnregenn* and two

PMOS pull-up devices; *mppulupp* and *mppulupn*. When CLK goes from low to high, the master latch is in sense mode while the slave latch is in store mode, and when CLK goes from high to low, the opposite occurs. In sense mode, the two NMOS devices *mnsensep* and *mnsensen* sense the differential inputs to the master latch, $\overline{D}$ and D. While CLK is high, the master latch outputs $\overline{Q}$ and Q can only change their differential state from high to low because the PMOS pull-up devices are off. The slave latch is constructed using the same cell shown in Figure 6-19. With its CLK input low, the slave latch is in store mode and will not change its differential state while the state of the master latch is changing from high to low.

Figure 6-20 shows a timing diagram for the operation of the divide-by-2 circuit shown in Figure 6-18. As shown in the figure, when the CLK input to one of the latches is high, it operates in the sense mode. For example, when CLK is high, the master latch is sensing the I input while the slave latch is holding the Q output. When CLK is low, that is when $\overline{CLK}$ is high, the master latch is sensing Q input while the slave latch is holding the I output. The role of the latches changes between being a master and a slave generating the I and Q outputs at half the frequency of the CLK input. The I and Q outputs change on the falling edge of CLK and $\overline{CLK}$ when any of the latches is in sense mode.

A block diagram of a typical LO section of the RF transceiver is shown in Figure 6-21. The LO section is comprised of the VCO, LO buffers close to the VCO at the start of the distribution line to supply the LO signal to various sections of the transceiver, the LO distribution lines and local LO buffers close to the circuits being driven by the LO.

In a typical implementation, the LO distribution lines can span the entire length of the die, depending on the location of the various blocks with respect to the VCO, even if layout is carefully planned. The buffers close to the VCO serve to isolate it from the load. These buffers can be implemented using active devices which consume small area but have very

high power consumption. Alternatively, a single tuned VCO buffer can be used where it uses an inductor which resonates with the parasitic capacitance of the LO lines at the VCO frequency. This type of buffer consumes less power but occupies substantial silicon area and therefore prohibits its practical use for ultra-low cost transceivers.

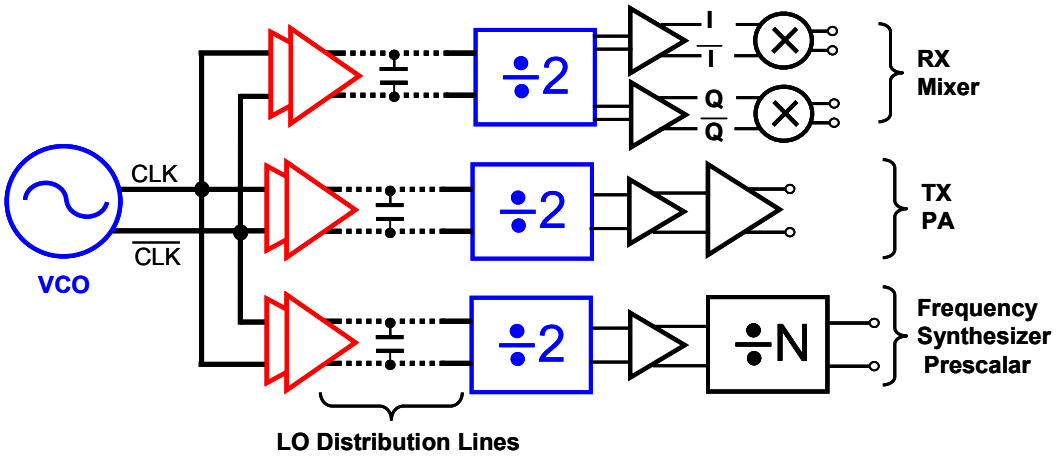


Figure 6-21 Block diagram of LO distribution using multiple buffered paths for the VCO.

The LO buffers also serve to supply a rail-to-rail voltage swing to the frequency dividers. In some cases LO buffers are distributed along the LO lines. This option is based on the merit of the power consumption of the LO buffers and the load they drive. At the output of the frequency dividers, additional buffers are used to drive the various circuitry which need the LO signal such as the RX mixer, the TX power amplifier (PA) and the frequency synthesizer prescalar circuitry. In addition, as shown in Table 6-2, it is very desirable to maximize the LO signal slope to improve the RF mixer performance.

The type of dividers shown in Figure 6-19 can catastrophically fail, rather than have degraded performance, if they are not designed with enough speed margin. For example, a divider which is required to operate with an input frequency of 4.8GHz, will typically require a 15-20% design safety margin on its input frequency at the worst-case process/design corner to

guarantee its reliable functionality. The reasons that this design safety margin has to be used are:

1. In these divider circuits, there're no means to control the behaviour of the circuit after it has been manufactured. The VCO output amplitude can be increased at the input of the divider but offers a limited means to enhance its speed. Unlike other architectures which use a current source that can be controlled in the event of a failure, low power architectures eliminate the fixed current source to provide more voltage headroom for the transistor stack between the supply and ground as shown in the implementation of Figure 6-19.
2. While the accuracy of extracting the parasitic capacitance in analog circuits has improved significantly in recent years, the capacitance of the individual transistors are still poorly modeled, especially at high RF frequencies where relatively accurate S-parameters are required for the transistors being used.
3. In addition, the transistor model parameters which correspond to the slow and fast process corners are conservatively set by the process foundry in order to minimize the design yield loss. While this could be beneficial from a manufacturing point of view, it's not suitable for ultra-low power RF transceiver design where the *exact* transistor model parameters need to be considered to avoid any unnecessary power to be consumed in the design. A 15-20% design margin on the input frequency in the worst-case process/design corner of the divider in addition to the conservative transistor simulation models leads to an increase in power consumption which can be as high as 60%.

From the preceding discussion, the drawbacks associated with prior-art implementations for frequency divider circuits are as follows:

1. The LO buffers at twice the operating frequency of the battery-operated transceiver consume a substantial amount of power. For example, a two-stage differential buffer consumes 2.5mA at 4.8GHz using a $3V_{pp,diff}$ VCO amplitude at its input to drive a

50fF differential capacitive load with a 2.4$V_{pp,diff}$ swing at its output. Two instances of these buffers can be required in either RX or TX modes which translate to a power consumption of 5mA; this is approximately 28% of the total power consumption budget for either the RX or TX modes.

2. The divider circuit has to be nominally designed with a significant design margin to be able to :
    a. Operate at the conservative worst-case process corner models supplied by the process foundry.
    b. Guarantee operation in the presence of transistor modeling inaccuracies.
    c. Allow for a design safety margin to avoid functionality failure.

    Having such a design margin could lead to an increase in the nominal power consumption of the frequency divider by as much as 60% compared to a design which does not have this high design margin.
3. For low power and low-supply voltage frequency divider circuits, there're currently no means to control the circuit operation and hence avoid its failure after manufacturing.

The design strategy to alleviate these drawbacks is as follows [53] [54]:

1. Remove the LO buffers operating at twice the operating frequency of the transceiver.
2. Design an adaptively biased frequency divider circuit which :
    a. Increases the frequency divider's current consumption at the worst case temperature corner to guarantee the operation of the circuit at this corner as well as to decrease its current consumption at other temperature corners while maintaining the lowest possible current consumption under nominal conditions.
    b. Have the flexibility to increase or decrease its current consumption after manufacturing to be able to assess how much margin is needed for the design.

Figure 6-22 shows a block diagram of the LO distribution network developed for this work. The design eliminates the LO buffers on the VCO side and relies on the LO distribution lines to deliver the VCO signal to multiple frequency divider circuits. The capacitive and resistive losses associated with the LO distribution lines and the frequency dividers will be directly seen by the VCO in this design. These are lumped as R_L and C_L in Figure 6-22. The VCO is typically designed using an LC tank with a high quality factor (low resistive losses) for low power consumption and low noise performance; hence, any degradation to this high quality factor has to be avoided. To achieve this, capacitor C_{vco} is added to act as an impedance transformer. Using the parameters highlighted in Figure 6-22, the impedance transformer can be described by the following set of equations assuming narrow bandwidth of operation and relatively high quality factor for the R_L and C_L network:

$$R_{LT} = R_L\left(1+\frac{2C_L}{C_{vco}}\right)^2 \tag{6.40}$$

$$C_{LT} = \frac{C_L C_{vco}}{2C_{vco}+C_L} \tag{6.41}$$

$$A_{cdiv} = \frac{1}{1+\frac{2C_L}{C_{vco}}} \tag{6.42}$$

By proper selection of the value of C_{vco} with respect to the value of C_L, the resistive part of the impedance, R_L, is transformed to a higher resistance R_{LT} across the VCO's LC tank, thereby, reducing the resistive loss seen by the VCO LC tank. The capacitive part of the impedance, C_L, is also transformed by the impedance transformer into the capacitor, C_{LT}, which is absorbed by the inductor of the LC tank of the VCO. The attenuation experienced by the VCO signal, due to the capacitance division formed by C_{vco} and C_L, is given by A_{cdiv} in (6.42). For example, if $C_{vco}=4\cdot C_L$, then based on equations (6.40) to (6.42), we have $R_{LT}=2.25\cdot R_L$, $C_{LT}=0.67\cdot C_L$ and $A_{cdiv}=0.67$. Hence, there is a trade-off between the attenuation of the VCO

signal through the capacitive divider formed by C_{vco} and the equivalent capacitance C_L on the one hand and the transformed impedance presented to the VCO in the form of R_{LT} and C_{LT}.

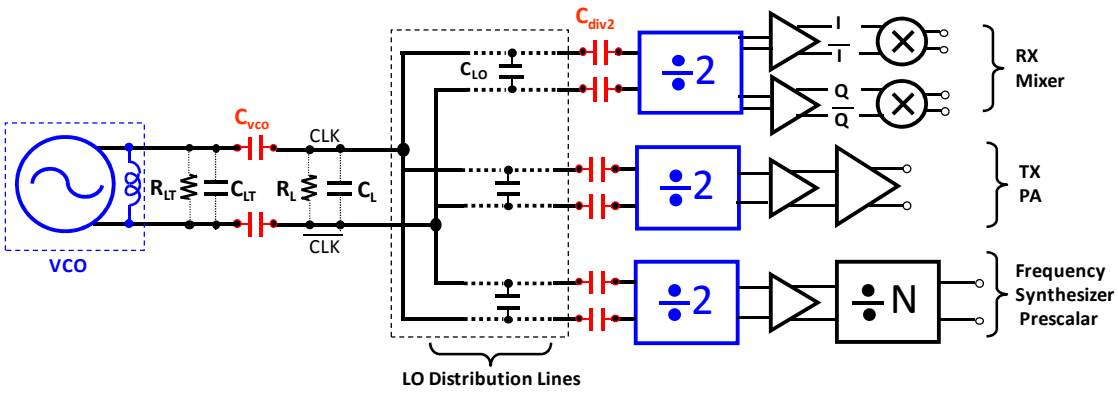


Figure 6-22 Block diagram for the LO distribution network in this work.

Since the VCO is based on an LC tank, it absorbs all the capacitive load of the LO lines as indicated. This capacitive load, in addition to the resistive load, R_{LT}, will only slightly degrade the intrinsic quality factor of the VCO LC tank. This effect will lead to an increase in the power consumption of the VCO by about 10% to counteract the degradation in the quality factor. The increase in current consumption, which is in the order of 0.2mA, is acceptable.

Since the LO distribution lines are now part of the VCO LC tank, the VCO might appear to be susceptible to spurious components that might arise on a large mixed-signal chip. Proper shielding and physical isolation between noisy circuits and the LO distribution lines are employed and there is no degradation in the spurious performance of the VCO observed on the manufactured silicon of the device.

The second aspect of this novel circuit is to adaptively control the power consumption of the frequency divider circuit according to the process corner and temperature condition of the design in which the circuit operates in order to reduce its nominal power consumption. This is partly fulfilled by using capacitor C_{div2} indicated in Figure 6-22.

A simplified schematic of the bias control circuit is shown in Figure 6-23. The idea is based on driving the *CLK* signals of the D latch with a non rail-to-rail voltage swing. This is facilitated by eliminating the LO buffers which drive the frequency dividers and directly driving the *CLK* signals of the frequency divider circuit using the VCO signal via the capacitor C_{div2}. The amplitude of the VCO signal determines the current in the transistors driven by the *CLK* signals. These are shown as *mp2* and *mp3* in Figure 6-23. The circuit further exploits the characteristics of these PMOS transistors as voltage controlled resistors. By controlling the DC bias voltage on the gates of these PMOS transistors, the current flowing through them is controlled. This is achieved by using the AC coupling capacitor C_{div2} and biasing the gates of transistors *mp2* and *mp3* using R_{div2}, as shown in Figure 6-23. A bias generator circuit generates the DC bias voltage on the gates of transistors *mp2* and *mp3* which is applied via R_{div2}. Hence, the current flowing in transistors *mp2* and *mp3* is controlled both by the DC bias voltage at their gates as well as the amplitude of the VCO signal. This, in turn, controls the average on-resistance of the PMOS transistors *mp2* and *mp3*.

An important aspect of this novel circuit is the bias generator circuit. This circuit is designed such that the DC bias voltage for the gates of the transistors driven by the *CLK* signal is *shaped* in a specific way to minimize the overall current consumption of the divider circuit. The circuit generates the DC bias voltage *v_bias* using two types of current sources; a PTAT (proportional to absolute temperature) current and a ZTAT (zero change with absolute temperature) current. The PTAT and ZTAT currents are *mixed together with a certain ratio* to generate the DC bias voltage. The ratio by which the PTAT and ZTAT currents are mixed is controlled by two 6-bit current mode DACs. These are controlled using data lines iztat_bias<5:0> and iptat_bias<5:0>, as indicated in the bias generator circuit depicted in Figure 6-23.

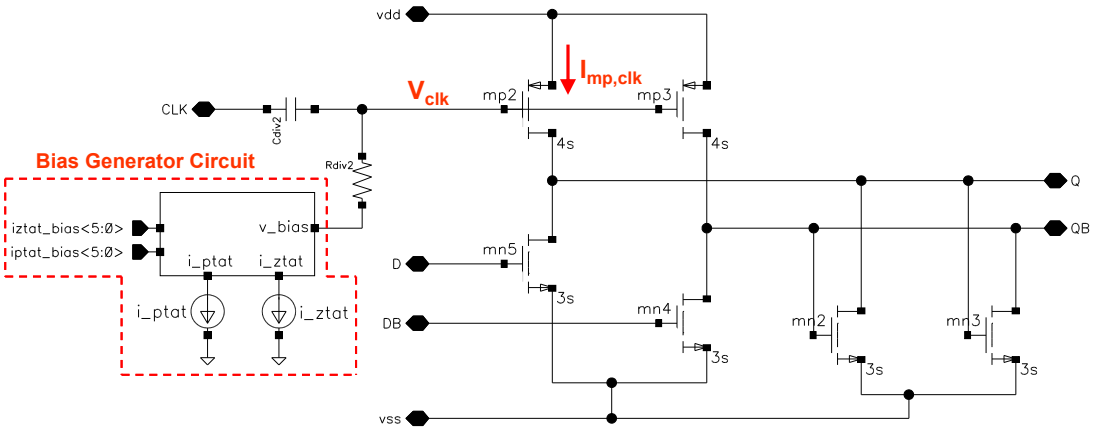


Figure 6-23 Simplified schematic for the bias control of the divider circuit.

The PTAT and ZTAT bias DACs are implemented with a programmable full-scale (FS) setting which can take the values of either 0 or 1. If FS=1, the DAC full-scale is doubled compared to the case where FS=0. Figure 6-24 shows the effect of changing the PTAT and ZTAT current DAC settings on the amount of current which flows in the *CLK* transistors *mp2* and *mp3*. The figure shows the instantaneous current $I_{mp,clk}$ which flows in the PMOS transistors which are driven by the *CLK* signal for a PTAT bias DAC code=8 and FS=0, PTAT bias DAC code=15 and FS=0, and PTAT bias DAC code=15 and FS=1. As the PTAT bias DAC code increases, the DC bias voltage *v_bias* decreases, where *v_bias* is the DC voltage of the signal V_{clk} and hence, the current $I_{mp,clk}$ flowing in the PMOS transistors increases. The value of $I_{mp,clk}$ is determined both by *v_bias* as well as the amplitude of the VCO signal. This is the fundamental property of this circuit where the amount of current in the D latch circuit is controlled by the bias generator circuit.

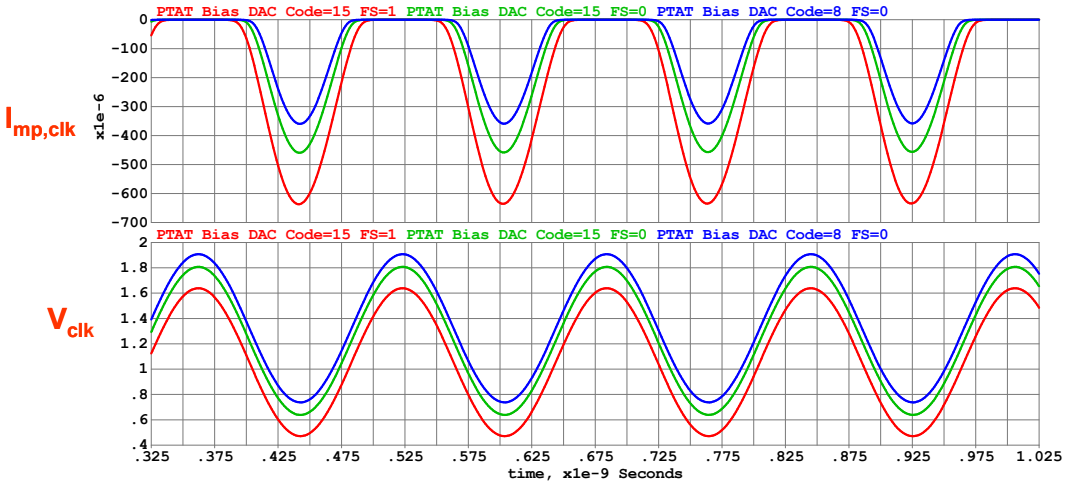


Figure 6-24 Current and voltage waveforms for the CLK PMOS transistors mp2 and mp3.

This property is exploited to *shape* the value of the DC bias voltage *v_bias* to minimize the overall current consumption of the frequency divider circuit. This shaping is done across the temperature of operation of the circuit. At high temperature, the on-resistance of the transistors constituting the D latch circuit is *higher* than the nominal value and hence higher current consumption is required to maintain the functionality of the circuit. At low temperature, the on-resistance of the transistors is *lower* than their nominal value and hence less current is needed to maintain the functionality of the circuit. The voltage shaping is achieved by the PTAT component of the current used to generate *v_bias* while the ZTAT component of the current is used to generate the constant component of *v_bias* across the temperature range.

Table 6-3 shows a summary of the current consumption savings achieved by eliminating the LO buffers and using the *bias current shaping* technique for the frequency divider. It can be seen from the table that the total nominal current consumption savings due to savings in the current consumption of the frequency divider and the LO buffer (while accounting for an increase of the current consumption of the VCO) is 6mA, which is almost one-third of the

total current consumption of the receiver path. The total current consumption saving across all temperature and process corners is 9mA.

Process and Temperature Corner	Frequency divider current consumption saving	LO buffer current consumption saving	Increase in VCO current due to excess resistive and capacitive loading	Total current consumption saving from 1.8V supply
Nominal	1.2mA	5mA	0.2mA	6.0mA
All	3.4mA	6mA	0.2mA	9.2mA

Table 6-3 Table summarizing the current consumption savings using the *bias current shaping technique.*

6.3 Measurement Results of the RF Receiver

Figure 6-25 shows a die photo of the RF transceiver IC. The total die area is 5.88mm^2. The digital section takes slightly less than half of the active chip area and the receiver area is approximately 1.8 mm^2. Figure 6-26 shows the evaluation board of the RF transceiver IC. The RF transceiver IC is packaged in a 5mm×5mm 32-pin LFCSP package with an exposed paddle. Two RF ports, RF1 and RF2 are indicated on the board denoting the two differential LNA input ports used for switched antenna diversity as described in Figure 6-1.

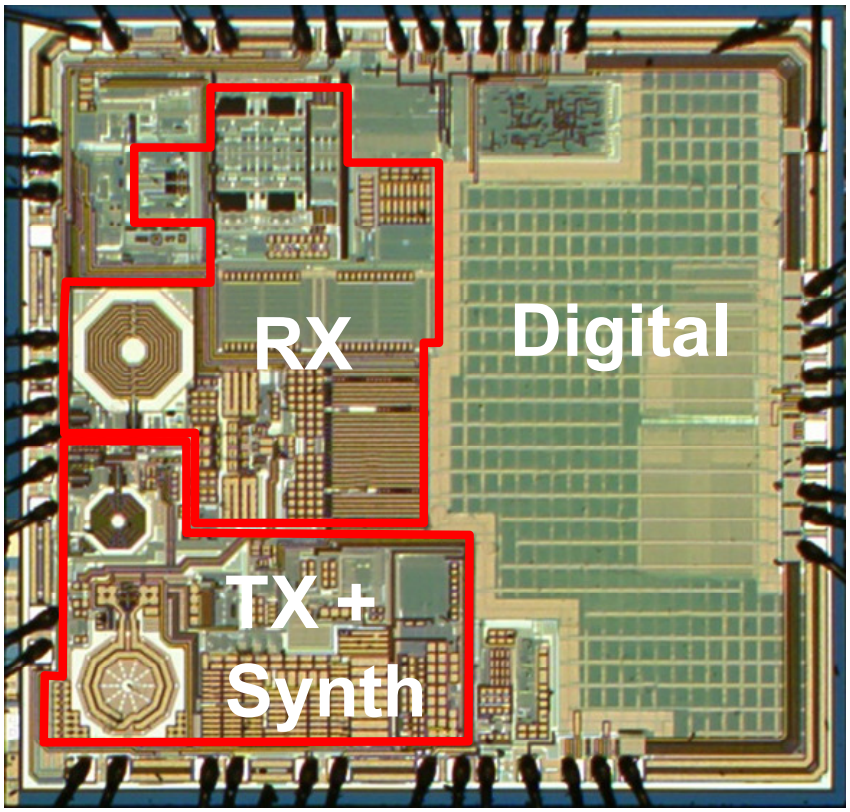


Figure 6-25 Die photo of the RF transceiver

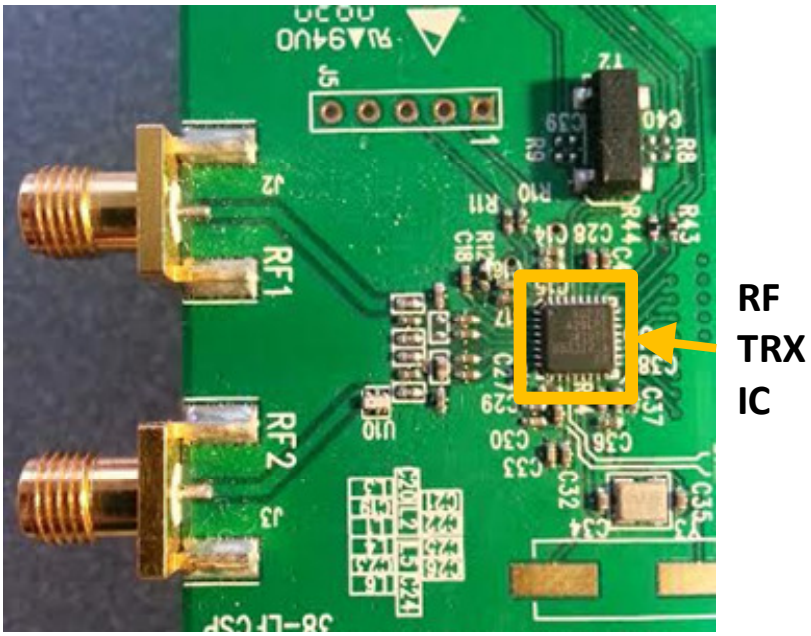


Figure 6-26 Evaluation board of the RF Transceiver

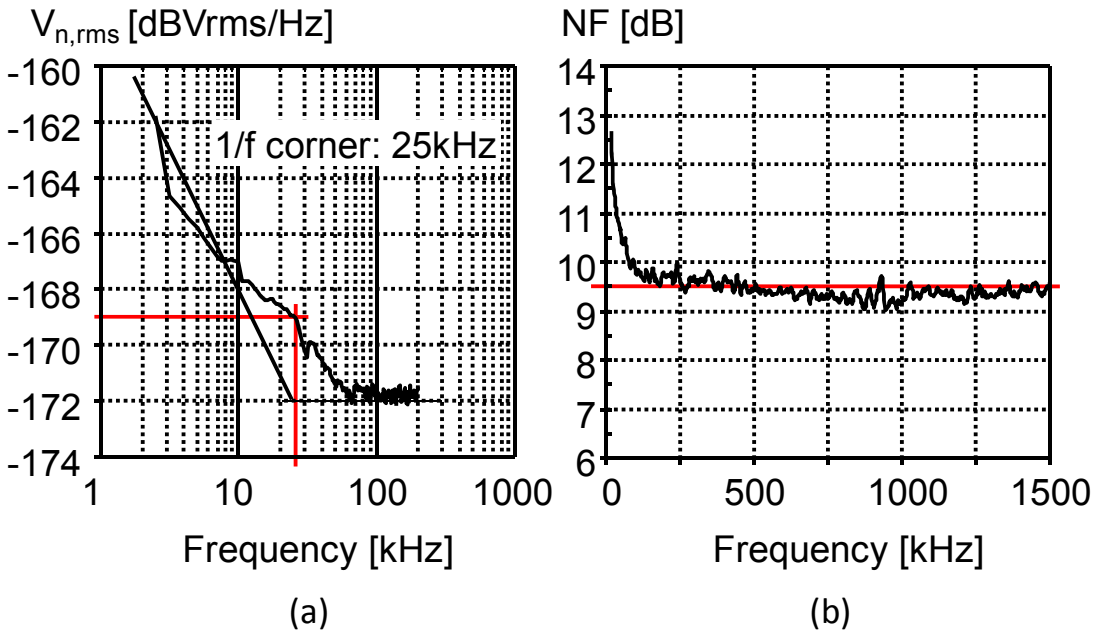


Figure 6-27 (a) Input-referred noise voltage density and (b) Noise figure of the RF receiver

Figure 6-27 to Figure 6-32 show the various measured receiver performance aspects. Figure 6-27 shows the measured noise performance of the RF receiver[4]. Figure 6-27 (a) shows the measured input-referred noise voltage density of the receiver and Figure 6-27 (b) shows the receiver's noise figure measured at the PGA outputs up to a frequency of 1.5MHz. The receiver front-end achieves a thermal noise figure of 9.5dB and a flicker noise corner frequency of approximately 25kHz. If the ADC noise contribution is taken into account, the receiver's noise figure is 9.6dB, which is within 0.4dB of the estimated noise figure in the analysis shown in Table 6-1 and Figure 6-2.

The RF receiver achieved an IIP3 of −13.6dBm at maximum gain using a two-tone test of 5 MHz and 10.1 MHz with an input RF power level of −35dBm at the antenna, and an IIP3 of −10.5dBm at maximum gain for two blockers placed at 40 MHz and 80.1 MHz for an input RF level of −35dBm. The 1-dB compression point of the RF receiver is −20.5dBm at

[4] Measurement provided by Guido Retz

maximum gain. This performance level exceeds the design targets of -13dBm and -23dBm for the IIP3 and the P1dB respectively as estimated for the receiver in Table 6-1.

The RF receiver's IIP2 measured at the PGA output is about +30dBm at maximum gain for blocker frequencies 30MHz and 30.1MHz with an RF input power level of −40dBm. This IIP2 level exceeds the requirement of +20dBm under the same conditions as outlined in (5.25).

The RF receiver's LO Level at the RF antenna is −100dBm. In addition, the RF receiver's spurious emissions comply with the EN 300 440 standard achieving a maximum of −57dBm spurious emissions in the 30 MHz to 1000 MHz band and −47dBm in the 1 GHz to 12.75 GHz band [28].

Figure 6-28 shows the IEEE 802.15.4 packet-error rate (PER) sensitivity versus temperature and supply voltage for RF channels 2.405GHz, 2.45GHz and 2.475 GHz[5]. The PER sensitivity is measured for the whole receiver from the antenna input to the packet RAM output. Hence it includes the entire analog and digital signal processing functions of the receiver. The PER sensitivity is measured as the RF input power at which the PER is equal to 1% for 10,000 IEEE 802.15.4 20-octet packets. From the figure, the nominal sensitivity is about -95dBm in the middle of the 2.4GHz band. The variation in the PER sensitivity is only 3dB across the supply voltage, channel frequency and device temperature which indicates the excellent robustness of the design. The achieved sensitivity of -95dBm matches the target set for the receiver in section 5.3.1.

[5] Measurement provided by Tony O'Connell

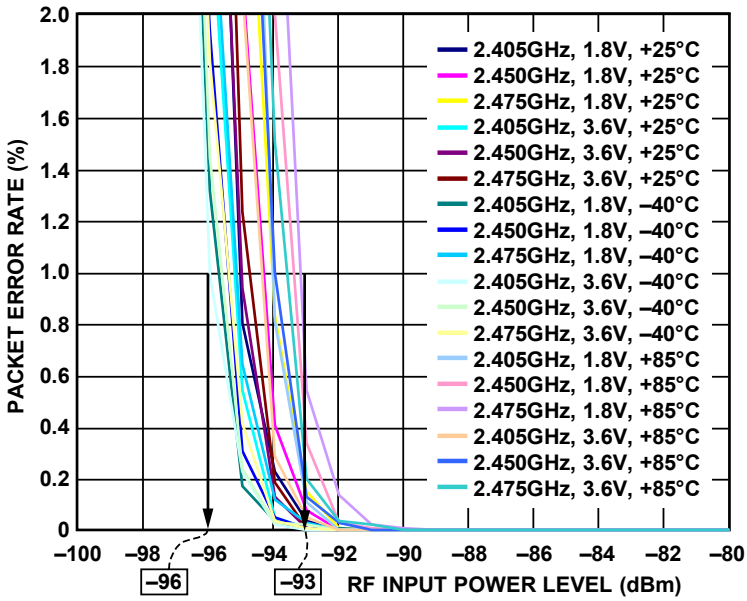


Figure 6-28 Measured IEEE 802.15.4 PER sensitivity versus temperature and supply voltage for RF channels 2.405GHz, 2.45GHz and 2.475 GHz

Figure 6-29 shows the 2Mbps GFSK PER sensitivity versus temperature and supply voltage for a channel frequency of 2.45GHz. The frequency deviation of the 2Mbps GFSK signal is ±500kHz. The minimum 1% PER sensitivity is -85dBm. The sensitivity ranges from -85dBm to -83dBm in the presence of temperature and supply variations. The achieved sensitivity of -85dBm is within 1dB of the target set for the receiver in section 5.3.1. It should be noted that the sensitivity measurements in Figure 6-28 and Figure 6-29 also show the performance of the digital demodulator of the receiver in addition to the receiver front-end.

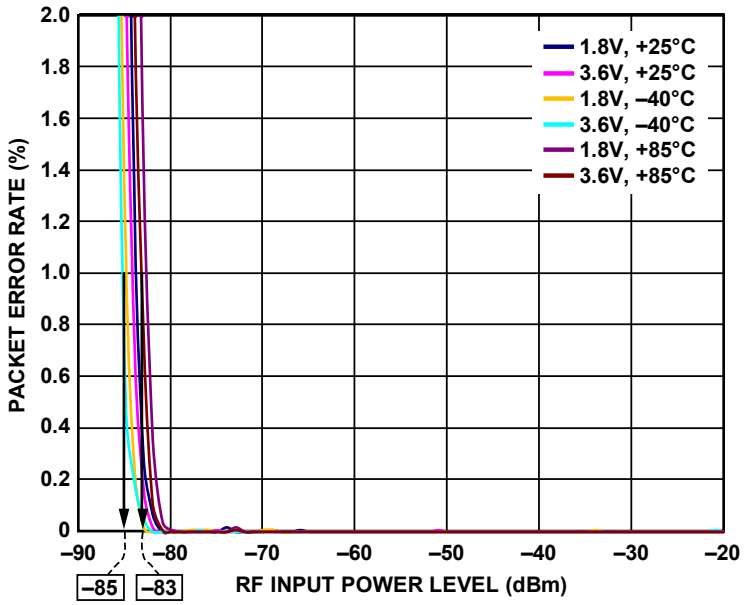


Figure 6-29 Measured 2Mbps GFSK PER sensitivity versus temperature and supply voltage for channel 2.45GHz

Figure 6-30 shows the continuous-wave (CW) blocker level that the RF receiver can handle in the presence of desired 2Mbps GFSK packets placed 3dB above the sensitivity level of -85dBm. The blocker level performance is measured for the entire receiver from the antenna input to the packet RAM output. Hence it includes the entire analog and digital signal processing functions of the receiver. The blocker level is measured by increasing the level of the CW blocker at each frequency offset in the presence of 10,000 2Mbps GFSK packets whose level is 3dB above the sensitivity level of -85dBm. In the absence of any blocker, ideally, all 10,000 packets are received. As the CW blocker level increases, some packets will be lost and will not be received in the packet RAM. The CW blocker level which causes the loss of 1% of the packets is the blocker level reported in the figure. This is a standard method of measuring the blocker level performance of packet-based RF systems [27].

The blocker level is about -31dBm at ±5MHz offset from an RF carrier of 2.45GHz, -26dBm at ±10MHz offset from the RF carrier and -23dBm at ±20MHz offset from the RF carrier. This shows that the receiver is only 1dB short of meeting the ETSI EN 300 440-1 class 1 CW

blocking specifications shown in Figure 5-5 for a 2Mbps GFSK modulated signal. It also highlights the excellent 1dB compression performance of the RF mixer as well as the phase noise performance of the frequency synthesizer at a very low power consumption budget. The plot also shows that the blocking level is very stable in the presence of temperature variations. This indicates the excellent stability of the design in terms of RX channel voltage gain, frequency synthesizer phase noise, low-pass filtering and the LNA's tuned load resonance frequency.

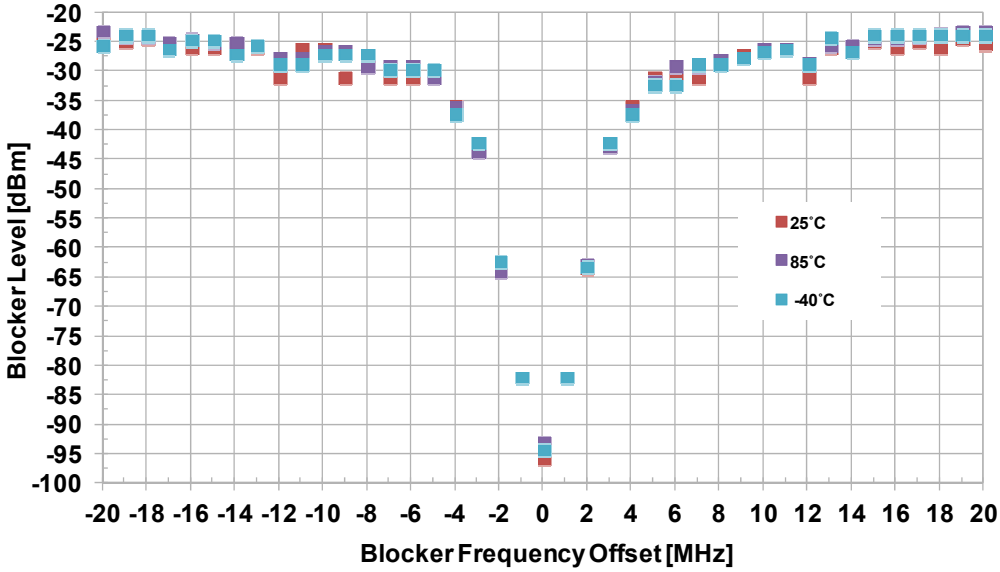


Figure 6-30 Measured CW blocker level for 2Mbps GFSK desired packets at the sensitivity level + 3dB versus temperature for a narrow-band frequency offset from the RF carrier

Figure 6-31 shows that, for the same conditions as in Figure 6-30, the CW blocker level in the presence of 2Mbps GFSK packets can be as high as -20dBm at frequency offsets of up to ±100MHz offset from the RF carrier of 2.45GHz. It is worth pointing out that Figure 6-30 and Figure 6-31 do not show the spurious reception of the RF receiver which degrades the blocker level performance. However, in any RF standard, several spurious reception frequencies are allowed since it is inevitable that the frequency synthesizer of the RF receiver will suffer from spurs particularly at the reference frequency and fractional channels.

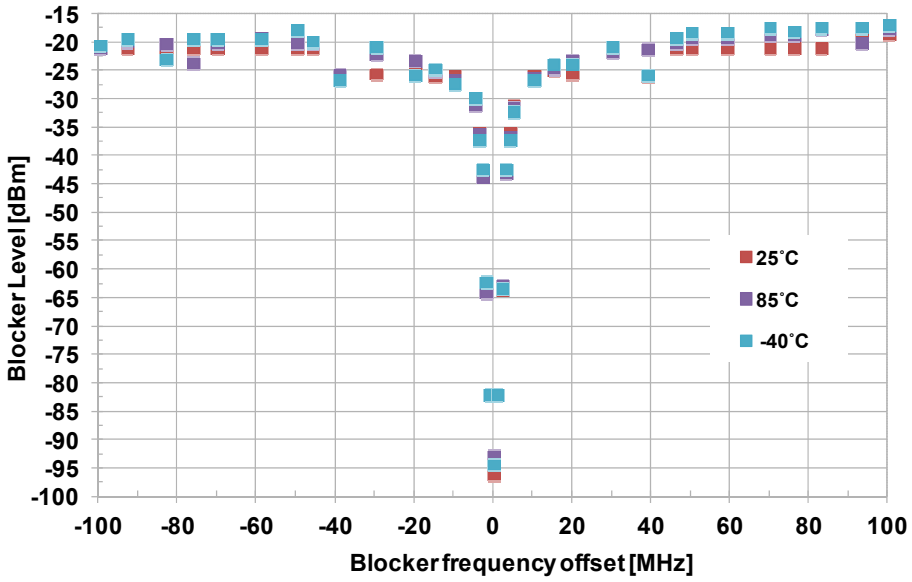


Figure 6-31 Measured CW blocker level for 2Mbps GFSK desired packets at the sensitivity level + 3dB versus temperature for a wide-band frequency offset from the RF carrier

Figure 6-32 shows the CW blocker level which the RF receiver can handle in the presence of IEEE 802.15.4 desired packets at 3dB above the sensitivity level of -95dBm. The blocker level is about -36dBm at ±5MHz offset from an RF carrier of 2.45GHz, -32dBm at ±10MHz offset from the RF carrier and -30dBm at ±20MHz offset from the RF carrier. It can be noticed that the CW blocker level which can be handled by the RF receiver in the IEEE 802.15.4 case is lower than the 2Mbps GFSK case by 5dB, 6dB and 7dB at ±5MHz, ±10MHz and ±20MHz offsets from the RF carrier, respectively. This is attributed to the fact that the IEEE 802.15.4 signal bandwidth is higher than that of a 2Mbps GFSK signal which translates to the need for a higher bandwidth for the RF receiver's LPF. This can be seen in the spectral plot shown in Figure 2-6.

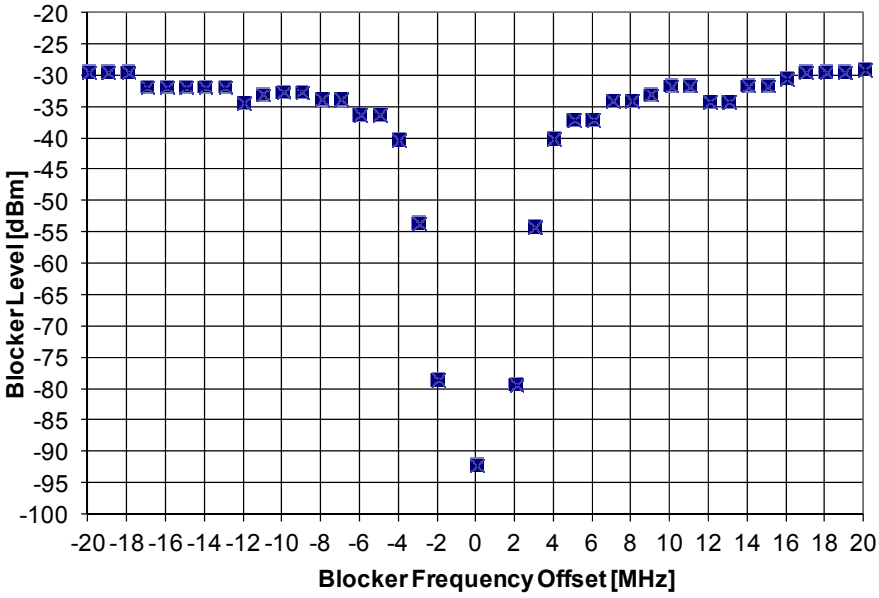


Figure 6-32 Measured CW blocker level for IEEE 802.15.4 desired packets at the sensitivity level + 3dB versus temperature for narrow-band frequency offset from the RF carrier

Figure 6-33 shows that, under the same conditions as in Figure 6-32, the CW blocker level in the presence of IEEE 802.15.4 packets can be as high as -30dBm at frequency offsets of up to ±100MHz offset from the RF carrier of 2.45GHz.

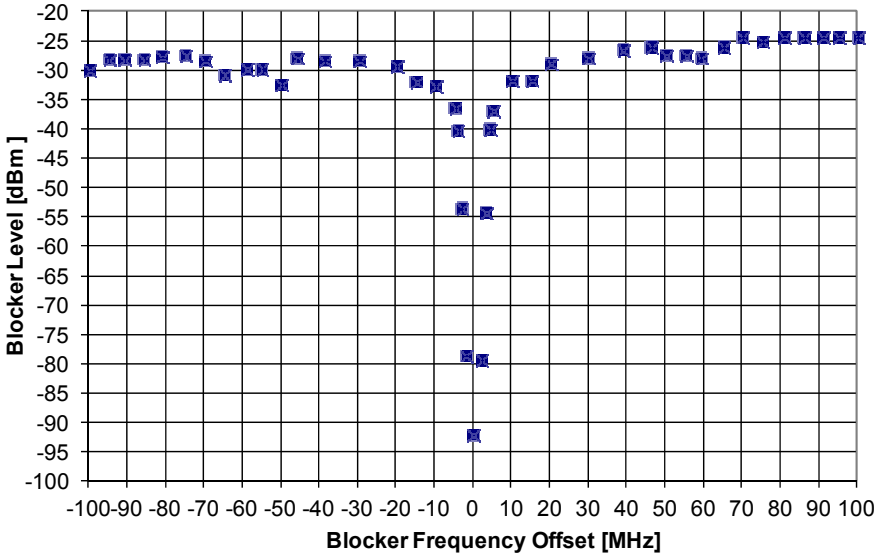


Figure 6-33 Measured CW blocker level for IEEE 802.15.4-2006 desired packets at the sensitivity level + 3dB versus temperature for a wide-band frequency offset from the RF carrier

Figure 6-34 shows a comparison between the measured CW blocker level of this work and the highest performance 2.4GHz commercial device, AT86RF230, available from Atmel Corporation [35], for IEEE 802.15.4-2006 desired packets at the IEEE standard reference sensitivity of -82dBm. This measurement is specified by the IEEE802.15.4 standard and is selected here to be able to fairly compare two devices at a common sensitivity level of -82dBm as specified by the standard. The AT86RF230 device is based on a LIFR architecture. Figure 6-34 reveals that there is no degradation in the adjacent channel rejection due to a mixer image in the ZIFR architecture of this work. This degradation can be seen in the LIFR architecture where the blocker rejection at -5MHz offset is worse by about 4dB when compared to the blocker rejection at +5MHz offset. In addition the ZIFR architecture of this work enabled the implementation of high-order channel filtering much more efficiently than it would have been possible in the LIFR architecture. This translated to an adjacent channel rejection which is about 20dB better for the ZIFR architecture of this work when compared to the LIFR architecture of the AT86RF230.

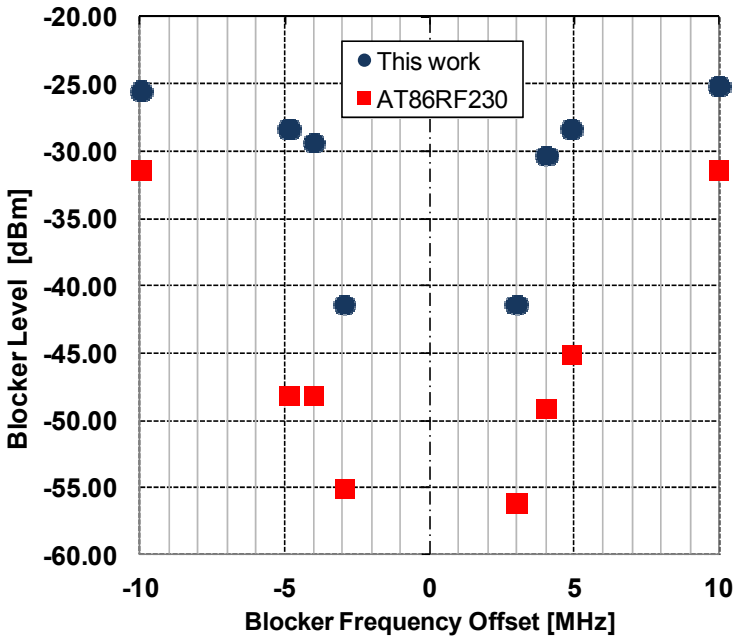


Figure 6-34 Comparison between the measured CW blocker level of this work and the closest high performance device for IEEE 802.15.4-2006 desired packets at the IEEE standard reference sensitivity of -82dBm

Overall, the RF receiver exceeds the ETSI EN 300 440-1 class 2 CW blocking specifications and comes very close to achieving the ETSI EN 300 440-1 class 1 CW blocking specifications owing to the excellent performance of the RF mixer and the frequency synthesizer phase noise. The RF receiver consumes 17mA from a 1.8V supply in a packet-based communication system while achieving the performance highlighted in the preceding figures.

A comprehensive analysis to meet the ETSI EN 300 440-1 class 1 specification is beyond the scope of this work. However, the author believes that reducing the LO phase noise at the expense of an increase in the power consumption of the receiver would be one avenue to pursue to improve the blocking performance by at least 1dB to meet the ETSI EN 300 440-1 class 1 specification.

6.4 Comparison with Prior Art

Table 6-4 shows a comparison of the RF receiver performance with the prior art. In comparison to the 0.18µm IEEE802.15.4 transceiver described by Kluge et al. in [35], the RF sensitivity of this work achieved the target sensitivity of -95dBm. While [35] achieved 6dB better sensitivity, the IIP3 of this work is better by about 2dB. Most importantly, the blocker rejection level of this work in the adjacent channel of ±5MHz from the carrier of an IEEE802.15.4 signal is almost 23dB better compared to [35] due to using a Zero-IF receiver.

Overall the RF receiver dynamic range defined as the blocker rejection level at ±5MHz relative to the RF receiver sensitivity for an IEEE802.15.4 signal is 17dB better compared to [35]. This is achieved with only 15% increase in area and power consumption compared to [35]. In addition, the RF transceiver of this work is a multi-mode transceiver that has a range of modulation schemes and data rates whereas [35] is only an IEEE802.15.4 transceiver.

	Target	This Work (ISSCC'09)	JSSC'06, Kluge [33]
Technology		0.18um CMOS	0.18um CMOS
Receiver Architecture		Zero-IF	Low-IF
Frequency Range	2.402-2.48GHz	2.335-2.6GHz	2.402-2.48GHz
RF Sensitivity (2Mb/s)	-86dBm	-85dBm	Not Applicable
RF Sensitivity (IEEE802.15.4)	**-95dBm**	**-95dBm**	**-101dBm**
IEEE802.15.4 Blocker Level at ± 3MHz		**-41dBm**	**--55dBm**
IEEE802.15.4 Blocker Level at ± 5MHz		**-29dBm**	**-52dBm**
IEEE802.15.4 Blocker Level at ± 10MHz		**-25dBm**	**-32dBm**
IEEE802.15.4 Dynamic Range at ± 5MHz		**66dB**	**49dB**
Noise Figure	**9.2**	**9.6**	**6**
IIP3 (5MHz & 10MHz Blockers)	**-16dBm**	**-13.6dBm**	**-16dBm**
P1-dB (5MHz & 10MHz Blockers)	**-26dBm**	**-24dBm**	
IIP3 (40MHz & 80MHz Blockers)	**-13dBm**	**-10.5dBm**	**Not Reported**
P1-dB (40MHz & 80MHz Blockers)	-23dBm	-20.5dBm	Not Reported
IIP2 (30MHz Blocker)	20dBm	30dBm	24dBm
Phase Noise at 5MHz	-132dBc/Hz	-135dBc/Hz	Not Reported
LO Leakage		-100dBm	-76dBm
Area		1.8mm²	1.45mm²
Power Consumption		31mW (incl. DSP)	27mW

Table 6-4 Comparison of the RF receiver performance with the prior art

6.5 Concluding Remarks

In this chapter, specifications for the building blocks of the ZIFR receiver were developed to meet the system specifications outlined in Chapter 5. Fundamentals of active and passive RF mixers were introduced and compared. The flicker and thermal noise generation mechanisms were also summarized and compared. A design based on a current-commutating passive mixer was described along with the trade-offs in the design.

A novel quadrature generation circuit was detailed in the chapter. The circuit saves up to 9mA in current consumption across process and temperature corners when compared to conventional approaches. Measurements done on the receiver show that key performance parameters such as IIP3, noise figure, 1dB compression, sensitivity and blocker rejection meet or exceed the targets set out for the receiver at the start of the chapter. Specifically, the RF receiver exceeds the ETSI EN 300 440-1 class 2 CW blocking specifications and comes very close to achieving the ETSI EN 300 440-1 class 1 CW blocking specifications.

Chapter 7

RF Receiver's Offset Correction System

7.1 Challenges of Offset Correction Systems in Zero-IF Receivers

Direct conversion receivers offer an opportunity for significant savings in power consumption by down-converting the RF signal directly to the base-band, hence allowing the base-band filtering chain to operate at much lower frequencies compared to other receiver topologies. It also offers superior receiver blocking performance due to the absence of any image rejection constraints which are common in other receiver architectures, most notably in low-IF receivers. Nevertheless, direct-conversion receivers suffer from several drawbacks, mainly flicker noise and dynamic offsets which pose many challenges for the receiver design. In Chapter 6, techniques to mitigate the effect of flicker noise were discussed. This chapter will illustrate design techniques to mitigate the effects of static and dynamic offsets in a direct-conversion receiver.

DC offsets have adverse effects on the operation and performance of wireless communication receivers. They can prevent a desired signal from being received and can seriously degrade the receiver's dynamic range. Two types of offsets exist:

1. Static offsets due to :
    a. Circuit mismatches.
    b. Local oscillator (LO) self-mixing due to the finite isolation between the LO and RF inputs of the mixer.
2. Dynamic offsets due to:
    a. LO radiation from the receiver reflecting from nearby surfaces can eventually self-mix in the direct conversion receiver mixer stages causing time-varying offsets.

b. The LO can also couple to the inputs of the low noise amplifier (LNA) at the receiver input and, due to its high gain, the coupled LO signal is amplified and eventually self-mixes in the direct conversion mixer stage, causing an offset.

c. If the receiver operates in an unlicensed and hence uncontrolled RF frequency band, for example the Industrial, Scientific, and Medical (ISM) band, a near-by transmitter operating on the same channel can self-mix with the LO and cause a time-varying offset at the output of the receiver.

Communication receivers employ an automatic gain control (AGC) circuit which adjusts the receiver gain according to the signal being received to keep the receiver in its linear region of operation. An AGC system cannot differentiate between a desired signal and an offset in the receiver. It reacts to both at the same time and will ultimately fail unless the offset is cancelled well in advance of the AGC acquisition phase of the desired signal.

There are certain requirements which have to be considered in ultra low power receivers:

1. The receiver should be powered up for the least amount of time while waiting for the desired signal to arrive in order to minimize the power consumed while the receiver is idle.
2. The receiver should be able to detect an incoming signal in a very short time window defined by different wireless standards. During this short time window, the receiver is required to adjust its gain using the AGC system and synchronize to the incoming bit pattern.
3. The design of the receiver has to satisfy both ultra low power operation and very small silicon area. This has to be achieved while meeting relatively low noise and high linearity specifications for the circuits used to cancel the offset.

In light of the above requirements, there is a need to:

1. Design an offset correction loop (OCL) which cancels static and dynamic offsets in the least amount of time. The target for the IEEE 802.15.4 receiver of this work is less than 20μs.
2. The OCL has to operate with very low power and occupy a small silicon area.

There are several OCL implementations which attempt to overcome the aforementioned challenges in highly integrated RF transceivers. For example, Vassiliou *et.al.* [55] use a look-up table DC offset correction approach by stepping through all the base-band gains as well as all channel frequencies. The DC offset at the receiver output is measured in each case and stored in the look-up table where it is subsequently subtracted from the base-band input using an offset correction DAC. While simple, this implementation means that the receiver has to stop its normal signal reception function whenever an offset correction is performed. In addition, the implementation does not account for time-varying offsets and consumes a significant amount of time in building the look-up table for cancelling the DC offsets. Magoon *et.al.* [56] use multiple analog DC offset cancellation loops for every gain stage, as well as an offset-frequency architecture to avoid the offset correction challenges associated with direct conversion receivers. However, an offset-frequency architecture uses power-hungry multipliers for LO generation which would be detrimental for power-sensitive applications. Perraud *et al.* [57] use an integrated offset correction DAC to cancel the DC offsets and an external controller to sense the offset and provide an input to the offset correction DAC; using a DSP or a microcontroller is a rather expensive solution for a cost-sensitive application.

7.2 RF Receiver's Offset Correction Architecture

In order to meet the requirements outlined in the previous section, several design methodologies are adopted in this work:

1. The power consumption of a digital implementation is easier to scale down with supply voltage, operating frequency and process geometries. In addition, the OCL can be designed to fit in a small area while achieving low noise. The approach is to push the majority of the design of the OCL into the digital domain and to use a minimal amount of analog circuitry, hence easing the trade-offs between low power consumption, small area and low noise.
2. Minimize the requirements of the inevitable analog circuitry to be used in the OCL design in terms of noise, power consumption and silicon area. This can be done by using digitally-assisted techniques to improve the performance of the analog circuitry.

The proposed OCL uses digitally-assisted analog techniques and cancels the two types of offsets in two major phases [58]; first, a static DC offset cancellation phase and subsequently, a dynamic offset cancellation phase. This partitioning is vital because:

1. It reduces the complexity of the digital-to-analog converters (DACs) used in the receiver in terms of resolution and dynamic range since the OCL needs a low resolution DAC for static DC offset cancellation but needs a high resolution DAC to track and cancel the time-varying offsets without interfering with signal reception.
2. It reduces the amount of time needed to cancel dynamic offsets in the receiver because it allows the OCL to employ various techniques to speed up the cancellation of this type of offset without worrying about the static DC offsets which have been already cancelled in the first phase. By design, the static DC offsets do not change significantly once they have been cancelled at the maximum base-band gain.

The two phases of the OCL are discussed in the following subsections.

7.2.1 Static DC Offset Cancellation Phase

Figure 7-1 shows a simplified block diagram of the equivalent analog OCL concept adopted in this work. G_{rx} and $H_{rx}(s)$ are the gain and transfer function of the cascade of the receiver's

baseband low-pass filter and programmable gain amplifier respectively. G_{fb} and $H_{fb}(s)$ are the gain and the transfer function of the feedback path of an equivalent analog OCL respectively. V_{os} is the static DC offset to be cancelled by the OCL

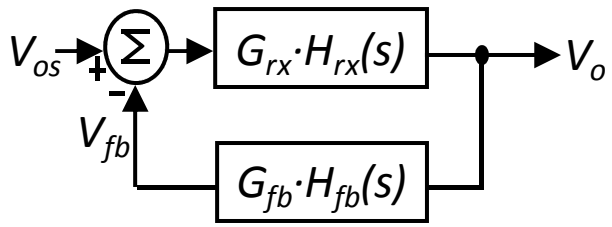


Figure 7-1 Simplified block diagram of the OCL

The closed-loop transfer function of the OCL is given by:

$$H_{ocl}(s) = \frac{G_{rx}H_{rx}(s)}{1 + G_{rx}G_{fb}H_{rx}(s)H_{fb}(s)}, \tag{7.1}$$

Here,

$$H_{fb}(s) = \frac{1}{\left(\frac{s}{\omega_{ugf}}\right)}, \tag{7.2}$$

where, ω_{ugf} is the unity-gain frequency of the integrator. Intuitively, placing an integrator in the feedback path of the receiver's baseband creates a high pass filter in the receiver transfer function. Since the gain of the integrator is infinite at DC, the integrator forces the output V_o to be zero at DC. At DC, the gain of the integrator is infinite which forces its input V_o to zero and V_{fb} to be equal to V_{os}. As the frequency increases, the integrator gain is reduced until it reaches unity at its unity-gain frequency ω_{ugf}.

If, for simplicity, we assume that $H_{rx}(s) = 1$ in (7.1), the closed-loop transfer function of the OCL is given by:

$$H_{ocl}(s) = \frac{G_{rx}}{1 + \frac{G_{rx}G_{fb}\omega_{ugf}}{s}} \tag{7.3}$$

Equation (7.3) shows that the closed-loop transfer function of the OCL exhibits a high-pass characteristic. As the frequency increases towards infinity, i.e, s→∞, the magnitude of the OCL transfer function approaches G_{rx}. The high-pass corner of the OCL transfer function is approximately given by the magnitude of the loop gain $G_{rx}.G_{fb}$ times the unity-gain frequency of the integrator:

$$\omega_{hpf} = G_{rx} G_{fb} \omega_{ugf} \tag{7.4}$$

The relationship indicated by (7.4) is essential to the operation of the OCL. Figure 7-2, shows a block diagram for the OCL adopted in this work. The OCL shown in the figure is based on the concept shown in Figure 7-1 where a discrete-time integrator is added to the feedback path to facilitate a fully digital implementation. The OCL operates in two phases; the first phase is the static DC offset cancellation phase and the second phase is the dynamic offset cancellation phase.

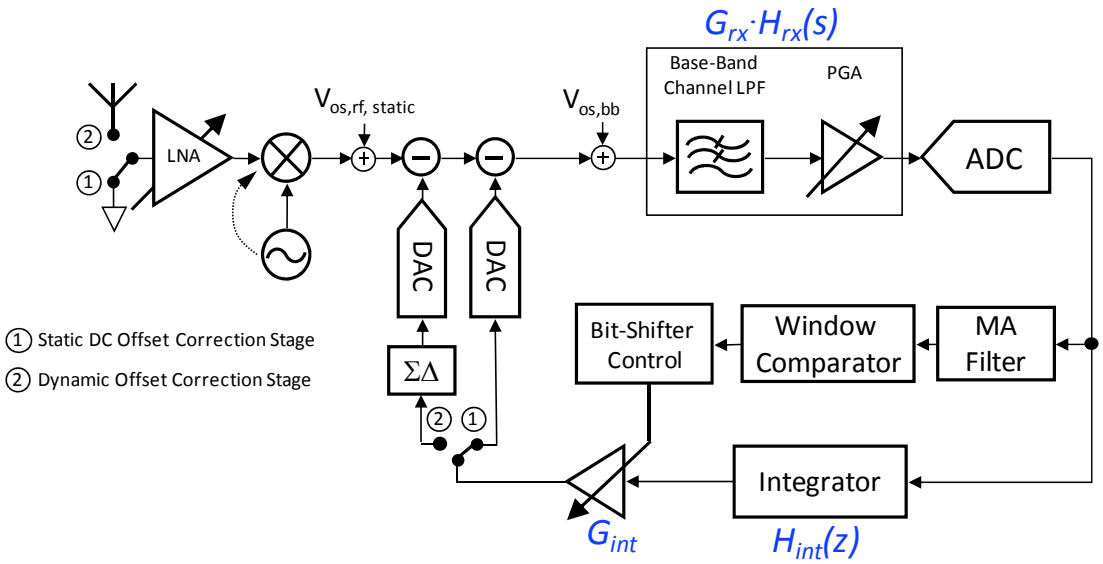


Figure 7-2 Simplified block diagram of the OCL (only the I channel of the receiver is shown)

The static DC offsets are represented as $V_{os,bb}$ and $V_{os,rf,static}$. $V_{os,bb}$ represents the DC offsets in the base-band channel of the receiver after the RF mixer due to circuit mismatches. $V_{os,rf,static}$

represents the DC offsets resulting from the on-chip coupling between the LO and RF ports of the RF mixer due to the finite isolation between these ports.

The OCL is implemented by integrating the output of the receiver's ADC using a discrete-time integrator in the digital domain whose transfer function is given by:

$$H_{\text{int}}(z) = \frac{1}{1 - z^{-1}} \tag{7.5}$$

G_{int}, in Figure 7-2 is the gain of the digital integrator and is equivalent to G_{fb} in (7.1). The equivalent analog closed-loop OCL transfer function for the OCL shown in Figure 7-2 is given by:

$$H'_{ocl}(s) = \frac{G_{rx}H_{rx}(s)}{1 + G_{rx}G_{\text{int}}H_{rx}(s)H_{\text{int}}(e^{sT_s})}, \tag{7.6}$$

where, $H_{int}(e^{sTs})$ is the analog equivalent of the discrete-time integrator and T_s is the sampling time of the integrator. The output of the discrete-time integrator is gained by G_{int} using a simple bit-shifting operation to realize a divide or a multiply by two for the samples at the output of the integrator. Depending on the amount of bit-shifting, the unity-gain frequency of the discrete time integrator can be set according to (7.4) which, in turn, changes the high-pass corner of the OCL. This implementation has two advantages:

1. The ability to control the bandwidth of the OCL system by simple bit-shifting operations translates into being able to speed-up and slow-down the system easily in different phases of offset cancellation according to the offset level. This will be discussed in detail in subsequent sections.
2. The ability to adjust the feedback path gain of the OCL easily by using the bit-shifter allows for an easy and fast method for the system to compensate for the change in gain in the feed-forward path. The gain in the feed-forward path of the OCL feedback loop is adjusted according to the signal level in the receiver chain and is controlled by the AGC. This gain change takes place in the programmable gain amplifier (PGA)

shown in Figure 7-2 when the receiver input is enabled and is ready to receive the desired signal.

If an undesired signal of a relatively high power level appears at the input of the receiver during the static DC offset cancellation phase, the receiver output can saturate. This will cause the OCL to fail to cancel this offset. During the static DC offset cancellation phase, the receiver input is grounded, as shown in Figure 7-2. Hence, most of the RF power appearing at the receiver's input will be reflected.

The effect of the bit-shifting operation of the digital feedback gain on the high-pass corner of the closed-loop transfer function of the OCL described by (7.6) is shown in Figure 7-3. In the figure, for a nominal value of the integrator gain G_{int0}, the nominal high-pass corner is 5kHz. If a digital gain of $1/4 \cdot G_{int0}$ is employed using a digital operation in the form of a shift-right by 2, the high-pass corner becomes 1.25kHz or 1/4·5kHz. On the other hand, if a digital gain of $4 \cdot G_{int0}$ is employed using a digital operation in the form of a shift-left by 2, the high-pass corner becomes 20kHz or 4·5kHz. The OCL system has a programmable range for the high-pass corner between 0.125kHz and 1504kHz.

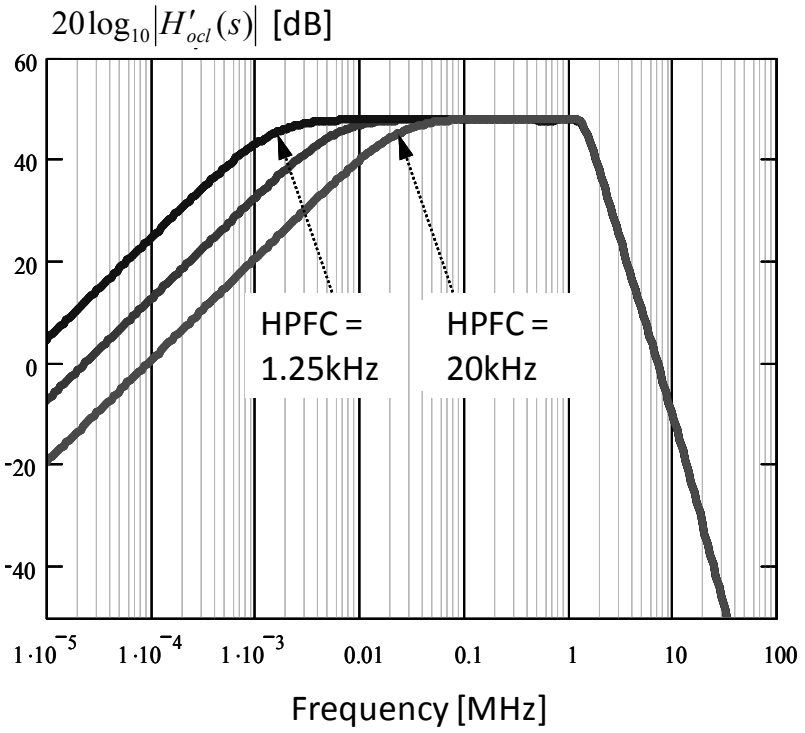


Figure 7-3 Effect of changing the digital feedback gain on the closed-loop transfer function of the OCL

Figure 7-4 shows the effect of compensating for a change in the feed-forward gain of the receiver by adjusting the digital feedback-gain to keep the high-pass corner constant. In the figure, the PGA gain is reduced by 42dB. The value of G_{int} is increased by a factor of 128 to keep the OCL loop gain approximately constant. The high-pass filter corner of the OCL stayed approximately unchanged at 6kHz.

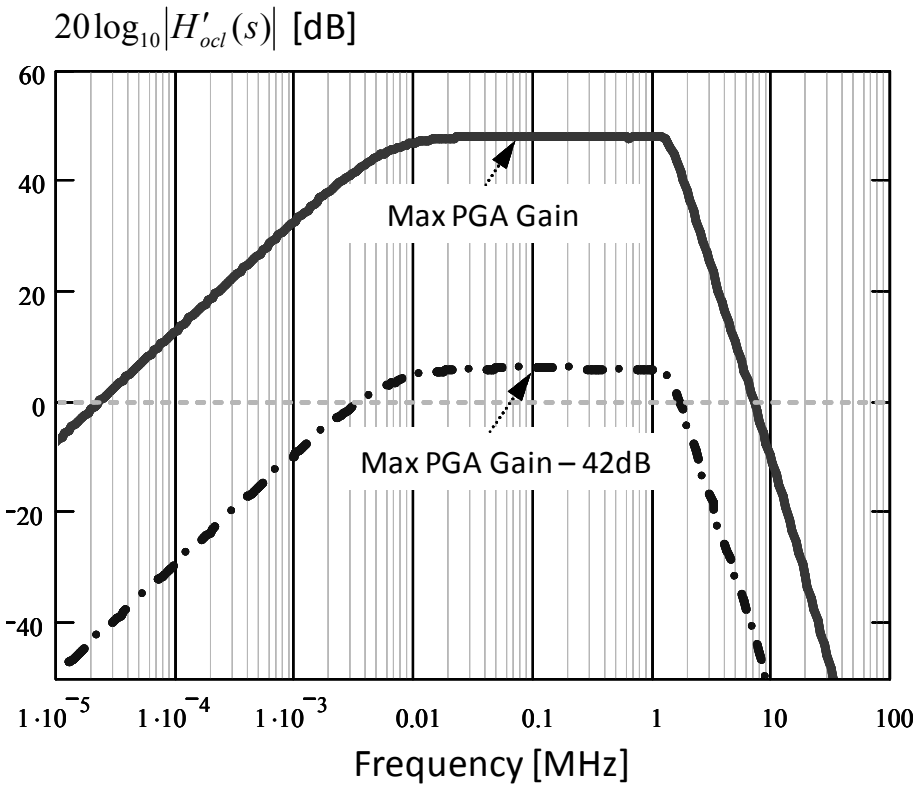


Figure 7-4 Effect of adjusting the digital feedback gain to keep the high-pass corner of the OCL closed-loop transfer function constant with PGA gain changes

As shown in Figure 7-2, the output word of the bit-shifter is fed into a current steering DAC. The output of the DAC is converted into voltage in a trans-impedance amplifier at the output of the RF mixer (For simplification, the details of this conversion are not shown in Figure 7-2). The LSB size of the DAC is limited by the residual offset required at the output of the ADC. The dynamic range of the DAC is set at the lower end by this LSB size and at the higher end by the full-scale offset which the DAC needs to cancel.

Since the static DC offsets in the receiver will most likely cause the ADC output to saturate, it is possible to operate the OCL at very high speed until the DC offsets are mostly cancelled and the receiver baseband chain leaves the saturation condition and enters a linear region of operation. Once the majority of the DC offset is cancelled, the OCL has to be slowed down to avoid instability in the feedback loop. This speed-up of the OCL saves valuable power-up

time for the receiver compared to operating the system at a constant speed regardless of the DC offset level. The speed-up and slow-down operation is controlled using the window comparator indicated in Figure 7-2. A moving average (MA) filter averages the ADC output for a specified period of time and a window comparator indicates the level of the DC offset at the ADC output. The window comparator output is used to control the amount of bit-shifting performed on the output of the integrator which in turn sets the high-pass corner of the OCL to control its speed. The MA filter has a programmable range for the number of samples to be averaged between 4 samples and 1024 samples.

The static DC offset cancellation is performed while using the maximum base-band gain which guarantees the minimum residual DC offset at the ADC output. When the AGC changes the base-band gain in subsequent stages of operation, the DC offset $V_{os,bb}$ could change slightly. To reduce the effect of any change in the static DC offset, a fixed gain of 12dB is maintained at the input of the base-band chain to suppress the variation of the input-referred offset $V_{os,bb}$ when the gain changes.

Once the window comparator indicates that the DC offset at the ADC output has been cancelled to the desired number of LSBs, the OCL terminates this phase and moves to the dynamic offset cancellation phase. The static offset DAC code is held during the dynamic offset cancellation phase. Figure 7-5 shows a simulation for the overall static offset cancellation phase. The plot shows the OCL state, the output of the window comparator (offset level), the input to the ADC in the receiver, and the output of the coarse DAC used for static offset correction.

At the start of the cancellation phase, the offset level is high; this is indicated by the window comparator output as level 2. As a result, the bandwidth of the OCL is increased to the maximum possible value until the offset level drops to the level that allows the receiver chain to operate linearly. The window comparator indicates that the offset level has dropped to a

medium value, labeled as level 1. As a result, the OCL decreases the bandwidth of the loop to prevent the system from becoming unstable. This continues until the offset level drops to the minimum value which is indicated by the output of the window comparator as level 0. As soon as this occurs, the OCL terminates this phase and moves on to subsequent phases. Cancelling a full-scale static DC offset takes 9μs as a result of these speed-up mechanisms.

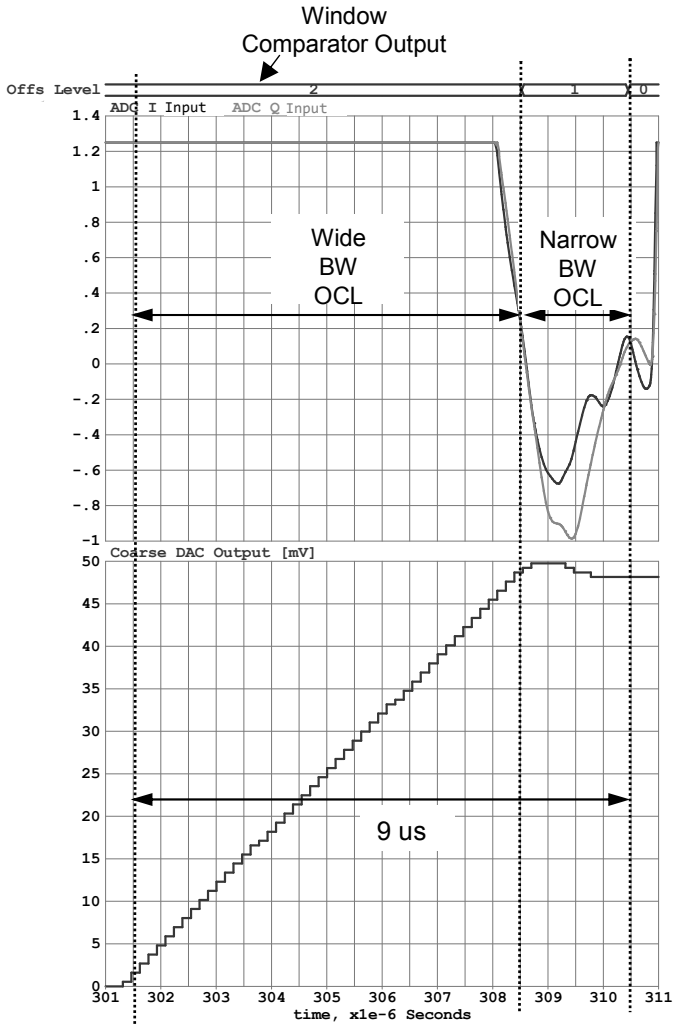


Figure 7-5 Simulation result of the static DC offset cancellation phase.

7.2.2 Dynamic Offset Cancellation Phase

Figure 7-6 shows the second phase of the OCL which is the dynamic offset cancellation phase. In this phase, the OCL operates as follows:

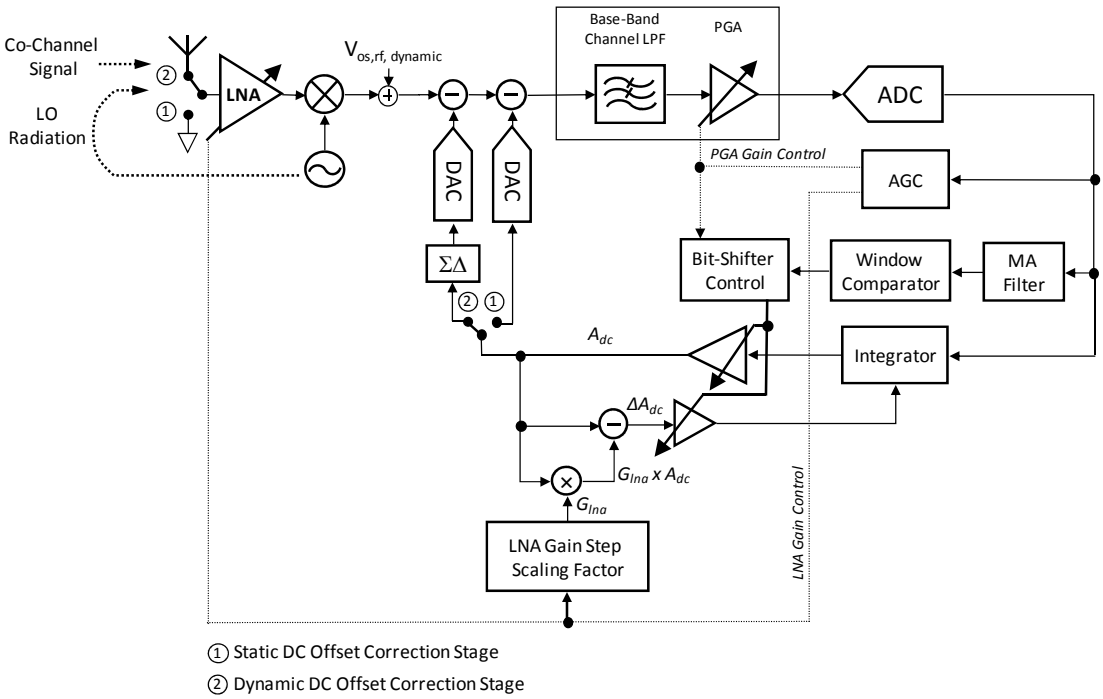


Figure 7-6 Block diagram of the dynamic time-varying offset cancellation loop

The offset $V_{os,rf,dynamic}$ is the dynamic time-varying offset due to LO radiation and reflection back to the receiver input as well as co-channel signals. To cancel this type of offset at the mixer's output, the dynamic offset cancellation phase starts by enabling the LNA. The static DC offset cancelled in the first phase is held constant during the dynamic offset cancellation phase using the static DC offset DAC.

The dynamic offset in this phase is cancelled during signal reception. Hence, the quantization noise of the dynamic offset correction DAC has to be much lower than the noise contributed by the receiver chain, i.e. the contribution of the DAC to the overall noise figure of the receiver has to be negligible.

From the receiver's system analysis in section 6.1.2, it was found that in order to reduce the DAC quantization noise, a high resolution DAC is required. The resolution required to minimize the degradation of the noise figure of the receiver is 11-bits over the Nyquist bandwidth of the DAC. The DAC has to have very low noise in addition to maintaining its

monotonicity over that range. For a low power, area-sensitive receiver design, a conventional current-steering DAC, with this large dynamic range, could consume a large silicon area and is prohibitive.

The solution adopted in this work is a sigma-delta (ΣΔ) modulator current-steering DAC. A simplified block diagram of the concept of a ΣΔ modulator, using an error-feedback noise-shaping loop, is shown in Figure 7-7. The equations governing the operation of the ΣΔ modulator are as follows:

$$E_q(z) = Y(z) - E_i(z) \tag{7.7}$$

$$X(z) - E_q(z) \cdot H(z) = E_i(z) \tag{7.8}$$

where, $E_i(z)$ and $E_q(z)$ are the quantization errors of the signal before and after truncation respectively.

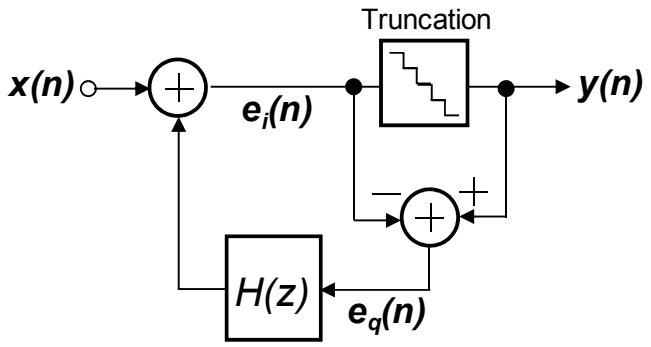


Figure 7-7 Simplified block diagram of the concept of an error-feedback ΣΔ modulator

From equations (7.7) and (7.8), one can deduce the following:

$$Y(z) = STF(z) \cdot X(z) + NTF(z) E_q(z), \tag{7.9}$$

where $STF(z)$ and $NTF(z)$ are the signal and noise transfer functions of the error-feedback ΣΔ modulator respectively and are given by:

$$STF(z) = 1 \tag{7.10}$$

$$NTF(z) = 1 - H(z) \tag{7.11}$$

For a third order ΣΔ modulator, $NTF(z)$ is given by:

$$NTF(z) = (1 - z^{-1})^3 \quad \textbf{(7.12)}$$

Equation (7.12) indicates that the zeros of the NTF are located at DC and provide a null for the quantization error, $E_q(z)$, resulting from the truncation of the input signal, $x(n)$. Hence, a ΣΔ DAC has the potential to preserve the quantization level of the input signal even after it is truncated by several bits. This substantially reduces the analog requirements of the OCL DAC needed for time-varying offsets.

Figure 7-8 shows the concept of the ΣΔ DAC using a third-order error-feedback noise-shaping loop [58] [59]. Despite being a powerful choice, the ΣΔ DAC design comes with a number of challenges:

1. The ΣΔ DAC needs to have a low in-band quantization noise over the receiver channel bandwidth of 1.3MHz so as to negligibly degrade the receiver's noise figure.
2. The ΣΔ DAC needs a low-pass filter at its output in order to filter the out-of-band quantization noise beyond the receiver's channel bandwidth of 1.3MHz and thereby avoid any noise aliasing which could increase the in-band noise of the receiver.

Figure 7-8 shows the detailed implementation of the ΣΔ DAC used in this work. With a 15-bit output from the digital engine of the OCL, 8 bits are truncated and fed-back to the ΣΔ modulator. The remaining 7 bits act as an input to a current steering DAC. The dynamic range of a 7-bit current steering DAC is sufficient to cancel the dynamic offset, $V_{os,rf,dynamic}$, of the receiver. The ΣΔ modulator operates at 13MHz which gives an over-sampling rate (OSR) of 10 relative to the receiver channel bandwidth of 1.3MHz. This OSR is not particularly high. To meet the noise requirements, the modulator was chosen to be third order. A third-order modulator keeps the in-band quantization noise low at the expense of increasing the out-of-band quantization noise which is eventually filtered with a low-pass filter. The design does not use a separate low-pass filter to filter the out-of-band quantization noise. Rather, the

receiver's base-band channel filter acts as one at the desired bandwidth of 1.3MHz as shown in Figure 7-8. This significantly reduces the area and power consumption of the receiver.

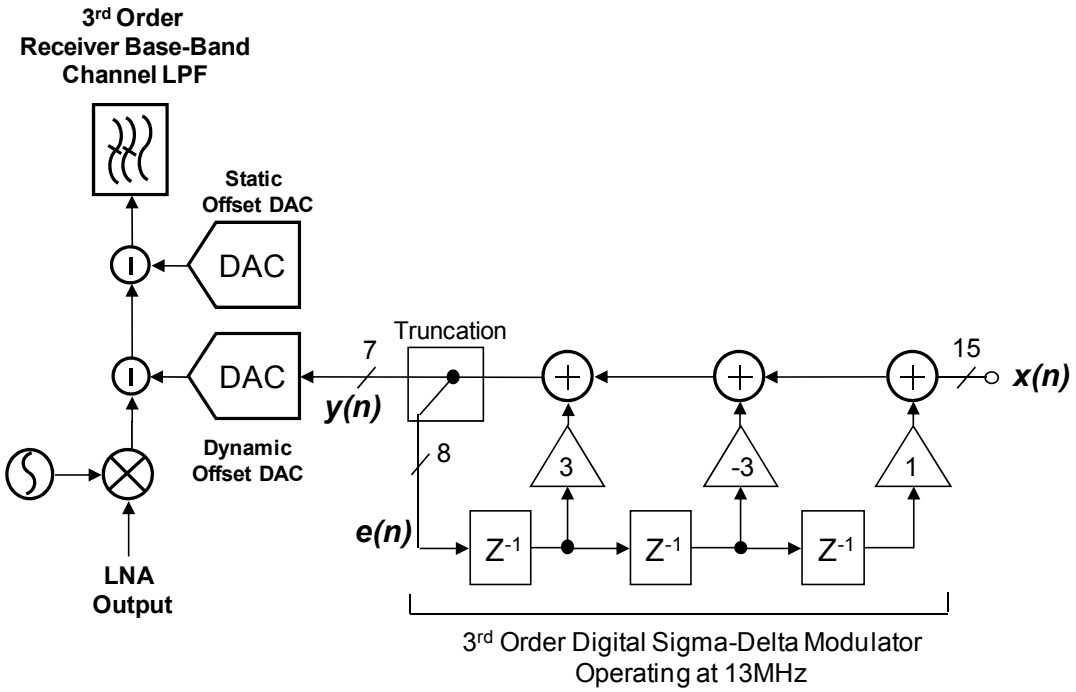


Figure 7-8 Details of a third-order error-feedback ΣΔ DAC

Figure 7-9 shows the power spectral density of the input and output of the ΣΔ DAC for an input tone frequency of 5.15kHz with a 90% of the full-scale amplitude of the 15-bit input of the ΣΔ modulator. The plot shows the normalized power spectral density in dB/Hz relative to the peak amplitude versus the normalized frequency relative to the ΣΔ DAC sampling frequency of 13MHz. As shown in Figure 7-8, the input of the ΣΔ DAC is 15-bits while the output is truncated to 7-bits. The theoretical SNR of the 15-bit input signal to the ΣΔ modulator is approximately 99dB over the bandwidth of the receiver's channel low-pass filter of 1.3MHz which is 10% of the sampling frequency of the ΣΔ DAC. As a result of using an error-feedback ΣΔ modulator, the in-band quantization noise of the output signal is equivalent to 15-bits. However, the third order ΣΔ modulator pushes the out-of-band quantization noise to a higher level at a slope of 60dB/decade, as shown in Figure 7-9. Hence, the SNR of the

output signal of the ΣΔ modulator over the bandwidth of the receiver's channel low-pass filter of 1.3MHz is 77dB due to the noise shaping characteristics of the ΣΔ modulator, yielding an effective number of bits (ENOB) of 12.5-bits. There is no explicit filtering provided at the output of the ΣΔ modulator except for the receiver's channel low-pass filter. Using the architecture shown in Figure 7-8, an explicit filter is avoided due to the additional noise incurred by such a filter in the receiver's signal path.

The important aspect of using a ΣΔ modulator is the reduction of the analog resolution needed in the DAC from 15-bits to 7-bits, which is a significant reduction in analog complexity. It is important to also note that the SNR of a 7-bit signal is approximately 51dB over the bandwidth of the receiver's channel low-pass filter of 1.3MHz without using a ΣΔ modulator. Hence, a ΣΔ modulator improves the SNR at the 7-bit DAC output by 26dB over the same bandwidth. With an ENOB of 12.5-bits, the integrated quantization noise of the ΣΔ DAC is 23dB below the integrated noise of the RF mixer in the receiver's channel bandwidth. Hence, the contribution of the ΣΔ DAC to the noise figure of the receiver is negligible.

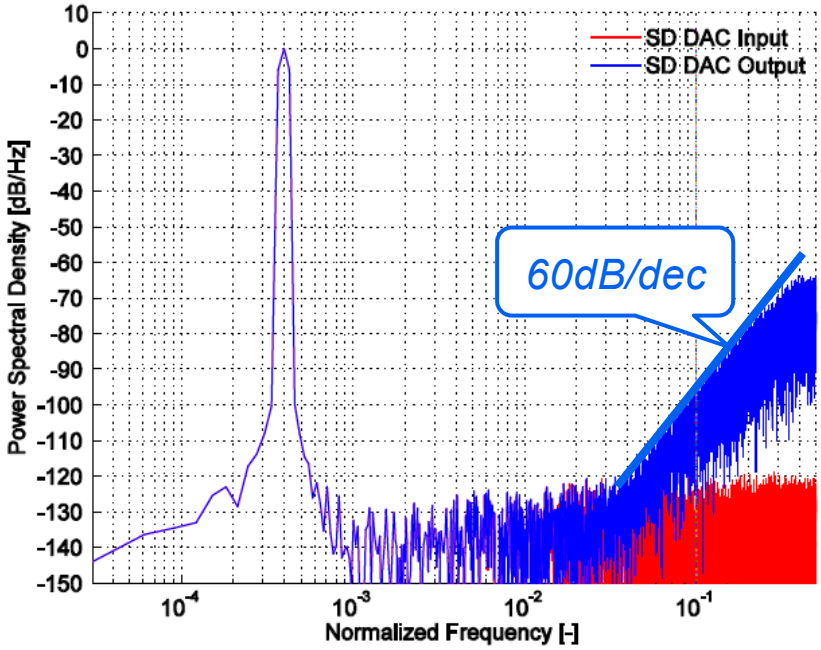


Figure 7-9 Power spectral density of the input and output of the ΣΔ DAC

Referring back to Figure 7-6, at the start of the dynamic offset cancellation phase, the AGC system is disabled and the receiver gain is set to its maximum value. Since the receiver is enabled, a strong desired signal could saturate the receiver and prevent the OCL from fully cancelling the dynamic offsets. Even if the desired signal is not immediately present at the receiver's input, a strong co-channel signal, originating from another unregulated communication system, could be present at the receiver's input and this could cause the receiver to saturate. The OCL and AGC systems have to cope with this scenario. Let us consider two cases which the OCL system could potentially handle; one in which a strong co-channel signal is present at the receiver input and another in which a strong co-channel signal is absent.

In the absence of a strong co-channel signal, the OCL operates in a similar manner to the static offset cancellation phase. The discrete-time integrator integrates the offset appearing at the ADC output. The output of the integrator is bit-shifted according to the set OCL system's bandwidth. The output of the bit-shifter, A_{dc} in Figure 7-6, acts as an input to the ΣΔ DAC. In addition, a moving average filter averages the ADC samples and a window comparator detects the level of the offset in the integrated ADC output and accordingly adjusts the bandwidth of the OCL until the offset is fully cancelled. After the OCL detects that the offset has been fully cancelled, the following occurs:

1. The OCL system enables the AGC system.
2. The OCL system reduces its bandwidth considerably such that it only filters a small portion of the spectrum of the received signal, so as not to affect its signal-to-noise ratio. For example, for a 2Mbps GFSK signal, the maximum high-pass filter corner of the OCL is set to 2kHz, whereas for a 250kbps DSSS MSK signal, the maximum high pass filter corner is 15kHz.

If a strong co-channel signal is present, the OCL will not be able to cancel the dynamic offset $V_{os,rf,dynamic}$ fully in the allocated time. This is because the receiver is saturated due to the high

signal level present at its input which makes the offset estimation process very long. The OCL has a time-out period after which it moves to the next state. If the offset has not been fully cancelled, which is indicated by the window comparator, the timeout value will be reached and the OCL will move on to enable the AGC system.

Once the AGC is enabled, the receiver's gain is reduced due to the high co-channel signal level. In our communication system, the co-channel signal is always lower than the desired signal. For example, for an IEEE802.15.4 signal, a co-channel can only be up to 6dB below the desired signal level. Hence, the AGC will establish a higher gain in the receiver chain in the presence of the co-channel signal than that for the desired signal. The OCL will fully cancel the residual offset which wasn't cancelled before enabling the AGC. This residual offset is also cancelled at a higher gain level than the one which the AGC will establish when the desired signal arrives. This results in an even lower residual offset.

As indicated earlier, as soon as the AGC is enabled, the receiver is ready for the desired signal and the OCL reduces its bandwidth to a considerably low value depending on the type of signal being received. If the signal level is very high, the AGC will change the LNA gain. Since the majority of signals causing dynamic offsets pass through the LNA as shown in Figure 7-6, the level of the dynamic offset will change according to the LNA gain.

The LNA gain updates occur instantaneously. Hence, the OCL, due to its narrow bandwidth, will not be able to quickly cancel the new dynamic offset level as a result of an LNA gain change. This means that the AGC will detect a high dynamic offset level at the ADC output which will confuse its signal detection algorithm. As a result, the AGC can arrive at the completely wrong gain level in the receiver. Since the AGC system is required to establish the receiver gain in the smallest possible time (the target is less than 20μs), it is not possible to stop the AGC and cancel the offset for every gain update. To overcome this challenge, the solution adopted in this design is as follows:

1. The OCL is provided with an estimate of the new offset level when the LNA gain changes. This estimate is equal to a scaled value of the existing offset level (before an LNA gain change takes place) with the current LNA gain step.
2. Whenever an LNA gain update occurs, the OCL bandwidth is increased substantially such that any errors in the offset estimate in the previous step (1) can be quickly cancelled before the AGC reacts to it. This bandwidth extension takes place during the LNA gain update and is controlled by a time-out period.
3. Figure 7-6 shows the implementation of the scaling mechanism. The mechanism works as follows:
    a. The idea is to provide an estimate for the dynamic offset when there is an LNA gain change. This is implemented by adding an estimate of the dynamic offset, ΔA_{dc}, when there's an LNA gain change to the current dynamic offset DAC code, A_{dc}. ΔA_{dc} is computed by scaling A_{dc} with the current LNA gain step, G_{lna}, and subtracting A_{dc} from the result i.e, $\Delta A_{dc} = G_{lna} \times A_{dc} - A_{dc}$. Thus for example, if the LNA gain drops by 12dB, A_{dc}, is scaled by a factor of 1/4 and then A_{dc} is subtracted from this value, yielding a value of $-3/4 \times A_{dc}$ for $\Delta A_{dc.}$
    b. ΔAdc is then inversely scaled with the current feedback gain (bit-shifting setting) in the feedback path and added to the OCL integrator. The resulting effect is adding the value of ΔA_{dc} to the current dynamic offset DAC code, A_{dc}, when there is a change in the LNA gain. This yields a total value of $1/4 \times A_{dc}$ hence the current value of the offset is scaled by the exact amount of the LNA gain step.
    c. Since the addition of ΔA_{dc} occurs in the integrator, any errors in the estimation of the scaling factor by which the offset is scaled will eventually be corrected by the OCL loop. The error can be minimized by providing a look-up table (LUT) for the LNA gain step scaling factors which can be adjusted based on silicon results.

d. After ΔA_{dc} has been applied to the integrator, the bandwidth of the OCL is increased for a specified period of time to correct for any errors made in the estimation of ΔA_{dc} before the AGC reacts to any of these errors.

The bandwidth of the OCL has to be maintained whenever the PGA gain is changed. This is done by updating the feedback path gain using bit-shifting whenever there is a 6dB PGA gain step. The following is considered:

1. The update made to the feedback path gain does not cause any steps at the output of the offset correction DAC to avoid corrupting the signal being received with glitches from the DAC. These glitches can also prevent the AGC system from determining the signal level correctly. This is done by adding a value which is equivalent to the step caused by the bit-shift-by-2, due to the bandwidth change, to the integrator. As a result, the step is hidden from the feedback system when the OCL bandwidth changes.

2. The change in the static DC offset levels due to the PGA gain changes should be kept to a minimum. This is satisfied using the following:
    a. The static DC offset cancellation phase is done at the maximum PGA gain setting. Hence, the residual offset is minimized at lower PGA gain settings.
    b. The gain line-up in the receiver is chosen such that there is a fixed gain of 12dB at the input of the base-band chain to reduce the input-referred static DC offset. Hence, the small residual offset at lower PGA gain steps does not significantly affect the total input-referred DC offset.

Figure 7-10 to Figure 7-13 show simulations of the dynamic offset correction loop in its various phases. Figure 7-10 shows the initial phase of the dynamic offset correction loop. After the LNA is enabled, a dynamic offset appears at the RF mixer output. The OCL cancels the dynamic offset once the LNA is enabled. The figure shows the target offset to be

cancelled as well as the output of the offset correction ΣΔ DAC. The AGC is not enabled while the OCL is initially cancelling the dynamic offset. Furthermore, the PGA and the LNA gains are held at their maximum values. The OCL starts the cancellation phase with a very wide bandwidth in order to zero the offset quickly. The residual dynamic offset is measured using a MA filter and the window comparator. Once the dynamic offset level drops below a specified level, the OCL bandwidth is reduced to the minimum value which is suitable for the signal being received.

If either the dynamic offset has been reduced to zero or a specified time-out period has elapsed, the OCL state machine enables the AGC system. The duration of the time-out is limited by the amount of time allocated for the initial power-up of the receiver. Once the AGC system is enabled, and if there is a desired signal present at the receiver's input, the AGC will update the LNA and PGA gains to adjust the total receiver gain.

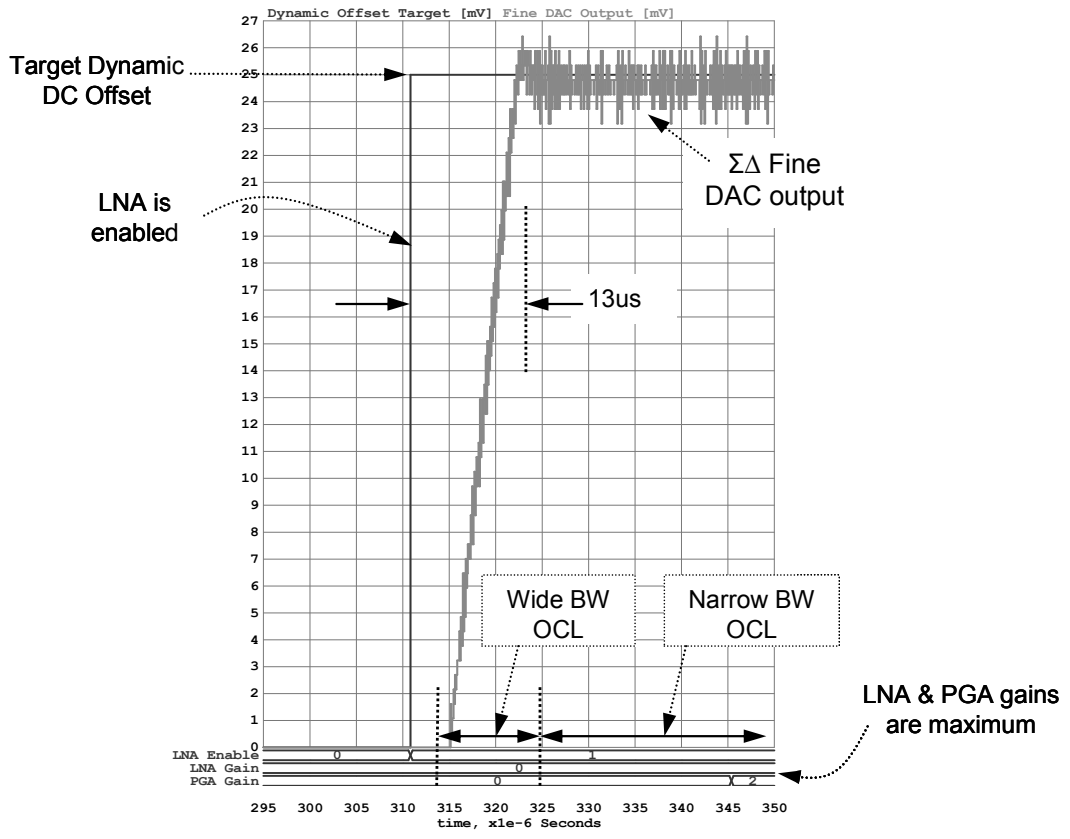


Figure 7-10 Simulation of the OCL during the dynamic offset cancellation phase

Figure 7-11 shows a simulation for a -50dBm signal at the receiver's input shortly before the AGC is enabled. Once the AGC is enabled and starts to acquire the signal, the LNA and the PGA gain changes take place, as shown in the figure. Note that during the LNA gain updates, the output of the ΣΔ DAC is scaled accordingly to minimize the settling time of the OCL and to allow the AGC to predict the correct signal level while operating simultaneously with the OCL.

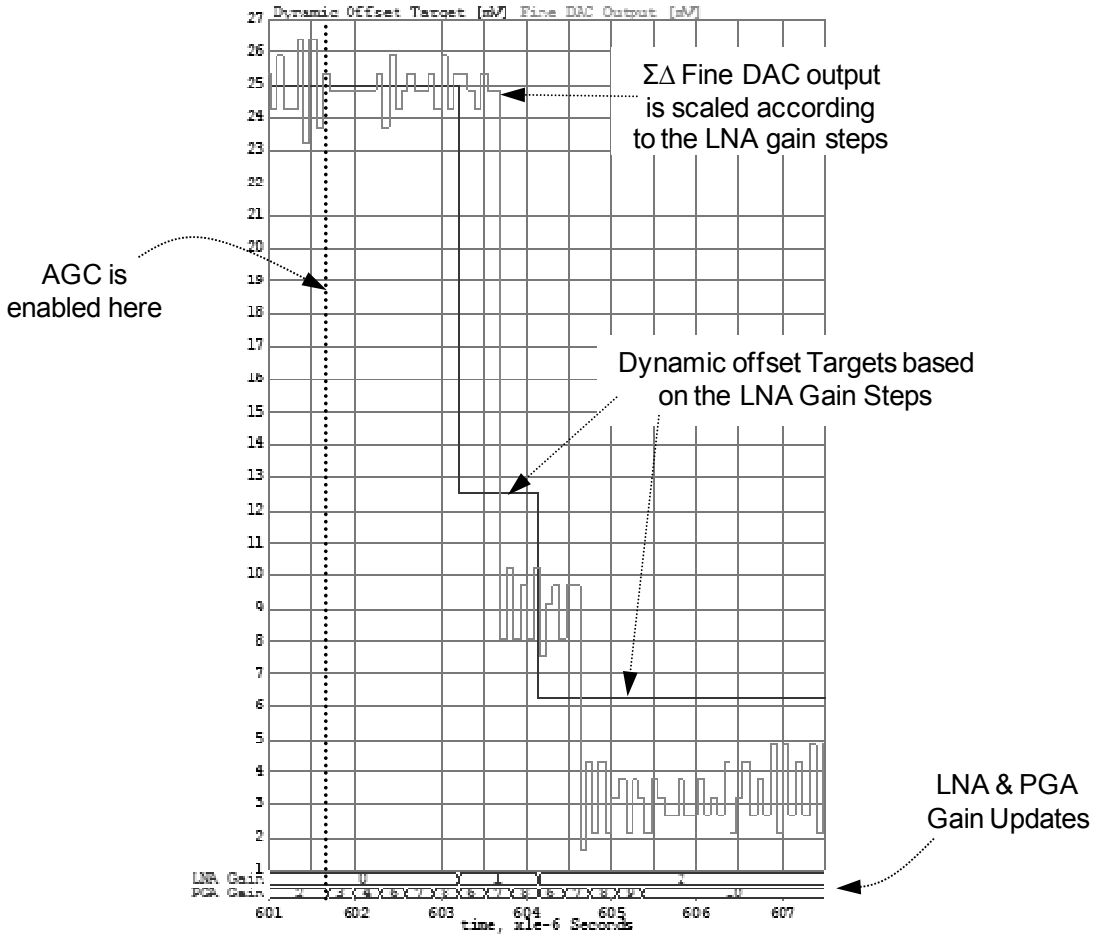


Figure 7-11 Simulation of the OCL during LNA gain changes after the AGC system is enabled in the dynamic offset cancellation phase.

As shown in Figure 7-11, there is an error between the target value of the dynamic offset and that of the ΣΔ DAC. This error is due to the non-ideal scaling of the offset with the LNA gain step. To allow the OCL to settle this error as quickly as possible, the OCL bandwidth is increased whenever there is a change in the LNA gain. In addition, the OCL bandwidth is

kept at the extended bandwidth for a time-out period after every LNA gain change. This guarantees that the error resulting from the scaling mechanism relative to the target offset is cancelled within the given time-out period. After this time-out period, the OCL bandwidth is reduced back to the bandwidth required for signal reception.

Figure 7-12 shows the wide bandwidth phase of the OCL during and after two LNA gain changes. As shown, the OCL is kept in its wide bandwidth state for a time-out period. This time-out period is determined from simulations such that the residual offset is sufficiently low after this phase that the AGC system is not triggered once more. After this time-out period, the OCL enters the lowest bandwidth state for correct signal reception.

It is worth pointing out that the DC content of the received data has to be specified in such a way that the dynamic offset correction does not cancel any relevant information in the signal itself. The DC content of the signal is measured by the run-length of the data being transmitted. For example, a run-length of 3 means that no more than three consecutive bits are identical. From simulations, the run-length for various modulation schemes is determined.

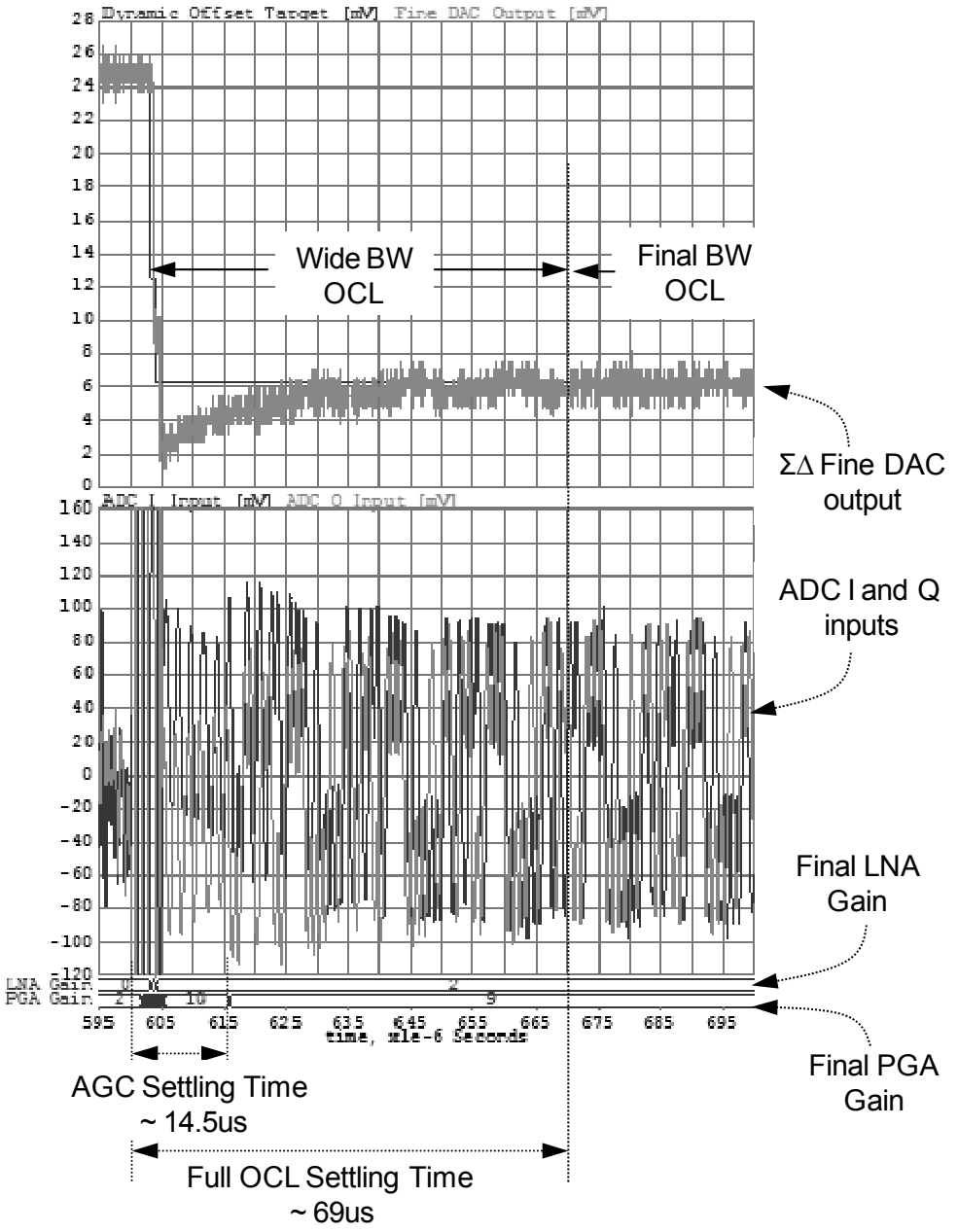


Figure 7-12 Simulation of the OCL showing the wide bandwidth phase during and after LNA gain changes in the dynamic offset cancellation phase.

Figure 7-13 shows a simulation of the OCL without using the scaling mechanism of dynamic offsets when the LNA gain changes. The OCL uses the bandwidth extension scheme after an LNA gain change. It can be seen that without the proposed scheme, the OCL system's settling time increases by a factor of 2.8 and more importantly, that the AGC system's settling time increased by more than a factor of 13 as a result. This is because the AGC system was

misguided by the fact that the dynamic offset in the receiver was not fully cancelled while the AGC was making a decision on the receiver gain level.

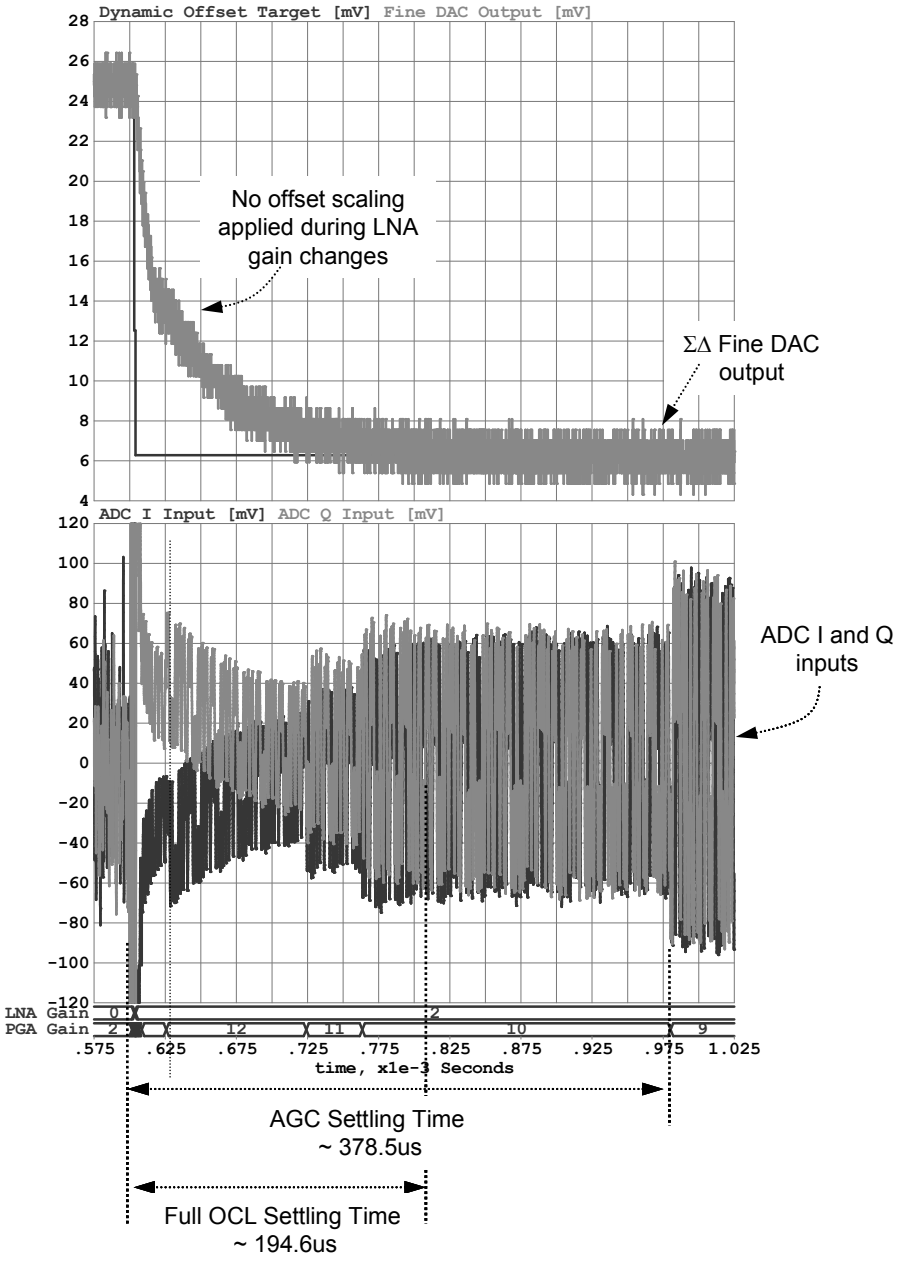


Figure 7-13 Simulation showing the OCL and AGC system performance without applying the offset estimation ΔA_{dc} during LNA gain changes

7.3 Measurement Results

Figure 7-14 to Figure 7-17 show measurement results for the OCL and AGC systems. Figure 7-14 shows the measurement results for the static DC offset cancellation phase for the I and Q channels of the receiver at the PGA output. The settling time of the OCL in the static DC offset cancellation phase to cancel a DC offset which caused the receiver to saturate is about 11µs. It should be noted that the I and Q channels settle to their common-mode voltage at 0.9V in Figure 7-14.

Figure 7-15 shows the measurement result for the effect of the dynamic OCL using the ΣΔ DAC on the receiver's noise. As shown in the figure, the thermal noise of the receiver is unchanged at the PGA output in the case when the dynamic offset cancellation loop is enabled. It is also shown that the flicker noise at the PGA output is removed when the dynamic offset cancellation loop is enabled due to OCL system's high-pass filtering characteristics. This filtering is very desirable for direct-conversion receivers. It should be noted that Figure 7-15 shows that the OCL bandwidth is around 2kHz as expected from the design.

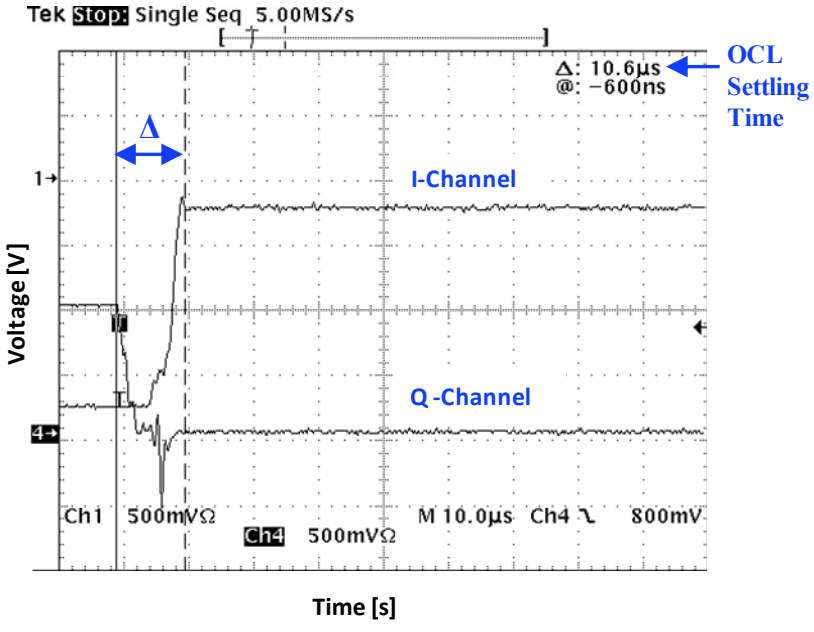


Figure 7-14 Measurement result of the static DC offset cancellation phase at the PGA output

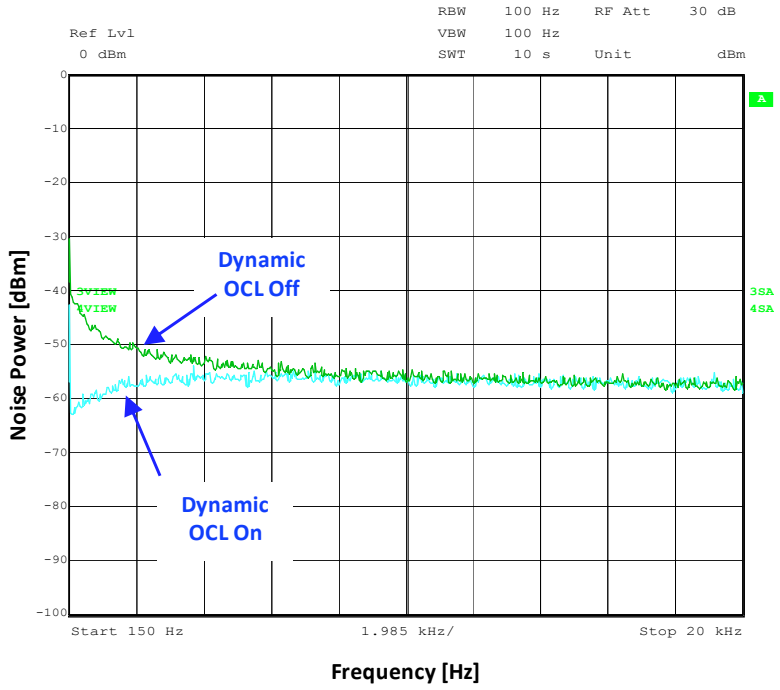


Figure 7-15 Measurement result of the receiver's noise performance during the dynamic offset cancellation phase using the ΣΔ DAC at the PGA output

Figure 7-16 shows the measurement result of the dynamic offset cancellation phase of the OCL when a -53dBm signal is applied to the receiver's input after static and dynamic offset cancellations are completed. This signal level causes the LNA gain to change by 12dB. The figure shows the settling behavior of the OCL and the AGC systems during the LNA gain change. The OCL applies the scaling and the bandwidth extension mechanisms during the LNA gain change and quickly recovers after the LNA gain change occurs. In this measurement, there is an error between the actual and the estimated offset level when the LNA gain changes. This can be observed in the voltage step appearing when the LNA gain change takes place. Despite this, the OCL corrected the offset; the overall settling time for the OCL and the AGC system for that input signal power level is 50µs.

Figure 7-14 shows the measured received signal strength indicator (RSSI) error in dB between the measured and the actual RF signal power at the receiver's input. It can be seen from the figure that the maximum error is ±3dB. This indicates that the OCL correctly cancels

the static and dynamic offsets and allows the AGC to produce the correct gain line-up for the receiver, especially when there are LNA gain changes, which is the most dynamic event for the OCL.

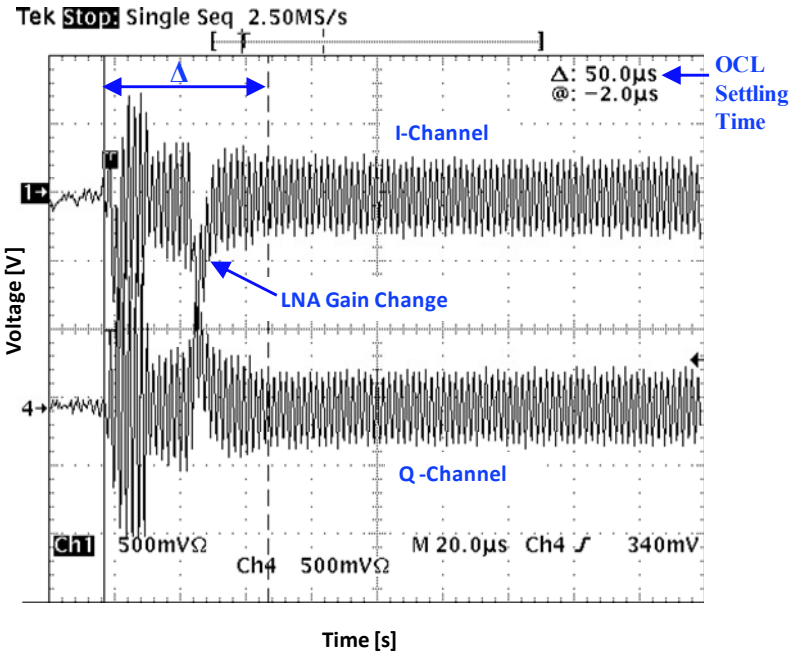


Figure 7-16 Measurement result for the settling performance of the dynamic OCL during an LNA gain at the PGA output

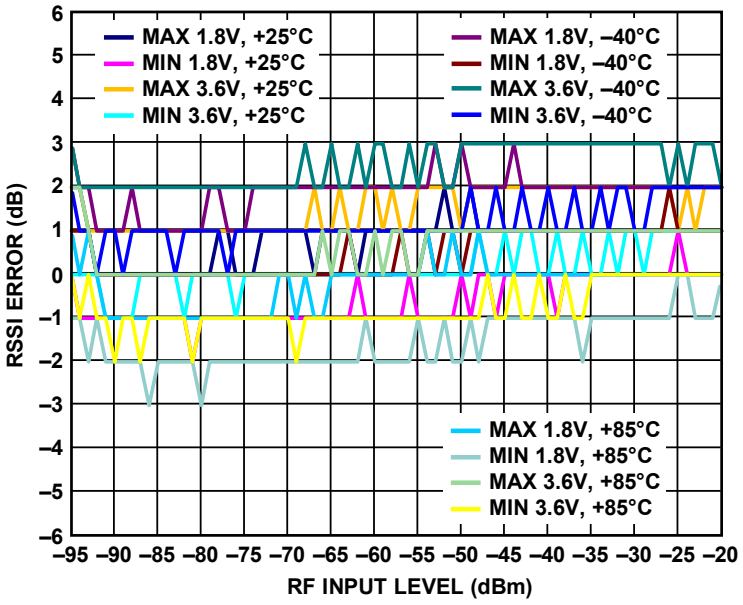


Figure 7-17 Measurement result for the RSSI error of the received signal after an OCL and AGC acquisition

7.4 Conclusions

This chapter illustrated a novel offset cancellation loop using digitally-assisted analog techniques which overcomes a significant number of challenges associated with the use of direct conversion receivers. The main aspects of this novel implementation are:

1. The offset cancellation loop (OCL) reduces the area and power consumption compared to previous analog and mixed-signal offset cancellation system, primarily due to its digital implementation and its use of a dual-phase approach which reduces the area of the offset correction DACs
2. The OCL cancels both static and dynamic offsets in a wireless receiver in two separate phases to reduce the area and power consumption of the system by using two DACs -a static DC offset cancellation DAC and a dynamic ΣΔ DAC- without the need for an explicit low-pass filter; this significantly reduces the area compared to previous mixed-signal offset cancellation loops discussed at the beginning of this chapter.
3. The OCL can continuously track and cancel dynamic time-varying offsets due to LO radiation and self-mixing, as well as process, voltage and temperature drifts using a ΣΔ DAC which can cancel these offsets without degrading the receiver's noise and linearity, while simultaneously saving significant silicon area.
4. A method of dynamically controlling the bandwidth of the OCL according to the offset levels in the receiver significantly reduces the acquisition time of the OCL system. This is done using a simple bit-shifting operation in the feedback path of the OCL. The OCL bandwidth can be controlled from around 125kHz down to 1504kHz. This bandwidth adjustment mechanism is designed to be seamlessly independent of the feed-forward PGA gain changes.
5. A method for fast cancellation of dynamic offsets occurring due to LO radiation and self-mixing through the receiver LNA. The method uses a scaling mechanism which scales the current output of the ΣΔ DAC according to the LNA gain, allowing the

OCL to move close to the correct offset target. This significantly reduces the OCL settling time. The bandwidth of the OCL is also momentarily widened to allow for faster settling in the presence of any incorrect prediction of the exact scaling factor by which the offset is scaled with the LNA gain.

Chapter 8

Conclusions

Wireless communication networks revolutionized the way humans interact with each other and with the world around them. Those networks are poised to play an even greater role in solving some of our key future challenges form preserving our energy resources to reducing the costs of our ever increasing healthcare needs. The internet of everything is our profession's next frontier. At the heart of this challenge is the need for ubiquitous wireless communications utilizing RF transceivers which consume the lowest possible energy. Towards this end, the thesis focused on the architecture, design and evaluation of an RF transmitter and receiver front-end which are part of a commercial RF system on a chip. One of the key contributions of this work is the development of a number of digitally-assisted analog and RF techniques to enable a fully integrated, low energy, low cost and high performance RF transmitter and receiver. In addition, a digitally assisted design simplifies the migration of the design from one process technology node to another with a smaller feature size.

The following are the key contributions of this work to the field of low energy RF receivers and transmitters:

1. The architecture and design of a wide-bandwidth low power RF transmitter using a digitally-assisted pre-emphasis technique to extend the analog bandwidth of the frequency synthesizer by at least a factor of four. This enables RF modulation of FSK signals up to 2Mbps while reusing the frequency synthesizer circuitry and avoiding the area and power consumption which comes with traditional RF transmitters. The transmitter uses a calibration system to maintain the accuracy of the digital modulation at its output in the presence of process, temperature and supply variations. The calibration system is based on a mathematical property of second-order control systems. This property was applied to frequency synthesizers whose closed-loop

transfer function is at least a third order system. The use of a number of digitally assisted calibration techniques simplifies the hardware requirements for the calibration as well as its energy consumption. Overall, this work presented a versatile RF transmitter capable of transmitting IEEE802.15.4 signals with a minimum of 31dB MER, 2Mbps GFSK signals with a maximum of 9.5˚ phase error and meeting the Bluetooth v1.2 specifications; all in the presence of up to ±40% variation in the transmitter's on-chip components across the desired frequency range. The RF transmitter has 60% smaller die area, 50% less power consumption and its calibration system consumes 90% less energy when compared to the closest prior art. From a 1.8V supply, the RF transmitter consumes a total of 18.2mA and occupies a total area of 1.1mm^2.

2. The design of a low power zero-IF receiver for wireless sensor networks by overcoming the challenges posed by the need for a high performance RF front-end and a fast cancellation loop for static and time-varying offsets. These are the key obstacles in the adoption of zero-IF receivers for wireless sensor networks. This work shows novel techniques which address both challenges:

    a. A digitally-assisted offset cancellation loop which enables the higher RF blocking performance of the zero-IF receiver architecture over the widely used low-IF architecture. This is achieved while minimizing the energy consumed by the zero-IF receiver. The offset cancellation loop (OCL) reduces the area and power consumption compared to previous analog and mixed-signal offset cancellation systems, primarily due to its digital implementation and its use of a dual-phase approach which reduces the area of the offset correction DACs. In addition, the use of a ΣΔ DAC without the need for an explicit low-pass filter also significantly reduces the OCL area compared to the prior art. The OCL continuously tracks and cancels dynamic

time-varying offsets due to LO radiation and self-mixing, as well as process, voltage and temperature drifts using the novel ΣΔ DAC which cancels these offsets without degrading the receiver's noise and linearity.

b. The design of a low power and high performance RF front-end. Typically, the RF mixer sets the dynamic range of the receiver. Hence, challenging noise figure and linearity requirements are placed on the mixer with an equally challenging low power consumption budget. The LO circuitry of the RF mixer consumes the most power since the LO needs to drive a large load presented by the RF mixer's transistors. Research typically focuses on improving the RF mixer performance without considering the LO driver's power consumption. This is not the case with low power transceivers used in wireless sensor networks. The thesis presented a novel LO driver circuit which substantially reduces its power consumption and makes the choice of a zero-IF receiver even more attractive than its counterparts.

c. The receiver front-end achieves a thermal noise figure of 9.5dB with a flicker noise corner frequency of approximately 25kHz. It achieves an in-band IIP3 of −13.6dBm and a 1-dB compression point of −20.5dBm at maximum gain. The IEEE 802.15.4 packet-error rate (PER) sensitivity is -95dBm and the 2Mbps GFSK PER sensitivity is -85dBm. In addition, the RF receiver exceeds the ETSI EN 300 440-1 class 2 CW blocking specifications and comes within 1dB of achieving the ETSI EN 300 440-1 class 1 CW blocking specifications. From a 1.8V supply, the RF receiver consumes 17mA. Reducing the LO phase noise at the expense of an increase in this power consumption would be one avenue to pursue to improve the blocking performance by at least 1dB to meet the ETSI EN 300 440-1 class 1 CW blocking specification. Furthermore, the ZIFR architecture of this work

demonstrated an adjacent channel rejection which is about 20dB better than the best LIFR architecture of the prior art.

Bibliography

[1] Retz, G., Shanan, H. et al., "*A highly integrated low-power 2.4GHz transceiver using a direct-conversion diversity receiver in 0.18µm CMOS for IEEE802.15.4 WPAN,"* Digest of Technical Papers, IEEE International Solid-State Circuits Conference. pp. 414-416, Feb. 2009.

[2] Retz, G., Shanan, H. et al., "*Radio transceivers for wireless personal area networks using IEEE802.15.4,"* IEEE Communications Magazine, Vol. 47, Issue 9, pp. 150-158, Sept. 2009

[3] Razavi, B., *"RF Microelectronics,"* Prentice Hall Publishing, 1998

[4] Pamarti, S., Jansson, L. and Galton, I., "*A Wideband 2.4-GHz Delta-Sigma Fractional-N PLL With 1-Mb/s In-Loop Modulation,"* IEEE Journal of Solid-State Circuits, Vol. 39, Issue 1, pp. 49-62, Jan. 2004.

[5] Meninger, S. and Perrott, M., " *A 1-MHz Bandwidth 3.6-GHz 0.18µm CMOS Fractional-N Synthesizer Utilizing a Hybrid PFD/DAC Structure for Reduced Broadband Phase Noise,"* IEEE Journal of Solid State Circuits, Vol. 41, Issue 4, pp. 966-980, April 2006.

[6] Ferriss, M. A., et al., " *A 14mW Fractional-N PLL modulator with a digital phase detector and frequency switching scheme,".* IEEE Journal of Solid-State Circuits, Vol. 43, Issue 11, pp. 2464-2470, Nov. 2008.

[7] Filiol, N. et al. , "*A 22mW Bluetooth RF Transceiver with Direct RF modulation and on-chip IF filtering,"* Digest of Technical Papers, IEEE International Solid-State Circuits Conference. pp. 202-203, Feb. 2001.

[8] Staszewski, RB. et al., "*All-Digital PLL and Transmitter for Mobile Phones,"* IEEE Journal of Solid-State Circuits, Vol. 40, Issue 12, pp. 2469-2482, Dec. 2005.

[9] Perrott, M. H., "*A 27-mW CMOS Fractional- Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation,"* IEEE Journal of Solid-State Circuits, Vol. 12, pp. 2048-2060, 1997.

[10] Craninckx, J. and Steyaert, M., "*A Fully Integrated CMOS DCS-1800 Frequency Synthesizer,"* IEEE Journal of Solid-State Circuits, Vol. 33, Issue 12, Dec. 1998.

[11] Lo, C. and Luong, H., "*A 1.5-V 900MHz monolithic CMOS fast-switching frequency synthesizer for wireless applications,"* IEEE Journal of Solid State Circuits, Vol. 37, Issue 4, pp. 459-470, April 2002.

[12] Crawford, James A., "*Frequency Synthesizer Design Handbook,"* Artech House Microwave Library, 1994.

[13] Shanan, H. et al., "*A 2.4GHz 2Mb/s versatile PLL-based transmitter using digital pre-emphasis and auto calibration in 0.18µm CMOS for WPAN,"* Digest of Technical Papers, IEEE International Solid-State Circuits Conference, pp. 420-421, Feb. 2009.

[14] Arora, H. et al., "*Enhanced Phase Noise Modeling of Fractional-N Frequency Synthesizers,"* IEEE Transactions on Circuits and Systems-I: Regular Papers, Vol. 52, Issue 2, Feb. 2005.

[15] McMahill, D.R. and Sodini, C.G., "*Automatic calibration of modulated frequency synthesziers,"* IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vols. 49, Issue 5, May 2002.

[16] Fontaine, P.H., Bellaouar, A. and Bakkaloglu, B., "*Efficient modulation compensation of sigma delta fractional phase locked loo,"* US Patent 6,806,780, Mar 2003.

[17] O'Sullivan, C., Lyden, C. and Shanan, H., "*Phase lock loop RF modulator system,"* US Patent 7,420,433, Sept. 2008.

[18] Akamine, Y. et al., "*ΔΣ PLL Transmitter With a Loop-Bandwidth Calibration System,"* IEEE Journal of Solid-State Circuits, Vol. 43, Issue 2, pp. 497-506, Feb. 2008.

[19] Balboni, E., "*Method of modulation gain calibration and system thereof,"* US Patent 6,670,861, Dec. 2003

[20] Ogata, K., "*Modern Control Engineerin,"* Prentice Hall Publishing, 1991

[21] Kreyszig, E., *"Advanced Engineering Mathematics,"* 7th Edition, John Wiley & Sons Inc., 1993.

[22] Razavi, B., "*Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design,"* Wiley-IEEE Press, 1996.

[23] Shanan, H., "*Calibration system and method for phase-locked loops,"* U.S. Patent No. 8,049,540, Nov. 2011.

[24] Shanan, H., "*Calibration for phase-locked loop,"* U.S. Patent No. 8,188,778, May 2012

[25] *Direct Conversion Receivers in Wide-Band Systems.* Parssinen, A., Kluwer Academic Publishers, 2001.

[26] Friis, H.T., "*Noise figure of radio receivers,"* Proc. IRE, Vol. 32, July 1944.

[27] *Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs)*, IEEE Computer Society, 2006.

[28] *ETSI EN 300 440: Short-range devices; Radio equipment to be used in the 1 GHz to 40 GHz frequency range.* European Telecommunications Standards Institute, 2000.

[29] *ETSI EN 300 328: Data transmission equipment operating in the 2.4 GHz ISM band and using wide band modulation techniques.* European Telecommunications Standards Institute, 2006.

[30] Retz, G., "*Analog Devices Internal Memo"*

[31] Gutierrez, J. et al., "*Low-Rate Wireless Personal Area Networks : Enabling Wireless Sensors with IEEE 802.15.4,"* IEEE Press, 2004.

[32] Razavi, B., "*Design Considerations for Direct-Conversion,"* IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 44, Issue 6, Jun 1997.

[33] Camus, M. et al., "*A 5.4mW 0.07mm2 2.4GHz Front-End Receiver in 90nm CMOS for IEEE802.15.4 WPAN,"* Digest of Technical Papers, IEEE International Solid-State Circuits Conference, pp. 368-620, Feb. 2008.

[34] Niknejad, A., "*Mixer Noise and Design Course Notes,"* University of California at Berkeley, 2009.

[35] Kluge, W. et al., "*A Fully Integrated 2.4GHz IEEE802.15.4 Compliant Transceiver for Zigbee Applications,"* Digest of Technical Papers, IEEE International Solid-State Circuits Conference, pp. 1470-1479, Feb. 2006.

[36] Vedral, A.R. et al., "*Development and performance evaluation of an antenna diversity module for industrial communication based on IEEE 802.15.4,"* IEEE Conference on Emerging Technologies and Factory Automation, pp. 177 – 186, Sept. 2007.

[37] Redman-White, W. et al., "*1/f noise in passive CMOS mixers for low and zero IF integrated receivers,"* Proceedings of the 27th IEEE European Solid-State Circuits Conference. pp. 41 - 44, Sept. 2001.

[38] Smith, David R., "*Digital Transmission Systems,"* Springer Publishing, 1993.

[39] Quinlan, P. et al., "*A multi-mode 0.3-128kb/s transceiver for the 433/868/915MHz ISM bands in 0.25µm CMOS,"* IEEE Journal of Solid-State Circuits, Vol. 39, Issue 12, pp. 2297 - 2310, Dec. 2004.

[40] Lee, T., "*The Design of CMOS Radio Frequency Integrated Circuits,"* Cambridge Univeristy Press, 1998.

[41] Sodini, C.G. et al., "*The Effect of High Fields on MOS Device and Circuit Performance,"* IEEE Transactions on Electron Devices, Vol. ED-31, Issue 10, Oct. 1984.

[42] Darabi, H. and Abidi, A., "*Noise in RF-CMOS Mixers: A Simple Physical Model,"* IEEE Journal of Solid-State Circuits, Vol. 35, Issue 1, Jan. 2000

[43] Gray, P. R., et. al., "*Analysis and Design of Analog Integrated Circuits,"* John Wiley & Sons, 2001.

[44] Antoine, P. et al., "*A direct-conversion receiver for DVB-H,"* IEEE Journal of Solid State Circuits, Vol. 40, Issue 12, pp. 2536–2546, Dec. 2005.

[45] Poobuapheun, N. et al., "*A 1.5-V 0.7–2.5-GHz CMOS quadrature demodulator for multiband directconversion receivers,"* IEEE Journal of Solid- State Circuits, Vols. 42, Issue 8, pp. 1669–1677, Aug 2007.

[46] Brown, W.T. et al., "*Prediction and Characterization of Frequency Dependent MOS Switch Linearity and the Design Implications,"* Proceedings of IEEE Custom Integrated Circuits Conference, pp. 237-240, Sept. 2006.

[47] Zhou, S. et al., "*A CMOS Passive Mixer With Low Flicker Noise for Low-Power Direct Conversion Receivers,"* IEEE Journal of Solid State Circuits, Vol. 40, Issue 5, May 2005.

[48] Chehrazi, S. et al., "*Noise in passive FET mixers: a simple physical model,"* Proceedings of the IEEE Custom Integrated Circuits Conference, pp. 375 - 378, Oct. 2004.

[49] Chehrazi, S. et al., "*Noise in Current-Commutating Passive FET Mixers,"* IEEE Transactions on Circuits and Systems-I: Regular Papers, Vol. 57, Issue 2, Feb. 2010.

[50] Chen, WH. et al., "*A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation,"* IEEE Journal of Solid State Circuits, Vol. 43, Issue 5, May 2008.

[51] Razavi, B. et al., "*A 13.4-GHz CMOS Frequency Divider,"* Digest of Technical Papers, IEEE International Solid-State Circuits Conference, pp. 176-177, Feb. 1994

[52] Razavi, B. , "*Design of High-speed, Low-Power Frequency Dividers and Phase-Locked Loops in Deep Submicron CMOS,"* IEEE Jounral of Solid-State Circuits, Vol. 2, pp. 101-109, 1995.

[53] Shanan, H., "*Low-Power Frequency Dividers,"* US Patent Number 8,294,493, Oct. 2012.

[54] Shanan, H., "*Low-Power Frequency Dividers,"* US Patent Number 8,598,923, Dec. 2013.

[55] Vassiliou, I. et al., "*A single-chip digitally calibrated 5.15-5.825GHz 0.18um CMOS transceiver for 802.11.a Wireless LAN,"* IEEE Journal of Solid-State Circuits, Vol. 38, Issue 12, Dec. 2003.

[56] Magoon, R. et al., "*A single-chip quad-band (850/900/1800/1900 MHz) direct conversion GSM/GPRS RF transceiver with integrated VCOs and fractional-N synthesizer,"* IEEE Journal of Solid-State Circuits, Vol. 37, Issue 12, Dec. 2002.

[57] Perraud, L. et al., "*A direct-conversion CMOS transceiver for the 802.11a/b/g WLAN standard utilizing a Cartesian feedback transmitter,"* IEEE Jounral of Solid State Circuits, Vols. 39, Issue 12, Dec 2004.

[58] Shanan, H., "*DC offset correction system and method for communication receivers,"* US Patent Number 8,666,343, Mar. 2014.

[59] Schreier, R. and Temes, G., "*Understanding Delta-Sigma Data Converters,"* IEEE Press, 2005.

[60] Sacchi, E. et al., "*A 15 mW, 70 kHz l/f Corner Direct Conversion CMOS Receiver,"* Proceedings of IEEE Custom Integrated Circuits Conference, pp. 459 - 462, Sept. 2003.

[61] Ingel, M. et al., "*A 5 mm2 40 nm LP CMOS Transceiver for a Software-Defined Radio Platform,"* IEEE Journal of Solid State Circuits, Vol. 45, Issue 12, Dec. 2010.

[62] Valla, M. et al., "*A 72-mW CMOS 802.11a direct conversion front-end with 3.5-dB NF and 200-kHz 1/f noise corner,"* IEEE Journal of Solid State Circuits, Vol. 50, Issue 4, pp. 970–977, Apr 2005.



ARCHITECTURE AND DESIGN OF AN RF RECEIVER FRONT-END AND TRANSMITTER FOR WIRELESS SENSOR NETWORKS, HEALTHCARE AND SMART ENERGY SYSTEMS

Copyright © Hyman Shanan, 2016