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Article

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Engineering the Palladium–WSe_2 Interface Chemistry for Field Effect Transistors with High Performance Hole Contacts

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Abstract

Palladium has been widely employed as a hole contact to WSe_2 and has enabled, at times, the highest WSe_2 transistor performance. However, there are orders of magnitude variation across the literature in Pd–WSe_2 contact resistance and I_{ON}/I_{OFF} ratios with no true understanding of how to consistently achieve high–performance contacts. In this work, WSe_2 transistors with impressive I_{ON}/I_{OFF} ratios of 10^6 and Pd–WSe_2 Schottky diodes with near–zero variability are demonstrated utilizing Ohmic–like Pd contacts through deliberate control of the interface chemistry. The increased concentration of a $PdSe_x$ intermetallic is correlated with an Ohmic band alignment and concomitant defect passivation, which further reduces the contact resistance, variability, and barrier height inhomogeneity. The lowest contact resistance occurs when a 60 minute post metallization anneal at 400 °C in forming gas (FG) is performed. X-ray photoelectron spectroscopy indicates this FG anneal produces 3× the concentration of $PdSe_x$ and an Ohmic band alignment, in contrast to that detected after annealing in ultra–high vacuum, during which a 0.2 eV hole Schottky barrier forms. Raman spectroscopy and scanning transmission electron microscopy highlight the necessity of the fabrication step to achieve high–performance contacts as no $PdSe_x$ forms and WSe_2 is unperturbed by room temperature Pd deposition. However, at least one WSe_2 layer is consumed by the necessary interface reactions that form $PdSe_x$ requiring strategic exploitation of a sacrificial WSe_2 layer during device fabrication. The interface chemistry and structural properties are correlated with Pd–WSe_2 diode and transistor performance and the recommended processing steps are provided to enable reliable high–performance contact formation.

Introduction

In 3D semiconductor based devices, the continuous engineering of commercially viable contacts utilizes a detailed understanding of relationships between processing conditions (*e.g.* deposition chamber ambient, post metallization annealing ambient), interface chemistry, and contact performance.[1] Transition metal silicides[2] in the case of Si, or salicides in the case of compound 3D semiconductors (*e.g.* InGaAs),[3,4] have long been the industry standard contacts in conventional CMOS technology. These materials exhibit phase and stoichiometry dependent electronic properties, which are tunable with carefully designed processing conditions. Analogous chalcogen–based intermetallic species may be available for engineering superior contacts in TMD–based devices. However, processing condition–contact performance relationships in TMDs remain largely unexplored to date. State–of–the–art contact resistance to TMDs (R_c = 0.2 kΩ-μm) remains a few times greater than target values established in the most recent International Technology Roadmap for Semiconductors (ITRS).[5] A large parasitic contact resistance is also problematic because it can convolute the intrinsic properties (*e.g.* mobility) of a TMD device.[6,7] A variety of new strategies have been employed[8–13] to lower TMD contact resistance, but direct deposition of bulk metals in top contact architectures are the easiest to implement in a full field effect transistor (FET) process flow and are preferred for future technologies.

Pd contacts are widely employed in WSe_2 FETs as they have been used to demonstrate the best FET properties with Ohmic–like p-type behavior and I_{ON}/I_{OFF} ratios $>10^8$, which is orders of magnitude better performance than analogous devices with other metals.[5,13–18] However, reported

R_c (ranging from 10^{-1}–10^5 kΩ-μm) and transistor I_{ON}/I_{OFF} ratios (10^4–10^9) vary widely across WSe_2 devices with Pd contacts reported in the literature.[5,15,16,19–22] Pd is expected to be a good p-type contact to WSe_2 because of its (vacuum) work function and relative alignment to the WSe_2 valence band edge. However, choosing a contact metal based solely upon a low predicted Schottky barrier according to the Schottky–Mott rule[23] often results in unexpected contact performance.[13,24,25] In reality, defects within the TMD,[26–28] thermodynamically favorable reactions, and metal oxidation during deposition have been shown to result in variable contact performance.[29,30,31] In addition, metal–TMD reactions, often enhanced at elevated temperatures, disrupt the layered TMD structure in the contact regions of a mono or few layer TMD–based device. The number of layers consumed by interface reactions, and therefore resulting changes in the density of states within the underlying TMD, should be considered when interpreting variations in contact performance.[32] This necessitates a more comprehensive understanding of the interface chemistry–contact performance relationship in metal–TMD systems.

In this work, we determine the effects of deposition ambient and post metallization annealing conditions on the interface chemistry and band alignment with *in–situ* photoemission–based experiments using bulk WSe_2. In addition, the number of WSe_2 layers (single and few-layer flakes) consumed by reactions with the contact metal are evaluated with Raman spectroscopy, scanning transmission electron microscopy (STEM), and energy dispersive X–ray spectroscopy (EDS). Finally, we evaluate the electrical performance of optimized high work function Pd contacts to WSe_2 using Schottky diode (bulk WSe_2) and field effect transistor (FET, 7-10 layer WSe_2) structures. Recommendations based on these findings are provided to enable consistent, high performance Pd–WSe_2 contacts, which are confirmed through our outstanding FET performance metrics.

Results and Discussion

Effects of Processing Conditions on Pd–WSe_2 Interface Chemistry and Structure

i) van der Waals Interface at Room Temperature

The impingement rate of residual gas molecules under high vacuum (HV) conditions ($<2 \times 10^{-6}$ mbar) is orders of magnitude greater than that found under ultra–high vacuum (UHV) conditions ($<2 \times 10^{-9}$ mbar) according to the kinetic theory of gases. Such rates are further enhanced by species liberated through desorption of heated surfaces, which may be employed in a metal contact deposition process. A HV deposition ambient is often utilized for device contact fabrication. Significant interface chemistry differences with the deposition ambient have been demonstrated previously for other metal–TMD systems.[29–31] The chemistry at the interface formed between Pd and bulk WSe_2 is reflected in Figure S1 as a function of ambient pressure in the deposition chamber (see Methods for details). Reaction products for deposition at room temperature (RT) are not detected at the Pd–WSe_2 interface regardless of deposition conditions. Reactions between Pd and WSe_2 are not thermodynamically favorable at RT as the Gibbs Free Energy of Formation $\Delta G°_{f,Pd4Se}$ at 25 °C (-60.67 kJ/mol, which is similar to that of Pd_2Se and PdSe)[33] is slightly more positive than that of WSe_2 ($\Delta G°_{f,WSe2}$ = -67.44 kJ/mol).[34,35]

In contrast, when Pd is deposited under HV conditions, an additional chemical state is detected at higher BE from metallic Pd (Figure S1b,c). This corresponds with the formation of PdO, which likely occurs during air exposure before X–ray photoelectron spectroscopy (XPS) analysis (PdO formation is exothermic, $\Delta G°_{f,PdO}$ =-136 kJ/mol).[36]

Pd does not react with any adventitious species residing on the WSe_2 surface at RT regardless of reactor base pressure (Figure S1d). Adventitious carbon is detected on all exfoliated WSe_2

samples throughout this work at a BE of ~284.6 eV. In all cases, adventitious carbon is detected after Pd deposition, presumably at the Pd–WSe_2 interface. The adventitious carbon chemical state shifts 0.4 eV to lower BE upon Pd deposition, which is consistent with the corresponding BE shifts exhibited by the bulk WSe_2 chemical states and can therefore be attributed to upward band bending induced by the Pd (see Supporting Information for further discussion). Therefore, the C 1*s* core level will not be discussed for the remainder of the text.

ii) Thermally Induced Intermetallic Formation under Vacuum Conditions

Although performing a single deposition step under UHV and HV conditions offers a useful differentiation in interface chemistry with vacuum conditions, Pd grows as islands on WSe_2 and therefore may result in a band alignment inconsistent with that of a thick, continuous Pd contact to WSe_2 typically employed for a device. In addition, post metallization annealing often drives interface reactions and concomitant E_F shifts. Therefore, the interface chemistry and band alignment between Pd and WSe_2 was tracked by *in–situ* XPS throughout stepwise Pd deposition and post metallization annealing under UHV conditions (1 hr at each temperature, see Methods for more details). The general process flow employed in fabricating and annealing Pd-WSe_2 samples for XPS analysis throughout Pd deposition and subsequent anneals in UHV or FG is depicted in Figure 1a.

Figure 1b displays the evolution of integrated intensities (including both spin–orbit split peaks and corrected by atomic sensitivity factors, see Supporting Information) of chemical states related to the Pd–WSe_2 interaction in the Se 3*d*, W 4*f*, and Pd 3*d* core level spectra throughout stepwise Pd deposition and post metallization annealing under UHV conditions. In addition, the Pd 3*d* core level spectra obtained throughout the experiment is shown in Figure 1c. Bulk WSe_2

chemical states are the only detectable species in the Se 3*d* and W 4*f* core level spectra throughout Pd deposition at RT. The absence of detectable reaction products at RT (*e.g.* Pd–Se bond formation) agrees with thermodynamic predictions but contrasts with the (ideal) covalent Pd–WSe_2 interface in a top contact configuration predicted by Kang *et al* using augmented density functional theory methods that employ defect–free interfaces where Pd–Se bonding is prominent even at 0 K.[37] It is noted that the Pd $3d_{5/2}$ core level spectrum detected following Pd deposition on WSe_2 in UHV exhibits a larger full width at half maximum (FWHM) than that of the metal Pd $3d_{5/2}$ reference spectrum (Figure S1b). However, the BE of the Pd $3d_{5/2}$ core level obtained following deposition under UHV and HV conditions (Pd^0: 334.96 eV) agrees well with that of the Pd reference film obtained in this work (334.93 eV). The shape of the Pd $3d_{5/2}$ peak is discussed in greater detail in the Supporting Information.

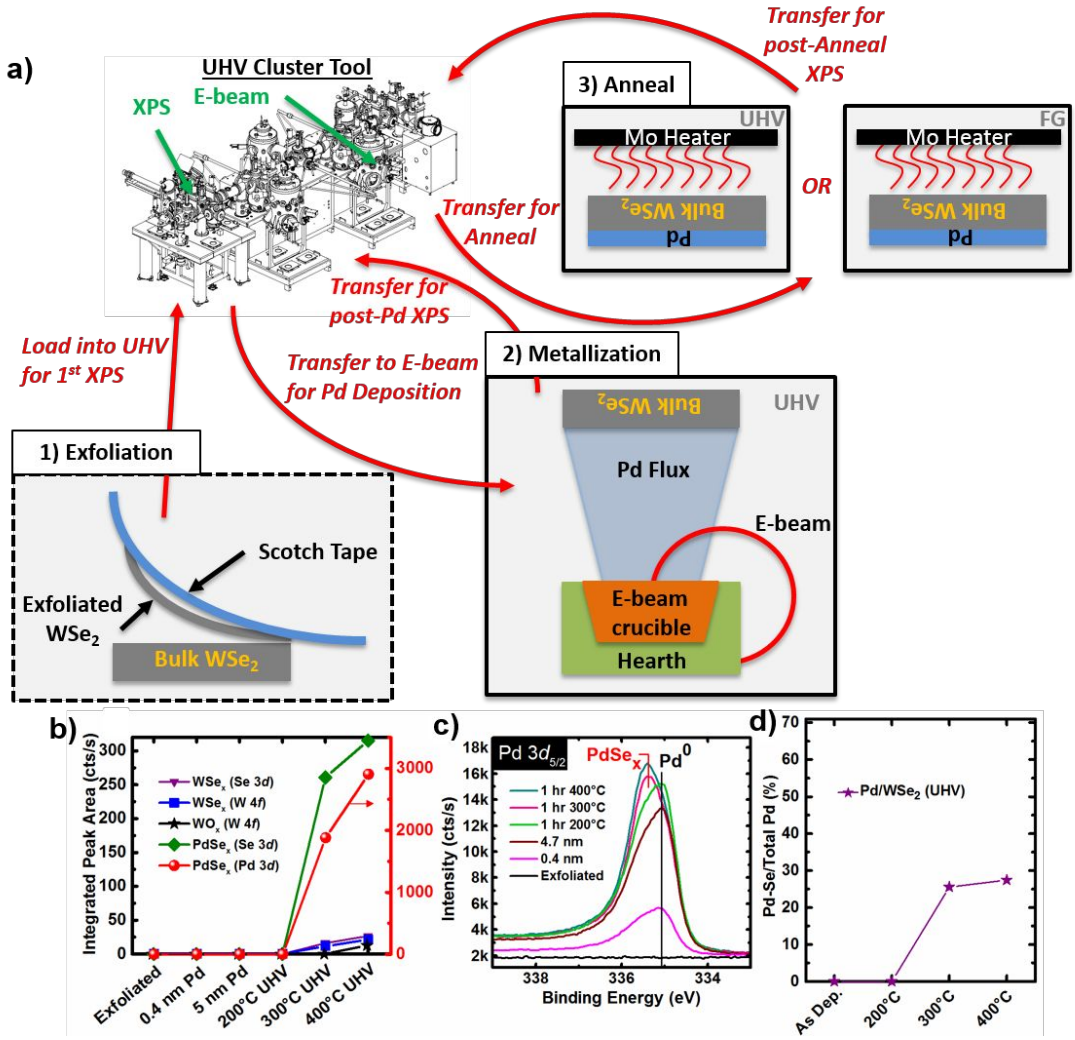


Figure 1: a) Schematic illustrating the process flow employed in fabricating Pd-WSe_2 samples for XPS analysis *in–situ* throughout 1) exfoliation, 2) Pd deposition in UHV and 3) subsequent anneals in UHV or FG. After (69). © 2008 The Electrochemical Society. b) Integrated intensities of chemical states in the Se 3*d*, W 4*f*, and Pd 3*d* core level spectra associated with various reaction products as well as the c) Pd 3*d* core level spectra obtained throughout Pd deposition on WSe_2 and post metallization annealing under UHV. It is explicitly noted that the integrated peak areas shown in b) represent only the areas of the respective chemical state fitted to each denoted core level spectrum. The red line (spheres) in b) is plotted vs the right y–axis while all other data points are plotted vs the left y–axis. d) Interfacial reactivity gauged by the ratio of the intensity of the chemical state in the Pd 3*d* core level corresponding with $PdSe_x$ to the total intensity of the respective core level after depositing at RT and subsequent *in–situ* annealing in UHV showing the onset of $PdSe_x$ formation at 300 °C and 28% Pd to $PdSe_x$ conversion at 400 °C.

No additional chemical states are detected in any core levels following the 200 °C anneal consistent with the formation of reaction products. In contrast, annealing at 300 °C under UHV

conditions causes Pd to reduce the underlying WSe_2 resulting in the formation of $PdSe_x$ and WSe_x as seen in the Se 3*d*, W 4*f* (Figure S3), and Pd 3*d* core level spectra. This is similar to the reducing behavior observed for Pd deposited on Bi_2Se_3, another Se–based layered material.[38] $PdSe_x$ and WSe_x chemical states detected in the Se 3*d* and W 4*f* core level spectra intensify following the 400 °C anneal (Figures 1b, S3). In addition, chemical states associated with WSe_x exhibit BE shifts consistent with a decreased oxidation state, suggesting that WSe_x reduction is enhanced at higher annealing temperatures. (A small concentration of WO_x forms during the 400 °C anneal, the origins of which are discussed in the Supporting Information.) It is important to note that any reactions between metal and WSe_2 could manifest due to WSe_2 instability at the annealing temperatures employed in this work. However, such thermal instability is ruled out based upon our study of the chemical stability of bare WSe_2 up to 450 °C under UHV and FG conditions (see Supporting Information).

The BE of the chemical state consistently detected in the Pd $3d_{5/2}$ core level (334.91 eV) agrees well with the Pd reference (334.94 eV) indicating the deposited film is composed solely of metallic Pd throughout RT deposition and after annealing at 200 °C in UHV. A chemical state in addition to metallic Pd is detected in the Pd 3*d* core level after 300 °C anneal at a BE of 335.49 eV corresponding with the formation of $PdSe_x$.[39] The $PdSe_x$ chemical state binding energies in the Pd 3*d* and Se 3*d* core levels do not appreciably change following the 400 °C anneal but do increase in intensity. In addition, the intensity ratio between the $PdSe_x$ and the metallic Pd chemical states in the Pd 3*d* core level increases from 0.34 to 0.40 (Figure 1d) upon annealing at 400 °C corroborating an increasing $PdSe_x$ concentration with increased annealing temperature. The BE of the $PdSe_x$ chemical state in the Pd 3*d* core level spectra obtained after annealing at 300 °C and 400 °C is 0.22 eV lower than that of the PdO chemical state detected following Pd deposition under

HV conditions, which rules out the formation of PdO at elevated temperatures in UHV (Figure S4).

$PdSe_x$ formation at 300 °C in UHV is reasonable considering the $\Delta G°_{f,WSe2}$ and $\Delta G°_{f,Pd4Se}$ variation with temperature. $\Delta G°_{f,Pd4Se}$ ($\Delta G°_{f,WSe2}$) becomes increasingly negative (positive) as temperature increases. At 300 °C, $\Delta G°_{f,Pd4Se}$ and $\Delta G°_{f,WSe2}$ (-62.34 kJ/mol[33] and -63.62 kJ/mol,[34] respectively) are within the ±3.2 kJ/mol uncertainty of each other associated with the uncertainty in the temperature set point of the heater employed for annealing (±25 °C). In addition, reactions are more favorable at surface and edge defects commonly found in TMDs.[26,27] Furthermore, there are a number of stable phases in the palladium selenide binary system across a wide range of compositions stable down to room temperature.[39] It is known, however, that stable alloys of Pd–W are not expected to form at the temperatures examined here (T<500 °C).[40] Therefore, Pd–Se formation at or above 300 °C in UHV is thermodynamically favorable either in the top or edge contact configuration. Finally, based on these results, it is noted that the DFT predictions[37] indicating Pd–Se bond formation at temperatures well below room temperature suggest that further refinements of the interaction potentials and methods (such as including the impact of defects) are needed for better agreement with experimental contact metal reaction studies.

iii) Enhanced Reactions and Defect Passivation by FG Anneal

Post metallization annealing is often performed in various gases (*e.g.* H_2, N_2+H_2) and is well–established in conventional device fabrication technologies (*e.g.* Si, Ge, III–V, etc.) for interface passivation. Forming gas (FG, 90% N_2:10% H_2) is more reductive than UHV conditions and can also enable defect passivation by hydrogen, which can penetrate to various interfaces within a TMD–based device.[41] Since Pd is a powerful H_2 catalyst,[42,43] the effects of annealing a

Pd contact in FG is of particular interest as it may facilitate hydrogen transport to the Pd–WSe_2 interface and affect interface chemistry.

Annealing the Pd–bulk WSe_2 structure in FG (1 mbar, 1 hr at each temperature) results in a markedly different interface, both chemically and electrically, compared to UHV. Annealing at 200 °C in FG drives Pd to reduce WSe_2 and form substoichiometric WSe_x ($x \approx 1.1$) as well as $PdSe_x$, which is detected as the chemical state that appears in the corresponding Pd 3*d* core level spectrum (Figure 2a). The concentration of $PdSe_x$ increases with increasing temperature in FG as seen in the increase of intensity ratio between the $PdSe_x$ and WSe_2 chemical states in the corresponding Se 3*d* core level spectra (0.3±0.1 after 200 °C FG anneal to 0.6±0.1 after 400 °C FG anneal, Figure S5). Furthermore, the $PdSe_x$ concentration increases from 17.4% of the total Pd 3*d* intensity after 200 °C FG anneal to 70.4% of the total Pd 3*d* intensity after 400 °C FG anneal (Figure 2b,c). The WSe_x:WSe_2 concentration ratio does not change after the annealing steps.

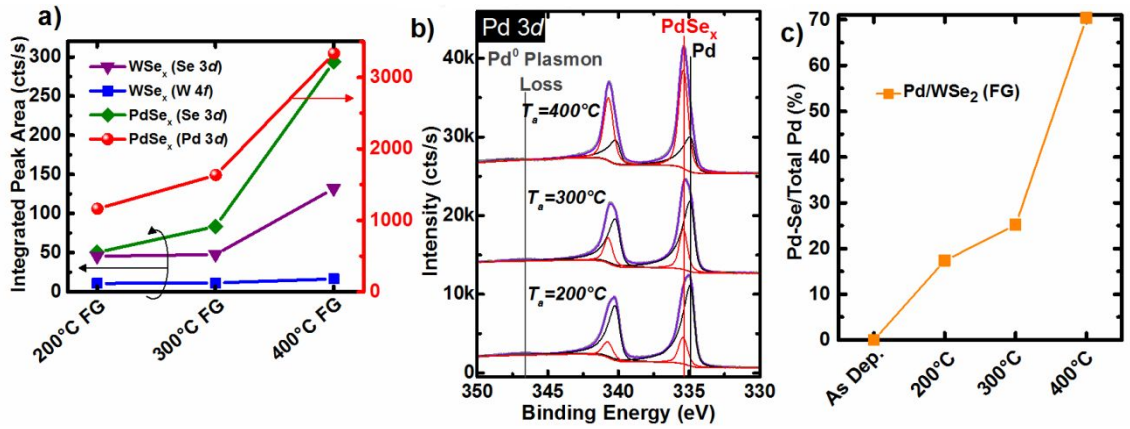


Figure 2: a) Integrated intensities (including both spin orbit split branches in each core level) of chemical states in Se 3*d*, W 4*f*, and Pd 3*d* core level spectra associated with various reaction products as well as the b) Pd 3*d* core level spectra obtained after annealing a ~50 Å Pd–WSe_2 structure under ambient pressure forming gas at 200 °C, 300 °C, and 400 °C, respectively, for 1 hr each. It is explicitly noted that the integrated peak areas shown in a) represent only the areas of the respective chemical state fitted to each denoted core level spectrum. c) Interfacial reactivity gauged by the ratio of the intensity of the chemical state in Pd 3*d* core level corresponding with $PdSe_x$ to the total intensity of the respective core level after depositing at RT and subsequent *in–situ* annealing in FG showing the onset of $PdSe_x$ formation at 200 °C and 70% Pd to $PdSe_x$ conversion at 400 °C.

The concentration of $PdSe_x$ relative to metallic Pd after annealing at 400 °C in FG (70.4%) is far greater than that detected after the 400 °C UHV anneal (27.5%) despite nearly identical final Pd film thicknesses on each sample according to the attenuation of the WSe_2 chemical state in the Se 3*d* core level. Metallic W remains below the limit of detection, suggesting that WSe_x is stable in FG despite enhanced $PdSe_x$ formation at 300 °C and 400 °C. It is already clear that annealing ambient can significantly affect the resulting interface chemistry. When the anneal is performed in FG, Pd readily dissociates H_2[43] and supplies atomic hydrogen (H*) to the interface with WSe_2. The energy associated with breaking the H–H bond (bond dissociation energy, $BDE_{H\text{-}H}$ = 432.1 kJ/mol; see Table S2 for all relevant BDE values)[44] is much greater than that of the W–Se bond (418.1 kJ/mol).[45] Therefore, W–Se and Pd–H bond scission with corresponding Se–H and W–H bond formation is energetically favorable during the FG anneals. H*, which has been reported to act as an amphoteric passivant in chalcogen based systems,[46] passivates the resulting dangling

bonds in WSe_2 thereby stabilizing the structure. Additional energy released by H_2 splitting throughout the anneal breaks Se–H bonds facilitating the exothermic reaction with Pd to form $PdSe_x$ and resulting in an intimate contact with WSe_2.

The significant differences in Pd–WSe_2 interface chemistry observed between samples annealed in UHV or FG translate to differences in band alignment and contact performance, which will be discussed in greater detail later.

iii) Thermally Induced Structural and Chemical Perturbation in Pd–WSe_2

The results discussed thus far were obtained from bulk WSe_2 crystals whereas typical TMD–based devices are comprised of single to few layer films. Therefore, it is of great interest to investigate the number of WSe_2 layers affected by interface reactions as controlling this may offer another route to tunable contact properties.

The effects of metal–TMD interactions on the vibrational and electronic properties of TMDs has previously been investigated with Raman spectroscopy.[47–49] In one report, the partial coverage of single layer MoS_2 with deposited Pd films resulted in a complex convolution of the E^1_{2g} and A_{1g} vibrational modes due to spatially varying strain across the TMD.[48] Here, Raman spectroscopy is similarly employed to investigate the effects of interfacial perturbations on the characteristic vibrational modes of exfoliated single and few layer WSe_2 flakes. However, special care was taken to ensure full coverage of the deposited Pd films. Furthermore, a full coverage Si cap was deposited *in–situ* after Pd deposition and post metallization annealing ruling out any spurious effects on the interface due to air exposure during *ex–situ* experiments (Raman, TEM). Therefore, the spectral variations are presumed to reflect only the effects of metal–WSe_2 reactions.

The number of WSe_2 layers consumed by the interface reactions are also quantified by Raman spectroscopy. The first order vibrational modes of some TMDs exhibit layer number dependent Raman shifts (*e.g.* MoS_2, WS_2).[50,51] However, these modes are degenerate in WSe_2[51,52] and do not exhibit any discernible systematic shift or intensity dependence with layer number. This degeneracy can only be broken if uniaxial strain (*i.e.* along either the arm–chair or zig–zag directions) is applied to single or few–layer WSe_2.[53] Therefore, the second order longitudinal acoustic mode at the M point in the Brillouin zone [2LA(M)] has been employed here to track the number of layers present in WSe_2 flakes. The 2LA(M) mode is detectable with resonant excitation conditions, which occur in WSe_2 when a 532 nm laser is utilized,[53] so a He–Ne laser (λ=532 nm) is employed in this work to access the E^1_{2g}, A_{1g}, and 2LA(M) modes. The 2LA(M) mode exhibits 2.5, 0.5, 0.5, and 0.3 cm^{-1} red shifts from 1L (261.3 cm^{-1}) to 2L, 2L to 3L, 3L to 4L, and 4L to 5L WSe_2 (Figure 3a inset), respectively, permitting accurate layer number identification for mono and few layer flakes.

Laser interrogation can impart significant damage (*e.g.* roughness) upon TMD surfaces.[54] The parameters employed here in obtaining Raman spectra from WSe_2 were carefully chosen according to control experiments to avoid damaging WSe_2 and interpret spectral changes originating from chemical or physical Pd–WSe_2 interactions rather than laser induced intermixing (see Supporting Information for more details).

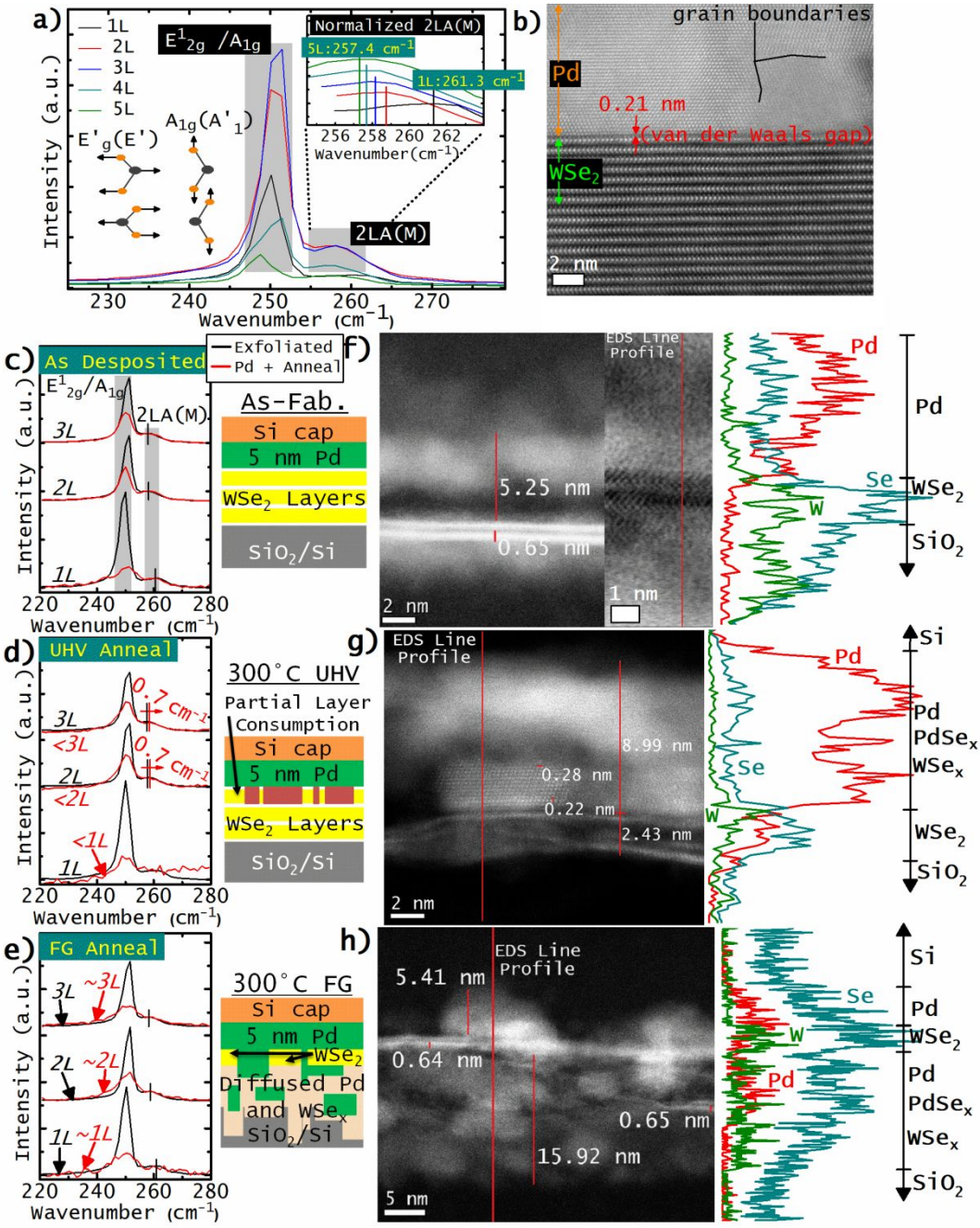


Figure 3: a) Characteristic layer number dependent shifts of E^1_{2g}, A_{1g}, and 2LA(M) vibrational modes of WSe_2 from one layer (1L) to 5 layers (5L) thick. The inset in a) displays zoomed in, normalized regions of the spectra in a) explicitly showing the layer number dependent wavenumber shift. b) Cross section TEM image highlighting the van der Waals gap formed between Pd and bulk WSe_2 at RT. Raman spectra obtained from 1L, 2L, and 3L WSe_2 prior to (black) and following (red) c) 5 nm Pd deposition under UHV conditions and subsequent annealing in d) UHV or e) FG at 300 °C. f-h) TEM images and EDS spectra obtained from FIB cross sections of the same 2-3L WSe_2 from c-e). Schematics of Pd/WSe_2 interface chemistry according to Raman Spectra are displayed adjacent to associated plots.

Raman spectra obtained from 1L, 2L, and 3L WSe_2 following Pd deposition under UHV conditions at RT (Figure 3) are expected to reflect an absence of interface reactions characteristic of a vdW interface as indicated by XPS. Phonon mode splitting, due to inhomogeneous Pd growth or interface bonding–induced non–uniform strain[48] in WSe_2 layers, is not observed in any of the spectra following Pd deposition at RT (Figure 3c). More importantly, the 2LA(M) shift detected from the 1L, 2L, and 3L flakes is much less than the ±0.2 cm^{-1} error of the spectrometer following Pd deposition at RT, indicating unperturbed WSe_2. However, the intensity of the E^1_{2g}/A_{1g} peak decreases slightly relative to that of the 2LA(M) peak following RT Pd deposition. The A_{1g} mode is expected to be 8× the intensity of the E^1_{2g} mode. Therefore, it is reasonable to conclude that, although RT Pd deposition does not result in detectable reactions with WSe_2, the full coverage film dampens the out of plane vibrations resulting in decreased A_{1g} intensity relative to the 2LA(M) peak.

Annealing Pd/1L WSe_2 under UHV conditions at 300 °C results in partial quenching of the E^1_{2g}/A_{1g} modes and complete quenching of the 2LA(M) modes suggesting partial layer consumption due to the interface reactions (Figure 3d). Therefore, the anneal transforms the predominantly top Pd contact configuration at RT into a pseudo–edge contact, which is predicted to exhibit superior electrical performance compared with a top Pd–WSe_2 contact.[37] A weak feature detected around the initial E^1_{2g}/A_{1g} peak position after annealing indicates only traces of the 1L 2H–WSe_2 structure persist. The E^1_{2g}/A_{1g} peaks detected from both 2L and 3L WSe_2 after annealing at 300 °C under UHV conditions exhibit asymmetric broadening to lower wavenumber consistent with a direct proportionality between the concentration of defects in WSe_2 and the magnitude of E^1_{2g} blue shift.[55] In addition, the 2LA(M) peak exhibits an apparent 0.7 cm^{-1} redshift and noticeable broadening in the cases of both 2L and 3L WSe_2 after 300 °C UHV anneal, suggesting the

consumption of one layer according to the expected 0.5±0.2 cm^{-1} 2LA(M) red shift transitioning from 3L to 2L WSe_2. However, a 0.7 cm^{-1} red shift is significantly less than that expected of a transition from 2L to 1L WSe_2. This suggests layer consumption is incomplete during the 300 °C UHV anneal, which manifests as broadening from a convolution of multiple peaks in the spectrum around 260 cm^{-1} (Figure 3d).

In contrast, after annealing at 300 °C in FG, neither the E^1_{2g}/A_{1g} nor 2LA(M) modes detected from any of the 1L, 2L, or 3L WSe_2 flakes exhibit appreciable shifts (Figure 3e). Additionally, these modes remain above the limit of detection even in the case of 1L WSe_2 and exhibit significant broadening in all cases indicating reactions with Pd induced by FG anneal. The broadened but detectable E^1_{2g}/A_{1g} and 2LA(M) modes even in the case of 1L WSe_2 suggests there are regions in which the original 2H structure of WSe_2 is preserved adjacent to the disordered regions. These results corroborate XPS–indicated persistence of WSe_x throughout post metallization annealing in FG.

After probing with Raman spectroscopy, lamella were milled from the same WSe_2 flakes with a focused ion beam (FIB). Each interface was interrogated by high resolution STEM and EDS (Figures 3f–h) and corroborate the interpretation of the Raman spectra discussed above before and after Pd deposition and post metallization anneal. The STEM image and corresponding EDS profile obtained from a 2L WSe_2 flake after Pd deposition at RT (Figure 3f) confirm the vdW nature of the Pd–WSe_2 interface (Figure 3b) as Se and W are below the limit of EDS detection throughout the Pd film. In addition, the two WSe_2 layers are represented by parallel regions of bright contrast ~0.7 Å thick with a darker contrast region between them corresponding to the interlayer vdW gap. A narrow region of bright contrast in direct contact with the top WSe_2 layer corresponds with a wetting layer of Pd as indicated by the EDS spectrum in Figure 3f. The oxygen

concentration is on the order of the noise level in EDS spectra (<0.1 at. %) within the Pd–WSe_2 region for all lamella discussed here (Figure S8). Any crystalline structure within the Pd film deposited at RT is not evident in the TEM image shown in Figure 3f, but a thicker Pd film (~20 nm) deposited at RT on WSe_2 exhibits polycrystallinity (Figure 3b). The 5 nm Pd film deposited on WSe_2 flakes could be below the critical thickness for Pd crystallization at RT on WSe_2.

The 3L WSe_2 and deposited Pd film are altered structurally while annealing under UHV conditions (Figure 3g) compared with the ordered nature observed only after RT deposition. The EDS spectrum in Figure 3g shows Se outdiffusion into the Pd, which corroborates $PdSe_x$ formation at the expense of the underlying WSe_2, which is consistent with the XPS and Raman data. There is also a thin region of W–rich WSe_x localized to the Pd–WSe_2 interface corresponding to the WSe_x that forms while annealing under UHV conditions (observed in the XPS spectra). Se outdiffusion and WSe_2 fragmentation indicated by STEM and EDS agree well with the disordering of the 1L WSe_2, observed in the corresponding Raman spectra. Interestingly, Pd undergoes partial crystallization at 300 °C in UHV. The {111} plane of the nanocrystal, visible in Figure 3g, interfaces with the underlying WSe_x as evidenced by the 0.22 nm interatomic distance and 0.28 nm interplanar distance, which are consistent with the ⟨110⟩ family of directions and {111} family of planes in face–centered cubic Pd (a = 0.39 nm), respectively.[56] The statistical distribution of different Pd nanocrystal facets in direct contact with WSe_2 could significantly affect the contact performance and band alignment as Φ_{Pd} varies by up to 0.4 eV depending on the crystallographic orientation.[57]

STEM images and EDS spectra obtained from 2L WSe_2 after post metallization FG annealing at 300 °C show an extremely disordered Pd–WSe_2 structure (Figure 3h), similar to post metallization annealing under UHV conditions. Interestingly, EDS indicates Pd diffuses through

WSe_2 and up to 16 nm into the underlying SiO_2 (region of patchy bright contrast below WSe_2). Previous reports have demonstrated the highly favorable nature of Pd diffusion into SiO_2 even at moderate annealing temperatures such as those employed here.[58] In addition, Se and W are detected by EDS throughout the Pd/SiO_2 layer formed under WSe_2 suggesting Se and W are carried into the SiO_2 substrate with the Pd diffusion front. Both layers of the structure towards the right of the STEM image in Figure 3g are ~7 Å thick and a region of dark contrast between the layers is resolvable, which indicates a vdW gap is present. This suggests the kinetics of Pd diffusion through WSe_2 and into the underlying SiO_2 enables the movement of whole WSe_2 fragments into the substrate. Only Se diffuses upwards into the Pd clusters remaining on top of the WSe_2. Despite fragmentation, the 2L structure of remaining WSe_2 fragments is preserved during post metallization annealing in FG in agreement with the corresponding Raman spectra. It is important to note here that the WSe_2 FETs described below are fabricated on an Al_2O_3 substrate, not thermally grown SiO_2. The Pd–Al_2O_3 interface is stable at the annealing temperatures employed here unlike the Pd–SiO_2 interface.[59] Therefore, the conclusions drawn regarding the Raman spectroscopy and TEM results discussed above only apply to WSe_2 devices fabricated on an SiO_2 substrate and do not extend to the WSe_2 FETs discussed below. The effects of significant Pd diffusion into the back gate SiO_2 in the contact regions of a FET are unknown.

These results clearly show post metallization annealing can perturb not only the interface chemistry but also the structure of Pd–WSe_2, with more significant disordering at elevated temperature under FG conditions in which Pd not only disrupts the WSe_2 but also the SiO_2 substrate (Figure 3c-h). In addition, a pseudo edge contact is formed during the post metallization anneal which enhances hole injection efficiency (discussed in the next section). These results are

consistent with predictions of Pd–Se covalent bonds and a lower carrier injection barrier in the edge contact configuration.[37]

Understanding how many TMD layers are affected by reactions at the metal–TMD interface could offer an additional robust approach to improve contact performance in TMD–based devices. In a device where the contact metal consumes at least one TMD layer, the intermetallic formed likely remains in lateral contact with the adjacent TMD channel. Therefore, any TMD layers in the contact region consumed by reactions at the metal–TMD interface should be considered pseudo edge contacts, while simultaneously in top contact with underlying, unperturbed layers. Therefore, it may be possible to tune charge injection by deliberately choosing the number of TMD layers in the contact region of a TMD–based device according to the number of 'sacrificial' layers consumed by reactions and the resulting band structure of preserved layers. Competing contributions from lateral injection from the channel to the intermetallic and vertical injection from the underlying unperturbed TMD to the intermetallic must be considered when designing a representative device.[60,61]

Band Alignment and Electrical Performance in Pd–WSe_2 Stacks and Transistors

Figure 4a displays the absolute binding energies of the WSe_2 chemical state in the Se $3d_{5/2}$ core level spectra detected from bulk WSe_2 after exfoliation and subsequent stepwise metal deposition and post metallization annealing.[62]

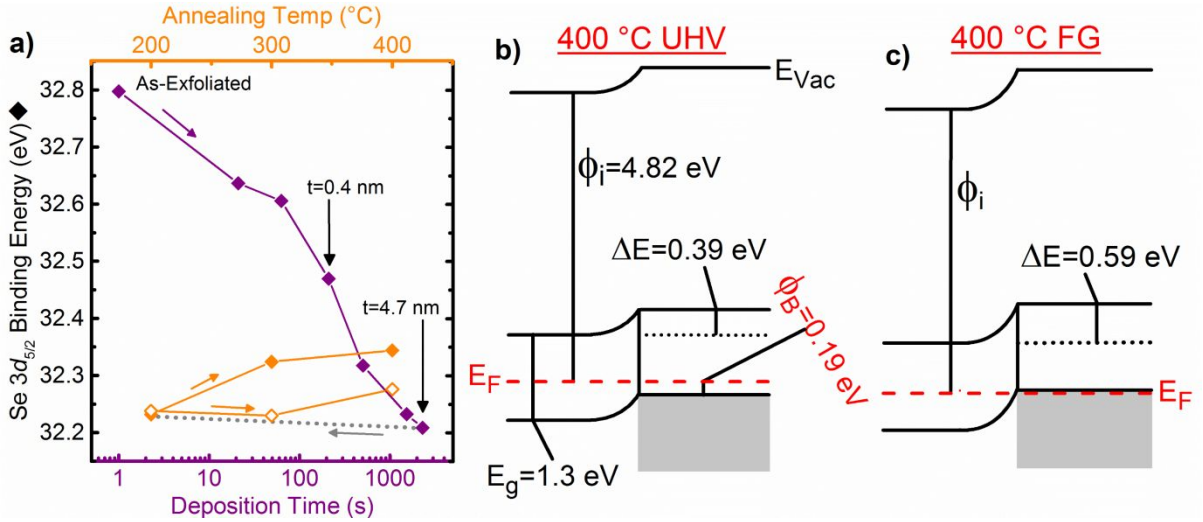


Figure 4. a) Binding energies of the bulk WSe_2 chemical state in the Se 3*d* core level spectra throughout stepwise Pd deposition and post metallization annealing under either UHV or FG conditions. The Se $3d_{5/2}$ binding energy shifted to virtually the same value after the final Pd deposition step on each sample. Therefore, only the data obtained from the 'UHV annealed' sample prior to annealing is shown (purple). The Se $3d_{5/2}$ binding energy detected on the UHV (FG) annealed sample are represented by the closed (open) diamonds. b, c) Corresponding band diagrams obtained from initial WSe_2 work function and valence band edge offset (Figure S9) in conjunction with core level shifts throughout annealing, which show the hole Schottky barrier formed by the UHV anneals and Ohmic hole band alignment formed by the FG anneals.

Exfoliated WSe_2 prior to Pd deposition exhibits a Fermi level (E_F) = 0.58 eV from the valence band edge considering the initial Δ_{VB} offset and work function (0.58±0.07 eV and 4.82±0.06 eV, respectively; Figure S9). The bulk WSe_2 chemical states shift to lower BE throughout Pd deposition. A total shift of -0.59 eV is detected after 4.7 nm Pd is deposited (Figure 4a), which corresponds with substantial upward band bending and a E_F position within the VB. Therefore, XPS indicates that a Pd contact deposited on WSe_2 under UHV conditions should exhibit Ohmic hole behavior, which agrees well with device performance reported previously[14] and obtained in this work. The E_F position does not change during the 200 °C UHV anneal consistent with an absence of reaction products detected by XPS. A cumulative +0.19 eV E_F shift is detected after anneals at 300 °C and 400 °C under UHV conditions, which is associated with the formation of a 0.19 eV hole Schottky barrier (Figure 4b) and corresponds with a subsequent

increase in concentration of $PdSe_x$ and WSe_x (Figure 1d). The increase in concentration of $PdSe_x$ and of Se vacancies in WSe_x[63] likely contributes to the formation of a hole Schottky barrier, but the most important effect of the 400 °C UHV anneal is the formation of Pd–Se bonds and corresponding enhanced contact performance.

Prior to Pd deposition and FG anneals, WSe_2 exhibits a $E_F = 0.48 \pm 0.08$ eV above the valence band edge (Figure 4a, S9). Impurities typically detected in WSe_2 (even in synthetic crystals) can act as unintentional dopants, which likely causes the spatial E_F variation (up to 0.1 eV) observed across the exfoliated WSe_2 samples investigated here.[64] The E_F remains unperturbed after annealing at 300 °C in FG but exhibits a minor +0.06 eV shift after 400 °C FG anneal. Therefore, the E_F remains within the VB after 400 °C FG anneal in contrast to the hole Schottky barrier created by annealing Pd–WSe_2 at 300 °C under UHV conditions (Figure 4c). Interestingly, annealing in FG converts Pd to $PdSe_x$ in a much greater concentration compared with that under UHV conditions regardless of annealing temperature (Figure 2c). Because of this, the E_F remains within the VB throughout annealing in FG unlike under UHV conditions. Therefore, hydrogen, which likely diffuses throughout the Pd–WSe_2 interfacial region while annealing in FG, seems to play a significant role in passivating defects (*e.g.* WSe_x) generated by the reactions. In addition, certain species of $PdSe_x$ (*e.g.* Pd_4Se, Pd_7Se_4) exhibit metallic conductivity ($\sigma \approx 10^4$–10^5 Ω^{-1} cm^{-1}). The combination of maximizing $PdSe_x$ concentration and passivating defects at the Pd–WSe_2 interface by performing the anneal in FG is critical to forming consistent high–performance Pd hole contacts to WSe_2.[39]

To corroborate the XPS–derived band alignments discussed above with electrical behavior of representative devices, bulk WSe_2 Schottky diodes and back gated, few layer (7-10 layer flake thickness) WSe_2 transistors were fabricated with Pd contacts and subjected to anneals in either FG

or UHV at 200 °C, 300°C, and 400 °C for 1 hr each. Their electrical performance was evaluated throughout the experiment. It is important to note that the WSe_2 FETs were fabricated on an Al_2O_3 substrate deposited on Si by atomic layer deposition unlike the Si/Pd/WSe_2/SiO_2/Si samples fabricated for analysis by Raman spectroscopy and TEM.

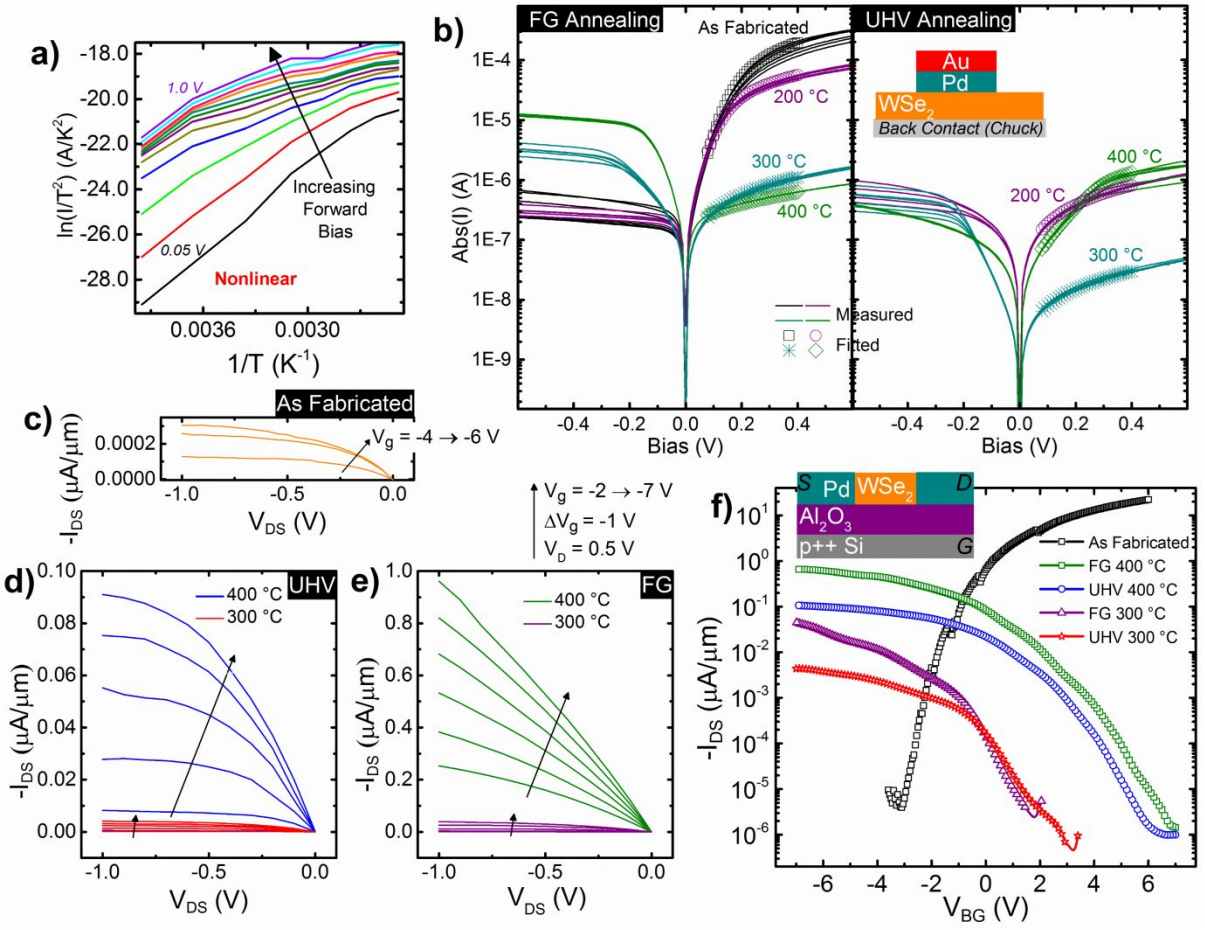


Figure 5. a) Representative Arrhenius plot of Pd–WSe_2 Schottky diodes after fabrication and throughout annealing in either UHV or FG showing nonlinear temperature dependence. b) I-V curves obtained from Pd–WSe_2 Schottky Diodes after metallization and annealing in UHV or FG (lines) with nonlinear regression fits (symbols) obtained using an inhomogeneous Schottky barrier height model. Reverse bias I_{DS}–V_{DS} of Pd contacts to back gated WSe_2 devices after c) fabrication and annealing at 200 °C (not shown), 300 °C, and 400 °C in d) UHV and e) FG. f) I_{DS}–V_{BG} of the same devices showing dramatic improvements in the hole conduction after annealing.

Figure 5a shows a nonlinear Arrhenius plot reflecting I–V measurements obtained from a Pd–WSe_2 Schottky diode at forward bias voltages from 0.05 V to 1.00 V and temperatures from -

20 °C to 130 °C. Nonlinear temperature dependence is observed for all samples regardless of annealing temperature except after the 400 °C FG anneal (Figure S12), in which case the barrier height is significantly underestimated (see Supporting Information for discussion). Therefore, thermionic emission does not accurately describe the conduction mechanism for all annealing conditions investigated here. TMDs can exhibit high defect densities that dominate the electrical behavior of a metal–TMD junction.[27] Therefore, a Schottky barrier model[65] that accounts for the effects of an unknown aerial density (ρ_p) of circular low Schottky barrier regions with radius r_p surrounded by non–defective regions with a different electron Schottky barrier height (SBH, Φ_{B0}) was employed to extract Φ_{B0}, ρ_p, the modified Richardson constant (A**), series resistance (R_s), and difference in Schottky barrier height between defective and non–defective regions (Δ) according to annealing conditions. Eq. (1) was fitted to the measured forward bias I–V data in Figure 5b via nonlinear regression.

$$I_{total} = AA^{**}T^2 e^{\frac{-\Phi_{B0}}{kT}}\left[e^{\frac{q(V_{applied}-R_s I_{total})}{kT}}-1\right]\left[1+\rho_p\frac{\pi kT\left(r_p^2\Delta\right)^{\frac{1}{3}}\eta^{\frac{2}{3}}}{3q(V_{bb})^{\frac{2}{3}}}\exp\left(\frac{-q\phi_{B0}}{kT}+\frac{3q\left(r_p^2\Delta\right)^{\frac{1}{3}}(V_{bb})^{\frac{1}{3}}}{kT\eta^{\frac{1}{3}}}\right)\right] \quad \text{Eq. (1)}$$

where

$$V_{bb} = \phi_{b0} - V_{b0} - V_{applied} + R_s I_{total} \quad \text{Eq. (2)}$$

and

$$\eta = \frac{\varepsilon_s \varepsilon_0}{q(N_a - N_d)} \quad \text{Eq. (3)}$$

The model also considers the area of the diode (A), the temperature (T), the applied bias ($V_{applied}$), the band bending of the barrier in the non–defective regions (V_{b0}), the bulk WSe_2 dielectric constant (ε_s), and the unintentional doping density of the WSe_2 (N_a-N_d). WSe_2 doping densities of $1.30 \times 10^{17} \pm 0.35 \times 10^{17}$ cm^{-3} and $1.19 \times 10^{17} \pm 0.39 \times 10^{17}$ cm^{-3} for the samples annealed in UHV and FG, respectively, were determined by the $1/C_2$ vs V method (Figure S13), which is described in detail in the Supporting Information.

SBH extracted after fabrication and annealing in UHV or FG are listed in Table 1. The r_p was fixed at 1.5 nm according to a previous detailed STM study of defects in WSe_2.[64] A close fit of the forward bias I–V data is obtained in all cases ($R^2 > 0.99$), yielding a relatively low $R_s \approx 80 \pm 16$ Ω, reasonable A** ≈ 10 ± 2 A/cm^{-2} K^{-2}, $\Phi_{B0} = 1.29 \pm 0.05$ eV, $\Delta = 1.10 \pm 0.05$ eV and $\rho_p = 3.6 \times 10^{12} \pm 3.1 \times 10^{12}$ cm^{-2} prior to annealing in UHV or FG are extracted from the two respective samples (Table 1, Figure 6, R_s and A** are averaged from six diodes on each sample). The extracted Φ_{B0} and ρ_p are in good agreement with the XPS–derived band alignment (electron Schottky barrier height of 0.01 ± 0.10 eV) and previous STM–derived aerial defect density (10^{12} cm^{-2}).[64] The ρ_p is relatively high (compared to defect densities in more mature semiconductors) but below the XPS detection limit (0.1 at. %), which explains why additional chemical states corresponding with the low SBH regions are not detected in W 4*f* and Se 3*d* core levels prior to annealing (Figures S1–3). The effective Richardson constant previously extracted from an Au–WSe_2 Schottky diode (27.6 A/cm^{-2} K^{-2}), which corresponds to a hole effective mass of $0.23m_0$,[66] is larger than the A** obtained here employing a hole effective mass of $0.33m_0$. It would be useful to compare the ideality factor of the Schottky diodes fabricated in this work with other reports in the literature, but the ideality factor is not included in the model[65] employed here to extract key parameters from the I–V characteristics.

The 400 °C UHV anneal suppresses (enhances) the reverse (forward) bias current (Figure 5b), corresponding with an increased hole SBH ($\Phi_{B0} = 1.07 \pm 0.02$ eV), which is in close agreement with the XPS–derived appreciable hole Schottky barrier formed by the UHV anneal (XPS: electron Schottky barrier height of 0.19 eV).

Table 1: Electron and hole Schottky barrier heights and the corresponding WSe_2 band gap extracted from Pd–WSe_2 Schottky diodes and FETs after fabrication and subsequent annealing in either UHV or FG.

Schottky Diode		**UHV**			**FG**		
	As Fab.	*200 °C*	*300 °C*	*400 °C*	*200 °C*	*300 °C*	*400 °C*
Φn (eV)	1.29	1.29	1.27	1.07	1.29	1.29	1.29
Φp (eV)	0.01	0.01	0.03	0.23	0.01	0.01	0.01
Band Gap (eV)	1.3	1.3	1.3	1.3	1.3	N/A	1.3
FET		**UHV**			**FG**		
	As Fab.	*200 °C*	*300 °C*	*400 °C*	*200 °C*	*300 °C*	*400 °C*
Φn (eV)	0.73	0.99	1.02	1.05	0.99	N/A	1.33
Φp (eV)	0.65	0.5	0.43	0.34	0.44	N/A	0.06
Band Gap (eV)	1.38	1.49	1.45	1.39	1.43	N/A	1.39

After the 400 °C FG anneal, the reverse (forward) bias current is increased (suppressed) by 100×, which corresponds with a $\Phi_{B0} = 1.29 \pm 0.01$ eV and corroborates the XPS–derived Ohmic band alignment (E_F resides within the valence band). Furthermore, the 400 °C FG anneal effectively eliminates the diode–to–diode I–V variability and reduces the ρ_p to 2.0 x 10^7 cm^{-2}, facilitating the dramatic improvement in hole conduction, contact performance consistency, and defect passivation achievable through enhanced $PdSe_x$ formation and H* radicals provided by the FG anneal.

It is difficult to accurately extract electron and hole SBH from the transfer characteristics of ambipolar ultra–thin body FETs. Employing a thermionic emission model, which neglects tunneling, is of questionable validity considering tunneling current is appreciable in devices where

the depletion width is defined by the channel thickness, as is the case in few layer TMD FETs.[17] Therefore, in this work we employ an analytical Schottky barrier height model based on Landauer theory to extract both the electron and hole SBH from the transfer characteristics of back gated WSe_2 FETs before and after annealing (method and equations described elsewhere).[67] This model accounts for both thermionic and tunneling contributions to the total current density and therefore the band alignment can be accurately extracted from the measured I_{DS} in the subthreshold region, where conduction depends on the Schottky barriers at the contacts and scattering in the channel is negligible. The band gap of the 7-10 layer WSe_2 flakes employed in the FETs is ~1.4 eV according to previous work, which is slightly larger than the band gap of bulk WSe_2 (~1.3 eV). The larger band gap in the few layer WSe_2 FETs is accounted for in the Landauer theory-based model. Another study demonstrated the band gap increase from many to single layer WSe_2 manifests as an increase in the ionization energy, while the electron affinity remains roughly constant regardless of the number of WSe_2 layers. Therefore, the band gap discrepancy between the few layer WSe_2 FETs and the bulk WSe_2 samples is accounted for by assuming the conduction band edge is constant relative to the vacuum level and applying band gap differences between bulk and few layer WSe_2 to the corresponding ionization energy, as indicated in Figure 6 (E_V: few layer). The SBH extracted from Pd–WSe_2 FETs after fabrication and subsequent annealing in either UHV or FG are listed in Table 1 and the corresponding fits obtained using the analytic Schottky barrier model are displayed in Figure S14. Prior to annealing, the E_F is pinned near the middle of the bandgap in contrast with the as–fabricated band alignments extracted from Pd–bulk WSe_2 discussed earlier (Figure 6). Photoresist residue in the contact regions, which is not present in samples fabricated on bulk WSe_2, could play a role in pinning the E_F near midgap in as–fabricated FETs, which would explain the near–midgap E_F position. The discrepancy between the band

alignment of the FETs and the bulk WSe_2 samples is reduced after the 200 °C and 300 °C anneals, which indicates the anneals neutralize the organic residue that causes the Fermi level pinning as the temperature is increased. However, a detailed study is needed to quantitatively determine the effects of photoresist residue on the band alignment between metal contacts and TMDs.

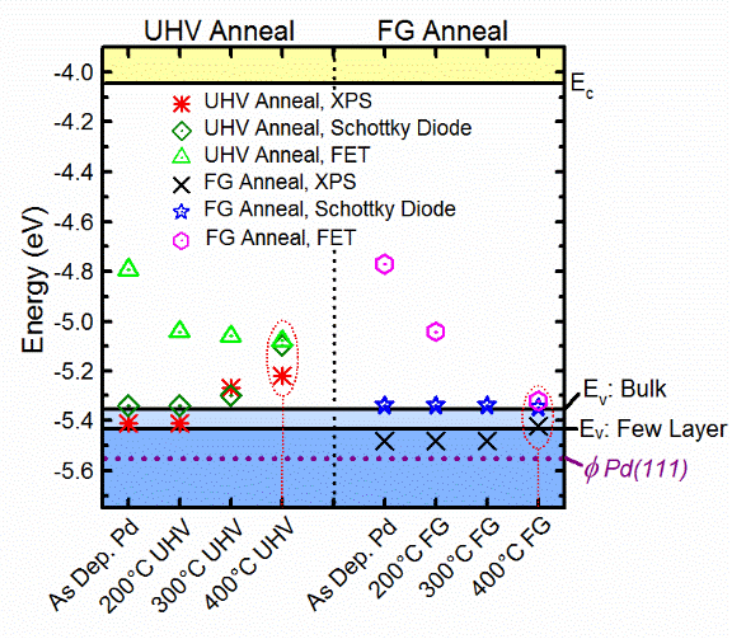


Figure 6. Pd–WSe_2 band alignment determined by XPS (UHV *, FG ×), Schottky diodes (UHV ◇, FG ★), and FETs (UHV △, FG ⬢) after fabrication and throughout post metallization annealing showing the appreciable hole Schottky barrier formed by the 400 °C UHV anneal and the Ohmic hole band alignment formed by the 400 °C FG anneal in the case of all barrier height extraction techniques.

According to the analytic Schottky barrier model, the 400 °C FG (UHV) anneal decreases the hole Schottky barrier to 0.10 eV (0.23 eV), corresponding with a significant increase in reverse bias I_{DS} by ~10^4 (~10^3) (Figure 5c–e). Regardless of annealing ambient, increasing the annealing temperature from 300 °C to 400 °C results in an off state V_G shift of 4–5 V and the saturation current increases by ~10^2 (Figure 5f), which is consistent with hole–dominant conduction that is enhanced as the annealing temperature increases. The 400 °C FG anneal produces I_{DS}–V_{DS} that are linear beyond V_{DS} = -1 V (at V_{DS} = -5 V, $I_{DS,sat}$ = ~5 μA/μm) unlike devices annealed under UHV,

which reach saturation around V_{DS} = -1 V. Critically, annealing to 400 °C in FG results in an Ohmic band alignment according to the analytic Schottky barrier model as well as a 10× increase in I_{ON}/I_{OFF} ratio compared with the 0.23 eV hole Schottky barrier and I_{ON}/I_{OFF} achieved at 400 °C under UHV. This confirms an Ohmic hole band alignment is formed by annealing in FG and indicates contact performance greatly improves with increasing $PdSe_x$ concentration. Therefore, Pd–WSe_2 contacts annealed under FG conditions will exhibit superior performance compared to UHV annealed or as–deposited Pd–WSe_2 contacts (Figures 5,6). Furthermore, annealing in FG at 400 °C decreases the I_{OFF} by 10^2 compared with the I_{OFF} prior to annealing (Figure S14). Interfacial defects passivated by H* during the FG anneal could play a significant role in reducing the I_{OFF}. This highlights FG annealing as a critical step to superior Pd–WSe_2 contact performance.

Based on the physical and electrical characterization, the E_F shifts according to XPS, Schottky diodes, and FET transfer characteristics, it is clear that a post metallization anneal at 400 °C in FG results in an Ohmic Pd hole contact to WSe_2 with reduced performance variability. Furthermore, the I_{ON}/I_{OFF} ratio achieved by annealing Pd–WSe_2 transistors in FG (4×10^6) is more than an order of magnitude greater than that achieved by annealing under UHV (1×10^5). This correlates to an enhanced $PdSe_x$ formation after annealing at 400 °C in FG. The relative concentration ratio of $PdSe_x$:Pd is 2.3 for the FG anneal compared with just 0.7 after annealing at 400 °C in UHV. This work demonstrates Pd–WSe_2 interface engineering for high performance Ohmic–like hole contacts, an applicable strategy in many metal–TMD systems, and represents significant progress towards achieving low power electronics benchmarks.[14]

Conclusions

This work demonstrates 10^5 increase in drain current under reverse bias for Pd hole contacts to WSe_2 by deliberately forming a $PdSe_x$ interfacial intermetallic and passivating pre–existing defects with hydrogen through post metallization annealing at 400 °C in FG. Furthermore, $PdSe_x$ formation in FG corresponds with a 0.6 eV reduction in hole SBH, I_{ON} increase of 10^4, and an I_{OFF} decrease by 10^2 compared with as–fabricated Pd–WSe_2 transistors. These metrics highlight the need for the 60 minute 400 °C FG anneal to achieve high performance Pd contacts and suggests hydrogen plays an integral part in defect passivation. XPS indicates ~3× higher $PdSe_x$ concentration and Ohmic band alignment form as a result of the 400 °C FG anneal compared with the $PdSe_x$ concentration and 0.2 eV hole Schottky barrier that form during 400 °C UHV anneal. Raman spectroscopy and STEM corroborate the van der Waals interface formed with WSe_2 during RT Pd deposition, representing the first reported experimental observation by STEM of the often theorized van der Waals gap between a non–reactive metal and TMD, and explicitly show a much greater degree of intermixing after FG annealing than after UHV annealing. A sacrificial WSe_2 layer in addition to the 400 °C FG anneal is needed to accommodate the $PdSe_x$ formation critical to achieve the high performance Pd contacts to WSe_2 demonstrated here. This work shows that a carefully chosen combination of characterization techniques can be leveraged to engineer high performance in any metal–semiconductor based device beyond the Pd–WSe_2 system discussed here. A more comprehensive understanding of the relationships between processing conditions, contact chemistry, and device performance would significantly advance TMD–based technology.

Methods

Metal Deposition, Post–Metallization Annealing, and in–situ *Characterization.*

a) Single Deposition Step Under UHV or HV Conditions: All WSe_2 samples throughout this work were obtained from the same bulk WSe_2 crystal (HQ Graphene).[68] Prior to deposition under

UHV or HV conditions, WSe_2 and Pd metal source were prepared and metal deposition rates and reference metal core level spectra were obtained identical to that employed in similar work described elsewhere.[29,30] The reference Pd 3*d* core level spectrum was obtained *in–situ* from a 50 nm Pd film evaporated on Si at RT in UHV. A standard Scotch Tape© method was employed *ex–situ*. The surface chemistry was probed with XPS both after exfoliation and subsequent metal deposition under UHV conditions (base pressure $<2 \times 10^{-9}$ mbar).

b) Step–wise Deposition and Post–Metallization Annealing: After outgassing the metal source and determining the deposition rate, Pd was deposited in steps on separate bulk WSe_2 crystals under UHV conditions to target thicknesses of 1, 2, 10, 20, 30, and 50 Å. Each sample was then annealed in UHV or FG (10% H_2, 90% N_2; 1 mbar) at 200 °C, 300 °C, and 400 °C. The surface chemistry was probed with XPS after exfoliation and each subsequent deposition and annealing step. The secondary electron (SE) cutoff was also probed with XPS throughout metal deposition steps and post metallization annealing to track the work function. Additional details regarding the procedure employed in fitting high resolution core level spectra and band diagram construction can be found in the Supporting Information. The cluster tool in which deposition and analysis were performed is described in detail elsewhere.[69,70]

XPS Instrumentation, Parameters, and Data Analysis. XPS characterization was performed via a monochromated Al Kα source and Omicron EA125 hemispherical analyzer with ±0.05 eV resolution. In addition, a takeoff angle of 45°, acceptance angle of 8°, and pass energy of 15 eV were employed during high resolution spectral acquisition. The analyzer was calibrated with polycrystalline Au, Ag, and Cu foils according to ASTM E1208.[71] Spectra were deconvolved using AAnalyzer,[72] a curve fitting software.

Quantifying Layer Number Consumption: Sample Fabrication and Characterization. WSe_2 flakes were exfoliated onto a SiO_2(270 nm)/Si substrate and annealed *in–situ* at 300 °C in Ar (base pressure $<2 \times 10^{-8}$ mbar, backfilled with Ar to 10^0 mbar) to remove tape residue. Numerous 1 to 5 layer (*i.e.* 1L to 5L) flakes were then identified with optical microscopy, atomic force microscopy (AFM) and Raman spectroscopy (see Supporting Information for more details). Special care was taken to ensure 5 nm thick Pd films subsequently deposited at RT under UHV conditions were full coverage and pinhole–free (see Supporting Information). Separate samples were annealed after metallization *in–situ* in UHV or FG at 300 °C for 1 hr. Immediately following metal deposition and, in the case of two of three samples, post metallization annealing, a full coverage 10 nm thick Si film was deposited *in–situ* as a capping layer to protect Pd–WSe_2 samples from oxidation upon air exposure during *ex–situ* Raman spectroscopy. After capping with Si, the samples were removed from vacuum and Raman spectroscopy was performed on the same flakes as were probed after exfoliation. Any annealing steps were performed prior to Si capping to prevent potentially erroneous results due to intermixing between Si and underlying Pd at elevated temperatures.

A laser power density of 0.49 mW/μm^2 and detector with 0.2 cm^{-1} resolution were employed in obtaining all Raman spectra shown in the main text. Exposure times of 1 s (5 s) with 10 (5) total accumulations were employed in obtaining Raman spectra from exfoliated WSe_2 flakes after thermal cleaning (and subsequent *in–situ* metallization and, in the case of two of three samples, post metallization annealing). These parameters were carefully determined to prevent laser induced damage to WSe_2 (see section S6 for a discussion of the Raman measurement parameters and their impact on WSe_2).

Raman spectra were deconvolved with the peak fitting software AAnalyzer to obtain vibrational mode shifts. Peak shapes were defined by a combination of Gaussian and Lorentzian functions. The Lorentzian contribution was held constant for each set of spectra representing a certain number of WSe_2 layers from a given sample.

High Resolution STEM and EDS. $Si/Pd/WSe_2/SiO_2$ samples fabricated for interrogation via Raman spectroscopy were cross sectioned for high resolution STEM in an aberration corrected JEM-ARM200F instrument operated at 200 kV. STEM cross–sectional samples were prepared in a FIB microscope (FEI Nova 200 Dual Beam), images were obtained by annular bright field and high angle annular dark field (HAADF), and EDS experiments performed in an Aztec Energy Advanced Microanalysis System according to the procedure outlined in detail elsewhere.[70]

Device Fabrication and Measurements.

a) Al_2O_3 was first deposited (~27 nm) at 250 °C onto a p++ Si wafer and was followed by a 400 °C anneal under FG to reduce charge traps. The Al_2O_3 layer serves as the 'substrate' for exfoliated WSe_2 flakes. Al was then deposited as the backside contact by electron beam evaporation. Using photolithography, source/drain contacts were defined and Pd/Au (20/150 nm) contacts were then deposited under UHV by electron beam evaporation. Finally a lift–off process was performed. The devices were electrically characterized under ambient temperature and pressure in a Cascade Probe Station using a Keithley 4200 Semiconductor Characterization System.

b) Schottky Diodes: A bulk WSe_2 crystal with mirror–like surface (low surface defect density) was exfoliated and loaded into a UHV cluster tool. 60 nm Pd followed by 100 nm Au were deposited in UHV to form periodic arrays of circular Au/Pd contact pads (diameters = 50, 100, 200 μm) across the WSe_2. Forward and reverse bias I–V curves were obtained by sweeping from 0 to 2 V

and 0 to -2 V (0.01 V step), respectively, to avoid hysteresis effects. Measurements were obtained after metallization and anneals in FG (1 mbar) at 200 °C, 300 °C, and 400 °C. C–V measurements were obtained from the same diodes (in parallel with I–V measurements) at frequencies of 100 kHz, 500 kHz, and 1MHz.

Conflict of Interest. The authors declare no competing financial interest.

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Supporting Information. Se 3*d*, W 4*f*, Pd 3*d*, O 1*s*, and C 1*s* of Pd–WSe_2 at room temperature; calculating stoichiometry based on XPS; chemical stability of bulk WSe_2 up to 450 °C; W 4*f*, Se 3*d*, and O 1*s* core level spectra throughout stepwise Pd deposition and UHV post metallization annealing; W 4*f* and Se 3*d* core level spectra throughout post metallization annealing in FG; relevant bond dissociation energies; investigating laser induced damage in WSe_2 with AFM to determine optimum Raman laser parameters to both prevent WSe_2 damage and maximize spectral intensity; oxygen in EDS spectra; valence band edge and secondary electron cutoff spectra from all 'exfoliated' WSe_2 employed in determining initial band alignment; constructing band diagrams from XPS and secondary electron cutoff; AFM images and Raman spectra of mono and few layer

WSe_2 flakes prior to metal deposition; determining critical thicknesses of Pd and Si for full coverage films; Arrhenius plots and $1/C^2$ vs V plots obtained from Pd–WSe_2 Schottky diodes; measured I_{DS}–V_{BG} transfer characteristics of WSe_2 FETs fitted according to the analytic Schottky barrier height model.

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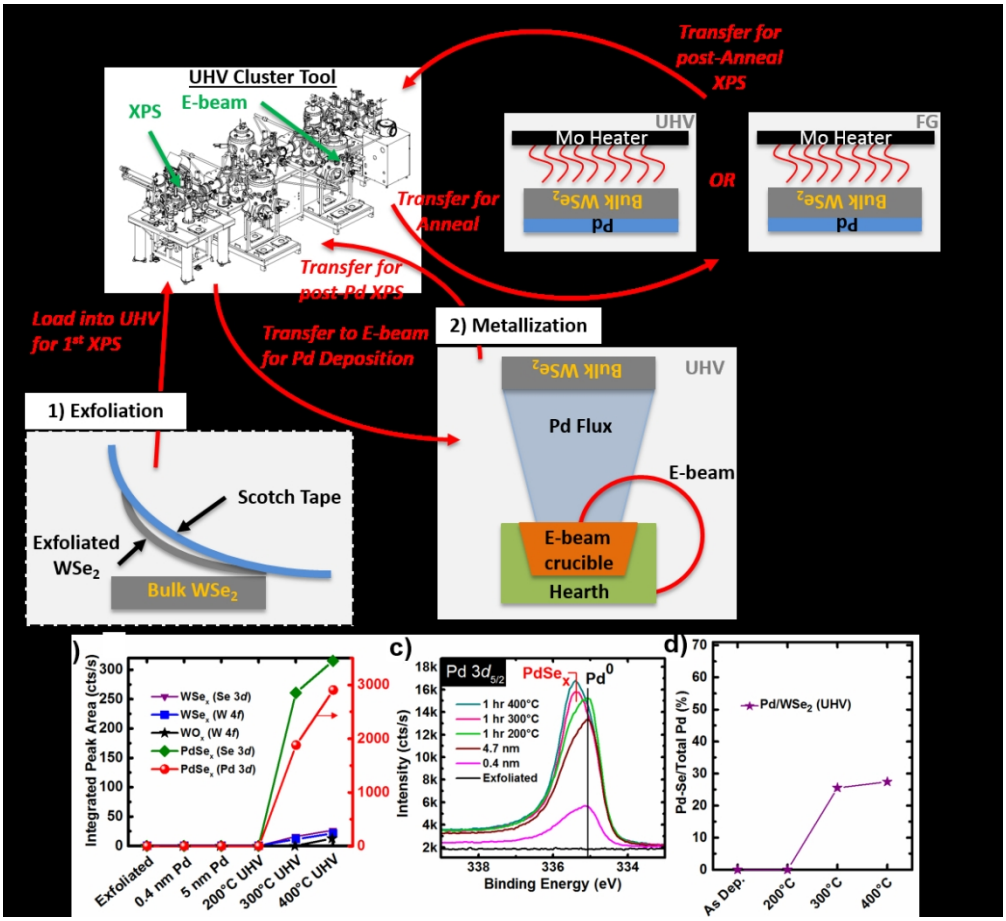


Figure 1. a) Schematic illustrating the process flow employed in fabricating Pd-WSe_2 samples for XPS analysis in–situ throughout 1) exfoliation, 2) Pd deposition in UHV and 3) subsequent anneals in UHV or FG. b) Integrated intensities of chemical states in the Se 3d, W 4f, and Pd 3d core level spectra associated with various reaction products as well as the c) Pd 3d core level spectra obtained throughout Pd deposition on WSe_2 and post metallization annealing under UHV. It is explicitly noted that the integrated peak areas shown in b) represent only the areas of the respective chemical state fitted to each denoted core level spectrum. The red line (spheres) in b) is plotted vs the right y–axis while all other data points are plotted vs the left y–axis. d) Interfacial reactivity gauged by the ratio of the intensity of the chemical state in the Pd 3d core level corresponding with $PdSe_x$ to the total intensity of the respective core level after depositing at RT and subsequent in–situ annealing in UHV showing the onset of $PdSe_x$ formation at 300 °C and 28% Pd to $PdSe_x$ conversion at 400 °C.

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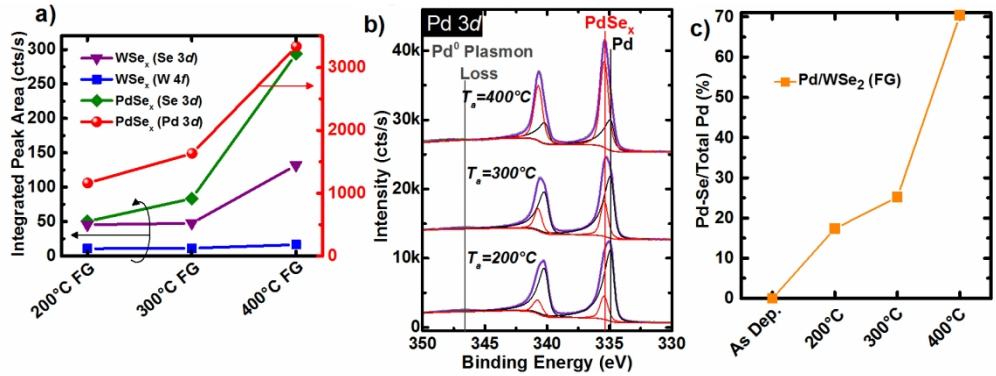


Figure 2. a) Integrated intensities (including both spin orbit split branches in each core level) of chemical states in Se 3d, W 4f, and Pd 3d core level spectra associated with various reaction products as well as the b) Pd 3d core level spectra obtained after annealing a ~50 Å Pd–WSe_2 structure under ambient pressure forming gas at 200 °C, 300 °C, and 400 °C, respectively, for 1 hr each. It is explicitly noted that the integrated peak areas shown in a) represent only the areas of the respective chemical state fitted to each denoted core level spectrum. c) Interfacial reactivity gauged by the ratio of the intensity of the chemical state in Pd 3d core level corresponding with $PdSe_x$ to the total intensity of the respective core level after depositing at RT and subsequent in–situ annealing in FG showing the onset of $PdSe_x$ formation at 200 °C and 70% Pd to $PdSe_x$ conversion at 400 °C.

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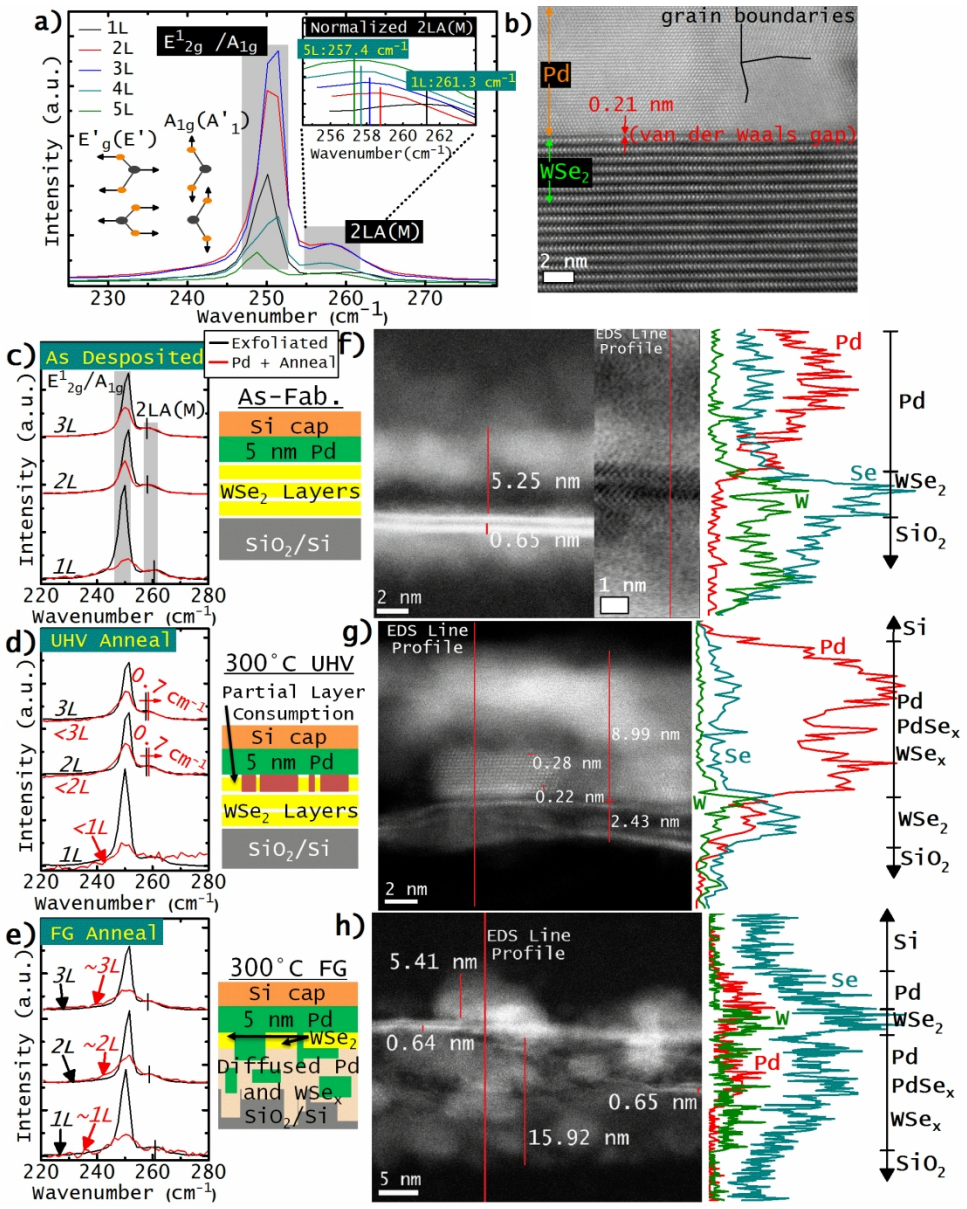


Figure 3. a) Characteristic layer number dependent shifts of E^1_{2g}, A_{1g}, and 2LA(M) vibrational modes of WSe_2 from one layer (1L) to 5 layers (5L) thick. The inset in a) displays zoomed in, normalized regions of the spectra in a) explicitly showing the layer number dependent wavenumber shift. b) Cross section TEM image highlighting the van der Waals gap formed between Pd and bulk WSe_2 at RT. Raman spectra obtained from 1L, 2L, and 3L WSe_2 prior to (black) and following (red) c) 5 nm Pd deposition under UHV conditions and subsequent annealing in d) UHV or e) FG at 300 °C. f-h) TEM images and EDS spectra obtained from FIB cross sections of the same 2-3L WSe_2 from c-e). Schematics of Pd/WSe_2 interface chemistry according to Raman Spectra are displayed adjacent to associated plots.

169x209mm (300 x 300 DPI)

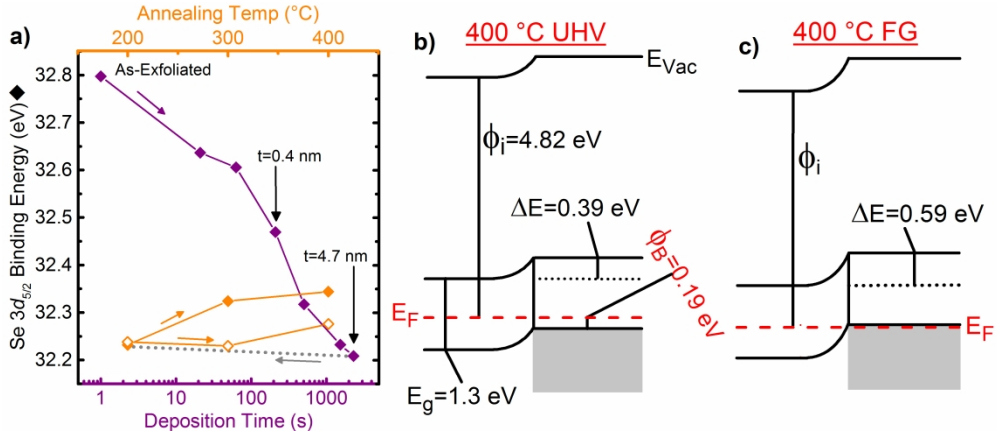


Figure 4. a) Binding energies of the bulk WSe_2 chemical state in the Se 3d core level spectra throughout stepwise Pd deposition and post metallization annealing under either UHV or FG conditions. The Se $3d_{5/2}$ binding energy shifted to virtually the same value after the final Pd deposition step on each sample. Therefore, only the data obtained from the 'UHV annealed' sample prior to annealing is shown (purple). The Se $3d_{5/2}$ binding energy detected on the UHV (FG) annealed sample are represented by the closed (open) diamonds. b, c) Corresponding band diagrams obtained from initial WSe_2 work function and valence band edge offset (Figure S9) in conjunction with core level shifts throughout annealing, which show the hole Schottky barrier formed by the UHV anneals and Ohmic hole band alignment formed by the FG anneals.

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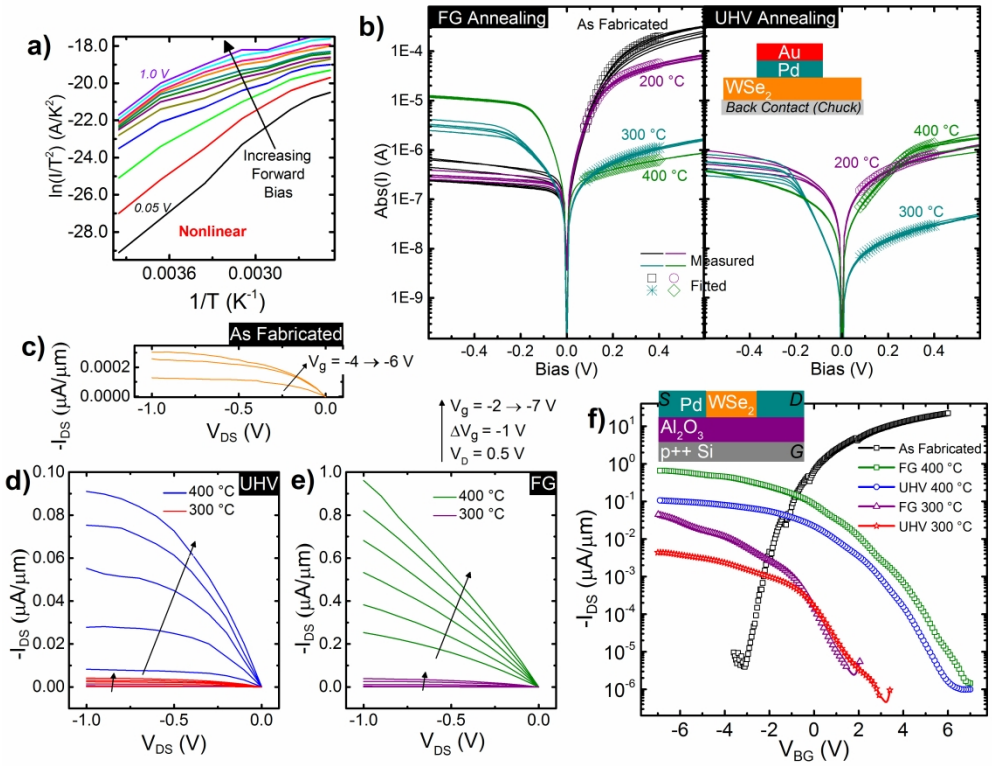


Figure 5. a) Representative Arrhenius plot of Pd–WSe_2 Schottky diodes after fabrication and throughout annealing in either UHV or FG showing nonlinear temperature dependence. b) I-V curves obtained from Pd–WSe_2 Schottky Diodes after metallization and annealing in UHV or FG (lines) with nonlinear regression fits (symbols) obtained using an inhomogeneous Schottky barrier height model. Reverse bias I_{DS}–V_{DS} of Pd contacts to back gated WSe_2 devices after c) fabrication and annealing at 200 °C (not shown), 300 °C, and 400 °C in d) UHV and e) FG. f) I_{DS}–V_{BG} of the same devices showing dramatic improvements in the hole conduction after annealing.

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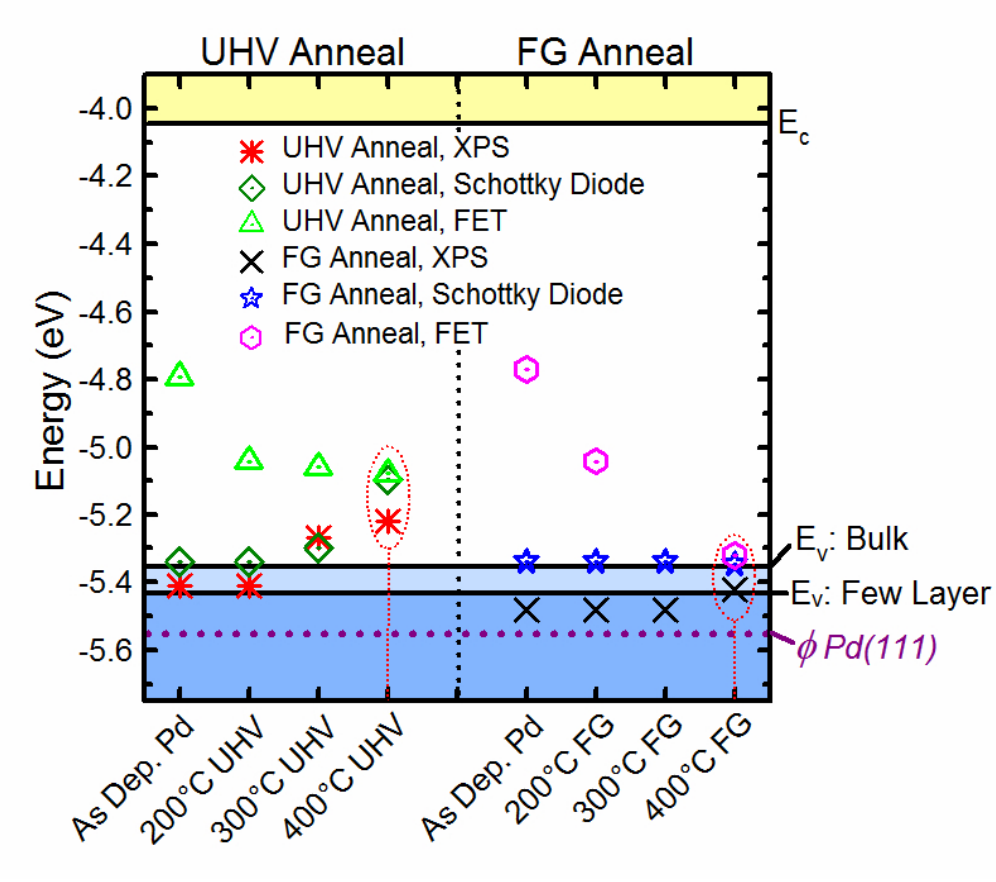
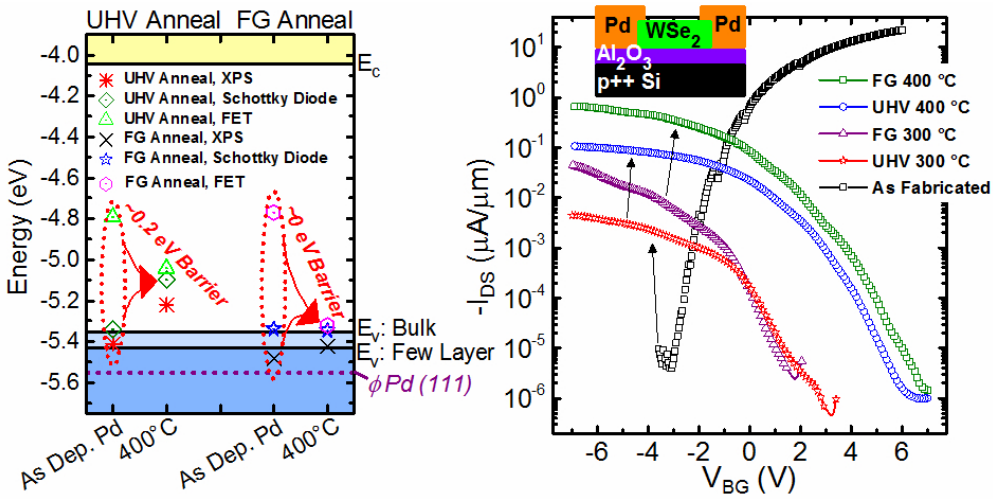


Figure 6. Pd–WSe_2 band alignment determined by XPS (UHV *, FG ×), Schottky diodes (UHV □, FG □), and FETs (UHV △, FG □) after fabrication and throughout post metallization annealing showing the appreciable hole Schottky barrier formed by the 400 °C UHV anneal and the Ohmic hole band alignment formed by the 400 °C FG anneal in the case of all barrier height extraction techniques.

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Caption : Table of Contents Only: Schottky barrier heights of Pd contacts to WSe2 extracted by XPS (Pd/bulk WSe2) and electrical measurements (Pd/WSe2 Schottky diodes and back gated FETs) at room temperature and after 400 °C anneals in ultra-high vacuum or forming gas (FG) showing a 400 °C FG anneal is the ideal post metallization process for consistent, high-performance, Ohmic-like Pd hole contacts to WSe2. The transfer characteristics of Pd/WSe2 FETs clearly demonstrate a dramatic ~105 increase in the hole branch ON current after the 400 °C FG anneal, which is more than an order of magnitude greater than that achieved by the 400 °C UHV anneal.

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