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Surface Doping and Stabilisation of Alternative CMOS Material Systems

Thesis presented by

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for the degree of

Doctor of Philosophy

University College Cork

School of Chemistry

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Declaration

This is to certify that the work I, Giuseppe Alessio Verni, am submitting is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents. I have read and understood the regulations of University College Cork concerning plagiarism and intellectual property.

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Giuseppe Alessio Verni

Abstract

Current electronic devices are built by employing numerous materials and a diverse array of fabrication processes. Semiconductors are the main building block which are used to create transistors. For the past 50 years, the size of a transistor has halved every 18-24 months, in accordance with Moore's Law, allowing the semiconductor industry to pack more of them into a single chip, which has resulted in a significant increase in the processing power of computers over this period. However, this scaling of the transistor cannot continue indefinitely due to material limitations when dev ice sizes reach the order of only a few hundred atoms; this has led to the definition from the International Technology Roadmap for Semiconductors (ITRS) of key technical challenges and requirements to sustain this scaling by going More Moore. Some of the most interesting challenges include implementation of high-mobility CMOS materials, for example by introducing Ge or III-V compounds as channel materials, as well as scaling of Si (and its alternatives) CMOS, for which it will be necessary to tackle numerous issues such as parasitic control and gate stack engineering. The introduction of alternative CMOS channel materials comes with a wide array of problems, as each material comes with its set of advantages and disadvantages. Ge CMOS has higher intrinsic mobility than Si, both for *n*-type and *p*-type carriers, but *n*-channel implementation is challenging due to source-drain doping and contacting issues. III-V materials in general lack good mobility for *p*-type carriers and therefore would need to be integrated together for example with Ge, even if this then adds to the complexity of the whole process. As already mentioned, in addition to these integration challenges there is a whole set of scaling issues that must be addressed. In order to successfully continue scaling devices down and meet performance requirements, a wide array of process and material innovations will be needed,

particularly as we transition from planar transistor, to finFET and gate-all-around (GAA) architectures which come with some manufacturing challenges. One of such challenges is the engineering of the transistor junction by conformal doping, in which the dopant addition must be precisely controlled, both spatially and quantitatively. Monolayer doping (MLD) has the potential to satisfy these needs as it allows for precise dopant control, due to its intrinsic self-limiting nature, while also being inherently conformal as it relies on surface reactions between a dopant molecule and a target surface. Chapters 3 & 4 of the thesis describe the application of MLD on high-mobility alternative channel materials, such as germanium and gallium nitride. Another challenge identified by the ITRS for future devices is the overall reduction of processes and materials used in device fabrication in order to simplify the whole process flow. For example, the implementation of a monolithic material CMOS *n*- and *p*-channel would simplify process and material requirements as there would be no need to engineer different gate dielectrics or gate metals for different channels. Bismuth has recently been shown as a potential material for the formation of monolithic transistors in which the source, drain and channel are all made of the same material and where thickness can be used as the knob to tune the electrical properties of each element of the device. This would in turn allow to greatly reduce the number of steps in the channel fabrication, thus reducing integration complexity. However, bismuth readily passivates in air and forms a surface oxide which can potentially hinder further processing steps. Chapter 5 of this thesis focuses on a novel method for the removal of the oxide and the subsequent bare bismuth surface passivation which then allows for ambient handling of the now stabilised material.

List of abbreviations

2D	**Two dimensional**
3D	**Three dimensional**
ABAPE	**Allyl boronic acid pinacol ester**
ADP	**Allyldiphenyl phosphine**
AFM	**Atomic Force Microscopy**
APTES	**Aminopropyl triethoxysilane**
CFET	**Complementary Field Effect Transistor**
CMGT	**Confinement Modulated Gap Transistor**
CMOS	**Complementary Metal Oxide Semiconductor**
CVD	**Chemical Vapour Deposition**
DI	**Deionised Water**
ECV	**Electrochemical Capacitance Voltage**
EUV	**Extreme UltraViolet**
FET	**Field-Effect Transistor**
FFT	**Fast Fourier Transform**
FIB	**Focused Ion Beam**
FinFET	**Fin Field-Effect Transistor**
FTIR	**Fourier Transform InfraRed**
GAA	**Gate All Around**
GeOI	**Germanium on insulator**
HRTEM	**High Resolution Transmission Electron Microscopy**
IPA	**Isopropyl alcohol**
ITRS	**International Technology Roadmap for Semiconductors**
MBE	**Molecular Beam Epitaxy**
MLCD	**Monolayer Contact Doping**
MLD	**Monolayer Doping**
MOCVD	**Metal Organic Chemical Vapour Deposition**
MOSFET	**Metal Oxide Semiconductor Field-Effect Transistor**
MOVPE	**Metal Organic Vapour Phase Epitaxy**
NGL	**Next Generation Lithography**
NIST	**National Institute of Standards and Technology**
NMOS	**n-channel MOSFET**

NMR	**Nuclear Magnetic Resonance**
NW	**Nanowire**
PMOS	**p-channel MOSFET**
PV	**Photovoltaic**
RCA	**Radio Corporation of America**
RTA	**Rapid Thermal Anneal**
SAM	**Self Assembled Monolayer**
SEM	**Scanning Electron Microscopy**
SIMS	**Secondary Ion Mass Spectrometry**
SOI	**Silicon on insulator**
TAA	**Triallylarsine**
TEM	**Transmission Electron Microscopy**
TOF-SIMS	**Time-of-flight SIMS**
UHV	**Ultra-high vacuum**
UV	**Ultraviolet**
XPS	**X-ray photoelectron spectroscopy**

Acknowledgments

After a lengthy writing process, I am very relieved to have finally managed to finish up my doctoral thesis. The journey that began in 2011 with my Erasmus over in UCC has come to an end. First and foremost, my thanks to Prof. Justin Holmes for giving me an opportunity to join his group and supervising me during these last years. Even after few years working in industry, I still consider him one of the best managers I have ever had the privilege to work for; extremely down-to-earth, a true lab leader and always ready to challenge and give criticism in order to form the spirit for whatever came after the labwork. I am also forever grateful to Dr. Brenda Long, for bringing me into the MLD world and for helping me in learning unvaluable skills both inside and outside the lab. Never once I was denied a chance to go outside my comfort zone and I was always encouraged to take on new challenges.

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Dedication

Dedicated to my family, my wife, and my son

Chapter 1

Introduction

1.1 Introduction

Materials for electronics play a dominant role in our everyday lives. Silicon, for example, is the foundation of the integrated circuit present in all devices we interact with daily, such as mobile phones, cars, or personal computers. The integrated circuit generates revenue of > $300 billion for the semiconductor industry which, in turn, fuels the > $1.5 trillion global electronics market[1]. Given the massive scale of this market, as devices have reached nanometre scales, where surface or interfacial properties can dominate over the bulk[2], understanding materials properties and surface chemistry is a very important area of study.

This thesis explores novel, non-destructive methods for doping of silicon alternatives, such as germanium and gallium nitride, as well as passivation methods for bismuth, which has potential for future nanoelectronics applications. such as confinement modulated gap transistors (CMGT)[3].

Semiconductor surface chemistry has been studied for several decades, where highly sensitive analytical techniques such as X-ray photoelectron spectroscopy (XPS) or secondary ion mass spectroscopy (SIMS), have enabled an in-depth understanding of the first few nanometers of the surface. With the rapid growth of the semiconductor market, fuelled by device miniaturisation, the number of publications has steadily increased with currently more than 300 publications per year on semiconductor surface chemistry (**Figure 1.1**).

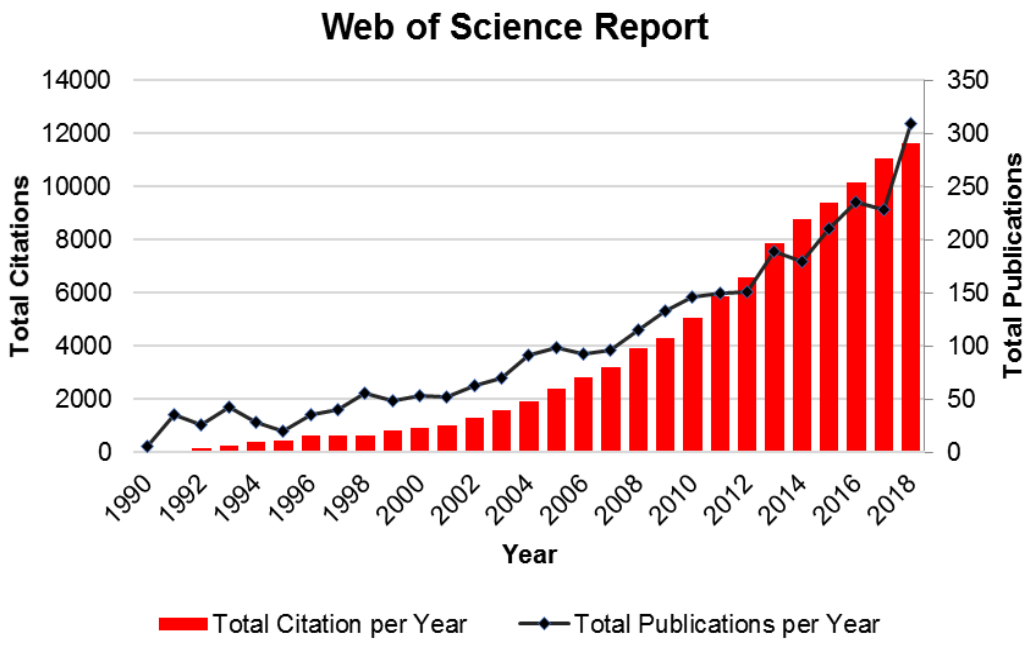


Figure 1.1: *Web of Science Citation Report. Included are the total citations and publications per year with "Surface Chemistry" and "Semiconductor" in the title.*[4]

To a degree, the reactivity of semiconductor surfaces parallels that of its solution-phase equivalents, *e.g.* silanes for Si and germanes for Ge, however, there are many cases where effects from the bulk can influence the reaction outcome[5]. Organic functionalisation of semiconductors is an actively growing field examining the attachment of organic groups to surfaces, both in vacuum and in solution[2]. Functionalisation can then lead to changes in the properties of surfaces which can be exploited in various ways, such as wetting[6], sensing[7], biomolecular applications[8] or nano-patterning[9]. Surface passivation[10] is one of the methods described in this thesis, highlighting the ability of certain classes of molecules to render a surface inert. As mentioned, one of the topics investigated in the research described in this thesis is monolayer doping[11] via organic functionalisation, for electronic applications. The surface chemistry of the semiconductor of choice is exploited in order to graft a

dopant-containing organic molecule which, upon annealing, is decomposed and leads to diffusion of the dopant into the bulk of the material[12].

The reactivity of a semiconductor is partly controlled by the dangling bonds present at its surface, due to the bulk structure being truncated; since the 1950s it has been known that these surfaces undergo reconstruction compared to the bulk[13]. Duke[14,15] has set out principles that describe the reconstruction of tetrahedral semiconductor surfaces, *e.g.* Ge and Si. The first principle describes how the semiconductor surface atoms re-arrange their position to remove any dangling bonds (which in turn would give rise to metallic bands) and revert the surface state to semiconducting to minimise Gibbs energy.[14] This energy minimisation is a trade-off between energy gained by eliminating the dangling bonds with energy lost because of bond strain, resulting from the new configuration. Consequently, both Si and Ge undergo extensive surface reconstruction, *i.e.* the surface atomic geometry differs significantly from that of the bulk[2,15]. This is true for both crystal orientation of Ge, *i.e.* (100) and (111). In the (111) surface the surface atoms retain the same position as the bulk. On the other hand, the (100) surface reconstructs to form germanium dimer pairs, thus reducing the amount of dangling bonds from two to one per surface atom; this leads to buckled dimer pairs in which the up atom is more nucleophilic and down atom is more electrophilic, which in turn affects how the surface behaves towards functionalisation[15,16], as described in detail in **Chapter 3** of this thesis..

The surface functionalisation of GaN was the focus of my research described in **Chapter 4** of this thesis. GaN presents a wurzite structure, with a polar axis that is parallel to the *c*-direction of the crystal lattice. Because of this axis, GaN grown on a heterosubstrate can have two inequivalent orientation, named Ga-face (also known as (0001), *c*) or N-face (also known as (000-1), -*c*) polarities according to the atoms of the Ga-N bilayer that are facing the surface (**Figure 1.2**)[17]. The polarity of the wurzite structure leads to piezoelectric behaviour along the [0001] direction leading to detrimental effects on optoelectronic devices.[18] However the Ga-polar GaN is the most widely used orientation, as it leads to higher quality epitaxial layers with lower dislocation density compared to non-polar layers[19]; due to these differences, the surfaces display different sensitivity towards chemical treatments, as well as different oxidation behaviour.[20]

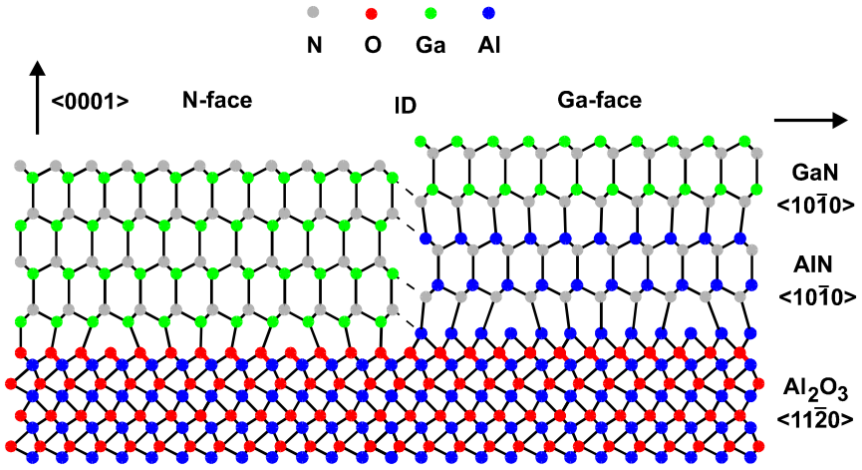


Figure 1.2: *Schematic of a GaN/sapphire interface with (right) or without (left) an AlN buffer layer. This causes polarity inversion*[15].

Chapter 5 describes my research on oxide removal and stabilisation of bismuth thin films. The aim of working with bismuth was to remove the oxide and passivate the surface to enable ambient air handling. Semimetals, such as Bi, present a behaviour that, as the name suggests, is intermediate between a semiconductor and a metal;

depending on structural details or external parameters, *e.g.* materials thickness, the surface can be expected to either turn into a metal or a semiconductor[21]. The latter case is what happens in the case of bismuth, with its surface displaying semiconducting behaviour when reaching a critical thickness and behaving as a two-dimensional material[21]. However, as bismuth readily oxidises when exposed to air, it is necessary to either protect the surface against reoxidation, or remove the insulating oxides in order to restore the metallic behaviour of the thin films.

1.2 Alternative Semiconductor Doping Methods

1.2.1 The Evolution of the Transistor

1.2.1.1 Scaling down Device sizes

The semiconductor industry has been driven since its inception, by what is long since known as Moore's Law[22–24], which states that the density of components, *i.e.* transistors in an integrated circuit doubles roughly every two years (**Figure 1.3)**. However, in recent years, the push from industry has been more targeted towards pushing this scaling by employing more complex architectures, such as nanosheet, forksheet and multi-tiered complimentary FET (CFET) (**Figure 1.4**). As a direct consequence, the size of features is constantly downscaling to accommodate as many transistors as possible per unit area. By industry standards, each generation of the technology node is designated by the gate length. While the first commercially available Intel CPU used in 1971 was manufactured using the 10 µm node process, current Intel household processors are part of the 14 nm node (>700 times smaller), thanks to the development of more advanced fabrication techniques, as well as a better understanding of the behaviour of physics at extremely small scales. Smaller devices

lead to better manufacturing efficiency, lower production costs, reduced power consumption and better performing processors.

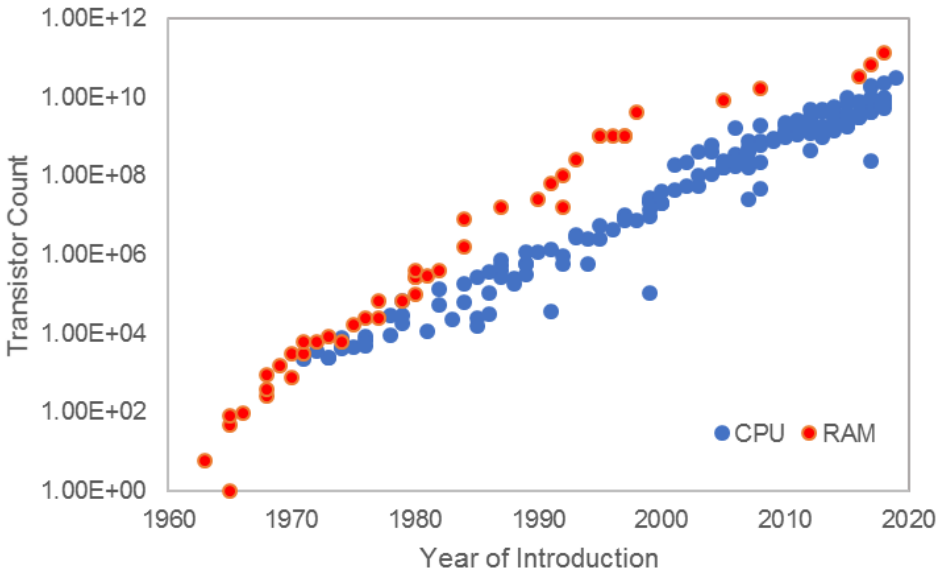


Figure 1.3: *Moore's law showing transistor counts for commercially available processors used for logic CPUs and RAM modules, the two largest segments of the semiconductor market.*[25]

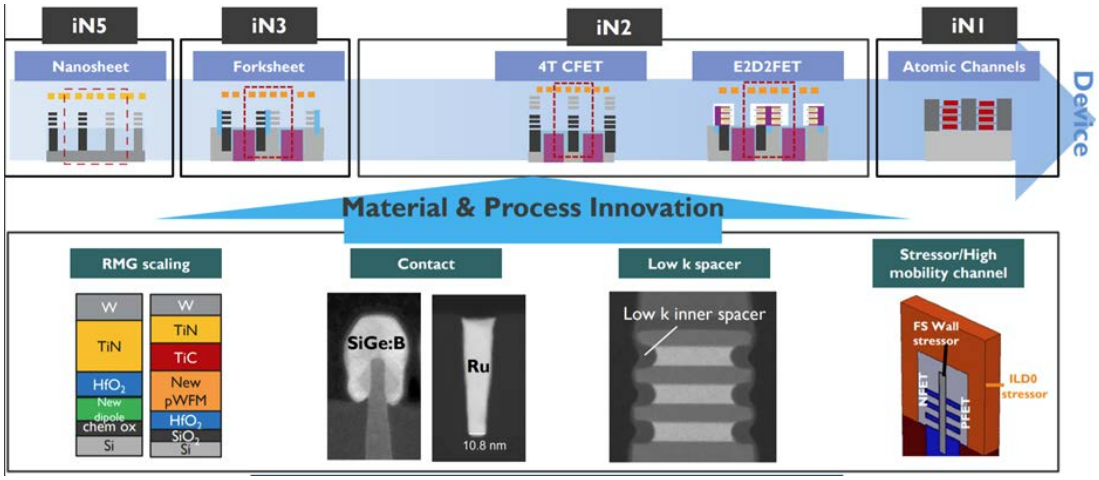


Figure 1.4: *Overview of the IMEC Logic Device technology roadmap; on top are the expected gate architectures for the next technology nodes. On the bottom are illustrate the material and process innovations that can enable the development and integration of the new architectures in the next nodes.*[26]

1.2.1.2 Transistor Fabrication

Although germanium (Ge) was the material of choice for the fabrication of the first ever transistor in 1947, the industry quickly transitioned to silicon (Si) as the material of choice for device fabrication; being the most abundant material in the Earth's crust, its cost is cheaper than all other potential materials, thus leading to cheaper devices despite its mobility being lower than most semiconductors. In addition, its native oxide (silicon dioxide, SiO_2) is an excellent dielectric material due to its exceptional chemical and thermal stability, high dielectric strength and relatively wide band-gap[27]. SiO_2 can be easily thermally grown or deposited on numerous materials[28], thus again keeping the overall device cost down and allowing for efficient production.

Current devices are being fabricated at the industrial level using photolithography, which involves a series of spin coating, baking and UV etching steps, used to transfer a predefined pattern onto the surface of a substrate with the final goal of building an integrated circuit. As the minimum resolvable linewidth is directly dependent on the wavelength of the source used during the etch, etching systems have evolved from using a UV light source at 365 nm, to deep-UV excimer laser exposure systems with wavelengths down to 193 nm, which allow for a minimum feature size of 100 nm. However, it is very challenging to create lasers with wavelengths lower than this as they require vacuum systems and purge equipment to prevent UV absorption from air. To further improve the resolution, the air gap between the focusing lens and the wafer surface was replaced by a liquid medium, thus increasing the resolution due to the different refractive index; immersion lithography allows resolutions down to 22 nm when using 193 nm ArF lasers. As we are currently moving towards the 7 nm node, lower resolutions are required; the current industry standard relies on ArF immersion

lithography, with up to 4 patterning steps used to achieve smaller features. However, this leads to an increase in production costs due to the added processing steps.

Consequently, next-generation lithography techniques (NGL) are being currently investigated, with the aim of replacing immersion photolithography. One of these candidates is e-beam lithography, which is currently being used to produce sub-10 nm features; instead of using light, a beam of electrons is used to directly write patterns into the resist, with the wavelength being adjusted by changing the energy (kV) of the incident beam. Thus, control over the generation of secondary and back scattered electrons is possible. Their lateral spread and interaction with the resist determine the resolution of the technique. However, the main drawback to this technique is that the patterning process is serial and not parallel, respectively, thus leading to very low throughput. This, together with its very prohibitive cost, makes EBL unviable for patterning on an industrial scale. Another candidate being actively explored by manufacturers is extreme ultraviolet (EUV) lithography, which allows for below 20 nm resolution in a conventional lithography setup; however, this comes at about a quarter of the throughput of immersion lithography tools, as well as stochastic printing failures[29], which increases the number of defects on the patterned substrate, and the steep cost of the equipment.

With device size scaling down and new architecture designs being considered, such as free-standing nanowires and nanosheets, the relatively low carrier mobility of silicon is becoming increasingly more problematic. At sub-10 nm dimensions, scattering effects become more dominant, leading to higher power consumptions therefore higher mobility materials are required to compensate for this[30].

Different enablers (**Figure 1.5**) have been implemented as industry standards in order to mitigate these issues; high-k dielectrics, such as HfO_2, have long been used as substitutes of SiO_2 in order to better control the current flow by the gate using a thicker gate oxide layer. Different substrate materials, such as Ge, SiGe or III-V compounds, *e.g.* AlGaN, InGaAs, are also being slowly integrated as Si-channel substitutes due to their higher carrier mobilities, which leads to lower power consumption to achieve the same electrical performance of their Si counterparts. From an architecture perspective, devices have transitioned from planar designs to three dimensional geometries, such as Fin Field Effect Transistors (FinFETs), with gate-all-around (GAA) FETs being explored as next-generation solutions.

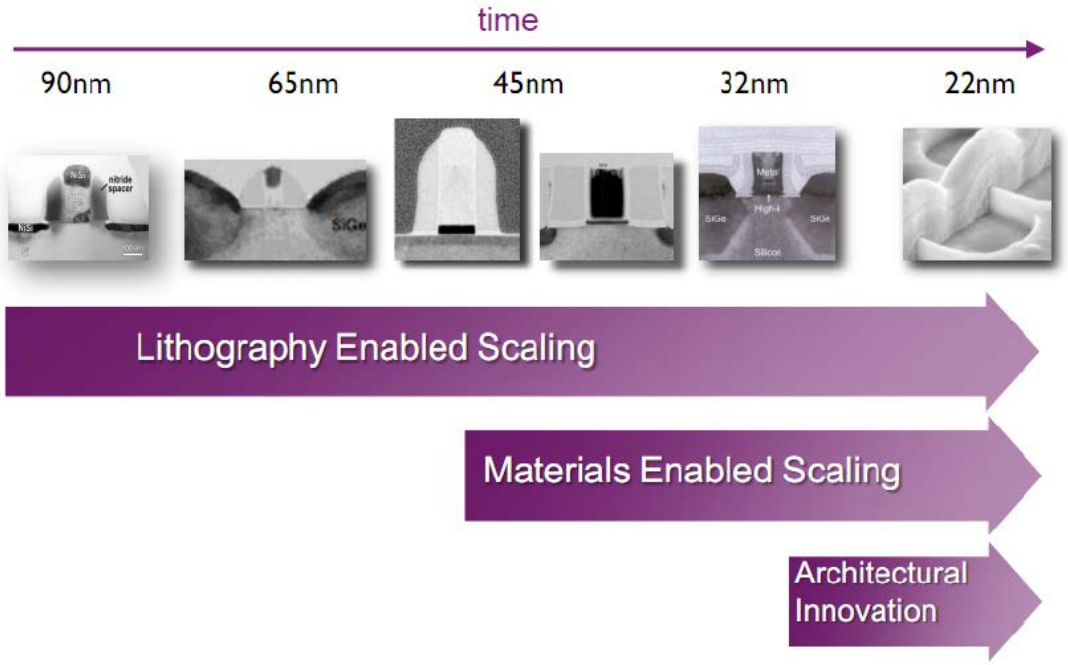


Figure 1.5: *Schematic showing how the device scaling has been allowed to progress over time. At first, the lithography process was enough to scale down to roughly 45 nm gate length. Following that, higher-k material such as HfO_2 allowed further scaling of dimensions by substituting SiO_2 and, recently, architectural innovation in the form of FinFET, GAA FETs and CFET, allowing the scaling and increase in transistor density to continue.*[31]

As in 3D architectures the gate encircles the transistor on different sides, it is possible to control the short channel effects more efficiently than traditional MOSFETs and reduce the drain currents at small sizes[32,33]. To confine the current at the semiconductor-dielectric interface and thus allow better current control, devices require ultra-shallow junctions with very sharp dopant depth profiles. Ideally, the dopant employed should have (i) low diffusivity to allow for better junction control as dimensions are reaching a limit and architecture complexity increases and (ii) high solid solubility in order to get high dopant concentrations.[34]

Doping is the intentional introduction of impurities inside a semiconductor to modulate its electrical properties by substituting atoms in the lattice. Two different types of impurities can be used for this purpose: acceptors (or p-dopants), or donors (or n-dopants). Acceptor atoms have fewer valence electrons than the target semiconductor. When introduced into the host lattice they leave a 'hole' which can carry current as it travels around the lattice. In a similar fashion, donor atoms have more valence electron than the target semiconductor. When introduced into the lattice, extra electrons are be liberated from the matrix and are free to move around. Electrons and holes are known as charge carriers.

The current industry standard technique used for semiconductor doping is ion implantation, due to its high adaptability and low cost compared to other methods such as epitaxy, MOCVD[35] or plasma doping[36]. Ion implantation relies on accelerating ions of one element into a solid target. However, there are major drawbacks when using ion doping on nanoscale structures, such as lack of depth control, shadowing effects and random dopant distribution[37]. In addition, the high-energy beam employed causes crystal damage to the irradiated substrate; while defects can be annealed out in planar devices, for sub-10 nm tri-dimensional structures, this process leads to irreversible

amorphisation and, as a consequence, to poor electrical performance[38]. The chemical doping methods herein discussed below in this Chapter have proven successful in the non-destructive and conformal doping tri-dimensional nanoscale structures, unlike more established techniques such as ion implantation.

1.2.2 State-of-the-Art in MLD

Current doping techniques are becoming less suitable for sub-10 nm structures, due to irreversible substrate amorphisation and non-conformality, both proving to be problematic for the final electrical characteristics of the devices. Monolayer doping (MLD) is a potential substitute technique to more conventional methods.

First used on Si substrates by Ho *et al.*[11] in 2008 (see **Figure 1.6**), MLD it comprises of two main steps: (i) functionalisation of the semiconductor with a dopant containing molecule and (ii) diffusion of the dopant atoms into the semiconductor *via* an annealing step. Surface functionalisation is usually achieved through a reduction reaction between a hydrogen-terminated semiconductor surface and a labile C=C site on the dopant containing molecule[11,12]. Therefore, numerous aspects of the MLD process, such as surface termination, choice of molecule, capping layer or annealing parameters, can be tailored and optimised according to the required application of the material. The MLD process is, as such, very simple and straightforward; in its simplest form, it can be carried out in a research lab setting on a gas-vacuum manifold where substrate re-oxidation can be minimised prior to its functionalisation. The process can also be easily scaled up to 300mm wafer level[39] and has been successfully applied to

nanowires and other nanostructures with the formation of sub-5 nm junctions[12,40] using both *p*-[11,41–43] and *n*-dopants.[44–46]

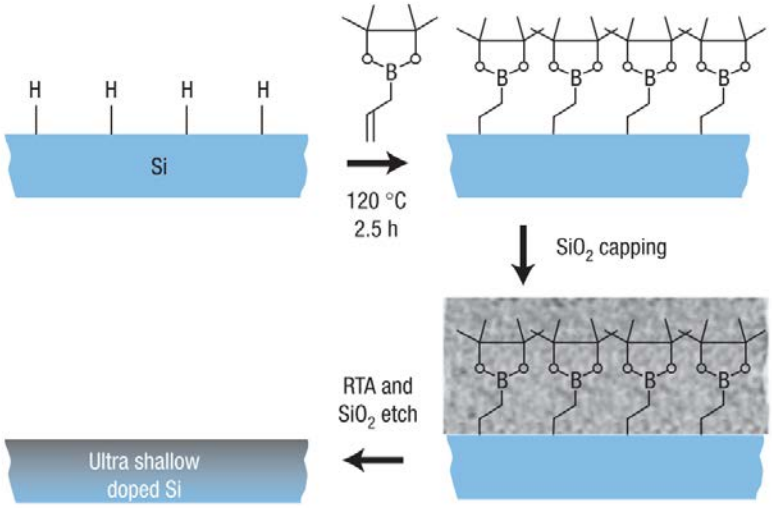


Figure 1.6: *Schematic of the MLD process described by Ho et al.[12] using allylboronic acid pinacol ester on a Si surface.*

1.2.2.1 Monolayer Doping of Group IV Materials

Ho *et al.*[12] used allylboronic acid pinacol ester (ABAPE) in mesitylene to dope a Si:H wafer with boron. A standard rapid-thermal-annealing recipe, with temperatures ranging between 950 – 1000 °C for 5 seconds, was used to drive in and activate the dopant. The B content of the samples was measured using Secondary Ion Mass Spectroscopy (SIMS) which showed a B peak carrier concentration of 5×10^{20} at/cm^3, with the smallest junction depth achieved of 18 nm (see **Figure 1.7**). In the same study, the MLD process was also applied to CVD grown nanowires with metal contacts, which showed lowered resistance, and to silicon-on-insulator (SOI) substrates containing fabricated FETs[12]. This study laid the foundation to further research on MLD, with many parameters, such as substrate choice, molecular footprints, dopant

variation, thermal annealing parameters and impurity incorporation being investigated.

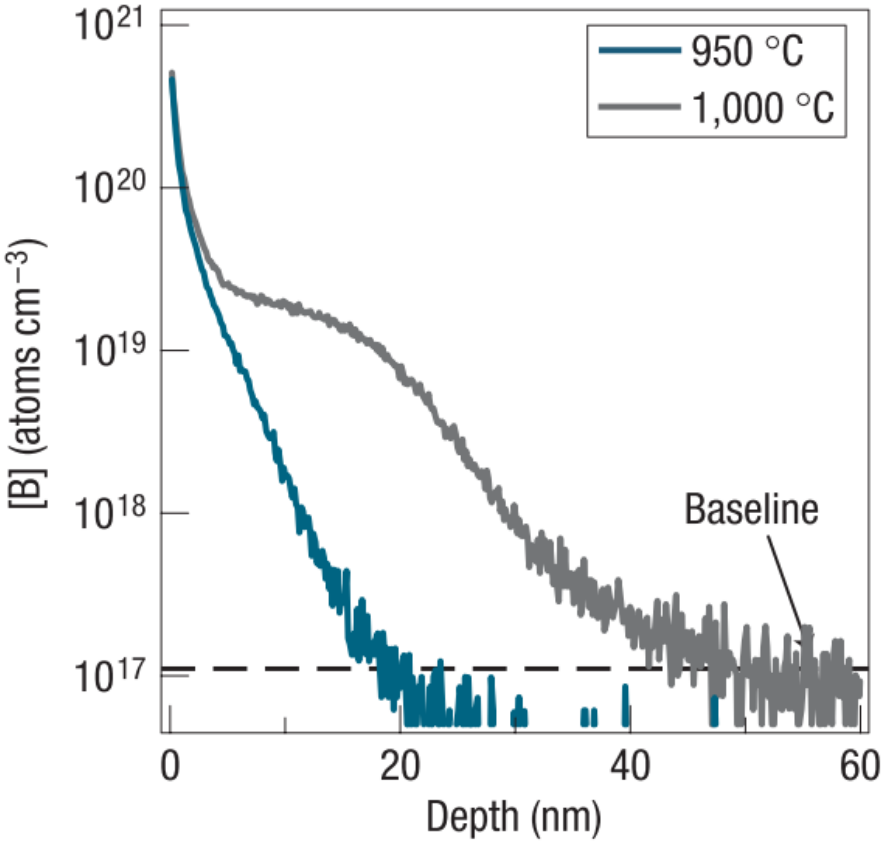


Figure 1.7: *SIMS profile of B-MLD doped Si with 5 s annealing at 950 and 1000 °C.*[12]

Further studies from Ho *et al.*[12] proceeded to apply the same method to 4" wafers using spike annealing and phosphorus and boron-based dopant precursors, where peak carrier concentrations of up to 5.5×10^{20} at/cm^3 were observed, exceeding the solid solubility limit of P in Si. Moreover, a junction depth of 2 nm was achieved for the B doped samples. The effect of C on the final electrical properties was also investigated and the leakage currents were found to be lower than the then state-of-the-art junction leakage currents[47]. Subsequently, Ang *et al.*[39] used the MLD approach of Ho *et al.* to conformally doped a silicon wafer with a phosphorous-based precursor; the SIMS

measurement of the samples post-MLD showed a peak P carrier concentration of 1×10^{22} at/cm^3, with a junction abruptness of 0.6 nm/dec. By comparison, ion implanted samples showed an 11 nm/dec slope whereas in-situ doped samples had a 4.5 nm/dec slope (**Figure 1.8)** therefore proving how MLD can be an effective doping technique when it comes to high concentration/low junction depths. The same process was then applied to a FinFET with a 20 nm width; the data showed that it was possible to maintain a defect-free fin even after processing, which makes MLD a more suitable doping alternative when compared to ion implantation.

A variation of the traditional MLD process, named monolayer contact doping (MLCD) was reported by Hazut *et al.*[40,48], where the dopant containing monolayer was formed not directly on the substrate of choice, but rather on a "donor" substrate which was then brought into contact with the target to be doped (**Figure 1.9**). The two substrates were then annealed together, resulting in the diffusion of the dopant from the donor to the target substrate. Compared to traditional MLD, this method does not require any capping layer and used phosphine-oxide based molecules bound onto a SiO_2 substrate. MLCD is more advantageous than traditional methods as fewer processing steps are needed. The same method was also employed to modify undoped silicon nanowires into parallel p-n junctions using a one-step MLCD process[49]. More recently Ye *at al.*[50] used silane chemistry to bind a boron containing molecule to an SiO_2 donor substrate which could be used to dope multiple substrates.

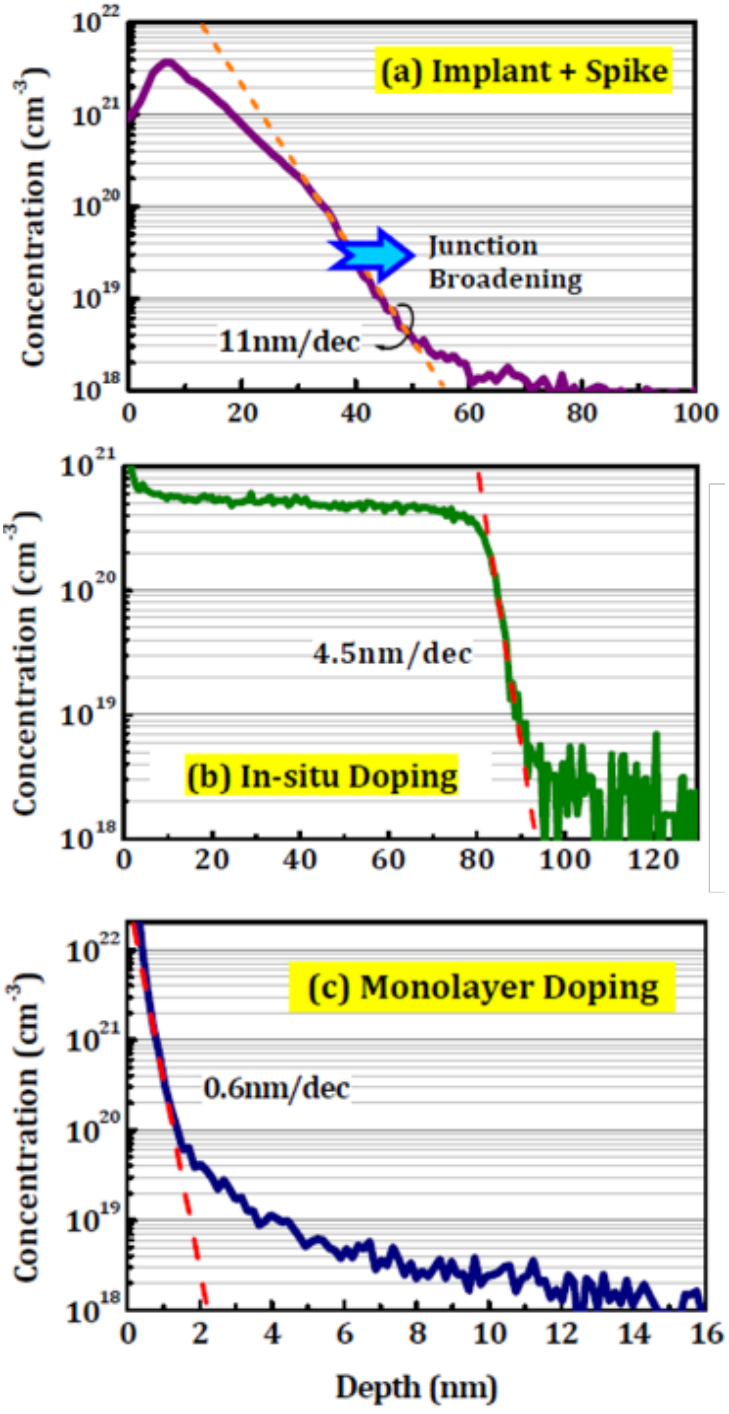


Figure 1.8: *SIMS analysis of (a) ion implanted, (b) in-situ doped and (c) MLD doped samples, highlighting the steep junction abruptness which will be critical in enabling pitch scaling.*[39]

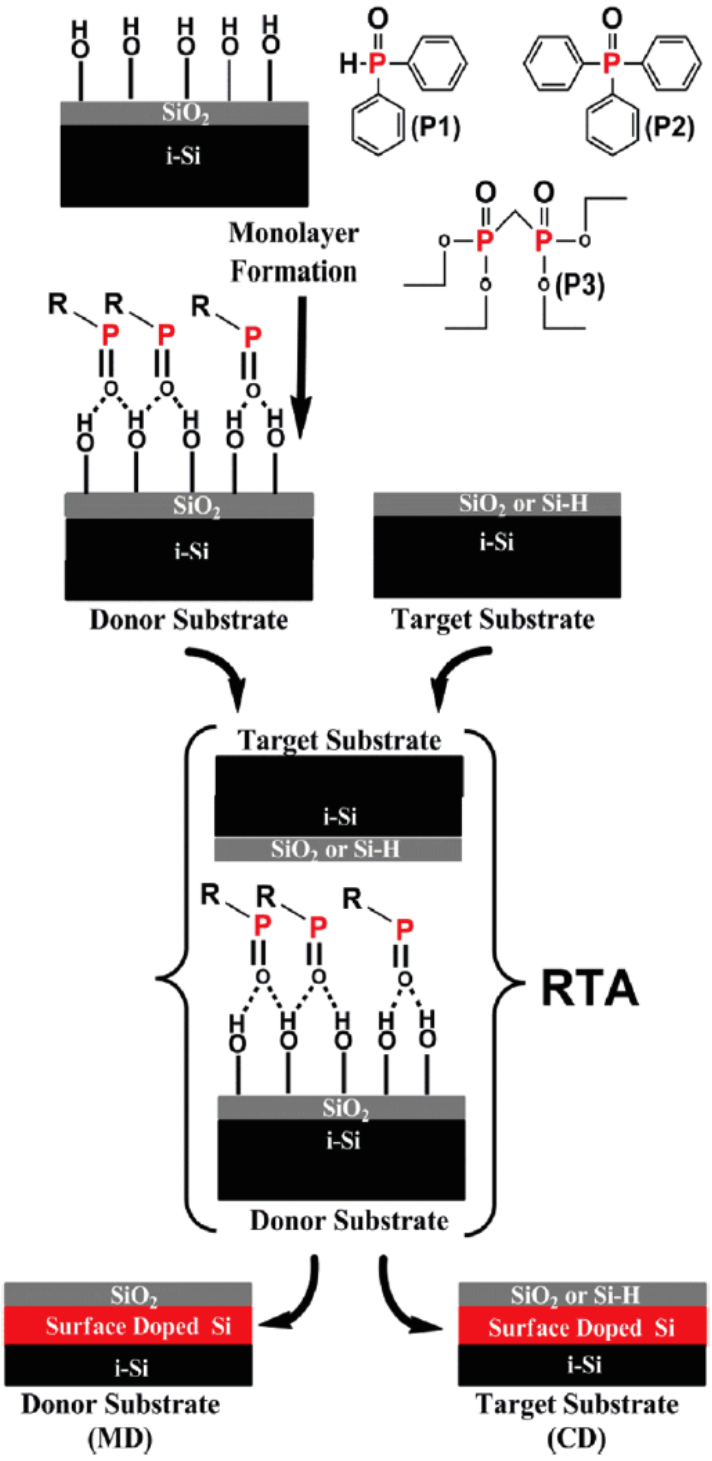


Figure 1.9: *Monolayer contact doping (MLCD) schematic: a monolayer containing dopant atoms is formed on a donor substrate. The donor and target substrates are brought into contact and annealed using rapid thermal anneal (RTA). During the annealing dopant atoms diffuse into both donor and target substrates.*[48]

While the first MLD studies all relied on B- and P-containing molecules with short anneal times to reduce diffusion and form shallow junctions, subsequently different dopant atoms have been employed. Guan and co-workers[46] used MLD to introduced N into Si, a dopant with a low thermal diffusion coefficient, by employing a standard hydrosilylation reaction. Despite the negligible electrical activity of N in Si, the study clearly showed how the thermal diffusion coefficient does impact the junction depth without affecting other parameters; in their paper, a peak carrier concentration of 4×10^{19} at/cm^3 was achieved for N, with a junction depth of ca. 50 nm, compared with 100 nm obtained for a P doped sample (**Figure 1.10**). The activation rates and diffusion coefficients were also found to be in line with literature values.

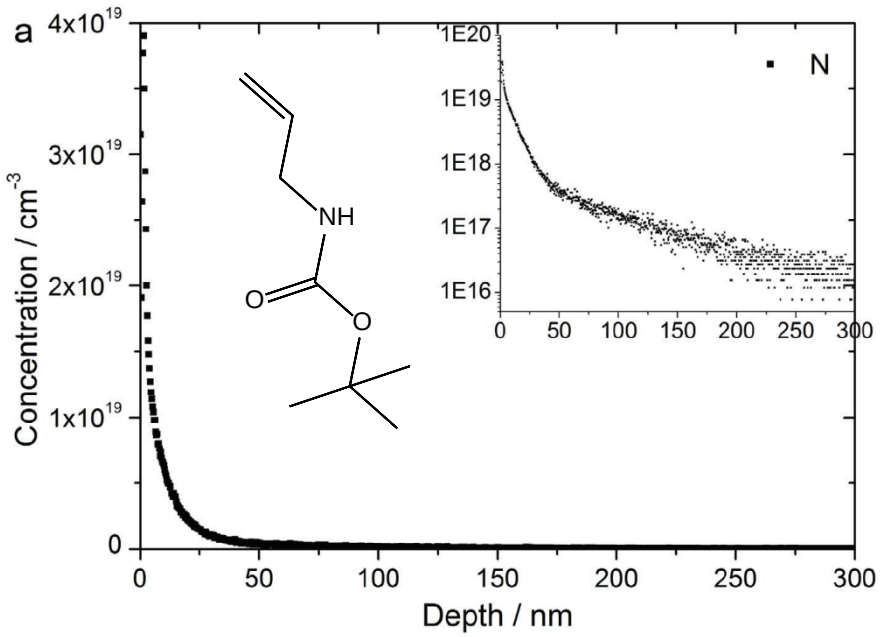


Figure 1.10: *SIMS profile from a N-MLD doped Si sample. Inset shows the SIMS data in the log scale.*[46]

O'Connell *et al.*[45] published the first application of As-based MLD on bulk silicon and on nanowire devices. A standard hydrosilylation reaction was used to bind the As

precursor to a Si:H surface; the samples were then capped and annealed using RTA. A peak carrier concentration of up to 2×10^{20} at/cm^3 was achieved, with the shallowest junction depth of 75 nm; from the diffusivity data, an extrinsic diffusion regime was observed (see **Figure 1.11**), where the dopant concentration was above the intrinsic carrier concentration and the diffusion coefficient became concentration dependent. The doped nanowire devices displayed a significant reduction in resistivity and transmission electron microscopy data showed that the devices remained highly crystallinity, with no crystal damage, after the MLD process.

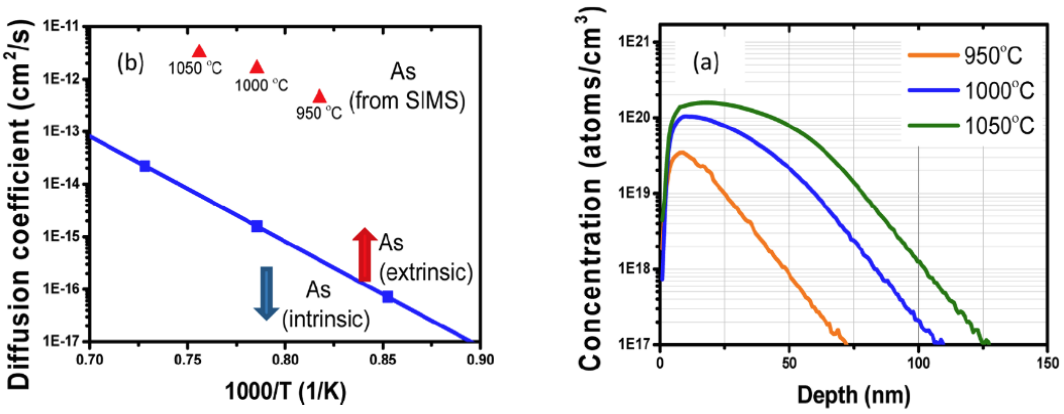


Figure 1.11: *Data for As-MLD doped samples. (a) SIMS profiles of three samples processed at varying temperatures for 5 s. (b) Diffusivity data extracted from SIMS analysis. As can be seen in the measured data in red, the samples exhibit diffusivity in the extrinsic regime as the diffusion coefficient is concentration dependent.*[45]

1.2.2.2 Monolayer Doping of Group III-V Materials

III-V materials can be doped by introducing substitutional impurities into their lattice. However, unlike group IV semiconductors, a much wider range of dopants can be used, *e.g.* group II elements can be used as acceptors and group VI elements can be used as donors. In addition, isoelectric doping can be carried out by substituting either the group III or the group V parts of the compound with other group III/V elements.

Lastly, group IV elements can be used to obtain amphoteric doping, as they can potentially be either donor or acceptors[51]. Given the challenging and relatively unexplored surface chemistry of III-V materials, when compared to group IV materials, the application of MLD has been quite limited. The first report of MLD performed on group III-V substrates was by Ho *et al.*[52] in 2009 on InAs. Exploiting the well-known ammonium sulphide cleaning procedure widely used on InAs, they were able to form a perfect sulphur monolayer on the substrate surface. They then employed the well-established MLD procedure of capping and annealing to in-diffuse this dopant, achieving a maximum electrically active concentration of *ca.* 8×10^{18} at/cm^3 for S, which is still the highest active sulphur concentration reported in literature to date[53].

In a similar fashion, Cho *et al.*[54] first performed sulphur MLD on InP nanopillars (see **Figure 1.12**). The organic layer was capped and annealed in a tube furnace at 650 °C for 15 minutes. An ultra-shallow conformal junction depth of *ca*. 10 nm was formed, with a peak chemical concentration of above 10^{21} at/cm^3 and an electrically active S concentration of of 10^{19} - 10^{20} at/cm^3, estimated by Hall effect measurements.

Following this, research has moved towards InGaAs; the first application of solution-based sulphur MLD on this material was performed by Yum *et al.*[55]; the surface functionalisation was again performed using ammonium sulphide, obtaining ultra-shallow junctions and active carrier concentrations of 4.9×10^{19} at/cm^3. The study also showed that sulphur MLD is sensitive to capping conditions, such as the growth temperature and the capping precursor reaction energy at the surface and concluded that a SiNx/BeO bilayer structure as a capping layer should lead to higher activation efficiencies resulting in better performing III-V devices. Further studies explored the use of phosphorous pentasulfide (P_2S_5) as an additive to the ammonium sulphide

solution in order to enhance the quality of the surface coverage with the aim of increasing the maximum dose[56]; SIMS was used to calculate a maximum dose of *ca.* 7×10^{14} at/cm^2 for the ammonium sulphide solution with the P_2S_5 additive versus *ca.* 2×10^{14} at/cm^2 for the solution without the additive. Sulphur-MLD was scaled up and applied to 300 mm wafers, where shallow junction and dopant activations were found to be in line with previous results on coupons[57]. This study also incorporated advanced annealing techniques such as laser or flash lamp annealing, which showed that they might lead to better dopant activation efficiencies.

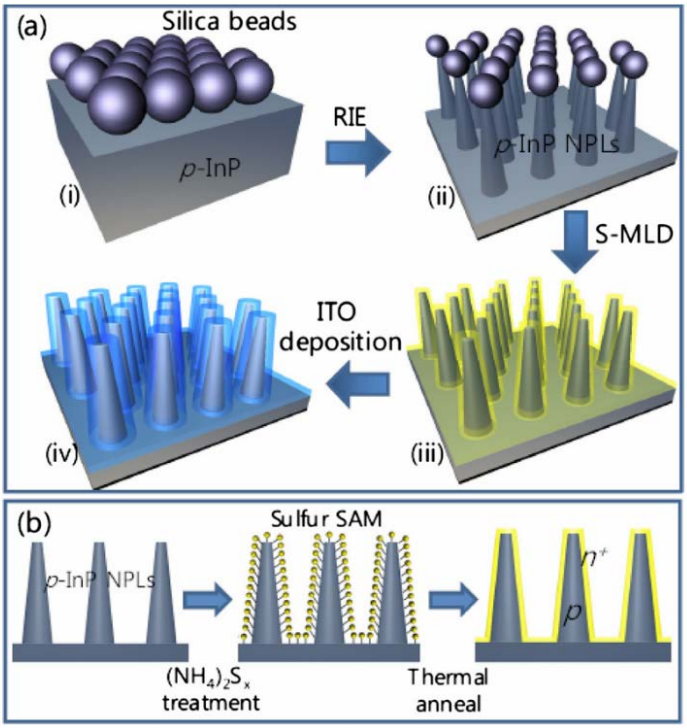


Figure 1.12: *Schematics showing (a) the fabrication process for producing InP NPL solar cells and (b) the S-MLD process as reported by Cho et al.*[54]

Recently Kong *et al.*[58] employed MOCVD to deposit silane monolayers on InGaAs substrates which were subsequently capped and laser annealed, achieving dopant concentrations of up to 5×10^{20} at/cm^3 with depths of *ca.* 10 nm.

More in line with typical liquid-phase MLD procedures, O'Connell *et al.*[59] reported the first instance of Si/S and Sn doping of InGaAs using organometallic molecules (**Figure 1.13**). A mercaptosilane molecule was used to demonstrate the feasibility of Si/S co-doping using liquid-phase surface chemistry. Junction depths of *ca*. 50 nm were achieved but, due to the amphoteric dopant nature of Si and the simultaneous presence of both Si and S, it was not possible to characterise the active dopant concentration of these samples. The peak chemical concentration of S and Si were *ca*. 1×10^{20} at/cm^3 and ca. 1×10^{19} at/cm^3, respectively. In the Sn-MLD process, allyltributylstannane was reacted with the H-terminated surface of InGaAs substrates through the labile C=C site. In this study junction depths of *ca*. 75 nm were obtained with doping concentrations of *ca*. 1×10^{20} at/cm^3. The large junction depth suggests that more advanced annealing techniques are needed to obtain shallow doping.

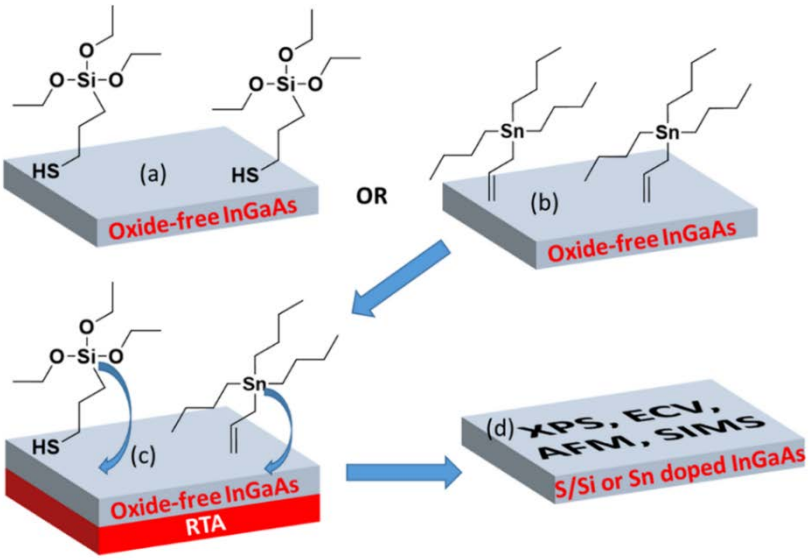


Figure 1.13: *General schematic for the InGaAs MLD process reported by O'Connell et al.*[59]*. The Si/S or Sn precursors were used to functionalise the surface. After capping and annealing, the dopants diffuse in the substrate, leading to doped InGaAs surfaces.*

1.2.3 Alternative Materials to Silicon

1.2.3.1 Germanium

1.2.3.1.1 Overview of Germanium

Germanium (Ge) has been presented as a viable substitute material for silicon (Si). Being another group IV semiconductor, Ge and Si share many properties, such as its diamond cubic crystal structure, and its CMOS (complementary metal oxide semiconductor) compatibility would allow for its incorporation into already established production lines without requiring any alterations. From an electronic perspective when compared to Si, Ge has a mobility enhancement 4 times higher for holes (from 450 cm^2/Vs for Si to 1900 cm^2/Vs for Ge) and 2 times higher for electrons (from 1500 cm^2/Vs for Si to 3900 cm^2/Vs for Ge) [60]. These enhanced mobilities would contribute to the lowering of power consumption and leakage currents in devices fabricated using Ge when compared to their Si-channel counterparts (see **Table 1.1**).

Table1.1: *A comparison of the characteristic properties of Si, Ge and GaN.*[23,60,61]

Semiconductor		**Silicon**	**Germanium**	**GaN**
Characteristic	**Unit**			
Bandgap	**eV**	1.1	0.66	3.49
Electron Mobility (300K)	**cm^2/Vs**	1500	3900	1000-2000
Hole Mobility (300K)	**cm^2/Vs**	450	1900	350
Critical Breakdown Field	**MV/cm**	0.3	1	3
Thermal Conductivity	**W/cm·K**	1.5	0.6	>1.5
Relative dielectric constant	**ε_t**	11.8	16.2	9

1.2.3.1.2 Germanium Oxides

One of the reasons that Si and not Ge is still used as the material of choice for transistors is due to the native oxides Ge. Ge exhibits a complex oxidation environment at the surface which makes it problematic as a gate dielectric. Germanium can form +1, +2, +3 and +4 oxidation states, with the +4 (GeO_2) oxide, being the most stable and the full range of suboxides (*i.e.* GeO_x) forming already at room temperature when exposed to O_2.[62] GeO_2 is water soluble and upon annealing above 250 °C readily converted to Ge. GeO is thermally stable up to 420 °C, at which point it evaporates and acts as a reducing gas which negatively affects the electrical properties of the material[63–65]. This complex oxide behaviour makes surface handling and passivation of Ge substrates a challenging matter when compared to Si. HF and HCl have been shown to successful remove the GeO_2 but have little impact on GeO[66]. These two treatments leave the surface H- and Cl- terminated respectively; although the surface integrity is largely maintained, these surfaces are only stable for few minutes[67]. In order to remove the suboxide, HBr or an HF/HCl mix must be used[66]; in this case the Br-terminated surface (when treated with HBr) is more stable than its H- and Cl-terminated counterparts and can remain completely oxide free for up to 6 hours[68].

1.2.3.1.3 Functionalisation of Germanium

Like Si, the surface of Ge can be readily functionalised with organic molecules in solution and under vacuum; three main methods of wet chemical functionalisation have been studied for Ge: (i) Grignard reactions, (ii) alkanethiol reactions and (iii) hydrogermylation reactions[16] (see **Figure 1.14**). Grignard reactions have been performed on chlorine-terminated surfaces that are reacted with an alkyl Grignard reagent; different length alkyl chains, as well as phenyl and alkenyl groups, were

attached to the surface. The functionalised surfaces showed promise in terms of stability, with no change in the XPS spectra after up to 5 days in air[69,70].

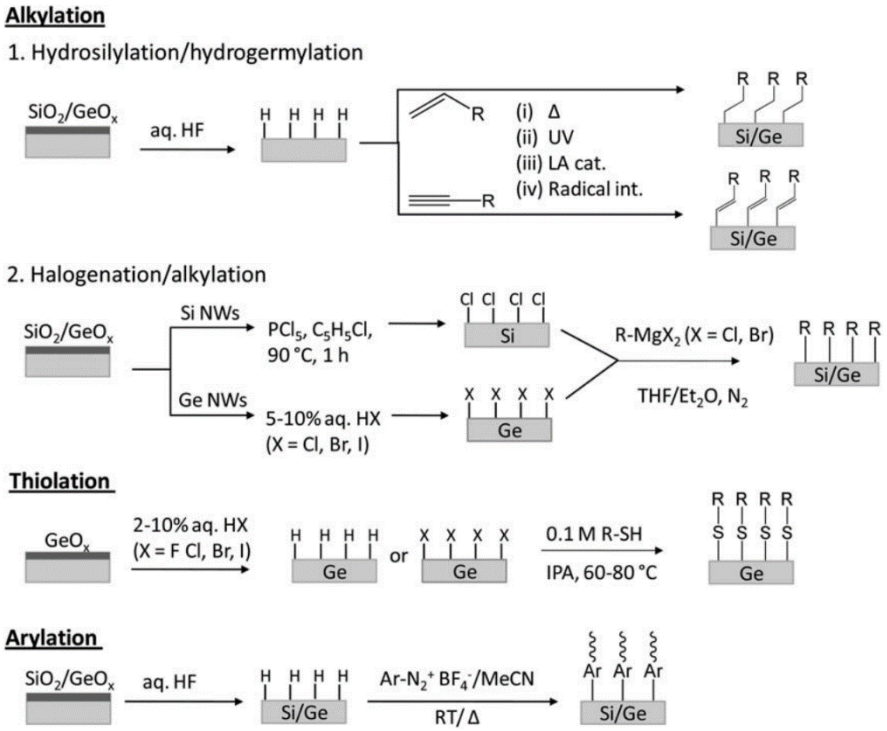


Figure 1.14: *Schematic illustrating the various functionalisation reactions that can be carried out on Si and Ge surfaces.*[71]

A Ge-S bond can be formed by reacting 1-alkanethiols with either hydrogen or chlorine-terminated Ge surfaces[72]. Well-ordered arrays of self-assembled monolayers (SAMs) have been formed on Ge substrates using alkanethiols[10,72–75] of various chain lengths, resulting in complete surface coverage and no germanium oxide formation after exposure to ambient air for 24 hours[73]. Alkanethiol monolayer were however, found to be less stable than their alkyl counterparts, due to the more labile Ge-S bond compared to the Ge-C bond. Atmospheric water tends to attack the Ge surface, breaking the Ge-S bond, ultimately leading to the desorption of the monolayer[74]. Similarly ethyl disulphide and 1,8-naphtalene disulphide have been used to passivate Ge surfaces for up to 12 hours through the formation of Ge-S bonds[76].

In the hydrogermylation of Ge surfaces, an unsaturated C-C bond (alkene or alkyne) is reacted with Ge-X (X= H, Cl, Br) forming a Ge-C bond. Choi and Buriak[67] first demonstrated hydrogermylation on hydrogen-terminated Ge (100) surfaces. Three approaches were used to carry out the reaction: i) Lewis acid mediation, ii) thermal activation and iii) UV light. The Lewis acid mediated reaction used ethylaluminium dichloride ($EtAlCl_2$) leads to formation of alkenyl and alkyl monolayers after 1 and 12 hours respectively[67]. The Lewis acid approach is potentially more advantageous than the Grignard route, which usually requires more than 12 hours at elevated temperatures to complete the reaction[70]. Thermally induced hydrogermylation is the more commonly used approach for Ge functionalisation and has been successfully employed with different alkenes and alkynes[10,67,71,77,78]. Whilst UV-light induced hydrogermylation has not been studied as extensively as the other methods, it has been successfully employed using 1-hexadecene[67] and a 254 nm wavelength light source. An issue with using UV sources is that they readily oxidise oxygen to ozone, which rapidly corrode Ge surfaces to GeO_2[79]. Extreme care must be taken when carrying out reactions to remove any O_2 present. Like the surfaces alkylated via Grignard reagents, hydrogermylated surfaces show excellent stability, albeit dependent on the reaction route used. Overall, thermally-induced hydrogermylation surfaces appears to be more stable those produced by Lewis acid-mediated routes, giving well-ordered monolayers that are stable even in boiling solvents[67]. **Chapter 3** of this thesis describes a UV-induced hydrogermylation approach to react triallyl arsine and allyldiphenylphosphine oxide with the surface of Ge wafers for MLD.

1.2.3.2 Gallium Nitride

1.2.3.2.1 Overview of GaN

Group III-nitride materials are well established in every-day life as blue light-emitting diodes (LEDs) that, when coupled with phosphorus to obtain white light, can be found in mobile phone displays or as energy-saving light sources[80,81]. The compound has a wurtzite crystal structure with a wide band gap of 3.4 eV and a melting point of above 2500 °C. GaN is typically grown using molecular beam epitaxy (MBE)[82] or metal organic vapour physical epitaxy (MOVPE)[83].

1.2.3.2.2 Preparation of GaN

In MOVPE, trimethylgallium and ammonia are typically used as Ga and nitrogen sources respectively. The MOVPE process involves the high-temperature nitridation of a substrate, *e.g.* sapphire, with ammonia, the low-temperature deposition of a thin buffer nucleation layer, *e.g.* aluminium nitride, followed by the high-temperature growth of GaN. High temperature growth increases the mobility of the adsorbed adatoms which in turn leads to the formation of highly crystalline films[83–85]. The buffer layer significantly improves the electrical and optical properties of GaN by supplying nucleation centres with the same orientation as the substrate; these in turn reduce the amount of dislocations arising from the lattice mismatch between GaN and the substrate[86].

1.2.3.2.3 Properties of GaN

While the electron and hole mobilities of intrinsic GaN are slightly lower than Si[61], when GaN is combined with other materials, *e.g.* Al to form AlGaN for high electron mobility transistors (HEMT), GaN outperforms Si, particularly for applications that

require both high power and high frequency handling[87]. Moreover the wide bandgap and high thermal stability of GaN (see **Table 1.1**), make it a perfect material for high-temperature operations[88]. The main issue which hinders the quality of the GaN and other III-nitride materials, is the lack of a low-cost substrate. Even though free-standing GaN and AlN substrates do exist, they are very expensive, only available in small sizes and contain impurities that reduce the transparency of visible light. For this reason, heteroepitaxy is widely employed, whereby template substrates, such as sapphire or silicon carbide, which have a relatively low lattice mismatch with GaN, 14.8 and 3.3 % respectively, are used. These substrates are very expensive and drive up the final device cost, thus making GaN-based electronics, at the moment, only viable for specialised applications, *i.e.* radar systems, space electronics, broadband satellites[88].

1.2.3.2.4 Functionalisation of GaN

Ambient exposure of clean GaN surfaces leads to the growth of a native Ga_2O_3 self-passivating phase[89], with a thickness of only a few monolayers[90], which can be easily hydroxylated by piranha solution[91,92]. GaN has a natural chemical stability that requires very extreme pH environments to induce oxide etching[20], which is usually carried out using molten NaOH[93], KOH[94], phosphoric acid[95], sulfuric acid[96] and oxalic acid[97].

While organic wet chemical functionalisation of group IV semiconductors is a very well established field (as Buriak's[5] and Bent's[16] reviews show), there are relatively few methods for modifying bulk and nanostructured GaN surfaces both in vacuum[98–100] and under ambient conditions[101–104]. Wet chemical functionalisation is the most commercially viable option, as it uses cheaper equipment when compared to UHV

conditions. Based on the structure of the molecule being used for functionalisation, different surface preparations are required. For example, thiol attachment requires complete removal of the oxides present on the surface to ensure binding to the available Ga sites[105], whereas phosphonic acid linkages require the presence of oxygen atoms in order to form a bond between the phosphonic acid groups and the surface[103]. Similarly to this, silanisation of GaN relies on the presence of hydroxyl groups on the surface to successfully form an organosilane layer[91,106], whereas Grignard reactions rely on chlorinated surfaces, similar to their Ge counterparts[94]. As previously discussed, oxide cleaning requires relatively harsh conditions which might make this step non-viable from an industrial standpoint. Therefore, silanisation or phosphonic acid-based methods might prove to be more successful as they do not require complete oxide removal, making these approaches more scalable (see **Figure 1.15**). In general all methods lead to organic functionalised surfaces which are stable in aqueous solutions for periods ranging from 1 week[103,104] to 20 days[107]. **Chapter 4** of this thesis explores the use of siloxanes to functionalise a pristine GaN surface. As an MLD proof of concept, the functionalised surfaces were capped and annealed, and it was shown that Si diffusion and activation is possible for GaN.

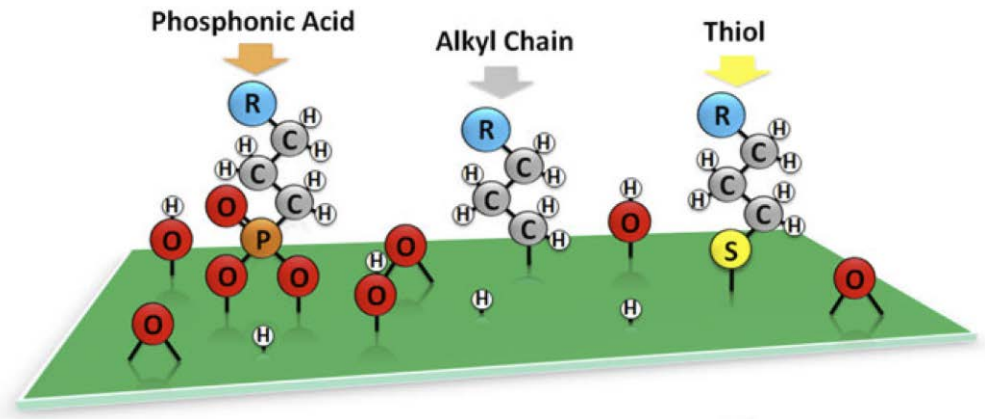


Figure 1.15: *Difference in the possible binding topologies for some of the common possible adsorbates on GaN surfaces.*[20]

1.3. Oxide Removal and Surface Passivation of MBE Grown Bismuth Thin Films

1.3.1 Potential of Bismuth

Bismuth is a group V semimetal which has attracted attention due to its interesting electronic properties, arising from its high electron mobility, low effective mass and high anisotropy of the Fermi level[108]; the low effective mass and long carrier mean free path also lead to high magnetoresistance[109–111]. Even more interesting are the changes in properties that Bi thin-films exhibit once the film approaches a critical thickness. The electrons in bismuth have unusually long mean free paths, ranging from a few nanometers at room temperature to millimeter range when cooled with liquid helium[112]. This, together with the large Fermi wavelength of the carriers, leads to effects of quantum confinement observable in both 2D films and in nanowires which give rise to semimetal-to-semiconductor transitions[21,113–116]. This feature can be exploited to form a semiconducting channel between the semi-metallic source and drain regions, in what is defined as a confinement modulated gap transistor (CMGT)[117]; thus virtually eliminating the need to dope the nanostructure. A theoretical study published by Ansari *et al.*[118], reported that a Schottky junction can indeed be formed in a semimetal nanowire, *e.g.* bismuth. Gity *et al.*[3,119] proceeded to fabricate a working hetero-dimensional rectifier, consisting of a thicker three dimensional (3D) semi-metallic region abutting a thinner two dimensional (2D) semiconducting region, without the need to dope the structure to achieve near ideal diode behaviour (see **Figure 1.16**).

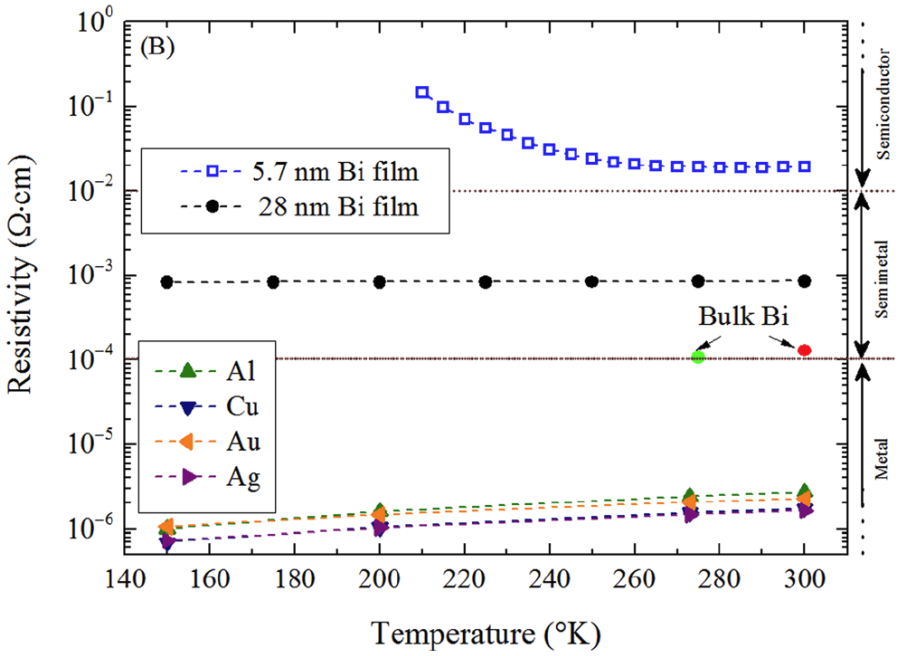


Figure 1.16: *Resistivity of Bi thin films measured at different temperatures, as reported by Gity et al.*[119] *. Bulk Bi values and some common metals have been included for reference.*

1.3.2 Bismuth Oxide and Surface Functionalisation

One of the main issues of Bi thin films is their tendency to readily oxidise in air, thus requiring all processing to take place in UHV systems. While this might be feasible for a lab scale environment, it is not viable for large scale applications due to the high processing cost. The oxidation of bismuth films was first reported by Hapase *et al.*[120] in 1967; vacuum deposited films were oxidised in O_2 rich environments at a range of temperatures in order to understand the mechanism of oxygen uptake. They reported that oxidation proceeds through the diffusion of Bi from the substrate into the oxide film, as already hypothesised by Palkar *et al.*[121], through a Wagner mechanism. In 1978 Komorita *et al.*[122] further explored the oxidation of Bi thin films, by varying parameters such as the oxidation time, temperature and the oxygen content. This study

further confirmed that a diffusion process takes place and they were able to correlate the thickness of the oxide film to a diffusion equation. Moreover, the group was able to show that a metastable crystal phase of the oxide is present which tends to evolve to a different stable phase when heated.

In 1990 Puckrin *et al.*[123] compared the oxidation of bulk bismuth and thin films using Auger electron spectroscopy, electron energy loss spectroscopy and work function measurements. The data showed that, in both cases, BiO was the first oxide formed on the surface of the samples and, for an exposure time in air of about 1 second, the total oxide thickness was roughly 8 monolayers, *ca*. 2 nm. These data were then further confirmed by a study from Kowalczyk *et al.*[124], in which Bi nanostructures were shown to oxidise anisotropically. XPS showed that after exposure to air for 1 second the oxide formed on the surface was BiO. 5-day air exposure led to further oxidation of the film and to the formation of Bi_2O_3 (see **Figure 1.17**). In general, the oxidation behaviour of Bi thin films has not been extensively studied, and it is further complicated by the large array of oxidation states that Bi can form. However, if Bi processing is to become a viable area of study, it will be necessary to tackle the issue of oxide removal and passivation to allow for ambient air handling.

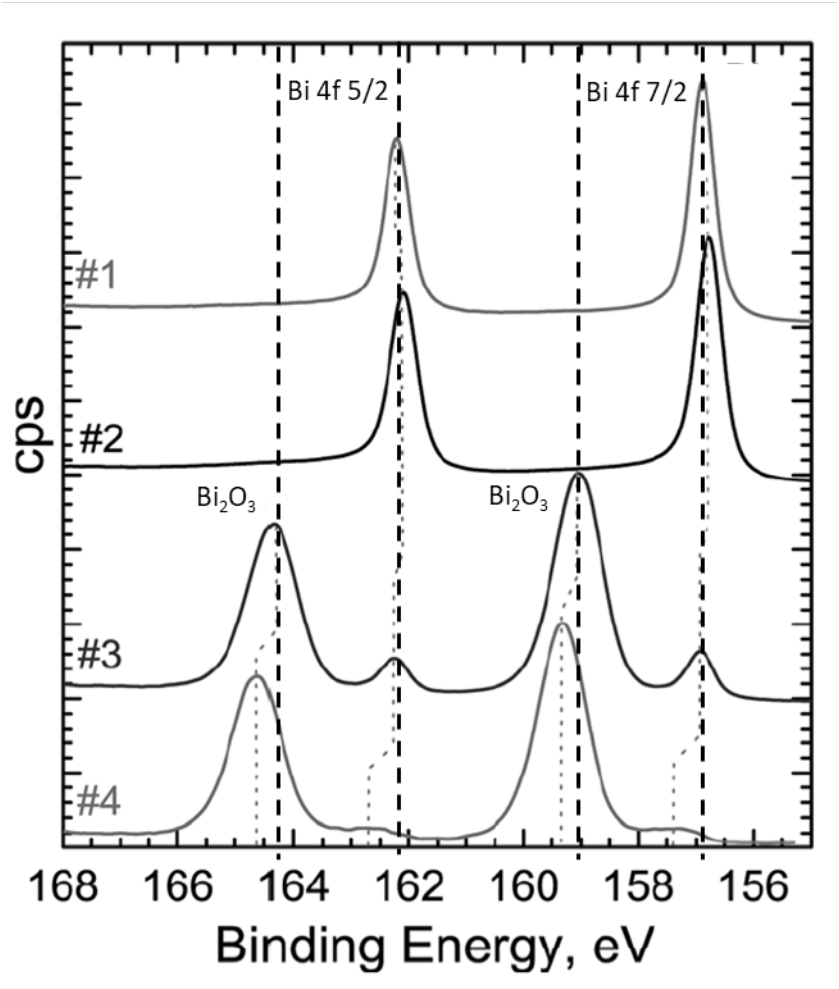


Figure 1.17: *Bi 4f XPS spectra of (1) Bi(111) and (2) Bi(110) nanostructures. XPS spectrum (3) shows Bi(110) after 1s air exposure and (4) shows Bi(110) after 5 days air exposure. Adapted from* [124]

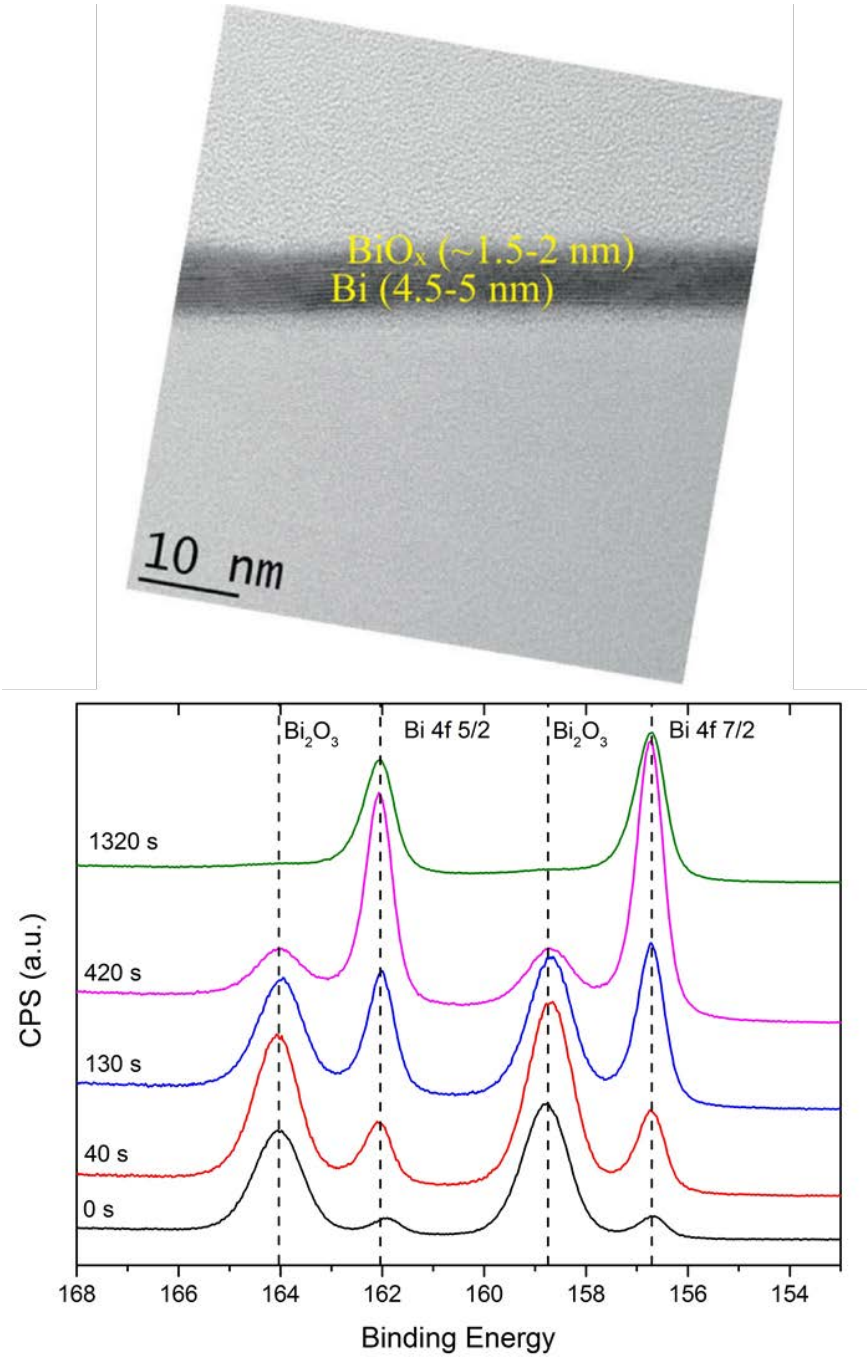


Figure 1.18: *(Top) HR-TEM of MBE grown Bi thin films showing an oxide formed on the surface and (bottom) XPS spectra of the film after different etching times using Ar ions to remove the surface oxide*[3].

Later studies by Gity *et al.*[3] analysed by TEM the surface of Bi thin films grown via MBE and further confirmed that a native oxide with a thickness of 1.5-2 nm is indeed present on the surface when the film is exposed to air. XPS depth profiling allowed for removal of the surface oxide using an Ar-ion cluster, in order to characterise the spectra lines of the underlying elemental Bi film (**Figure 1.18**).

While there are no reports of reactions carried out on the surface of Bi thin films, there are extensive reports on the chemistry of Bi compounds as early as 1966[125]. Bismuth oxide and other derivatives have been used extensively as catalysts for the oxidation of numerous organic compounds, as the reviews from Postel[126], Bothwell[127] and Ollevier[128] describe in detail. Moreover, organobismuth compounds[129,130] and coordination complexes[131] have been employed for a long time in organic synthesis and have been extensively studied. **Chapter 5** of this thesis will discuss a novel method for the removal of bismuth oxide from Bi thin films and concurrent passivation of these films to prevent reoxidation and enable ambient handling.

1.4 Bibliography

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Chapter 2

Experimental

2.1 Dopant Precursor Synthesis

Arsenic trichloride, anhydrous diethyl ether, stabilised deuterated chloroform and mesitylene were purchased from Acros Organics. Mesitylene was dried, distilled from calcium hydride and stored over 3 Å molecular sieves before use. All other chemicals were used as received. Allylmagnesium bromide was purchased from Sigma-Aldrich and used as-received. All chemical manipulations were carried out under inert conditions in a high purity argon (Air Products Inc.) atmosphere using a combination of Schlenk apparatus and an inert-atmosphere glovebox. Triallylarsine (TAA) was synthesised according to literature procedures.[1] Allylmagnesium bromide (138.5 ml, 138.5 mmol) was set stirring in a three-neck round bottom flask. To one arm was attached a water condenser with an argon inlet. A pressure-equalising addition funnel containing arsenic trichloride (5.0 g, 2.3 ml, 28 mmol) in anhydrous diethyl ether (25 ml) was attached to the middle arm and the remaining arm was closed. The arsenic trichloride solution was added to the Grignard reagent over a period of 30 min under vigorous stirring, while keeping the solution at 0 °C. On completion of the addition, the reaction was left to warm up to room temperature and was then heated to reflux for 2 h. The reaction was then cooled back to 0 °C and a deoxygenated, saturated solution of NH_4Cl at 0 °C was added very slowly to neutralise the remaining Grignard reagent. The mixture was filtered into an extraction funnel and the organic phase was extracted with a 25 ml portion of diethyl ether. The aqueous phase was then washed with 3 × 25 ml portions of diethyl ether and the organic fractions were combined with the previously extracted organic phase. The organic phase was then dried with granular magnesium sulphate and filtered into a round-bottom flask. Excess diethyl ether was removed by rotary evaporation and the oily residue was distilled twice using a Kugelrohr short path distillation apparatus.

2.2 Characterisation Techniques

2.2.1 X-Ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is a surface analysis technique used to qualitatively characterise the chemical states and binding environment as well as quantitatively measure the elemental compositions. An XPS spectrometer measures the kinetic energy of electrons emitted from the core levels of the surface atoms when they are illuminated by X-ray photons of energy $h\nu$. The kinetic energy (Ek) measured is then converted to binding energy (BE) according to the photoelectric effect equation, $BE = h\nu - Ek - \Phi$,[2] where Φ stands for the spectrometer work function. Only electrons which are emitted without losing kinetic energy contribute towards the elemental photoelectric lines. Electrons from deeper within the sample, which lose kinetic energy through inelastic scattering when impacting the other atoms in the lattice during escape, contribute toward the background spectrum; while X-rays can penetrate in the sample down to few micrometers, only the electrons from the first tens of nanometers of the substrate can escape without losing enough kinetic energy to be detected.

An X-ray photoelectron spectrometer typically consists of a hemispherical electron energy analyser and an anode X-ray source, *e.g.* Mg Kα (1253.6 eV) or Al Kα(1486.6 eV) within an ultra-high-vacuum chamber (typical system base pressures are in the 1 × 10^{-10} mbar range). The photons emitted by the Mg and Al anodes offer the best energy resolution while still able to excite at least one core level for each known element. The analyser is normally operated by selecting an energy "window",

accepting only the electrons having an energy falling within the range of this fixed window, referred to as the pass energy.

XPS spectra were acquired on an Oxford Applied Research Escabase XPS system equipped with a CLASS VM 100 mm mean radius hemispherical electron energy analyser with multichannel detectors in an analysis chamber with a base pressure of 5.0×10^{-9} mbar. Survey scans were recorded between 0-1400 eV with a step size of 0.7 eV, dwell time of 0.5 s and pass energy of 100 eV. Core level scans were acquired at the binding energy relative to the element analysed with a step size of 0.1 eV, dwell time of 0.5 s and pass energy of 20 eV averaged over 20 scans. A non-monochromated Al-kα X-ray source at 200 W power was used for all scans. All spectra were acquired at a take-off angle of 90°with respect to the analyser axis and were charge corrected with respect to the C 1s core level line with an assigned binding energy of 284.8 eV. Spectra were processed using CasaXPS software where a Shirley background correction was employed, and peaks were fitted using Voigt profiles.

2.2.2 Fourier Transform Infrared Spectroscopy (FTIR) and Attenuated Total Reflectance (ATR) FTIR

Different chemical groups absorb different frequencies of radiation that are characteristic of their chemical structure and the immediate bonding environment. When subject to infrared radiation (IR, with wavelength comprised between 4000 – 500 cm^{-1}) molecular bonds can stretch, bend and vibrate according to the functional groups present. FTIR analysis involves guiding an IR beam through an interferometer and then through the sample. This allows the full range of IR frequencies to be scanned simultaneously allowing for fast data acquisition and high quality spectra. The FTIR

response is an interferogram which is then converted to a spectrum via Fourier transformation.

Attenuated total reflectance infrared spectroscopy (ATR-FTIR) involves passing an incident ray of infrared light first through a hemispherical crystal of a high refractive index material, which must have higher refractive index than the substrate being measured. The crystal then reflects off the internal surface in contact with the sample. The internal reflectance coming from the crystal creates an evanescent wave which extends into the sample which is in tight contact with the crystal. Functional groups on the surface which absorb IR will then cause attenuation of the evanescent wave; the wave is then measured as it exits the crystal. Attenuated total reflectance infrared (ATR-FTIR) spectra were recorded using a Nicolet 6700 Infrared Spectrometer with a VariGATR and a liquid N_2 cooled MgCdTe detector using 3000 scans at a resolution of 2 cm^{-1}. Spectra were collected under p-polarisation in an ambient atmosphere and an ambient scan was carried out prior to measuring the samples, in order to subtract background signal coming from ambient moisture and atmosphere.

2.2.3 Electrochemical Capacitance Voltage Dopant Profiling

Capacitance-voltage (CV) measurements are one of the most widely used electrical characterisation techniques used to measure active dopant distributions in samples, as the depth distribution of the carriers is closely related to the dopant profile. Unfortunately, the maximum depth for Schottky-CV measurements is limited due to reverse-bias voltage breakdown. To rectify this problem, Ambridge and co-workers[3] suggested that an electrolyte, when in contact with a semiconductor can form a quasi-Schottky contact, creating a depletion region that is devoid of conducting

electrons/holes but contains ionised donors and electrically active defects or traps. This depletion region then behaves like a capacitor and can allow for calculation of the density of electrically active carriers. The main advantage of this technique is that the maximum depth is not limited as the Schottky barrier is replaced by an electrolyte. The ECV profiling is then carried out in two main steps: i) measurement of the CV of the electrolyte-semiconductor capacitor and ii) self-limited etching of the material. The etching takes place either using forward bias, in the case of *p*-doped samples, or UV illumination and reverse biasing where *n*-type samples are being analysed. Repeated etch and measurement cycles enable a depth vs active dopant (carrier) concentration profile to be obtained. ECV analysis was carried out on a WEP Control CVP21 wafer profiler using 0.4 M disodium 4,5-dihydroxy-1,3-benzenedisulfonate (Tiron) as the etchant for Ge. Scanning parameters were automatically controlled by the instrument by selecting the appropriate sample type, layer map and etchant combination, with etching depths down to 300 nm. Error in active carrier concentration did not exceed 10 % for ECV analysis on Ge.

2.2.4 Secondary Ion Mass Spectrometry

Secondary Ion Mass Spectrometry (SIMS) is a technique used to analyse the chemical compositions of thin films and surfaces by using a focused primary ion beam to sputter the surface of a sample and analyse the ejected secondary ions emitted. The standard technique is usually qualitative but, when combined with standards of known composition, it can be considered a quantitative technique. A Time-of-Flight SIMS (TOF-SIMS) instrument generally consists of a primary ion gun, UHV system chamber to increase the mean free path of the ions, a linear flight path using an ion reflective mirror and a mass analyser. TOF-SIMS can allow for elemental and

molecular information of the outermost surface of a sample as virtually no sputtering occurs during the analysis of the samples as the beam ion dose is too low ($<1 \times 10^{12}$ at/cm^2). An auxiliary sputtering source can then be used to carry out depth profiling of a sample. If used for dopant analysis, SIMS yields the total chemical concentration of an element, *i.e.* combined active and inactive carrier concentrations. SIMS spectra for **Chapter 3** were collected in collaboration with the Centre de Microcaractérisation Raimond Castaing at the University of Toulouse, France. The measurements were carried out on a CAMECA IMS 4F6 spectrometer equipped with a O_2^+, O^- and Ar^+ source. A low energy mode of 2 kV accelerating voltage and beam current of 20 nA was used to analyse the composition of the sample. SIMS spectra for **Chapter 4** were collected using a TOF-SIMS 5 system from ION® TOF in the Leti CEA-tech laboratories in France. Sputtering was performed with a 2 keV Cs^+ ion beam incident at 45° and analysis was performed using a 30 keV Bi^+ ion beam incident at 45°. The sputtered crater was 200 µm × 200 µm whereas the analysed zone was 50 µm × 50 µm. The Si concentration was quantified using relative sensitivity factors from an n-doped reference sample; the reference sample was also used to measure the sputter rate in GaN to quantify the depth scale.

2.2.5 Nanowire Electrical Measurements

Measurements on 4-point nanowire test structures were carried out using a Cascade 4-probe Manual Prober together with an Agilent B1500 Device analyser. All the data was collected at room temperatures with voltage sweeps from -2 to 2 V.

2.2.6 Electron Microscopy

Electron microscopy a widely used method for morphological characterisation of nanomaterials. The very short wavelength of the electron (2.5 pm at 200 kV), mean it is possible to achieve atomic scale resolution of some materials. Transmission electron microscopy (TEM) studies the interaction of an electron beam which is transmitted through a sample. Samples were prepared by cutting a thin lamella which was then loaded onto a Cu grid for TEM analysis. TEM is useful in determining the crystallinity of materials and any lattice defects. The TEM lamellae for analysis were prepared on a FEI Helios Nanolab SEM/FIB cutter. TEM images were acquired on a JEOL 2100 HRTEM microscope operating at an accelerating voltage of 200 kV.

2.2.7 Atomic Force Microscopy

Atomic force microscopy (AFM) is a technique used to map the topography of a sample. A sharp tip at the end of the AFM cantilever is brought near to the surface of a sample. A laser is shining on top of the cantilever. The cantilever is deflected when it interacts with the surface and the tip movement is then registered by the laser and converted into height values. AFM images were collected was a Veeco® instrument. All scans were carried out on a 3 µm × 3 µm area in non-contact mode in air at room temperature with scan speeds ranging from 0.300 to 0.500 Hz and 512 lines.

2.2.8 Nuclear Magnetic Resonance

Nuclear magnetic resonance (NMR) spectroscopy was used to verify the formation of reaction compounds during the oxide removal of bismuth. ^{1}H (300 MHz) and ^{13}C (75.5 MHz) NMR spectra were recorded on a Bruker Advance 300 MHz NMR

spectrometer. All spectra were recorded at 300 K in deuterated chloroform ($CDCl_3$) using tetramethylsilane (TMS) as internal standard.

2.2.9 Photoluminescence spectroscopy

Photoluminescence (PL) spectroscopy analysis allows for the evaluation of the crystalline quality of III-V semiconductors such as GaN or InP, as well as the quantifications of defects and impurities[4]. PL analysis was performed by irradiating GaN samples with an Argon ion laser (354 nm) and detecting the emission with a Horiba *i*HR320 imaging spectrometer, equipped with a Synapse® thermoelectrically cooled CCD detector. The measurement was averaged over 4 scans and 2nd order diffraction peaks from the laser have been removed from the final spectra.

2.2.10 Hall Measurements

Hall effect measurements exploit the Hall effect that electrons experience when placed in a magnetic field. A magnetic field is applied perpendicular to the current flow in a semiconductor material and due to Hall effect electrons accumulate to one side of the sample, thus leading to an electric field across the sample due to uneven distribution of charge. This effect in turn leads to a potential difference which is known as the Hall voltage V_H. From the measured Hall voltage, it is possible to extract the n_s sheet carrier density of the sample from the relation, as shown in equation 2.1 below:

$$V_H = \frac{IB}{qn_s} \qquad (2.1)$$

Where I is the current applied in ampere, B is the magnetic field, in Wb/cm^2, and q is the elementary charge in coulombs. The samples can be measured using the Van der

Pauw method, which employs a four-point probe placed around the perimeter of the sample. With this method it is possible to measure samples of any shape, as long as they are flat, have homogeneous composition and are isotropic, the contacts are at the edges of the sample and the area of the contacts is at least one order of magnitude smaller than the area of the entire sample.[5–7] This measurement setup allows the resistivity of the material, the doping type, the sheet majority carrier density and the mobility of the majority carriers to be calculated.

Hall effect measurements were carried out on a LakeShore® 8600 series instrument; the excitation current ranged from 10 µA to 100 µA while the excitation field was 1.7 T. Sample geometry type was approximated to a Van der Pauw square but, while every care was taken to cut samples to a perfect square, some error needs to be accounted in the results. To get a good electrical contact a Ga-Sn eutectic was deposited on the corners of the samples to perform the measurement, which also contributes to experimental error on the order of D/L, where D is the mean diameter of the contact and L is the distance between the contacts.

2.3 Molecular Layer Doping (MLD) of Germanium Substrates and Nanowires using organoarsenic and organophosphorus precursors

2.3.1 Functionalisation Procedure for Ge substrates using Triallylarsine (TAA) and Allyldiphenylphosphine oxide (ADPO)

All glassware was cleaned with a piranha wash and dried overnight at 130 °C prior to undertaking any molecular layer doping (MLD) experiments. The precursors allyldiphenylphosphine oxide (ADPO) and Triallylarsine (TAA) were dissolved in isopropyl alcohol (IPA) to make up a 1 % vol. solution. The solutions were degassed under nitrogen using a freeze-pump-thaw cycle that was repeated 3 times, before being

left to purge under nitrogen. P-type and n-type Ge wafers (mean background doping concentration of 5×10^{17} at/cm^3) were purchased from Umicore. Ge samples were cut from the wafer to squares of *ca*. 1 cm^2. The Ge wafers were degreased by sonication in acetone for approximately 180 s and subsequently rinsed in IPA. Each wafer was dried with N_2 followed by immersion for 10 min in a 10 wt% solution of HBr or HF, to remove the oxides and passivate the surface. Samples were then dried with N_2, rinsed once more with IPA and then dried again after which they were placed immediately into a two-neck quartz round bottom flask under N_2 to prevent re-oxidation. The degassed TAA or ADPO solutions were then cannulated under a positive pressure of N_2 to the flask containing the passivated samples. The UV lamp used for the UV reaction was a UVP Pen-Ray with mercury source and wavelength of 254 nm. The quartz flasks was irradiated with the UV pen for 3 hr; the reaction flask and the UV pen were covered in aluminium foil for the whole duration of the reaction. After the reaction had completed, the substrate was removed from the flask and sonicated in IPA for 90 s to remove any physisorbed species. The sample was then dried with N_2 and stored in a N_2 glovebox, or in a N_2 filled sample preserver, before subsequent processing and characterisation steps.

2.3.2 Fabrication of Ge-on-insulator Nanowire Test Structures

Intrinsically doped germanium-on-insulator (GeOI) substrates were patterned using a Raith e-Line Plus electron beam lithography (EBL) system and a high-resolution EBL resist known as hydrogen silsesquioxane (HSQ) purchased from Dow Corning. The substrates were firstly degreased by ultrasonicating them subsequently in acetone and IPA solvents. They were then blown dry with a N_2 gun and immersed in 1-2 wt% hydrofluoric (HF) acid for 30-40 s and rinsed under flowing DI water. The substrates were subsequently dipped in 4.5 M HNO_3 for 20 s, rinsed under DI water and

immediately submerged in a solution of 7.5 M HCl for 10 min. This step provided Cl-terminated Ge surfaces. The substrates were then dried thoroughly under flowing N_2 and a 1:2 concentration solution of HSQ in methylisobutyl ketone (MIBK) was spun on the substrates with 2000 rpm for 33 s (lid closed). This gave approximately 50 nm thick HSQ film on any substrate. The substrates were then baked at 120 °C for 3 min prior to EBL exposure.

EBL exposure was a two-step process where the first lithography step was used to expose only the high-resolution fin structures. In the second step the gold contact pads for the four probes were exposed. To attain a highly focused beam for the first step, a 10 kV beam voltage and a 100 μm write-field was chosen. To avoid the large exposure time, low-resolution contact pads were written with a 1 kV beam voltage and 400 μm write-field. After the EBL exposures, the substrates were developed in 0.25 M NaOH and 0.7 M NaCl solution mixture for 15 s followed by 60 s rinse in DI water and 15 s immersion in IPA. For the second lithography step the substrates were Cl terminated as before, excluding the HF dip, and developed using the same method. To transfer the HSQ pattern into the top Ge layer of the GeOI substrates, they were subjected to reactive ion etch (RIE) using Cl_2 chemistry in Oxford Instruments Plasmalab 100 system.

2.4 Molecular Layer Doping of GaN Substrates with Silicon

2.4.1 GaN Substrate Growth

Nominally undoped and n-doped GaN films, grown by metalorganic vapour phase epitaxy (MOVPE) were used for MLD experiments. The films were deposited onto AlN buffer layers supported on *c*-plane sapphire substrates, using an Aixtron close coupled showerhead 3 × 2” MOCVD reactor. The AlN buffer layer significantly

improves the electrical and optical properties of GaN by supplying nucleation centres with the same orientation as the substrate; these in turn reduce the amount of dislocations arising from the lattice mismatch between GaN and the substrate.[8] GaN was then deposited using trimethylgallium and ammonia as Ga and N precursors, respectively. The GaN films were grown at a temperature of 1060°C and a pressure of 150 mbar in a hydrogen atmosphere.

2.4.2 Functionalisation GaN Substrates with (3-Aminopropyl)triethoxysilane

All glassware was cleaned with Alconox detergent followed by a water rinse, a piranha wash and dried in an oven overnight at a temperature of 130 °C. (3-aminopropyl)triethoxysilane (APTES 99 %, Sigma), was used as a silicon MLD precursor. The sonication reaction was replicated from previous work[9] where the APTES was diluted to a 20 mM solution in toluene. The GaN was cleaved in coupons of *ca*. 1 cm^2 and cleaned in a hot piranha solution (H_2SO_4/H_2O_2, 3:1) by dipping for 20 min. The coupons were then rinsed in DI water to hydroxylate the surface and then sonicated in the 20 mM APTES solution for 90 min at temperature of 50 °C. The samples were then rinsed in methanol and toluene to remove any physisorbed species.

2.5 Oxide removal and stabilization of bismuth thin films through chemically bound thiol layers

2.5.1 Bismuth Thin Film Growth

Bi films used in this study were grown by molecular beam epitaxy (MBE) on undoped Si [111] wafers. Prior to deposition the Si substrates were chemically cleaned using a HF-last RCA[10] procedure to remove the native oxide and to passivate the surface with hydrogen. The substrates were subsequently heated in-situ to a temperature of 700 °C for 20 min to desorb hydrogen atoms from the Si surface. The Bi material flux was

generated by an effusion cell operated at a temperature of 550 °C, which yielded a growth rate of 17 nm/hr. Thickness and crystallographic orientation are the key parameters determining the resulting electronic structure of the thin films.

2.5.2 General Passivation Procedure of Bismuth with 1-dodecanethiol

A round bottom flask was preheated using a heating mantle to a temperature of 180 °C and left for 30 min. The bismuth MBE substrates were then placed in the flask which was kept under N_2 for the remainder of the reaction. The samples were annealed for 1 hr and the flask was then left to cool down at room temperature. Solutions of 1-dodecanethiol in IPA and hexane were prepared, with concentrations ranging from 1 to 100 mM. The solutions were then degassed using three freeze-pump-thaw cycles and transferred in the sample flask by cannula transfer, thus preventing any contact with the outer atmosphere.

The bismuth samples were left immersed in solution at room temperature overnight. The solution was then pumped out of the flask using a cannula and the samples dried by gently heating the flask using a heat gun in order to evaporate the remaining solvent. Clean IPA was then pumped into the sample flask to rinse off any adsorbed molecules. The IPA was then pumped out and the solvent dried once again. The same reaction procedure was used for bismuth powder which was used as received. The still inert sample flask was then transferred in a glovebox where the samples were transferred from the flask to a gelbox, which was carried in a N_2 filled sample preserver. The gelbox was kept in the sample preserver until XPS measurements were

carried out; the exposure time due to loading procedure in the XPS entry chamber was always below 30 s.

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Chapter 3

Molecular Layer Doping (MLD) of Germanium Substrates and Nanowires using Organoarsenic and Organophosphorus Precursors

Some of the data in this Chapter has been published as part of a peer reviewed article in *Mater. Sci. Semicon. Process* and in the proceedings of the *20th International Conference on Ion Implantation Technology (IIT).* My contribution to the research involved synthesising the dopant precursors, substrate cleaning and functionalisation and electrochemical capacitance voltage analysis.

Long, B.; **Alessio Verni, G.**; O'Connell, J.; Shayesteh, M.; Gangnaik, A.; Georgiev, Y. M.; Carolan, P.; O'Connell, D.; Kuhn, K. J.; Clendenning, S. B.; Nagle, R.; Duffy, R.; Holmes, J. D. 'Doping top-down e-beam fabricated germanium nanowires using molecular monolayers', *Mater. Sci. Semicon. Process.,* **2017**, *62*, 196-200.

Long, B.; **Alessio Verni, G.**; O'Connell, J.; Holmes, J.; Shayesteh, M.; O'Connell, D.; Duffy, R. 'Molecular Layer Doping: Non-Destructive Doping of Silicon and Germanium'. In *2014 20th International Conference on Ion Implantation Technology (IIT)*; IEEE: Portland, **2014**; pp 1–4. https://doi.org/10.1109/IIT.2014.6939995.

3.1 Abstract

As transistor architecture continuously evolves to more advanced designs and critical dimensions are still scaling down, the demand for alternative processing technologies and substitute materials is swiftly escalating. One such alternative is provided by molecular layer doping (MLD), a novel technique already well-established for materials such as Si and InAs. The process is based on (i) the reaction of dopant-containing molecules with a semiconductor surface and (ii) annealing to diffuse the dopant atom from the surface into the substrate. This Chapter details the successful MLD of crystalline Ge wafers and nanostructures by As and P atoms, to obtain an active carrier concentration of up to 9×10^{18} at/cm^{-3}. Atomic force microscopy imaging showed that the surface roughness of the films was not affected by any of the MLD steps. X-ray photoelectron spectroscopy analysis showed that functionalisation was successful and dopant profiling allowed for the extraction of the active carrier concentration and for an estimate of the dopant activation efficiency. The electrical resistivity of top-down fabricated Ge nanowires was found to decrease by several orders of magnitude after the MLD process, with no evidence from transmission electron microscopy analysis that the crystallinity of the nanowires had been compromised.

3.2 Introduction

Controlling the doping of nanoscale devices is becoming crucial as device size scale[1,2] and the architecture evolves from planar to non-planar, *e.g.* bulk to finFETs[3]. New and reliable doping methods that can be easily controlled, in terms of doping depth and conformality[4,5], are required. Traditional doping techniques, such as ion implantation, are becoming obsolete for tri-dimensional thin body structures, *e.g.* finFETs. One of

the main issues is the shadowing effect that arises when trying to implant a tightly packed array of nanofins, such as those found on an integrated circuit. Shadowing limits the maximum angle that can be used for ion implanting, often resulting in low and non-uniform doping and structural amorphisation[6]. Whilst amorphised structures can be recrystallised at high temperatures, achieving this with thin body semiconductor structures, *e.g.* finFETs, can be problematic. Studies have shown that in a narrow 3D thin-body fin structure, surface proximity leads to the formation of twin boundary defects in implanted regions. Theoretical studies have shown that if recrystallisation is retarded in Si fin structures, random nucleation and growth may occur, with partial transformation of the fin into polycrystalline Si[7]. However, this polycrystalline nature of Si results in poor device performance, *e.g.* high resistance and high leak currents even at small voltages.

In 2008 Ho *et al.*[8] developed a novel method for doping nanostructures termed molecular layer doping (MLD). The technique is based on (i) forming a self-assembled monolayer (SAM) of dopant containing molecules on the surface of a semiconductor followed by (ii) thermal diffusion of atoms via rapid thermal annealing (RTA). Thermal decomposition of this molecular layer enables dopant atoms to diffuse into the underlying substrate; the surface functionalisation is usually achieved through a reduction reaction between a hydrogen-terminated semiconductor surface and a labile C=C site on the dopant containing molecule[8,9]. According to the required application, MLD can be finely tuned as numerous parameters, such as the thermal budget or the molecular footprint of the dopant precursor, can be modified as required. MLD is already well-established for Si, with reports of doping being carried out with B, P and As-containing molecules on both bulk crystalline Si and on nanowire devices, leading to the formation of ultra-shallow junctions[8–10]. The technique has also been applied to

InAs[11], InP[12] and InGaAs[13–15] using S, Si and Sn dopant precursors. In these reports, MLD did not damage the semiconductor surfaces and the surface functional layers were found to be inherently conformal[16–18].

As far as semiconductor materials are concerned, Ge is a viable substitute for Si in semiconductor processing. Being from the same group as Si, Ge is compatible with complementary metal oxide semiconductor (CMOS) processing, allowing its implementation in already established production lines. Moreover, Ge has higher carrier mobilities than Si, leading, in theory, to better performing electrical devices. In general, processing and chemical techniques employed on Si are broadly transferrable to Ge. However, due to the complex and unstable oxides of Ge[19], the surface chemistry is vastly more challenging to control that Si and requires effective surface cleaning and passivation to prevent reoxidation. The data presented in this Chapter focuses on MLD of Ge wafers and nanowires with As and P. The choice of dopants was dictated mainly by their relatively high equilibrium solubility in Ge and their ability to easily in-diffuse. The surfaces were functionalised using a UV-initiated hydrogermylation reaction[20], due to the low decomposition temperature of the organic precursors used.

3.3 Results and Discussion

3.3.1 Surface Passivation and Functionalisation

Initial experiments were carried out on bulk crystalline Ge substrates, given the quicker turnaround time between processing and data collection, allowing for faster optimisation of the cleaning and passivation process and the subsequent thermal budget parameters. These optimised MLD process parameters were then applied to top-down fabricated Ge nanowires. The synthesis of the triallylarsine (TAA) arsenic

precursor is outlined in **Chapter 2** (**Section 2.1**) whereas the allyldiphenylphosphine oxide (ADPO) molecule was purchased from Sigma-Aldrich.

Surface cleaning and passivation were achieved using dilute HBr or HF, following previously outlined procedures[19], leading to the complete removal of surface GeO_2 and part removal of the GeO suboxide, making the surface accessible for hydrogermylation reactions. Atomic force microscopy (AFM) was employed to assess the surface roughness of the substrates before and after processing. For a process to be suitable for nanoscale device application, the surface roughness root mean square (RMS) value must be minimised, preferably below 0.5 nm. In the case of the mineral acid cleaning, there was no discernible increase in surface roughness post-processing with RMS values of <0.5 nm (see **Figures 3.1 (a), (b) and (c)**)

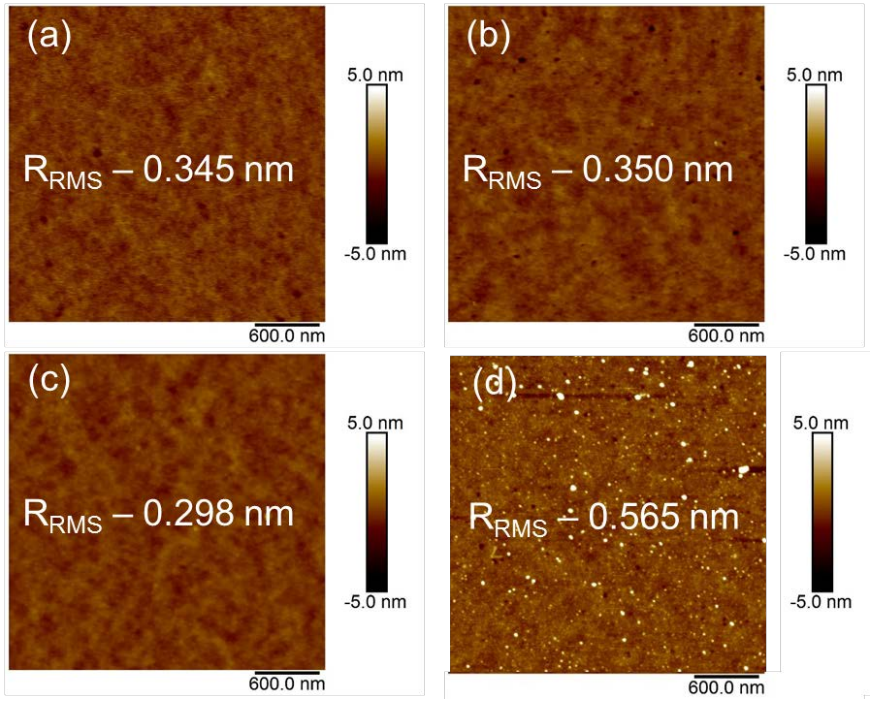


Figure 3.1: *Representative AFM comparison between (a) an as received Ge wafer (b) an HBr cleaned Ge wafer (c) an HF cleaned Ge wafer and (d) an allyldiphenylphosphine oxide (ADPO) functionalised Ge wafer. The increased roughness post functionalisation could be attributed to the presence of some multilayer islands of ADPO.*

Oxide removal from the Ge substrates was checked by comparing high resolution X-ray photoelectron spectroscopy (XPS) spectra (Ge 3d core level) before and after passivation (see **Figure 3.2**). Even though the GeO_x peak was greatly reduced after the cleaning process, some oxide still remained on the wafers, likely due to the presence of small quantities of water insoluble germanium suboxides (GeO) which can only be completely removed after more prolonged mineral acid dips[19]. However, this suboxide was found to have a negligible effect on subsequent functionalisation steps.

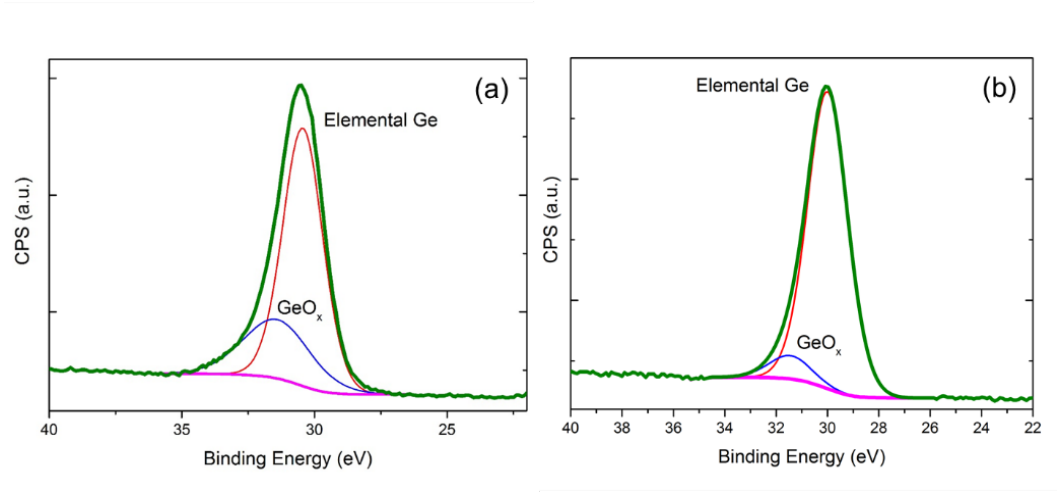


Figure 3.2: *(a) High resolution XPS Ge 3d core level scan of an as received Ge wafer; the native oxide as well as the suboxides are present. (b) After acid cleaning the native oxide is removed whereas some of the suboxides, harder to remove via wet chemical methods, are still present.*

The reaction between the dopant precursors and the surface of the Ge substrates was carried out through a UV-initiated hydrogermylation reaction[20] (see also **Chapter 2, Section 2.3**) chosen due to the low boiling/melting temperature of the precursors used, *i.e.* a melting point of 78 °C for ADPO[21] and a boiling point of 111 °C for TAA.[22] The C=C double bond of the ADPO and the TAA undergoes a radical breakdown and

reacts with the passivated surface to form a covalent Ge-C bond. The substrate was then sonicated in isopropyl alcohol (IPA) and acetone to remove any physisorbed species. **Figure 3.3(a)** shows an XPS survey spectrum of the surface of a Ge wafer after functionalisation with ADPO, and highlights the presence of a surface phosphorus group (see inset). However, it was not possible to use the P 2p core level peak for accurate quantitative analysis, as this overlaps with a Ge plasmon peak. **Figure 3.3(b)** shows the survey spectra of a TAA functionalised sample and the presence of arsenic on the surface was identified by the 3*d* L_3-$M_{4,5}M_{4,5}$ As Auger line (where the line is generated by an electron from the 3*d* dropping to the 2*p* vacancy and a 3*d* Auger electron being emitted) present at 266 eV (see inset). Even in this case the main core level peaks for As overlap with the Ge core levels plasmon peaks so it was not possible to use them for quantitative analysis. However, based on the molecular footprint and the extracted dopant dose values (see section **3.3.3**, **Table 3.1**), as well as the low surface roughness post AFM (**Figure 3.1d**), the surface was estimated to consist of a molecular monolayer with some small multilayer islands forming.

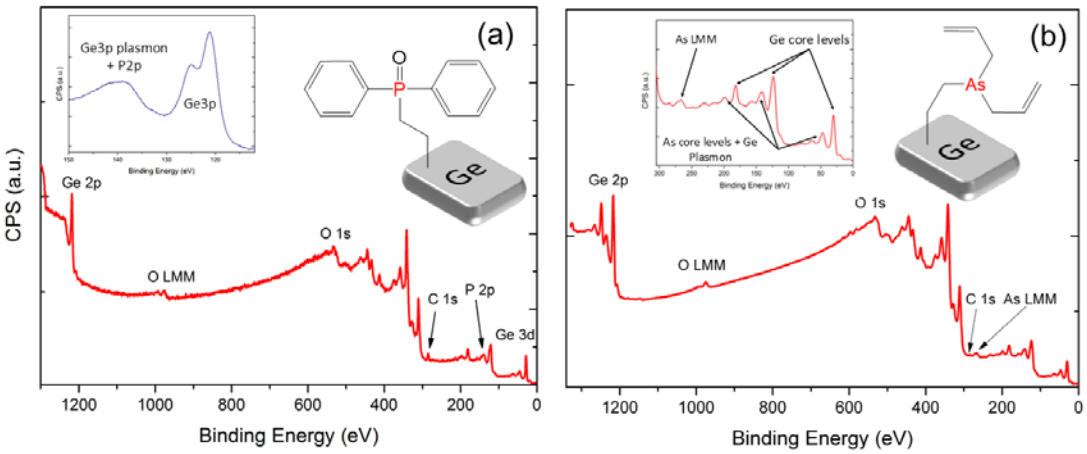


Figure 3.3: *Survey scan of (a) an ADPO functionalised Ge wafer and (b) a TAA functionalised Ge wafer with peaks of interest labelled. Insets shows a representation of the functionalised surfaces and the core level of the dopant atoms.*

3.3.2 Thermal Budget and Capping Study

Initial studies focused on the annealing conditions required to diffuse dopant atoms from molecules attached to the surface into a Ge substrate. The use of RTA required a thermal budget to be established where the aim was to maximise the concentration of dopant atoms in the first 10 nm while minimising their diffusion depth. Initial thermal budgets employed were 650 °C for 60 s and 700 °C for 300 s, using TAA functionalised samples. Data from these anneals were obtained from both electrochemical capacitance voltage (ECV) and secondary ion mass spectrometry (SIMS) profiling (**Figure 3.4**). ECV measures the active dopant concentration while SIMS measures the total dopant concentration. As both ECV and SIMS gave the same dopant profiles, within experimental error, this suggests that all of the diffused dopant atoms were activated; the dopant doses, *i.e.* area under the curve both for ECV and SIMS, obtained for the 650 °C annealed sample were 2×10^{14} at/cm^2 and 2.2×10^{14} at/cm^2, respectively. The diffusion of As atoms at a temperature of 700 °C was considered too deep as it passed the 500 nm mark; in addition, RTA specifications allow for a maximum operating temperature of 2/3^{rds} of the melting point of the substrate. For these reasons, 650 °C was considered the optimal annealing temperature. As-functionalised Ge wafers were then annealed for 1, 10 and 100 s at a temperature of 650 °C. The ECV profiles (**Figure 3.5**) show a peak carrier concentration of 7×10^{18} at/cm^3 for all three different thermal budgets, suggests that the solubility limit of As in Ge was reached at 650 °C.

This hypothesis is further confirmed by ECV data of a sample after two subsequent MLD cycles. **Figure 3.6** shows how only the total dose, and not the peak carrier concentration, were increased after the second cycle, going from 6.9×10^{13} at/cm^2 for the first MLD cycle to 1×10^{14} at/cm^2 after the second cycle. Moreover, there is no

difference in the depth profile after annealing for 1 and 10 s, indicating that the depth of the dopant diffusion cannot be controlled below 10 s, likely due to limitations in the ramp-up and cool-down stages of the RTA furnace employed (**Figure 3.5**).

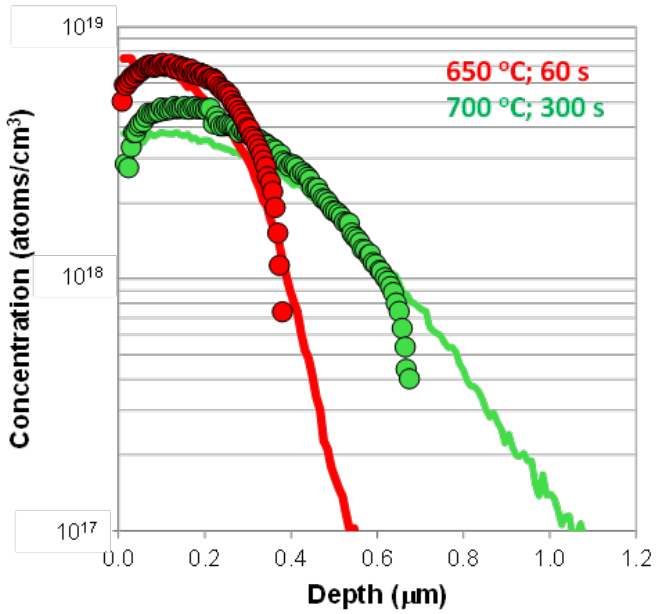


Figure 3.4: *ECV (Circles) and SIMS (continuous line) carrier measurement of an As-doped Ge substrate after rapid thermal annealing at two different temperatures/times and post cap removal.*

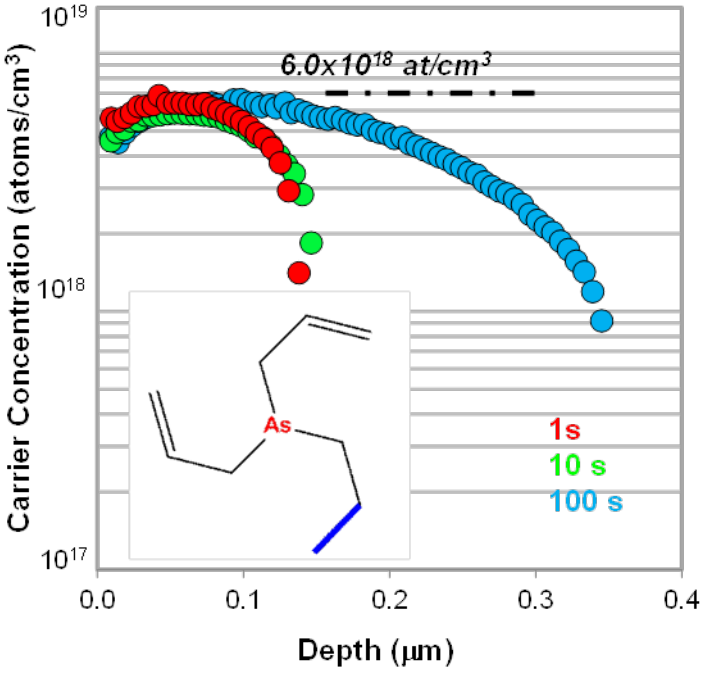


Figure 3.5: *Carrier profiling of As-doped Ge performed by MLD and RTA for 1, 10 and 100 s. The inset shows the molecule used (TAA).*

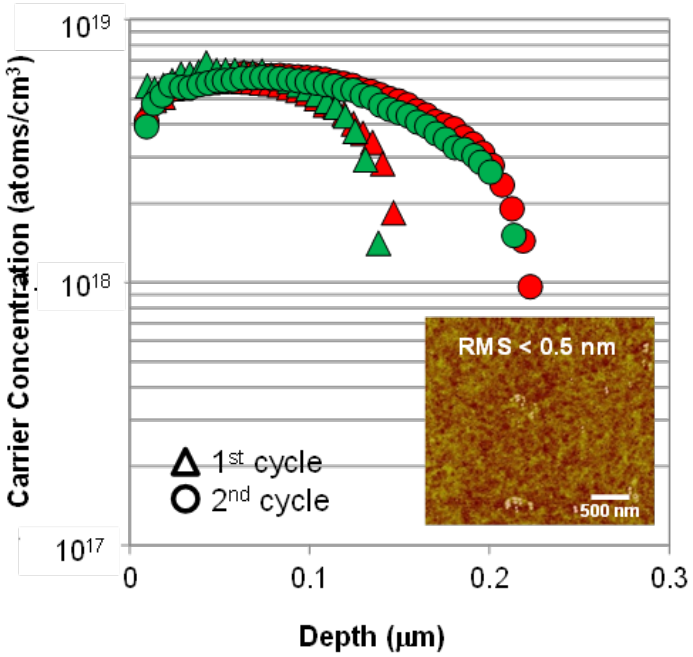


Figure 3.6: *Carrier profiling of two separate samples (green and red) of Ge doped by As after 1 MLD cycle (triangle) and after 2 MLD cycles (circle). RTA was carried out for 10 s at a temperature of 650 °C. The inset shows an AFM of a Ge sample after undergoing 2 MLD cycles.*

Once the thermal budget was defined, the influence of the capping layer on the diffusion profile was analysed. Traditional MLD processing uses a capping layer during the annealing step to prevent evaporation of the molecular layer. However, as the nanowires used in this study were fabricated on germanium-on-insulator (GeOI) substrates, a capping layer was not used to avoid detaching the fabricated nanostructures upon its removal with hydrogen fluoride.

To investigate the effect a capping layer has on the diffusion profile, SiO_2 was deposited by three different methods onto the surface of TAA-functionalised Ge substrates. 50 nm of SiO_2 were deposited by (i) sputtering, (ii) chemical vapour deposition (CVD) and (iii) evaporation. A fourth sample was processed alongside these where no capping layer was used. In all cases the samples were annealed for 10 s at a temperature of 650 °C. **Figure 3.7** shows the data from the capping layer study. Looking at carrier concentration values at a depth 50 nm, a sample with an evaporated

SiO_2 cap (known to have a low density and often porous) resulted in a carrier concentration of 2×10^{18} at/cm^3, much lower when compared with either CVD deposited (4.4×10^{18} at/cm^3) or sputtered SiO_2 (5.2×10^{18} at/cm^3) capping layers. For the sample with no capping layer, it was interesting to note that, although the incorporated carrier concentration of 3.4×10^{18} at/cm^3 was lower than for some of the capped samples, the As dopant still managed to diffuse into the Ge substrate. Hence, this data shows that it is possible to reduce the complexity of the MLD process, by reducing the number of steps required, *i.e.* no capping layer, which holds significant industrial value.

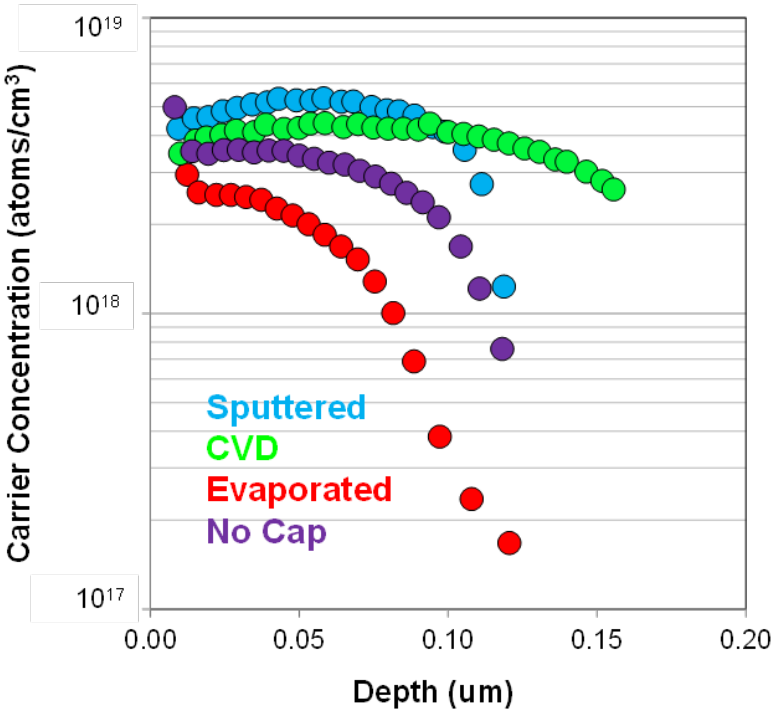


Figure 3.7: *ECV data for As-doped Ge samples with different capping conditions. RTA was carried out at temperature of 650 °C for 10 s. All caps were SiO_2.*

3.3.3 Dopant Diffusion

Once the final annealing recipe was determined to be a temperature of 650 °C for 10 s, the As- and P-functionalised samples were annealed in a nitrogen atmosphere by RTA. **Figure 3.8** shows ECV *vs* depth data of P and As-doped Ge samples. The data highlights the presence of dopants inside the substrate, with a mean peak carrier concentration of 7×10^{18} at/cm^3. The dopant profile of the samples follows a square box profile with a constant carrier concentration up to ~200 nm in the substrate. Active dose and diffusivity values extracted are summarised in **Table 3.1**. The molecular footprint of the precursors was estimated to be roughly 1 nm^2, thus giving a total maximum dose of 10^{14} at/cm^2 compared with the extracted dose, suggesting that all the available dopant atoms diffused into the Ge substrate and were activated, leading to a high doping efficiency.

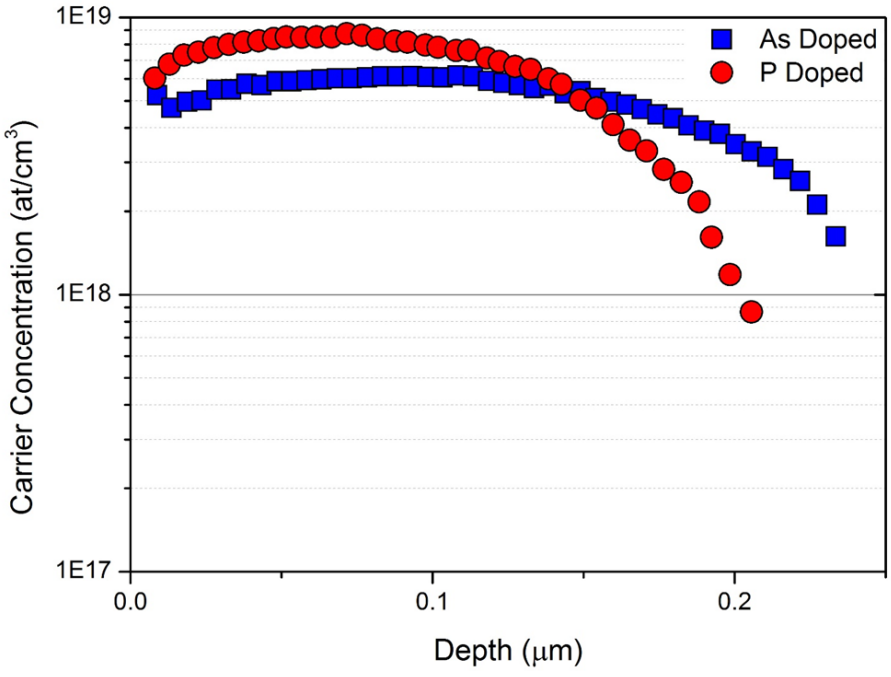


Figure 3.8: *ECV carrier measurement of As and P-doped samples after RTA and cap removal (annealing was carried out at a temperature of 650 °C for 10 s for both samples).*

Table 3.2: *Peak carrier concentration, total dose and diffusion coefficient extracted from ECV data of samples doped via As-MLD and P-MLD.*

Dopant	**Peak Carrier Concentration (at/cm^3)**	**Total Dose (at/cm^2)**	**Extracted Diffusion Coefficient (cm^2/s)**
Arsenic	6.18×10^{18}	1.13×10^{14}	4.59×10^{-12}
Phosphorus	8.73×10^{18}	1.24×10^{14}	1.08×10^{-10}

For the construction of metal oxide semiconductor field effect transistors (MOSFETs) a sharp doping profile, with an active carrier concentration above 10^{20} at/cm^3 and a sub 5-nm junction depth is desirable, particularly as overall architecture complexity increases and space requirements are becoming more stringent. Nonetheless, for a light source, a more uniform, box shaped doping profile such as the one shown in **Figure 3.8**, is preferable when Ge is used as a lasing material[23].

Dopant diffusion in Ge is mainly mediated by vacancies[24]; to diffuse in the crystal lattice a dopant needs to pair up with a vacancy to travel. However, at high dopant concentrations, a high proportion of dopants can become trapped in electrically inactive dopant-defect clusters. This trapping process can be prevented with higher processing temperatures during the annealing step, albeit leading to diffusion of the dopant further into the substrate[25,26]. Annealing at high temperatures for short reaction times, to avoid deep carrier diffusion and prevent dopant deactivation, has been demonstrated using laser and flash lamp techniques[27].

As and P are, together with Sb, the best *n*-dopants for Ge, due to their high diffusivity and ionisation energies. P, when compared to As, has a lower diffusivity, making it a more suitable dopant choice for the formation of shallow junctions. P concentrations

of up to 7×10^{19} at/cm^3 have been reported[23] in Ge using spin-on dopants, with the shallowest junction depth obtained being 500 nm. For ion implantation the highest dopant concentration achieved is 5×10^{19} at/cm^3, using a post implant rapid thermal processing (RTP) activation anneal, and 2×10^{20} at/cm^3 when using laser annealing[28]. Given this information, it should be possible to further improve the MLD technique using advanced annealing techniques, such as spike, flash lamp or laser annealing.

3.3.4 Resistance Reduction in GeOI Nanowire Devices

The MLD technique was also applied to top-down fabricated nanofin devices, with widths ranging from 20 to 1000 nm. The fabricated nanowire structures (see **Figure 3.9**) allowed a voltage to be applied to the inner contacts, while sensing the current at the two outer contacts (four-point probe measurement), eliminating lead and contact resistance from any measurements.

Figure 3.10 shows current *vs* voltage (*I*-*V*) data from P-doped nanowires of differing widths, between 20 and 1000 nm and fixed lengths of 10 µm. All nanowires displayed Ohmic behaviour, *i.e.* the current was found to depend linearly on the voltage, passing through the origin at zero volts. As the nanowire width decreased, the current passing through the nanowires decrease at a fixed voltage, *e.g.* at a fixed voltage of 1 V, a current of 6.6×10^{-6} and 1×10^{-7} A was obtained in nanowires with widths of 1 µm and 40 nm, respectively.

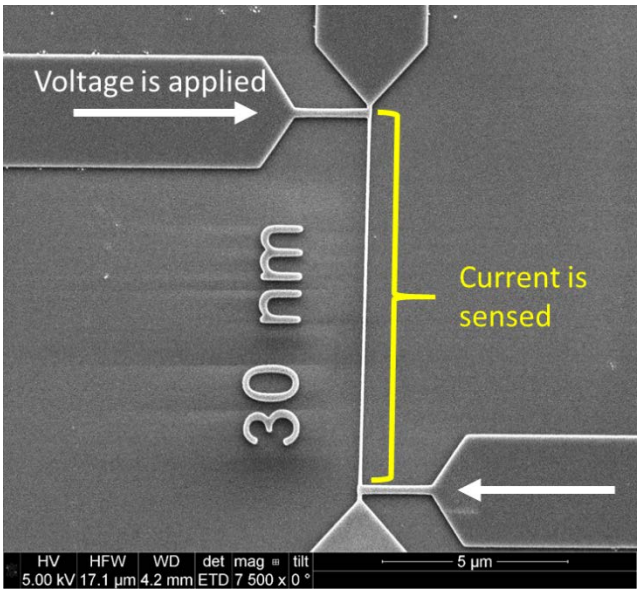


Figure 3.9: *An SEM micrograph of a nanowire test structure. The four electrodes used for the four-point probe measurement are shown; the voltage was swept between the inner electrodes and the current variation was sensed at the outer ones. Resistance was then extracted using Ohm's law.*

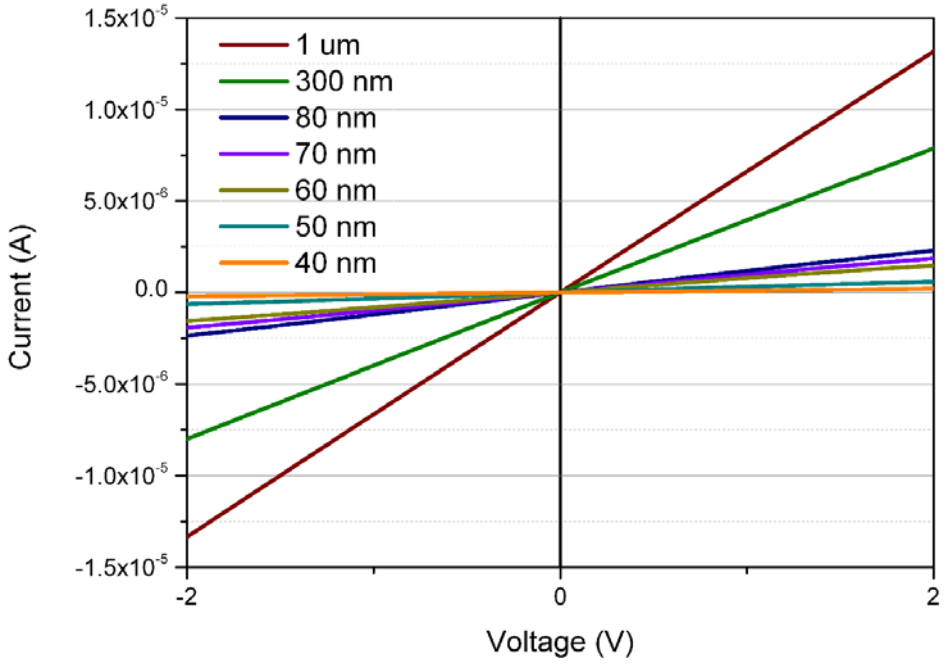


Figure 3.10: *I-V data of P-doped nanofin devices measured using a 4-probe method. The nanofins show Ohmic behaviour with scaling current for narrower fins. The 20 nm and 30 nm fins could not be measured as they got damaged during the handling of the sample.*

Figure 3.11 shows how the resistivity of intrinsic and MLD-doped Ge nanowires changes as a function of nanowire width, for a constant length of 10 µm. The resistivity of MLD doped Ge nanowires, particularly those with widths above 100 nm, decreased by up to five orders of magnitude compared to intrinsic Ge nanowires, *e.g.* 1×10^8 and 1×10^3 Ωµm for undoped and P and As doped wires with widths of 1 µm respectively, reaching levels comparable to those of bulk ion implanted Ge. However, as the dimension of the fin decreases, the resistivity change is less dramatic; one possibly is that carbon co-doping is happening, with the C supplied by the dopant molecule itself. Carbon has been shown to slow down the diffusion of both P and As in Ge but, at the same time, it does not suppress donor deactivation due to clustering as well as formation of inactive C_i-P pairs [24,25,29]. As the nanofin width decreases, the proportion of inactive clusters increases, and it limits the effective channel diameter.

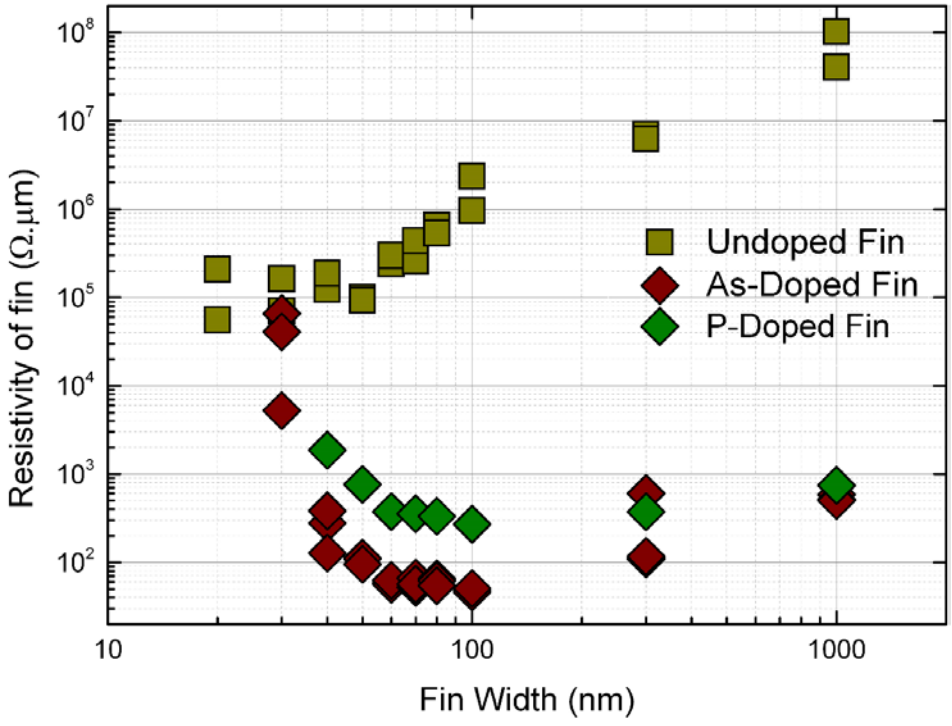


Figure 3.11: *Plot of resistivity of nanowire fins vs width. Plot shows how the MLD process successfully reduces resistivity for large fins but becomes ineffective as dimensions scale down.*

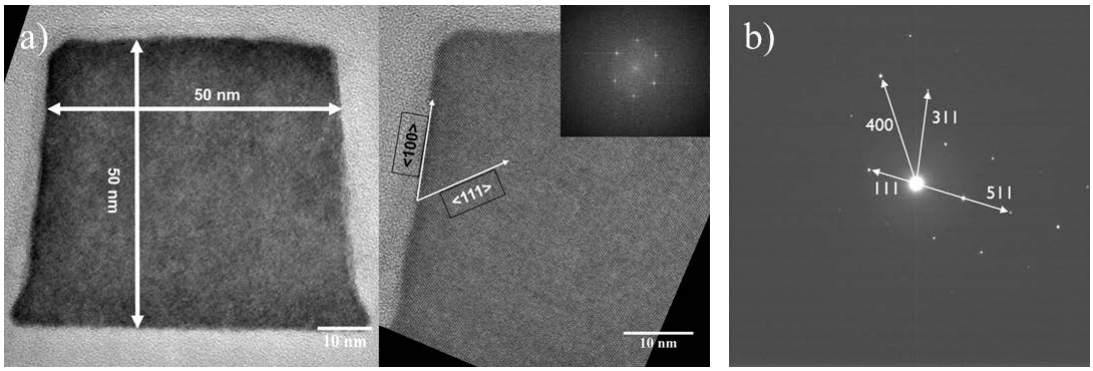


Figure 3.12: *a) Cross-sectional TEM of a P MLD-doped Ge FinFET. The image shows no evident of crystal damage (main crystallographic directions are indicated). The inset shows the FFT, which highlights how the sample is perfectly crystalline and no amorphisation has occurred. b) Electron diffraction pattern of the nanowire sample confirming good crystallinity – the main crystallographic directions are indicated on the pattern.*

To confirm that the MLD process did not damage the crystal structure of the nanowires, cross-sectional TEM imaging of the nanofins was performed. **Figure 3.12** shows the cross-section of a 50 nm top-down fabricated Ge nanowire after MLD processing. There was no evidence from the TEM images, or the electron diffraction patterns, that the nanowires were damaged by the MLD process, *e.g.* crystal defects or amorphisation typically observed with ion implantation. This is consistent with the gentle nature of the MLD process and shows that the technique can be transferred to nanostructured devices. Some improvements in the process are however necessary to avoid clustering and dope more effectively sub-30 nm structures. Dopant molecules with minimal carbon content should be ideally chosen, to minimise any co-doping effects. An alternative, high thermal budget/short time anneal, like millisecond laser or flash annealing, could help to promote the diffusion of faster moving P or As dopants when compared to slower moving carbon complexes[30]. Otherwise, as box-

shape like doping profiles could be arising from diffusion enhancement from high dopant concentration[31], it might also be necessary to reduce the initial dopant dose coming from the first MLD cycle and perform multiple MLD cycles so to avoid fast dopant diffusion.

3.4 Conclusions

Doping of non-planar nanostructures is problematic due to issues such as the non-conformality of conventional doping methods, as well as crystal damage arising from high energy ion implantation. The controlled doping of bulk and nanostructured Ge has been successfully demonstrated in this Chapter using organo arsenic and phosphorus molecular monolayers. High active dopant concentrations approaching 9×10^{18} at/cm^3 for P and 6×10^{18} at/cm^3 for As were achieved for bulk Ge; moreover it was possible to decrease the resistivity of MLD P-doped GOI nanowires up to five orders of magnitude when compared with the undoped wires. The MLD process was also observed to have no effect on the crystallinity of Ge nanowires produced and no visible damage or defects were observed. However, in this study the RTA system employed was found to be a limiting factor in achieving an abrupt doping profile with a high peak carrier concentration. Research must now continue into the optimisation of the doping profile, with data in the literature suggesting that more advanced annealing methods, such as laser or spike annealing, should provide the thermal budgets required.[32,33]

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Chapter 4

Monolayer Doping of GaN Substrates with an Organosilicon Precursor

4.1 Abstract

Silicon is the most commonly used n-dopant for GaN due to its high solubility; in the order of 10^{20} at/cm^3. However, if incorporated during growth of the GaN crystal, the maximum concentration achievable is approximately 10^{19} at/cm^3, above which the crystal lattice quality of the GaN starts to degrade[1]. Alternative *ex-situ* doping methods could lead to higher dopant concentrations as well as preventing parasitic SiN growth reactions that occur when high concentrations of Si-precursors are used during MOCVD growth.[2] One such *ex*-situ alternative is provided by molecular layer doping (MLD), a technique already applied on various group IV semiconductors as well as III-V materials.

This Chapter describes the MLD of GaN substrates with Si to a maximum concentration of 2×10^{19} at/cm^3. Morphological characterisation of the substrates showed that the surface quality was retained through the processing steps, with a final RMS value of 0.161 nm; active dopant dose, diffusivity and electron mobilities were also extracted, with values in line with other reports of Si-doped GaN. The focus of the experiments was a matrix of annealing temperatures and times ranging from 300 to 900 °C and 1 to 100s respectively, with the goal of achieving the highest active carrier dose and mobility.

4.2 Introduction

Gallium nitride is a III-N compound of great interest in nanoelectronics; when combined with other materials it can be used to form high electron mobility transistors (HEMT) that outperform Si for those applications that require high power and high frequency handling[3]. Moreover, given its high thermal stability and wide bandgap, GaN is a material well suited to high temperature applications[4] (see **Table 4.1**). When

compared with SiC, the other alternative for high power applications, GaN has a potential cost advantage and performs better for low voltage/high power applications, *e.g.* data centres, photovoltaics, electric vehicles, and targets the higher volume and cost-sensitive market of Si metal–oxide–semiconductor field-effect transistors (MOSFETs)[3].

Table 4.1: *Material characteristics for Si and the most common III-V compounds*[5–7]

Semiconductors		**Si**	**GaAs**	**InP**	**SiC**	**GaN**
Characteristic	**Unit**					
Bandgap	**eV**	1.1	1.42	1.35	3.26	3.49
Electron Mobility (300 K)	**cm^2/Vs**	1500	8500	5400	700	1000-2000
Critical Breakdown Field	**MV/cm**	0.3	0.4	0.5	3.0	3.0
Thermal Conductivity	**W/cm·K**	1.5	0.5	0.7	4.5	>1.5
Relative dielectric constant	**ε_t**	11.8	12.8	12.5	10.0	9.0

While doping *via* ion implantation is a well-established method in the semiconductor industry, it has not gained widespread use in III-V systems due to the damage induced by the high energy bombardment; these defects act as non-radiative recombination centres, thus leading to a decrease or suppression in the photoluminescence intensity and rendering the material useless.[8] Moreover, the high temperature anneals required for dopant activation is usually in the order of two thirds of the melting point of the material. For GaN this would mean reaching temperatures of 1500 °C or higher[9], well above its nitrogen desorption threshold at 800 °C, which would lead to vacancy formation and damage to the substrate surface due to GaN decomposition[10]. Therefore,

doping of GaN is typically carried out during growth, both in vacuum and vapour phase epitaxy methods. The amount of dopant introduced into the material during growth can be easily controlled either by varying the precursor flux in a molecular beam epitaxy (MBE) system, or by varying the flow rate of the dopant-containing gases into a vapour phase reactor[11].

The growth of GaN-based heterostructures can be achieved by different techniques, such as molecular beam epitaxy[12], hydride vapor phase epitaxy[13] and metal-organic chemical vapour deposition (MOCVD)[14]. The latter is mainly used in the semiconductor industry for growing GaN due to high growth rate and low operating costs. In MOCVD, films are typically formed by heating metal organic precursors, such as trimethylgallium (TMGa) or tryethylgallium (TEGa), in the presence of ammonia (NH_3) over a substrate at a temperature ~1000 °C. N_2 or H_2 are also often used as carrier gases in the growth process (see **Figure 4.1**).[15]

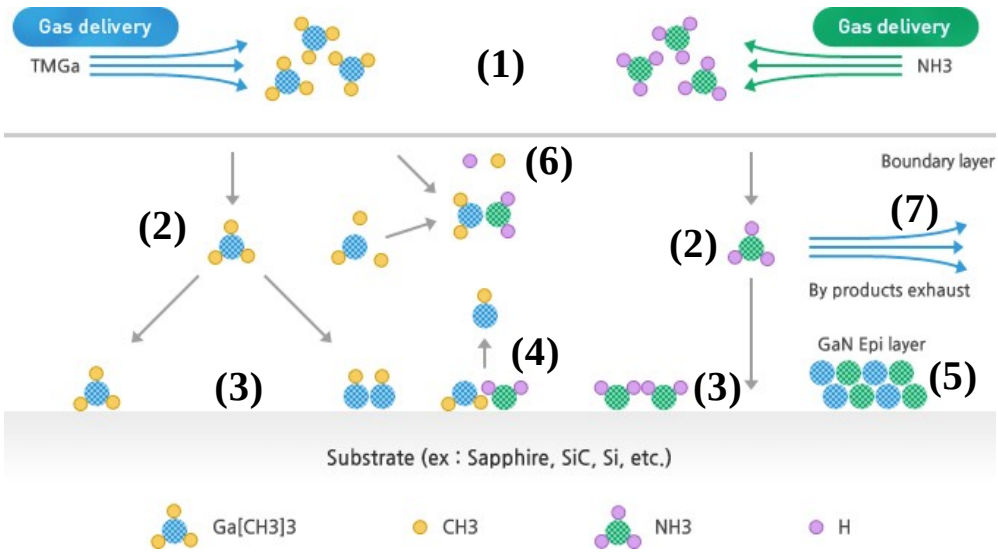


***Figure 4.1**: Schematic of GaN growth by MOCVD: (1) bulk transport of reactant into the process volume; (2) gaseous diffusion of reactant to the surface; (3) adsorption of reactant on the surface; (4) surface reaction; (5) crystal lattice incorporation; (6)*

reaction by-product desorption; (7) gaseous transport of by-products out of the process area.[16]

N-doping of GaN can be achieved using group IV atoms (such as C, Si and Ge), if incorporated as substitutions for Ga, or using group VI atoms (such as O, S and Se) when they substitute for nitrogen. Si is the most commonly used n-dopant due to its high solubility in GaN (in the order of 10^{20} at/cm^3 for the growth temperatures used) and relative ease of incorporation into the crystal lattice[11]. For MOCVD systems the gases normally used are silane[1] (SiH_4) or disilane[17] (Si_2H_6). While Si can be incorporated as a dopant up to carrier concentrations of about 10^{19} at/cm^3 [1], at higher dopant values the quality of GaN starts to degrade very quickly due to the build-up of lattice strain[18]. An excess concentration of Si atoms pin dislocations, preventing them from climbing and thus releasing the stress that occurs during growth, thereby rendering *in-situ* high concentration Si incorporation virtually impossible.[19]

An alternative *ex-situ* doping technique could therefore potentially achieve higher dopant concentrations as opposed to the current *in-situ* dopant incorporation methods described above; moreover it might also prevent parasitic reactions that occur when high concentrations of Si-precursors are used during MOCVD growth.[2] *Ex-situ* doping of III-V materials with Si-based in-diffusion doping could also be useful for nanostructures that require selective area doping; it has already been shown that through UV photopatterning it is possible to functionalise a confined area of a surface, thus allowing for potential precise control of the area to dope[20]. As already described in the Chapters 1 and 3, MLD has already been successfully applied to a large variety of substrates and architectures, from group IV semiconductors like Si and Ge[21–23] to III-V compounds such as InGaAs[24,25], InAs[26] and InP[27]. The MLD process is

extremely flexible as all reaction parameters, such as molecule choice, surface preparation and capping layer, can be finely tuned to optimise the final dopant concentration and diffusion.

The data presented in this Chapter focus on the application of Si doping of GaN by MLD. **Figure 4.2** shows the different process steps employed to carry out the cleaning, functionalisation and doping of the GaN substrate using MLD. A more detailed description of the method employed can be found in the Chapter 2 Section 2.4.2. A matrix of experiments was undertaken to identify optimal annealing conditions as to the best of my knowledge, Si-MLD has never been carried out on MOCVD grown GaN outside of a reactor.

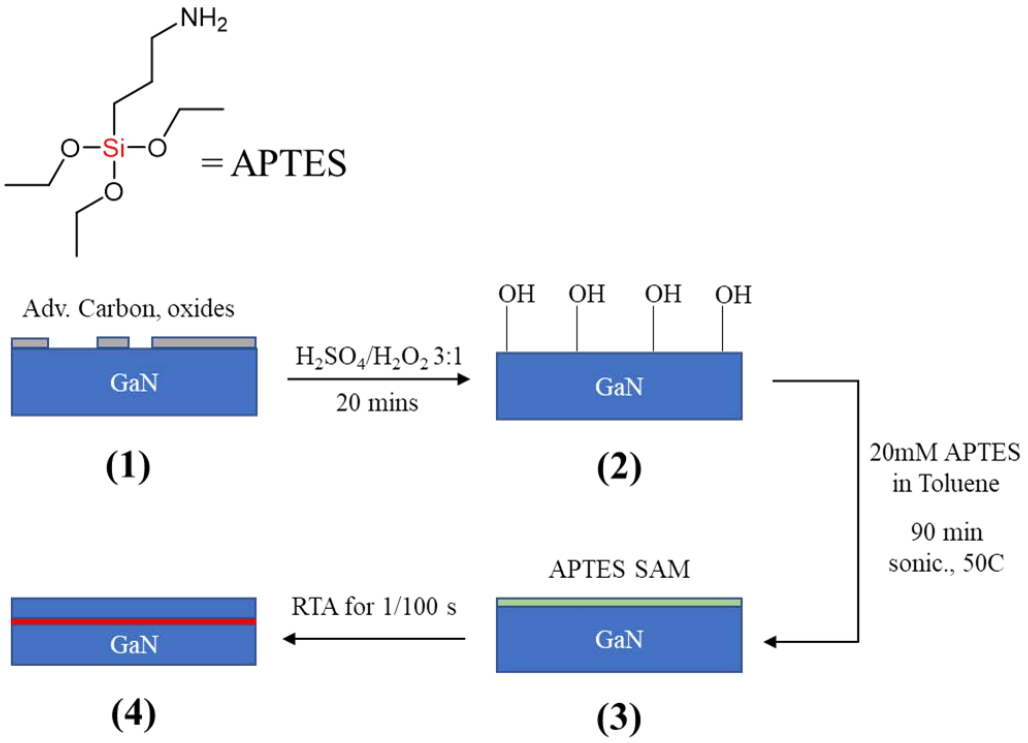


Figure 4.2: *Schematic of the MLD procedure carried out in this study: (1) as received surface is cleaned with Piranha solution leaving (2) OH- terminated GaN, which is then sonicated in the APTES solution to form (3) a self-assembled monolayer (SAM). The sample is the annealed to drive in the Si in the GaN (4).*

4.3 Results and Discussion

4.3.1 Surface functionalisation

The functionalisation reaction was carried out following the procedure outlined in the experimental section (see also **Figure 4.2** and **Chapter 2, Section 2.4**)[28]. The surface quality of the GaN films was analysed by atomic force microscopy (AFM) before and after functionalisation. When dealing with processes that can potentially be transferred to nanoscale devices, a root mean square (RMS) roughness value of < 1 nm is deemed acceptable at the end of the processing steps. **Figure 4.3** shows AFM images at different stages in the reaction process: (a) as received, (b) after cleaning with Piranha solution, (c) functionalisation with (3-aminopropyl)triethoxysilane (APTES) via sonication and (d) after subsequent capping, annealing and cap removal.

Before and after Piranha clean (**Figures 4.3(a) & (b)**) it is possible to see how the surface roughness is slightly improved as the RMS value goes from 0.321 nm to 0.266 nm post clean. After the subsequent functionalisation step with APTES (**Figure 4.3 (c)**) surface roughness is still maintained and some small agglomeration features start to appear in the AFM images, likely due to the hydrolysation and condensation of the APTES as the reaction is being carried out in a non-inert environment. The final capping, anneal and cap strip steps (**Figure 4.3 (d)**) have no impact on the quality of the surface, with a final RMS value of 0.161 nm, well below the 1 nm upper limit mentioned before.

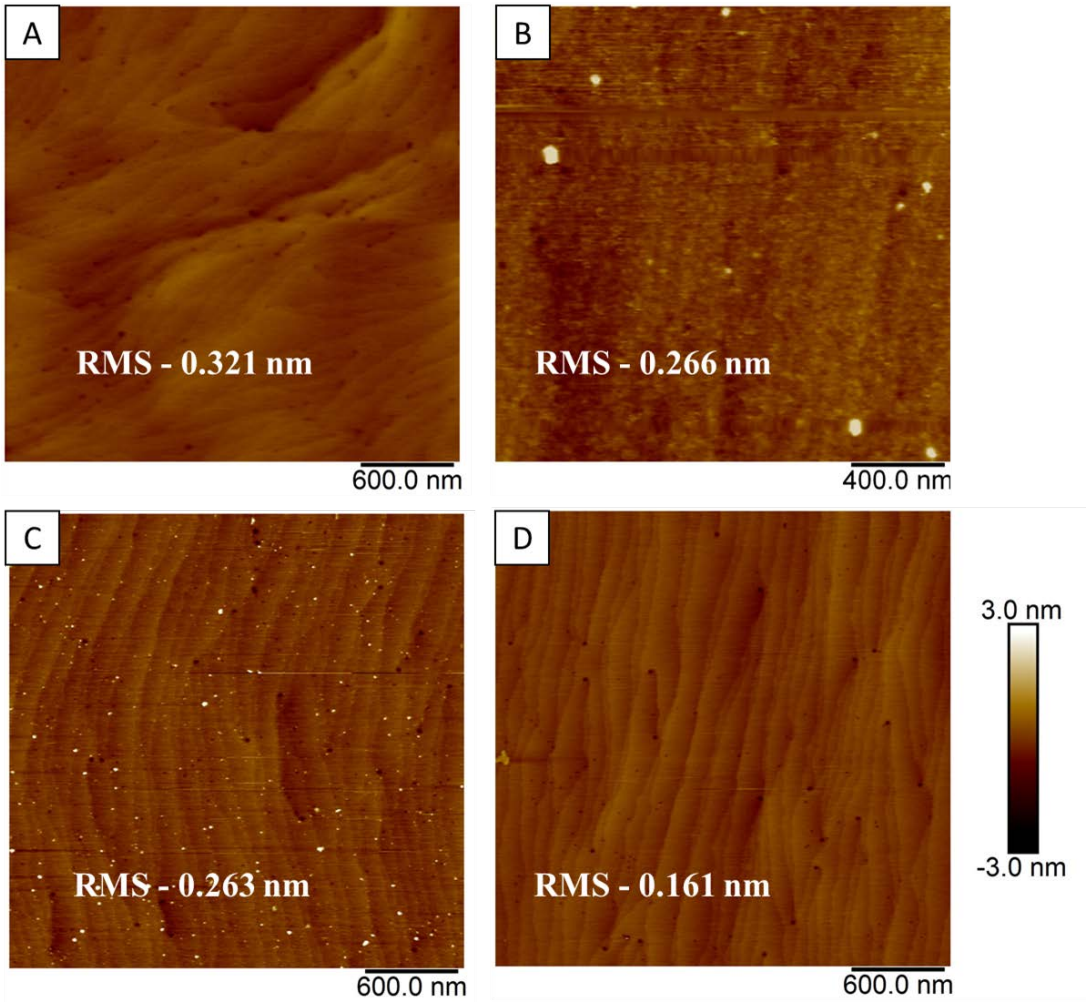


***Figure 4.3**: AFM imaging of a GaN film (a) as-received, (b) after Piranha clean (c) after APTES functionalisation with sonication and (d) after subsequent capping, annealing and cap removal. The surface integrity is maintained even after high temperature annealing if cap is used, preventing outgassing and degradation of the surface. The RMS of each AFM image is also indicated.*

The capping layer and annealing temperatures were also the object of a small preliminary study to optimise the process, see **Table 4.2**.

Table 4.2*: Matrix table of the annealing screening experiments. For each condition the RMS value from AFM is indicated.*

Temperature/Cap	**50 nm Sputtered SiO_2**	**No Cap**
700 °C	0.154 nm	0.151 nm
900 °C	0.159 nm	0.192 nm
1100 °C	0.279 nm	0.189 nm

GaN films functionalised with APTES, with and without 50 nm sputtered silica (SiO_2) caps, were annealed at temperatures of 700, 900 and 1100 °C. As also described in **Chapter 3**, a capping layer might be necessary in order to prevent dopant outgassing during the subsequent drive-in anneal step; moreover it was deemed necessary in order to preserve surface quality, as GaN starts to degrade at temperatures above 800 °C due to nitrogen desorption[10]. The effect of the cap was therefore checked by employing 50 nm of sputtered SiO_2 because the MLD studies on Ge outlined in **Chapter 3** showed that it leads to the best dopant dose being delivered. The annealing temperatures were chosen by keeping in mind the RTA thermal budget limitation of 2/3rd melting point of the material, *i.e.*, 2500 °C for GaN, giving a maximum operating temperature of ~1600 °C, as well as the maximum temperature limit of the tool, *i.e.*, 1100 °C; an anneal time of 10 s was employed for all samples for this first screening. At an annealing temperature of 1100 °C both capped and uncapped GaN samples showed signs of surface degradation as the RMS is increased when compared with the other

samples (**Figures 4.4 (c) & (f)**). Moreover, the AFM image for the uncapped sample (**Figure 4.4 (f)**) also shows pitting appearing due to onset of N_2 outgassing. While the uncapped samples started to show surface degradation starting from 900 °C (**Figure 4.4 (e)**), the capped samples showed the lowest RMS value up to 900 °C (**Figure 4.4 (b)**). Therefore, capping can allow for higher temperature anneals by delaying the onset of nitrogen desorption, thus broadening the range of thermal budgets that can be applied to the samples.

X-ray photoelectron spectroscopy (XPS) was carried out on surface functionalised GaN samples, prior to capping and/or annealing, to check for the presence of APTES bound to the surface of the films. **Figure 4.5** displays high resolution XPS survey and core level spectra for an APTES-functionalised GaN sample. **Figure 4.5(a)** shows the survey spectra from a functionalised film with the main peaks of Ga *2p*, O *1s*, N *1s* and C *1s* being highlighted. **Table 4.3** shows the percentage of the main peaks before and after the functionalisation; consistent with the functionalisation taking place, the Ga percentage decreases while the O, N and C signal increase as the surface of the GaN is covered with the APTES molecule.

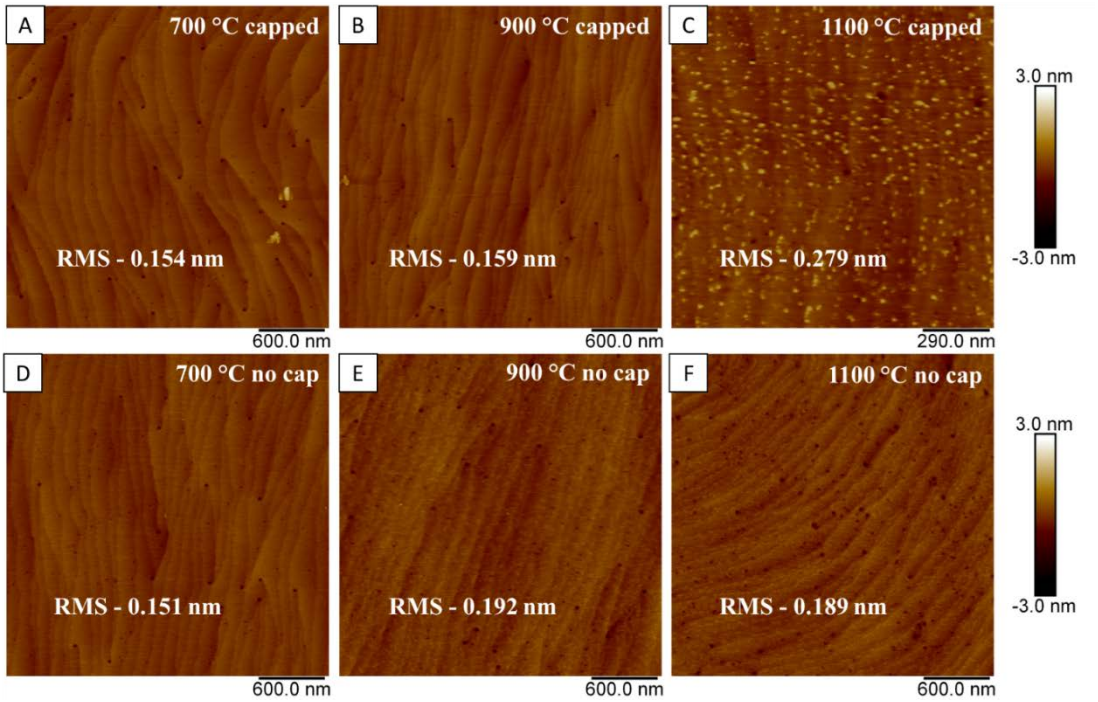


***Figure 4.4**: AFM images of the GaN annealing matrix: A – C, capped with sputtered SiO_2, annealed at the defined temperature and after cap strip. D – F, annealed without any cap at the defined temperatures. The RMS value increases with higher processing temperature due to onset of nitrogen desorption which can also be identified by the increased pitting in image F.*

***Table 4.3**: Percentage of XPS peak area from the survey spectra of GaN as received and after cleaning and APTES functionalisation. The functionalised surface shows a drop in Ga signal, due to signal attenuation from the self-assembled monolayer, as well as an increase in O, N and C signals due to the APTES molecule present on the surface.*

	Ga 2p	O 1s	N 1s	C 1s
As received	11.0 %	1.3 %	84.3 %	3.4 %
Post clean and functionalisation	3.3 %	22.0 %	57.5 %	17.2 %

As shown in **Figure 4.5(b)**, the Ga *3s* XPS core level emission peak at 160.2 eV was analysed for GaN films before and after surface functionalisation. This peak shows a 15 % decrease in intensity after functionalisation, also in this case due to signal attenuation resulting from the APTES surface groups. Moreover, **Figure 4.5(b)** shows the appearance of two additional peaks in the XPS spectrum of the APTES-functionalised GaN film which were not present in as-received samples; the peak at 153.8 eV[29] is the Si *2s* peak, further proof that the silane molecule is indeed present on the surface. The peak at 168.9 eV, assigned as a S *2p* peak, is likely due to sulphur remnants left on the surface of the GaN films due to the H_2SO_4/H_2O_2 cleaning; although this peak has never been shown in the GaN surface cleaning literature, it has been reported that high concentration H_2SO_4 based cleans on GaN can leave sulphate residues.[30] **Figure 4.5(c)** shows XPS data from the C *1s* core level peak; three different components can be identified. The first component at 284.8 eV is due to C-C signal contribution from the molecule skeleton and adventitious carbon, the second component at 286.3 eV[31] can be attributed to the C-amino features present on the molecule, whereas the last peak at 287.2 eV[32] is associated to the C-methoxysilane bond. The XPS N *1s* peak shown in **Figure 4.5(d)** can be deconvoluted into two components; one at 397.1 eV[33] due to nitrogen in the GaN surface, and one at 398.6 eV[34,35], due to the amino group present on the APTES molecule. At 402.8 eV a N *1s* a plasmon energy loss component is present.

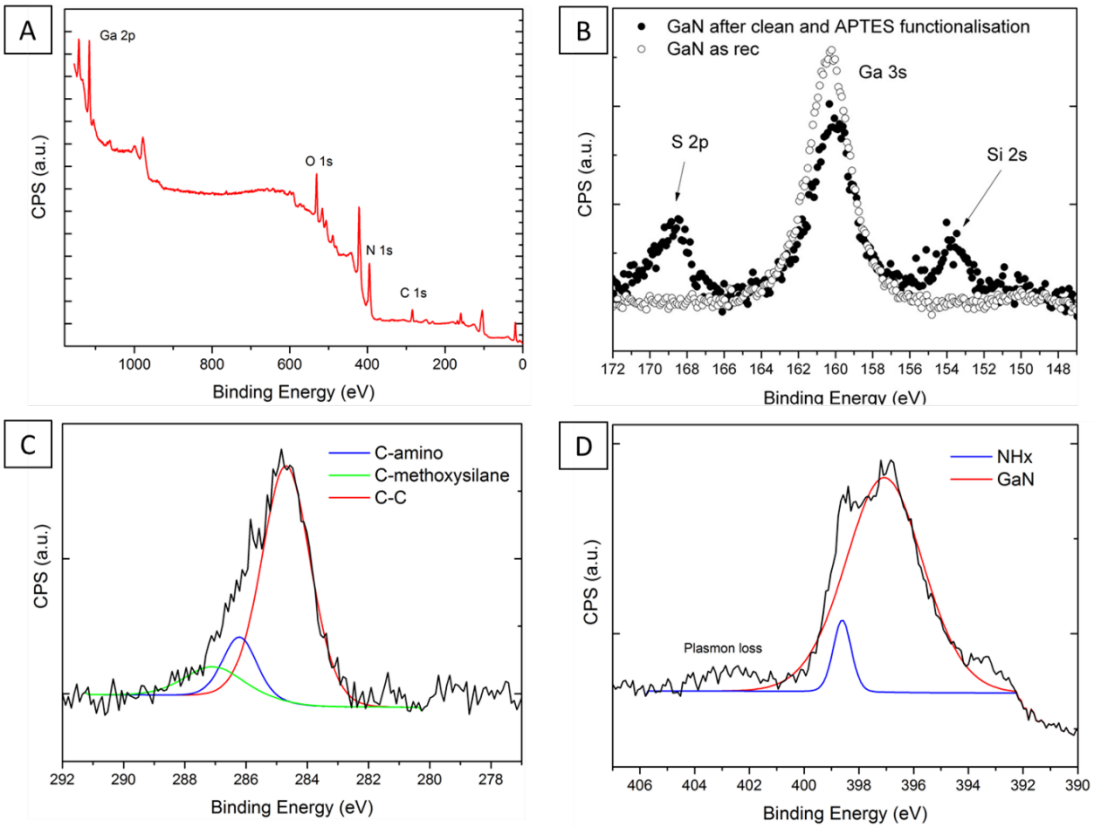


Figure 4.5: *XPS of an APTES-functionalised GaN film showing (a) a survey spectrum of the functionalised surface with main peaks highlighted, (b) core level Ga 3s peaks as well as S 2p and Si 2s before and after functionalisation, (c) core level C 1s peaks with deconvoluted components and (d) core level N 1s peak with the deconvoluted components arising from GaN and NH_x groups of the APTES molecule.*

The thickness of the organosilicon layer formed by the APTES molecules was estimated using XPS data and following a method originally defined by Cumpson[36], as shown in equation 4.1:

$$\ln\left(\frac{I_0 S_0}{I_s S_s}\right) - \left(\frac{\lambda_0}{\lambda_s}\right)\frac{1}{\lambda_0 \cos\theta} - \ln 2 = \ln\sinh\left(\frac{t}{2\lambda_0 \cos\theta}\right) \qquad (4.1)$$

where I_0 and I_s represent the respective measured peak intensities of the overlayer (APTES layer) and substrate peaks in arbitrary units, S_0 and S_s refer to the unitless relative sensitivity factors for the overlayer and the substrate respectively, with λ_0 and λ_s referring to the attenuation lengths of electrons in the overlayer and substrate in nm.

θ is the emission angle with respect to the surface normal. To minimise the effect of potential errors arising from surface roughness and inelastic scattering a photon emission angle of 35° was used in conjunction with a 90° take-off angle with respect to the sample normal. The peak intensity of the overlayer peak, I_o, and the peak intensity of the substrate peak, I_s, were determined using CasaXPS software after automatic transmission correction. The relative sensitivity factors for the substrate peak S_s and the overlayer peak S_o were obtained from the database in the XPS instrument acquisition software and manually inputted into the data processing software in order to scale the two peaks, *i.e.* substrate and overlayer. The attenuation length of photoelectrons in the overlayer, λ_o, was estimated using the NIST Electron Effective Attenuation Length database[37] to be 4.2 ± 0.4 nm for the Si *2s* component. The surface was thoroughly cleaned by prolonged sonication in anhydrous solvents prior to characterisation to remove all physisorbed species prior to analysis to minimise contributions from contaminants to the overlayer thickness. The thickness of the overlayer was calculated to be 1.1 ± 0.2 nm. As the length of a full APTES molecule is *ca*. 0.8 nm, it appears that there is a little more than a monolayer of the molecule on the surface. This correlates with the AFM micrographs (**Figure 4.3 (c)**) showing agglomeration at the surface as this would lead to an increase in the amount of silane deposited on the substrate.

4.3.2 Dopant profiling

Based on the AFM surface analysis (**Figure 4.4**) and on the capping studies carried out for Ge MLD (see **Chapter 3**), it was decided to use a capping layer to prevent any surface degradation and in order to maximise the amount of dopant delivery in the sample. Undoped GaN substrates were functionalised, capped with 100 nm of SiO_2,

annealed and then the cap was removed. The samples were then capped with 10 nm of Al_2O_3 which acts as an artificial barrier preventing sputtering of analytes during time-of-flight secondary ion mass spectrometry (TOF-SIMS) analysis thus avoiding the common artificial increase of analyte concentration seen in the first few nanometres of a SIMS scan. Al_2O_3 was chosen to prevent any Si signal overlap that might occur if a SiO_2 cap was going to be used. SIMS analysis of the samples was undertaken in collaboration with Dr. Jean-Paul Barnes of CEA-Leti as part of the ASCENT European Nanoelectronics Access program. For the SIMS analysis, annealing temperatures of 300, 600 and 900 °C were used with annealing times of 1 and 100s (see **Table 4.4**). Three *in-situ* Si-doped ($N_d = 3 \times 10^{18}$ at/cm^3) samples were also submitted: one sample was a calibration reference for the Si signal, one sample was capped with 100 nm of SiO_2, annealed at 700 °C for 1s and the cap was stripped in order to check for Si diffusion originating from the cap, and one sample was just annealed at 700 °C for 1s to see if the dopant profile would be affected by the thermal budget applied.

Figure 4.6(a) shows depth profiling of Si concentrations (at/cm^3) obtained from SIMS analysis for the samples. Data from the first 10 nm of each spectrum has been removed, due to the Al_2O_3 cap. Si had diffused into all of the samples; the highest Si concentration and dose, *i.e.* the area under the SIMS curve from 0 to 150 µm, were achieved for samples annealed at 600 °C for 1 s, with values of 4×10^{20} at/cm^3 and 10^{15} at/cm^2 respectively; the rest of the samples showed Si doses ranging from 2×10^{12} at/cm^2 for 300 °C/1 s, up to 10^{13} at/cm^2 for a 900 °C/1 s anneal. The theoretical maximum dose for a single monolayer where a silane group binds to three OH groups on the surface is *ca*. 3×10^{14} at/cm^2 [38]. As XPS data suggests that there is a little more than a single monolayer covering the surface of the GaN samples, it appears that

incomplete diffusion has occurred, with some Si possibly out-diffusing in the SiO_2 during the annealing step.[39] When compared with the chemical concentration values for the rest of the samples and considering that Hall measurement showed a dose value in line with the other samples (see **Table 4.2**), the SIMS data for this particular sample is likely an outlier. Moreover, the 300 °C/100 s sample could not be measured.

Table 4.4: *Matrix of experiments submitted for SIMS analysis to CEA-Leti with data extracted. The surface concentration was taken at the 10 nm depth to exclude the Al_2O_3 and the artificial dopant increase. The dose was extracted by integration of the SIMS curve from 0.1 to 150 nm, and the diffusivity was calculated following* ***Equation 4.2.***

Sample	Anneal Temperature (°C)	Anneal Time (s)	SIMS Surface Concentration (at/cm^3)	SIMS Dose (at/cm^2)	Diffusivity (cm^2/s)
D01	300	1	4.0×10^{18}	2.4×10^{12}	2.7×10^{-13}
D02	300	100	Sample broken		
D03	600	1	4.2×10^{20}	1.1×10^{15}	4.9×10^{-12}
D04	600	100	2.5×10^{18}	2.5×10^{12}	7.5×10^{-15}
D05	900	1	2.4×10^{19}	1.3×10^{13}	2.3×10^{-13}
D06	900	100	3.4×10^{18}	5.4×10^{12}	2.0×10^{-14}

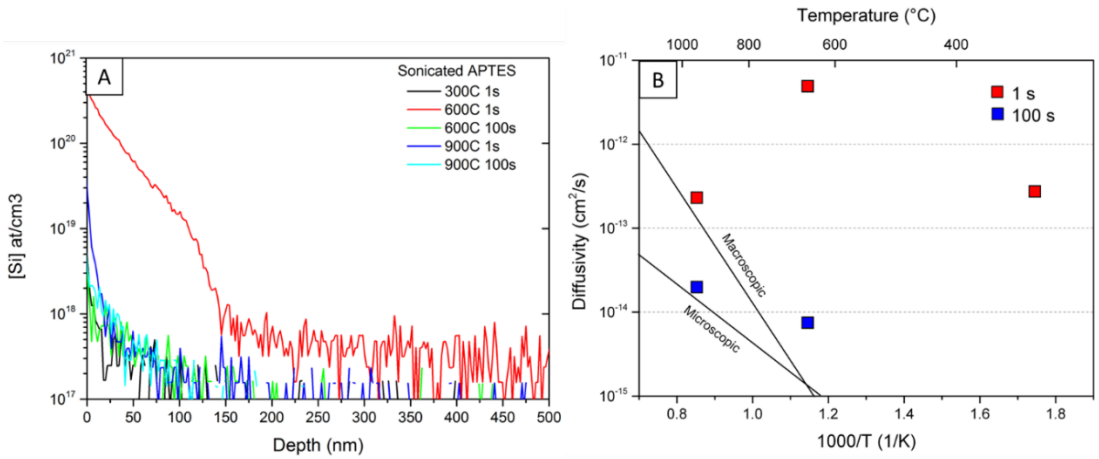


Figure 4.6: *(a) SIMS analysis of the GaN samples and (b) diffusivity plot with values extracted from the SIMS plots. The fast and slow diffusions regimes have been taken from Jakiela et al.*[40]

Diffusion constants for Si in the GaN films were extracted from the SIMS data using **Equation 4.2**:

$$D = \left(\frac{Q_{(t)}}{2C_s}\sqrt{\pi}\right)^2 \frac{1}{t} \qquad (4.2)$$

where $Q_{(t)}$ is the calculated dose in at/cm^3, C_s is the surface carrier concentration at 10 nm depth in at/cm^2 and t is the annealing time in seconds. These calculated values were then plotted against literature values, as shown in **Figure 4.6(b)**. The diffusivity values calculated, except for the outlier of the 600 °C/1s run, are dependent on the carrier concentration and therefore confirm that extrinsic diffusion of Si in GaN is occurring, further confirmed by the low diffusivity value of Si in GaN at 810 °C of 3.5×10^{-18}cm^2/s.[41] The result is also in line with other MLD reports which have shown that introduced dopants have displayed diffusivity in the extrinsic regime, where the dopant concentration was above the intrinsic carrier concentration with concentration dependent diffusion coefficients[21].

Moreover, the calculated diffusivity values appear to be time dependent at constant temperature, decreasing with time. This time dependency might be due to the inhibition of a "slow" diffusion mechanism when the annealing time is kept short; the "slow" mechanism is then activated when annealing for longer times, leading to an increase in the diffusion constant. Previous literature reports[40] suggest that the slow diffusion mechanism is driven by microscopic diffusion where Si employs Ga vacancies and fast diffusion is driven by a macroscopic mechanism in which the Si diffuses by grain boundaries or dislocations. Capping layers have also been shown[40] to promote slow diffusion over fast diffusion when annealing conditions are kept constant. This result suggests that for GaN where shallow doping is required, *e.g.* good contact formation, no caps and short anneals are preferred, perhaps by employing more advanced techniques such as laser annealing or flash lamp annealing. On the other hand, when deep and box-shaped profiles are required, *e.g.* for optical applications, conventional annealing such as RTA or furnace anneal should be used in conjunction with a capping layer.

Figure 4.7 shows the SIMS Si depth-profile for the three n-doped control samples sent for calibration and to evaluate the potential effect that the annealing and SiO_2 cap could have on the Si signal. From the three spectra, it is clear that the doping profile is unchanged for all 3 conditions (as received, capped and annealed at 700 °C for 1s and just annealed at 700 °C for 1s) therefore the Si signal for the functionalised samples is coming from in-diffused dopants.

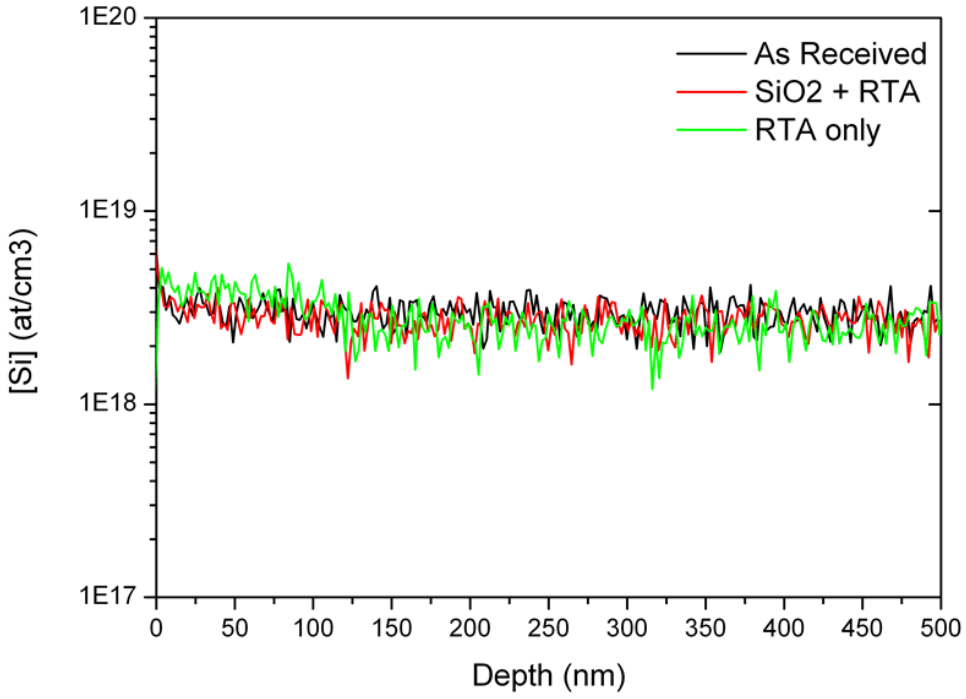


Figure 4.7: *SIMS analysis of the three control doped samples used to decouple the effect of the capping and the anneal on the Si levels.*

Hall effect measurements were also performed on all samples to quantify the active dopant concentration and determine the activation efficiency of the MLD process. **Table 4.5** shows dose values extracted from the SIMS measurement, which represent the total Si concentration (at/cm^3) in each sample, compared to the Hall effect measurement, which detects only the active dopants in the sample. The data show how the total activated dose for all samples was *ca.* 1×10^{13} at/cm^2 with a good match between the SIMS extrapolated doses and the Hall doses.

***Table 4.5**: Doping data extracted from SIMS and Hall effect measurements.*

Annealing Temperature / °C (Time, sec)	SIMS Dose (at/cm^2)	Hall effect Dose (at/cm^2)	Chemical conc. SIMS (at/cm^3)	μ_e (cm^2/V·s)
300 (1s)	2.4×10^{12}	4.0×10^{9}	4.0×10^{18}	34.6
600 (1 s)	1.1×10^{15}	8.0×10^{12}	4.2×10^{20}	4.6
600 (100 s)	2.5×10^{12}	1.2×10^{13}	2.5×10^{18}	4.7
900 (1 s)	1.3×10^{13}	2.0×10^{13}	2.4×10^{19}	3.6
900 (100 s)	5.4×10^{12}	1.3×10^{13}	3.4×10^{18}	4.6

The mismatch between some of the results can be attributed to error arising from both set of measurements. As mentioned before, the SIMS measurement for the 600 °C/1 s sample was considered an outlier due to the diffusivity value and carrier concentration not being in line with the other samples. Moreover, as already discussed in **Chapter 2, Section 2.2.10**, the GaN samples used for Hall measurement did not satisfy all the conditions for optimal Hall measurements, as the area of the contacts were not at least one order of magnitude smaller than the sample area; leading to a degree of error in the resistivity and Hall effect measurements in the order of D/L, where D is the average contact diameter and L is the distance between the contacts[42–44]. The electron mobility (μ_e) values of the Si-doped GaN films, calculated from Hall measurements and displayed in **Table 4.5**, are in good agreement with each other but are lower than the expected values for GaN[45], *i.e.* between 135 cm^2/V s at 300 K for a Si concentration of 2×10^{19} at/cm^3 and 369 cm^2/V s at 300 K for a Si concentration of 1×10^{17} at/cm^3 . This difference can be explained both by the non-uniform doping profile of the MLD method, considering that the Hall effect measurement assumes a uniform profile throughout the thickness of the sample, and from scattering effects arising both from impurities being introduced by the diffusion process, *i.e.* C and O, see **Figure 4.8(a)**.

Surface states[46–48] which are related to dangling bonds, impurities, surface reconstruction or random stress on the surfaces of the GaN films can also influence the electron mobility data obtained. Moreover, there have been reports on the correlation between C impurities and mobility collapse in Si-doped GaN which might also explain the low mobility data obtained due to the C introduced in the film[49]. As already discussed, future experiments should be aimed at improving the reaction as a whole, both by using C and O free precursors as well as by employing different surface preparation techniques which could reduce the amount of surface states[50].

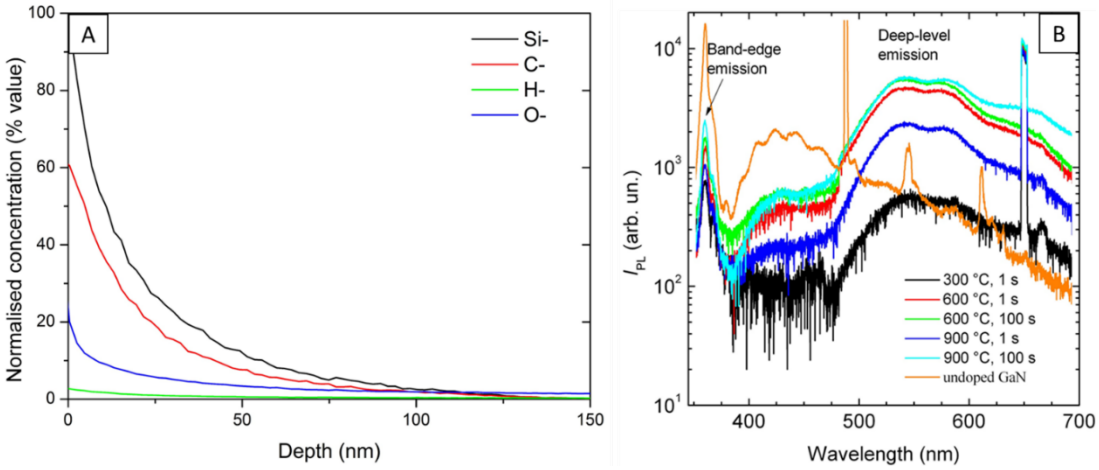


Figure 4.8: *(a) TOF-SIMS plot of Si, C, H and O, outlining how impurities from the dopant molecules are introduced into the sample after annealing and (b) Photoluminescence data from of Si-doped GaN samples*

Figure 4.8(b) displays photoluminescence data collected on the Si-doped GaN samples after SIMS analysis. The data demonstrates the presence of impurities in the samples after MLD treatment due to deep level (DL) yellow emission, starting at a wavelength of around 475 nm which is absent from the as received undoped samples. The emission can be attributed to either active Si atom diffusion into the GaN films from the surface, to non-radiative centres arising from dopant clustering and more likely, diffusion of C and O into the GaN lattice which act as recombination centres

not participating in electron exchanges[51,52]. The SIMS data shown in **Figure 4.8(a)** also suggests that both C and O diffuse into the GaN lattice upon annealing. Therefore, the efficiency of doping GaN films with Si using this approach might be improved by employing molecules with a smaller carbon skeleton, *e.g.* trimethoxysilane, vinyltrimethoxysilane, methyltrimethoxysilane, thus reducing the total amount of carbon being deposited on the surface and inside the films. In addition, carrying out the reaction in inert environment, *e.g.* under a N_2 atmosphere, should help reduce the amount of O_2 being adsorbed into the films.

4.4 Conclusions

MLD of GaN could allow Si doping concentrations on par with those achieved with conventional *in-situ* doping methods but with the potential of preventing parasitic SiN growth which occurs in MOCVD reactors when Si process gases are utilised for doping. By doping GaN outside of a reactor, it could also be possible to prevent strain build-up in films which can happen when a high concentration of dopant is introduced during growth. Moreover, in-diffusion doping would be useful for nanostructures that require selective area doping; by employing techniques such as UV photopatterning it has already been shown that it is possible to functionalise a pre-determined area of a surface[20]. The data reported in this Chapter has shown that, as a proof of concept, it is possible to dope GaN films outside of a reactor by in-diffusing Si from a self-assembled monolayer on the surface. The highest Si concentration achieved was 2×10^{19} at/cm^3, with optimal dopant activation and minimal impact to the surface quality. However, in-diffusion through MLD is still challenging due to the very low electron mobility likely caused by the C and O impurities that are driven in the substrate during the process. By using different dopant precursors, it could be possible to maximise the

active dopant content in the films without introducing such non-radiative impurities, thus achieving better electrical properties.

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Chapter 5

Oxide Removal and Stabilisation of Bismuth Thin Films Through Chemically Bound Thiol Layers

Some of the data in this Chapter has been published as part of peer reviewed articles in *RSC Advances*[1] and *Microelectronics Engineering*.[2] My contribution to the *RSC Advances* paper was sample preparation and functionalisation, data collection and analysis and the paper drafting. Thin films of Bi were supplied by the Jülich Research Centre, in Jülich, Germany .

Alessio Verni, G.; Long, B. Gity, F.; Lanius, M.; Schüffelgen, P.; Mussler, G.; Grützmacher, D.; Greer, J.; Holmes, J. D., 'Oxide removal and stabilization of bismuth thin films through chemically bound thiol layers', *RSC Adv.*, **2018**, *8* (58), 33368-33373.

Gity, F.; Ansari, L.; König, C.; **Alessio Verni, G.**; Holmes, J. D.; Long, B.; Lanius, M.; Schüffelgen, P.; Mussler, G.; Grützmacher, D.; Greer, J. C., 'Metal-semimetal Schottky diode relying on quantum confinement', *Microelec. Eng.*, **2018**, *195*, 21-25.

5.1 Abstract

Semiconductor surface passivation and stabilisation is of paramount importance as it allows for processing under ambient conditions, thus simplifying the fabrication flow and ultimately lowering the cost of device manufacture. Additionally, a common problem in semiconductor processing is unplanned downtime, which can lead to oxidation of non-passivated semiconductor and metallic surfaces. Extensive surface passivation methods have been developed over the past decade for the main semiconductors used in industry, *i.e.* Si, Ge, III-Vs, but as alternative materials such as Bi (a semimetal) are being explored for future applications, new surface stabilisation chemistries are required. This Chapter describes the surface passivation of bismuth thin films, grown by molecular beam epitaxy (MBE), using an ambient wet chemistry method. Alkanethiol molecules were used both to dissolve bismuth oxides from the surface of Bi thin films, through a catalytic reaction, and subsequently passivate these 'cleaned' surfaces. The organic thiol layer formed on the surface of the Bi films showed resistance to complete reoxidation for up to 10 days. Although complete removal of bismuth oxide was not possible, due to the high reactivity of the Bi surface, the data reported highlights the potential use of organic molecules in the passivation of Bi thin films.

5.2 Introduction

Bulk Bi has always been a material of interest, due to its extremely high electron mobility, low effective mass and high anisotropy in the Fermi level, which leads to high magnetoresistance[3–5]. Moreover, Bi is a good example of a material where differences exist between its surface and bulk properties. In particular, the surface of Bi has more metallic characteristics compared to its bulk, due to the existence of

electronic surface states which cross the Fermi level[6]. As a semimetal, Bi lies between a semiconductor and a metal; a small band-gap of 13.6 meV at 0 K exists between the L-point valence and conduction bands like in a semiconductor[7]. On the other hand, a small indirect overlap of the T-point valence band and the L-point conduction bands (38 and 98 meV at 2 and 300 K, respectively)[7] make bulk Bi a semimetal (**Figure 5.1**).

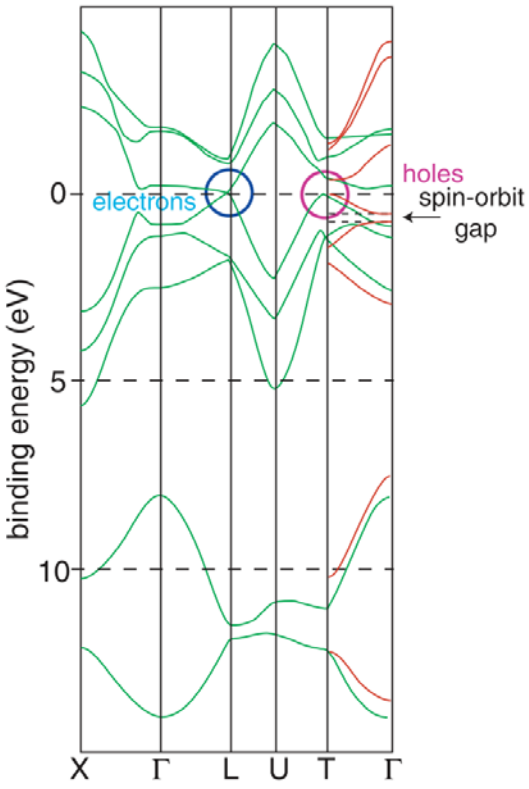


Figure 5.1: *Bulk band structure of Bi from tight-binding (green) and first-principle (red) calculations.*[8]

When the surface of Bi is metallic, it acts a pseudo-two-dimensional metal deposited on a semiconductor, *i.e.* bulk Bi[8]. The properties of bulk Bi are also radically altered by quantum size effects; quantum mechanics dictates that when particles with an effective de Broglie wavelength of λ_B are confined to structures with dimensions smaller or comparable to λ_B, interference effects and quantised states arise[9]. By achieving quantum confinement in nanoscale semimetals, such as Bi, it is possible to

get a semimetal-to-semiconductor transition as the physical size of the nanostructure becomes comparable to the de Broglie wavelengths of electrons and/or holes. Given the low Fermi energy of Bi and the small effective mass of its carriers (0.003 m_e)[10], the de Broglie wavelength in Bi is approximately 12 nm, which means that quantum confinement effects can potentially be observed for thin films or nanowire structures[8,11–14]. This form of band gap engineering can be exploited to form a transistor using a single element, in what is defined as a confinement modulated gap transistor (CMGT)[15]. In a CMGT, the semiconducting channel is formed by a nanowire or a quasi-two dimensional region which is placed between the bulk semi-metallic source and drain regions. By varying the cross section of the nanowire (or the thickness of the two dimensional region) it is possible to modulate the energy gap of the transistor, thus eliminating the need to dope the nanostructure, and use a single element to fabricate a transistor. Calculations by Ansari *et al.*[16] have shown that a Schottky junction can indeed be formed in a semimetal nanowire, *e.g.* Bi and Gity *et al.*[17] have then proceeded to fabricate a working hetero-dimensional rectifier consisting of a three dimensional (3D) semimetallic region abutting a thinner quasi-two dimensional (2D) semiconducting region, without the need to dope the structure to achieve near ideal diode behaviour.

However, the creation of a CMGT with Bi requires the formation of a metal-semimetal junction under vacuum, via a reactive ion etch step to prevent surface reoxidation. Gity *et al.*[2] showed in subsequent work that bismuth oxides form on Bi thin films upon contact with air. To retain its semiconducting behaviour, the research team had to strip away the oxide via Ar sputtering before proceeding to *in-vacuo* metallisation. An *in-situ* passivation cap would therefore be beneficial for such processing to protect the Bi surface from oxidising, allowing sample handling in air. However, the precursors used

during the capping process must be inert towards Bi, preventing oxidation but with enough etch contrast to Bi for easy removal if required.

The oxidation of bismuth thin films was first reported by Hapase *et al.*[18] as far back as 1967. Oxidation of Bi proceeds by diffusion of Bi ions from the bulk of the substrate through the oxide film [19], via a Wagner mechanism (**Figure 5.2**).

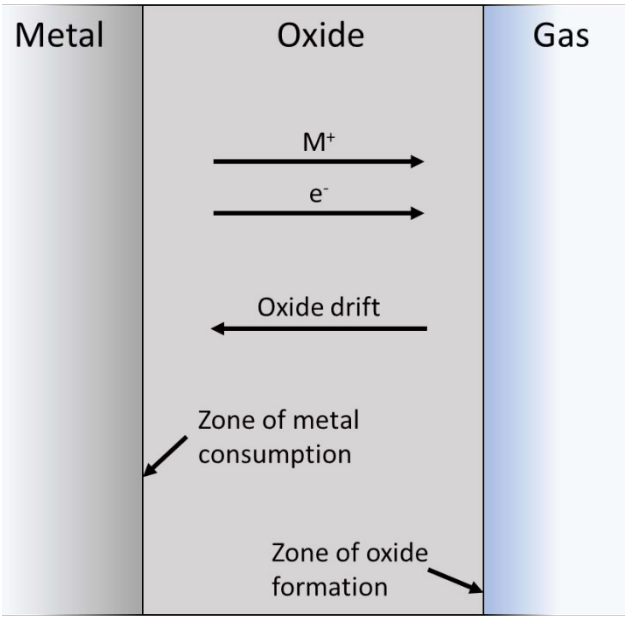


Figure 5.2: *Schematic of the Wagner diffusion mechanism of oxide formation; the oxide forms at the surface thanks to metal ions (M^+) diffusing from the metal bulk, through the oxide, all the way to the oxide-gas interface.*

Rather than oxygen diffusing to the metal-oxide interface and controlling oxide growth rate (such as in the case for SiO_2 growth on Si), the oxidation rate of a Wagner-type mechanism is determined by the ion transport from the metal-oxide interface to the oxide-gas interface, under the combined effects of concentration gradients and electric fields. The growth kinetics in most cases are controlled by the diffusive properties of the oxide.[20]

To further support this, studies by Komorita *et al.*[21] correlated the oxide thickness on the surface of Bi films, *X*, to Bi diffusion as shown in **Equation 5.1**:

$$X = \left[\frac{(C_{Bi}^{S} - C_{Bi}^{0})}{N_0 \rho} \cdot MDt\right]^{1/2} \quad (5.1)$$

Where C_{Bi}^{S} is the concentration of Bi at the Bi/Bi_2O_3 interface, $C_{Bi}^{0}$is the concentration of Bi near the surface of Bi_2O_3, N_0 is Avogadro's number, ρ is the density of Bi_2O_3, *M* is the molecular weight of Bi_2O_3, *D* is the diffusion coefficient of Bi and *t* is the time. The authors showed that first a metastable cubic crystal phase of the oxide forms on the surface, which then slowly evolves to a more stable phase either when heat is applied or over time[21]. In 1990 Puckrin *et al.*[22] compared the oxidation of bulk Bi and thin films using different spectroscopy techniques. In both cases, BiO was the first oxide to form on the surface of the samples, with a total thickness of roughly 8 monolayers (*ca*. 2 nm). Further exposure to air oxidation lead to the formation of Bi_2O_3, which then relates back with the studies of Hapase[18] and Komorita[21] who showed that B_2O_3 is the thermodynamically stable phase[23]. Despite these results which focused on bulk films, the oxidation behaviour of Bi thin films has not been studied extensively.

This Chapter describes oxide removal and subsequent passivation of Bi thin films by thiol molecules. While complete removal of the surface oxide was not achieved, due to the high surface reactivity of Bi towards atmospheric oxygen, data reveals that oxide removal is possible outside a vacuum. With further optimisation, the potential exists to apply this method developed to larger scale processing.

5.3 Results and Discussion

Figure 5.3 shows XPS scans of the Bi *4f* core level peaks for Bi films as received, after annealing the film at 180 °C for 3 hr, after treatment with 100 mM solution of 1-dodecanethiol and after combined anneal and subsequent thiol treatment without air exposure. The peaks at 156.5 and 161.8 eV are from Bi metal (*4f* 7/2 and 5/2 components respectively)[24], whereas the peaks at 158.6 and 163.4 eV[25] are from the Bi-X interactions (*4f* 7/2 and 5/2 components respectively); where X is a heteroatom (usually O). The XPS shows how thermal treatment by itself does not lead to any oxide reduction, as the two BiO_x components are not reduced. On the other hand, the thiol only treatment leads to a partial reduction in the oxygen content, as the metallic Bi peak increases in intensity. The combination of anneal and the thiol treatment without an air break in between, allows for a more dramatic reduction in the BiO_x component. The thermal treatment is likely removing any moisture adsorbed onto the surface, thus allowing for a more efficient reaction of the thiols with the substrate.

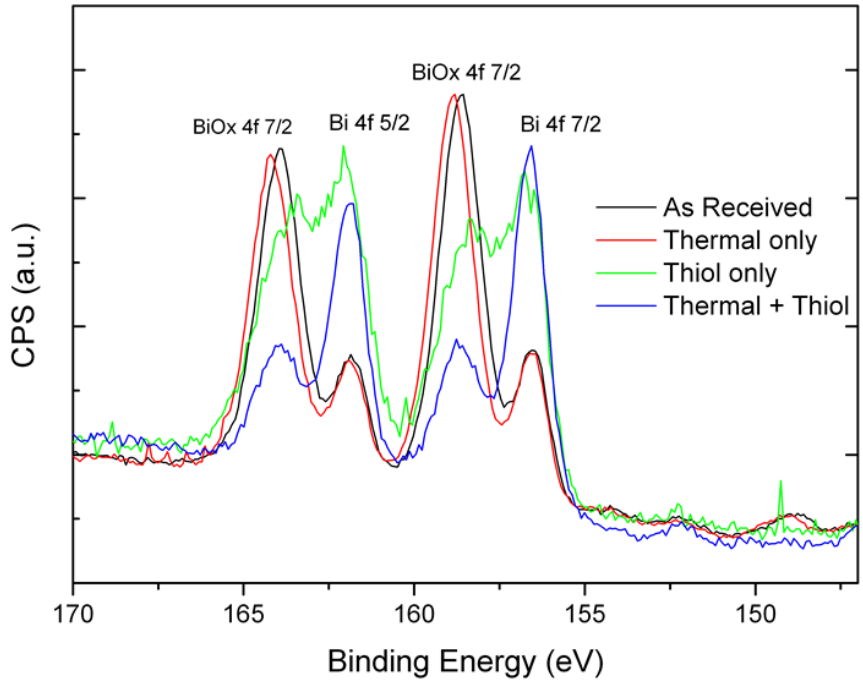


Figure 5.3: *Overlaid Bi 4f core level XPS spectra of as received Bi and after annealing and treatment with 1-dodecanethiol solution. Graphs have been normalised to the Bi* $4f_{7/2}$ *peak of the as-received sample to better show the oxide reduction effect.*

Figure 5.4 shows XPS scans of the Bi *4f* core level peaks for Bi films before and after reaction with different concentrations of 1-dodecanethiol solutions. **Table 5.1** shows the relative percentages of the peak areas of Bi metal and Bi-X for each of the 4*f* components. Treating the Bi films with thiols at a concentration of 1 mM did not significantly alter the intensities of the Bi-X peak considerably, as shown in **Figure 5.4** and **Table 5.1**. The 10 and 100 mM treatments, on the other hand, were clearly progressively more effective in increasing the intensity of the Bi metal component when compared to the as-received sample.

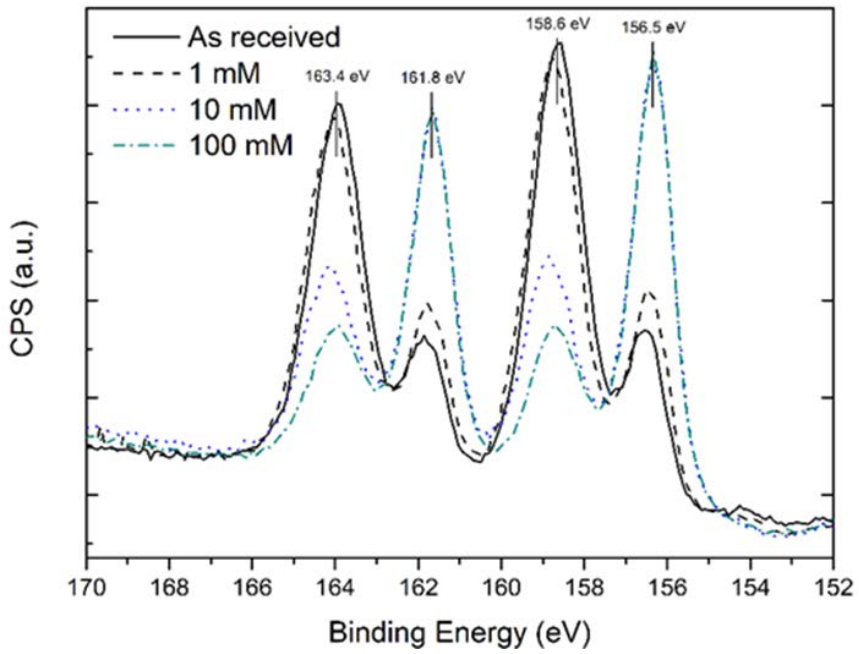


Figure 5.4: *Overlaid Bi 4f core level XPS spectra after reaction with 1-dodecanethiol solutions at different concentrations. Graphs have been normalised to the Bi $4f_{7/2}$ peak of the as-received sample to better show the oxide reduction effect.*

Table 5.1*: Percentages of XPS peak areas for elemental Bi and Bi-X for each Bi 4f core level component acquired on as-received and thiol-treated Bi thin films as well as as-received and thiol-treated Bi powder.*

Sample	**Bi $4f_{5/2}$ 161.8 eV**	**Bi $4f_{7/2}$ 156.5 eV**	**BiX $4f_{5/2}$ 163.4 eV**	**BiX $4f_{7/2}$ 158.6 eV**
Wafer as rec.	23.5		76.5	
Wafer + 1 mM thiol solution	28.0		72.0	
Wafer + 10 mM thiol solution	59.1		40.9	
Wafer + 100 mM thiol solution	64.9		35.1	
Wafer + 100 mM thiol + air exp.	57.5		42.5	
Powder as rec.	23.5		76.5	
Powder + 100 mM	45.6		54.4	

The XPS shoulder peaks at the peaks at 158.6 and 163.4 eV, while usually being associated with the Bi-O component of Bi_2O_3, can also be associated with a Bi-S component; in order to decouple the two components, we can compare the thickness of the total overlayer (oxide + thiol) and the thickness of just the oxide by following the method originally defined by Cumpson[26], see **Equation 5.2**. As the method cannot be used for more than one overlayer and to directly compare the thickness calculations, the overlayer was approximated as just the oxide Bi_2O_3,

$$\ln\left(\frac{I_0 S_0}{I_s S_s}\right) - \left(\frac{\lambda_0}{\lambda_s}\right)\frac{1}{\lambda_0 \cos\theta} - \ln 2 = \ln \sinh\left(\frac{t}{2\lambda_0 \cos\theta}\right) \quad (5.2)$$

where I_0 and I_s represent the respective measured peak intensities of the overlayer and substrate peaks, S_o and S_s refer to the relative sensitivity factors for the overlayer and the substrate respectively, with λ_o and λ_s referring to the attenuation lengths of electrons in the overlayer and substrate. θ is the emission angle with respect to the surface normal. To minimise the effect of potential errors arising from surface roughness and inelastic scattering a photon emission angle of 35° was used in conjunction with a 90° take-off angle with respect to the sample normal. The peak intensity of the overlayer peak, I_o, and the peak intensity of the substrate peak, I_s, were determined using CasaXPS software after a transmission correction. The relative sensitivity factors for the substrate peak S_s and the overlayer peak S_o were obtained from the database in the XPS instrument acquisition software and manually inputted into the data processing software to remove instrumental factors which may affect quantification. The method requires for the binding energy difference between the substrate and the overlayer peaks to be as little as possible. To calculate the thickness of the total overlayer (oxide+thiol), the Bi-X $4f_{7/2}$ shoulder at 158.6 eV was used as the overlayer peak and the Bi $4f_{7/2}$ peak at 156.5 eV as the substrate peak; to calculate

the thickness of the oxide the O *1s* Bi_2O_3 peak at 530.3 eV was used as the overlayer peak and the Bi $4d_{5/2}$ peak at 440.4 eV as the substrate peak. The attenuation length of photoelectrons in the overlayer, λ_o, was estimated using the NIST Electron Effective Attenuation Length database[27] to be 2.1±0.2 nm for the Bi *4f* component, and 1.7±0.2 nm for the Bi $4d_{5/2}$ component. The surface was thoroughly cleaned by prolonged sonication in anhydrous solvents prior to characterisation to remove all physisorbed species prior to analysis; to minimise contributions from contaminants to the overlayer thickness. The thickness of the total overlayer was found to be 0.95±0.10 nm whereas the thickness of the oxide is 0.43±0.05 nm. This discrepancy in thickness is likely due to S also bound to surface Bi atoms, thus leading to a higher intensity Bi *4f* shoulder peak, *i.e.* Bi-S and Bi-O. Moreover, TEM imaging of the as-received Bi films (see **Figure 5.5**) shows oxide layers of between 1.5 – 2 nm; therefore, oxide removal takes place as there has been a considerable reduction in the total oxide thickness.

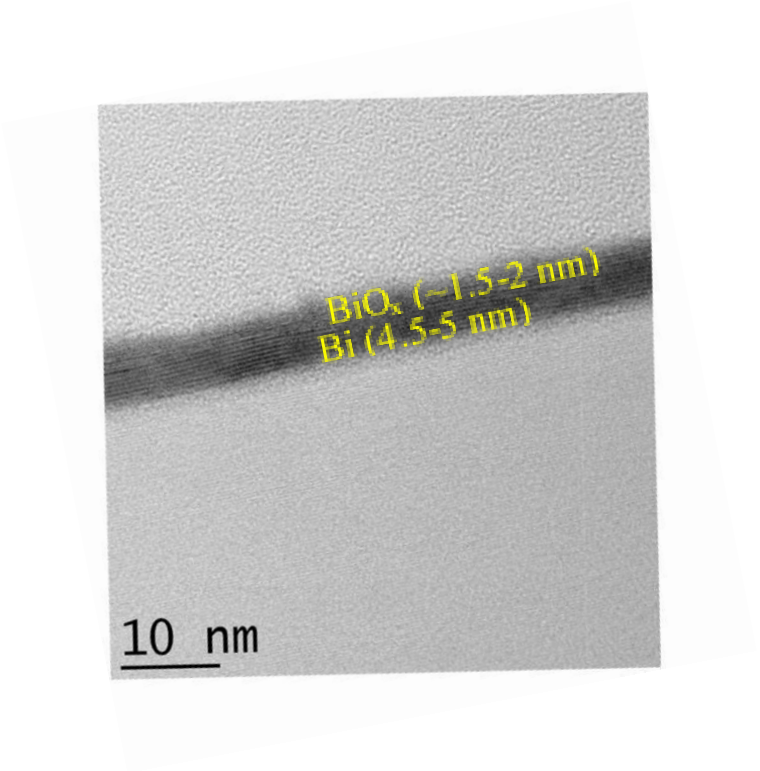


Figure 5.5: *High resolution TEM image of an MBE-grown Bi thin film showing the native Bi oxide).*[2]

Thiol-functionalised Bi thin films were left in air for up to 10 days and analysed by XPS to determine the extent of reoxidation with time. **Figure 5.6(a)** shows a comparison of the Bi *4f* core level peaks of the 100 mM functionalised samples measured after 0 hr, 1 hr, 2 days and 10 days of air exposure. XPS analysis showed that complete reoxidation of the functionalised Bi films did not occur; the small increase in the peaks at 158.6 and 163.4 eV[25] (Bi-X *4f* 7/2 and 5/2 components respectively) is likely due to partial oxidation of the exposed surface to wafer, due to non-continuity of the layer as shown by AFM (**Figure 5.7(c)**). Post functionalisation (**Figure 5.7(c)**) it is possible to see an increase in the RMS of the samples (0.79 nm to 2.30 nm) and the surface topography shows that the film is not fully closed and leaves some small areas of the underlying surface exposed to reoxidation.

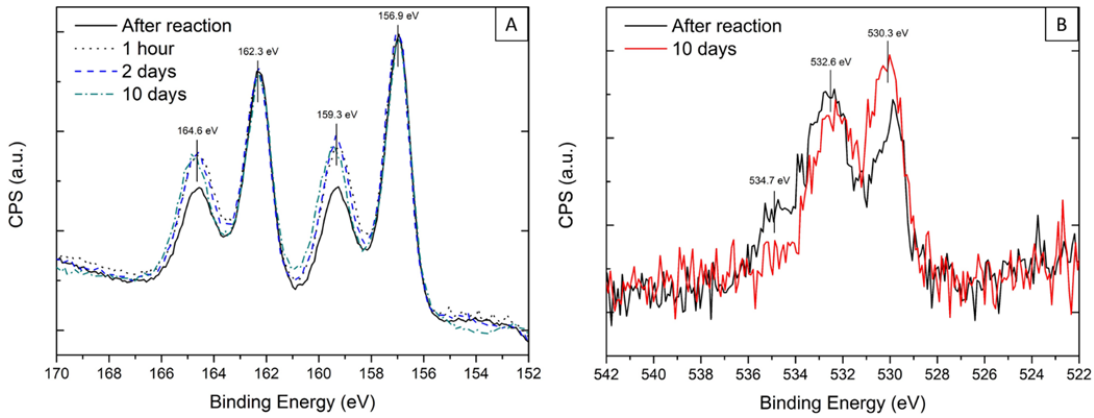


Figure 5.6: *(a) XPS Bi 4f core level spectra from thiol-functionalised Bi thin films before and after exposure to air. Spectra have been normalised to the Bi $4f_{7/2}$ peak of the sample after reaction to better outline the reoxidation process. (b) XPS O 1s core level spectra taken from thiol-functionalised Bi films before and after reoxidation with main component peaks being highlighted.*

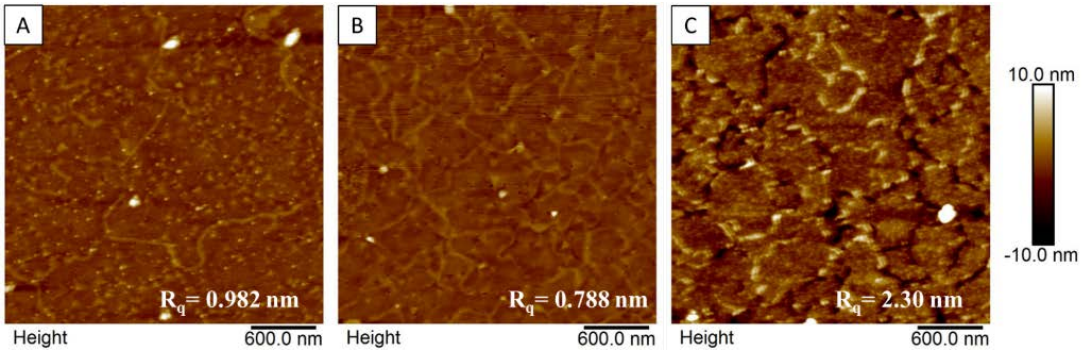


Figure 5.7: *AFM images and RMS roughness values of (a) as received Bi film on Si substrates, (b) Bi films after annealing at 180 °C for 1 hr, (c) annealed Bi films after functionalisation with 1-dodecanethiol. Note in image (c) the non-continuity of the film which causes some areas of the wafer to reoxidise.*

As further proof, **Figure 5.6(b)** shows XPS O *1s* spectra of thiol-functionalised Bi thin films before and after exposure to air. The surface Bi_2O_3 peak at 530.3 eV[28] increases in intensity after air exposure, further proof that partial surface reoxidation does occur. This increase is accompanied by a general decrease in the intensity of two peaks at 532.6 eV[29,30] and 534.7 eV[31] belonging to O-H/S-O and H_2O respectively; surface hydroxyl groups arise from H-termination of the surface oxide, sulphoxide groups from oxidation of the surface-bound and adsorbed thiol groups, and the water from adsorption on the layer of the reaction by-product due to hydrophilicity of the outer facing thiol group.[32,33]

Figure 5.8(a) shows an ATR-FTIR scan of the Bi wafer surface before and after the functionalisation process. The solvent-cleaned as-received Bi thin film wafer presents vibrations only due to adventitious carbon adsorbed on the surface. After functionalisation and air exposure, multiple vibrations were observed at 2993 and 2909 cm^{-1}, arising from C-H and vibrations from the aliphatic carbon chains of the thiol molecules. In the fingerprint region between 1500 – 750 cm^{-1} there are the two peaks for asymmetric stretching of SO_2 at 1367 cm^{-1} and 1174 cm^{-1} and one peak for the symmetric stretching at 1083 cm^{-1}.[34] This data suggests that the outer facing thiols

from the second adsorbed layer, due to the oxidative environment created by the Bi_2O_3/Bi pair,[35,36] are readily oxidised to their sulphonic acid equivalents (see **Figure 5.8(b)**). It has already been shown that surface bound thiols progressively oxidise to sulphonic acids in the presence of strong oxidative environments.[37,38] The Bi(III) catalyses the formation of a disulphide bond between two 1-dodecanethiol molecules, similarly to what has already been observed for copper[39] with water as a by-product. As the sample/solution system is kept under N_2, the oxide layer cannot form again and is consumed.[35]

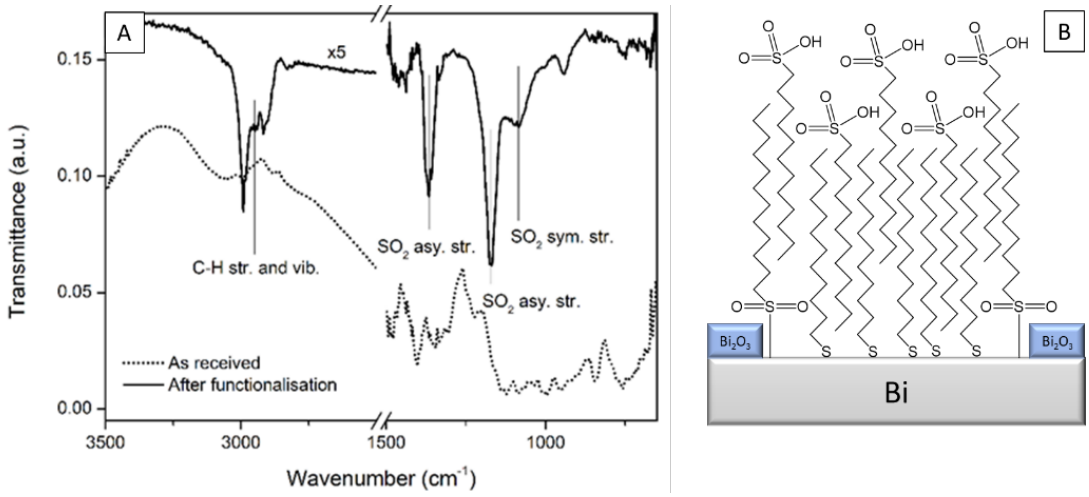


Figure 5.8: *(a) IR spectra of the surface of a Bi thin film before and after surface functionalisation and (b) schematic of a functionalised Bi surface after exposure to air.*

Similar "bilayer" structures formed with long alkyl chain molecules can be easily formed both on nanoparticles[40,41] and on 2-D films[33,42] when using a polar solvent. Moreover, a previous study on silver colloidal nanoparticles[43] has shown that an excess of precursor molecules can lead to bilayer structures which in turn lead to an increase in the air stability of films. In a similar fashion, Cu films and powders functionalised with excess thiols, leads to multilayer formation of self-assembled

copper thiolate layers.[39] The formation of a thiol bilayer structure on the Bi thin films is further corroborated by XPS thickness measurements which have quantified a surface carbon layer thickness of 4.3 ± 0.5 nm, which equates to about 2.7 layers of 1-dodecanethiol. This bilayer configuration delays the surface oxidation of the Bi films in air. In contrast, an oxide-free Bi metal surface obtained by reactive ion etching (RIE), would completely reoxidise in air in less than 2 min.

Oxide removal and passivation of the Bi films with thiols likely proceeds due to a sulphur oxidation reaction catalysed by surface Bi_2O_3. Bi(III) catalyses the formation of a disulphide bond between two 1-dodecanethiol molecules and, as the sample/solution system is kept under N_2, the oxide layer cannot form again and is consumed[35]. Once the bare Bi surface is exposed, the thiol passivates the surface thanks to the higher thermodynamic stability of Bi-S bonds over Bi-O bonds[44,45]. This theory is supported by experiments carried out on Bi powder where the as-received powder was annealed, similarly to the films, and submerged in 1-dodecanethiol solutions made in isopropyl alcohol (IPA) and hexane. After 3 hr, the solution changed from colourless to yellow, and a precipitate was formed (**Figure 5.9**).



Figure 5.9: *Photos of (a) a flask containing Bi powder and a 100 mM solution of 1-dodecanethiol in IPA, under N_2, (b) a sample vial containing Bi powder and 100 mM solution of 1-dodecanethiol in IPA, in air.*

The precipitate was collected and dissolved in deuterated chloroform ($CDCl_3$) for NMR analysis. An NMR of the as received 1-dodecanethiol was also collected and used for comparison to check for the presence of the starting material at the end of the reaction. **Figure 5.10** shows stacked NMR scans for the as-received 1-dodecanethiol. A quartet of resonance peaks at 2.51 ppm (J = 7.33 Hz) arise from the α-methylene of the thiol group. The β-methylene and the thiol proton resonate at 1.60 ppm (quintet, J = 7.58 Hz) and 1.39 ppm (unresolved multiplet) respectively, the methyl of the C12 carbon is found at 0.87 ppm (triplet, J = 6.90 Hz) and the remaining protons on C3-C11 form an unresolved multiplet at 1.26 ppm[46]. For the NMR of the reaction product the two α-methylene groups of the disulphide moiety resonate as a triplet at 2.68 ppm (J = 7.35 Hz); the two β-methylene groups resonate at 1.67 ppm (quintet, J = 7.31 Hz) and between 1.26 and 1.39 ppm there is an unresolved multiplet formed by the protons on the two alkyl chains. The remaining two methyls at the end of the chains resonate at 0.88 ppm (triplet, J = 6.70 Hz)[47].

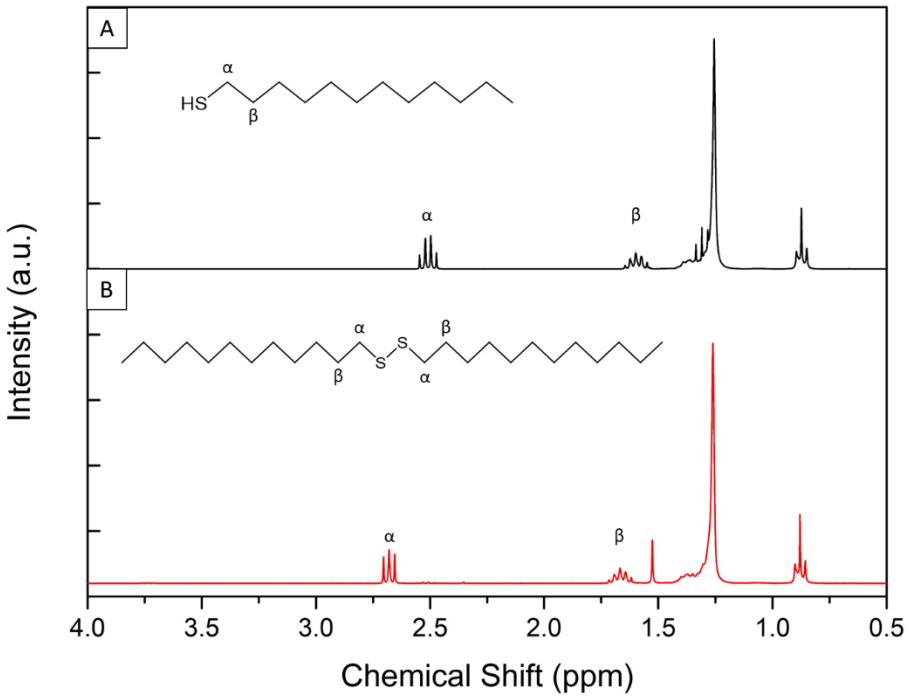


Figure 5.10: *NMR spectra of (a) the as-received 1-dodecanethiol used for the reaction and (b) the dodecyldisulphide product found after reacting 1-dodecanethiol solution with Bi powder.*

Based on the NMR data, 1-dodecanethiol was completely converted to disulphide in the presence of the Bi powder, without the formation of impurities; no thiol was found in the NMR spectrum of the final product, *i.e.* the distinctive α-methylene quartet absent. The reaction carried out with the Bi powder in air can proceed indefinitely until all the thiol starting material is oxidised; the powder is in fact allowed to reoxidise, unlike under N_2, thus catalysing the reaction. No precipitate or colour change of the solution was observed when functionalising the Bi films with thiols, probably due to the much smaller surface area of the films compared to the powder samples and the small quantity of thiol used in the experiments. Also, at a thiol concentration of 10 mM only partial oxide reduction on the Bi films was observed (when compared to higher concentrations, see **Figure 5.4**), probably due to most of

the thiol molecules in solution becoming oxidised upon removing the outer oxide layer, leaving only few available molecules to actually bind to the surface. Using thiol concentrations higher than 100 mM however lead to visible corrosion of the sample surface and therefore was considered not a viable solution to further improve oxide removal.

Bi powder samples, as-received and thiol-functionalised, were also analysed by XPS (**Figure 5.11**) to determine the extent of surface oxide. Although surface oxide reduction was not as dramatic as for the Bi thin film samples, the total surface oxide reduced by 22 % (see **Table 5.1**). The oxide reduction in the Bi powders was less than with the Bi films (where the surface oxide reduction was 41 %) due to the higher surface area of the powders and the difficulty in completely covering the surface of the powdered samples with the thiol solution due to its poor dispersity in the solvent.

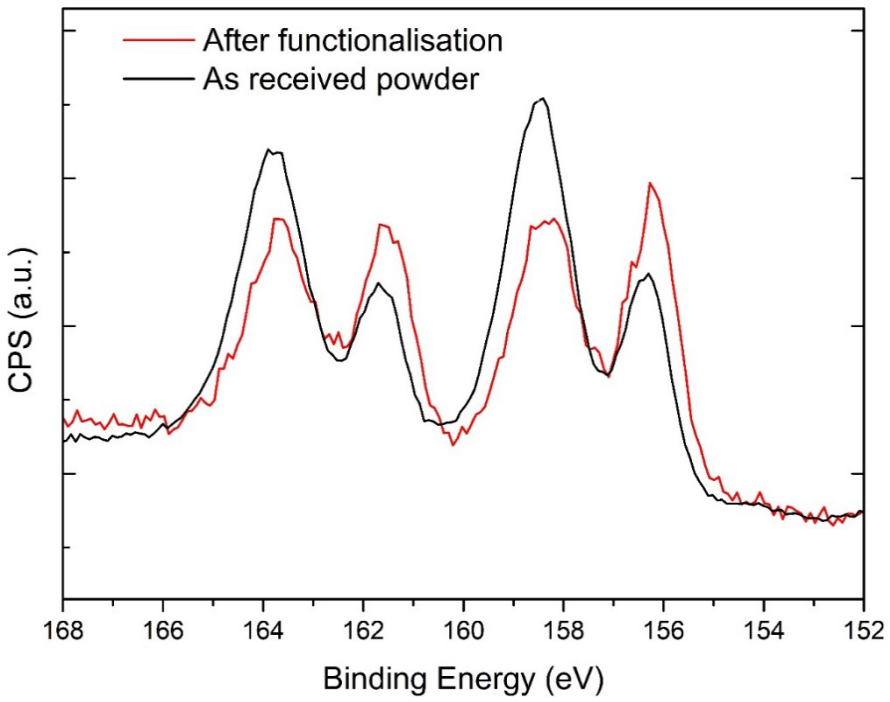


Figure 5.11: *Overlaid XPS spectra of Bi 4f core level of Bi powder before and after reaction with 100 mM 1-dodecanethiol in IPA. Spectra have been normalised to the minimum of the as-received sample to highlight the oxide reduction effect.*

5.4 Conclusions

In conclusion, I have shown that oxide removal and stabilisation of nanoscale Bi thin film is possible outside of a vacuum using long chain alkyl thiols. Complete surface reoxidation was prevented for up to 10 days, as opposed to less than 2 min for unpassivated surfaces. Oxide removal takes place due to a catalytic reaction between bismuth oxide and 1-dodecanethiol. Once the oxide has been removed the thiol groups passivate the bare Bi surface. While there is a basic understanding of the possible mechanisms behind the passivation reaction and oxidation resistance, there is still potential for improvement, for example by employing different length thiol molecules or by coating the surface with an inorganic protective layer once the oxide has been removed by chemical methods.

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Chapter 6

Conclusions and Future Work

6.1 Conclusions

The evolution of current logic devices is constantly requiring materials and processes which can lead to better performances, higher device reliability and more energy efficiency. Integration in current manufacturing processes is of paramount importance as current chip architectures require hundreds of subsequent steps that are closely interlinked with each other. Moreover, as the source-drain and channel dimensions are scaling down towards atomic layer scale and device complexity increases to more advanced three-dimensional geometries, it will be of the utmost importance to be able to functionalise and dope these materials in the most controllable way possible, while at the same time eliminating any possible source of defect introduction.

Surface functionalisation with organic monolayers will become increasingly more vital as the surface to volume ratio of current transistors keeps increasing. Materials such as Ge, SiGe and III-V compounds are starting to replace Si as a channel material, due to their higher carrier mobilities, leading to lower power consumption for the equivalent performance of their Si-counterparts. 2D transition metal dichalcogenides (TMDs) are also being explored as the next generation channel materials, due to their structural stability, direct bandgap and electron mobility comparable to Si. However, these materials introduce a whole new set of challenges when it comes to doping and functionalisation. Application of molecular layer doping (MLD) to next generation architectures and new materials will require a coordinated effort from industrial partners, device physicist, chemists and chemical suppliers as the demand from the logic industry for new solutions is constantly increasing.

Chapter 1 gave an overview of the transistor evolution over the last few years and how MLD has been applied to both group IV and group III-V materials. A summary of alternative channel materials has also been included, with the focus on Ge and GaN,

their surface chemistry and functionalisation. Finally, a summary has been made of Bi, its interesting electrical properties as well as its oxide and surface functionalisation.

Chapter 2 outlined the experimental methods used to functionalise Ge and GaN surfaces with dopant-containing precursors, as well as the passivation procedure of Bi developed using organothiol self-assembled monolayers (SAMs). The synthesis of custom-designed molecules was also described. NMR was used to determine the purity of the molecules prior to their use in the functionalisation process. Characterisation methods for coupons included XPS, AFM, FTIR, SIMS, ECV, Hall effect measurements and PL spectroscopy. For nanostructured devices, TEM was used to monitor the nanowire morphology and to verify that there was no damage caused to the crystal lattice of the test-structures throughout the MLD process. The fabrication of the nanostructured devices by EBL and their testing procedure was also outlined. The substrate growth parameters for the GaN and Bi substrates used for this work have also been described.

Chapter 3 described the first application of organo-arsenic and organo-phosphorous monolayers on Ge for MLD. A custom-synthesised organo-arsenic molecule and a commercially available organo-phosphorous precursor were used to successfully functionalise planar Ge substrates and GOI nanowire devices ranging from 1000 to 20 nm. High dopant concentrations approaching 9×10^{18} at/cm^3 for P and 6×10^{18} at/cm^3 for As were achieved for bulk Ge. The resistivity of MLD P-doped GOI nanowires was also decreased by up to five orders of magnitude using the MLD technique when compared with the undoped nanowires. TEM analysis showed that the MLD process had no effect on the crystallinity of the nanowires and no visible damage or defects were observed, further proof that the MLD process is more than suitable for non-destructive nanoscale doping.

Chapter 4 expanded upon the work reported in Chapter 3 by applying MLD to GaN in order to introduce Si dopants. As a proof of concept, it was shown that it is possible to dope GaN films outside of an MOCVD reactor by in-diffusing Si from a self-assembled monolayer on the surface. XPS was used to successfully verify that the functionalisation with APTES was reproducible from literature.[1] The highest Si dopant concentration achieved was 2×10^{19} at/cm^3, with almost complete dopant activation and no impact on the quality of the surface, as seen by AFM. The study focused on determining the best capping and annealing conditions by analysing the Si in-diffusion via SIMS, Hall measurements and PL spectroscopy.

Chapter 5 investigated the oxide removal and surface passivation of Bi using alkyl thiols. XPS was used to study the surface chemistry of the Bi films, pre and post passivation, exploring different thiol concentrations and verifying the stability of the film towards reoxidation over a period of 10 days. AFM was used to analyse surface quality throughout the process and FTIR was employed to study the bonding environment present on the surface of the thin films. Based on NMR analysis of the reaction by-product of the functionalisation of Bi powders, it was possible to postulate that oxide removal takes place due to a catalytic reaction between bismuth oxide and the alkyl thiol. Once the oxide had been removed the thiol groups passivate the bare Bi surface and stabilises it towards ambient exposure.

6.2 Future Work

The surface functionalisation approaches used in Chapters 3 and 4 are extremely adaptable for applications where different dopant atoms are required. Chapter 3 outlined the functionalisation of Ge substrates and nanowire devices with triallylarsine and diphenylphosphine oxide monolayers. To extend this work, as there are no other

reports of MLD on Ge it should be possible to attempt doping employing alternative dopants such as Sb, B, Al, Ga, In. Moreover RTA was found as the limiting factor to achieve an abrupt doping profile, due to the high diffusivity of P and As in Ge, therefore it would be ideal to test alternative annealing techniques such as millisecond laser annealing or spike annealing.[2,3] Carbon is also known to co-dope Ge and control the diffusion depth[4–6]. Therefore, in order to obtain a more controllable process it would be ideal to minimise the amount of carbon in the precursor use in order to better control the elements diffusing in the substrate.

The work of Chapter 4 could be expanded in a similar fashion by exploring different dopants, such as Mg or Ge. Moreover, due to the influence of carbon and oxygen on the behaviour of the dopants being introduced, it would be interesting to explore the use of molecules with a smaller carbon skeletons, such as trimethoxysilane, vinyltrimethoxysilane and methyltrimethoxysilane. The functionalisation strategy could then be further expanded to nanowire devices, to also confirm on III-V materials that crystal integrity is maintained after the MLD process. The photopatterning prowess of APTES[1] could also be further investigated, with the aim of achieving area selective doping of GaN by functionalising, patterning and then in-diffusing of Si in specific areas of a sample. This approach could also be used on group IV materials as a selective process could allow for targeted doping of the source-drain areas without adding complexity to the device fabrication process.

Finally, the work carried out in Chapter 5 could be expanded to different length thiols, to check for the effect of the carbon chain length on the oxidation resistance properties of Bi films, as well as to determine surface binding and molecular packing densities. The scalability of the gas phase oxide removal and passivation process also warrants further investigation. Moreover, it would be of interest to apply the passivation to an

actual device, to check how the electrical properties would be affected by the SAM and to see if, when carrying out potential subsequent steps for the fabrication of Bi based devices (*e.g.* contacting of the Bi source/drain, metal gate deposition on the Bi channel) would the chemically passivated surface remain oxide free at the end of step or will there be an impact from the deposited SAM on factors such as metal nucleation.

6.3 Bibliography

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