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Crystallographically Controlled Synthesis of SnSe Nanowires: Potential in Resistive Memory Devices

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Abstract

Here the controlled growth of SnSe nanowires by a liquid injection chemical vapor deposition (CVD) method employing a distorted octahedral [$SnCl_4\{^nBuSe(CH_2)_3Se^nBu\}$] single source diselenoether precursor is reported. CVD with this single source precursor allows morphological and compositional control of the $SnSe_x$ nanostructures formed, including the transformation of $SnSe_2$ nanoflakes into SnSe nanowires and again to SnSe nanoflakes with increasing growth temperature. Significantly, highly crystalline SnSe nanowires with an orthorhombic Pnma 62 crystal structure could be controllably synthesized in two growth directions, either <011> or <100>. The ability to tune the growth direction of SnSe will have important implications for devices constructed using these nanocrystals. The SnSe nanowires with a <011> growth direction display a reversible polarity dependent memory switching ability, not previously reported for nanoscale SnSe. A resistive switching on/off ratio of 10^3 without the use of a current compliance limit was seen, illustrating the potential use of SnSe nanowires for low power non-volatile memory applications.

Keywords: Nanowires, Layered materials, Chemical vapor deposition, SnSe, RRAM

Introduction

The drive to further advance energy technologies,[1,2] optoelectronic[3–6] devices and nanoelectronic[7–13] applications, such as memory[14–16] devices, has led to great interest in layered metal chalcogenide materials, which exhibit strong in-plane chemical bonds, but weak out-of-plane van der Waals bonds. This group of layered materials have been comprehensively studied, both theoretically and experimentally, particularly the exfoliation and synthesis of few-layer two dimensional (2D) structures of these materials.[17–19] In general, 2D materials possess highly interesting electrical, optical, electrochemical and mechanical properties, such as layer dependent bandgaps, leading to tunable optical and electrical properties.[20–23] Whilst 2D variants of layered chalcogenides have developed a firm grounding in the literature, one dimensional (1D) forms of these metal chalcogenides have recently begun to garner interest due to their potential for scalable device architectures, larger surface areas and lower active device volumes due to the small diameter of the nanowire. Due to the lower active volumes, limiting the region where any electronic, heating or chemical interaction will take place, scaling the dimensions of devices down to nanowire form is appealing for increased stability[24] and also reduced device power requirements.[25] Confining 2D materials into a 1D morphology would constitute the basis for further developing 1D nano/opto-electronics, where some of the novel physics of 2D ultra-thin lattices can be incorporated into 1D materials. Current reports of 1D metal chalcogenide layered materials are mostly centered on transition metal dichalcogenides (TMDCs) such as MoS_2. [26],[27]

Recently IV-VI monochalcogenide layered materials have been proposed as promising candidates for sustainable electronic and photonic devices.[28] Among these materials, SnSe with a layered puckered crystal structure, has the advantage of being relatively Earth abundant and non-toxic compared to other popular materials for energy and memory device applications, such as Bi_2Te_3 and GeTe. SnSe is

an indirect bandgap semiconductor, with a small difference between the indirect and direct band gaps (bulk indirect band gap of 0.90 eV and a direct band gap of 1.30 eV),[29] giving opportunities for an indirect to direct bandgap crossover with external perturbation such as strain. An advanced study of 1D SnSe is also of importance for many technological areas of interest, with SnSe having great potential for applications in non-volatile memory devices,[15,16] field effect transistors,[30] sensors[31,32] and photodetectors.[31,33] Engineering these materials in nanowire form is particularly appealing for device scaling and integration, as well as potentially lower power consumption, particularly in relation to nanoscale memory devices, such as phase change random-access memory (PCRAM) and resistive random-access memory (RRAM) devices.[25,34–36] SnSe has recently presented interest for use in RRAM devices, with SnO_x/SnSe/SnO_x layered devices shown to exhibit unipolar resistive switching.[37] Structuring the RRAM device in a nanowire form can offer added benefits such as controlled orientation of the SnSe crystal. For memory applications, control over the morphology of the nanowire is important as this can drastically affect the optical and electronic properties of the material. Additionally, 1D nanostructures provide an excellent route to facilitate the construction of devices with tailored crystal direction. This is more important for SnSe as it is a highly anisotropic material, and has been shown, for example, to exhibit vastly different thermoelectric figures of merit along its different crystal orientations.[38]

Nanowires of tin monoselenide (SnSe) have been sparsely reported previously, through both high-temperature CVD and solution based methods containing toxic catalyst metals and solvents.[39–41] But the tailored growth of 1D SnSe nanowires has not been explored in great detail to date, with different growth methods producing nanowires with varying crystal growth directions, e.g. <011> growth by CVD[40] and <100> growth using a Bi-seeded solution phase approach.[41] Importantly, the previous reports on SnSe nanowires lack details on the effect of growth constraints on the structure, composition and morphology

of the nanocrystals formed [39–41], which is essential for the future development for this technologically relevant material. In this regard, as precursor decomposition kinetics can play a major role in CVD growth methods, by influencing the partial pressure of the vapor source, the use of a customized single source CVD precursor has advantages over using multi-precursor, elemental or powder sources. Single source precursors can have a single decomposition temperature, and can thus supply reaction species with pre-formed bonds, Sn-Se in the case of SnSe, leading to uniform control of the deposited material's composition.[42] The use of single source precursors also leads to controlled adsorption and deposition at the growth interfaces, which results in improved control over the morphology.[43–45]

Herein we report the controlled growth of SnSe nanowires via an atmospheric pressure CVD reaction from a single source diselenother precursor, [$SnCl_4${$^nBuSe(CH_2)_3Se^nBu$}]. The critical growth parameters for nanowire growth, as well as their crystal structure, were explored in detail. The diselenother precursor also allows morphology, phase and crystal orientation controlled synthesis of nanowire and 2D sheets of SnSe and $SnSe_2$ through manipulation of the CVD growth parameters. Due to the relatively low decomposition temperature of this precursor, the thermal budget required for the growth of these SnSe nanowires has also been significantly reduced from 850 – 950 °C to 500 – 550 °C, compared to previous reports of CVD grown SnSe nanowires.[40] We present electrical data from SnSe nanowires with a <011> growth direction, which are shown to undergo electrically stimulated bipolar resistive switching, illustrating the potential use of these SnSe nanowires in non-volatile memory applications.

Results and Discussion

$SnSe_x$ nanostructures were synthesized using a liquid-injection CVD method, utilizing $[SnCl_4\{^nBuSe(CH_2)_3Se^nBu\}]$ as a customized single source diselenoether precursor.[46] Nanowires were grown on silicon (100) substrates with Au catalyst via a conventional vapor-liquid-solid (VLS) growth (see supporting information S1 for a typical VLS growth schematic). Nanowire growth was investigated over the temperature range between 450 - 550 °C under a flowing Ar (1.1 sccm) atmosphere (see Supporting Information for detailed experimental and characterization methods).

The morphology of the nanostructures grown on Si substrates at different CVD growth temperatures (450 - 550 °C) are shown in the SEM images of Figure 1. At the lowest growth temperature of 450 °C, a material with a flower-like morphology was produced (Figure 1 (a)). These flowers were several tens of microns in size, in the range of 10 - 40 μm and consisted of many individual flakes growing in a vertical manner from the underlying silicon substrate, as commonly seen for other layered materials.[47] The "petals" of these flowers were easily separated by sonication in isopropyl alcohol (IPA) to obtain individual flake structures (see Supporting Information, Figure S2). These flakes had lengths and widths between 1 - 5 μm and thicknesses between 20 - 100 nm (inset of Figure 1 (a)). At this low growth temperature, *i.e.* 450 °C, whilst the Au film does melt to form droplets (see Supporting Information, Figure S3) on the Si surface, no indication of vapour-liquid-solid (VLS) growth, and the subsequent growth of 1D nanostructures was observed at this temperature. This suggests that the temperature of 450 °C is not high enough to form a liquid eutectic alloy with the Sn and Se to instigate VLS growth. Instead, the condensation of the $SnSe_2$ vapor leads to the vapor-solid (VS) growth of the flake structures, similar to previous studies using this precursor.[46] The growth of tin selenide materials in a flake structure is readily observed in the literature.[48,49] This predisposition for the formation of flake-like structures is attributed

to the slower growth rate along the <100> van der Waals bonding direction. The slower growth rate is ascribed to the much larger lattice spacing in this direction, and the subsequently increased difficulty of atomic addition to this plane, resulting in the radial growth of the flakes being more energetically favorable than the addition of <100> directional layers to the flakes.

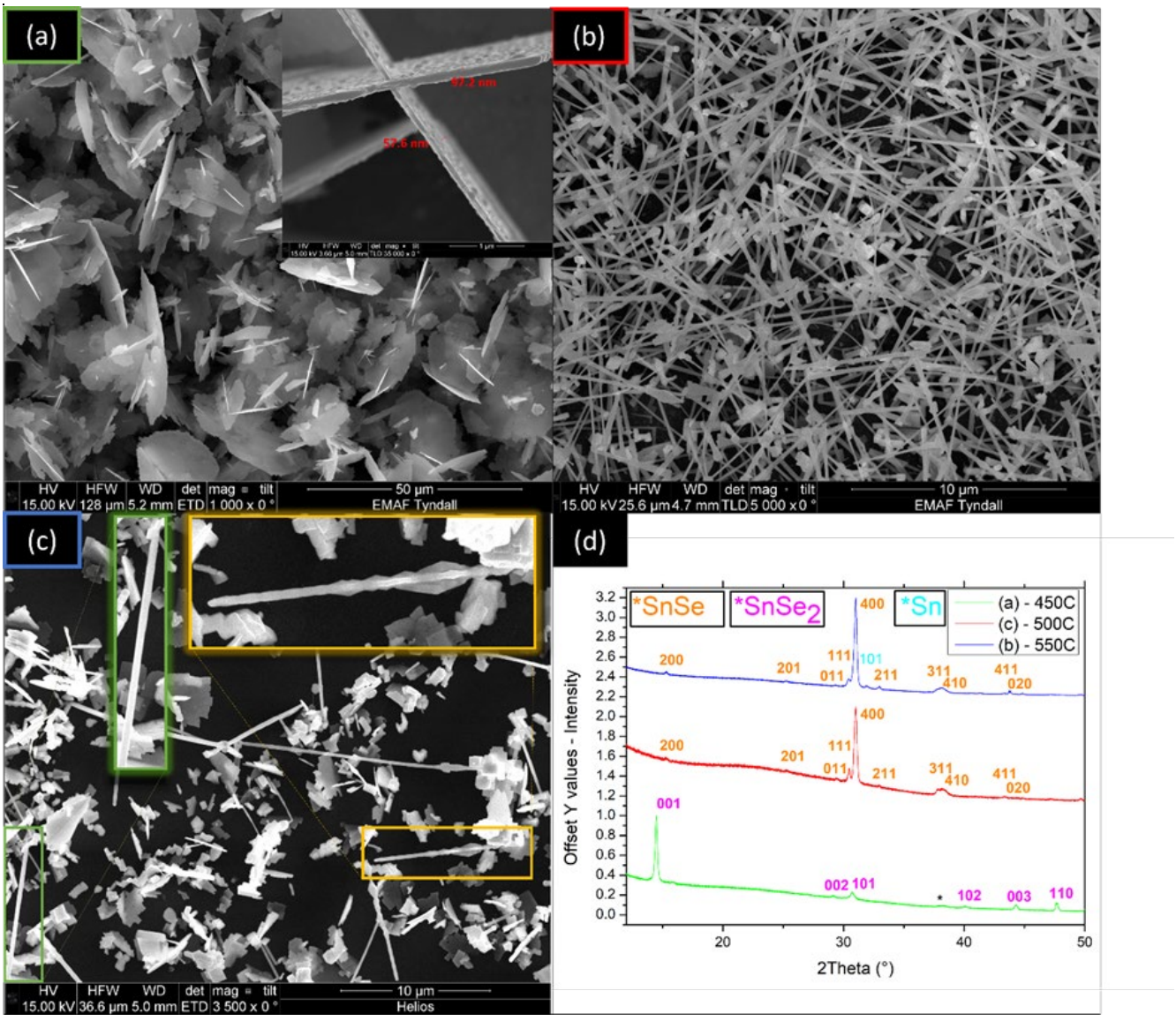


Figure 1. SEM images showing the evolution of the $SnSe_x$ nanostructures with respect to the growth temperature: (a) large flakes with diameters of several microns grown at 450 °C, with a thickness of ~ 60 nm shown in the inset, (b) high yield of nanowire growth at 500 °C. (c) A growth temperature of 550 °C

leads a further change in the morphology, with the formation of both 2D flakes and 1D wires. The insets show the wires formed at this temperature, which consist of two visually different types. A "type A" nanowire is shown in the green border inset, and a "type B" nanowire is shown in the yellow bordered inset. (d) XRD analysis of the samples shown in (a), (b) and (c), which are assigned to P-3m1 164 hexagonal $SnSe_2$ (JCPDS 23-0602) [Magenta] and Pnma 62 orthorhombic SnSe (JCPDS 48-1224) [Orange]. Also present is a very small peak indexed to 111 Au (marked by *), and trace quantities of Sn [141/amd 141 tetragonal (JCPDS 04-0673)] [Blue] at higher temperatures.

An increase of the growth temperature to 500 °C resulted in the prominent growth of nanowires on the Si substrate, which is shown in the SEM image in Figure 1(b). These nanowires were tens of microns long (on average 10-20 μm), with a mean diameter of 115 ± 42 nm (see Supporting Information for diameter distribution, Figure S4). Along with the predominant growth of the nanowires on the Si wafer, negligible amounts of flake-like structures were also observed at this temperature (Figure 1(b)). Although this growth temperature (500 °C) favors the VLS growth of nanowires, the negligible growth of flakes is also produced from a competitive VS growth process at this growth temperature. At a higher growth temperature of 550 °C (Figure 1 (c)), the relative yield of these homogeneously nucleated flakes increased greatly, with a roughly tenfold reduction of the amount of nanowires compared to the nanostructures grown at 500 °C growth temperature. However, upon further investigation of the nanowires formed under this growth temperature, two distinct types of nanowire were seen to exist (inset of Figure 1(c)). The first type (Type A) of nanowires is similar to those formed at the lower temperature of 500 °C (shown in the green bordered inset). These wires were relatively uniform in diameter along their length; with similar lengths and diameters to the nanowires grown at 500 °C. The second type of nanowire (Type B; shown in yellow bordered inset) however showed a different nanowire morphology, with a larger diameter of ~200 nm (see

Supporting Information for diameter measurement of a type B SnSe nanowire, Figure S5). These nanowires were very visually different, and less uniform in diameter along their length. The ratio of type A to type B nanowires was roughly 5:1 under these growth conditions.

The crystal structure and phase purity of the as-grown nanostructures were verified through XRD analysis. Figure 1(d) displays the XRD patterns of the flakes and nanowires, produced at 450 °C, 500 °C and 550 °C. The flakes grown at the growth temperature of 450 °C can be indexed to hexagonal $SnSe_2$ (P-3m1 (164) space group, JCPDS 23-0602), with the strongest reflection corresponding to the (001) plane. SEM analysis revealed that the flakes appeared to grow in a perpendicular manner to the silicon substrate (Figure 1(a)), and high resolution TEM (HRTEM) analysis confirmed that the flakes were stacked along the (001) plane (see Supporting Information, Figure S6). This preferred orientation of the flakes contributes to the strongest (001) reflection in the XRD pattern from the $SnSe_2$ flake sample (Figure 1(d)). Raman analysis (Figure S7 in Supporting Information) further confirmed the growth of $SnSe_2$ at 450 °C with clearly visible E_g and A_{1g} Raman modes corresponding to $SnSe_2$. At 500 °C a phase evolution of the nanomaterial was observed, with the XRD pattern from the sample indexed to orthorhombic SnSe (Pnma (62) space group, JCPDS 48-1224), with no visible $SnSe_2$ peaks present. At the higher growth temperature of 550 °C the orthorhombic SnSe phase of the sample was maintained, with the XRD pattern (Figure 1(d)) showing reflections corresponding to orthorhombic SnSe.

At a growth temperature of 450 °C, the VS growth of $SnSe_2$ flakes prevails, whereas at an increased temperature of 500 °C, the VLS growth of SnSe nanowires dominates. This is in agreement with the Sn-Se phase diagram, where at higher temperatures, SnSe is expected to predominate over $SnSe_2$,[50] and similar to previous studies using this precursor under low pressure CVD conditions, where $SnSe_2$ was

achieved for deposition temperatures of 480-500 °C[46] and SnSe was seen at a deposition temperature of 588 °C.[45]. This phase transformation is proposed to rely on the depletion of Se in the $SnSe_2$ atmosphere at relatively high growth temperatures. The high temperatures promote further dissociation of $SnSe_2$, either through a complete dissociation reaction of $SnSe_2$ followed by SnSe formation, or by a direct formation of SnSe from $SnSe_2$ with loss of the Se to the carrier gas.[51,52] This then leads to the predominant formation of SnSe in the CVD reactor. Precise knowledge of the decomposition mechanism of the precursor is hard to elucidate, thus a fully detailed reaction formula is not included.

This SnSe vapor interacts with the Au catalyst in a VLS-type growth, as indicated in the energy dispersive X-ray (EDX) map (Figure 2(a)) by the presence of the Au seed at the nanowire tip, leading to the 1D growth of SnSe. The self-seeded growth of SnSe nanowires has previously been reported,[40] but in our case the growth without any Au film results in the formation of only SnSe flake like structures (see supplementary information Figure S8). The EDX map of Figure 2(a) further confirms the uniformity in the distribution of Sn and Se in the nanowires, with no segregation or clustering of Sn or Se observed on the surface or in the bulk of the nanowires. For this particular nanowire an atomic ratio of 50.6:49.4 of Sn:Se was measured, which confirms the stoichiometric formation of the SnSe nanowires (see Supporting Information for EDX spectrum, Figure S9). Also, of importance is the clear observation of a spherical Au seed at the tip of the nanowires. Point EDX analysis was performed on the tip of a nanowire (see Supporting Information, Figure S10), which showed a high amount of both Sn and Se in the Au seed at the tip of a nanowire (21 % Se, 14 % Sn, and 65 % Au). This significant incorporation of both Sn and Se in the Au particle is an indication of a VLS growth mechanism. Figure 2(b) shows a room temperature Raman spectrum of an individual SnSe nanowire grown at 500 °C. All Raman measurements were carefully undertaken at a very low laser power to avoid laser induced heating (see supplementary

information Figure S11 for the effect of laser power on phase and morphology of SnSe flake). The B_g vibrational mode of SnSe can be clearly seen at ~110 cm^{-1}, with modes corresponding to the SnSe A^2_g and A^3_g modes also seen at ~132 cm^{-1} and ~152 cm^{-1} respectively in the Raman spectrum.[53,54]

The EDX map in Figure 2(c) shows the elemental distribution of Sn, Se and Au in a Type B nanowire formed at 550 °C. Similar to the nanowires formed at the lower temperatures, Sn and Se are seen to exist uniformly throughout the body of the nanowire grown at 550 °C. The clear presence of a semi-spherical Au tip was observed, with minimal Au contamination in the nanowire body. Notably, this semi-spherical Au seed is different to the spherical Au seed seen for the nanowires grown at 500 °C, indicating that there is a change in the nature of the VLS growth. A differently shaped metallic catalyst at the nanowire tip could infer a different eutectic composition for the metastable alloy during VLS growth which may influence the interfacial shape during nanowire growth, further influencing the morphology of the 1D crystal, resulting in a different variant of SnSe nanowires being formed. At this growth temperature additional VS growth of SnSe flakes also become more prominent than at 500°C, as seen in Figures 1(b) and (c), indicating that VS-type deposition is further enhanced under these reaction conditions. This additional competitive VS type growth is also observed in the less uniform nanowire diameter of the Type B nanowires, where additional nanowire sidewall growth is proposed to occur through a VS type process. The observation of Au seeds in both types of nanowires confirms the essential role of Au in 1D nanowire formation. Figure 2(d) shows a room temperature Raman spectrum of an individual Type B SnSe nanowire grown at 550 °C. The B_g vibrational mode of SnSe can be clearly seen at ~110 cm^{-1}, with the SnSe A^2_g modes also detected at ~132 cm^{-1}.[53,54] A clear red shift of about 5 cm^{-1} of the Raman modes was observed for the Type B nanowires, compared to the Raman modes for those grown at 500 °C (Type A) shown in Figure 2(b) (See inset of Figure 2(d)), indicating a clear difference in phonon dynamics between the two

nanowire types; possibly due to the different crystal growth directions of the two variants of SnSe nanowires.[55]

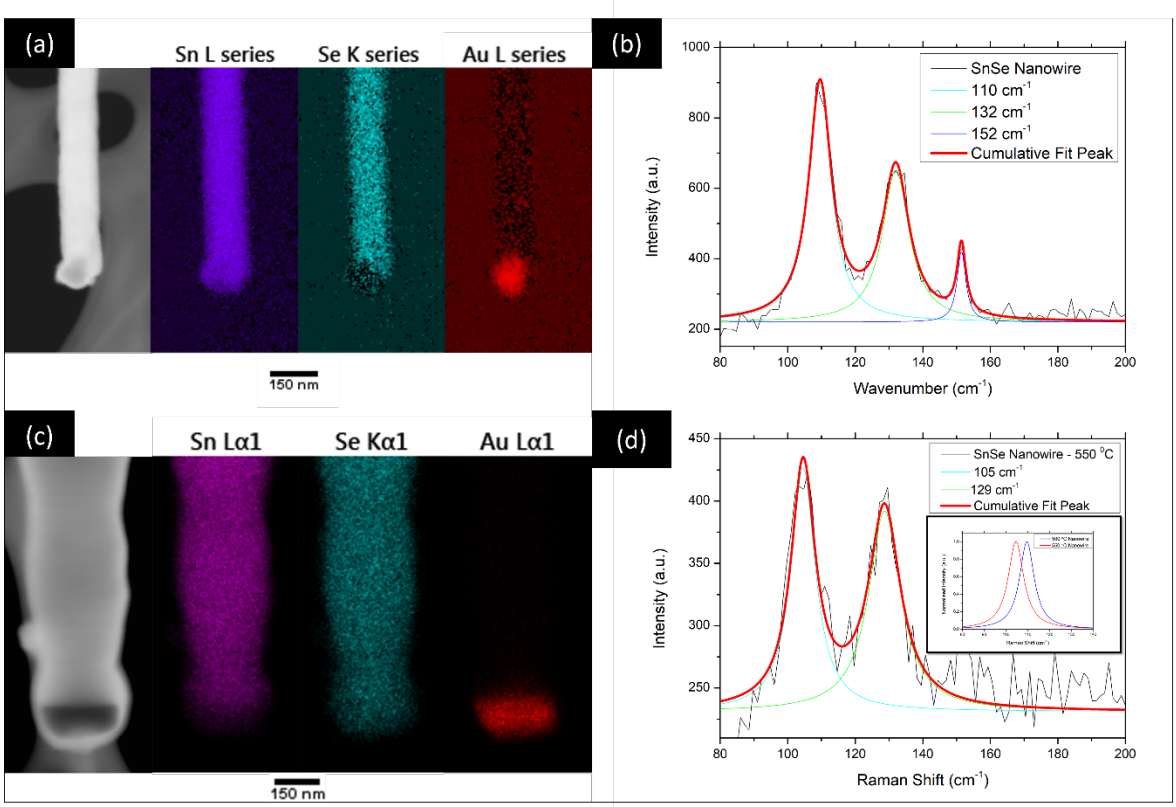


Figure 2: Individual nanowire elemental analysis: (a) STEM EDX mapping of a SnSe nanowire grown at 500 °C (referred to as type A in this report). The uniform distribution of Sn and Se in the wire is clearly evident. (b) Raman spectrum of an individual 500 °C nanowire, showing peaks at ~110 cm^{-1}, ~132 cm^{-1} and 152 cm^{-1}, corresponding to the B_{3g}, A^2_g and A^3_g SnSe Raman modes respectively (514 nm laser excitation, peaks fitted with a Lorentzian function). (c) STEM EDX mapping of a SnSe nanowire grown at 550 °C (referred to as type B in this report). The presence of a Au tip is clearly shown. (d) Raman spectrum of an individual nanowire grown at 550 °C, showing peaks at ~105 cm^{-1} and ~129 cm^{-1}, corresponding to the B_{3g} and A^2_g SnSe Raman modes. Inset shows the relative shift of the fitted B_{3g} mode

between nanowires grown at 500 and 550 °C (514 nm laser excitation, peaks fitted with a Lorentzian function).

The crystal structure and the structural quality of the SnSe nanowires grown at 500 °C was further examined through HRTEM and selected area electron diffraction (SAED) (Figure 3). Accurate knowledge of the crystal quality and structure of the grown nanostructures is imperative for device implementation, including memory devices such as PCRAM and RRAM. Figure 3(a) shows a TEM image of a single SnSe nanowire orientated down the [-100] zone axis, revealing its single crystalline nature with no apparent crystal defects, such as stacking faults or twin boundaries. SnSe is expected to form a surface oxide after being exposed to ambient air.[37] This oxide (Figure 3), determined to be SnO_2 by XPS analysis (see Figure S12, Supporting Information), forms within minutes, and after this the SnSe nanowires then remain further stable for many weeks. The thickness of this amorphous SnO_2 layer is generally uniform, as determined from HRTEM analysis, regardless of nanowire diameter (Figure S13, Supporting Information). The magnified HRTEM image and SAED pattern at the top right inset of Figure 3(a) confirmed the crystal structure of the type A nanowires grown at 550 °C, revealing d-spacing of 0.308 nm along the nanowire growth axis, corresponding to a <011> growth direction. This <011> growth direction is perpendicular to the <100> direction; *i.e.* the direction along which the SnSe layers are stacked. Given the expected slower growth rate along the van der Waals bond direction, *i.e.* <100>, for SnSe layered crystals, a direction perpendicular to this should be a favorable direction for nanowire growth to occur. This growth direction is in agreement with previous reports of SnSe nanowires, which have been shown to grow along the <011> direction for orthorhombic SnSe[40]. To explore the SnSe crystal structure in more detail, TEM investigations were undertaken for SnSe nanowires orientated down different zone axes. Figure 3(b) shows a SnSe nanowire orientated down the [01-1] zone axis, with a HRTEM image in the top right corner,

and an SAED pattern in the bottom right hand corner. A <011> growth direction was seen for this nanowire, in agreement with the previous observation for the SnSe nanowire viewed down the [-100] zone axis (Figure 3(a)). Figure 3(c) shows a TEM image of a cross section, taken from one of the SnSe nanowires. The cross section of the nanowire is seen to clearly exhibit a rectangular shape with a width of ~60 nm and a height of ~40 nm (~70 SnSe layers). This rectangular nanowire cross section explains the large standard deviation seen for the nanowire diameter distribution of these wires, and the presence of two apparent peaks in the data at 71.66 ± 2.86 nm and 119.47 ± 9.60 nm, indicating average thicknesses and widths respectively (supporting information Figure S4). The zone axis of this TEM cross section is assigned to the [0-1-1] direction, in agreement with the growth directions of <011> seen for the nanowires shown in Figures 3(a) and (b). The right insets show a fast Fourier transform (FFT) and two HRTEM images of this nanowire cross section, revealing clearly the (400) and (01-1) lattice planes. Figure 3(d) shows an illustration of the nanowire structure with a <011> growth direction, based on the TEM data

from Figures 3(a), (b) and (c). The planes labelled (a), (b) and (c) indicate the viewing directions of the wires in Figures 3(a), (b) and (c).

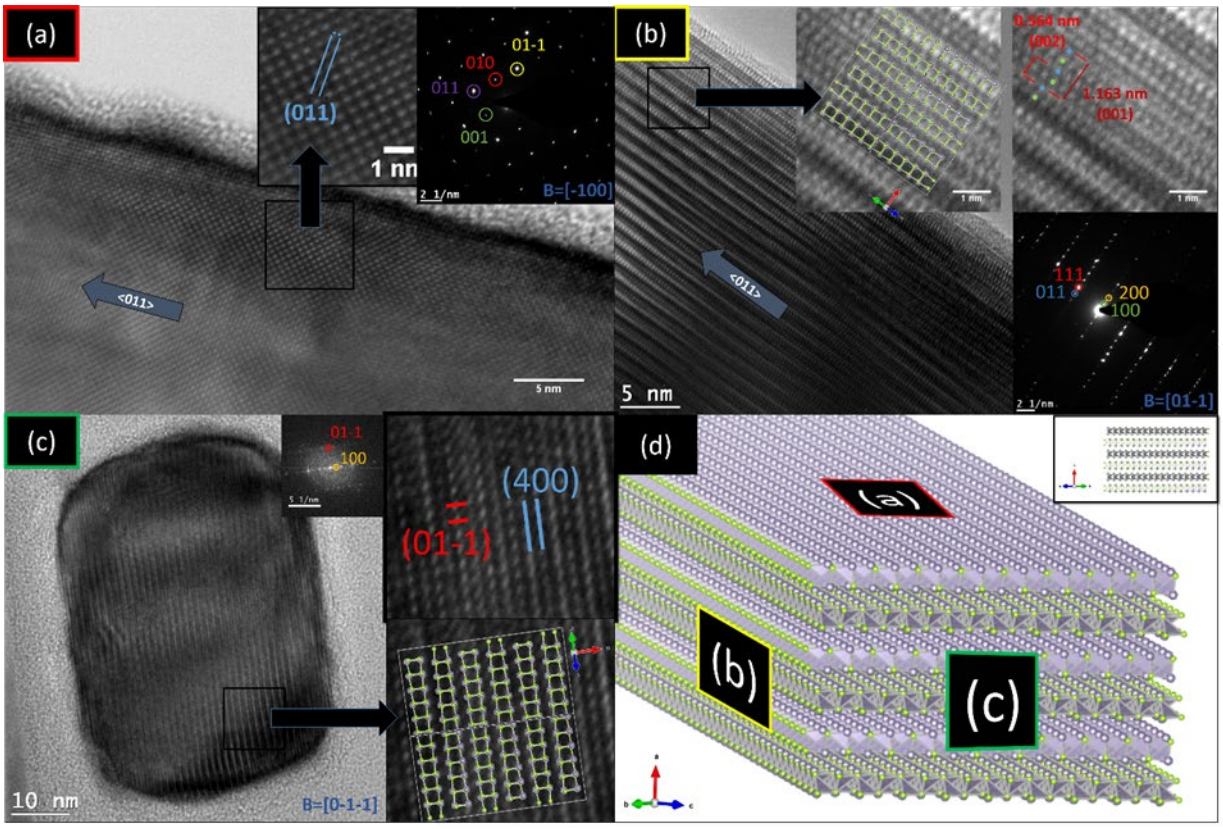


Figure 3: (a) TEM image of an individual nanowire. A thin-oxide shell is visible on the surface edge of the wire. Top middle inset is a HRTEM image of the nanowire, with an SAED pattern in the top right inset. The nanowire was observed to be oriented down the [-100] zone axis, and a nanowire growth direction d-spacing of 0.308 nm was measured, corresponding to the <011> growth direction. (b) TEM image of a single SnSe nanowire oriented down the [01-1] zone axis. Top middle and top right insets are HRTEM images of this wire, with a schematic of the SnSe crystal structure, viewed down the [01-1] zone axis overlaid on the HRTEM image. Bottom right inset is an SAED pattern of this nanowire. A growth direction d-spacing value of 0.308 nm was measured, assigned to the <011> growth direction. (c) TEM image of a cross section of a single SnSe nanowire aligned down the [0-1-1] direction. A visible surface

oxide was observed surrounding the body of the wire. Insets show a fast Fourier transform (FFT) of the nanowire cross-section, HRTEM images and the overlaid SnSe crystal structure viewed down the [0-1-1] direction. (d) Schematic of the SnSe nanowire crystal structure with a <011> growth direction. The planes labelled (a), (b) and (c) indicate the viewing directions of the wire in Figures 3 (a), (b) and (c). The inset shows the nanowire structure viewed down the [0-1-1] direction. The arrows in the bottom left corner indicate the directions of the a, b and c lattice directions. Red arrow: a-axis, green arrow: b-axis, blue arrow: c-axis.

Figure 4 shows TEM analysis of type B nanowires formed at a growth temperature of 550 °C. Figure 4(a) shows a low magnification TEM image of one of these SnSe nanowires. The dark contrasted hemispherical shaped Au seed can be seen at the tip of the nanowire. The top right inset shows an SAED pattern of this nanowire, which can be indexed to the [0-10] zone axis. Most significantly, in contrast to the SnSe nanowires grown at 500 °C, the type B nanowires grown at 550 °C are seen to grow along the <100> crystal direction. This growth direction is along the SnSe van der Waals bonded layer direction, and has only been seen before for very small diameter Bi-seeded SnSe nanowires.[41] Higher temperatures have been shown to play a major role in the growth orientation of other layered materials, such as with MoS_2 flakes,[47] and this higher temperature used here clearly alters the growth rate along the <100> direction. The different shapes of the Au seeds between these type A and type B nanowires (see Figures 2 (a) and (c)) indicate that the nature of the VLS growth of the SnSe nanowires is also effected, and this difference in the VLS growth properties could play a role in the growth of the nanowire in a different crystal growth direction. This change in the nanowire crystal direction between the two nanowire types offers a potential explanation for the red shift observed in the Raman spectra for type B compared to type

A nanowires (inset in Figure 2(d)). Similarly, changes in Raman spectra have previously been assigned to localized polarization effects from an anisotropic crystal lattice.[55]

At a growth temperature of 550 °C additional crystal growth was also observed on the sidewall of the nanowires which effects on their morphology, as is seen in the TEM image of Figure 4 (b). The nanowire morphology (dark contrasted region of the TEM image) is guided through a VLS process whereas the irregular jutted sidewall growth is triggered via the vaporization and condensation of growth species on the nanowire sidewalls, *i.e.* VS-type growth. These large bulges are seen for many of the SnSe nanowires produced at this temperature. Figure S14 shows the growth of these large bulb structures without any Au seed, and without any nanowires being produced. To explore this sidewall growth further, cross sectional TEM was taken of one of these nanowires (Figure 4(c)). A "cross-like" shape is clearly seen, with three branches sprouting from the center nanowire body. The top right inset shows an SAED pattern of this nanowire cross section, assigned to the [-100] zone axis. From this information, the overlaid red box can be seen as the [-100] viewed SnSe unit cell, corresponding to the nanowire body, with the sidewall growth indicated by the blue arrows in the <011> equivalent directions. The VLS-guided nanowire body is faceted by high surface energy (010) and (001) sidewalls, which lends to favorable VS addition to these planes, forming low surface energy (011) facetted surfaces. No obvious crystal defects are seen in these nanowires, and the small number of additional satellite spots that are seen in the SAED pattern of this cross-section in Figure 4 (c) are expected to be induced from the cross-sectioning process, as a fully single crystalline SAED pattern is seen for the as-grown pristine nanowire in Figure 4 (a). Figure 4(d) shows a schematic representation of the type B nanowires with a <100> growth direction, with the SnSe layers stacked along this direction. The insets show the SnSe structure down three major zone axes.

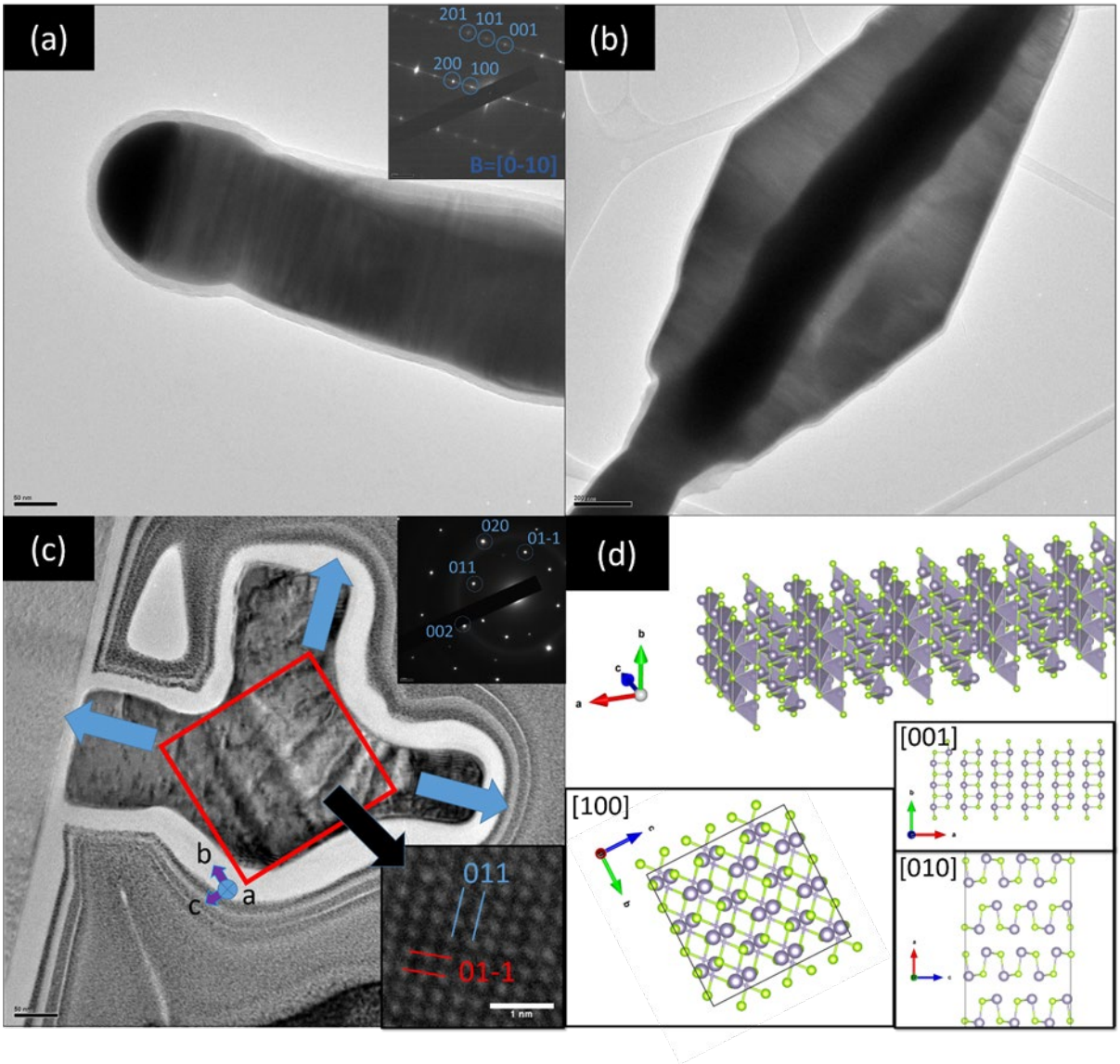


Figure 4: TEM analysis of the nanowires formed at 550 °C. (a) Low magnification TEM image showing the body of one of these nanowires. The dark contrast at the tip of the wire is indicative of the Au seed. Inset is an SAED pattern recorded from the bulk of the nanowire, indexed to orthorhombic Pmna SnSe viewed down the [0-10] zone axis. A growth direction of <100> was observed, which is perpendicular to the SnSe interlayer direction. (b) TEM image of a nanowire similar to that shown in image (a), with some additional sidewall growth. The dark contrast is due to the thickness of the layer from additional growth in this area. (c) Cross-sectional TEM image taken from a nanowire similar to that shown in image (b). A

T-shaped nanowire cross section is clearly observed. The top right inset shows the SAED pattern, indexed down the [100] zone axis. The red box overlaid on the image represents the orthorhombic Pnma 62 SnSe unit cell, with the blue arrows indicating the [011] equivalent growth directions. (d) Schematic of the crystal structure of a SnSe nanowire grown at a temperature of 550 °C. The top left image shows the simulated general structure of the nanowire, with a <100> growth direction. The bottom right shows the SnSe Pmna 62 structure down [100], [010] and [001] zone axes. The colored arrows indicate the directions of the a, b and c lattice directions. Red arrow: a-axis, green arrow: b-axis, blue arrow: c-axis.

The electrical behavior of the SnSe nanowires was studied using two terminal electrical contacts, as shown in the inset of Figure 5(a). Due to the high yield, and regular morphology of the SnSe nanowires produced at 500 °C (type A), this set of nanowires were chosen for electrical testing. For electrical device fabrication, SnSe nanowires were mechanically transferred from the growth substrate onto a clean Si substrate (1 μm thermal oxide) with optical lithography-defined contact pads. Single SnSe nanowires were contacted by electron beam lithography (EBL) using Ti-Al-Au contacts (for details of the device fabrication, see Supporting Information). The channel length of the electrodes was ~ 1 μm and the thickness was determined by the nanowire diameter. Figure 5(a) shows an *I-V* curve (first sweep) from a pristine, individual SnSe nanowire (black curve). The extremely low current levels under a low voltage (*V*) bias show that the device is initially in a high resistance state (HRS) due to the presence of a thin but insulating oxide surrounding the nanowire. This amorphous oxide layer of a few nanometers thick can be observed surrounding the nanowire in the HRTEM image in Figure 3 (a) and confirmed to be SnO_2 by XPS analysis (Figure S12, Supporting information). At ~ 4 V the current level suddenly increases and the device switches to a low resistance state (LRS). This change from a HRS to a LRS is referred to as the SET event,

with the reverse, a change of the LRS to a HRS describing the RESET event. Subsequent measurement, shown by the red curve, indicates that the LRS is sustained after the SET event. Figure 5(b) shows the resistance of the LRS, measured at 1 V, fluctuating slightly over time before spontaneously decaying to the HRS at just under 1000 s. Figure 5(c) displays the bipolar resistive switching (BRS) behavior as the voltage is swept from a positive to a negative bias. At ~ 4 V, the device experiences a SET event, transitioning from the HRS to the LRS, the large resistance of the device means that no current limiting compliance was necessary to operate between memory states, which is a desirable feature as current-limiting transistors bring additional complexity to memory circuitry. Under a sufficient negative bias, ~ -4 V, the measured current suddenly drops as the device returns to the HRS (RESET event). This voltage range is similar to previous reports of nanowire RRAM devices.[56]

The polarity dependent memory switching describes the bipolar process whereby a conducting filament (CF) must bridge the crystalline core of the wire and the metal contact through the insulating oxide shell. Unipolar resistive switching; where the SET and RESET events are controlled by the magnitude of current flow through the device, has been reported for SnO_x/SnSe/SnO_x layered nanoscale devices.[37] The RRAM measurement presents preliminary evidence that nanowire SnSe devices exhibit vastly different resistive switching properties to that of planar SnSe layer devices. The previous report on SnO_x/SnSe/SnO_x layered device[37] proposes a mechanism based on the formation of a CF composed of O vacancies through the SnO_x layer. Formation of an O vacancy CF is a highly likely mechanism for the BRS we observe, given the SnO_2 layer on the surface of the nanowire. The decay back to the HRS seen in Figure 5(b) is proposed to be due to the decay of the CF or a build-up of oxygen at the electrodes as described in previous reports on SnO_x/SnSe/SnO_x planar devices.[37] A BRS mechanism based on the formation of a CF has been reported in large SnSe and $SnSe_2$ crystals,[16] however BRS has not been previously reported for SnSe

nanowires. During application of a voltage bias, electrochemical oxidation may also occur at the anode, leading to the evolution of molecular O, injecting O vacancies into the oxide layer where they move towards and accumulate at the cathode, bridging the conductive nanowire core and the electrode through the formation of a CF.[57] The attracting and repelling of the O vacancies establishes the core-process of the BRS observed in these devices. O vacancies can give rise to both unipolar, and bipolar resistive switching behaviors, and is highly dependent on oxide structure, forming current and device area.[58] Through repetition of the bipolar *I-V* sweep the SnSe nanowire devices could be repeatedly switched between the HRS and the LRS. The difference between the HRS and the LRS for four such switching cycles (with each cycle plotted individually in the supporting information; see Figure S15-A, a second device is also shown in Figure S15-B) is shown in Figure 5(d). The level of the LRS was measured in the MΩ range with the HRS almost three orders of magnitude higher. The significant resistance difference between the LRS and the HRS indicates the potential for future memory devices based on this material.

To get an insight to the conduction mechanism at various points of the resistive switching cycle, resistive switching data for two devices were analyzed in log scale (Figure S16A, S16B). The results indicate a space-charge-limited current (SCLC) mechanism with trapped SCLC behavior ($I \propto V^{>2}$) when the voltage is below the SET threshold. The formation of the CF causes a rapid rise in current flow and SETs the device into the LRS. In the LRS, ohmic ($I \propto V$) and trap-free behavior are identified, whereby, the current is dominated by charge carriers injected from the contacts and the *I-V* characteristics becomes quadratic in what is termed the Child's square law region ($I \propto V^2$).[59] This is similar to stacked SnO_x/SnSe/SnO_x devices, where the conduction mechanism was interpreted to follow the shallow trap-associated theory. Memory device studies on oxide coated II-VI semiconductor nanowire materials have also shown trapping of electrons by O vacancies to be the responsible mechanism.[56] SCLC conduction has been observed in

a wide range of materials, it is commonly accepted that the defect-related traps, e.g., O vacancies contribute to the SCLC conduction.[60] Other conduction mechanisms such as Schottky and Poole-Frenkel (PF) emission were also investigated through plots of log (I/V) versus √V and log(I) versus √V (Figure S17A, S17B). The linear relationship determining PF conduction is poor across both devices, however, regions of Schottky conduction can be observed in the high bias portions (Figure S17-B (b, d)). From this we can conclude that both trap-controlled SCLC and Schottky conduction mechanisms play a role in the device behavior (detailed discussion in Supporting Information).

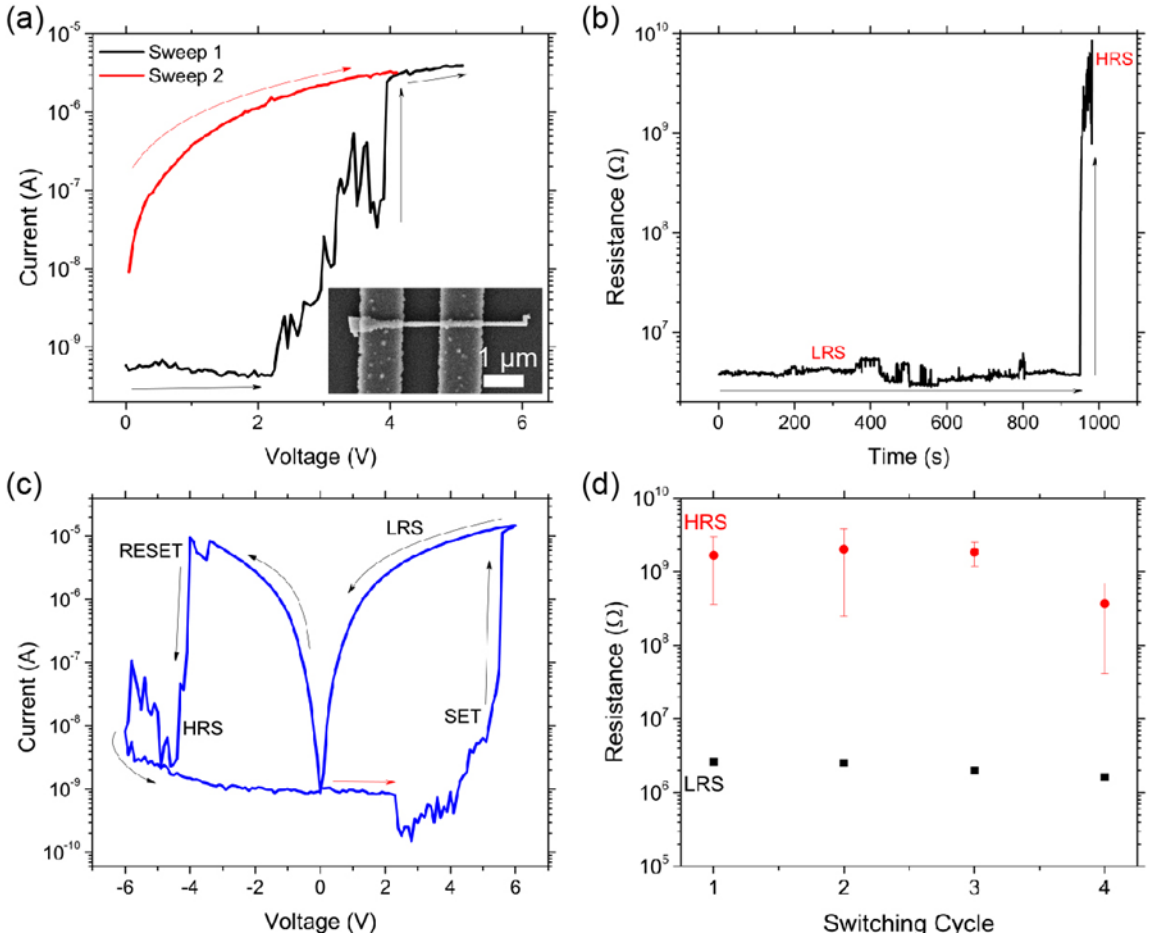


Figure 5: (a) First and second *I-V* sweeps of a single SnSe nanowire device. The inset shows a SEM image of a SnSe nanowire between 2 electrical contacts with a separation of 1 µm. The black curve details

the initial sweep, where the device was initially in the high resistance state (HRS), at 4 V there is a sudden increase of current and the device resistively switches to a low resistance state (LRS). The second sweep shows that the device remains in the LRS. (b) The LRS remains for 1000 s before spontaneously decaying to the HRS. The read voltage during this experiment was 1 V. (c) Polarity dependent resistive switching is demonstrated through the positive SET event to the LRS, and the RESET event which returns the device to the HRS under application of a sufficient negative bias. (d) The single SnSe nanowire could be repeatedly switched between the LRS and the HRS with an on/off ratio of ~10^3.

Conclusions

Highly crystalline, defect free SnSe nanowires have been grown via a CVD method, utilizing a single source diselenoether precursor and Au catalyst. The morphologies, phase and the crystal structure of the nanostructures produced have been tuned from $SnSe_2$ to SnSe flakes and to two uniquely different types of SnSe nanowires. The growth direction for the SnSe nanowires can be engineered from <011> to <100> by simply varying the nanowire growth temperature from 500 to 550 °C. The tailoring of the SnSe nanowire crystal structure and growth orientation has important consequences for future device engineering including thermoelectric devices, as SnSe crystals tend to show prominent anisotropic behavior. The control over directionality of the 1D crystals also expands the scope of obtaining hierarchical nanostructures from this set of materials. The knowledge obtained on the growth and crystal structure of differently oriented nanowires will cater to the future objective; which is to synthesize high yields of uniform nanowire morphology of chalcogenide materials with different crystal orientations for large scale applications. Electrical results from two-terminal <011> oriented SnSe nanowires showed polarity dependent resistive switching, without the use of a current compliance limit, and an on/off ratio

of 10^3. Compared to previous studies on layered SnSe based planar RRAM devices, these nanowire devices show bipolar switching behavior as opposed to unipolar switching, and such a nanowire form presents greater capacity for efficient scaling down of SnSe RRAM devices. These results could form a route for more in-depth memory studies, such as temperature dependent and stability measurements. Also the electrical behavior of SnSe nanowires shown in the paper could pave the way to explore anisotropically tailored SnSe nanowire devices with different crystal orientations, materials geometry, and device architectures (e.g. nanowire arrays, vertical devices).

Supporting Information:

The following files are available free of charge.

Detail experimental method, Illustration of VLS growth mechanism, SEM image of $SnSe_2$ flake, SEM image of Au nanoparticles, SnSe nanowire diameter measurements, HRTEM of $SnSe_2$ flake, Raman analysis of $SnSe_2$ flake, SEM image of SnSe flakes, EDX analysis of SnSe nanowire and Au tip, Raman analysis of SnSe flake at high laser power, XPS analysis of SnSe nanowires, SEM image of substrate after growth without Au present, Oxide thickness vs. nanowire diameter, I-V curves showing cyclic bipolar resistive switching. Resistive switching curves plotted as log(I) versus log(V), log (I/V) versus $\sqrt{V}$ and log(I) versus $\sqrt{V}$.

Conflict of Interest:

The authors declare no competing financial interest.

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