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# A study on a tether-less approach towards Micro-transfer-printing of large-footprint power micro-inductor chiplets


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***Abstract*—In recent years, need for large-scale, multi-layer, high-capacity integration for electronic systems has sky-rocketed. In this regard, a novel heterogeneous integration technique called Micro-transfer-printing ($\mu$TP) has attracted a lot of attention due to its unique ability to integrate chiplets from heterogeneous sources on to a target substrate. Typically, the chiplets are picked up from a donor substrate using an elastomer stamp by breaking the surrounding micro-tethers and then printed onto a target substrate for further processing. Despite its success in applications like sensors, photovoltaics, photonics, etc., $\mu$TP finds its limitation in handling chiplet dimensions larger than 100 x 100 x 20 $\mu m^3$. Therefore, reports on $\mu$TP of passive components like micro-inductors and micro-transformers with dimension in mm x mm and thickness of 100s of $\mu$m are non-existent. In this paper, a completely novel, non-classical, tether-less approach has been demonstrated for micro-inductors with large footprint. This paper also reports a customized PDMS stamp fabrication and optimized post-fabrication sample preparation steps, such as, substrate thinning and polishing while retaining device performance intact.**



***Index Terms*—micro-transfer-printing, $\mu$TP, micro-inductor, heterogeneous integration, tether-less, large-footprint chiplet, PDMS stamp**


## I. Introduction

In past decade, with increased demand for intelligent systems with improved performance, functionality, and reduced SWaP-C (Size, Weight, Power and Cost); several large-scale, multi-layer, high-capacity, advanced heterogeneous integration technologies have been invented for developing scalable and flexible electronics [1]–[3]. In heterogeneous integration, various system components, such as, sensors, microprocessors, memory devices and other functional blocks from different origin and form factors are integrated into a single system or package. Over the past decade, among all the various Heterogeneous Integration techniques, Micro-Transfer-Printing ($\mu$TP) has gained significant interest due to its several advantages over other integration techniques. In $\mu$TP, micro-scale components from heterogeneous origin can be transferred onto a target substrate using a transfer stamp [4] by pick-and-place method. It is capable of high-precision component positioning on non-planar surfaces facilitating development of complex systems with high degree of flexibility and scalability. Furthermore, $\mu$TP can also be utilized to interconnect components fabricated using different materials and processes, which is a limitation for other integration techniques. This technology has enabled a growing number of applications, including flexible electronics, sensors, photovoltaics, wearable devices and micro-LED displays [5].

While this technology has been quite successful in those applications, it face challenges for chiplets with large-footprint and higher substrate thickness. This challenge in $\mu$TP for large-footprint devices lies in designing and developing suitable tethers [5]. These tethers must be able to withstand the body-load of larger chiplets when they are released via sacrificial etch, as well as, they must break while the chiplets are picked up from the source substrate. For example, an on-chip power supply development requires large-footprint and thick micro-inductors and transformers (with size of 1000s of $\mu$m x 1000s of $\mu$m x 100s of $\mu$m) to be transfer printed. $\mu$TP of such large-footprint chiplets has not been demonstrated yet.

In this paper, we successfully addressed the limitation by developing and optimizing a tether-less process for $\mu$TP of large-footprint micro-inductors. The process starts with sample


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preparation steps such as post-fabrication substrate grinding, polishing and chiplet dicing followed by tether-free transfer printing of singulated devices. This paper also describes a detailed stage-wise device characterization methodology to study the effect of these process steps on the performance of the micro-inductors. The fabrication process of a customized PDMS stamp is also discussed in this paper.

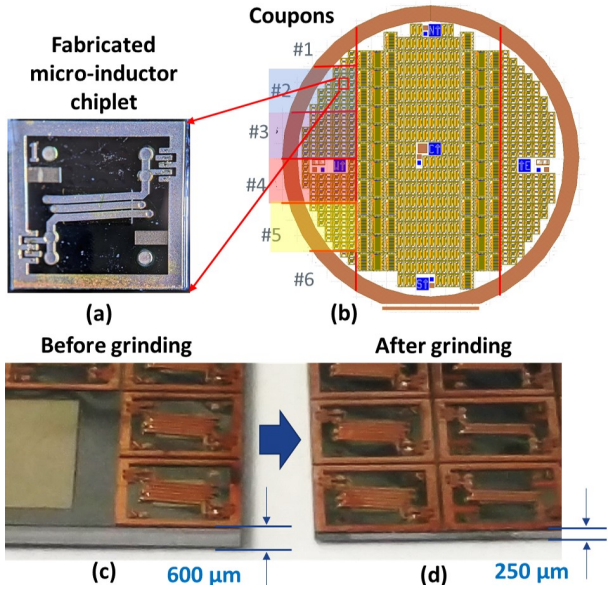



Fig. 1. (a) An optical micrograph of a Tyndall fabricated micro-inductor, (b) the mask layout of the full wafer with coupon cut-out plan, (c) an optical micrograph of a section of a coupon with micro-inductors before backside substrate grinding, (d) an optical micrograph of the same after grinding of the coupon.

## II. Experimental

Integrated magnetic-core power micro-inductors on silicon (footprint 2.62 x 2.5 in mm, Fig. 1a) were fabricated using in-house micro-fabrication facility [6]. One of the fabricated wafers was diced into small coupons as shown in Fig. 1b. The coupons containing micro-inductors were flipped and the device-side of the coupons were attached with glass carriers using a temporary mounting adhesive (Crystalbond™ 509). This was done to protect the fabricated micro-inductors during the following grinding and polishing processes. The backside of these coupons were ground and polished to reduce the coupon thickness from 600 $\mu$m (Fig. 1c) to 250 $\mu$m (Fig. 1d) using a Logitech PM5 precision lapping and polishing tool. This was necessary to enable $\mu$TP and to maintain planarity with other electronic components on the target substrate. A calcinated aluminium oxide abrasive powder with 3 $\mu$m particle size was used during the lapping process whereas the polishing was done using a polishing fluid SF1 containing alkaline colloidal silica. The grinding pad rotation rate was kept at 40 rpm for both grinding and polishing [7]. The measured average grinding rate for these coupons were found to be approximately 2.2 $\mu$m per minute, as shown in Fig. 2a.

Backside surface roughness of the chiplets is extremely critical for successful $\mu$TP [5]. This is because, smoother

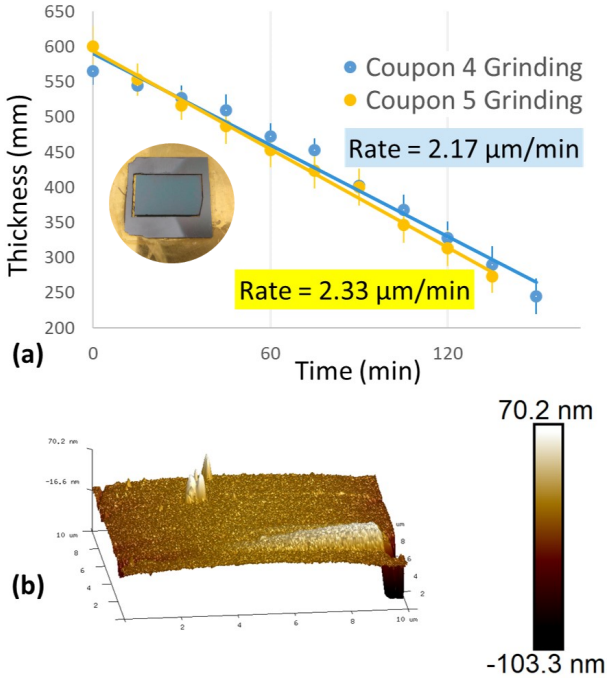



Fig. 2. (a) A plot showing grinding rate (thickness vs. time), (b) an AFM measurement showing surface roughness of the polished backside of the coupons.

surface promotes stronger adhesion to the target substrate during transfer-printing. Therefore, post-polishing backside surface roughness of the coupons (one of such coupons being shown in the inset of Fig. 2a) were measured using a Bruker AFM tool. The scanning area for the measurement was 10 $\mu$m x 10 $\mu$m. The measured value of average surface roughness was about 100 nm as shown in Fig. 2b. The thinned and polished coupons were transferred on UV-curable dicing tape with the polished side of the devices sticking to the dicing tape. The coupons were then diced into singulated micro-inductor chiplets. A custom fabricated PDMS stamp was used to pick-up singulated devices from the dicing tape and printed on an Intervia®-coated target substrate. The entire process flow of $\mu$TP of the micro-inductors has been schematically shown in Fig. 3.

The PDMS stamps were fabricated in-house by using a master mould on silicon wafer as shown in Fig. 4. The master mould fabrication started with creating stamp patterns by etching trenches on silicon <100> wafer using 5% TMAH solution and using SiNx as the hard mask. Once the stamp patterns were etched, the hard mask was then removed and an anti-stick coating (Perfluorodecyltrichlorosilane) was applied to the surface of the etched silicon in order to facilitate release of the PDMS. The PDMS (Sylgard 184) was degassed and poured onto the Si master mold and cured at 50 °C overnight and released. The stamps were then singulated into individual pieces. The stamp height was achieved as 100 $\mu$m with a sidewall slope of 54° which was defined by the sidewall of the mould. Several different sizes of the PDMS stamps were fabricated, ranging from 1300 $\mu$m x 1300 $\mu$m to 3500 $\mu$m x

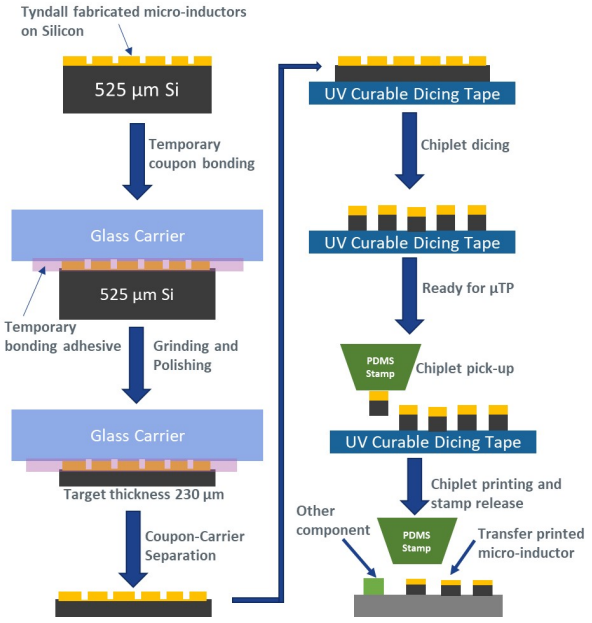



Fig. 3. The process flow diagram of the tether-less $\mu$TP used in this work.

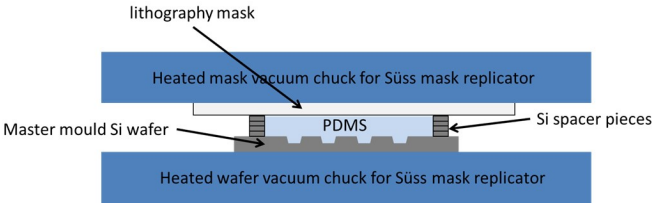



Fig. 4. A schematic of the custom PDMS stamp fabrication process.

3500 $\mu$m. Out of which, the 2300 $\mu$m x 2300 $\mu$m stamp was found to be more suitable for successful $\mu$TP of the micro-inductors used in this work.

An adhesive-assisted $\mu$TP was chosen for this work. Prior to $\mu$TP, a 2.2 $\mu$m thin-film of diluted Intervia® (diluted with PGMEA with a ratio of 1:1) was spin coated onto the target substrate (a standard silicon wafer in this case) to enhance adhesion between the chiplets and target substrate. The Intervia® coated wafer was heated at 130 °C for 4 minutes for removal of residual solvent. $\mu$TP is typically done within 3 hours of Intervia® spin coating. It was found that longer time gap between Intervia® coating and $\mu$TP increases the risk of printing failure.

$\mu$TP of the micro-inductors was performed using a table-top tool - MTP1002. A set of tool parameters, related to stamp pick-up and printing, were optimized for successful $\mu$TP. These parameters are - pick-up overdrive distance, pick-up overdrive speed, pick-up acceleration, printing overdrive distance, printing shear distance, and printing shear speed. Fig. 5 shows the table-top $\mu$TP tool along with the source substrate (in this case, a singulated micro-inductor coupon mounted on a UV-curable dicing tape) and an Intervia®-coated silicon target substrate (placed on the target chuck) with a few transfer-printed micro-inductors on it.

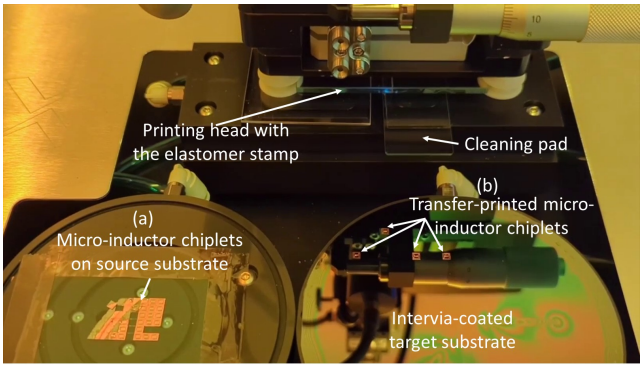



Fig. 5. The $\mu$TP table-top tool (MTP1002) with both the substrates - (a) the source substrate with a few micro-inductors picked up, and, (b) the Intervia®-coated target substrate with a few transfer-printed micro-inductors.

After performing $\mu$TP of the micro-inductors, the Intervia® on the target substrate was cured to reconstitute the printed devices onto the substrate. For this, the target substrate was flash exposed for 2 minutes followed by a hot plate baking at 100 °C for 3 min. Finally, the substrate was placed in an oven under $N_2$ environment at 90 °C for 30 min, then the chamber temperature was ramped up to 175 °C for 3 hours to achieve final curing.

## Results and Discussion

The micro-inductors underwent four major unit processing steps to complete $\mu$TP, namely (i) grinding and polishing of inductor coupons, (ii) dicing of the coupons to singulate the devices, (iii) post-$\mu$TP pre-curing, and (iv) post-$\mu$TP curing. The effect of the entire process sequence on the key device performance, i.e. measured inductance up to 3 GHz (Agilent 5071C VNA), was studied before grinding and after each of the aforesaid four processing steps. The effect of substrate grinding and polishing is shown by measuring two-port S-parameters of the devices present in two coupons (coupon-2 and coupon-4 as shown in Fig. 1b), and then by extracting inductances [8] before and after this process. It is observed

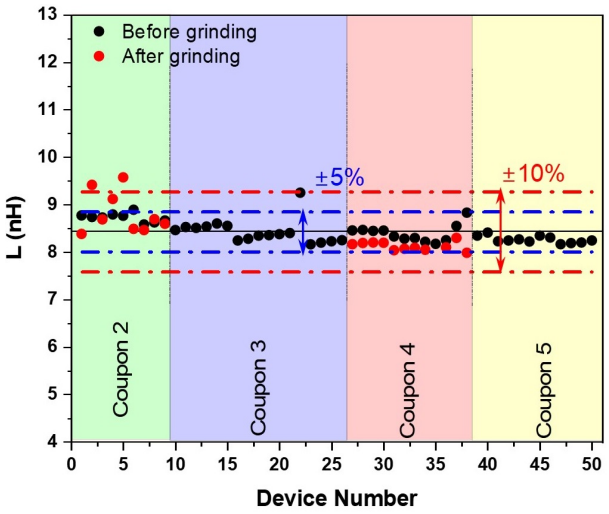



Fig. 6. Statistical analysis of device performance of measured micro-inductors during pre and post grinding stages.

through the statistical analysis (shown in Fig. 6) that the substrate thickness reduction process does not affect the inductor performance significantly. The variation in extracted inductance of most of these devices at their designated operating frequency of 100 MHz was found to be $\pm 0.8$ nH around it's nominal value of 8.5 nH which is well within the industry-accepted tolerance range of $\pm 10\%$.

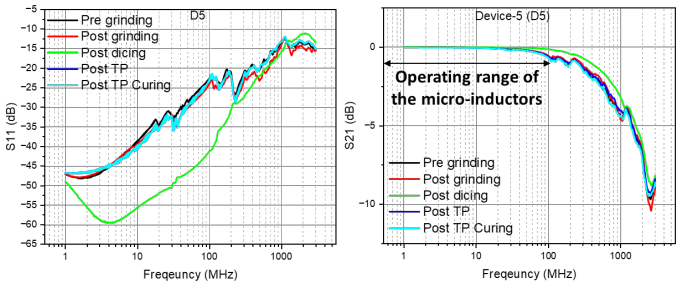



Fig. 7. S-parameters (S11 on left and S21 on the right) of one of the micro-inductors from coupon-2 measured at different stages of processing.

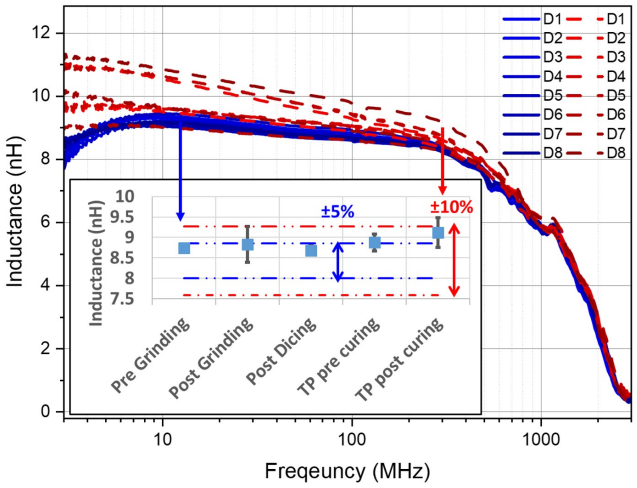



Fig. 8. Statistical analysis of inductance values of the micro-inductors from coupon 2 at two different stages of the process - pre-grinding and post $\mu$TP curing, the inset image shows the measured inductance values at every stages starting from sample preparation to post $\mu$TP curing.

Singulated micro-inductors from coupon-2 was processed further towards $\mu$TP. The two-port S-parameters of the micro-inductors on coupon-2 were again measured after dicing, post-$\mu$TP pre-curing, and post-curing stages. Fig. 7 represents the S11 and S21 of one of the eight micro-inductors present in coupon-2 measured at every steps. Beside the measurement anomaly observed during the post-dicing measurement in all coupon-2 devices (not shown here), the measurements are very consistent. The measured (rather extracted) inductance are plotted versus frequency for all eight micro-inductors from coupon-2 (denoted by D1 to D8) at various process stages starting from before grinding to post-$\mu$TP Intervia® curing as shown in Fig. 8. The variation of inductance values measured at different stages throughout these processes remained within industry-accepted tolerance band (inset of Fig. 8). Therefore, it can be summarized from these demonstrated results that the tether-less $\mu$TP process has finite impact on the measured inductance value, but, it remained within the industry-accepted tolerance of $\pm 10\%$.

## Conclusion

A novel tether-less way of micro transfer printing ($\mu$TP) process has been developed and the successful $\mu$TP of large-footprint (>100 x 100 x 20 $\mu m^3$) thin-film micro-inductor chiplets has been demonstrated in this article for the first time. The micro-inductors underwent four major unit processing steps to complete $\mu$TP, such as substrate grinding and polishing from 600 $\mu$m down to 250 $\mu$m, dicing of the coupons to singulate the devices, post-$\mu$TP pre-curing to enable proper adhesion between transfer printed devices and the target substrate, and post-$\mu$TP post-curing to reconstitute transfer-printed components. Each process steps were optimised and the effect of these processes on the device performance were assessed. The measurement results indicate that the micro-inductors were successfully transfer-printed without inductance variations exceeding $\pm 10\%$ of the nominal values at 100 MHz. The result presented here will enable heterogenous integration of large-footprint chiplets including thin-film magnetics and other ASIC dies for futuristic power delivery system packaging.

## Acknowledgments

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