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ABSTRACT

In this work, we investigate the physical and electrical properties of WS_2 thin films grown by a plasma-enhanced atomic layer deposition process, both before and after device fabrication. The WS_2 films were deposited on thermally oxidized silicon substrates using the $W(NMe_2)_2(NtBu)_2$ precursor and a H_2S plasma at 450 °C. The WS_2 films were approximately 8 nm thick, measured from high-resolution cross-sectional transmission electron imaging, and generally exhibited the desired horizontal basal-plane orientation of the WS_2 layers to the SiO_2 surface. Hall analysis revealed a p-type behavior with a carrier concentration of 1.31×10^{17} cm^{-3}. Temperature-dependent electrical analysis of circular transfer length method test structures, with Ni/Au contacts, yielded the activation energy (E_a) of both the specific contact resistivity and the WS_2 resistivity as 100 and 91 meV, respectively. The similarity of these two values indicates that the characteristics of both are dominated by the temperature dependence of the WS_2 hole concentration. Change in the material, such as in sheet resistance, due to device fabrication is attributed to the chemicals and thermal treatments associated with resist spinning and baking, ambient and UV exposure, metal deposition, and metal lift off for contact pad formation.

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The use of two-dimensional transition metal dichalcogenide (TMD) materials has the potential for a diverse range of integrated and multifunctional applications, including sensors, optoelectronics, and electronic and photochemical devices.[1,2] Their electronic properties span from being semi-metals through to being wide-bandgap semiconductors depending on their physical and chemical properties, including the transition metal element, the stoichiometric value, and the number of monolayers that make up the thickness.[3,4] From a technological perspective, these materials come with some difficult challenges, including achieving large area defect-free growth,[5,6] stable approaches to doping,[7] and realizing the required values of specific contact resistivity.[8]

The TMD WS_2 has been actively researched for many years, in some cases, through fundamental precursor chemistry or synthesis material studies[9–12] or with a specific application area in mind, such as lubricants,[13–16] batteries,[17,18] photovoltaics,[19] sensors,[20] opto-electronics,[21] or catalysis.[22] In relation to nanoelectronic applications, WS_2 is of particular interest due to its semiconducting nature and indirect bandgap, on the order of 1.3–1.4 eV in bulk form, and large intrinsic carrier mobility and stability to oxidation.[23–26] The possibility of fabricating field-effect-transistors (FETs) and complementary-metal-oxide-semiconductor (CMOS) circuits has stimulated research into this exciting TMD material. While work on mechanically exfoliated flakes of 2D materials generates valuable insight into the physical and electronic properties of these material systems,[27–29] it is generally accepted that large area synthesis is required to take the research area to the next level.[30–32]

Foremost in that field, atomic layer deposition (ALD) is CMOS compatible and enables precision deposition of large area materials on the nanometer thickness scale with compositional control[33,34] and

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conformity to 3D surfaces at relatively low processing temperatures. WS_2 large area deposition has also been explored using chemical vapor deposition (CVD),[35–38] van der Waals epitaxy,[39,40] and sulfurization of WO_x.[41,42] Notably, ALD chemistry studies of WS_2 synthesis have been undertaken by Heyne *et al.*[43] and Groven *et al.*,[44] demonstrating 3 nm thick thin films in FETs. Furthermore, Balasubramanyam *et al.* produced area-selective ALD WS_2 films in the nanometer range.[45]

For most practical nanoelectronics applications, large-area high-quality thin-films will be required, and this is our focus here. For example, Dorow *et al.*[39,40] and Lin *et al.*[46] fabricated electron devices, and both showed benchmarking of the latest WS_2 thin-film FETs. Schram *et al.* compared ALD and CVD WS_2 FETs with low-temperature device integration flows and highlighted substrate adhesion issues.[47] Recently, Yang *et al.*[48] produced impressive ALD WS_2 FET current ratios of 10^5 as well as Nb-doping in ALD deposited WS_2 films;[49] however, those thin films were annealed at high temperatures in a sulfur atmosphere before measuring. In our work, the maximum temperature of processing is 450 °C.

Despite the recent progress, in terms of electronic understanding of ALD WS_2, the number of studies is small, and there are many gaps in the knowledge. With that in mind, we investigate the structural and electrical behavior of ALD-grown WS_2 thin films. We report Hall analysis of the WS_2 films as well as an examination of the temperature dependency of the bulk WS_2 resistivity and specific contact resistivity based on electrical circular transfer length method (CTLM) structures.

WS_2 thin films were synthesized by plasma-enhanced atomic layer deposition (PEALD) in a commercial FlexAL ALD reactor from Oxford instruments. Full details and material characterization of the ALD processes can be found in the work of Balasubramanyam *et al.*[50] The substrates were p-type silicon with 450 nm of thermally grown SiO_2 on the surface. The substrates were treated with a 10 s O_2 plasma (250 W) in the ALD reactor before deposition. The WS_2 films were formed by plasma-enhanced ALD using the $W(NMe_2)_2(NtBu)_2$ precursor with a $H_2 + H_2S$ plasma combination as coreactants. In previous works on WS_2 thin-film synthesis by ALD, there was more discussion on the effects of the H_2S/H_2 ratio as well as XPS results of the WS_2. Further information can be found in Balasubramanyam *et al.*[50,55] Prior to the PEALD process, the samples were subjected to a 20 min preheating step in a 200 mT Ar environment. For the films characterized in this work, depositions were carried out at 450 °C.[50,55]

Transmission electron microscopy (TEM) cross-sectional analysis was performed using a JEOL 2100 HRTEM operated at 200 kV in Bright Field mode using a Gatan Double Tilt holder. Raman spectra were collected using a Renishaw Invia Raman microscope equipped with a 514 nm laser at a power of ≈0.5 mW. The laser spot size was ≈5 μm. Atomic force microscopy (AFM) data were acquired both before and after device processing using a Bruker Dimension Icon. Peak force tapping scanning with SCANASYSTAIR AFM probes was performed. A surface roughness study was done to understand the impact of vertical growth of "fins" of WS_2.

Hall effect measurements at room temperature were performed using a Lakeshore HMS 8404 Hall Measurement System with both DC and AC magnetic field capability. Both DC and AC magnetic field methods were used, with field reversal strength of ±1.7 T for the DC technique and +1.2 T_{rms} for the AC method. A Hall factor of unity is assumed in the absence of literature guidance. To remove errors, geometry and current reversal procedures were used. Two-point (2P) and four-point (4P) resistance/resistivity measurements were also performed with the Hall measurement system.

The CTLM structures were fabricated by UV lithography and patterning Ni/Au metal stack using the standard liftoff process. A 20 nm Ni layer was used as the adhesion layer underneath a 200 nm Au layer. The temperature-dependent electrical measurements on CTLMs were performed using an Agilent B1500A semiconductor device analyzer with a Cascade Microtechprobe station (model Submit 12971B). The range of measurement temperatures was between −50 and +90 °C, with 20 °C intervals.

First, Raman spectra of the multi-layer WS_2 were studied, as shown in Fig. 1(a). For WS_2, the Raman spectra includes two Brillouin zone first order modes—$E_{2g}{}^1$ and A_{1g}. There is also a longitudinal acoustic mode at the M point—2LA(M). At $\lambda_{exc} = 514$ nm, the $E_{2g}{}^1$ peak is found at 356.6 cm^{-1} and the A_{1g} at 419.0 cm^{-1}. These results follow those found in the literature.[51] It must be noted that the $E_{2g}{}^1$ is broad since the 2LA(M) mode is also present (approximately within 5 cm^{-1}).[52] Cross-sectional TEM images of the WS_2 films are shown in Figs. 1(b) and 1(c). The cross-sectional analysis reveals the layered structure of WS_2 where the layered structure is primarily parallel to the SiO_2 surface. The average thickness of the WS_2 film is approximately 8 nm, corresponding to 13 monolayers of WS_2, with an interlayer spacing of 0.62 nm. It was found that uniform films formed from fewer ALD cycles. The TEM analysis also indicates some out-of-plane features, which can be at an angle to, or perpendicular to, the WS_2 film, and further investigations into these fin-like structure is discussed in Balasubramanyam *et al.*[55] The height of the perpendicular feature in Fig. 1(c) is approximately 10 nm above the planar WS_2 surface.

Figure 2 shows an AFM 10 × 10 μm^2 scan of the WS_2 thin film before CTLM device processing. The pre-device process root mean square (RMS) gave a value of approximately 1.3 nm, while a post-

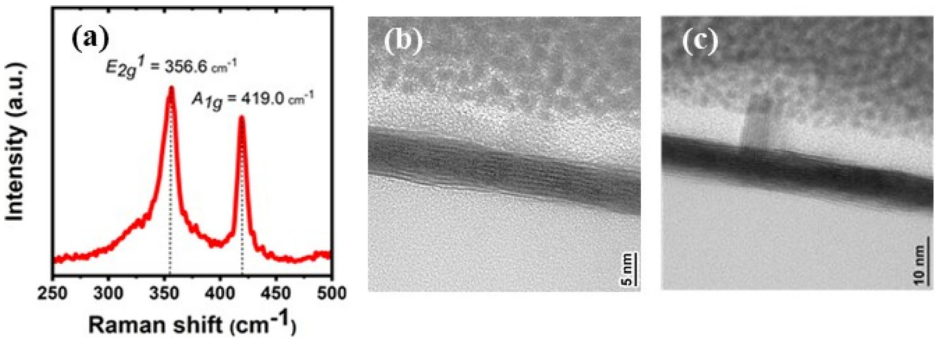


FIG. 1. (a) Representative Raman shift data of WS_2 pre-device processing showing the presence of characteristic WS_2 peaks—$E_{2g}{}^1$ and A_{1g}. (b) and (c) Representative cross-sectional TEM images of the thin-film WS_2 on SiO_2 pre-device processing, for the most part with the desired horizontal basal-plane orientation, along with a few out of plane features.

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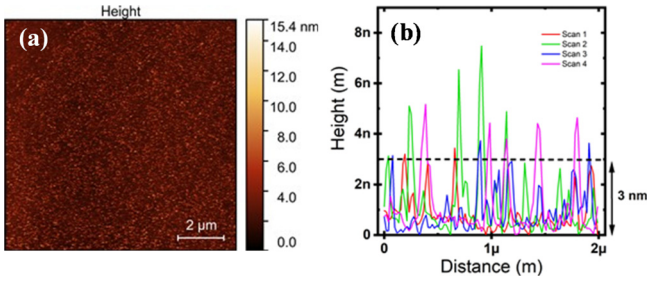


FIG. 2. (a) Representative $10 \times 10\ \mu m^2$ scan cross-sectional AFM image of WS_2 pre-device processing. (b) Graph of 4 (of 20) line profiles from (a) with a length of 2 μm.

device process AFM scan gave a value of 3.8 nm. The fabricated devices were subjected to the thermal budgets of resist processing (e.g., baking, approximately 120–150 °C), but were not annealed outside of that. We theorize that this increase in surface roughness is possibly linked with natural degradation over time[29] as well as some ambient contaminants[53,54] and the factors associated with device processing such as resist spinning and baking, UV exposure, metal deposition, and metal liftoff for contact pad formation. These vertical fins have already been investigated by Balasubramanyam *et al.*, which showed a reduction of vertical nanostructure using H_2 plasma during growth.[55] In our analysis, we focus on the AFM-based characterization of these vertical features. Here, these fins survived the device processing, as Fig. 2(b) shows a graph representing 4 of 20 different line profiles within the $10 \times 10\ \mu m^2$ scan. The profile lines were taken at different orientations and directions. However, it must be noted that the orientation of the fins do not impact the AFM scans due to the scale at which it is tested. The 3 nm scale bar shows the general surface roughness, while the peaks above that we theorize to be the fin features. A statistical analysis on the number of peaks per 2 μm, which was considered as the smallest length of AFM that could be tested with reliable results per sample. Over 20 scans, the average number of peaks is 4.25. If we compare this to work done by Balasubramanyam *et al.*, we find a close correlation between the two. The width of the fins cannot be picked up on these particular line scans, just the height. This is due to the width and length of the fins being around 5 and 25 nm, and the step size of the AFM line scan is 25 nm, while the scan covers 2 μm with a 25 nm step size. Consequently, whatever the orientation of the fin to the line scan, the height is the only parameter affecting them. Figures 1(b) and 1(c) showed that some fins grow at an angle, while others grew directly vertical.

There is very limited data available regarding Hall measurements of TMD materials, primarily taken from flakes mechanically exfoliated from crystals,[56] while for ALD or CVD deposited WS_2 thin films, the mobility values reported in the literature are field effect mobility values extracted from transistor characteristics. In this work, we analyzed the Hall effect mobility of the WS_2 films prior to any device fabrication. Two-point (2P) resistance, four-point (4P) resistivity, and DC/AC Hall-effect analysis were carried out on a 1 cm^2 sample at room temperature. It was only possible to obtain results from 2P, 4P, and DC Hall measurements (AC Hall failed due to a low signal to noise ratio, SNR). 2P Ohmic average resistance showed $1.6 \times 10^7\ \Omega$. 4P resistivity measurements gave a signal to noise ratio (SNR) of 370:1 at room temperature (21 °C). The results showed a 4P average resistance of $5.5 \times 10^5\ \Omega$, with a 4P sheet resistance (R_{sh}) of $2.4 \times 10^6\ \Omega$/sq and 4P resistivity (ρ) of 2.0 Ω cm. The DC Hall results can only be described as weakly indicative since the SNR is only 3.8:1. The same can be inferred on a number of other parameters extracted from the DC Hall results, which indicate p-type WS_2 with a mobility of approximately 23.2 cm^2/V s and carrier concentration of $1.31 \times 10^{17}\ cm^{-3}$. It is encouraging to p-type conduction in TMD thin-films, as it is less common than n-type, and, of course, is desired to make CMOS circuits from both n-type and p-type channels.[57]

While, our DC Hall results had a SNR of 3.8:1, it is noted that Ballif *et al.*[58] also observed p-type behavior in thin-film WS_2 (100–200 nm) with Hall mobility of 10 cm^2/V s. By contrast in that work, the WS_2 was formed by reactive rf sputtering of a S-rich WS_{3-4} film, which was subsequently annealed for 1 h under argon flow at 850 or 950 °C. Moreover, in the work of Lin *et al.*,[30] the Hall mobility benchmark plot showed that chemical vapor deposition (CVD) MoS_2 had a Hall mobility of approximately 20 cm^2/V s for 8–9 layer thick films, which is not far off the indicative value we have found in this work.

We can also compare the Hall values to the temperature-dependent electrical measurements. The CTLM structures had an inner diameter of 25 μm, and the electrode gap values available were 2–125 μm. Note, as the contact resistivity to TMD devices continues to be researched by many expert groups, and progress will be made down to lower and lower values, and sub-micron dimensions for contact studies will become essential in future studies. Further details of our approach to CTLM processing and parameter extraction can be found in our previous works.[59,60] CTLM structures on WS_2 were tested electrically between −50 and +90 °C. Figures 3(a) and 3(b) show an optical image of the CTLM structures and a schematic diagram of the parameters, respectively. At each temperature, the sample showed Ohmic behavior, as seen in Fig. 3(c). The total resistance vs electrode separation was derived using standard methods by applying a geometrical correction factor[61] and is shown in Fig. 3(d). From this total resistance, a number of parameters can be extracted. The sheet resistance (R_{sh}) at room temperature is calculated at $1.58 \times 10^7\ \Omega$/sq. Transfer length gives 1.73×10^{-4} cm, a specific contact resistivity (ρ_c) of 0.46 Ω/cm^2 and contact resistance (R_c) of $1.71 \times 10^5\ \Omega$.

Table I compares 4P and CTLM results at room temperature. The R_{sh} value obtained from the CTLM structures is approximately six times larger than that from the unprocessed WS_2 film. We attribute this to the impact of the processing required to form the CTLM structures, which involves the deposition of resist, UV exposure, metal deposition, and a liftoff process. It is noted that from the Hall analysis of the film, the hole carrier concentration is $1.31 \times 10^{17}\ cm^{-3}$. For a film thickness of 8 nm, this corresponds to a total sheet charge of $1.54 \times 10^{11}\ cm^{-2}$. It is expected that the exposed WS_2 surface will have a surface charge, and any change in this surface charge density during the CTLM processing will change the associated R_{sh} of the WS_2. Any slight change to the surface, in this case, due to metal patterning, will impact the R_{sh}. Connecting this consideration with the AFM data shows a change in surface roughness following device processing; it is not surprising that there is a difference in R_{sh} values obtained from the Hall analysis and the CTLM data.

The temperature dependence of the WS_2 resistivity (ρ) and specific contact resistivity (ρ_c) are shown in Fig. 4, where an activation

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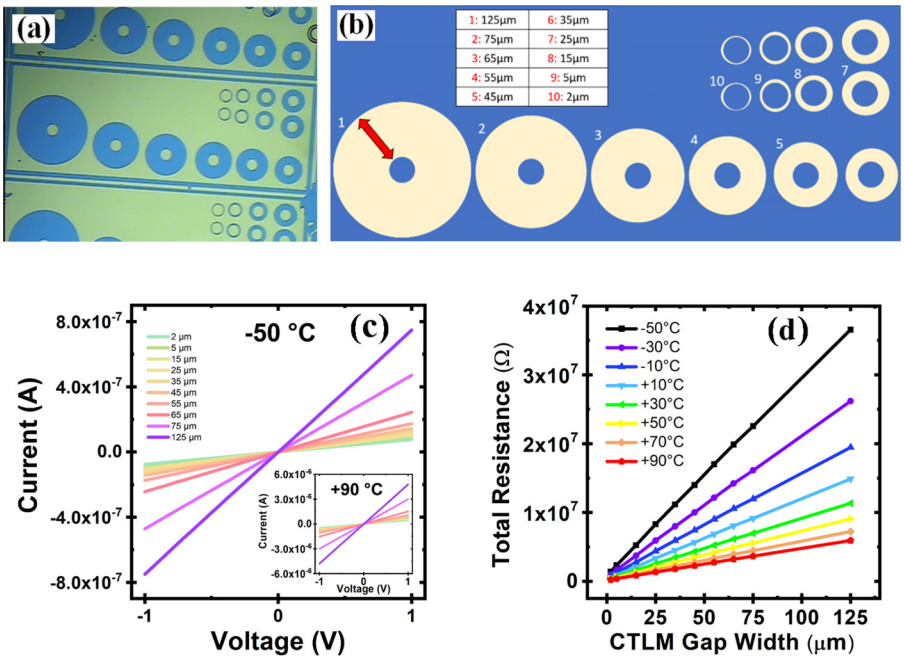


FIG. 3. (a) Optical microscope image of the CTLM structures. (b) Schematic diagram of CTLM structures. (c) Electrical data from the CTLM devices. Representative current vs voltage taken on each site at −50 °C for different gap spacings in the CTLM structure. Inset shows data at +90 °C. (d) Total resistance for each gap spacing at various temperatures after applying the usual CTLM geometrical correction factor.

TABLE I. Resistive properties of WS_2 from four-point probe (4P) before device fabrication and CTLM electrical data after device fabrication.

Property	Units	4P (pre-device fabrication)	CTLM (post-device fabrication)
Resistivity (ρ)	Ω cm	2.0	12.9
R_{sh}	Ω/sq	2.38×10^6	1.58×10^7
R_c	Ω	1.58×10^7	1.71×10^5

energy (E_a) is extracted for each. For specific contact resistivity, E_a is determined primarily by the doping concentration in the WS_2, as it controls the barrier height and tunneling distance at the metal–TMD contact. For the bulk WS_2 resistivity, E_a can be influenced by both mobility and carrier concentration temperature dependence. The E_a of specific contact resistivity (100 meV) and WS_2 resistivity (91 meV) are close in value. With both having nearly equal values, and with carrier concentration temperature dependence present for both ρ and ρ_c; we therefore theorize that carrier concentration dominates the E_a for both parameters, and, thus, there is a lower impact of the carrier mobility temperature dependence in these WS_2 thin films.

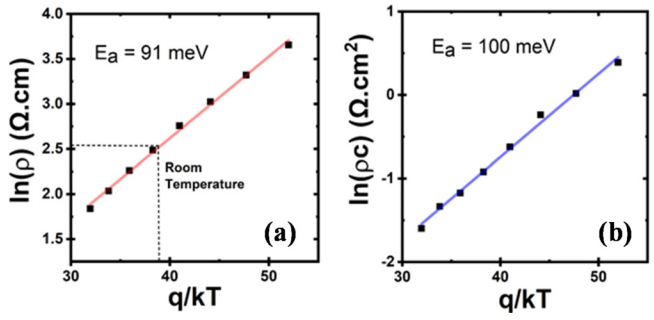


FIG. 4. (a) Extraction of activation energy of resistivity, with highlighted resistivity value at room temperature. (b) Extraction of activation energy of specific contact resistivity. Based on the electrical data from the CTLM resistor devices.

In summary, our work demonstrates that these plasma ALD deposited 8 nm WS_2 thin films exhibit a p-type behavior with the unintentional active doping concentration of 1.31×10^{17} cm^{-3} and an indicative hole mobility comparable to that of 8–9 monolayer CVD MoS_2 thin films. Analysis of the temperature dependence of the WS_2 resistivity and the specific contact resistivity between the WS_2 and the Ni/Au contacts indicates similar E_a values of 91 and 100 meV, consistent with both E_a values being controlled by the temperature dependence of the hole concentration.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Emma Coleman: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Scott Monaghan:** Conceptualization (equal); Data curation (equal); Formal analysis

28 August 2023 09:40:34

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(equal); Investigation (equal); Writing – review & editing (equal). **Farzan Gity:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Gioele Mirabelli:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Ray Duffy:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Brendan Sheehan:** Data curation (equal). **Shashank Balasubramanyam:** Data curation (equal); Formal analysis (equal); Investigation (equal). **Ageeth A. Bol:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Writing – review & editing (equal). **Paul K. Hurley:** Formal analysis (equal); Funding acquisition (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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28 August 2023 09:40:34

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