Degradation dynamics and breakdown of MgO gate oxides

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Abstract

The degradation dynamics of magnesium oxide (MgO) layers in MOS structures has been investigated. It is shown that the shift of the conduction characteristics caused by both ramped and constant voltage stresses is well described by power-law models and that the signature of charge trapping is still visible even after the dielectric breakdown (BD) of the insulating film. The occurrence of progressive BD in 20-nm thick films is also reported.

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1. Introduction

Charge trapping in MOS structures has been extensively investigated in the past, mainly in connection with thick SiO_2 films (>10 nm) [1]. However, with the advent of new large integration technologies based on the replacement of SiO_2 by alternative materials with higher permittivities and larger physical thicknesses, the issue of charge trapping in gate dielectrics has attracted renewed attention [2]. Two critical consequences of this phenomenon include a hysteresis effect in the C-V curve and a shift of the I_D-V_G characteristic in MOS transistors that leads to threshold voltage instabilities. In this paper, the degradation dynamics of MgO layers grown on Si substrates is explored in order to achieve better insight into its feasibility as a gate insulator. This alkaline earth oxide shows some interesting features such as: a large band gap in the range 7.3-7.8 eV [3,4] that ensures sufficient large band offsets with Si and therefore a low leakage current; a dielectric permittivity κ ranging from 6.7 [5] to 10 [4]; high thermal conductivity suitable for power applications [4]; higher breakdown field (12 MV/cm) compared to SiO_2 [4]; and chemical inertness that seems to minimize the formation of an interfacial layer when deposited onto Si substrates [3]. The trap creation and charge buildup in MgO is monitored by means of ramped voltage stress (RVS), constant voltage stress (CVS), and progressive voltage stress (PVS), and the results are analyzed using a previously published model for the degradation dynamics of high-κ gate dielectrics [6].

2. Sample Details

Hydrogen terminated Si surfaces were prepared by dipping n and p-type (100) Si wafers ($10^{15}cm^{-3}$) in a solution of 5% HF, rinsed in D.I. water, then dried using nitrogen

gas and immediately loaded into the deposition system. 20 nm thick MgO films were deposited by electron beam evaporation from 99.9% MgO pellets at a rate of 0.2 Å/s at 180 ^{o}C. For the NiSi gate process, nickel was deposited ex-situ by e-beam evaporation (~80 nm) through a patterned resist mask and subsequent lift-off process. The RTA is a one step process at 500 ^{o}C for 30 s in N_2. Following excess Ni removal in H_2O:H_2SO_4 (1:3), the silicon outside the capacitor area was removed by reactive ion etching using SF_6. From the C-V measurement in accumulation, the permittivity of the MgO films was calculated as 8.1. The dimensions of the capacitor devices tested are 40x40 μm^2.

3. Experimental results and analysis

Figure 1 shows a sequence of J-V characteristics measured on a p-type Si sample after the application of RVS (successive voltage sweeps with an end voltage V_{max}=10 V). Notice the shift of the curves towards higher voltages, a behavior that is compatible with negative charge trapping within the insulator. Identical results are obtained for the n-type Si samples. The most important change takes place after the first sweep and any subsequent stress does not significantly alter the slopes of the characteristics. The difference between the initial and subsequent I-Vs can be attributed to the large generation of defects caused by the first sweep and the trapped charge distribution effect on the potential barrier profile [1,7]. Similar results are obtained for a CVS sequence (see Fig. 2). Again, the gate current decrease is consistent with negative charge trapping and the most important effect takes place after the first stress. As shown in the same figure, the J-t curves are well described by the power-law model $J=J_0t^{-\alpha}$ as proposed in [6] for HfO_2 and Al_2O_3, where J_0 and α are voltage dependent constants. In order to show the accuracy of the considered model, Fig. 3 exhibits a fitting result using linear

axes. In addition, Figs. 4a,b and 5 show that power-law expressions can also be used to model the gate voltage shift at a constant current (ΔV_g@J=const.) in n and p-type samples, and the gate current density at a constant gate voltage (J@V_g=const.) as functions of the voltage sweep number after RVS, respectively. As illustrated in Fig. 6, the MgO layers exhibit progressive BD during a CVS [8]. This stage of degradation corresponds to the earliest manifestation of the formation of a leakage spot and is frequently observed in oxides which are much thinner (<2 nm in SiO_2) than the one studied here. Notice that the current fluctuations follow the decreasing trend associated with charge trapping (localized and distributed conduction mechanisms in parallel). Finally, in order to capture the complete picture of the degradation-breakdown process, a PVS sequence with incremental voltage ΔV_g=0.2 V was applied to an n-type Si sample. Figure 7 shows three distinctive failure mechanisms: uniform charge trapping, progressive BD, and soft BD. This latter regime corresponds to the complete formation of a BD spot with transmission probability lower than unity [8]. Whereas for progressive BD the curves are very unstable and do not have a clear current-voltage relationship, the soft BD I-V characteristics exhibit the typical power-law voltage dependence $I=aV^b$, where *a* and *b* are constants, in a voltage range (~10V) that largely exceeds the average voltage range reported for the observation of SBD in SiO_2 (~5 V in [8]). Further degradation leads to the diode-like behavior typical of hard BD.

4. Conclusions

The voltage and current shifts occurring in metal gate/MgO/Si structures caused by electrical stresses were investigated. It was shown that the first stress is the one that causes the largest damage to the samples. Subsequent stresses only produce an almost parallel shift of the conduction characteristics. The shifts both in current and voltage can

be fitted by power-law expressions as functions of the stress time and voltage sweep number. The degradation eventually leads to the formation of soft breakdown sites so that localized currents flow in parallel with a distributed current. To our knowledge, progressive and soft breakdown in a 20 nm-thick high-κ dielectric layer have never been reported before.

Aknowlegments

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Figure captions

Fig. 1- J-V characteristics after negative bias ramped voltage stress (RVS) with maximum end voltage 10 V. Notice that the largest effect is observed after the application of the first voltage sweep.

Fig. 2- J-t curves after a CVS sequence with Vg=-7 V. Notice that the largest effect is observed after the application of the first stress. The solid lines correspond to the power-law model described in the text.

Fig. 3- Detail of the fitting of an I-t curve after a CVS. In order to show the accuracy of the considered expression, linear axis scales were used.

Fig. 4- Gate voltage shifts at constant current levels for a) n and b) p-type Si samples after RVS as function of the voltage sweep number. In all cases, the experimental data can be fitted by power-law expressions. *a* and *b* are the parameters of the model. Data extracted from Fig. 1.

Fig. 5- Current density decrease for different voltage levels after RVS as function of the voltage sweep number. Again, the experimental data can be fitted by power-law expressions where *a* and *b* are the model parameters. Data extracted from Fig. 1.

Fig. 6- Detection of the onset of progressive BD during a constant voltage stress. Notice that the post-BD current exhibits the signature of charge trapping.

Fig. 7- Effect of progressive voltage stress on the I-V characteristics: charge trapping, progressive BD, and soft BD.

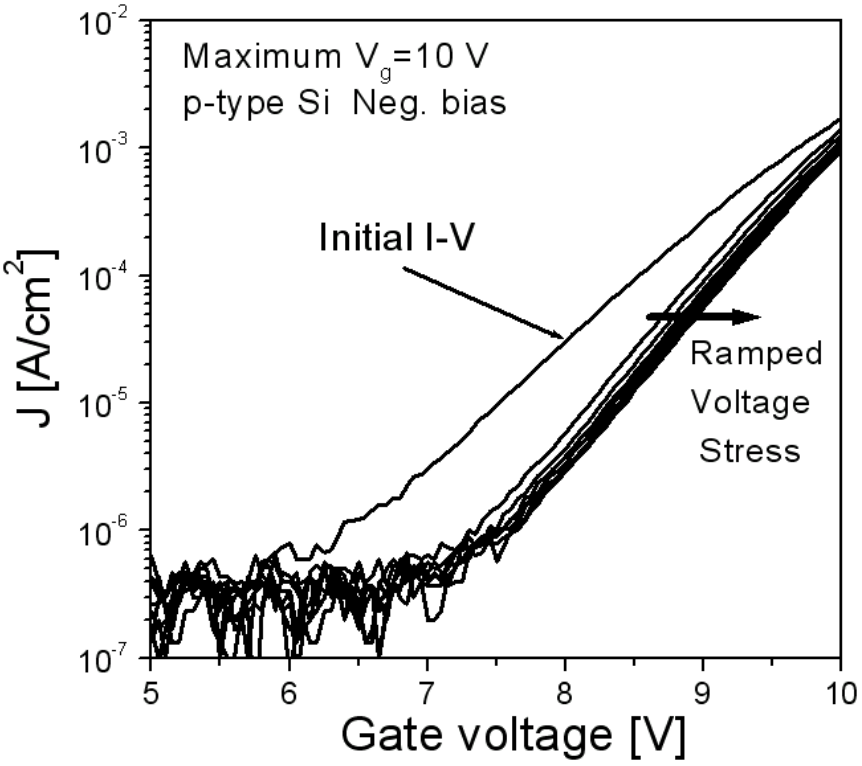
Maximum V_g=10 V
p-type Si Neg. bias
Initial I-V
Ramped
Voltage
Stress
J [A/cm^2]
Gate voltage [V]
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
5
6
7
8
9
10

FIGURE 1

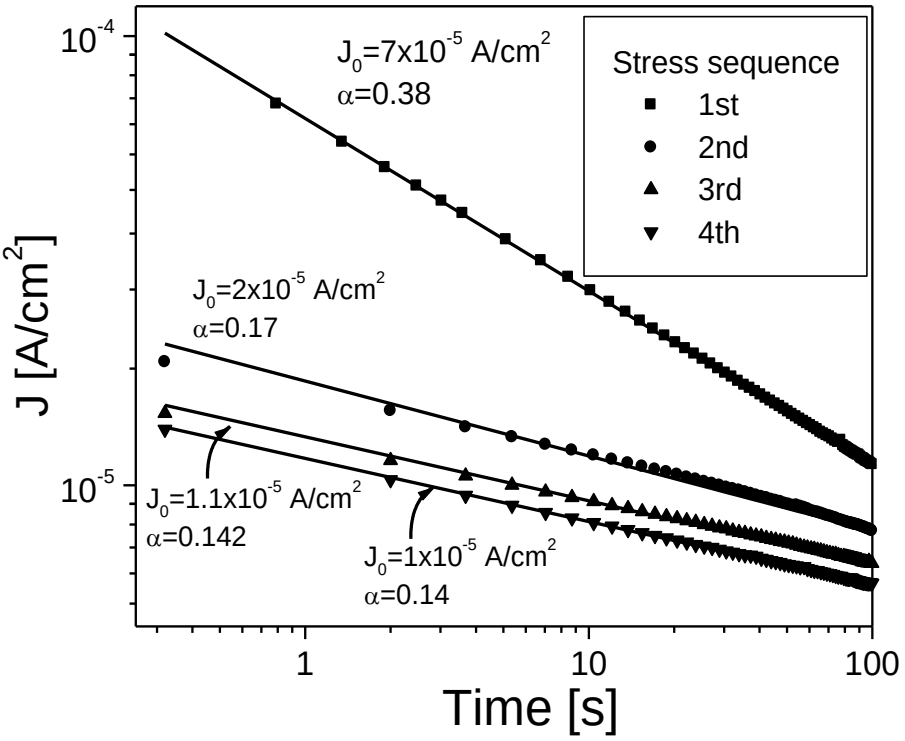
10^{-4}
10^{-5}
J [A/cm^2]
1
10
100
Time [s]
J_0=7x10^{-5} A/cm^2
α=0.38
J_0=2x10^{-5} A/cm^2
α=0.17
J_0=1.1x10^{-5} A/cm^2
α=0.142
J_0=1x10^{-5} A/cm^2
α=0.14
Stress sequence
1st
2nd
3rd
4th

FIGURE 2

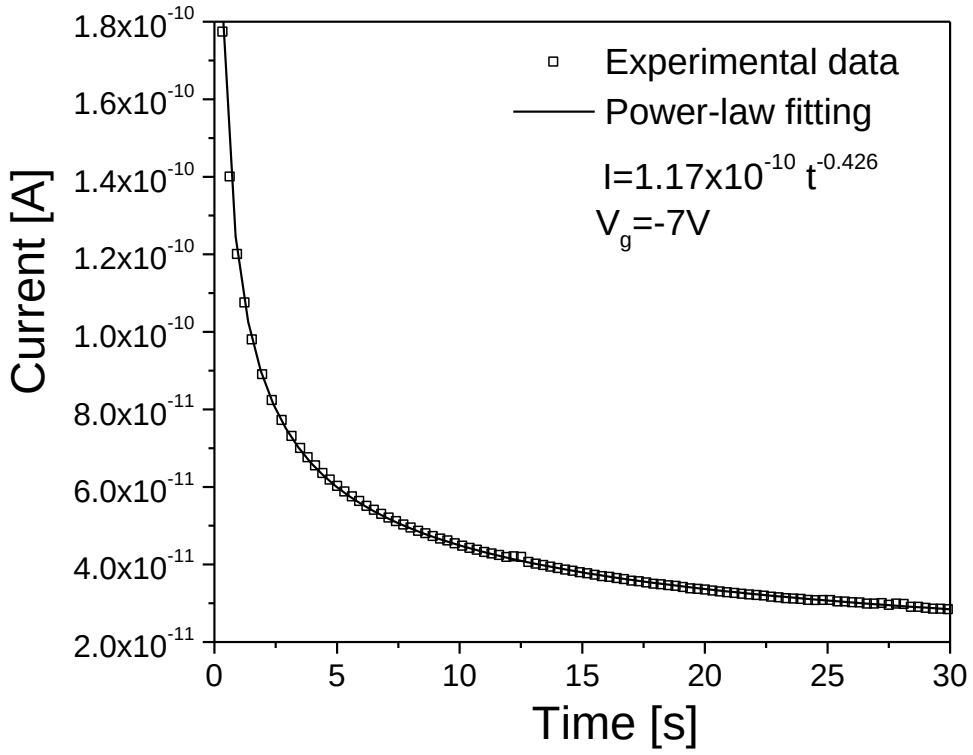
Current [A]
1.8x10-10
1.6x10-10
1.4x10-10
1.2x10-10
1.0x10-10
8.0x10-11
6.0x10-11
4.0x10-11
2.0x10-11
0
5
10
15
20
25
30
Time [s]
Experimental data
Power-law fitting
I=1.17x10-10 t-0.426
Vg=-7V

FIGURE 3

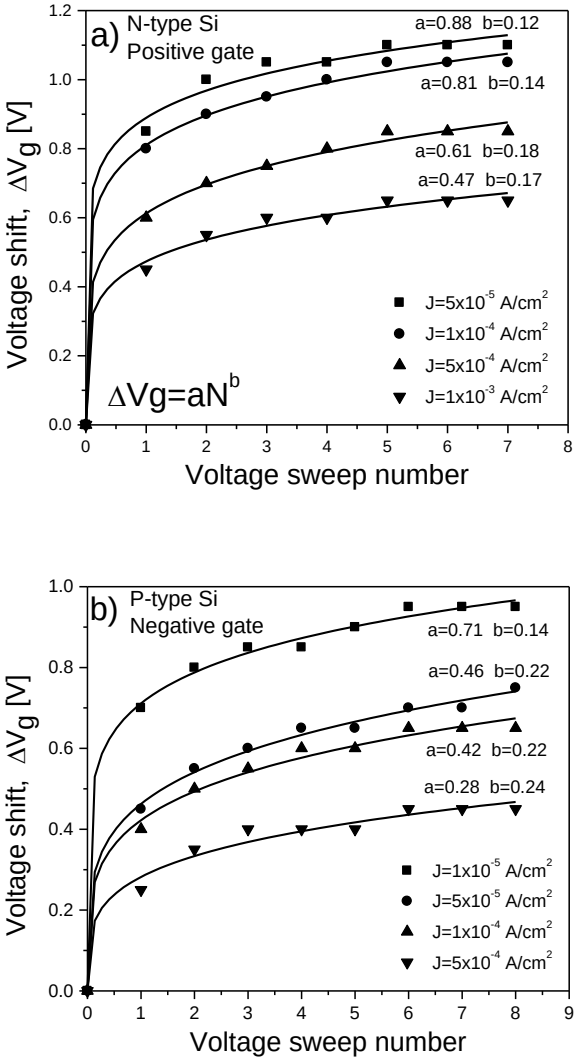
a) N-type Si
Positive gate
a=0.88 b=0.12
a=0.81 b=0.14
a=0.61 b=0.18
a=0.47 b=0.17
J=5x10-5 A/cm2
J=1x10-4 A/cm2
J=5x10-4 A/cm2
J=1x10-3 A/cm2
ΔVg=aNb
Voltage shift, ΔVg [V]
Voltage sweep number
b) P-type Si
Negative gate
a=0.71 b=0.14
a=0.46 b=0.22
a=0.42 b=0.22
a=0.28 b=0.24
J=1x10-5 A/cm2
J=5x10-5 A/cm2
J=1x10-4 A/cm2
J=5x10-4 A/cm2
Voltage shift, ΔVg [V]
Voltage sweep number

FIGURE 4

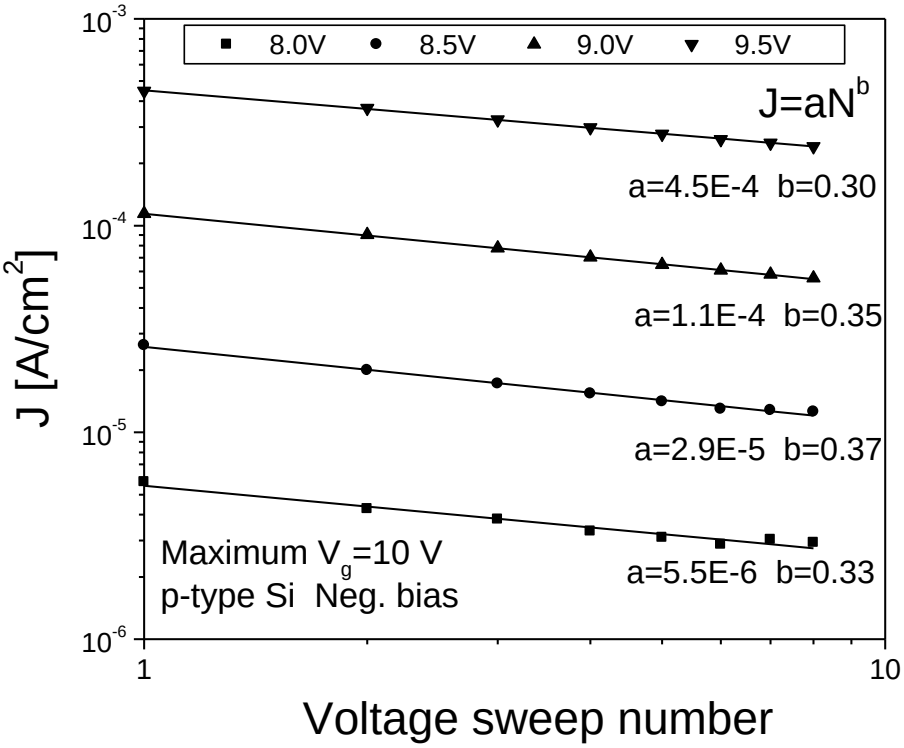
8.0V
8.5V
9.0V
9.5V
J=aN^b
a=4.5E-4 b=0.30
a=1.1E-4 b=0.35
a=2.9E-5 b=0.37
a=5.5E-6 b=0.33
Maximum V_g=10 V
p-type Si Neg. bias
J [A/cm^2]
Voltage sweep number
10^-3
10^-4
10^-5
10^-6
1
10

FIGURE 5

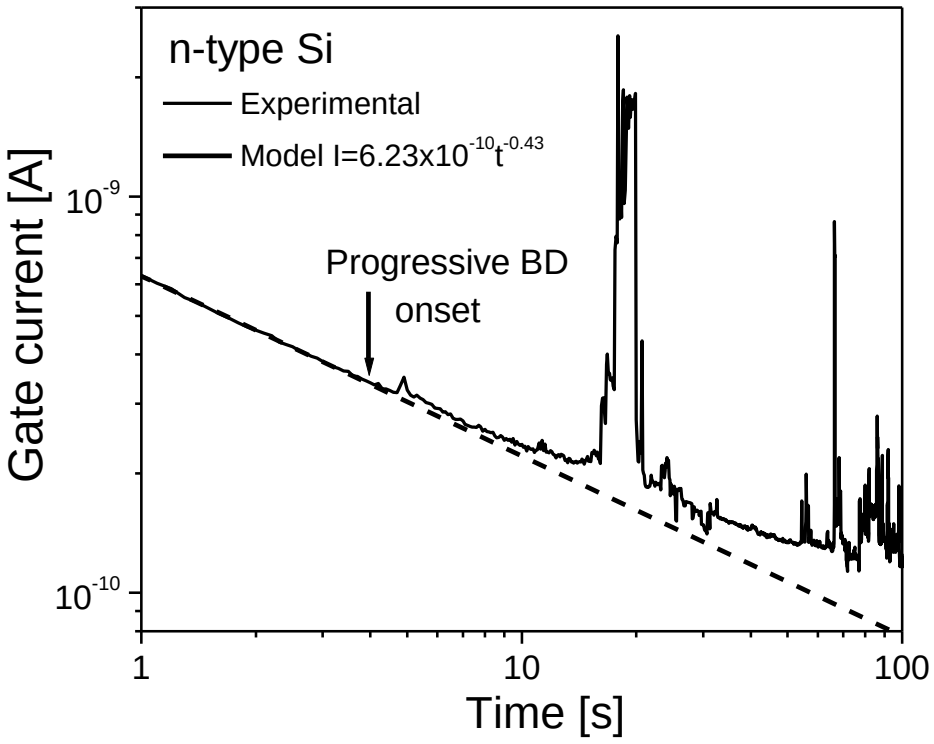
n-type Si
Experimental
Model I=6.23x10^-10 t^-0.43
Progressive BD
onset
Gate current [A]
10^-9
10^-10
1
10
100
Time [s]

FIGURE 6

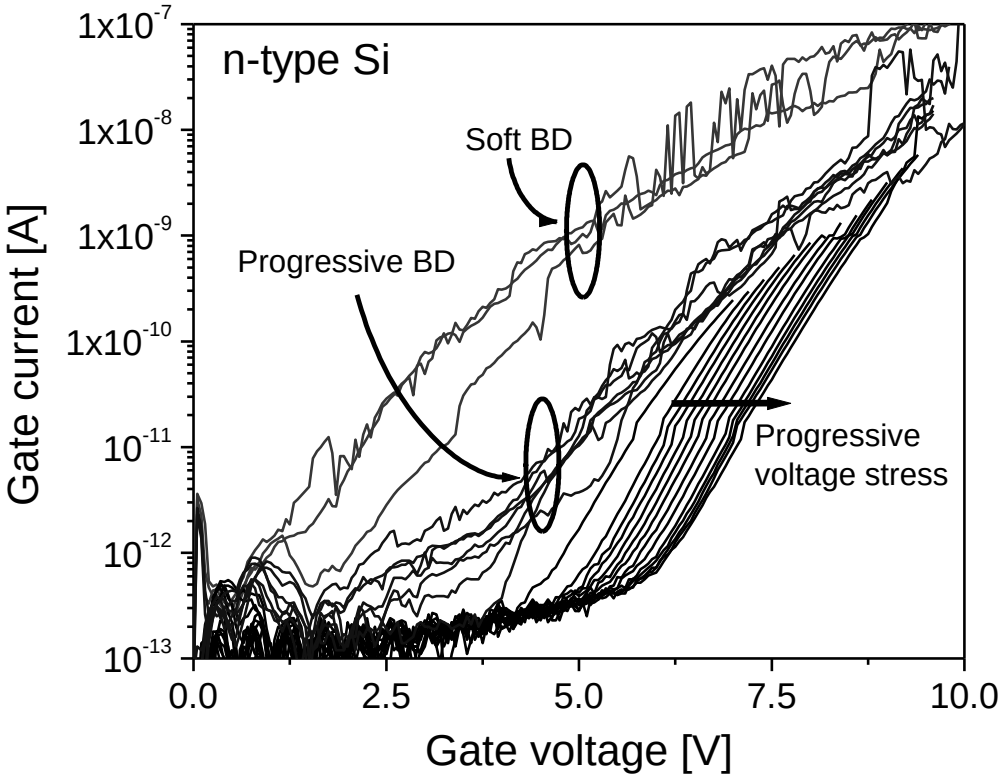
n-type Si
Soft BD
Progressive BD
Progressive
voltage stress
Gate current [A]
Gate voltage [V]
1x10-7
1x10-8
1x10-9
1x10-10
10-11
10-12
10-13
0.0
2.5
5.0
7.5
10.0

FIGURE 7