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Systematic Modeling of Electrostatics, Transport, and Statistical Variability Effects of Interface Traps in End-Of-The-Roadmap III-V MOSFETs

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***Abstract*— Thanks to their superior transport properties, Indium Gallium Arsenide (InGaAs) Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) constitute an alternative to conventional Silicon MOSFETs for digital applications at ultra-scaled nodes. The successful integration of this technology is challenged mainly by the high defect density in the gate oxide and at the interface with the semiconductor channel, which degrades the electrostatics and could limit the potential benefits over Si. In this work, we *i)* establish a systematic modeling approach to evaluate the performance degradation due to interface traps in terms of electrostatics and transport of InGaAs Dual-Gate Ultra-Thin Body (DG-UTB) FETs, and *ii)* investigate the effects of random interface-trap concentration as another roadblock to the scaling of the technology, due to statistical variability of the threshold voltage. Variability is assessed with a Technology CAD (TCAD) simulator calibrated against Multi-Subband Monte Carlo (MSMC) simulations. The modeling approach overcomes the TCAD limitations when dealing with ultra-thin channels (i.e., below 5 nm) without altering crucial geometrical parameters that would compromise the dependability of the variability analysis. Our results indicate that interface-trap fluctuation becomes comparable with the other variability sources dominating the total variability when shrinking the device dimensions, thus contrasting the trend of reduced variability with scaling. This in turn implies that interface and border traps may strongly limit the benefits of InGaAs over Silicon if not effectively reduced by gate process optimization.**

***Index Terms*— III-V MOSFETs, Variability, Interface Traps, Modeling, Scaling.**

I. Introduction

LOW effective-mass semiconductors such as $In_{0.53}Ga_{0.47}As$ are widely explored as possible replacement of Silicon for end-of-the-roadmap MOSFETs thanks to their high electron mobility and injection velocity [1], [2]. Besides the well-known limit of $In_{0.53}Ga_{0.47}As$ related to the low Density of States (DOS) in thin films operating in the quantum limit reducing the maximum achievable electron density [3], the most detrimental issue related to this technology is the high defect density in the gate oxide and at the interface with the channel [4]–[6]. In fact, defects reduce the electron mobility and degrade the electrostatic integrity of the devices, thus partially compensating the benefits of InGaAs over Si MOSFETs. In addition, another major roadblock to the successful scaling of InGaAs technology is related to the statistical (or local) variability [7] that causes identically drawn devices to have different performance [8].

In this work, we establish a systematic modeling approach that allows assessing the performance degradation due to interface traps (in terms of electrostatic and transport behavior) of DG-UTB devices. In addition, we evaluate the effects of random interface-trap concentration on the variability of the threshold voltage (V_T). The variability analysis is performed with a TCAD simulator via the statistical Impedance Field Method (IFM) [9], [10] that allows obtaining accurate results with limited computational time compared to the more sophisticated approaches of MSMC or atomistic simulators [11]. The design of the DG-UTB devices is developed by following the ITRS indications for Ge/III-V semiconductors [12], carefully adjusted to preserve electrostatic integrity and to limit leakage due to Source-to-Drain Tunneling (SDT) [13]. The device characteristics and associated variability are evaluated with the TCAD simulator with a quantum-corrected Drift Diffusion model (QDD), calibrated against MSMC simulations. The calibration was successfully achieved by implementing a systematic calibration procedure that overcomes the limitations of TCAD related to the electron-wave-function distribution when simulating devices with ultra-thin body (i.e., below 5 nm).

The variability analysis was carried out with the addition of the Interface-Trap Fluctuation (ITF) source to other variability sources, namely: *i*) Random-Dopant Fluctuation (RDF) [14];

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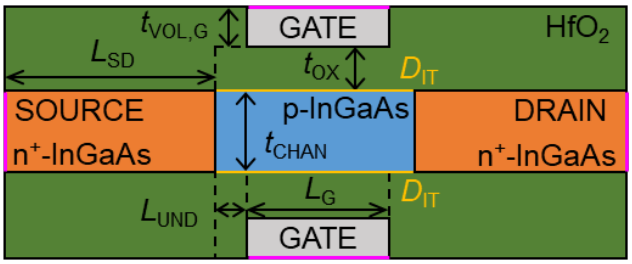


Fig. 1. Schematic view of the simulated Dual Gate – Ultra Thin Body (DG-UTB) device. The geometrical parameters are: L_G = 10.4 nm, t_{CHAN} = 4 nm, t_{OX} = 3.3 nm, $t_{VOL,G}$ = 3 nm, L_{SD} = 22 nm and L_{UND} = 2 nm. D_{IT} indicates the presence of the trap distribution at the interfaces between the channel and the gate oxide. The same parameter set was used for the long-channel device with L_G = 100 nm.

ii) gate metal Work-Function Fluctuation (WFF) [15]; *iii*) InGaAs Band-Gap Fluctuation (BGF) [16]; and *iv*) Body- and Gate- Line-Edge Roughness (BLER, GLER) [8].

The variability analysis here presented complements the research previously carried out by the authors [9], [16], with the inclusion of ITF. Moreover, it allows determining the impact of randomized interface-trap concentration on the total variability providing insights into the limitations of InGaAs-technology scaling. The variability due to random interface-trap density (D_{IT}), trap number, and location was evaluated for Si Multi-Gate (MG) MOSFETs finding that its impact increases due to the generation of defects as a consequence of aging [14], [17], [18]. As InGaAs MOSFETs exhibit higher native D_{IT} (i.e., even before degradation due to aging) compared to Si [19], here we focus on the variability to assess due to native interface traps. The employed D_{IT} energy distribution was derived from a distribution matching experimental data that also reproduced mobility degradation and transfer-characteristic hysteresis in InGaAs devices [5], [13], [19], [20]. The systematic modeling approach developed in this work provides a consistent agreement between QDD and MSMC not only in terms of the transfer-characteristics (I_D–V_{GS} curve) but also in terms of inversion and trapped-charge density in the channel, as well as the mobility. Thus, electrostatic and transport properties were correctly simulated without altering sensitive parameters such as the body/channel thickness as done in previous works [21], which is critical to provide meaningful variability predictions. The methodology developed in this work could potentially be extended to other III-V devices when considering the effects of interface traps on extremely scaled structures for which experimental data is lacking and calibration of TCAD on more sophisticated simulators is required.

The rest of the paper is organized as follows. In Sections II and III, we describe the methodology used to model the interface-trap effects within the MSMC simulations and to calibrate the QDD over the MSMC simulations, respectively. In Section IV, the modeling of the variability sources and the methodology to calculate the performance variations is discussed. Then, the variability results obtained for V_T are shown, along with a discussion on the effects of scaling and a comparison between InGaAs technology and Si. Finally, conclusions follow in Section V.

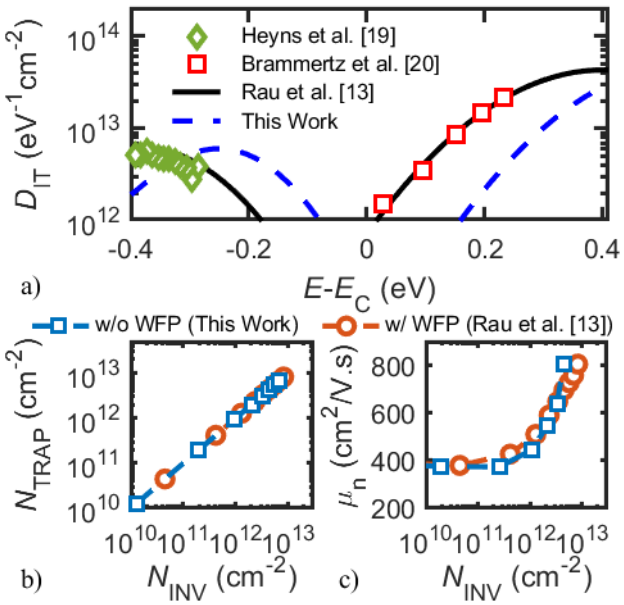


Fig. 2. a) D_{IT} energy distribution employed in the MSMC simulations. The black solid curve is the model proposed in [13] to match the experimental data (green diamond and red square symbols) found in [19], [20], respectively, w/ WFP. The model is then modified to obtain the D_{IT} (blue dashed line) to be used in the QDD and the MSMC w/o WFP. b), c) show the trapped charge density (N_{TRAP}) and electron mobility (μ_n) vs the inversion charge density (N_{INV}) with the two trap distribution [black solid (blue dashed) curve in a) used in the MSMC w/ WFP (w/o WFP)], showing that the proposed approach does not modify the electrostatic and transport behavior of the device even when the WFP in the gate oxide is not accounted for.

II. Multi-Subband Monte Carlo Modeling

The Multi-Subband Monte Carlo (MSMC) simulator [22] employs a non-parabolic effective mass approximation (NP-EMA) energy model [23] for both quantization and transport. The MSMC simulator operates by dividing the device in a finite number of sections along the transport direction. In each section, the 1D Schrödinger equation is solved to obtain the subband profile. The subband occupation along the transport direction is computed by solving the Boltzmann Transport Equation (BTE) with the Monte Carlo method [24]. In this way, far-from-equilibrium transport and quantization normal to the transport direction are accounted for. Interface traps have been introduced in the out-of-equilibrium solution of the coupled Schrödinger and Poisson equations as a sheet of charge at the interface between the channel and the gate dielectric, as reported in [25]. MSMC simulations account for scattering mechanisms, such as elastic intravalley and inelastic intervalley phonons, remote phonons from the high-κ dielectric, local polar phonons, Coulomb, alloy, and surface roughness scattering [24]. The schematic view of the simulated ultra-scaled DG-UTB structure is shown in Fig. 1.

The device considered in this work is a simplified template structure that resembles existing InGaAs technology including only HfO_2 as the gate oxide [26]. Other common device realizations include a thin Al_2O_3 interfacial layer (~5-10 Å) between HfO_2 and the semiconductor [27]. The geometrical parameters are reported in the caption of Fig. 1, and were chosen starting from the semiconductor roadmap (ITRS)

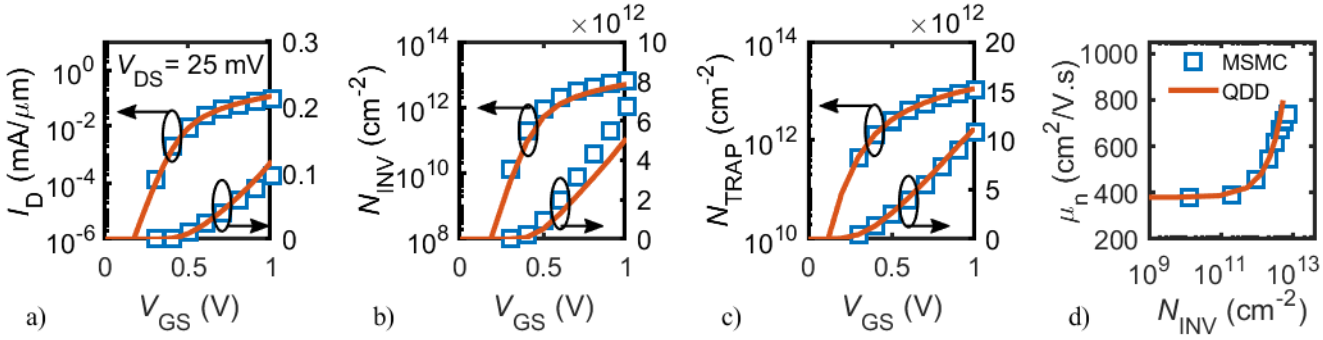


Fig. 3. Calibration of the QDD (orange solid curves) over MSMC (blue square symbols) simulations. The panels show the calibrated I_D–V_{GS} a), N_{INV}–V_{GS} b), N_{TRAP}–V_{GS} c), μ_n– N_{INV} d). The simulated device in this case has a long-channel (L_G = 100 nm) and low bias (V_{DS} = 25 mV) to avoid quasi-ballistic transport and velocity saturation, respectively.

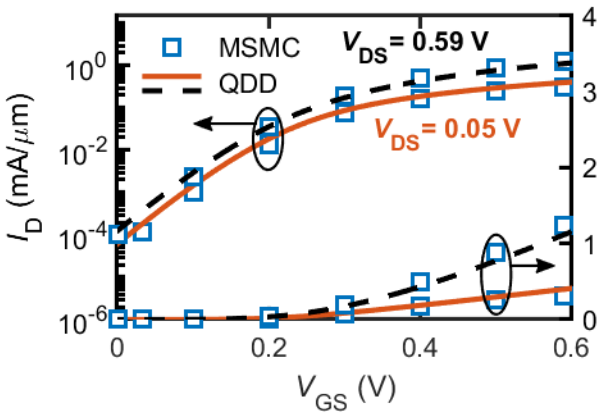


Fig. 4. I_D–V_{GS} calibration of the QDD (orange solid and black dashed curves) over MSMC (blue square symbols) simulations for the ultra-scaled reference device (L_G = 10.4 nm) used in the variability analysis in the linear and saturation regimes.

indications for Ge/III-V semiconductors [12], carefully adjusted to preserve electrostatic integrity in terms of subthreshold slope (SS) and drain-induced-barrier-lowering (DIBL). While MSMC simulations do not take into account possible SS deterioration due to SDT, full-quantum atomistic simulations showed limited V_T-shift (due to SS degradation at given Ioff) for the DG-UTB devices under study [2]. Theoretical studies have also shown that by properly reducing the body thickness and employing sufficiently long underlaps it is possible to downsize DG-UTB InGaAs MOSFETs to L_G = 5 nm [28]. These considerations point to the fact that the SDT in the device under study is not a major concern, allowing the successful scaling down to L_G = 10.4 nm. The modeling of the device electrostatics with the inclusion of interface traps was carried out by: *i*) employing a D_{IT} matching experimentally measured data; *ii)* preserving the device geometry, particularly by not increasing the channel thickness as done in previous works [21]. The latter is a crucial point, since t_{CHAN} strongly influences the variability of the device, especially at ultra-short L_G [9]. In other words, to avoid compromising the dependability of the variability analysis, unaltering t_{CHAN} is mandatory. The reference MSMC simulation setup in this work is taken from [13].

Figure 2a) shows the calibrated distribution (black solid curve) [13], along with the experimental data (green diamond and red square symbols) [19], [20]. The trap distribution in [13] was originally employed to reproduce mobility degradation and transfer-characteristic hysteresis of InGaAs planar devices (as discussed in [5]), and was calibrated on distributions measured on InGaAs MOS test structures [19], [20]. While in general D_{IT} depends on material properties and on process conditions (and thus it is possible to have different D_{IT} for a given oxide/semiconductor interface) we chose this particular distribution because it is representative of actual InGaAs technology, satisfying the constraint *i*) discussed previously. To reproduce the MSMC results with the TCAD simulator, we employed a QDD model that considers both the increased confinement of carriers in the channel and the quasi-ballistic transport at very short channel length. The quantum-correction is implemented by the Modified Local Density Approximation (MLDA) model, [29], that requires no calibration parameter.

Since the QDD, differently from the MSMC, does not consider the electron-Wave-Function Penetration (WFP) in the gate oxide (stemming from the strong geometric confinement due to thin t_{CHAN}), the WFP was turned off in the MSMC as well [30]. To maintain the same results as the MSMC w/ WFP, in the MSMC w/o WFP and QDD setups we employed a modified trap distribution model [blue dashed curve in Fig. 2a)]. Such a distribution was obtained by translating the original model [black solid curve in Fig. 2a)] towards higher energies (compensating for the difference in the first available electron energy level that arises when not considering the WFP). This shift allowed recovering the same relationship between the trapped charge density in the channel (N_{TRAP}) and the inversion charge density (N_{INV}) as compared to that obtained with the MSMC simulations including the original trap distribution and WFP, as shown in Fig. 2b). Thus, the adopted systematic approach allowed preserving the electrostatic properties of the original device even without directly accounting for the WFP. In addition, the surface roughness parameters in the simulation w/o WFP were modified with respect to [13] to compensate for the different wave-function shapes that influence the scattering rates and the electron mobility (μ_n) [31]. After the recalibration, similar μ_n–N_{INV} to that of the original device w/ WFP was achieved, thus preserving the transport properties as shown in Fig. 2c).

The unusual increase of the mobility with inversion charge density is caused by the wave function confinement effect in DG-UTB MOSFETs, which is not observed in single-gate devices (like the mobility reported in [13], obtained with the same surface roughness and Coulomb scattering as well as the

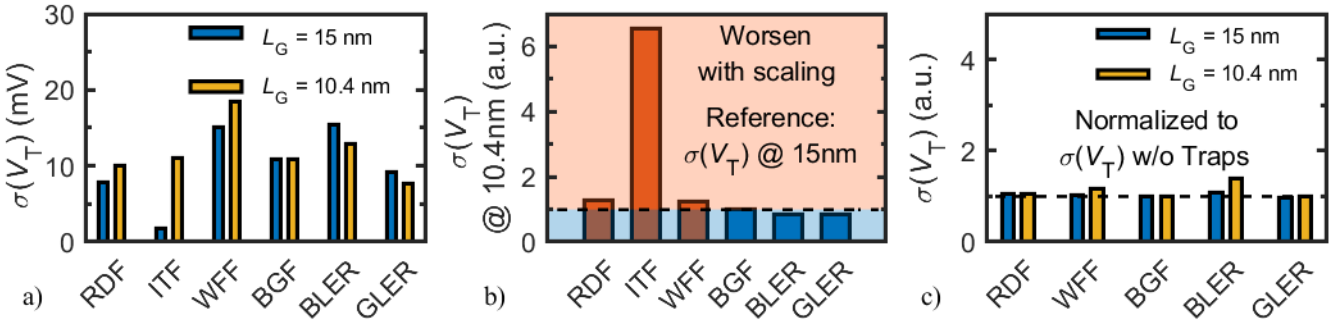


Fig. 5. V_T variations, $\sigma(V_T)$, induced by the six variability sources considered in this work. a) Comparison between the $\sigma(V_T)$ calculated from devices with L_G = 15 nm (blue bins) and L_G = 10.4 nm (yellow bins). b) $\sigma(V_T)$ for the 10.4-nm device normalized to the 15-nm device. Red (blue) bins are the variability sources that worsen (improve) with scaling [i.e., increase (reduce) the induced $\sigma(V_T)$]. c) $\sigma(V_T)$ for both 15- and 10.4-nm devices normalized to the one obtained for devices with the same L_G (respectively) but without interface traps.

TABLE I VARIABILITY SOURCES PARAMETERS: WORK-FUNCTION FLUCTUATION (WFF), BAND-GAP FLUCTUATION (BGF) AND LINE-EDGE ROUGHNESS (LER)

WFF	BGF	Body- and Gate- LER 15 nm (10.4 nm)
Avg. Grain Size = 5 nm	$\delta\chi$ = 10 meV	Λ_{rms} = 1.8 (1.2) nm
	Λ_{BGF} = 300 nm	
P_{WF1} = 60%	α = -1.3	
P_{WF2} = 40%	$\delta E_G = \alpha \times \delta\chi$	Λ_{LER} = 15.5 (8.3) nm

same D_{IT} profile used in this work). In fact, in the case of the DG-UTB MOSFET, the strong geometric confinement causes the device to operate in the quantum limit, with only the first subband of the conduction band being occupied. Thus, with increasing N_{INV}, the Fermi Level penetrates more deeply into the subband (since the charge can only be supplied from this subband) and this in turn leads to an increase of the mobility, as already observed in [32], [33].

III. CALIBRATION OF QUANTUM DRIFT-DIFFUSION SIMULATIONS

In this section, we describe the systematic calibration procedure developed to correctly reproduce both the MSMC electrostatics and transport with the QDD setup. The TCAD simulator employed in this work to implement the QDD model is the commercial software SDevice™ [34]. We employed the same trap distribution as the one used in the MSMC setup [shown in Fig. 2a), blue dashed curve] and calibrated the mobility vs carrier density curve in TCAD. The model employed to reproduce the MSMC mobility curve was the University of Bologna Model [35], available in SDevice™ [34]. The calibration of the mobility model of the QDD vs MSMC was performed on a long-channel device (then used for the short-channel device) (L_G = 100 nm) biased at low V_{DS} (25 mV) to avoid influence of short-channel effects, quasi-ballistic transport and velocity-saturation effects. Besides the calibration of the mobility model, no further parameter adjustment was required to obtain the agreement between MSMC and QDD shown in Fig. 3. The agreement is obtained in terms of a) I_D–V_{GS}, b) N_{INV}–V_{GS}, c) N_{TRAP}–V_{GS}, and d) μ_n–N_{INV} curves. The matching of the electrostatic and transport characteristic between MSMC and QDD was made possible by using the same D_{IT} and mobility curve. This allowed ultimately to reproduce the I_D–V_{GS} curve, as shown in Fig. 3a). The residual discrepancy between MSMC and TCAD [in particular for the N_{INV}–V_{GS} curve, see Fig. 3b)] is due to the different quantization models employed by the simulators [30]. In conclusion, the systematic calibration procedure adopted in this work guarantees that the QDD simulation results are consistent with the MSMC obtained with a trap-distribution model that matches the experimental data, thereby satisfying the two constraints defined in Section II.

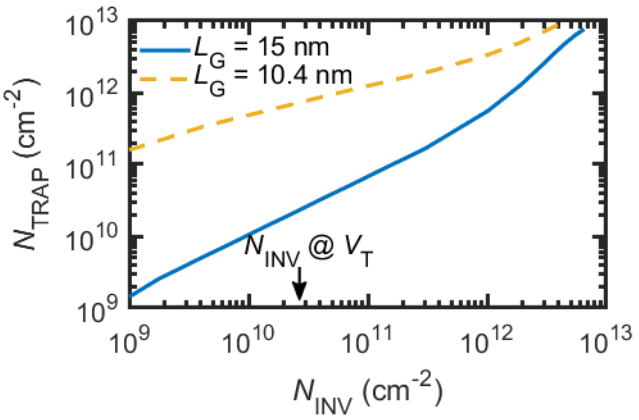


Fig. 6. N_{TRAP} vs N_{INV} for the 15-nm (blue solid curve) and 10.4-nm (yellow dashed curve) devices. The channel thickness t_{CHAN} is 7 nm and 4 nm, respectively. The N_{INV} for the results in Fig. 5, i.e. at threshold condition, is indicated. The increase in trapped charge density for lower t_{CHAN} is explained by the deeper penetration of the Fermi-level in the conduction band, thus probing the trap distribution where the trap density is higher, see Fig. 2a).

The calibrated QDD setup was then used to simulate the ultra-scaled DG-UTB 10.4-nm device and to compare with the MSMC results obtained with the same device geometry. Results are shown in terms of I_D–V_{GS} curves (Fig. 4), for two different V_{DS} biases (for the linear and saturation regimes, respectively). The same models used for calibration of the long channel device were used in this case (with the same parameter values) with the addition of an empirical ballistic mobility model and the Canali model accounting for velocity saturation effects, both available in SDevice™ [34]. The empirical ballistic model provides an additional contribution to the mobility which is L_G-dependent via a calibration parameter that was set in agreement with [36] to correctly reproduce transport in short-channel InGaAs devices. Note that the I_{ON}/I_{OFF} ratio of the DG-UTB device under study is about 4 orders of magnitude (see Fig. 4), which is in line with ITRS requirements [12] as well as state-of-the-art InGaAs Tri-

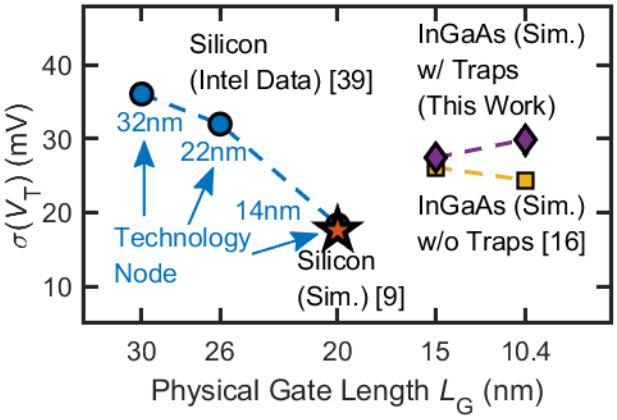


Fig. 7. Comparison of the scaling behavior of total V_T variability, $\sigma(V_T)$, for InGaAs with- (purple diamonds) and without- (yellow squares), from [16], interface traps, Silicon Intel Data (blue dots), from [39], and Si QDD simulations (orange star), [9].

Gate devices on Si-substrates [27], with record value as high as ~2000-2500 (for L_G as low as 13 nm). These remarks demonstrate that although the DG-UTB device in this work represents a simplified version of realistic technology, the variability analysis carried out can be considered to be relevant for current state-of-the-art InGaAs devices.

IV. Variability Analysis

The calibrated 10.4-nm device was then used as a reference to assess the effect of random interface-trap concentration on the variability on V_T. For brevity, we will refer to V_T variability as the standard deviation of the threshold-voltage distribution, $\sigma(V_T)$. The 2D structure of Fig. 1 was protruded in the third dimension by 14 nm (i.e., the gate width) to obtain a 3D mesh for the variability analysis. SDevice™ incorporates the statistical Impedance Field Method (IFM) [10] as an efficient yet accurate tool to assess the impact of several variability sources independently of each other. The statistical IFM treats variability akin to small perturbations of the nominal device [i.e., in this case the device calibrated as in Fig. 4)] by calculating the altered response for a large number M of randomized device realizations (in our case, M = 10,000) as the linear response to the device perturbations via a Green's function-based approach [34]. This is a simplified yet sufficiently accurate and efficient way of assessing variability, as the full (3D) QDD self-consistent device simulation needs to be solved only once. As variability sources, we considered all the relevant microscopic sources known for ultra-scaled MOSFETs [37], i.e.: RDF [14], WFF [15], BLER, and GLER [8]. In addition to these sources, we included BGF [16] and ITF. The modeling parameters adopted for WFF, BGF, B/G-LER are summarized in Table I (more details on the implementation of the randomized distribution for each source are provided in [9], [16]). The dependability of the variability analysis based on the IFM was verified in [9] by matching Si $\sigma(V_T)$ experimental data, due to the lack of the same for InGaAs devices (for statistically meaningful datasets).

BGF stems from the random variations of indium content (i.e., mole fraction) in $In_{0.53}Ga_{0.47}As$ which cause the channel volume to be subject to random variations in the bandgap. BGF is modelled following the approach adopted in [16] with parameters as shown in Table I. ITF reflects the random number of traps present at the interface between the gate oxide and the channel, in a similar way to the discrete random dopants in the semiconductor. Therefore, when constructing the M device samples, at each mesh vertex along the interface, the random number of traps is calculated from a Poisson distribution with an average equal to the nominal number of traps determined from the D_{IT} (shown in Fig. 2a). For the given trap distribution and gate area, we can estimate the (occupied) trap number to span from about 5 to 21 (depending on the position of the Fermi level). We considered the traps to be uniformly distributed (on average), as previous results on similar III-V DG MOSFETs showed that the influence of random single-trap position along the gate interface is negligible [38]. Note that ITF-induced variability (as well as that of the other sources) is obtained from the M device realizations assuming that it causes a small perturbation in the response of the reference device (so that the self-consistent QDD solution is solved only once). Thus, in this work, the trap filling ratio is computed only for the reference solution (for each bias point). This is a simplified approach with respect to more complex atomistic methods, that however require much higher computational effort compared to IFM.

The results of the analysis in terms of $\sigma(V_T)$ are shown in Fig. 5. Figure 5a) shows a comparison between the $\sigma(V_T)$ of the 10.4-nm and the 15-nm device. Variability results for the 15-nm device were calculated from QDD simulations calibrated on MSMC with an effective D_{IT} obtained from the model of Fig. 2a) (black solid curve). The effective distribution was obtained following the same procedure as that described in Section II for the 10.4-nm device, to preserve the N_{TRAP} vs N_{INV} relationship (results not shown for brevity). From Fig. 5a), it can be seen that, upon scaling, both RDF- and WFF-induced $\sigma(V_T)$ increase, BLER and GLER decrease (due to reduction of the associated amplitude, Δ_{rms}, following ITRS, see [9] and Tab. I) and BGF shows a negligible variation. Notably, ITF-induced $\sigma(V_T)$ has a ~6× increase, negatively impacting the total V_T variations. This increase is a consequence of the higher trapped charge density for the scaled device, as shown in Fig. 6. The plot compares N_{TRAP} vs N_{INV} for the 15-nm (blue solid curve) and 10.4-nm (yellow dashed curve) devices. Since the interface traps are Poisson-distributed, if their mean value increases (proportional to N_{TRAP}) then also the standard deviation does, thus explaining the ITF increment shown in Fig. 5a) [14], [17]. The ITF trend is more clearly shown in Fig. 5b), where the $\sigma(V_T)$ for the 10.4-nm device for each source is normalized to that of the respective source for the 15-nm device. These results indicate that scaling strongly worsens ITF. Similar trends of increased trap-induced variability due to higher trapped charge were found also for Si MG-MOSFETs [14], [17], [18]. However, conversely to InGaAs, in Si devices the increased N_{TRAP} was attributed to the effects of aging [14], [18] rather than to increased quantum confinement (which is stronger in InGaAs due to its low effective mass). Stress-induced trap generation is expected to take place in InGaAs devices too, but is out of the scope of the present work.

The effect of interface traps on the $\sigma(V_T)$ induced by all

other variability sources (i.e., other than ITF) can be appreciated with the aid of Fig. 5c). It shows the $\sigma(V_T)$ for both the 15- and 10.4-nm devices normalized to the $\sigma(V_T)$ obtained for the same devices without interface traps. (The reference devices without interface traps were calibrated to MSMC simulations as well, as reported in [16]). Remarkably, for both nodes, the other variability sources appear not to be significantly affected by the presence of interface traps, except for BLER. This result indicates that the device with interface traps is more sensitive to BLER, especially at the 10.4-nm node. This is clear from the fact that electrostatic integrity is reduced by the presence of traps, and, since BLER acts as a random variation of the channel thickness, the V_T fluctuations increase for the trap-affected devices.

The increase of ITF-induced $\sigma(V_T)$ also impacts the total $\sigma(V_T)$ calculated as the quadrature sum of the contribution of all the different sources, assuming each source to be independent of each other (similar to the approach adopted in our previous work [9]). This is shown in Fig. 7, along with data obtained from our previous work without considering interface traps [16] and data for Si devices, from both an existing technology [39] and our results [9]. The comparison shows that InGaAs variability is higher than the latest reported from Intel regarding Si (at the 14nm node) [39], and that is further increased when considering interface traps. Moreover, the scaling of the InGaAs technology further increases the total $\sigma(V_T)$, thereby contrasting the scaling trend of improved performance with reduced dimensions observed in Si technology. This result indicates that the significant increase of variability due to interface traps could be a serious bottleneck for the adoption of InGaAs for ultra-scaled nodes for general purpose digital applications.

V. Conclusions

We presented a systematic modeling approach to evaluate in TCAD the effects of interface traps electrostatics, transport and in DG-UTB III-V MOSFETs. Moreover, we assessed the impact of random interface-trap concentration on the statistical variability of the threshold voltage (V_T) via quantum-corrected drift-diffusion (QDD) simulations calibrated on MSMC results. The systematic modeling approach adopted in this work allowed reproducing a full set of MSMC electrostatic and transport results with QDD simulations by employing the same D_{IT} distribution (obtained from experimental data) and by calibrating the mobility curve. This approach was instrumental to achieve agreement between MSMC and QDD results without altering key geometrical parameters that would compromise the variability analysis. Moreover, our approach is applicable in other extremely scaled III-V devices where experimental data is lacking and comparison between TCAD and more sophisticated simulators is required. From the variability analysis we found that although the most detrimental variability source is the Work-Function Fluctuation (WFF), the contribution of Interface-Trap Fluctuation (ITF) to V_T variability increases significantly when scaling the device dimensions. This is due to the stronger confinement that shifts the Fermi level towards higher energies and thus increases the trapped-charge density. The significant ITF impact on the total V_T variability contrasts the trend of reduced variability with smaller dimensions, as opposite to Si devices. Thus, we conclude that ITF could be a serious bottleneck for InGaAs technology at ultra-scaled nodes for general-purpose digital applications.

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References

[1] J. A. Del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, Nov. 2011. DOI: 10.1038/nature10677.

[2] L. Selmi, E. Caruso, S. Carapezzi, M. Visciarelli, E. Gnani, N. Zagni, P. Pavan, P. Palestri, D. Esseni, A. Gnudi, S. Reggiani, F. M. Puglisi, and G. Verzellesi, "Modelling nanoscale n-MOSFETs with III-V compound semiconductor channels: From advanced models for band structures, electrostatics and transport to TCAD," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2017, pp. 13.4.1-13.4.4. DOI: 10.1109/IEDM.2017.8268384.

[3] M. V. Fischetti, L. Wang, B. Yu, C. Sachs, P. M. Asbeck, Y. Taur, and M. Rodwell, "Simulation of Electron Transport in High-Mobility MOSFETs: Density of States Bottleneck and Source Starvation," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM)*, Dec. 2007, pp. 109–112. DOI: 10.1109/IEDM.2007.4418876.

[4] J. A. Del Alamo, D. Antoniadis, A. Guo, D. H. Kim, T. W. Kim, J. Lin, W. Lu, A. Vardi, and X. Zhao, "InGaAs MOSFETs for CMOS: Recent advances in process technology," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM)*, Dec. 2013, pp. 24–27. DOI: 10.1109/IEDM.2013.6724541.

[5] P. Pavan, N. Zagni, F. M. Puglisi, A. Alian, A. V. Y. Thean, N. Collaert, and G. Verzellesi, "The impact of interface and border traps on current–voltage, capacitance–voltage, and split-CV mobility measurements in InGaAs MOSFETs," *Phys. Status Solidi A*, vol. 214, no. 3, p. 1600592, Mar. 2017. DOI: 10.1002/pssa.201600592.

[6] L. Morassi, G. Verzellesi, H. Zhao, J. C. Lee, D. Veksler, and G. Bersuker, "Errors limiting split-CV mobility extraction accuracy in buried-channel InGaAs MOSFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1068–1075, Apr. 2012. DOI: 10.1109/TED.2011.2182513.

[7] IRDS, "International Roadmap for Devices and Systems (IRDS)," 2017.

[8] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254–1260, May 2003. DOI: 10.1109/TED.2003.813457.

[9] N. Zagni, F. M. Puglisi, G. Verzellesi, and P. Pavan, "Threshold Voltage Statistical Variability and Its Sensitivity to Critical Geometrical Parameters in Ultrascaled InGaAs and Silicon FETs," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4607–4614, Nov. 2017. DOI: 10.1109/TED.2017.2754323.

[10] F. Bonani, G. Ghione, M. R. Pinto, and R. Kent Smith, "An efficient approach to noise analysis through multidimensional physics-based models," *IEEE Trans. Electron Devices*, vol. 45, no. 1, pp. 261–269, 1998. DOI: 10.1109/16.658840.

[11] K. El Sayed, E. Lyumkis, and A. Wettstein, "Modeling Statistical Variability with the Impedance Field Method A systematic comparison between the Impedance Field and the ' Atomistic ' Method," in *2012 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sep. 2012, pp. 205–208. ISBN: 9780615717562.

[12] "2013 ITRS - International Technology Roadmap for Semiconductors," 2013. [Online]. Available: http://www.itrs2.net/2013-itrs.html. [Accessed: 09-Jun-2018].

[13] M. Rau, E. Caruso, D. Lizzit, P. Palestri, D. Esseni, A. Schenk, L. Selmi, and M. Luisier, "Performance projection of III-V ultra-thin-body, FinFET, and nanowire MOSFETs for two next-generation technology nodes," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM)*, Dec. 2017, pp. 30.6.1-30.6.4. DOI: 10.1109/IEDM.2016.7838515.

[14] X. Wang, A. R. Brown, B. Cheng, and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 103–106. DOI: 10.1109/IEDM.2011.6131494.

[15] A. R. Brown, N. M. Idris, J. R. Watling, and A. Asenov, "Impact of metal gate granularity on threshold voltage variability: A full-scale three-dimensional statistical simulation study," *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1199–1201, Nov. 2010. DOI: 10.1109/LED.2010.2069080.

[16] N. Zagni, F. M. Puglisi, P. Pavan, and G. Verzellesi, "Effects of mole fraction variations and scaling on total variability in InGaAs MOSFETs," *Solid. State. Electron.*, vol. 159, no. March, pp. 135–141, Sep. 2019. DOI: 10.1016/j.sse.2019.03.048.

[17] A. R. Brown, V. Huard, and A. Asenov, "Statistical simulation of progressive NBTI degradation in a 45-nm technology pMOSFET," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2320–2323, Sep. 2010. DOI: 10.1109/TED.2010.2052694.

[18] E. R. Hsieh, S. S. Chung, C. H. Tsai, R. M. Huang, C. T. Tsai, and C. W. Liang, "New observations on the physical mechanism of Vth-variation in nanoscale CMOS devices after long term stress," in *International Reliability Physics Symposium*, 2011, p. XT.9.1-XT.9.2. DOI: 10.1109/IRPS.2011.5784610.

[19] M. Heyns, C. Adelmann, G. Brammertz, D. Brunco, M. Caymax, B. De Jaeger, A. Delabie, G. Eneman, M. Houssa, D. Lin, K. Martens, C. Merckling, M. Meuris, J. Mittard, J. Penaud, G. Pourtois, M. Scarrozza, E. Simoen, S. Sioncke, and W. E. Wang, "Ge and III/V devices for advanced CMOS," in *Proceedings of the 10th International Conference on Ultimate Integration of Silicon, ULIS 2009*, Mar. 2009, pp. 83–86. DOI: 10.1109/ULIS.2009.4897544.

[20] G. Brammertz, H. C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, "On the interface state density at In0.53 Ga0.47 As /oxide interfaces," *Appl. Phys. Lett.*, vol. 95, no. 20, p. 202109, Nov. 2009. DOI: 10.1063/1.3267104.

[21] P. Aguirre, M. Rau, and A. Schenk, "2D and 3D TCAD simulation of III-V channel FETs at the end of scaling," *Solid. State. Electron.*, vol. 159, pp. 123–128, Sep. 2019. DOI: 10.1016/j.sse.2019.03.043.

[22] L. Lucci, P. Palestri, D. Esseni, L. Bergagnini, and L. Selmi, "Multisubband Monte Carlo study of transport, quantization, and electron-gas degeneration in ultrathin SOI n-MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 5, pp. 1156–1164, May 2007. DOI: 10.1109/TED.2007.894606.

[23] G. Zerveas, E. Caruso, G. Baccarani, L. Czornomaz, N. Daix, D. Esseni, E. Gnani, A. Gnudi, R. Grassi, M. Luisier, T. Markussen, P. Osgnach, P. Palestri, A. Schenk, L. Selmi, M. Sousa, K. Stokbro, and M. Visciarelli, "Comprehensive comparison and experimental validation of band-structure calculation methods in III-V semiconductor quantum wells," *Solid. State. Electron.*, vol. 115, pp. 92–102, Jan. 2016. DOI: 10.1016/j.sse.2015.09.005.

[24] D. Esseni, P. Palestri, and L. Selmi, *Nanoscale MOS Transistors: Semi-Classical Transport and Applications*, 1st ed. Cambridge (UK): Cambridge University Press, 2011. DOI: 10.1017/CBO9780511973857.

[25] P. Osgnach, E. Caruso, D. Lizzit, P. Palestri, D. Esseni, and L. Selmi, "The impact of interface states on the mobility and drive current of In 0.53Ga 0.47As semiconductor n-MOSFETs," *Solid. State. Electron.*, vol. 108, pp. 90–96, Jun. 2015. DOI: 10.1016/j.sse.2014.12.011.

[26] A. Vardi, J. Lin, W. Lu, X. Zhao, A. Fernando-Saavedra, and J. A. Del Alamo, "A Si-Compatible Fabrication Process for Scaled Self-Aligned InGaAs FinFETs," *IEEE Trans. Semicond. Manuf.*, vol. 30, no. 4, pp. 468–474, Nov. 2017. DOI: 10.1109/TSM.2017.2753141.

[27] C. Convertino, C. B. Zota, D. Caimi, M. Sousa, and L. Czornomaz, "InGaAs FinFETs 3D Sequentially Integrated on FDSOI Si CMOS with Record Perfomance," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 1–1, Jul. 2019. DOI: 10.1109/jeds.2019.2928471.

[28] M. V. Fischetti, B. Fu, and W. G. Vandenberghe, "Theoretical study of the gate leakage current in sub-10-nm field-effect transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3862–3869, 2013. DOI: 10.1109/TED.2013.2280844.

[29] O. Penzin, G. Paasch, and L. Smith, "Nonparabolic multivalley quantum correction model for IngaAs double-gate structures," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2246–2250, Jul. 2013. DOI: 10.1109/TED.2013.2264165.

[30] S. Carapezzi, E. Caruso, A. Gnudi, P. Palestri, S. Reggiani, and E. Gnani, "TCAD Mobility Model of III-V Short-Channel Double-Gate FETs Including Ballistic Corrections," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 4882–4888, Dec. 2017. DOI: 10.1109/TED.2017.2759420.

[31] D. Lizzit, D. Esseni, P. Palestri, and L. Selmi, "Surface roughness limited mobility modeling in ultra-thin SOI and quantum well III-V MOSFETs," *Proc. IEEE Int. Electron Devices Meet.*, pp. 5.2.1-5.2.4, Dec. 2013. DOI: 10.1109/IEDM.2013.6724565.

[32] D. Lizzit, O. Badami, R. Specogna, and D. Esseni, "Improved surface-roughness scattering and mobility models for multi-gate FETs with arbitrary cross-section and biasing scheme," *J. Appl. Phys.*, vol. 121, no. 24, Jun. 2017. DOI: 10.1063/1.4986644.

[33] M. Lenzi, P. Palestri, E. Gnani, S. Reggiani, A. Gnudi, D. Esseni, L. Selmi, and G. Baccarani, "Investigation of the transport properties of silicon nanowires using deterministic and Monte Carlo approaches to the solution of the Boltzmann transport equation," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2086–2096, Aug. 2008. DOI: 10.1109/TED.2008.926230.

[34] Synopsys, "Sentaurus SDevice Manual (N-2017.09)." 2017.

[35] S. Reggiani, E. Gnani, A. Gnudi, M. Rudan, and G. Baccarani, "Low-field electron mobility model for ultrathin-body SOI and double-gate MOSFETs with extremely small silicon thicknesses," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2204–2212, Sep. 2007. DOI: 10.1109/TED.2007.902899.

[36] O. Penzin, L. Smith, A. Erlebach, M. Choi, and K. H. Lee, "Kinetic Velocity Model to Account for Ballistic Effects in the Drift-Diffusion Transport Approach," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4599–4606, Nov. 2017. DOI: 10.1109/TED.2017.2751968.

[37] N. Agrawal, H. Liu, R. Arghavani, V. Narayanan, and S. Datta, "Impact of variation in nanoscale silicon and non-silicon FinFETs and tunnel FETs on device and SRAM performance," *IEEE Trans. Electron Devices*, May 2015. DOI: 10.1109/TED.2015.2406333.

[38] D. Esseni and M. G. Pala, "Interface traps in InAs nanowire tunnel FETs and MOSFETs - Part II: Comparative analysis and trap-induced variability," *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2802–2807, 2013. DOI: 10.1109/TED.2013.2274197.

[39] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, T. Ghani, M. Giles, S. Govindaraju, R. Grover, W. Han, D. Hanken, E. Haralson, M. Haran, M. Heckscher, R. Heussner, P. Jain, R. James, R. Jhaveri, I. Jin, H. Kam, E. Karl, C. Kenyon, M. Liu, Y. Luo, R. Mehandru, S. Morarka, L. Neiberg, P. Packan, A. Paliwal, C. Parker, P. Patel, R. Patel, C. Pelto, L. Pipes, P. Plekhanov, M. Prince, S. Rajamani, J. Sandford, B. Sell, S. Sivakumar, P. Smith, B. Song, K. Tone, T. Troeger, J. Wiedemer, M. Yang, and K. Zhang, "A 14nm Logic Technology Featuring 2 nd - Generation FinFET Interconnects , Self-Aligned Double Patterning and a 0.0588 μm2 SRAM cell size," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM)*, Dec. 2014, pp. 3.7.1-3.7.3. DOI: 10.1109/IEDM.2014.7046976.