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Orientation-Engineered $PtTe_2$ Schottky FETs: Quantum Transport Insights for Dopant-Free Advanced Technology Nodes

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ABSTRACT

As transistor scaling pushes beyond the 5 nm node, conventional silicon-based field effect transistors (FETs) face critical challenges including short-channel effects, high contact resistance, and power dissipation. This work presents a comprehensive quantum transport simulation study of monomaterial Schottky-junction FETs based on monolayer $PtTe_2$, leveraging its unique thickness-dependent electronic properties – where the semimetallic bilayer serves as the source/drain and the semiconducting monolayer forms the channel. First-principles simulations reveal that the device architecture enables efficient, doping-free carrier injection, sharp electrostatic switching, and directional performance tunability. The results show that transport along the Γ–M orientation achieves superior ON-state current, subthreshold swing (as low as 75 mV/dec), and suppressed OFF-state current, with OFF-currents and subthreshold swings comparable to IRDS-style low-power projections for sub-10 nm logic nodes. Projected local density of states (PLDoS) and energy-resolved current spectra further reveal distinct transport regimes and efficient Schottky barrier modulation. Compared to contemporary 2D-channel transistors, the monomaterial $PtTe_2$ Schottky FET offers a balanced trade-off between scalability, simplicity, carrier injection, and low-power operation. These findings highlight monolayer $PtTe_2$ as a promising candidate for ultra-scaled logic applications and demonstrate the strategic advantages of monomaterial, orientation-engineered architectures for beyond-CMOS nanoelectronics.

1 | Introduction

Continuous miniaturization of FETs toward sub-5 nm nodes highlights critical challenges, such as worsening short-channel effects and electrostatic degradation, which demand advanced contact engineering, channel orientation strategies, and device architectures like gate-all-around or nanosheets [1–3]. Traditional silicon-based transistors are approaching fundamental limits due to short-channel effects (SCEs), where direct source-to-drain tunnelling, increased OFF-state currents, and excessive power dissipation become major obstacles [4, 5]. These effects significantly impact the performance of modern integrated circuits, necessitating the exploration of alternative materials with superior electrostatic control, lower contact resistance, and enhanced transport properties [6, 7].

Among the materials explored for next-generation transistors, two-dimensional (2D) transition metal dichalcogenides (TMDs) have emerged as strong contenders. Their atomically thin structure provides excellent gate control and scalability, mitigating SCEs that typically degrade silicon-based devices [8–10]. Unlike bulk materials, TMDs exhibit tunable electronic properties,

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ranging from semimetals to semiconductors, depending on their thickness and external stimuli. This tunability makes them highly versatile for future electronic and optoelectronic applications [11–15]. While monolayer TMDs such as MoS_2, WSe_2, and SnS_2 have demonstrated promising transistor performance at sub-10 nm dimensions, they often suffer from high contact resistance and limited band alignment flexibility, which hinder their full integration into advanced semiconductor technologies [6, 8, 12, 16–19]. Moreover, recent high-throughput screening has shown that certain 2D semiconductors with isolated-band features can exhibit super-exponential suppression of OFF-state leakage and sub-thermionic subthreshold swing, further highlighting the promise of atomically thin channels for energy-efficient switching at scaled nodes [20].

$PtTe_2$ stands out among 2D TMDs due to its unique thickness-dependent electronic characteristics. In its bulk form, $PtTe_2$ behaves as a semimetal, allowing for low-resistance metallic contacts. However, when reduced to a monolayer, it transitions into a semiconductor with a bandgap comparable to conventional silicon-based materials [14, 21–23]. This natural transition from semimetal to semiconductor within the same material offers a promising avenue for monomaterial Schottky-junction FETs. Unlike conventional transistors, which rely on heavily doped source/drain contacts, monomaterial Schottky transistors leverage a single material system where the source, drain, and channel regions exist in different electronic states, thereby eliminating the need for extrinsic doping while maintaining excellent transport properties [24–27].

Beyond $PtTe_2$, other FETs such as SnS_2 and InSe have been extensively studied for their quantum transport performance. SnS_2-based FETs have demonstrated an on-state current (I_{ON}) exceeding 3400 μA/μm at 5.5 nm gate lengths, surpassing International Roadmap for Devices and Systems (IRDS) standards [28, 29]. Similarly, ballistic InSe-based transistors have maintained high-performance characteristics even at gate lengths as short as 2 nm, underscoring the feasibility of monolayer FETs for next-generation technology nodes [30]. These insights reinforce the need to explore the transport properties of $PtTe_2$-based Schottky FETs, particularly in the ballistic transport regime. Given its anisotropic electronic band structure, it is critical to investigate the impact of channel crystallographic orientation (Γ–M vs. Γ–K) on device performance, particularly under varying bias conditions.

This work employs ab-initio quantum transport simulations to investigate the performance of monomaterial $PtTe_2$ Schottky FETs, with a focus on ultra-scaled device applications. Specifically, we model bilayer $PtTe_2$ semimetallic contacts interfacing with a monolayer semiconductor channel and analyze charge transport using the nonequilibrium Green's function (NEGF) formalism. By systematically examining the impact of two high-symmetry orientations and gate length scaling, we evaluate the role of monomaterial-based Schottky junctions in enhancing carrier injection, minimizing contact resistance, and suppressing short-channel effects. We benchmark device performance against industry targets for both high-performance (HP) and low-power (LP) applications as defined by the IRDS. For clarity, we distinguish that the International Technology Roadmap for Semiconductors (ITRS) historically defined node scaling and dimensional targets up to 2016, while the IRDS provides updated benchmarks focused on performance metrics such as I_{ON}, I_{OFF}, and energy efficiency for emerging device technologies [31, 32].

2 | Computational Methodology

First-principles electronic structure calculations were performed based on fully relativistic Density Functional Theory (DFT) within the GGA, explicitly including spin–orbit coupling (SOC), as implemented in QuantumATK [33]. Norm-conserving pseudopotentials for the exchange correlation potential were considered. OpenMx numerical atomic orbital basis sets of *s2p2d2f1* were considered for both Pt and Te atoms [34]. Brillouin-zone integrations were performed over a grid of k points with a density of $\sim 9 \times k$ points per angstrom using the Monkhorst-Pack scheme [35], and the real-space quantities were calculated with an energy cutoff of 250 Rydberg. Structural optimization was performed by minimizing the total energy with respect to the atomic positions until the maximum force component became less than 0.03 eV/Å. We have included van-der-Waals (vdW) interactions for bilayer $PtTe_2$ structures by adding a nonlocal vdW term to the local and semi-local exchange correlation functionals utilizing Grimme's dispersion correction [36].

To evaluate charge transport, we performed atomistic quantum transport simulations using the NEGF formalism. The device consists of bilayer $PtTe_2$ source/drain contacts and a monolayer $PtTe_2$ semiconductor channel, forming a monomaterial Schottky junction. DFT combined with NEGF framework enables the modelling of realistic open systems, allowing for fully self-consistent calculations of coherent transport properties. For the quantum transport calculations, a dense discretization corresponding to approximately 975 and 635 sampling points along the transport (z) direction was employed for the longer and shorter channels, respectively, in the Green's function calculations, to ensure convergence of the density matrix and current. The energy integration required to obtain the density matrix within the NEGF framework was performed through a complex contour integration scheme, which includes integral over equilibrium and non-equilibrium states.

In the device transfer characteristics calculations, the electrode conditions are achieved by holding the source and drain regions at thermal equilibrium described by Fermi-Dirac distributions at T = 300 K, and by considering chemical potential difference $\mu_{DS} = qV_{DS}$ for the drain-source bias. Upon obtaining the electron transmission, the drain-source current (I_{DS}) is calculated using the Landauer–Büttiker formula [37]:

$$I_{DS} = \int i(E)\, dE,$$
$$i(E) = \frac{e}{h} T(E, V_{DS}, V_{GS}) [f_S(E) - f_D(E)]$$

where E, e, and h are energy, electron charge, and Planck's constant, respectively. T is transmission, and $f_S(E)$ and $f_D(E)$ are the Fermi-Dirac distribution functions at the source and drain electrodes, respectively. All simulated drain currents (I_{DS}) are reported normalized per device width, consistent with standard practice for 2D-device simulations.

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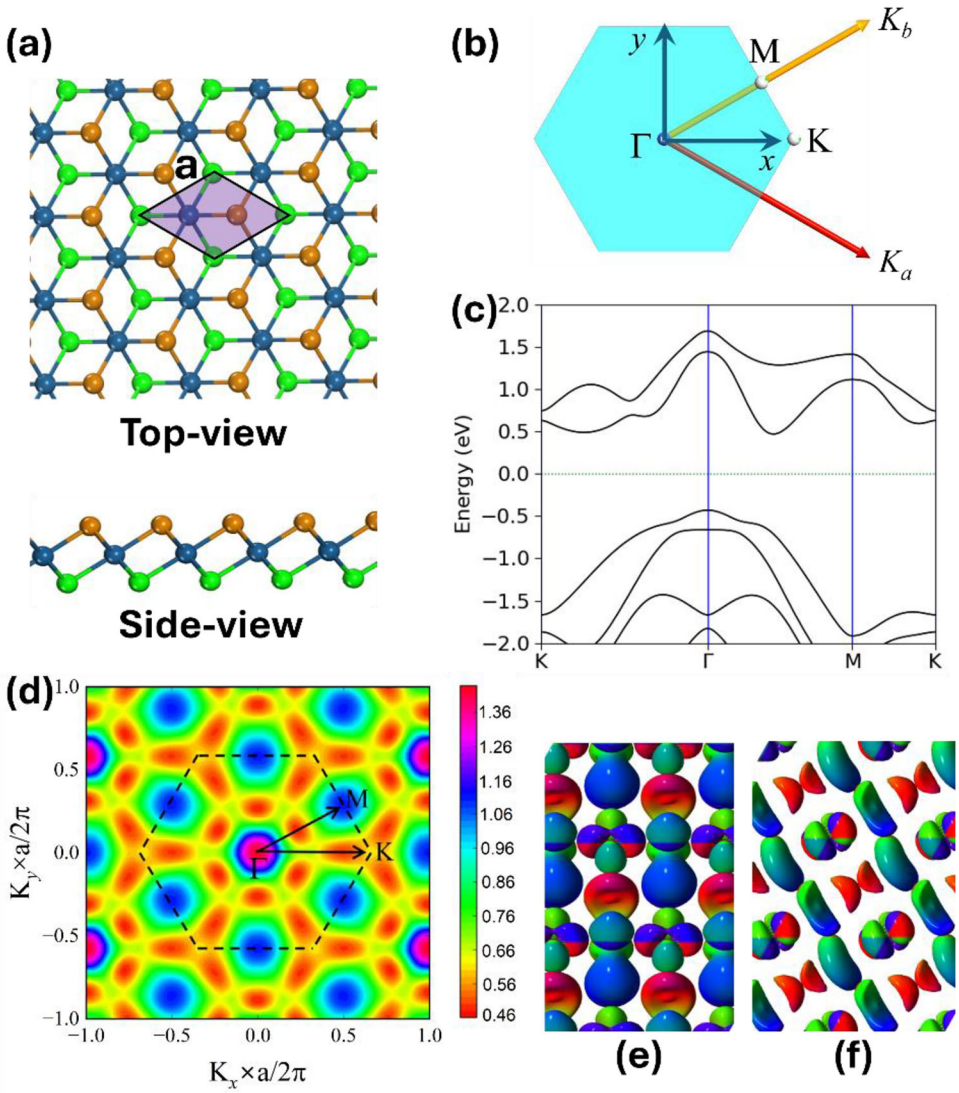


FIGURE 1 | Atomic configuration and electronic structure of monolayer $PtTe_2$. (a) Top and side views of the 1T-$PtTe_2$ monolayer structure with the lattice vector a ≈4 Å highlighted by the shaded region. (b) Wigner-Seitz primitive cell (first Brillouin zone) of the hexagonal unit-cell, showing the high symmetry points Γ, M, and K. (c) Electronic band structure of monolayer $PtTe_2$ exhibiting an indirect bandgap with the CBM located along the Γ–M direction. (d) Energy contour map of the CBM across the first Brillouin zone; high-symmetry points and valley directions (Γ–M and Γ–K) are indicated. Bloch wavefunction at the CBM along the (e) Γ–M, showing out-of-plane hybridization, and (f) Γ–K, revealing in-plane orbital character.

3 | Results and Discussion

3.1 | Electronic Structure

Monolayer $PtTe_2$ crystallizes in a 1T-phase hexagonal structure, where a layer of Pt atoms is sandwiched between two layers of Te atoms in an octahedral coordination, as shown in Figure 1a. This layered structure exhibits strong in-plane covalent bonding and weak interlayer van der Waals interactions, enabling thickness-dependent electronic properties. Notably, $PtTe_2$ undergoes a transition from semimetallic behavior in the bulk and few-layer form to a semiconducting state in the monolayer limit, which is central to the monomaterial Schottky junction concept explored in this work. The corresponding hexagonal Brillouin zone, shown in Figure 1b, is characterized by high-symmetry points Γ, M, and K, which also define the principal transport directions investigated in this study.

The electronic band structure of monolayer $PtTe_2$, calculated using DFT as detailed in the Methods section, is shown in Figure 1c. The material exhibits a semiconducting nature with an indirect bandgap, where the conduction band minimum (CBM) is located along the Γ–M direction. Figure 1d shows a 2D energy contour map of the CBM across the first Brillouin zone of the hexagonal lattice. The dashed hexagon denotes the zone boundary, and the high-symmetry points Γ, M, and K are indicated. The sixfold symmetry of the Brillouin zone results in six equivalent CBM valleys oriented along the Γ–M directions. The band structures of bilayer and trilayer $PtTe_2$ (Figure S1) confirms the semimetallic nature of thicker layers, consistent with prior theoretical and experimental reports [14].

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The CBM valleys exhibit anisotropic effective masses, extracted as $m_L = 0.35 \times m_0$ and $m_T = 0.15 \times m_0$ for the longitudinal and transverse directions, respectively, where m_0 is the free electron mass. These values indicate relatively low transport mass along the valley axis, which is advantageous for high carrier mobility. In addition to the primary CBM valleys, a secondary conduction valley emerges along the Γ–K direction, near the K-point, approximately 20 meV above the CBM. This valley displays a more pronounced mass anisotropy, with $m_L = 1.2 \times m_0$ and $m_T = 0.11 \times m_0$, respectively. Such pronounced anisotropy could influence charge transport, as further examined in the $PtTe_2$-based FET performance analysis section.

Figure 1e,f illustrates the Bloch wavefunctions corresponding to the conduction band edge at the Γ–M and Γ–K directions, respectively. The wavefunction in Figure 1e shows significant out-of-plane charge density distribution, highlighting hybridization between Pt *d*-orbitals and Te *p*-orbitals. In contrast, Figure 1f shows a more delocalized in-plane character for the Γ–K valley, reflecting a shift in orbital composition to in-plane *d*-orbitals with reduced out-of-plane overlap.

3.2 | Device Configurations and Performance Metrics

To investigate the device-level impact of these electronic properties, Figure 2a,b depicts atomic models of monolayer $PtTe_2$ FETs oriented along the Γ–M (Ori 1) and Γ–K (Ori 2) directions, respectively. The device architecture employs bilayer $PtTe_2$ – known to exhibit semimetallic behavior in its bulk-like form – as source and drain contacts, while a monolayer $PtTe_2$ channel provides a semiconducting transport path. This monomaterial design leverages the intrinsic electronic phase transition between bilayer and monolayer $PtTe_2$ to form a Schottky junction without external doping. A double-gate configuration, featuring 1.5 nm HfO_2 as both the top and bottom gate dielectrics and symmetric underlap (U) regions of 1 nm, is considered. The chosen underlap length provides a reasonable trade-off between suppressing direct source-to-drain tunnelling and limiting series resistance, thereby maintaining efficient carrier injection in ultra-scaled devices. All simulated devices employ the same underlap length to ensure a consistent and physically meaningful comparison. Additionally, the role of contact thickness on charge injection is explored for the Γ–M-oriented device (Ori 1), offering insight into how electrode thickness influences interfacial barrier profiles and carrier transmission.

Figure 2 also presents the transfer characteristics (I_{DS}–V_{GS}) of the monolayer $PtTe_2$-based Schottky FETs, modelled using the NEGF formalism, as described in the Methods Section. As noted, the two device orientations, i.e., Ori 1 (Γ–M), and Ori 2 (Γ–K), are evaluated at two representative bias conditions: V_{DS} = 0.6 V (high-bias condition) and V_{DS} = 0.1 V (low-bias condition often used to analyse low-power operation and leakage behavior). These orientations reflect the anisotropic transport properties of $PtTe_2$, as established in Figure 1. All current values are normalized per device width, and are compared qualitatively with IRDS-style ON/OFF current targets. The devices employ a double-gate structure with bilayer $PtTe_2$ as the source/drain (2L S/D) contact. A variant with 3-layer, i.e., 3L S/D, is also included to assess the impact of contact thickness.

In Figure 2c, for a gate length of 2 nm under HP conditions, Ori 1 exhibits a subthreshold swing (SS) of 136 mV/dec, significantly better than 204 mV/dec for Ori 2. The ON-current of Ori 1 reaches 131 μA/μm, with an OFF-current of 0.12 μA/μm, yielding an ON/OFF ratio of $\sim 1.1 \times 10^3$. In contrast, Ori 2 achieves a higher ON-current of 402 μA/μm but suffers from a substantially higher OFF-current of 3.3 μA/μm, resulting in a reduced ON/OFF ratio of $\sim 1.2 \times 10^2$. These results highlight the electrostatic and transport benefits of the Γ–M orientation, attributed to its lighter transport effective mass and out-of-plane orbital hybridization, consistent with the CBM characteristics discussed in Figure 1. For the 3L S/D configuration, the ON-current of Ori 1 improves to ~830 μA/μm, benefiting from increased density of states and enhanced carrier injection. However, this comes at the cost of increased OFF-current (~1.85 μA/μm), a degraded SS of 210 mV/dec, and an ON/OFF ratio of $\sim 4.45 \times 10^3$. This degradation is not solely due to contact-induced screening but is primarily driven by enhanced SCEs at 2 nm gate length. The thicker S/D regions increase the source/drain electric field penetration into the channel, reducing the gate's electrostatic control and amplifying drain-induced barrier lowering (DIBL). This weakens the channel potential barrier in the OFF state, leading to higher OFF-current and compromised subthreshold behavior – characteristic of ultra-scaled devices with poor electrostatic integrity [38]. Even within the ballistic NEGF-DFT framework, the ON-current is therefore limited primarily by the semimetallic $PtTe_2$ contact density of states and band dispersion rather than by intrinsic scattering in the monolayer channel. This contact-limited injection is a key feature of the monomaterial architecture and explains why ON-currents remain below those of some 2D FETs that employ optimized 3D metal contacts.

Figure 2d illustrates the transfer characteristics under LP bias (V_{DS} = 0.1 V). Ori 1 continues to outperform Ori 2, with SS values of 116 and 145 mV/dec, respectively. The ON/OFF ratio of Ori 1 reaches $\sim 5.45 \times 10^5$ (ON-current: 376 μA/μm, OFF-current: 6.86×10^{-4} μA/μm), while Ori 2 achieves an ON/OFF of $\sim 5 \times 10^4$ (ON-current: 308 μA/μm, OFF-current: 6×10^{-3} μA/μm). The 3L S/D variant enhances the ON-current to ~816 μA/μm, but again exhibits a degraded SS of 167 mV/dec, driven by increased OFF-current and compromised electrostatics, mirroring the HP regime trade-off.

To evaluate gate length scaling, Figure 2e compares Ori 1 and Ori 2 devices at 7 nm gate length under LP conditions. The longer channel significantly suppresses SCEs, resulting in improved SS values of 75 mV/dec (Ori 1) and 97 mV/dec (Ori 2). Ori 1 achieves an ON-current of ~334 μA/μm and an OFF-current of 6.9×10^{-7} μA /μm, yielding an ON/OFF ratio of $\sim 4.8 \times 10^8$. Ori 2 reaches an ON-current of ~181 μA/μm and an OFF-current of 7.4×10^{-4} μA/μm, corresponding to an ON/OFF ratio of $\sim 2.4 \times 10^5$. These results confirm the performance advantage of the Γ–M orientation in $PtTe_2$-based devices and the critical role of electrostatic gate control at sub-10 nm nodes.

It should be noted that the gate lengths considered in this study (L_G = 2 nm and 7 nm) are selected as representative limits to

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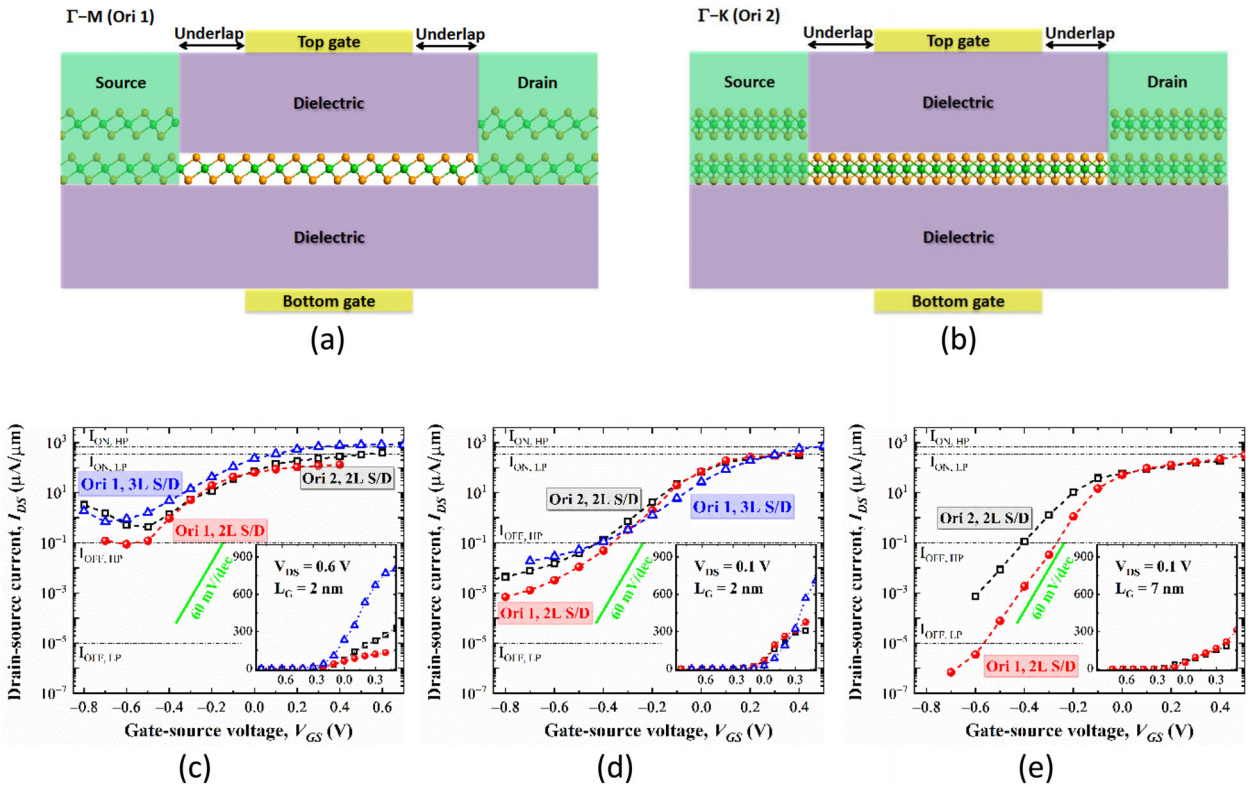


FIGURE 2 | Transfer characteristics of monolayer $PtTe_2$ FETs with different channel orientations and contact configurations. Device schematics of monolayer $PtTe_2$ FETs with bilayer $PtTe_2$ source/drain contacts oriented along (a) Γ–M (Ori 1), and (b) Γ–K (Ori 2) directions, respectively, employing a double-gate architecture with underlap regions. (c) I_{DS}–V_{GS} under high-performance (HP) bias (V_{DS} = 0.6 V) for 2 nm gate length. (d) Same for low-power (LP) bias (V_{DS} = 0.1 V). (e) Transfer characteristics at longer gate length L_G = 7 nm under LP bias. The influence of crystallographic orientation (Ori 1: Γ–M, Ori 2: Γ–K) and S/D contact thickness (2L vs. 3L) on device performance is shown. Dashed lines denote IRDS ON- and OFF-current targets for HP and LP applications. The reference SS for thermionic FET operation, i.e., 60 mV/dec, is indicated in each panel. The insets show the same I_{DS}–V_{GS} in linear-scale.

capture the transition between extreme short-channel behavior and improved electrostatic control in longer channels. A systematic exploration of intermediate gate lengths and additional geometrical parameters, such as underlap length variation, is beyond the scope of the present work. Such studies would require a large number of computationally intensive simulations within the fully self-consistent NEGF-DFT framework, particularly due to the inclusion of spin–orbit coupling and dense k-point sampling. These aspects are therefore left for future investigation.

It should also be noted that the underlap length is kept fixed at 1 nm across all simulated devices to ensure a consistent basis for comparison. While variations in underlap length can influence the trade-off between leakage suppression and series resistance, the chosen value provides a reasonable balance between suppressing direct source-to-drain tunnelling and maintaining efficient carrier injection in ultra-scaled devices. A systematic optimization of this parameter is beyond the scope of the present study and is left for future investigation.

Subthreshold swing (SS) for each configuration was extracted from the log-scale I_{DS}–V_{GS} characteristics using the standard definition:

$$SS = \left(\frac{d\left(log_{10}\left(I_{DS}\right)\right)}{dV_{GS}} \right)^{-1}$$

evaluated over the steepest portion of the subthreshold region, spanning one decade of current. The 60 mV/dec reference lines in Figure 2c–e indicates the ideal thermionic limit and serve as a visual benchmark. The approximate output characteristics (I_{DS}–V_{DS} curves at several gate voltages) obtained using the Landauer–Büttiker linear-response approximation are provided in (Figure S2), based on the converged NEGF solutions.

3.3 | Carrier Transport Mechanism

To gain deeper insight into the carrier injection mechanisms and electrostatic behavior of monolayer $PtTe_2$ Schottky FETs, Figure 3 presents the projected local density of states (PLDoS) and energy-resolved current spectra under different gate lengths, biasing conditions, and crystallographic orientations, with the positions of the source, drain, and underlap regions explicitly indicated along the transport direction. These simulations are performed for both the Γ–M (Ori 1) and Γ–K (Ori 2) directions, with the top row in each subfigure corresponding to Ori 1 and the bottom to Ori 2. For all cases, the left column illustrates the OFF-state, while the right column represents the ON-state. The current spectra decompose the total current into tunnelling (blue) and thermionic (red) components, allowing direct visualization of the dominant conduction mechanisms.

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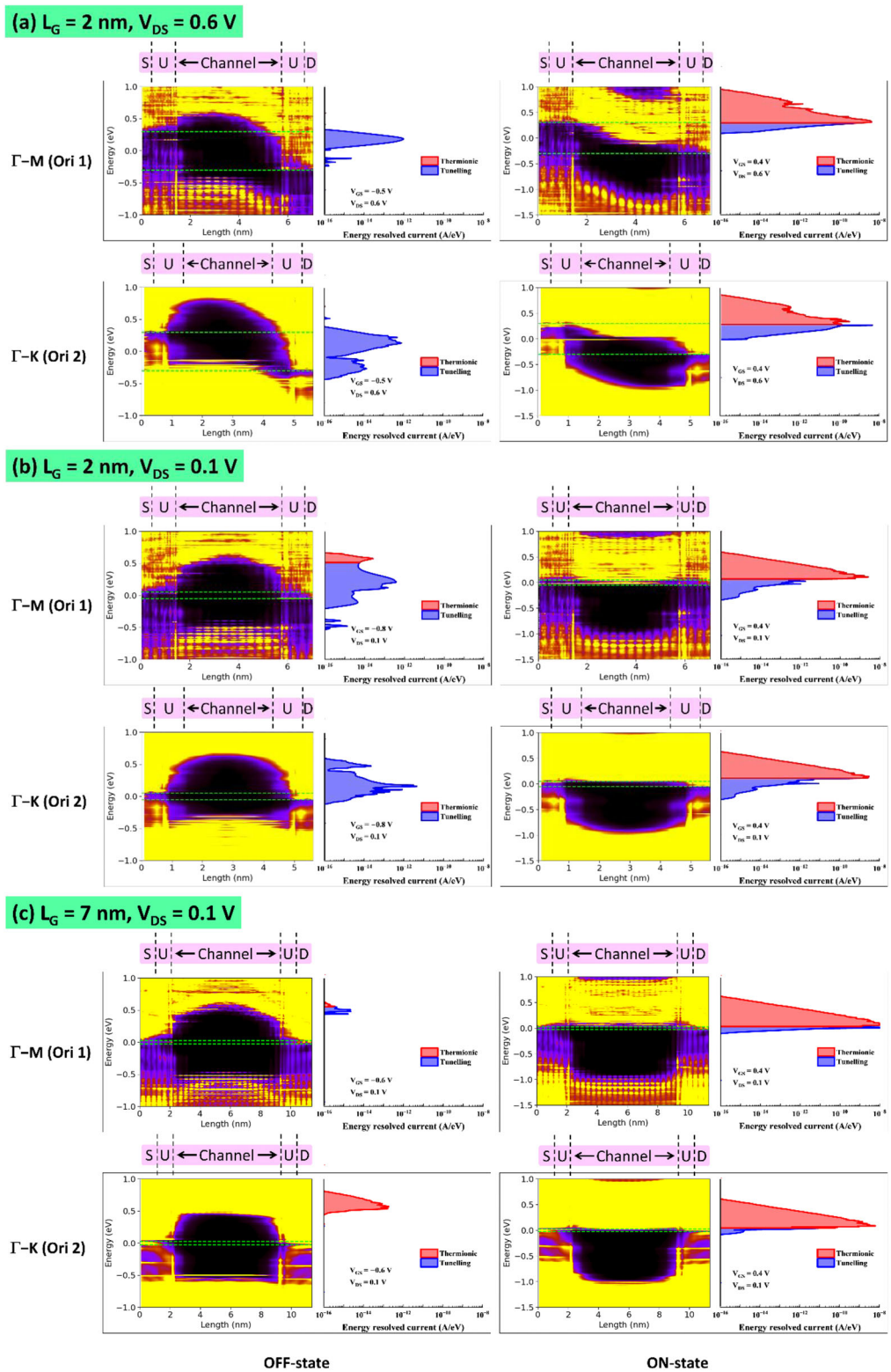


FIGURE 3 | Quantum transport mechanisms and carrier injection in $PtTe_2$ Schottky FETs. (a) Short-channel device ($L_G = 2$ nm) under HP operation ($V_{DS} = 0.6$ V). (b) Short-channel device under LP condition ($V_{DS} = 0.1$ V). (c) Long-channel device ($L_G = 7$ nm) under LP operation. For each subpanel, the top row corresponds to transport along the Γ–M direction (Ori 1), and the bottom row to the Γ–K direction (Ori 2). Within each subpanel, the left and right columns represent the OFF-state and ON-state, respectively. The PLDoS maps (left in each pair) illustrate the spatial and energy distribution of accessible states, where darker colors indicate low density of states and brighter colors indicate high density of states. The green dashed lines denote the bias-induced transport window (qV_{DS}), defined by the difference between the source and drain electrochemical potentials. The corresponding energy-resolved current spectra (right in each pair) decompose the total current into tunnelling (blue) and thermionic (red) components, revealing how electrostatics and orientation affect carrier injection and transport mechanisms. The positions of the Source (S), Channel, Drain (D), and Underlap (U) regions are explicitly indicated along the transport direction in the PLDoS plots.

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Figure 3a illustrates the PLDoS and energy-resolved carrier transport for the short-channel device (L_G = 2 nm) operating under HP bias condition. In the OFF-state (V_{GS} = −0.5 V), both transport orientations exhibit a pronounced carrier injection barrier, effectively suppressing conduction. For the Γ–M orientation, the injection barrier height is ∼0.2 eV, resulting in limited tunnelling leakage and a sharper subthreshold transition. In contrast, the Γ–K orientation, although exhibiting an increased barrier of ∼0.45 eV, displays a broader tunnelling spectrum and smoother potential slope. This suggests, despite the higher barrier, a higher susceptibility to band-to-band tunnelling leakage and stronger DIBL effects, as the PLDoS reveals extended tunnelling channels bridging source and drain. As the device transitions to the ON-state (V_{GS} = 0.4 V), the conduction band edge approaches the source Fermi level, lowering the barrier and enabling thermionic-dominated transport. The Γ–M channel achieves a higher energy-resolved current density compared to the Γ–K channel, consistent with the improved ON-state drive current observed in Figure 2c.

In the short-channel device under LP bias condition (Figure 3b), in the OFF-state (V_{GS} = −0.8 V), both transport orientations exhibit a substantial carrier injection barrier, effectively restricting thermionic conduction. For the Γ–M orientation, the injection barrier height is ∼0.44 eV, resulting in only a small thermionic over-the-barrier leakage component. This behavior correlates with the lower OFF-state current and improved subthreshold swing observed in Figure 2b. In contrast, the Γ–K orientation displays a higher tunnelling spectrum and a smoother potential slope near the source-channel interface. Due to a higher injection barrier of ∼0.53 eV, the leakage current is predominantly tunnelling-driven. Upon switching to the ON-state (V_{GS} = 0.4 V), the barrier is effectively suppressed in both orientations as the CBM approaches the source Fermi level. Transport becomes thermionic-dominated, improving carrier injection efficiency.

The long-channel device (L_G = 7 nm) under LP bias operation in Figure 3c demonstrates the impact of scaling on electrostatic integrity. In the OFF-state (V_{GS} = −0.6 V), both transport orientations show strong suppression of tunnelling leakage, with the PLDoS indicating a well-preserved injection barrier. For the Γ–M orientation, the barrier height remains high at ∼0.47 eV, resulting in negligible tunnelling contributions to the leakage current. This demonstrates excellent electrostatic control and minimal DIBL. The Γ–K orientation, while exhibiting a lower barrier of ∼0.37 eV, also experiences a significant reduction in tunnelling compared to its short-channel counterpart. Leakage is dominated by thermionic conduction near the band edge, confirming that increased channel length effectively mitigates short-channel electrostatic degradation. In the ON-state (V_{GS} = 0.4 V), the potential profile flattens for both orientations, enabling efficient thermionic transport. The Γ–M device sustains a higher current spectral density across the energy window, reinforcing its superior ON-current and subthreshold slope, consistent with the transfer characteristics observed in Figure 2.

These findings highlight the superior transport properties of the Γ–M orientation, particularly in ultra-scaled regimes, where aligning transport along this direction enables simultaneous suppression of OFF-state leakage and enhancement of drive current. This performance advantage, observed in the transfer characteristics (Figure 2), stems from the favourable electronic band curvature and orbital hybridization of Γ–M transport (Figure 1), which yield sharper energy filtering, stronger gate control, and higher carrier injection efficiency (Figure 3). The combined effects of reduced tunnelling, enhanced resilience to DIBL, and improved thermionic transport establish Ori 1 as a more energy-efficient option for future sub-5 nm logic devices compared to Ori 2. It is noted that all transport simulations are performed within a coherent, ballistic NEGF-DFT framework without explicit phonon, impurity, or intervalley scattering. As such, the reported ON-currents represent an upper bound set by the realistic band structure and electrostatics of $PtTe_2$, and additional scattering mechanisms in experimental devices are expected to further reduce the drive current. Incorporating electron-phonon and intervalley scattering into the transport framework is an important direction for future work.

3.4 | Benchmarking $PtTe_2$ FETs against State-of-the-Art 2D Devices

The performance of the proposed $PtTe_2$ Schottky FETs, as shown in Figure 2, demonstrates promising characteristics across a range of operating biases representative of HP and LP logic regimes in a qualitative sense, consistent with IRDS-style performance targets - i.e., higher V_{DS} and I_{ON} for HP conditions and lower V_{DS} and I_{OFF} for LP conditions. To contextualize these results, we benchmark them against a diverse set of monolayer and few-layer 2D FETs reported in literature. It is important to note that the comparison includes both experimentally fabricated devices and theoretical simulation studies, and is intended to provide a qualitative overview of performance trends rather than a direct one-to-one benchmarking. In particular, the results obtained in this work are based on ballistic NEGF-DFT simulations and therefore represent an upper performance limit, whereas experimental devices are subject to additional scattering mechanisms, contact resistance, and fabrication-related non-idealities. A comparative summary of ON-state current (I_{ON}), OFF-state current (I_{OFF}), ON/OFF ratio, and subthreshold swing (SS) of dopant-free 2D transistors is presented in Table 1.

Recent advances in monolayer MoS_2 transistors have established key milestones in sub-10 nm 2D device scaling. MoS_2 FETs with channel lengths around 7–8 nm [39–41] demonstrate excellent gate control, achieving ON/OFF ratios up to 10^6–10^7 and subthreshold swings near 120–140 mV/dec using high-κ dielectrics such as HfO_2. Further scaling toward the ultimate limit has been experimentally realized with a 1 nm gate-length MoS_2 device [42], in which a single-walled carbon-nanotube gate electrode enabled a near-ideal SS ≈ 65 mV/dec and ON/OFF ≈ 10^6. Complementary studies on self-aligned top-gated MoS_2 transistors [43] reported I_{ON} > 400 μA/μm and highlighted the onset of quasi-ballistic transport at L ≈ 10 nm, marking the transition from diffusive to ballistic conduction in monolayer channels. Moreover, MoS_2 devices with graphene source/drain contacts [44] achieved sub-10 nm operation with ON/OFF ratios above 10^5, revealing the critical role of Schottky-barrier modulation and contact engineering at this extreme scale.

Beyond MoS_2, other 2D semiconducting materials such as SnS_2, BP, InSe, GaSe, and WTe_2 have also demonstrated strong

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TABLE 1 | Performance benchmarking of $PtTe_2$ FETs against recent dopant-free 2D transistor technologies. Comparison of key device performance metrics, i.e., ON-state current (I_{ON}), OFF-state current (I_{OFF}), ON/OFF current ratio, and subthreshold swing (SS), for the proposed $PtTe_2$ monomaterial Schottky FETs and a representative selection of 2D FETs from literature. The data include both theoretical (simulation-based) and experimental results; these are presented for qualitative comparison only and should not be interpreted as a direct one-to-one performance benchmark. All simulated current values are normalized per device width; devices are not compared at identical I_{OFF}; the table is meant to illustrate trends and trade-offs rather than to rank record performance. Gr: Graphene; DG: double gate; EXP: experimental; SIM: simulation. The gate lengths of the $PtTe_2$ devices reported in this study ($L_G = 2$ and 7 nm) lie beyond current industrial technology nodes [49] and should be viewed as exploratory device-level studies rather than direct mappings onto specific commercial nodes.

Material	L_G or L_{ch} (nm)	V_{DS} (V)	I_{ON} (μA/μm)	ON/OFF ratio	Dielectric material /thickness (nm)	SS (mV/dec)	Type of report	Refs.
MoS_2	L_{ch}: 7.5	1	45	$<10^7$	HfO_2/10	120	EXP	[39]
MoS_2	L_{ch}: 7.5	1	250	10^7	HfO_2/10	120	EXP	[40]
MoS_2	$L_{ch} < 10$	1	2.7	10^6	HfO_2/6	140	EXP	[41]
MoS_2	L_g: 1	1	10	5×10^6	ZrO_2/5.8	65	EXP	[42]
MoS_2	L_{ch}: 10	0.1	1.5	10^3	AlO_2/5-6	250	EXP	[43]
MoS_2 with Gr S/D	L_{ch}: 8	0.1	8.1	1.5×10^6	SiO_2/300	7500	EXP	[44]
MoS_2 with Gr S/D	L_{ch}: 3.8	0.1	9	5×10^5	SiO_2/300	11500	EXP	[44]
SnS_2	—	2	—	2×10^7	hBN/25	239	EXP	[45]
BP	—	1	—	10^5	SiO_2/300	9000	EXP	[46]
InSe	L_{ch}: 10	0.4	1350	$>10^7$	HfO_2/2.6	75	EXP	[30]
GaSe	L_g: 3	0.64	1201	1.2×10^4	HfO_2/0.41	120.7	SIM	[47]
DG WTe_2 with VTe_2 S/D	L_g: 3	0.64	103.13	10^3	-/0.41	168	SIM	[48]
$PtTe_2$ (Ori 1)	L_g: 2	0.6	131	1.1×10^3	HfO_2/1.5	136		
$PtTe_2$ (Ori 2)	L_g: 2	0.6	402	1.2×10^2	HfO_2/1.5	204		
$PtTe_2$ (Ori 1, 3L S/D)	L_g: 2	0.6	830	4.45×10^3	HfO_2/1.5	210		
$PtTe_2$ (Ori 1)	L_g: 2	0.1	376	5.45×10^5	HfO_2/1.5	116		
$PtTe_2$ (Ori 2)	L_g: 2	0.1	308	5×10^4	HfO_2/1.5	145	SIM	This work
$PtTe_2$ (Ori 1, 3L S/D)	L_g: 2	0.1	816	4.4×10^4	HfO_2/1.5	167		
$PtTe_2$ (Ori 1)	L_g: 7	0.1	334	4.8×10^8	HfO_2/1.5	75		
$PtTe_2$ (Ori 2)	L_g: 7	0.1	181	2.4×10^5	HfO_2/1.5	97		

electrostatic control and promising current drives across various architectures [30, 45–48]. SnS_2 devices [45] achieve ON/OFF $\approx 10^7$ and SS $\approx$ 239 mV/dec, while BP transistors [46] display ON/OFF $> 10^5$ though limited by environmental stability, and tri-layer InSe [30] achieves SS $\approx$ 75 mV/dec through Ohmic-contact engineering. Simulated 3 nm-thick GaSe FETs [47] deliver $I_{ON} > 1200$ μA/μm at $V_{DS} = 0.64$ V, while double-gate WTe_2 devices [48] with metallic VTe_2 contacts satisfy projected IRDS high-performance benchmarks. Collectively, these results highlight the rapid progress of dopant-free 2D FETs in approaching the ultimate scaling and performance frontiers.

In comparison, our $PtTe_2$ Schottky FETs operate with a monomaterial, dopant-free design, eliminating the need for heterojunction interfaces or external doping. Their performance aligns well with recent trends and provides directional tuning of transport behavior, a unique advantage offered by the anisotropic electronic structure of $PtTe_2$. This positions $PtTe_2$ as a compelling candidate for ultra-scaled logic applications.

4 | Conclusion

This study demonstrates the feasibility and potential of monomaterial $PtTe_2$-based Schottky-junction FETs for future ultra-scaled beyond CMOS technologies. Using fully quantum mechanical NEGF simulations, we explored devices comprising semimetallic bilayer $PtTe_2$ contacts interfaced with a semiconducting monolayer channel. The unique phase transition across thicknesses enables self-aligned, doping-free junctions with efficient carrier injection and strong gate control. We find that device orientation plays a critical role: channels aligned along the Γ–M direction consistently outperform those along Γ–K, due to favorable effective mass anisotropy and orbital hybridization. Energy-resolved current and PLDoS analysis confirm reduced Schottky barrier resistance and minimal leakage under OFF-state biasing. While the 2 nm device provides physical insight into extreme scaling, its performance remains limited by short-channel effects, whereas the 7 nm variant achieves OFF-currents and subthreshold swings comparable to IRDS-style low-power projections. Compared to other 2D materials such as $SnSe_2$, and BP, $PtTe_2$ delivers a unique

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combination of monomaterial simplicity, scaling potential, and environmental stability. Challenges remain, including the scalable synthesis of uniform few-layer $PtTe_2$, long-term material stability, and compatibility with CMOS processing environments. Addressing these will be essential to experimentally realize the theoretical potential of $PtTe_2$ monomaterial Schottky FETs for next-generation nanoelectronics.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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